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DIP-COATING PROCESS

Silicon Sheet Growth Development for the Large-Area Silicon Sheet Task of the Low-Cost Silicon Solar Array Project

Quarterly Report No. 7

by

J.D. Zook, J.D. Heaps
R.B. Maciolek, B. Koepke,
C.D. Butter and S.B. Schuldt

Period Covered 9/20/77-12/27/77

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Bloomington, Minnesota 55420

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SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

During the past quarter, we demonstrated significant progress in several areas. Seeded growth of silicon-on-ceramic (SOC) with an EFG ribbon seed was demonstrated Different types of mullite received from Coors were successfully coated with silicon. A new method of deriving minority carrier diffusion length, L_n, from spectral response measurements was evaluated. Our ECOMOD cost projections were found to be in good agreement with the interim SAMIS method proposed by JPL. On the less positive side, there was a decrease in cell performance which we believe to be due to an unidentified source of impurities. Also, operation of the new coating system fell behind schedule but is expected to improve in the coming quarter, since construction has now been completed.

Results and accomplishments of the quarter can be summarized as follows·

- Three economic evaluation projections were made for the SOC sheet process. They include a "baseline," a pessimistic, and an optimistic projection. If final cost figures fall between the pessimistic and optimistic values, the $\$10/m^2$ (added value) target for sheet silicon can be met. There is remarkable agreement in the results between Honeywell's economic analysis method and JPL's interim method.

- Seeding experiments performed during the quarter, where a small section of an EFG-grown silicon ribbon is used to seed an SOC coating, promoted significant improvement in single-crystal grain growth.

- Initial tests indicated that the bond between the silicon coating and the substrate is actually stronger than the silicon coating itself.

- Smooth, continuous silicon coatings were applied to substrates which had flared slots cut into the green coupons prior to the high-temperature firing. Solar cells have not yet been fabricated from such substrates.

- Modeling studies showed that when slotted substrates are used to electrically contact the base layer of an SOC cell, the series-resistance problem is considerably reduced if the silicon does not penetrate the slots. We demonstrated that the degree of penetration can be controlled by the carbonization of the slots.

- Construction of our continuous coating (SCIM) facility was completed during the quarter and initial tests led to a few modifications most of which were completed. It was designed to silicon coat, in a continuous manner, 10-cm x 100-cm substrates.

- Fracture toughness and thermal shock measurements were made in an effort to better understand why failure of the ceramic during dip coating occurs more often in MV20 mullite substrates fabricated from some batch lots than it does in others. It is suspected that the differences in thermal shock resistance are due to differences in the density and size of larger flaws (e.g., surface folds due to the rolling operation).

- A new solar-cell test setup was made operational which was designed to scan the current-voltage (I-V) characteristics in three quadrants.

- A new phosphine furnace was also made operational which allows us to diffuse more material with greater control than we were previously able to do with our solid-diffusant (P_2O_5) furnace.

- The lower values of efficiencies obtained in SOC samples made during the quarter strongly suggest that we have an unidentified source of impurities. The lower values of J_{sc} are especially indicative of shorter diffusion lengths. Although the dip-coating system was cleaned several times and there was some improvement in cell performance, the problem was not identified or corrected during the quarter.

- Progress was made in the area of material evaluation using scanned LBIC (light-beam-induced currents) to measure minority carrier diffusion lengths within single grains and directly at grain boundaries L_n measured 45 μm and 10 μm, respectively, in the SOC material, giving approximately 8 percent efficiencies. This technique is being applied to the material with lower efficiencies to find out if the loss in efficiency is due to impurities within grains or at grain boundaries.

INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 12 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous coating process also being investigated have excellent scale-up potential which offer an outstanding cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length Crystal length is limited by the length of the substrate. More recently, EFG-grown silicon ribbons have been used to seed the SOC coatings and this procedure has promoted single-crystal grains approximately 1 cm in width. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and rate at which the substrate is withdrawn from the melt.

The solar cell potential of this SOC sheet silicon is promising. To date, 1-cm^2 solar cells have been fabricated from material with an as-grown surface and without the benefit of an antireflection (AR) coating and minimized series resistance, that have conversion efficiencies greater than 7 percent. Such cells typically have open-circuit voltages and short-circuit current densities of 0.51V and 20 mA/cm^2, respectively. Application of an AR coating to these cells would improve their efficiency in the direction of the ultimate 12-percent goal.

The SOC solar cell is unique in that its total area is limited only by device design considerations. Because it is on an insulating substrate, special consideration must be given to electrical contact to the base region. To date, this has been done using an interdigital electrode pattern. One method which offers considerable promise is to place small slots in the substrate parallel to the crystalline growth direction and contact the base region by metalizing the silicon that is exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing.

Development efforts are continuing in such areas as improvement in growth rate, reduction of progressive melt contamination, and optimization of electrical contacts to the base layer of the cell. The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The impurities from the substrate are believed to adversely affect solar-cell conversion efficiency. A special type of graphite coating on the substrate has shown a potential for inhibiting this dissolution of mullite. Should these coatings prove to satisfactorily isolate the substrate from the melt in a cost-effective manner, improved solar-cell performance should be forthcoming. An alternate method for reducing substrate dissolution is to reduce the contact area the substrate makes with the silicon melt. Therefore, a silicon coating facility has been constructed which is designed to coat large (10-cm x 100-cm) substrates in a continuous manner. It is expected that this new facility will not only improve the growth rate, but also minimize the silicon melt's contact with the substrate. This should reduce the rate at which the melt becomes contaminated. Further, this new facility will permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process.

TECHNICAL DISCUSSION

SUBSTRATE CHARACTERIZATION (B. Koepke and K. Wouri)

During the quarter, most of the efforts concerning substrate characterization were addressed to the mechanical properties, particularly the thermal shock resistance, of the materials. The emphasis on mechanical properties resulted from the observation that certain groups of substrates had a greater tendency to fracture during dip coating than others To control this behavior, a better understanding of the fracture behavior and thermal shock resistance of silicon-coated mullite is needed

Fracture Toughness Testing

The fracture toughness is an indication of the resistance of a material to fast, catastrophic crack propagation and is usually denoted by the critical stress intensity factor, K_{IC}. K_{IC} is a measure of the stress at a crack tip during fast fracture in terms of the crack tip and loading geometry, the crack size, and the remote applied stress according to $K_{IC} = Y \sigma_F \sigma_a$, where Y is a geometrical constant, σ_F is the fracture stress, and σ_a is the crack length. K_{IC} is a material property and is determined by measuring the load required to fracture precracked specimens with known loading and crack geometries

Two types of fracture toughness measurements are being made on mullite substrates In the first case, the fracture toughness of the mullite is measured by propagating a crack through the bulk of the substrate. In the second case, the relative adhesion of the silicon on the ceramic is measured by propagating a crack along the silicon-ceramic interface. The constant-moment modification of the double-cantilever-beam testing technique devised by Freiman, et al., is being used for these measurements. An advantage of this technique is that the stress intensity factor is independent of crack length. Thus, the fracture toughness measurement can be made by simply loading a precracked specimen to failure. Crack length measurements are not necessary. A schematic of the specimen and loading geometry is shown in Figure 1. A side groove is cut into the specimen, as shown, to guide the crack. To measure the adhesion of silicon to the ceramic with this technique, a composite specimen is produced by cutting a slot down about 80 percent of the length of the specimen. The slot is cut through the specimen thickness to the width of the side groove. The sides

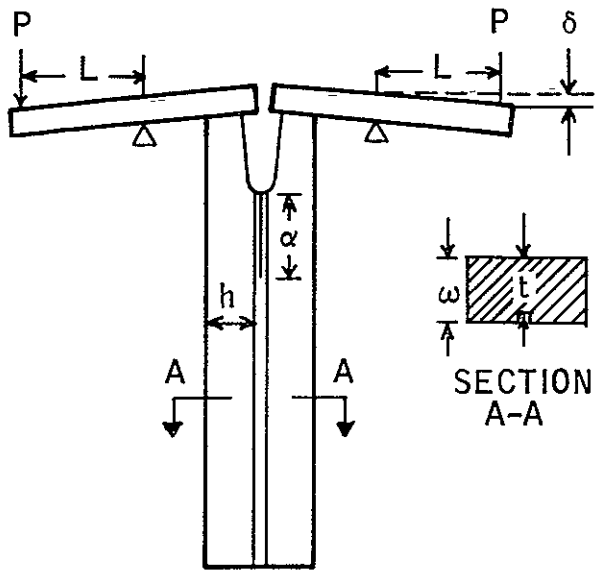

Figure 1. Schematic Showing Specimen and Loading Arrangement Used in the Constant-Moment Test. δ is the Deflection of the Point of Load Application During the Test

of the slot are carbon coated and the specimen is dipped in silicon so that a silicon web forms in the slot The slot is cut off-center so that the silicon-ceramic interface runs down the centerline of the specimen The crack is expected to then run down the silicon-ceramic interface to give a measure of the adhesion of the silicon on the ceramic

Fracture toughness measurements made on mullite samples cut from specimens that showed some tendency to fracture during dip coating are listed in Table 1

Table 1 Fracture Toughness of Mullite Substrates

Sample	K_{IC} ($MNm^{-3/2}$)
101977	2.24
7-67-1	2.26
7-67-2	1.84
7-67-3	1 71

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To put these values in perspective, values for the fracture toughness of ceramics range from 0.75 $MNm^{-3/2}$ for soda-lime glass to greater than 6 $MNm^{-3/2}$ for hot-pressed silicon nitride. Fine-grained alumina has a fracture toughness of about 5 $MNm^{-3/2}$ These measurements are continuing and a more complete comparison will be available at the end of the next reporting period.

In our attempts to propagate cracks along the silicon-ceramic interface, we were unsuccessful. In every case, the fracture propagated through the silicon. The measurements therefore give an indication of the fracture resistance of the polycrystalline silicon web in the specimen but not of the adhesion. In many of the composite specimens, the silicon web turned out to be hollow (i.e., the silicon coating merely bridged the top and bottom surfaces of the specimen) To date, two specimens have been produced with silicon completely filling the slot The fracture toughness measured on these specimens is listed in Table 2

Table 2 Fracture Toughness of Composite SOC Specimens

Specimen	K_{IC} ($MNm^{-3/2}$)
77-24M7X	1 95
76-7M7X	1.65

Thus, based on the data we have, the fracture resistance of the polycrystalline silicon appears to be the same as that of the substrates If the silicon penetrates the ceramic, a crack running along the interface is expected to experience more resistance than one running in the silicon. For comparison purposes, K_{IC} for (111) cleavage of a silicon crystal at 77°K is about 0.6 $MNm^{-3/2}$. K_{IC} for the polycrystalline silicon is much higher, as expected. These measurements are continuing. Since a number of different carbon coatings will be used, it is expected that some silicon-ceramic interface separation will be observed. In the tests run to date, thin Dag coatings were used and the silicon penetrated the coating and formed an interlocking bond with the substrate.

Thermal Shock Measurements

We have recently started a number of measurements to determine the relative thermal shock resistance of the different mullite substrates examined in this study. The method used is that attributed to Hasselman[2] in which the room temperature fracture strength (usually in bending) of samples quenched from elevated temperatures is measured as a function of quench temperature. When the quenching stresses are

sufficient to propagate localized flaws in the ceramic, the room temperature fracture strength decreases abruptly The critical quench temperature corresponding to the strength decrease is an indication of the thermal shock resistance Higher critical quench temperature implies greater thermal shock resistance

An example of these measurements is shown in Figure 2 In the figure, the fracture strength at 25°C of samples taken from one of the batches of MV20 mullite supplied by the Honeywell Ceramics Center is shown as a function of quench temperature The strength data were taken using four-point bending on bars annealed in air and quenched in ice water The critical quenching temperature for this material is in the interval 275° to 350°C. Measurements of this type were recently completed on all substrate materials used to date, but the data remain to analyzed Preliminary analysis shows that the critical quench temperature of most of the substrates lies in the same range as that shown in Figure 2

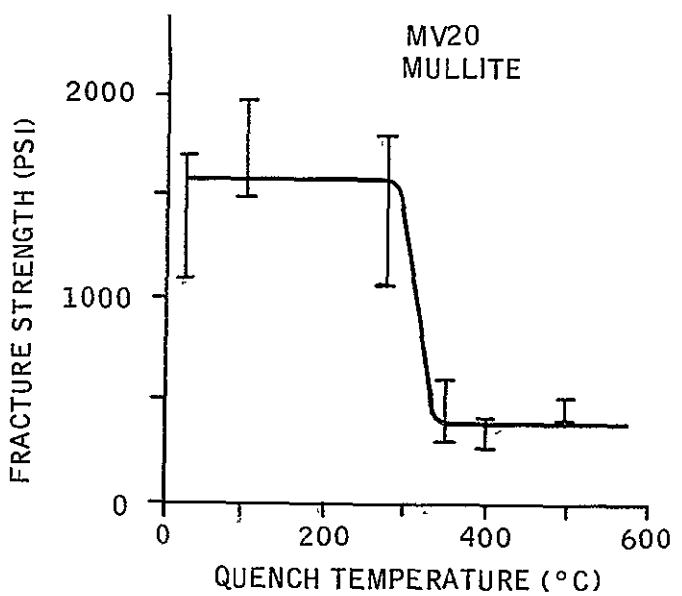

Figure 2. Fracture Strength of MV20 Mullite as a Function of Quench Temperature. Samples Were Annealed at Temperature Shown, Then Dropped Into Ice Water.

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Microstructural and Chemical Analysis

As mentioned earlier, we have noted that the tendency for MV20 mullite substrates produced at the Honeywell Ceramics Center to fracture during dip coating varied from lot to lot. Photomicrographs of samples of three MV20 batches exhibiting differences in fracture resistance during dip coating are shown in Figure 3. Lots A and B were found to break at a noticeably higher rate than Lot C. No noticeable differences were evident in the microstructures. All contained similar amounts of porosity and impurities such as those denoted by the arrows on the micrographs. An alternate explanation is that the differences in thermal shock resistance are due to differences in the density and size of larger flaws (e.g., surface folds due to the rolling operation) introduced during forming. The size and morphology of larger flaws can be characterized quite easily by measurements of the fracture strength. Unfortunately, strength measurements were not made while the earlier batches of MV20 were being dip coated and comparisons cannot be made.

During the quarter, a number of Coors substrates were analyzed by emission spectroscopy and can now be compared with the analyses run on the MV20 substrates and published in Annual Report No. 1. These comparisons are made in Table 3.

Table 3. Semiquantitative Emission Spectrochemical Analysis of Mullite Substrates in Wt. Percent

Sample	Ti	Cu	Mg	Fe	Ca	V	Ni	Cr	Mn
MV20	0.78	<0.01	0.20	0.89	0.11	0.031	---	---	0.041
SIS1	1.1	0.071	0.29	0.68	0.070	0.051	<0.03	0.030	<0.03
Open-porosity modification	1.45	0.038	0.29	0.57	0.062	0.036	<0.03	0.026	<0.03
Reducing-fire modification	1.0	0.27	0.27	0.52	0.062	0.042	<0.03	0.28	<0.03
High-purity modification	0.27	0.047	0.14	0.45	0.080	<0.03	<0.03	N.D.	<0.03

Notable differences include the lower impurity content in Coors high-purity material and the higher Ti and Cu and lower Fe in SIS1 compared with the MV20 materials.

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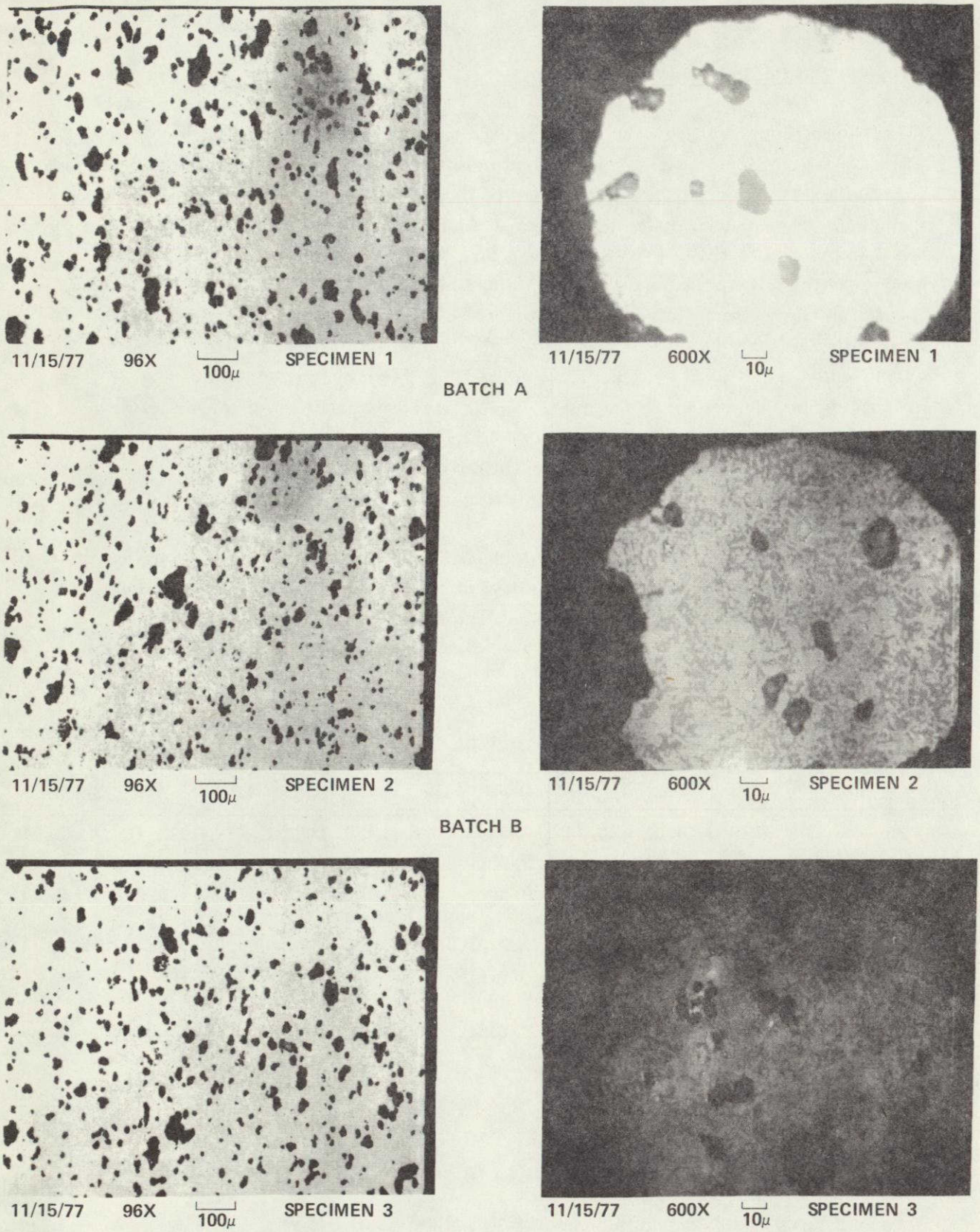

Figure 3. Photomicrographs of Three Batches of McDanel MV20 Mullite Substrates Produced at the Honeywell Ceramics Center. Batches A and B Showed a Greater Tendency to Fracture During Dip Coating than Batch C.

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SILICON FILM GROWTH (R. B. Maciolek, D. J. Sauve, S. J. Marquardt, and K. V. Wuori)

Apparatus and Procedure

Several changes were made during the quarter in both the dip-coating apparatus and the operating procedure. Another viewport was added to the top of the chamber. This permits viewing of both sides of the substrate during immersion and withdrawal. A new heating element of a more rugged design was installed. The boron-nitride collar on which the crucible support rested was replaced by one of thin-wall alumina. This was done because the boron-nitride collars deterioriated during service. An added benefit from this change was improved thermal isolation of the crucible. The WRP ceramic fiber insulation that was used to support the heat shields and electrically isolate them from the base of the heater was replaced by an array of alumina tubing. This was done because the WRP was also deteriorating during service. These changes resulted in better thermal response and easier maintenance.

Two changes were made in operating procedures. First, the Dag 154 used to carbon coat the substrates was diluted with toluene instead of alcohol. Dag diluted with alcohol, which was used previously, absorbed water from the air and caused the silicon coating to blister. Second, the rate of gas flow through the apparatus was increased from 0.4 liter per minute to 1.6 liters per minute. This action keeps the surface of the melt free of particulate matter which was observed to accumulate at lower flow rates.

Growth Experiments

Twelve runs were made and a total of 101 samples were dipped during the quarter. Two of the runs were dummy runs during which no substrates were dipped. This was done to check on contamination levels before and after cleaning and the previously mentioned materials modifications. Resistivity of the melt changed from 15 to 100 ohm-cm. Another run was terminated abruptly, before any samples could be coated, due to power supply failure.

The majority of the substrates that were dipped were carbon coated using Dag 154 diluted with toluene. One substrate was coated with a Dag-borosilicate mixture and another had electroless nickel deposited on the substrate beneath a Dag coating. The carbon-borosilicate mixture did not coat as well as plain carbon, and the carbon-nickel coating spalled off above the melt before dipping. Both experiments were attempts to make a back contact to the silicon layer.

Work continued on the seeded growth experiments. Thirteen substrates with seeds of EFG silicon ribbon {110} <112> attached were dipped. Some of the seeds shattered upon contacting the melt and in other cases the liquid film withdrew from the seed as the substrate was raised. However, in a number of instances it was possible to effectively seed the solidification of the silicon film and control the grain size. Figure 4 shows two examples of silicon films that were successfully seeded using EFG ribbon. The films' surfaces have been etched to reveal the grain structure. Note the wide grains extending down from the seeds.

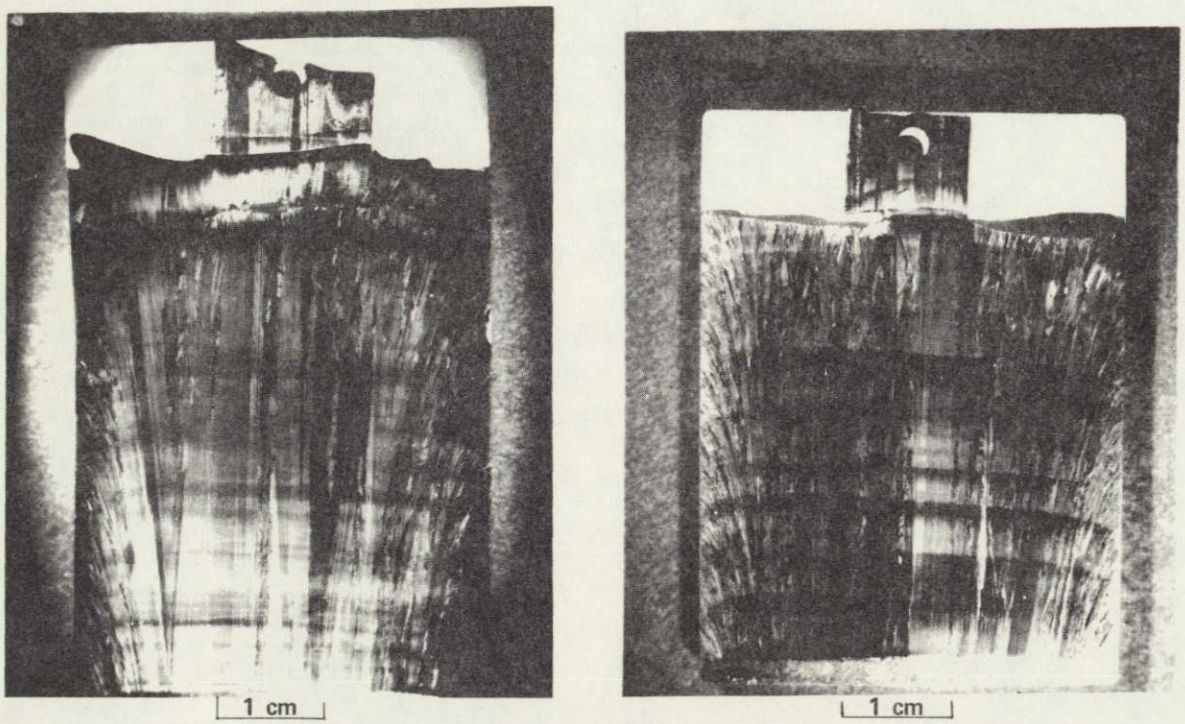

Figure 4. Examples of Silicon-on-Ceramic in Which Grain Size Has Been Altered by Seeding with EFG Silicon Ribbon (Seed Measures Approximately 11 mm Across. Samples Have Been Lightly Etched to Reveal Structure. Note Wide Grains Beneath Seeds Extending Length of Substrate.)

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Substrate Modifications

Two different substrate configurations were coated. Two substrates had grooves cut parallel to the pulling direction. The grooves were 2 mm wide and 1 mm deep. The idea was to apply a much thicker layer of carbon to the bottom of the groove to provide electrical access to the back of the silicon film. After dipping, it was apparent that the grooves were too deep and did not give a smooth surface. Two substrates with wire-sawed grooves 0.5 mm x 0.5 mm were then dipped. One had the grooves running parallel to the growth direction and one perpendicular. The resulting silicon films on these substrates were much smoother and their properties are being evaluated.

The other substrate configuration coated was the slotted configuration prepared by the Honeywell Ceramic Center. The slots are flared holes that go through the substrate and measure ~0.5 to 1.0 mm wide and 15 mm long. Five such substrates were dipped. One fractured upon cooling, and the silicon spalled off the others to varying degrees. However, the silicon did bridge the slots to give a continuous surface, and the spalling problem is thought to be associated more with the thickness of the carbon coating that was applied than with the substrate configuration.

A total of 18 mullite substrates prepared by Coors were coated this quarter. The majority were of the standard SIS1 composition, but at least one of each of the following compositions were also dipped:

- High-mullite SIS1 modification
- High-glass SIS1 modification
- Glass-property modification of SIS1
- Open-porosity modification of SIS1
- High-purity modification of SIS1
- Electrically-fused mullite

The electrically-fused sample was the only one which did not survive the dipping. It shattered above the melt before it was dipped.

Ten substrates made by the Honeywell Ceramic Center from a new batch of MV20 were also dipped. All ten survived the dipping. The new batch of MV20 was obtained because of strength problems associated with the last batch. In fact, tests made on

samples of the green, dried ceramics (60°C for approximately 12 hours) showed the new batch to have approximately four times the fracture strength of the last batch, making it roughly equivalent to the first batch. Scanning electron microscopy (SEM) was used to examine the fracture surfaces, but no correlation could be made between the differences in strength and observed structure. These observations indicate a need for better control and specification of incoming material.

In the course of dipping substrates, it has been observed from time to time that some silicon will adhere to the back (not carbon coated). Furthermore, it has been observed that such patches affect the solidification of the silicon on the front (carbon-coated) side. It appeared that the portion of silicon film opposite an adhered patch was thinner than the rest of the film. To confirm this, and to learn why the silicon was adhering to the back, such a substrate was sectioned and examined metallographically. The results are shown in Figures 5, 6, and 7.

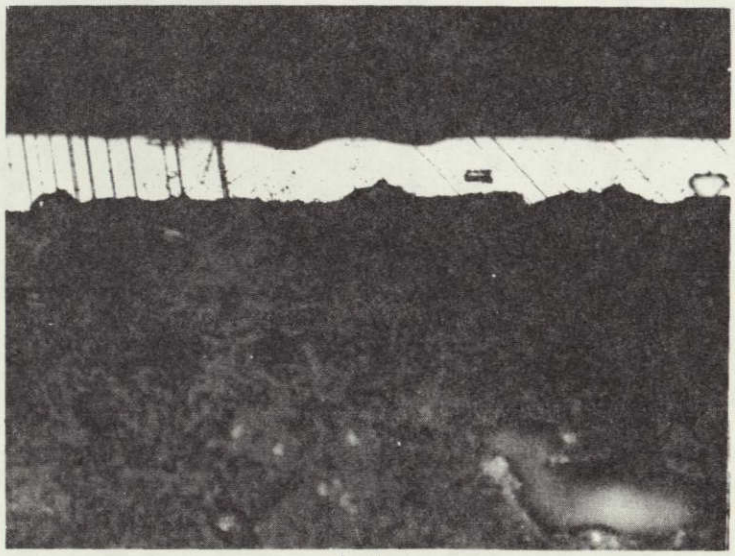

Figure 5. Undisturbed Film of Silicon Approximately 20 μm Thick

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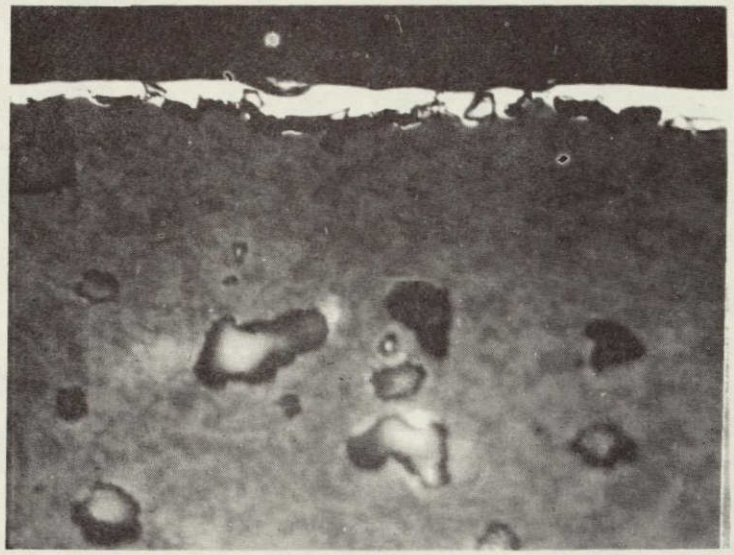
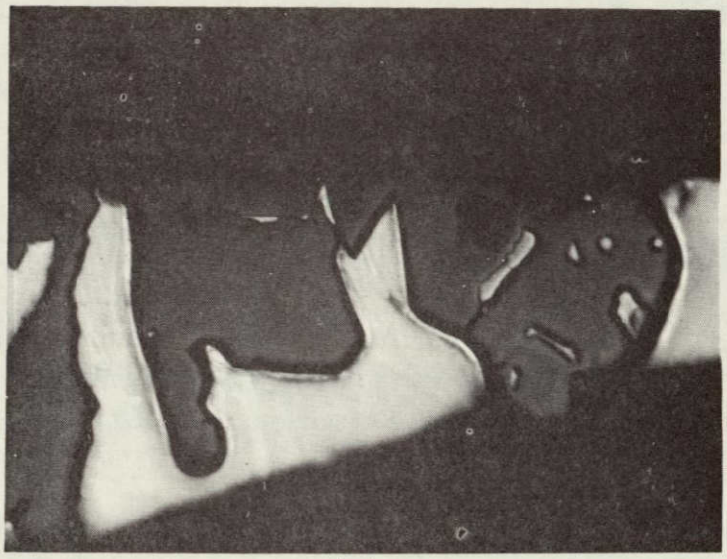


10μ

Figure 6. Silicon Film Opposite Patch Adhering to Back Side of Substrate, Approximately 10 μm Thick



10μ

Figure 7. Cross Section of Silicon on Back Side of Substrate. Note Large (Approximately 100 μm Across) Carbide Particles.

Figure 5 shows the undisturbed film approximately 20 μm thick. Figure 6 shows that the film opposite the patch adhering to the back is approximately 10 μm thick. Figure 7 shows the cross section of the silicon on the back, and, surprisingly, it contains massive (approximately 100 μm across) carbide particles. Thus, the mechanism of wetting promoted by carbon appears to be the same as on the front side but the source of the large amount of carbon has not yet been identified.

CONTINUOUS-COATING FACILITY (J.D. Heaps, C.D. Butter and L.D. Nelson)

During this reporting period, construction of the continuous-coating facility was completed and preliminary tests were made. Expected problems such as gas and water leaks and loose electrical connections were readily corrected. A few minor modifications were made to improve the thermal shielding and prevent overheating in various regions of the coating chamber.

The new coater, shown in Figure 8, was designed to Silicon Coat ceramic substrates using an Inverse Meniscus (SCIM). To date, this coating principle has not been demonstrated due to absence of power supplies which were scheduled for delivery on 9/6/77 but were not received until 12/28/77. They are now being installed.

To offset the delay, the coater was tested using smaller power supplies that were temporarily loaned to us by the manufacturer. The resistivity of the graphite and the thickness of the coater's heating elements were selected to give a resistance of 0.02 ohms to match the 1500-ampere, 30-volt capability of the power supplies which were ordered. The smaller power supplies, on the other hand, were rated at 600 amperes and 40 volts, maximum, corresponding to an element resistance of 0.067 ohm. When the coater was tested using these smaller units, the maximum attainable temperature was 1120°C, which will not melt silicon. To increase the resistance by thinning the heating elements to match the power supply would have rendered them impractically fragile. Therefore, the element resistance was increased by drilling a systematic pattern of holes. This, unfortunately, produced no improvement in achieving the temperature needed to melt silicon. This lack of improvement probably resulted from the reduced area of radiation which rendered the system less efficient in heating the crucible holder.

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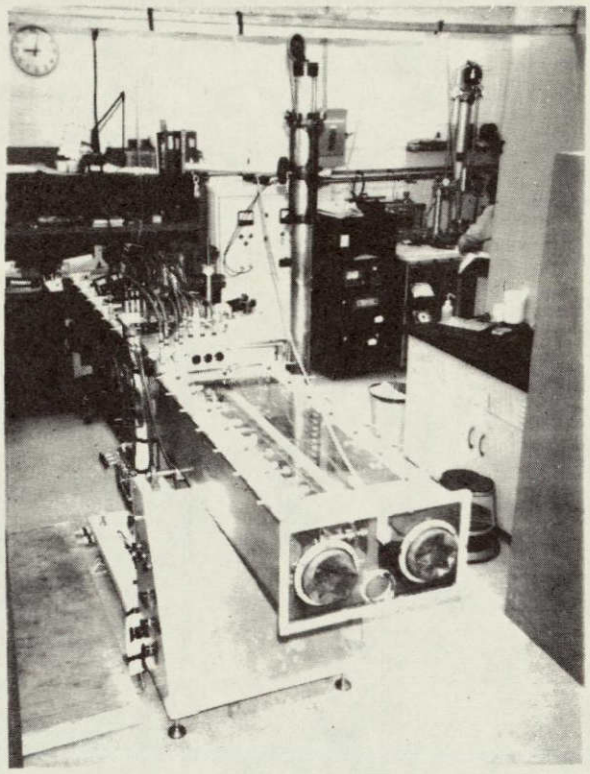

Figure 8. Coater Portion of Continuous Coating Facility

Tests conducted with the smaller power supplies made it apparent, however, that the melt crucible and the quartz trough over which the substrate passes should be heated by separate elements. In the original design, shown in Figure 9, both the quartz trough containing the silicon meniscus and the melt crucible share a common graphite holder. As also shown in Figure 9, the substrate top heating element is positioned directly above the quartz trough, whereas that portion of the graphite holder surrounding the melt crucible is free to radiate energy to colder parts of the coating chamber. Thus, with this design, the molten silicon in the quartz trough will be hotter than the silicon contained in the melt crucible. To correct this situation, two independent power supplies and two separate heating elements were designed to control the temperature of these two zones. The new design is shown in Figure 10.

Discussions held with other contract personnel regarding the most productive operating approach for the new coater led to the suggestion that the machine should be able to also coat substrates of various lengths. To do this, the coater was modified by installing

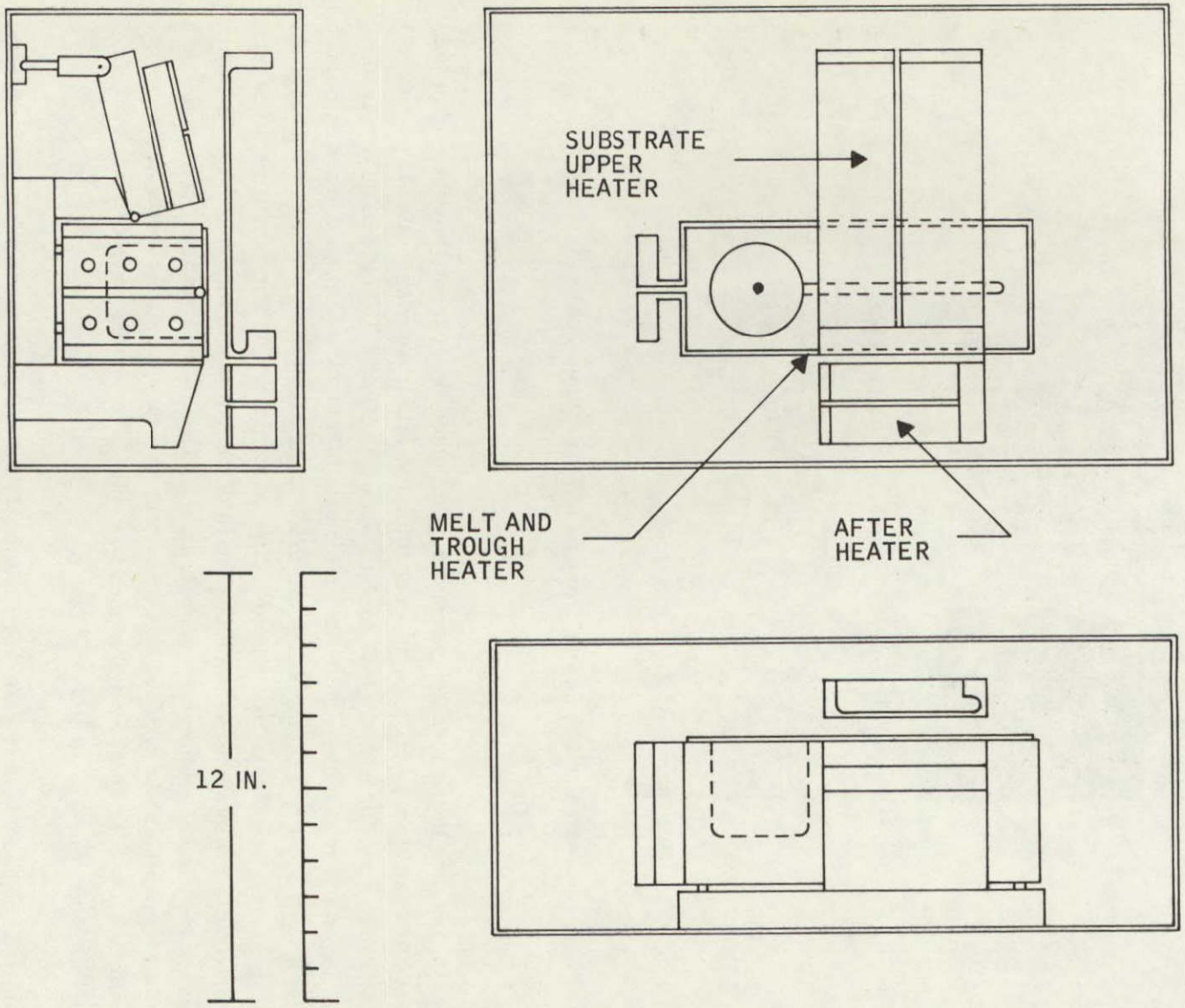

Figure 9. Original Heating-Element Arrangement in Coating Chamber of SCIM

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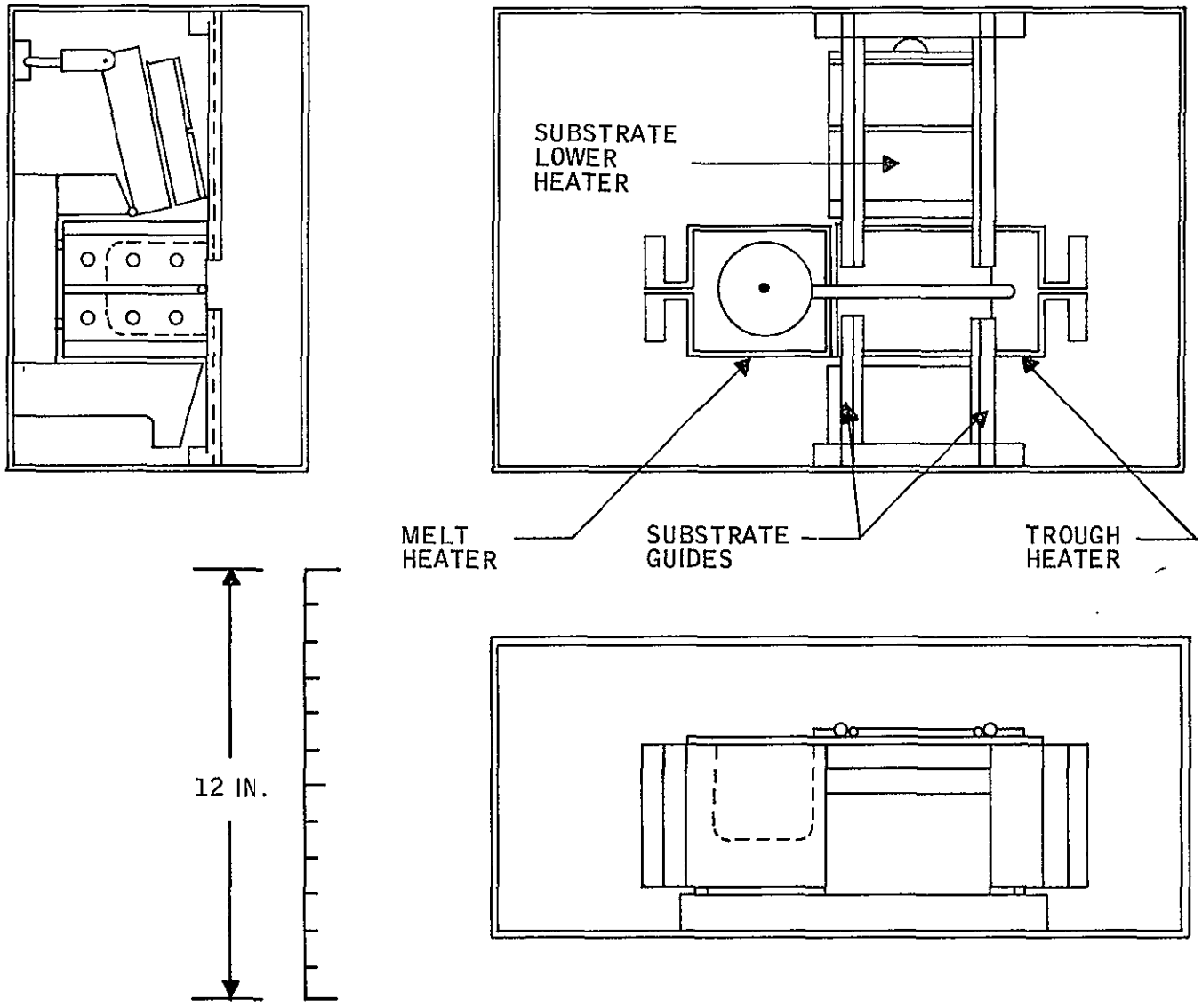

Figure 10. Modified Heating-Element Arrangement in Coating Chamber of SCIM Coater (Substrate Upper Heater not Shown)

ceramic (99.8 percent alumina) guides to direct various odd-sized substrates over the silicon meniscus. This feature is also shown in Figure 10. Note that the height of the entire heater assembly can be adjusted with respect to the fixed substrate conveyors. This provides a way for adjusting, as needed, the meniscus level with respect to the substrate. The ceramic substrate guides are attached to the coating chamber to provide adequate support for short substrates. The adjustments of meniscus height can, of course, be made while a coating run is in operation.

All the modifications described above are designed to increase the versatility of the system and we anticipate that the system will be thoroughly tested during January 1978.

MATERIAL EVALUATION (D. Zook, T. Schuller, and R. Hegel)

LBIC Measurements

Some notable progress was made in the area of material evaluation using scanned LBIC (light-beam-induced current) to measure minority carrier diffusion length, L_n. First, it was found that if extra care is taken to assure that the beam from the monochromator is indeed monochromatic, the ambiguity between the use of different sets of absorption coefficient data from the literature appears to be removed (the stress-relieved values of α were the only ones to give straight lines). Also, an improved method to determine L_n from the data was derived and a new method using bias modulation was evaluated. Measurements of L_n were discussed at the IEDM meeting during the quarter.[3]

The theory is based on the expressions given by Hovel[4] for photocurrents. The spectral quantum efficiency, S, is given by:

$$S = \frac{(1 - R)\,\alpha\,(L_n + W)}{L + \alpha L_n} \tag{1}$$

where R is the reflectance, α is the absorption coefficient, and W is the junction width. This expression is valid if the thickness, H, is so large that $\alpha H \gg 1$, and if $\alpha W \ll 1$. The expression can be rewritten as:

$$\frac{1 - R}{S} = \frac{1}{L_n + W}\left(\frac{1}{\alpha} + L_n\right) \tag{2}$$

so that the plot of $(1 - R)/S$ against α^{-1} should be linear with an intercept of $-L_n$ and a slope of $L_n + W$. The junction width, W, can be determined by capacitance measurements and generally is much less than L_n.

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Comparison with recent as well as earlier plots of LBIC data shows that the slope tends to give a higher value of L_n than the intercept. The difference amounts to as much as 30 percent. Since the intercept depends on the relative spectral response and the slope depends on the absolute spectral response, the discrepancy may indicate that the absolute calibration of our standard photodiode may be incorrect.

Another method of measuring L_n was investigated which does not depend on a calibration nor on a knowledge of α as a function of wavelength. This method, which we call bias modulation, is a variation of a method used at Honeywell by Paul Peterson to measure L_p in GaP. If a change in W is made in Equation (1), this results in a change in S which is proportional to the change in photocurrent, I. Equation (1) leads directly to the relationship:

$$\frac{\Delta I}{I} = \frac{\Delta S}{S} = \frac{\Delta W}{L_n + W} \tag{3}$$

where the change, ΔW, can be brought about by a change in bias. Capacitance measurements can be used to give the space charge width, W, as a function of bias voltage, V.

Bias modulation measurements were made at 0.9 μm with a focussed beam at points within grains and at grain boundaries. In both cases, the bias modulation gave too high a value of L_n in comparison with the spectral-response measurements. The modulation effect is biggest when the diffusion length is smallest, as expected. For example, diode 169A1-61b-5 gave results for L_n as shown in Table 4 and in Figure 11.

Table 4. Measured Values of Minority Carrier Diffusion Length, L_n

Location	Value	Method
Within a grain	38 to 43 μm	Intercept
	50 to 52 μm	Slope
At grain boundaries	8 to 10 μm	Intercept
	9 to 10 μm	Slope
	30 to 36 μm	Bias modulation
Overall cell average	15 μm	Intercept

The slopes and intercepts were all determined using SR (stress-relieved) data for α and spectral-response measurements at the six peaks of the xenon lamp between 0.8 and 1.0 μm.

Several tentative conclusions can be drawn from the above data. First, the bias modulation gives an unrealistically high value. Second, the intercept value is consistently

smaller than the slope value. On the whole, the method is quite meaningful. Work will be continued to define which procedure gives the most reproducible values of L_n. In cells having poor performance, we will see whether degradation occurs within grains, at grain boundaries, or at the surface. The latter can be determined from the ultraviolet response.

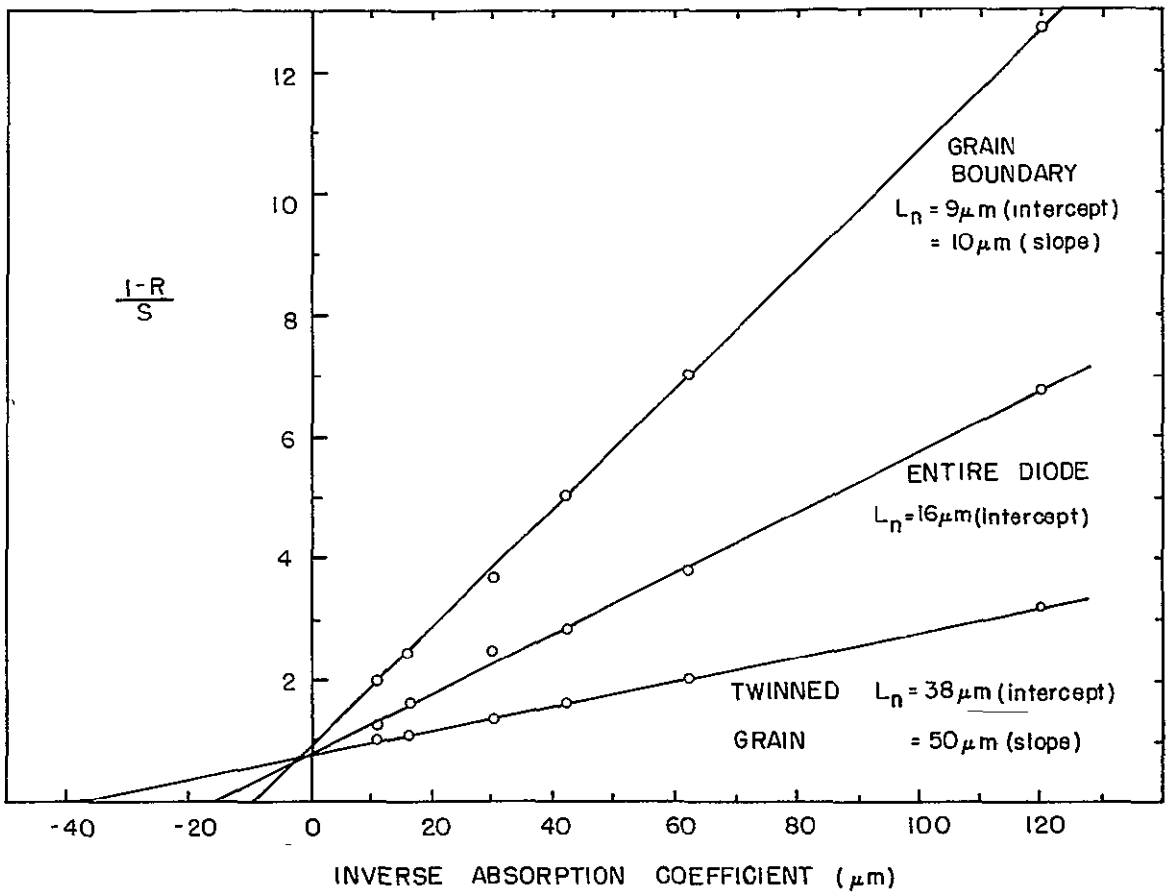

Figure 11. Plot of Spectral Response Data Used to Derive L_n

Silicon-Carbon Interface

Several attempts were made to improve the conductivity of the carbon-silicon interface using boron doping and Dag carbon coatings. Approaches used were:

1) A single mixed borosiliate glass (BSG) and Dag coating

2) A light HF etch of the ceramic followed by a BSG coating fired at 900°C and a layer of Dag also fired at 900°C

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Because of the possibility of contamination, the substrates were the last ones to be dipped in a dip-coating run.

In the first case, the carbon appeared to be quite well intact after the silicon coating had been applied, but there appeared to be no significant electrical conduction from the silicon to the carbon. To see if boron was still present in the carbon, a sample was heat treated at 1025°C for 49 hours, a condition which should have caused significant diffusion of boron into the silicon and given a p^+ back contact. A comparison of the sheet resistance before and after the heat treatment showed no decrease in resistance due to a p^+ back layer, however.

In the second case, it was hoped that by having the BSG soak into the porous boundary layer of the etched ceramic, it would stay intact during the dipping process. However, the resistance of the layer and of the melt were much lower than expected, indicating that the boron entered the melt. Portions of the silicon coating were removed by etching, leaving separated pads of silicon. In this way, the sheet resistance of the underlying carbon was determined to be about 190 ohms/□ and the contact resistance of the silicon-carbon interface was measured. It was found to be somewhat nonlinear, as shown in Figure 12, with a small signal value of about 1 ohm-cm^2.

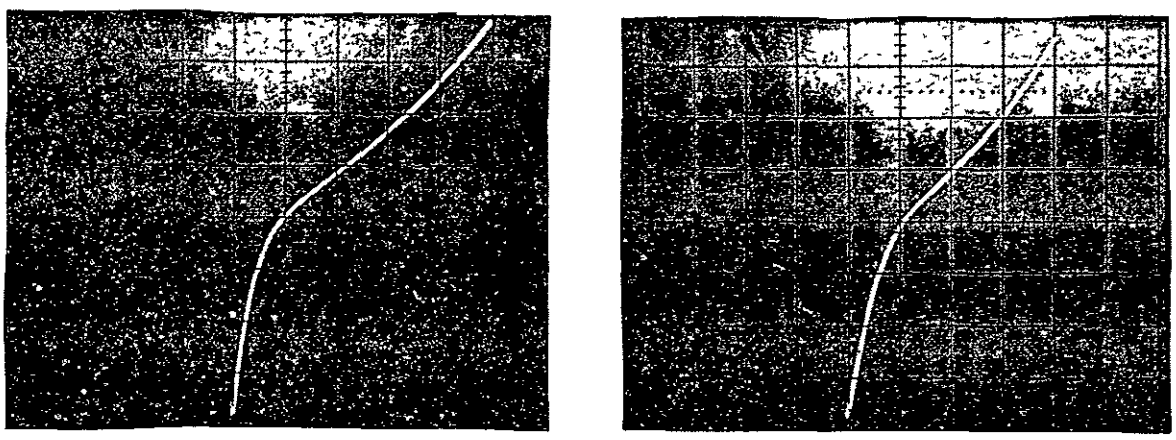

Figure 12. Current-Voltage Relationship of Silicon-Carbon Interface

Both the contact resistance and the sheet resistance of the carbon in this sample were clearly too high to be useful as a built-in base contact.

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Device Fabrication

During the quarter, the phosphine (PH_3) furnace became operational. This allows us to diffuse much more material with far greater control than we could with the solid-diffusant furnace previously used. It will also allow us to diffuse the larger silicon-on-ceramic material from the new continuous-coating facility when it becomes operational. Some trouble was experienced in obtaining uniform diffusions over an appreciable length of the furnace, even though thermal probing had been used to adjust the hot zone to be extremely uniform in temperature. The problem was reduced considerably by using baffles at both ends of the tube to ensure more-uniform gas flow. We acknowledge a helpful telephone conversation with John Scott-Monk of JPL on this subject. All samples on a 12-inch sample holder came out of the furnace very uniformly oxidized as judged by the color and uniform in sheet resistance.

We also modified our processing procedure slightly. We found that a thin layer of solder does not interfere with our photolithography. Solder is therefore applied before the final mesa etch, so that the cells never see a temperature higher than room temperature after the mesa is exposed. As indicated in Table 5, the changes in device processing did improve the performance of single-crystal control cells. Efficiencies range between 9 and 10 percent for uncoated cells. With P_2O_5 diffusions at 855°C for 30 minutes, the sheet resistances, ρ_s, varied from 33 ohms/□ to 50 ohms/□. The sheet resistance for the PH_3 diffusions at 854°C for 40 minutes was 40 to 45 ohms/□. Although the efficiencies do not change much with sheet resistance, there seems to be some correlation between sheet resistance and V_{oc}. On the whole, the device processing seems quite consistent and has high yield.

Cell Evaluation

During the quarter, the solar-cell test circuit was improved to speed up the testing of cells. The circuit is shown schematically in Figure 13. It is designed to scan the current-voltage (I-V) characteristics in three quadrants, starting at a given negative current, sweeping through the positive current and voltage quadrant, and ending at a given negative voltage. Thus, the dark and light I-V characteristics can be plotted on the same chart without resetting any of the controls.

The instantaneous current and voltage in the cell is displayed digitally at all times. There is provision for checking the zero and the J_{sc} and V_{oc} values. The current meter has four ranges, from 2 mA to 2 A full-scale. The scan rate can be varied as desired. A photograph of the solar-cell test setup is shown in Figure 14.

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Table 5. Single-Crystal Comparison Cells

Diodes	Number of Diodes Averaged	Active Area (cm^2)	P_s ($\Omega/\square$)	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill Factor	Efficiency (%)	Maximum Efficiency (%)	Comments
APDF-B1	7	0.078	45	0.53	26.9	0.69	9.9	10.2	Spin-on diffusion
APDF-B2	7	0.078	45	0.53	26.6	0.67	9.3	10 0	Spin-on diffusion
APDF-3	7	0.078	45	0.46	25.9	0.561	6.7	8.1	(Edge of wafer) (Spin-on diffusion source) (Nonuniform)
SC-79	3	0.09	36	0.526	24.0	0.68	8.6	9.2	
SC-80	2	0.11	38	0.54	24.8	0.74	9.9	9.9	Only three diodes made due to chip size; one bad
SC-81	3	0.090	33	0.54	24.3	0.72	9.5	10.1	Only three diodes made due to chip size
SC-82	3	0.090	35	0.55	23.7	0.74	9.7	9.8	
SC-83	7	0.078	42	0.54	24.3	0.728	9.5	9.9	
SC-84	5	0.092	50	0.52	26.6	0.707	9.8	10.4	
PH9-1	14	0.079	45	0.52	25.0	0.69	8.9	9.8	
PH9-2	13	0.072	44	0.52	27.4	0.69	9.7	10.4	
P-13S1	1	0 03	42	0.52	26.6	0.755	10.4	10.4	Phosphine diffusions
P-19-S1	14	0.078	44	0.53	23.7	0.743	9.3	9.7	
P-19-S2	14	0 078	43	0 53	23.4	0.752	9.4	9.6	

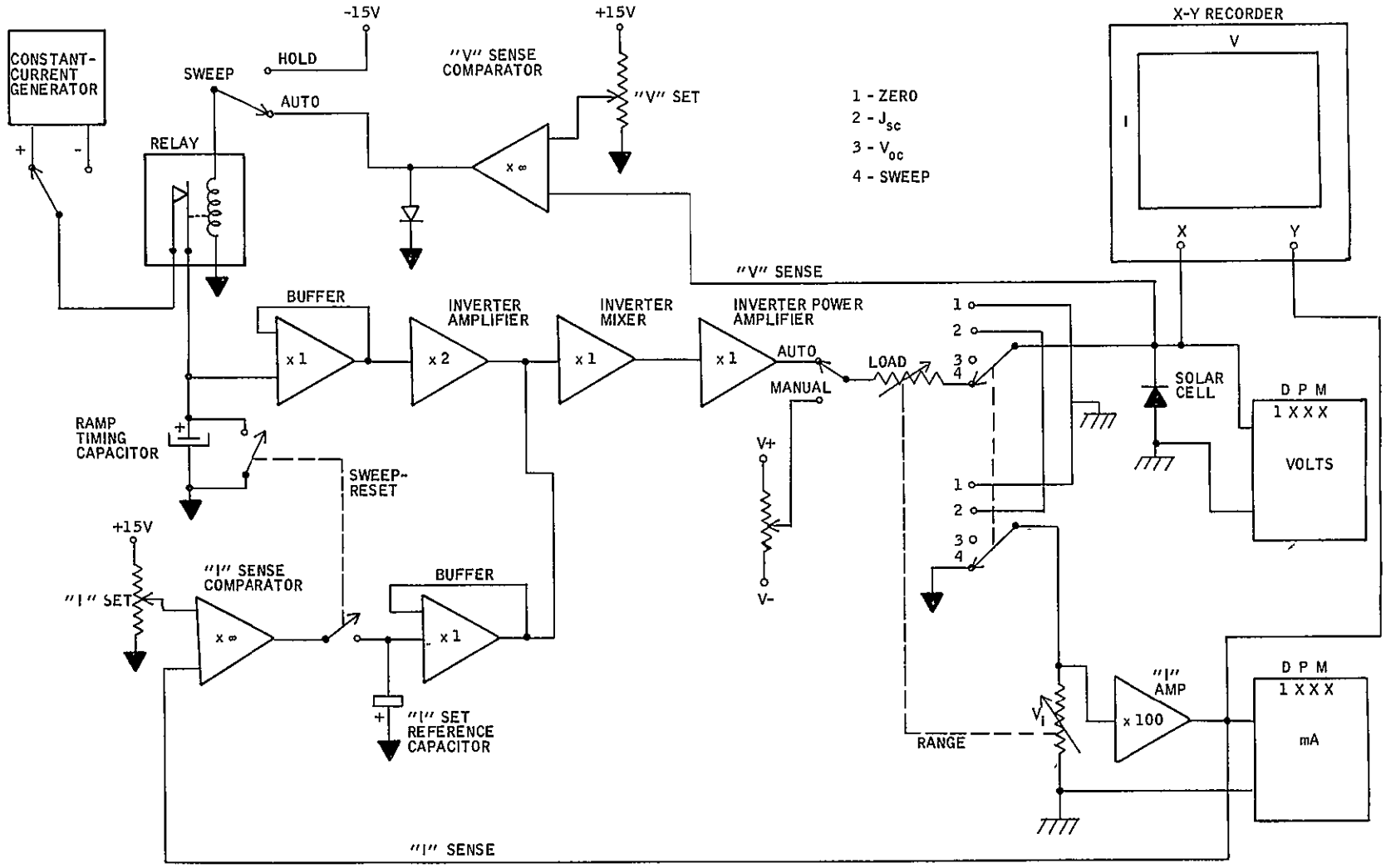

Figure 13. Solar-Cell Test Circuit Schematic

Figure 14. Solar-Cell Test Setup

Device Performance

The performance of SOC devices made during this quarter is summarized in Table 6. The first five lines show the results for substrates that were grown at higher growth speeds. Performance in these samples is definitely correlated with surface texture. The samples with a diffuse surface texture have poor performance, whereas sample R58-A-P13 had a smoother surface even though grown at the faster rate. Microscopic examination at high magnification shows that the roughness is due to small bumps on the surface that appear to be caused by particles trapped between the ceramic and the silicon film.

In the other samples which were grown at lower growth rates (0.03 to 0.06 cm/sec), the J_{sc} values range from 16 to 19 mA/cm^2, and the V_{oc} values range from 0.28 to 0.49 V. These values are lower than we had been getting, pointing to the probability of impurities causing decreased lifetime. In addition, the fill factors are lower than

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Table 6. Summary of SOC Cell and Diode Performance

Diodes	Number of Diodes Averaged	Active Area (cm^2)	P_s ($\Omega/\square$)	V_{oc} (V)	J_{sc} (ma/cm^2)	Fill Factor	Efficiency (%)	Maximum Efficiency (%)	Comments
R19A-P13	7	0.078	32	0.018	8.86	<0.4	---	---	0.1 cm/sec pull rate
R24A-P13	14	0.078	27	0.021	9.62	<0.4	---	---	0.1 cm/sec pull rate
R55A-P13	7	0.078	43	0.049	9.10	<0.4	---	---	0.08 cm/sec pull rate
R57A-P13	7	0.078	47	0.138	10.6	<0.4	---	---	0.08 cm/sec pull rate
R58C-P13	6	0.085	55	0.435	21.7	0.462	4.5	4.9	0.08 cm/sec pull rate
65-4A-82	1	1.05	40	0.462	18.76	0.501	4.34	---	
77-4A	1	1.05	38	0.49	15.8	0.64	4.9	---	
77-48	7	0.078	40	0.28	15.7	0.46	2.0	2.4	
80-1B-79	7	0.078	43	0.48	16.5	0.674	5.3	5.7	
80-1A	1	1.05	41	0.385	16.52	0.459	2.93	---	
80-2A	1	1.05	40	0.495	18.09	0.605	5.42	---	
80-2B	7	0.078	41	0.49	17.3	0.68	5.8	6.1	
85-2B-83A	7	0.078	49	0.43	18.5	0.519	4.2	5.3	
86-6D-84	6	0.062	62	0.43	18.4	0.610	4.8	5.4	
85-2B-83B	7	0.078	49	0.46	19.3	0.642	5.7	6.7	
92-8-P20	14	0.078	48	0.18	11.4	0.436	1.0	2.2	Borosilicate-doped substrate with Dag and baked
75-15-PH9-01	1	3.08	45	0.50	20.0	0.45	4.8	---	4.0 cm^2 total area
86-2-PH9-01	1	1.0	50	0.42	21.0	0.53	4.7	---	
85-7-PH9-01	3	0.048	50	0.47	16.9	0.56	4.5	4.8	
85-7-PH9-02	8	0.069	52	0.46	17.0	0.57	4.5	5.9	Poor yield
86-2PH9-02	7	0.073	47	0.38	19.2	0.56	4.0	4.7	
91-10E-P19	7	0.078	57	0.47	17.3	0.600	4.9	6.6	
91-10F-P19	1	1.0	52	0.47	18.1	0.571	4.9	4.9	
91-6C-P19	6	0.070	53	0.48	16.8	0.679	5.5	5.9	

those for the single-crystal control cells. This is probably due to the fact that these layers are thin, which causes increased values of series resistance. The series-resistance effect is especially noticeable in the larger cells, and points to the need for a good ohmic back contact. The impurities that are causing lower performance are undoubtedly at a concentration too low to measure by conventional means. Excessive boron was identified in samples by infrared transmission but this was reduced by the cleanup procedures. LBIC measurements of diffusion lengths, L_n, within grains on the poorer material were begun. The values of L_n measured in this way should be independent of grain structure, surface condition, or silicon thickness and should therefore correlate better with the concentration of impurities. Extensive and thorough cleaning of the dip-coating system is planned along with a reevaluation of the cleanliness of our sample-handling procedures.

In summary, the lower values of efficiencies obtained in SOC samples made during the quarter strongly suggest that we have an unidentified source of impurities The lower values of J_{sc} are especially indicative of shorter diffusion lengths. Although the dip-coating system has been cleaned several times and there has been some improvement in cell performance, the problem has not been identified or corrected.

DEVICE MODELING (S. B. Schuldt)

The series-resistance problem was analyzed in detail in Annual Report No. 2. The analyses drew attention to the critical problem of base-layer and back-electrode resistances. It was concluded that a shunting layer of some kind would be needed at the back of the base layer and possibly along the silicon-filled slots as well. Although this conclusion is still valid, it should be pointed out that most of the resistance was in the slots according to the geometry assumed (3 mm slot depth x 0.3 mm slot width).

The problem is considerably relieved if the silicon penetrates the slots to a relatively shallow depth, since this component of the series resistance is approximately proportional to the depth. Then the slots would be flared to provide access for metallization. (See Figure 15.)

The critical bwR_p product (area times series resistance) has been recalculated assuming a penetration depth of 0.5 mm instead of 3 mm. The significance of this product, according to Figure 40 of Annual Report No. 2, can be summarized as follows:

1) No series resistance losses are suffered if $bwR_p = 0$.

2) A 5 percent efficiency loss can be expected for $bwR_p = 0.83$ ohm-cm^2 (e.g., a 10 percent cell would be reduced to 9.5 percent).

3) A 10 percent efficiency loss occurs for $bwR_p = 1.66$ ohms-cm^2.

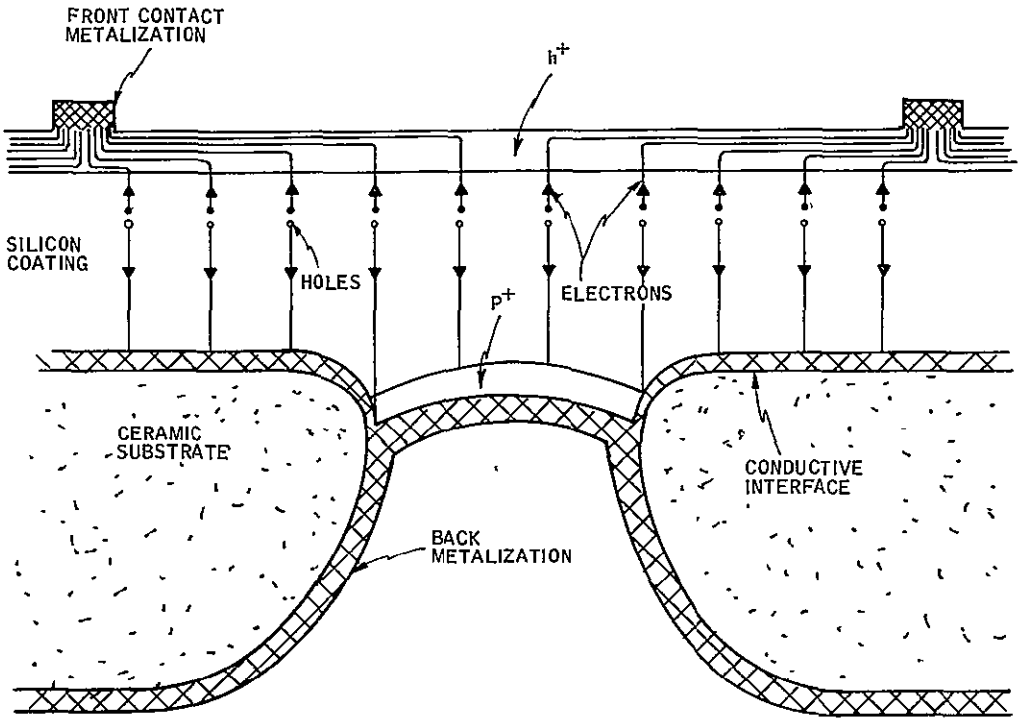

Figure 15. Schematic Drawing of Proposed Base Contact Method

Table 7 gives the new calculation (0.5 mm penetration depth) of bwR_p as a function of b for three values of base-layer resistivity ($\rho\beta = 0.3$, 1.0, and 3.0 ohms-cm). The last column in the table is bwR_p. The first four columns are the components of bwR_p due to 1) front contacts, 2) diffused layer, 3) base layer, and 4) back electrodes. The old calculation (3 mm penetration depth) is given in Table 8 for comparison. Only the fourth and last columns have changed. According to Table 7, the approximate electrode spacings, b, for 5 percent, 10 percent, and 20 percent efficiency losses are as shown in Table 9. No back-surface shunting layer is assumed.

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Table 7. bwR Product as a Function of b for Short (0.5 mm) Back-Electrode Structure (Diffused-Layer Sheet Resistance 50 Ohms/Square; Base Thickness 125 μm; Front and Back-Electrode Structures Both 0.3 mm Wide)

```
W=  1.0000E 00
BRATIO=  1.0000E 00
RHOCP=  1.0000E-05
RHOBP=  1.5000E-03
DP=  3.0000E-02
HP=  3.0000E-05
T=  5.0000E-02
D=  3.0000E-02
H=  1.2500E-02
```

RHOB= 0.30

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	2.000E-02	5.050E-02	1.133E-01
0.2	2.237E-03	1.667E-01	8.000E-02	1.010E-01	3.499E-01
0.3	3.356E-03	3.750E-01	1.800E-01	1.515E-01	7.099E-01
0.4	4.474E-03	6.667E-01	3.200E-01	2.020E-01	1.193E 00
0.5	5.593E-03	1.042E 00	5.000E-01	2.525E-01	1.800E 00
0.6	6.711E-03	1.500E 00	7.200E-01	3.030E-01	2.530E 00
0.7	7.830E-03	2.042E 00	9.800E-01	3.535E-01	3.383E 00
0.8	8.948E-03	2.667E 00	1.280E 00	4.040E-01	4.360E 00
0.9	1.007E-02	3.375E 00	1.620E 00	4.545E-01	5.460E 00
1.0	1.119E-02	4.167E 00	2.000E 00	5.050E-01	6.683E 00

RHOB= 1.00

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	6.667E-02	1.683E-01	2.778E-01
0.2	2.237E-03	1.667E-01	2.667E-01	3.367E-01	7.722E-01
0.3	3.356E-03	3.750E-01	6.000E-01	5.050E-01	1.483E 00
0.4	4.474E-03	6.667E-01	1.067E 00	6.733E-01	2.411E 00
0.5	5.593E-03	1.042E 00	1.667E 00	8.417E-01	3.556E 00
0.6	6.711E-03	1.500E 00	2.400E 00	1.010E 00	4.917E 00
0.7	7.830E-03	2.042E 00	3.267E 00	1.178E 00	6.494E 00
0.8	8.948E-03	2.667E 00	4.267E 00	1.347E 00	8.289E 00
0.9	1.007E-02	3.375E 00	5.400E 00	1.515E 00	1.030E 01
1.0	1.119E-02	4.167E 00	6.667E 00	1.683E 00	1.253E 01

RHOB= 3.00

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	2.000E-01	5.050E-01	7.478E-01
0.2	2.237E-03	1.667E-01	8.000E-01	1.010E 00	1.979E 00
0.3	3.356E-03	3.750E-01	1.800E 00	1.515E 00	3.693E 00
0.4	4.474E-03	6.667E-01	3.200E 00	2.020E 00	5.891E 00
0.5	5.593E-03	1.042E 00	5.000E 00	2.525E 00	8.572E 00
0.6	6.711E-03	1.500E 00	7.200E 00	3.030E 00	1.174E 01
0.7	7.830E-03	2.042E 00	9.800E 00	3.535E 00	1.538E 01
0.8	8.948E-03	2.667E 00	1.280E 01	4.040E 00	1.952E 01
0.9	1.007E-02	3.375E 00	1.620E 01	4.545E 00	2.413E 01
1.0	1.119E-02	4.167E 00	2.000E 01	5.050E 00	2.923E 01

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Table 8. bwR Product as a Function of b for Long (3.0 mm) Back-Electrode Structure. Other Parameters Same as in Table 7. (From Annual Report No. 2).

```
W=  1.0000E 00
BRATIO=  1.0000E 00
RHOCP=  1.0000E-05
RHOBP=  1.5000E-03
DP=  3.0000E-02
HP=  3.0000E-05
T=  3.0000E-01
D=  3.0000E-02
H=  1.2500E-02
```

RHOB= 0.30

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	2.000E-02	3.005E-01	3.633E-01
0.2	2.237E-03	1.667E-01	8.000E-02	6.010E-01	8.499E-01
0.3	3.356E-03	3.750E-01	1.800E-01	9.015E-01	1.460E 00
0.4	4.474E-03	6.667E-01	3.200E-01	1.202E 00	2.193E 00
0.5	5.593E-03	1.042E 00	5.000E-01	1.502E 00	3.050E 00
0.6	6.711E-03	1.500E 00	7.200E-01	1.803E 00	4.030E 00
0.7	7.830E-03	2.042E 00	9.800E-01	2.103E 00	5.133E 00
0.8	8.948E-03	2.667E 00	1.280E 00	2.404E 00	6.360E 00
0.9	1.007E-02	3.375E 00	1.620E 00	2.704E 00	7.710E 00
1.0	1.119E-02	4.167E 00	2.000E 00	3.005E 00	9.183E 00

RHOB= 1.00

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	6.667E-02	1.002E 00	1.111E 00
0.2	2.237E-03	1.667E-01	2.667E-01	2.003E 00	2.439E 00
0.3	3.356E-03	3.750E-01	6.000E-01	3.005E 00	3.983E 00
0.4	4.474E-03	6.667E-01	1.067E 00	4.007E 00	5.744E 00
0.5	5.593E-03	1.042E 00	1.667E 00	5.008E 00	7.722E 00
0.6	6.711E-03	1.500E 00	2.400E 00	6.010E 00	9.917E 00
0.7	7.830E-03	2.042E 00	3.267E 00	7.012E 00	1.233E 01
0.8	8.948E-03	2.667E 00	4.267E 00	8.013E 00	1.496E 01
0.9	1.007E-02	3.375E 00	5.400E 00	9.015E 00	1.780E 01
1.0	1.119E-02	4.167E 00	6.667E 00	1.002E 01	2.086E 01

RHOB= 3.00

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	2.000E-01	3.005E 00	3.248E 00
0.2	2.237E-03	1.667E-01	8.000E-01	6.010E 00	6.979E 00
0.3	3.356E-03	3.750E-01	1.800E 00	9.015E 00	1.119E 01
0.4	4.474E-03	6.667E-01	3.200E 00	1.202E 01	1.589E 01
0.5	5.593E-03	1.042E 00	5.000E 00	1.502E 01	2.107E 01
0.6	6.711E-03	1.500E 00	7.200E 00	1.803E 01	2.674E 01
0.7	7.830E-03	2.042E 00	9.800E 00	2.104E 01	3.288E 01
0.8	8.948E-03	2.667E 00	1.280E 01	2.404E 01	3.952E 01
0.9	1.007E-02	3.375E 00	1.620E 01	2.704E 01	4.663E 01
1.0	1.119E-02	4.167E 00	2.000E 01	3.005E 01	5.423E 01

```
STOP,
?
```

Table 9. Allowed Back-Electrode Spacing, b (mm), for 5, 10, and 20-Percent Efficiency Loss.

Base ρ (ohms-cm)	5% Loss	10% Loss	20% Loss
0.30	3.3	4.8	7.0
1.00	2.2	3.2	4.9
3.00	1.1	1.7	2.8

SILICON-ON-CERAMIC PROCESS COST ANALYSIS (S. B. Schuldt)

Introduction

The cost analysis presented here is applied to: 1) a 1977 "baseline" set of parameters, 2) a conservatively projected set of parameters, corresponding roughly to the year 1982, and 3) an optimistic set of parameters (for the year 1986).

The analysis is for a factory which puts the silicon only on panels. The method is to draw one face of the panel across and in the direction perpendicular to a line surface of molten silicon. The panel face is precoated with carbon which acts as a wetting agent. If the pulling speed and temperature profiles are correct, the silicon solidifies as a uniform film on the panel. Argon is used to provide an inert atmosphere. As indicated in Figure 16, the important raw materials are assumed to be (1) precut, packaged ceramic panels, (2) polycrystalline silicon, (3) carbon, and (4) argon. Factory output is repackaged, coated panels. As evident from Figure 16, there is no direct space-time link with other solar-cell processing steps, such as P-N junction formation, antireflective (AR) coating, and metalization. It is recognized that the product of this factory corresponds roughly to the Task 2 objective. This means that, based on an annual production of 5 million m^2 of coated panels, the 1986 projected added value should not exceed $10/$m^2$ in 1975 dollars.

Factory-Size Scaling Considerations

A best-case, worst-case scenario approach was used to define limits on production and plant equipment, factory area, and direct/indirect labor. A basic assumption was that the main production unit, or coating station, handles roughly 8 ft (240 cm) of total panel width, regardless of the width of individual panels. Unit throughput, in area per unit time, is therefore proportional to this total width times pull rate. Assuming three-shift operation and taking plant efficiency (E) and average yield (Y) factors into account, we can formulate the Unit Annual Productivity as:

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$$UAP = (2 \cdot 4) \cdot (0.01R) \cdot (31.5 \times 10^6)(E \cdot Y)\ m^2/year \quad (4)$$

where the pull rate, R, is expressed in cm/sec. The number of production units required by our hypothetical factory is then

$$\text{No. of Production Units} = 5 \times 10^6/UAP \quad (5)$$

If the efficiency-yield product is about 0.8, Equation (5) reduces to a simple rule of thumb, namely

$$\text{No. of Production Units} = 8/R \quad (6)$$

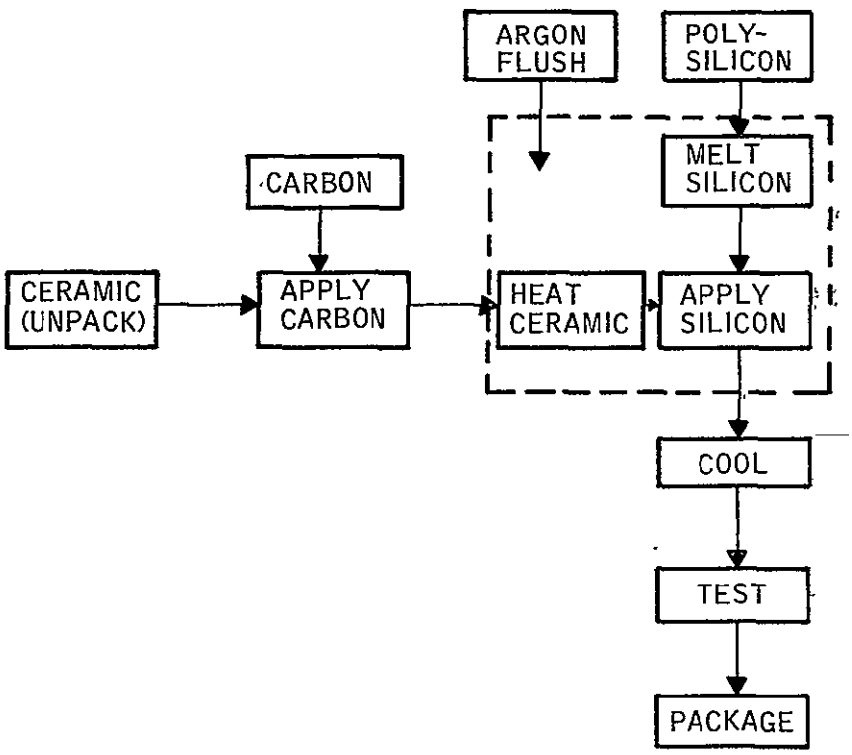

Figure 16. Silicon-on-Ceramic Production Flow Diagram

The as-yet undetermined factory size obviously is critically dependent on the pull rate, R. To accommodate a tenfold uncertainty (0.1 to 1.0 cm/sec) in the achievable R, it was decided that at least two scenarios were needed (Figure 17), since a factory plan

containing 80 production units would require a different kind of thinking than one containing only eight. Separate operating cost analyses were therefore made, according to the groupings shown in Table 10, for an eight-unit (best-case, R = 1.0) factory and an 80-unit (worst-case, R = 0.1) factory. As might be expected, it was found that most labor and capital requirements do not scale proportionately to the number of production units. For example, more workers would be required per machine for the fast rate than for the slow rate; also, because of relatively fixed space overhead, the large plant is not 10 times as large and expensive as the small plant. Moreover the burden rates, expressed as a percentage of direct labor, are different for the two cases.

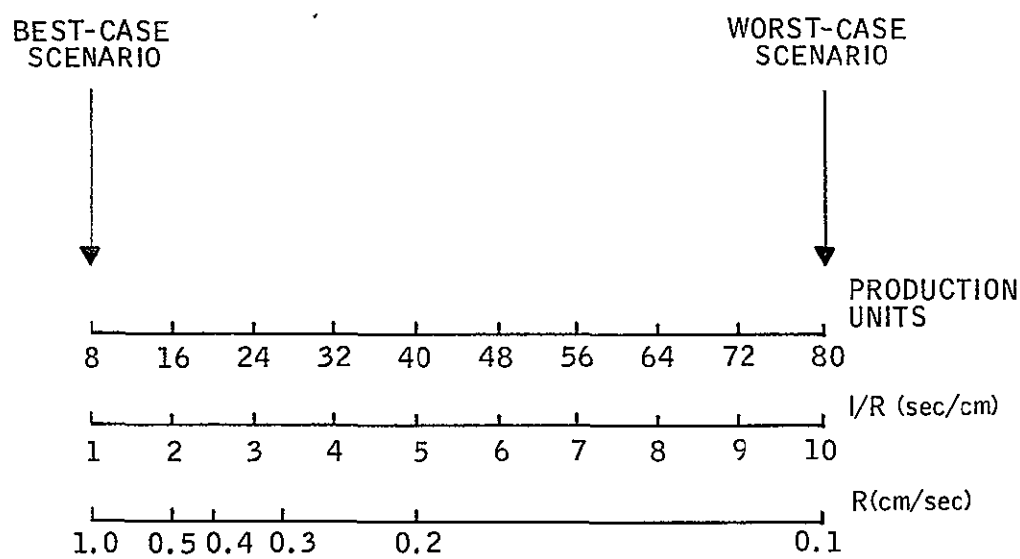

Figure 17. 1/R Scale for Linear Interpolation Between Best-Case and Worst-Case Scenarios

Intermediate Situations

For a pull rate in the range $0.1 < R < 1.0$, the R-sensitive costs are determined by linear interpolation with respect to the number of production units, using the best-case and worst-case costs as endpoints. If, for example, B_0 and B_1 are the costs of the smallest and largest buildings, respectively, then the building cost for a pull rate, R, is:

$$B_R = B_0 + (B_1 - B_0)\,(8/R - 8)\,/72 \qquad (7)$$

Table 10. Major Cost Groups Used in Scaled-Up Economic Analysis

Major Cost Group	Cost Item/Center
Capital equipment	• Building • Production equipment • Plant equipment
Materials and electric power	• Ceramic substrate • Polysilicon • Carbon • Argon • Power
Direct labor	• Production • Engineering • Inspection
Burden	• Indirect labor and salaries • Supplies and services • Department management and production planning • Allocation based on headcount, wages and salaries • Other allocations
General and administrative	---
Profit	---

Amortization of Capital

Capital costs are reduced to an annual basis by dividing purchase price by useful life, in years, and adding interest on debt. Useful life is assumed to be 20 years for the building, 7 years for production equipment, and 12 years for plant equipment.

Direct Materials and Electric Power

Direct material costs are insensitive to pull rate with the exception of argon, which is lost by constant-velocity seepage from each of the production units. Large quantities of electrical power (up to several hundred kVA) are required to heat the ceramic substrates and to heat and melt the silicon, not to mention capital costs of up to 1 million dollars to provide the electrical service. However, at normal utility rates, the total electric costs do not contribute significantly to the price or added value of the product.

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Computer Model

For systematic prediction of added value and selling price over a spectrum of uncertain factors, a computer program called ECOMOD is used. The primary input to the program is the following list of variables:

- Production unit price ($/each)
- Ceramic cost (m^2)
- Argon cost ($/100 ft^3)
- Pull rate (cm/sec)
- Silicon coat thickness (μm)
- Substrate thickness (cm)
- Electric rate (cents/kWh)
- Polysilicon cost ($/kg)

The other numbers, derived from the scenario exercises, are built into ECOMOD as data statements, as are the thermal constants and other physical data. Program output includes: (1) a partial cost breakdown, according to the major categories of Table 11, reduced to 1976 dollars/m^2, (2) added value and price per m^2, and (3) sensitivity information. The last gives incremental changes in added value and price with respect to small changes in each of the input variables.

Where We Stand "Now" and "Tomorrow"

ECOMOD calculations were made for a "baseline" case, a pessimistic projection, and an optimistic projection. In all three cases, three of the input variables were fixed as follows:

- Production units at $100,000 each
- Substrate thickness = 0.25 cm
- Electric rate = 4 cents/kWh

Three different polysilicon costs are used ($55, $25, and $10/kg) to compute selling prices (Tables 11, 12, and 13) but one particular value per case is assumed in the sensitivity profiles. (Figures 18, 19, and 20.) The three cases are discussed in more detail, next.

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Table 11. Baseline Case (Honeywell Corporate Technology Center Cost Analysis for Coating Silicon on Ceramic. Latest Revision 18 November 1977)

THIS ANALYSIS ASSUMES AN ANNUAL PRODUCTION OF 5.0 MILLION SQUARE METERS OF SI-COATED CERAMIC AND IS BASED ON THE FOLLOWING INPUT DATA:

8-FOOT COATING UNITS	100000.	$ EACH
SILICON	55.00	$/KG
CERAMIC	5.00	$/SQ M
ARGON	3.75	$/100 CU FT
RECIPROCAL PULL RATE	20.00	SEC/CM
SI THICKNESS	200.	MICRONS
SUBSTRATE THICKNESS	0.25	CM
ELECTRIC RATE	4.00	CENTS/KWH

NUMBER OF COATING UNITS REQUIRED IS 160

COST BREAKDOWN IN DOLLARS/SQ M:

CAPITAL INSTALLATION		
BUILDING	0.112	
PRODUCTION EQUIPMENT	0.586	
PLANT EQUIPMENT	0.059	
		0.757
DIRECT LABOR		
PRODUCTION	4.641	
PRODUCTION ENGINEERING	0.087	
INSPECTION	0.076	
		4.805
BURDEN OVERHEAD		9.379
DIRECT MATERIALS		
SILICON	-----	
CERAMIC	5.450	
CARBON	0.230	
ARGON	6.415	
		12.095
ELECTRIC POWER		0.338
FACTORY COST (SUBTOTAL)		27.376
GEN. & ADM.		4.928
TOTAL COST		32.303
PROFIT		4.845
ADDED VALUE		37.149

ADD POLY SI AT - - - - - - - -	$10.00/KG	$25.00/KG	$55.00/KG
PRICE $/SQ METER SOC	44.041	54.380	75.059
CENTS/WATT AT 10% EFFIC	44.0	54.4	75.1

Table 12. Pessimistic Projection (Honeywell Corporate Technology Center Cost Analysis for Coating Silicon on Ceramic. Latest Revision 18 November 1977)

THIS ANALYSIS ASSUMES AN ANNUAL PRODUCTION OF 5.0 MILLION SQUARE METERS OF SI-COATED CERAMIC AND IS BASED ON THE FOLLOWING INPUT DATA:

8-FOOT COATING UNITS	100000.	$ EACH
SILICON	25.00	$/KG
CERAMIC	5.00	$/SQ M
ARGON	2.00	$/100 CU FT
RECIPROCAL PULL RATE	10.00	SEC/CM
SI THICKNESS	150.	MICRONS
SUBSTRATE THICKNESS	0.25	CM
ELECTRIC RATE	4.00	CENTS/KWH

NUMBER OF COATING UNITS REQUIRED IS 80

COST BREAKDOWN IN DOLLARS/SQ M:

CAPITAL INSTALLATION		
BUILDING	0.059	
PRODUCTION EQUIPMENT	0.310	
PLANT EQUIPMENT	0.030	
		0.399
DIRECT LABOR		
PRODUCTION	2.766	
PRODUCTION ENGINEERING	0.056	
INSPECTION	0.049	
		2.872
BURDEN OVERHEAD		4.516
DIRECT MATERIALS		
SILICON	-----	
CERAMIC	5.450	
CARBON	0.230	
ARGON	1.711	
		7.391
ELECTRIC POWER		0.224
FACTORY COST (SUBTOTAL)		15.401
GEN. & ADM.		2.772
TOTAL COST		18.173
PROFIT		2.726
ADDED VALUE		20.899

ADD POLY SI AT - - - - - - - -	$10.00/KG	$25.00/KG	$55.00/KG
PRICE $/SQ METER SOC	26.068	33.823	49.331
CENTS/WATT AT 11% EFFIC	23.7	30.7	44.8

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Table 13. Optimistic Projection (Honeywell Corporate Technology Center Cost Analysis for Coating Silicon on Ceramic. Latest Revision 18 November 1977)

THIS ANALYSIS ASSUMES AN ANNUAL PRODUCTION OF 5.0 MILLION SQUARE METERS OF SI-COATED CERAMIC AND IS BASED ON THE FOLLOWING INPUT DATA:

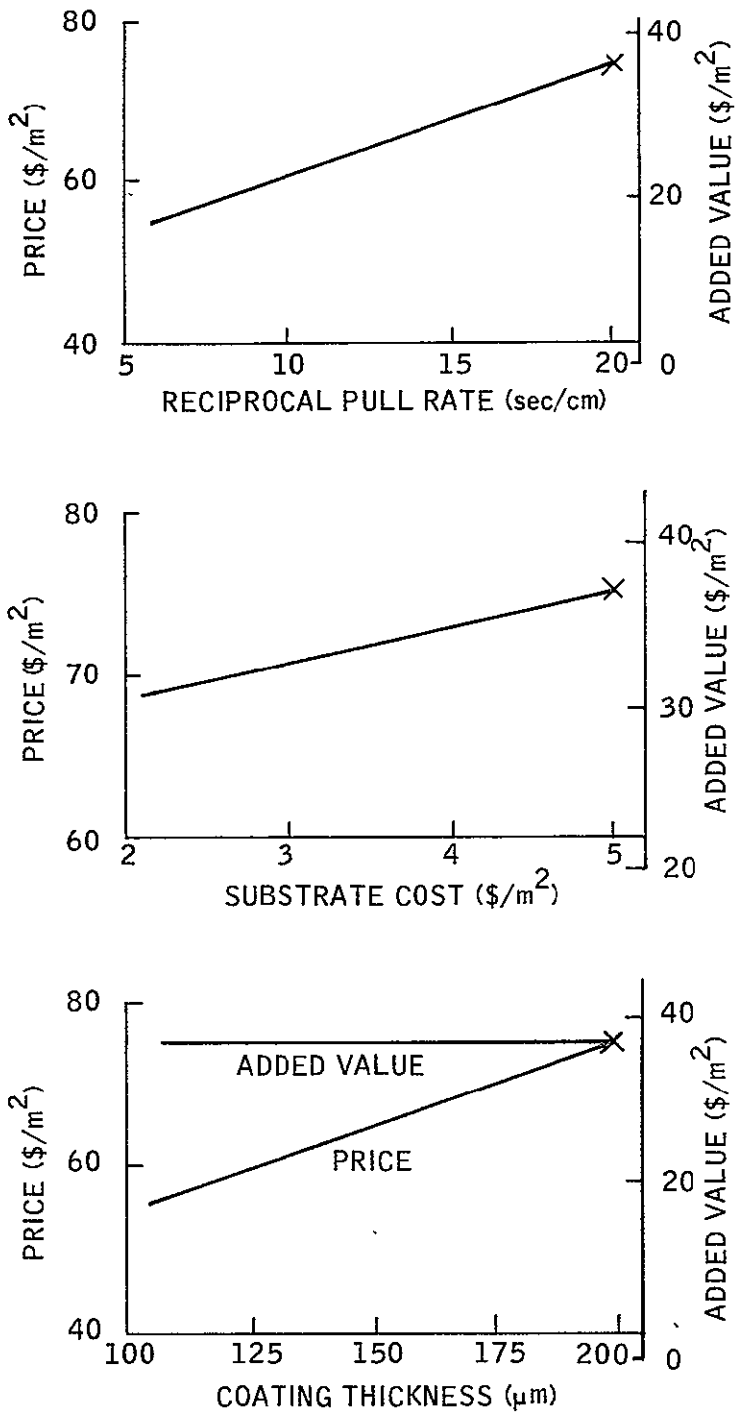
8-FOOT COATING UNITS	100000.	$ EACH
SILICON	10.00	$/KG
CERAMIC	2.00	$/SQ M
ARGON	2.00	$/100 CU FT
RECIPROCAL PULL RATE	1.00	SEC/CM
SI THICKNESS	100.	MICRONS
SUBSTRATE THICKNESS	0.25	CM
ELECTRIC RATE	4.00	CENTS/KWH

NUMBER OF COATING UNITS REQUIRED IS 8

COST BREAKDOWN IN DOLLARS/SQ M:

CAPITAL INSTALLATION		
BUILDING	0.010	
PRODUCTION EQUIPMENT	0.062	
PLANT EQUIPMENT	0.004	
		0.076
DIRECT LABOR		
PRODUCTION	1.079	
PRODUCTION ENGINEERING	0.028	
INSPECTION	0.025	
		1.131
BURDEN OVERHEAD		1.392
DIRECT MATERIALS		
SILICON	-----	
CERAMIC	2.180	
CARBON	0.230	
ARGON	0.171	
		2.581
ELECTRIC POWER		0.120
FACTORY COST (SUBTOTAL)		5.300
GEN. & ADM.		0.954
TOTAL COST		6.254
PROFIT		0.938
ADDED VALUE		7.192

ADD POLY SI AT - - - - - - - -	$10.00/KGM	$25.00/KGM	$55.00/KG
PRICE $/SQ METER SOC	10.638	15.808	26.147
CENTS/WATT AT 12% EFFIC	8.9	13.2	21.8



"BASELINE" CASE

PULL RATE 0.05 cm/sec
SUBSTRATE COST $5/m2)
SILICON THICKNESS 200 μm
POLYSILICON COST $55/kg
ARGON $3.75/100 ft3

Figure 18. Sensitivity Profiles for Baseline Case

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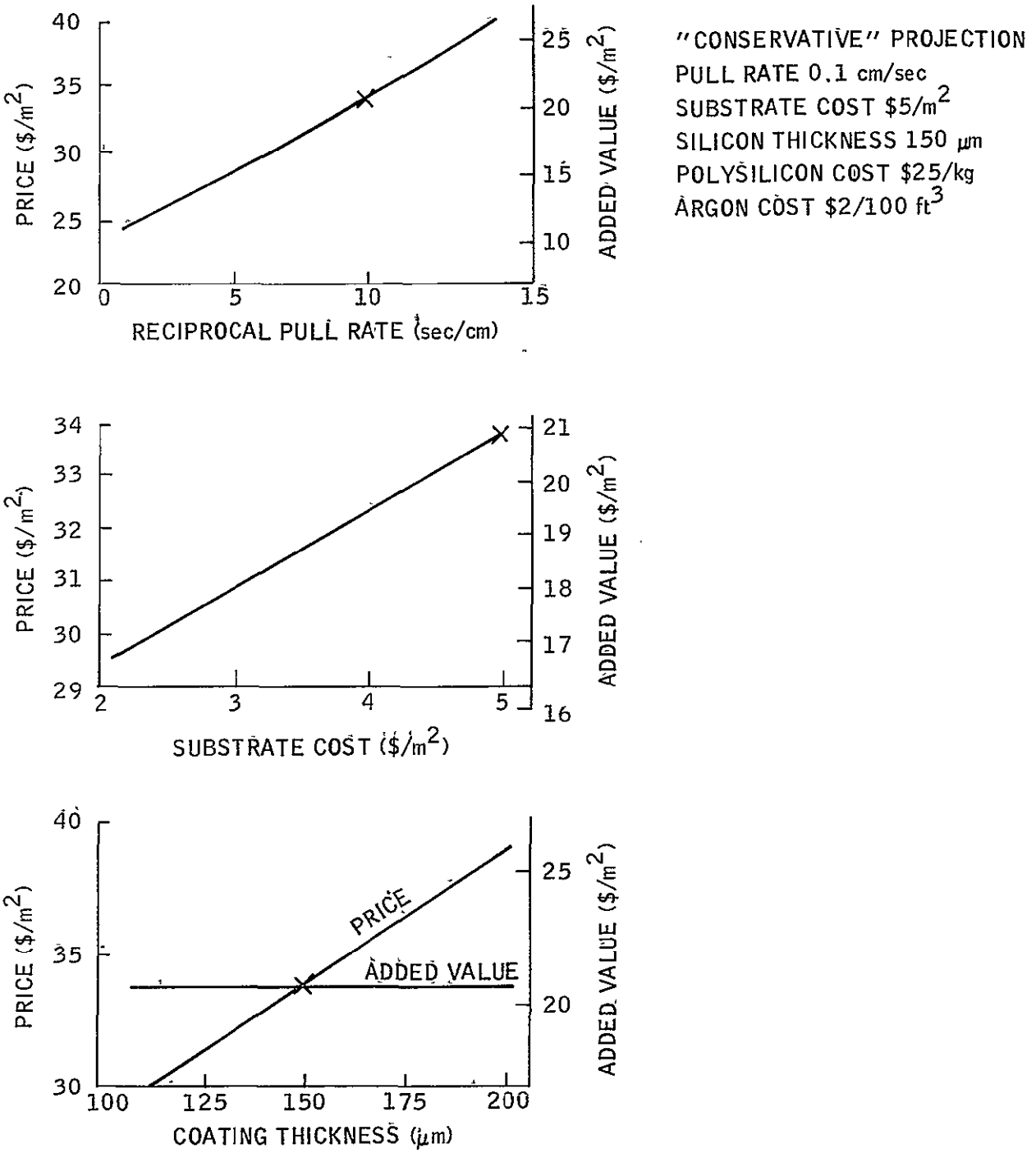
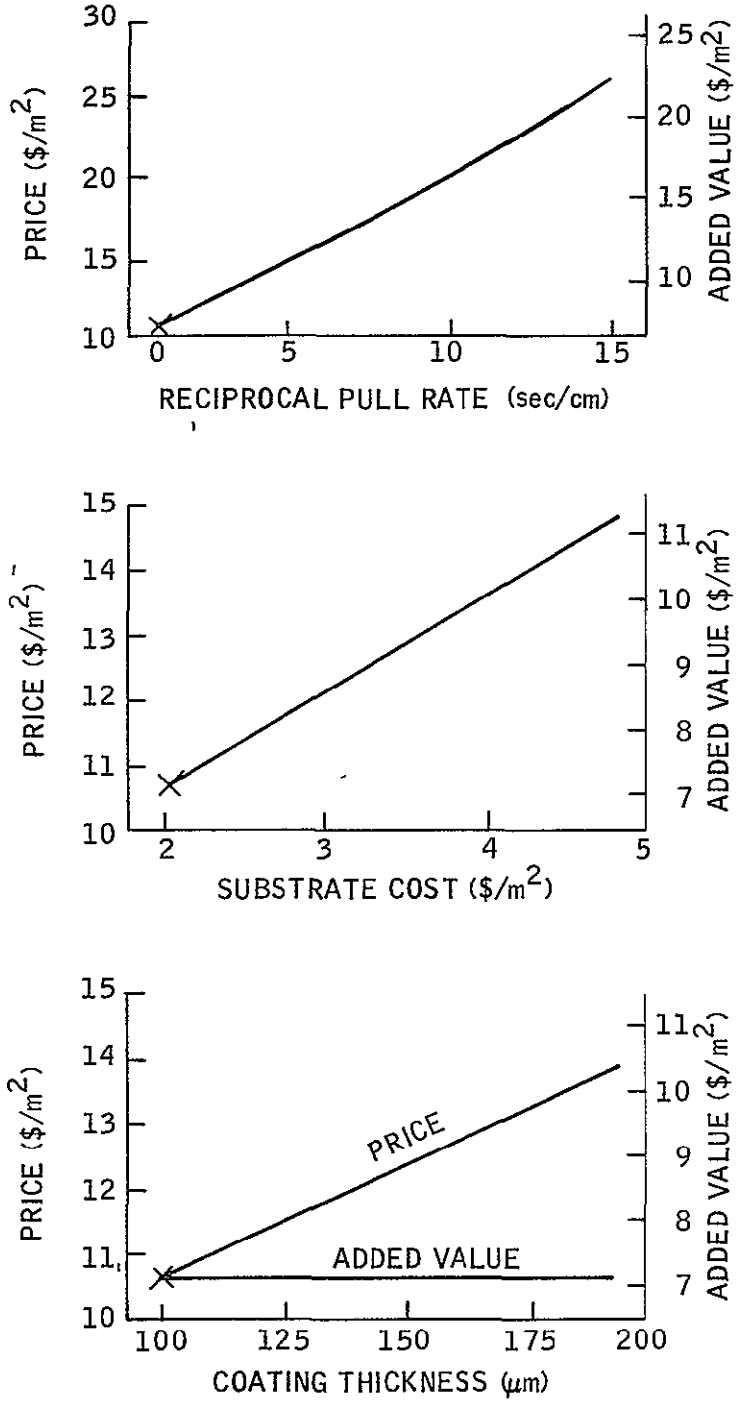


Figure 19. Sensitivity Profiles for Conservative Case



"OPTIMISTIC" PROJECTION
PULL RATE 1.0 cm/sec
SUBSTRATE COST $2/m^2$
SILICON THICKNESS 100 μm
POLYSILICON COST $10/kg
ARGON COST $2/100 ft^3$

Figure 20 Sensitivity Profiles for Optimistic Projection

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Baseline Case--This calculation assumes, in addition to the above,

- Ceramic = $\$5/m^2$
- Argon = $\$3.75/100\ ft^3$
- Pull rate = 0.05 cm/sec
- Silicon thickness = 200 μm
- Silicon cost = $55/kg (for sensitivity profiles)

Quotes are used for two reasons. First, the cost of ceramic panels is as yet undefined, with $\$5/m^2$ being near the high end of estimates from potential vendors. The other figures, except for the price of the production unit, are well known. The second reason is that the present pulling rate represents 160 production units, which is a rather severe extrapolation of the scenario data. It is particularly for this reason that the baseline results (Table 11 and Figure 18) should be interpreted cautiously. However, it seems safe to conclude that the goal of $\$10/m^2$ (added value) will not be met according to the present parameters.

Pessimistic Projection Case--This calculation is based on the following numbers·

- Ceramic = $\$5/m^2$
- Argon = $\$2/100\ ft^3$
- Pull rate = 0.1 cm/sec
- Silicon thickness = 150 μm
- Silicon cost = $25/kg (for sensitivity profiles)

Although the added value figure has been cut almost 50 percent from $37.15 to $20.90, it is still unlikely that the $10 target could be achieved. The sensitivity profiles (Figure 19) indicate that improvements would have to be made in more than one of the parameters to reach the $10 goal.

Optimistic Projection Case--The numbers used for the final example are:

- Ceramic = $\$2/m^2$
- Argon = $\$2/100\ ft^3$
- Pull rate = 1.0 cm/sec
- Silicon thickness = 100 μm
- Silicon cost = $10/kg (for sensitivity profiles)

In this case, the $7.19 calculated added value surpasses the $10 goal by a comfortable margin. Some idea of the tolerances provided by this margin may be shown as follows:

1) The added value becomes $10 if the pull rate is reduced to 0.25 cm/sec while other input variables remain unchanged.

2) The added value becomes $10 if the substrate cost is increased to $3.90/$m^2$ while other input remains unchanged.

General Conclusions

The cost calculations performed by ECOMOD are as accurate or inaccurate as the scenarios upon which they are based. Whatever their credibility, the computer printouts for the "now" and "tomorrow" cases all show that direct materials (excluding silicon) and labor/burden contribute almost equally to the added value of silicon on ceramic, whereas capital costs and electric power costs are relatively unimportant. The "now" case is hopeless in terms of reaching the $10/$m^2$ goal. The pessimistic projection is considerably better but still would require improvements in two or more cost-sensitive parameters to achieve the goal. The optimistic projection meets the goal with room to spare.

Comparison With JPL Interim Method

An alternate price estimation procedure was followed according to JPL's "Interim Price Estimation Guidelines: A Precursor and an Adjunct to SAMIS III Version 1," 10 September 1977. The price formula is simply:

$$\text{Price} = (0.49 * \text{EQPT} + 97. * \text{SQFT} + 2.1 * \text{DLAB} + 1.3 * \text{MATS} + 1.3 * \text{UTIL})/\text{QUAN}$$

where Price is in $/$m^2$, and the quantities EQPT, SQFT, DLAB, MATS, UTIL, and QUAN are defined in the handbook. JPL Figure 10 gives the input data and results as applied to our process, including the ECOMOD price estimates for comparison. The agreement is remarkable considering the wide differences in approach between the two methods.

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CONCLUSIONS

From the work performed during the quarter, we conclude that:

- The cost calculations performed by ECOMOD are as accurate or inaccurate as the scenarios upon which they are based. Whatever their credibility, the computer printouts for the "now" and "tomorrow" cases all show that direct materials (excluding silicon) and labor/burden contribute almost equally to the added value of silicon on ceramic, whereas capital costs and electric power costs are relatively very unimportant. The "now" case is hopeless in terms of reaching the $\$10/m^2$ goal. The pessimistic projection is considerably better but still would require improvements in two or more cost-sensitive parameters to achieve the goal. The optimistic projection meets the goal with room to spare.

- There is remarkable agreement in the results between Honeywell's ECOMOD analysis method and JPL's Interim method considering the wide differences in approach between the two methods.

- When EFG silicon ribbons are used to seed dip-coated layers, the resulting growth is definitely influenced in a positive manner. Single-crystal regions more than 0.5 cm in width have been produced.

- The alcohol used to dilute the Dag when carbonizing substrates was causing the silicon coating to blister due to the absorption of moisture prior to dip coating. A method for preventing this difficulty was found.

- The adhesion of the silicon coating to the substrate is sufficiently good to cause fractures in the coating when separation of the silicon from the substrate is attempted.

- If slotted substrates are used to electrically contact the base layer of an SOC cell, the slots should be flared from the back side, for access purposes, and silicon should not be allowed to deeply penetrate the slot. This minimizes the use of silicon and reduces the series-resistance problem.

- Smooth, continuous silicon coatings can successfully be applied to slotted substrates.

- Since no noticeable differences were evident in the microstructures of substrates examined from three different mullite batch lots, it is suspected that their differences in thermal-shock resistance are due to differences in the density and size of larger flaws (e.g., surface folds due to the rolling operation).

- The substrate breakage problem prior, during, and after the dip-coating procedure appears to result from variations in the moldability of the clay when it is being rolled into coupons.

- The critical quench temperature of most of the substrates tested lies in the same range, namely 275° to 350°C. Unfortunately, the mullite substrates originally used were never examined.

- The borosilicate glass which was added to the carbon coating on the substrate is simply diffusing into the silicon melt during dip coating.

- Neither the installation of the new PH_3 furnace nor the modifications in the processing procedure appear to have noticeably improved the cell performance.

- The lower values of efficiencies obtained in SOC samples made during the quarter strongly suggest an unidentified source of impurities in the silicon coating system.

- Using a scanned light beam (LBIC) and measurements of spectral response with a highly-focussed light beam, the diffusion length, L_n, within grains can be determined as well as effective L_n at grain boundaries. This technique may be useful in identifying the cause of the decreased efficiency in recently made cells.

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RECOMMENDATIONS

To date, the dip-coating apparatus has been used for the following two functions:

1) To provide the solar-cell program with adequate quantities of usable coated substrates.

2) To serve as an experimental coater in an effort to better understand growth parameters and to explore methods for increasing the coating rate.

The latter function requires the machine to be constantly modified in order to accomplish the program's goals. Unfortunately, such modifications cannot only contribute new impurities being introduced into the system, but also occasionally upset growth conditions which are conducive to producing usable silicon coatings.

We therefore recommend that the dip coater be thoroughly cleaned and henceforth used solely for providing usable silicon coatings to the program. To fulfill the other program goals, a new, more-versatile dip coater should be designed and built using the technology and experience gained from the original coater.

NEW TECHNOLOGY

There were no reportable "New Technology" items uncovered during the reporting period.

PROJECTION OF FUTURE ACTIVITIES

Future activities are projected as follows:

- The seeded growth using EFG ribbons will continue

- Adhesion tests of silicon to the ceramic will be made using normally grown films. Success will depend on the strength of the silicon-epoxy bond needed for this experiment

- Work on evaluating the strength of ceramics and the reason for occasional breakage during dip coating will continue

- The operation of the SCIM coater will begin now that the proper power supplies have been received and the modifications are nearly completed

- We plan to expand activity in the area of device fabrication An additional scientist, Dr B. Grung, has been hired and will begin working during the next quarter. This will permit a greater number of devices to be fabricated from SOC layers grown under a variety of conditions

- LBIC work will be used to measure diffusion lengths within crystals and at grain boundaries in an attempt to clarify more about the nature of the contaminating impurities

- Experiments to improve the conductivity of the silicon-carbon interface will continue The search for a low-cost, boron-doped, impermeable carbon coating will continue.

- Solar cells will be made on SOC materials on slotted substrates. The device models of cells on slotted substrates will be correlated with the actual performance.

- The device modeling effort will be expanded to include the effects of microscopic device parameters on the device performance

- The ECOMOD program for the economic analysis will be modified as needed and will be exercised with updated input parameters as they become available.

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PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 21, 22, and 23.

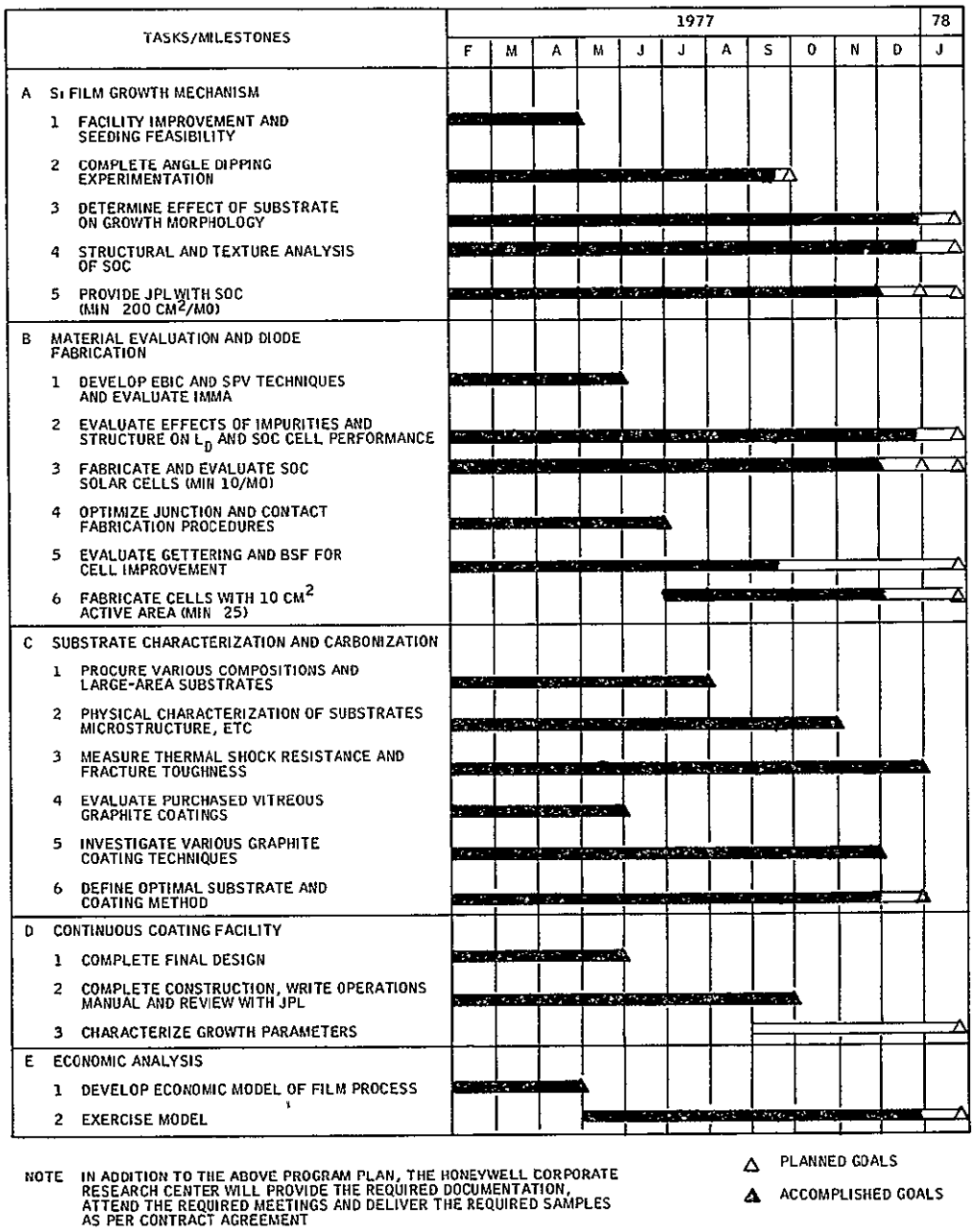

Figure 21. Updated Program Plan

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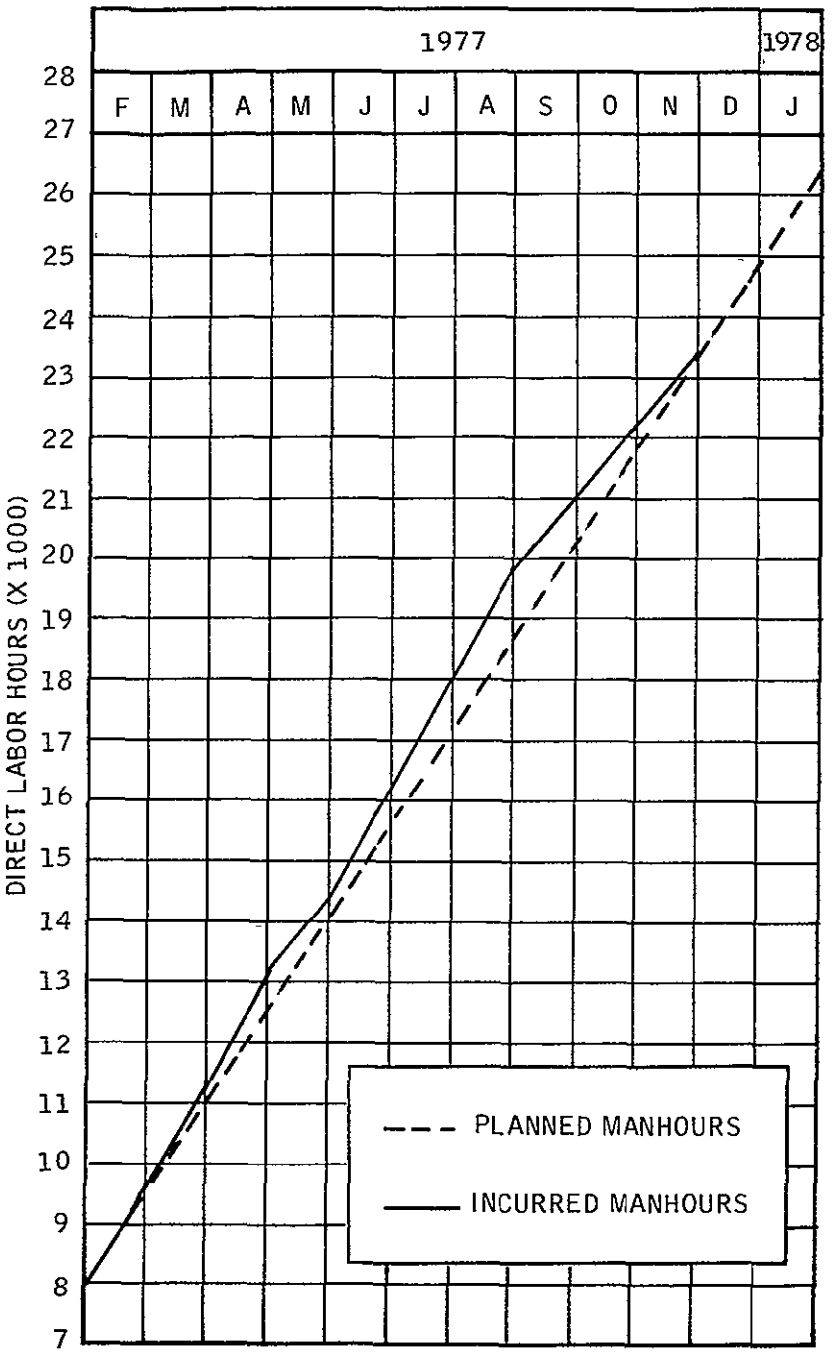

Figure 22. Updated Program Labor Summary

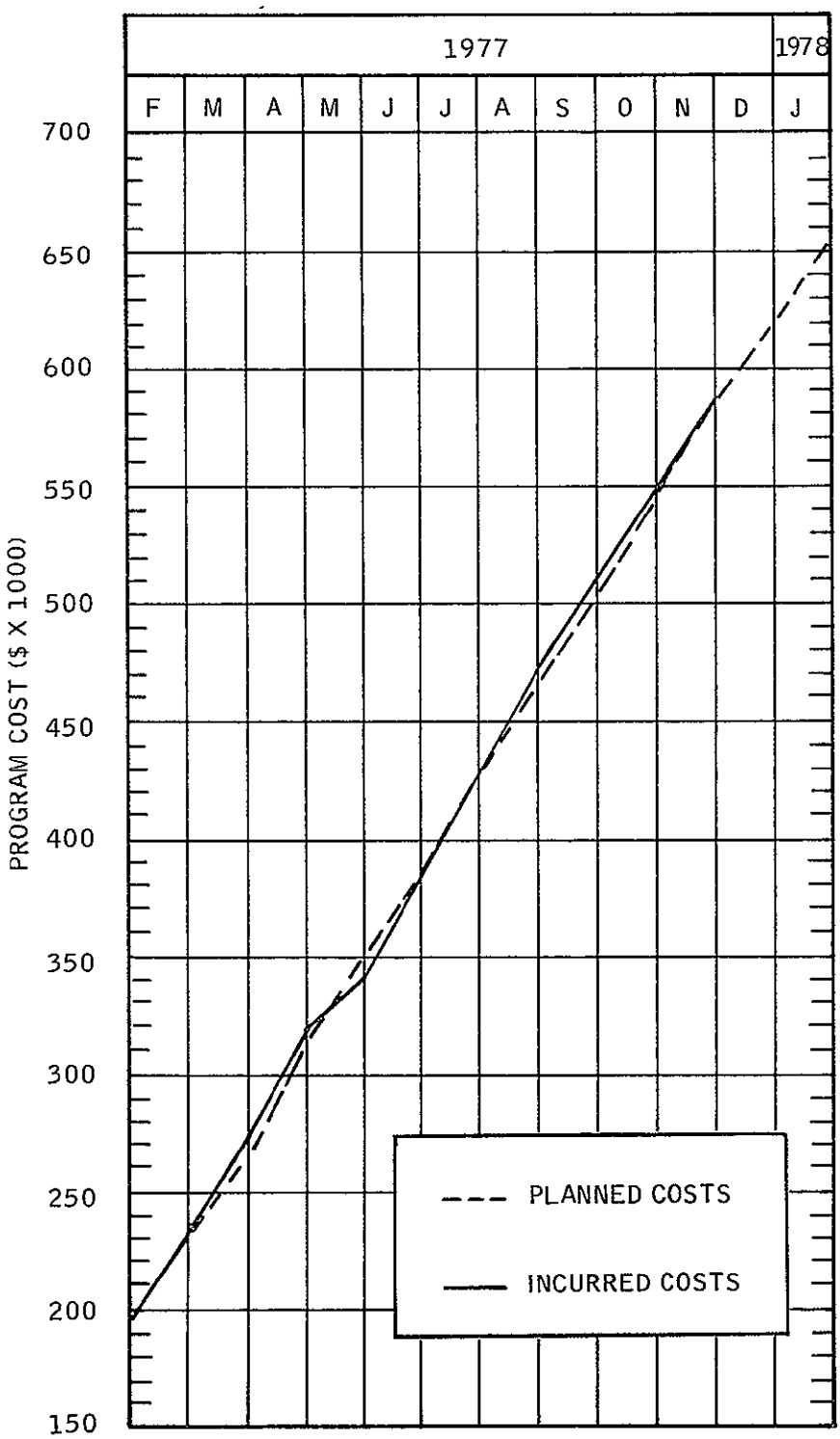

Figure 23. Updated Program Cost Summary

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