

TECHNICAL MEMORANDUM (NASA) 58

Temp. 78-23327
N78-26122

A VIDEO DISPLAY INTERFACE FOR THE
LORAN-C NAVIGATION RECEIVER DEVELOPMENT SYSTEM

A character-mode video unit is described which allows microprocessor-controlled display of program and navigation data with a small investment in logic.

by

Joseph P. Fischer
Robert W. Lilley

Avionics Engineering Center
Department of Electrical Engineering
Ohio University
Athens, Ohio 45701

May 1978

Supported by

National Aeronautics and Space Administration
Langley Research Center
Hampton, Virginia

Grant NGR 36-009-017

I. INTRODUCTION

As a part of the NASA Joint University Program in Air Transportation Systems, Ohio University project personnel have designed and fabricated a microprocessor-based development system for prototype test of navigation receiver designs. [1] During use of this system in the development of low-cost LORAN-C receiver/processor concepts, the limitations of the integral KIM-1 display were severely felt. It was to augment this numerical display that the video character display was produced.

The circuit design presented later in this paper meets the need for a flexible-format display capable of driving a small standard video monitor with only minimal demands upon microprocessor memory and MPU cycles.

II. OBJECTIVES

- A. Provide full ASCII 64-character set display in large-character format (double-scan in X and Y for visibility).
- B. Provide as many characters on screen as consistent with good viewability, but not less than 10 lines by 20 characters.
- C. Design should incorporate integral and refresh circuitry memory, to minimize computing load of host processor.
- D. Design must not depend upon external 60 Hz power-line frequency reference for video monitor horizontal and vertical timing, since airborne use is contemplated.
- E. Circuit must interface directly to a KIM-1 or equivalent microcomputer data and address bus.
- F. Screen read function is not required.
- G. Use standard components, and simplify design wherever possible for minimum cost.

III. CIRCUIT DESCRIPTION

Figure 1 shows a block diagram for the video interface. The unit is seen to be a rather standard design, using a crystal clock counted down to video horizontal and vertical frequencies. "Coarse sync" pulses are produced by monostable multivibrator timing circuits, and the final sync pulses are formed by synchronizing the coarse sync with the system clock. In this manner, the edges, top and bottom of the monitor display are forced to occur at appropriate times; namely at character or character line beginning or end. This method avoids partial characters and character lines in the display, and tends to stabilize the entire display through crystal control of sync.

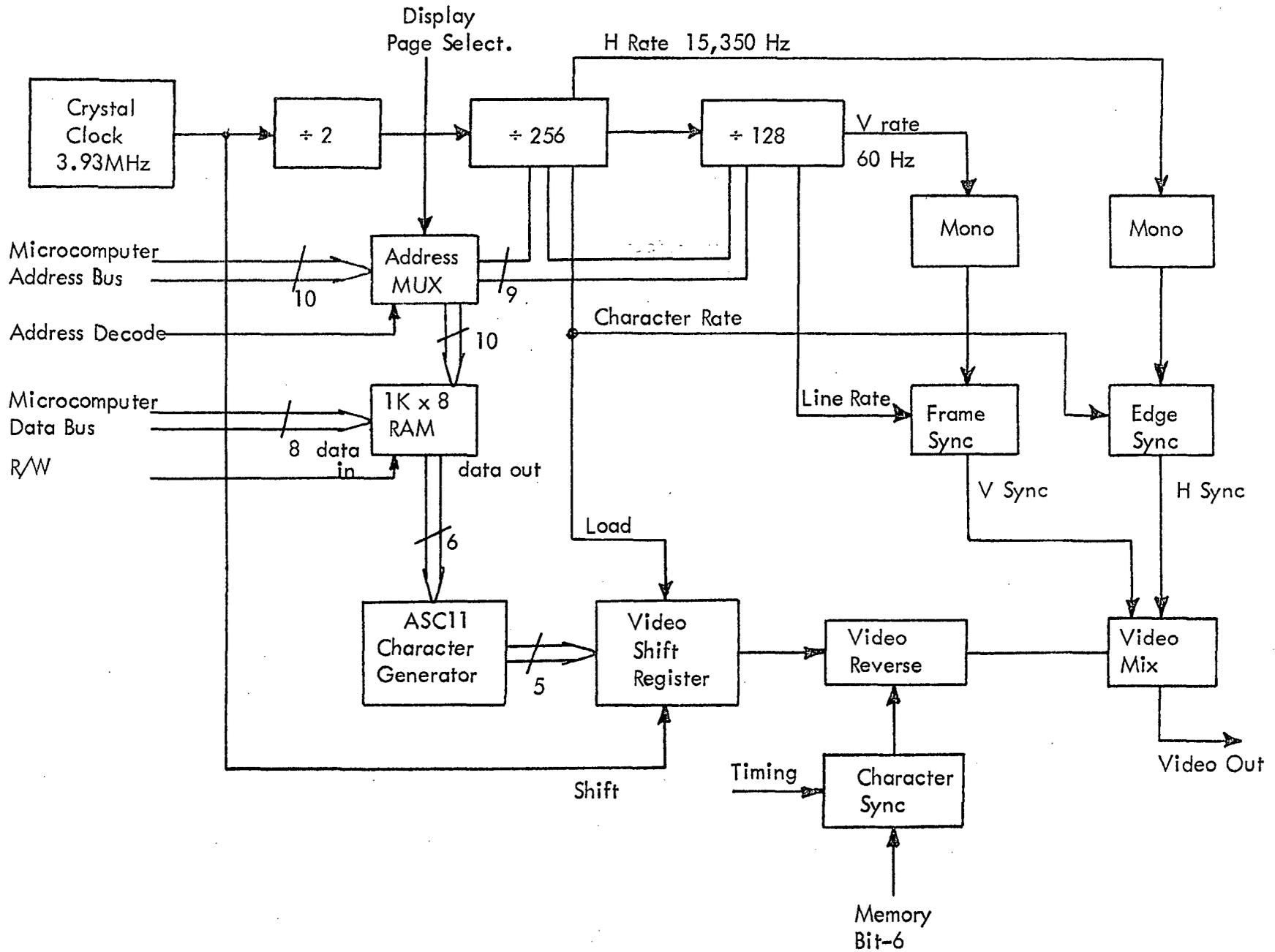


Figure 1. Video Interface Block Diagram.

Composite video is generated using a CMOS quad bilateral switch to blank video pulses during horizontal and vertical sync, and a resistor network to produce correct video levels for sync, black and white display.

Low-cost RAM memory provides the data storage medium for the unit, with its address lines shared by the display refresh counters and the microcomputer address bus. Multiplex control is effected by the address decode output, handing display memory address lines to the microcomputer whenever it needs to write to the display memory. In display mode, the memory addresses are cycled by the display counters, and six memory data outputs are sent to the standard character generator ROM. Video dot output is serialized by the shift register, and sent to the video reverse circuitry, which also receives memory bit 6 as character field control.

It will be noted that the crystal frequency has been chosen so that a simple binary countdown results in the 60 Hz vertical rate. The horizontal and vertical sync pulses are "overlaid" into this counter interval, resulting in some memory locations being addressed during sync intervals. It was found that such a design resulted in sufficient characters being displayed to meet the circuit objectives, reduced the video bandwidth required, and simplified the circuit.

IV. DETAILED DESCRIPTION OF VIDEO INTERFACE

The characters to be displayed are stored in the on-board memory. This memory consists of 1024 x 8 bytes of static read-only-memory (RAM). The memory is available to the counter circuitry most of the time. However, the decoding circuitry will respond when it "sees" address (hex) 2XXX, in which case, the microprocessor gains access to the memory. During this time, the microprocessor may write data into any of the locations. Insofar as the microprocessor is concerned, the memory appears no different than any other random access memory; however, the microprocessor has write-only access.

During periods when the microprocessor does not have the display memory accessed, the counter circuitry sequentially steps through the memory, and the data from the appropriate location is converted to a character which is then sent to the video display. An on-board option specifies that the counters will count through only the first 512 locations or the second 512 locations. Thus, two screen patterns may be stored in the display memory. The format of the video display yields 20 rows of 32 columns, some of which are not displayed and are used as blanking for synchronization.

The counting circuits are stabilized by a crystal-controlled clock operating at 3.93 MHz. The output of the clock is divided by two and then routed to two dual binary up-counters connected in series. Each counter is connected in a fashion such that each provides division by 256 with the intermediate power-of-two frequencies available. These intermediate signals are used to drive the address lines for the memory. Before these signals actually get to the memory address bus, they are sent to solid-state switches which determine if the memory is being addressed by the counters or the microprocessor.

Aside from selecting memory addressing, the counters also provide the timing signals for the synchronization circuit. The purpose of this circuit is to provide the synchronizing pulses for both the vertical and horizontal retrace intervals. Since both the vertical and horizontal scan rates are derived from the same base frequency, both are exact multiples of each other and assure a stable display. The vertical scan rate is the standard 60 Hz and the horizontal is 15720 Hz; this is due to the fact that a 262 non-interlaced line format is used. The width of the synchronization pulse for both vertical and horizontal may be adjusted for the particular monitor in use. It has been found that a width of a 4-6 μ s for horizontal and 100-500 μ s for the vertical work well. Careful note should be made that these are synchronization pulses only; a blanking interval must be provided by software. This is especially true for the vertical retrace interval; the pulse width must be kept short to keep the horizontal oscillator from drifting too far, and some vertical blanking must be included to allow the oscillator to settle down^[1] before character display begins in each frame.

As each memory location is selected, the contents of that location appear on the data bus. This data is assumed to be an ASCII character and is sent to the character generator.^[2] It should be noted that inputs A1, A2, and A3 provide selection of one of eight rows (see Figure 2) and inputs A4 through A9 provide selection of one of 64 matrix characters. The matrix characters are selected by the memory data bus and the rows are clocked by the counter circuitry. The output, then, consists of five dots which represent an entire row of the character matrix.

Each of the aforementioned rows is clocked into a parallel in/serial out shift register.^[3] Inputs A, G, and H of the shift register are tied low; this provides one blank dot before each character and two blank dots after. The clock inputs to the shift register and the timing of the row selectors to the character generator are chosen to provide the top row of dots for each of the 20 characters on screen to be displayed, then the second row, and so on down to the eighth row. Notice the top row for each character is blank to provide vertical spacing between characters. An ex-or gate is used to reverse the video background for each character as determined by the data bus bit six. If bit six is high, the background is white and if bit six is low, the background is black.

Up to this point, three signals are available: the horizontal and vertical synchronization pulses and the video dot information. These three signals are combined by a quad bilateral switch^[4](Figure 3). The divider resistors shown are chosen to provide the proper video levels. The final product now contains the character information along with the retrace synchronization pulses and is ready to be sent to the video monitor.

Additional logic has been included to force the dot information to the black (ground) level during the times the microprocessor has access to the video memory. This prevents glitches from appearing on screen while the microprocessor is loading memory and the rest of the display circuit is still running.

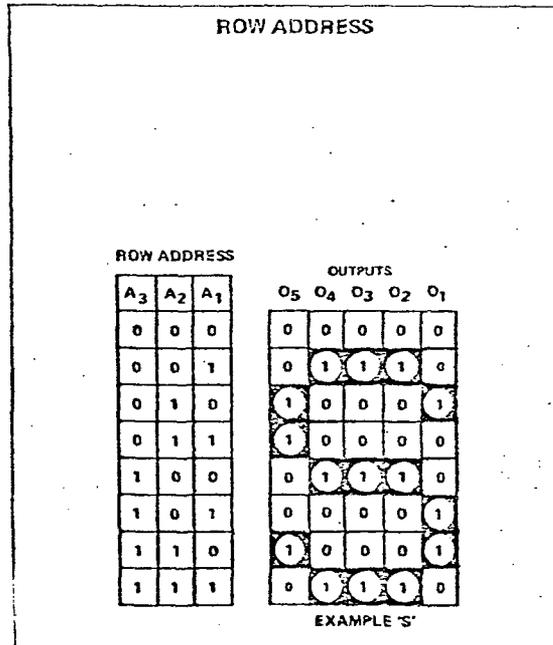


Figure 2. Row and Column Selection for Character Generator.

The remainder of this report contains the schematic (Figures 4,5,6) of the video interface and detailed diagrams of various parts of the interface. Figure 7 shows the parts placement as viewed from the top. Note there are ten 0.01 μ f bi-pass capacitors which are connected from the Vcc bus to the gnd bus on the underside of the board. This helps prevent random signals from interfering with normal operation, especially the memory circuit. Connections with the outside world are normally made through the edge connector which is described later. The composite video is made available through a BNC connector on the board.

The edge connector is shown in Figure 8. This connector brings in the various lines such as the address and data busses and the control signals. This connector is compatible with the plug for the stand-alone development system. [5]

Only two adjustments need to be made once the interface board is connected; these are the horizontal and vertical timing adjustments. The timing may be set with the aid of an oscilloscope such that the pulse widths of the vertical and horizontal synchronization pulses correspond to those given earlier. Best results may be obtained by making the adjustments with the monitor on and random memory data being displayed. The vertical and horizontal controls should be set so that the display is stable and there is minimum tearing of the top line.

Figure 9 shows a scheme for optimum mapping of memory data on the screen. The diagram shows the actual address for the data being displayed. This scheme gives good boundaries around the character field and may be tailored for the individual application. As was mentioned earlier, many address locations do not appear on screen and should be blanked out (by software) to provide vertical and horizontal blanking for the monitor.

V. SUMMARY

The objectives for this display interface were to provide a video display for the microprocessor-based development system using low-cost parts and using a simple circuit design. The video interface just described works well with the microprocessor system and is capable of being used for aircraft work as it contains its own time references and power supplies. The circuit has been developed and built so that future expansion is possible. Testing has shown that the interface provides a very usable character display and is easy to control by software.

VI. ACKNOWLEDGMENTS

Joseph Fischer is an undergraduate student intern in the NASA Joint University Program at Ohio University, and Robert W. Lilley is Research Engineer and Assistant Director of the Avionics Engineering Center.

The authors acknowledge the assistance of James Nickum, also a NASA student intern, and Ralph Burhans, Project Engineer, NASA Joint University Program.

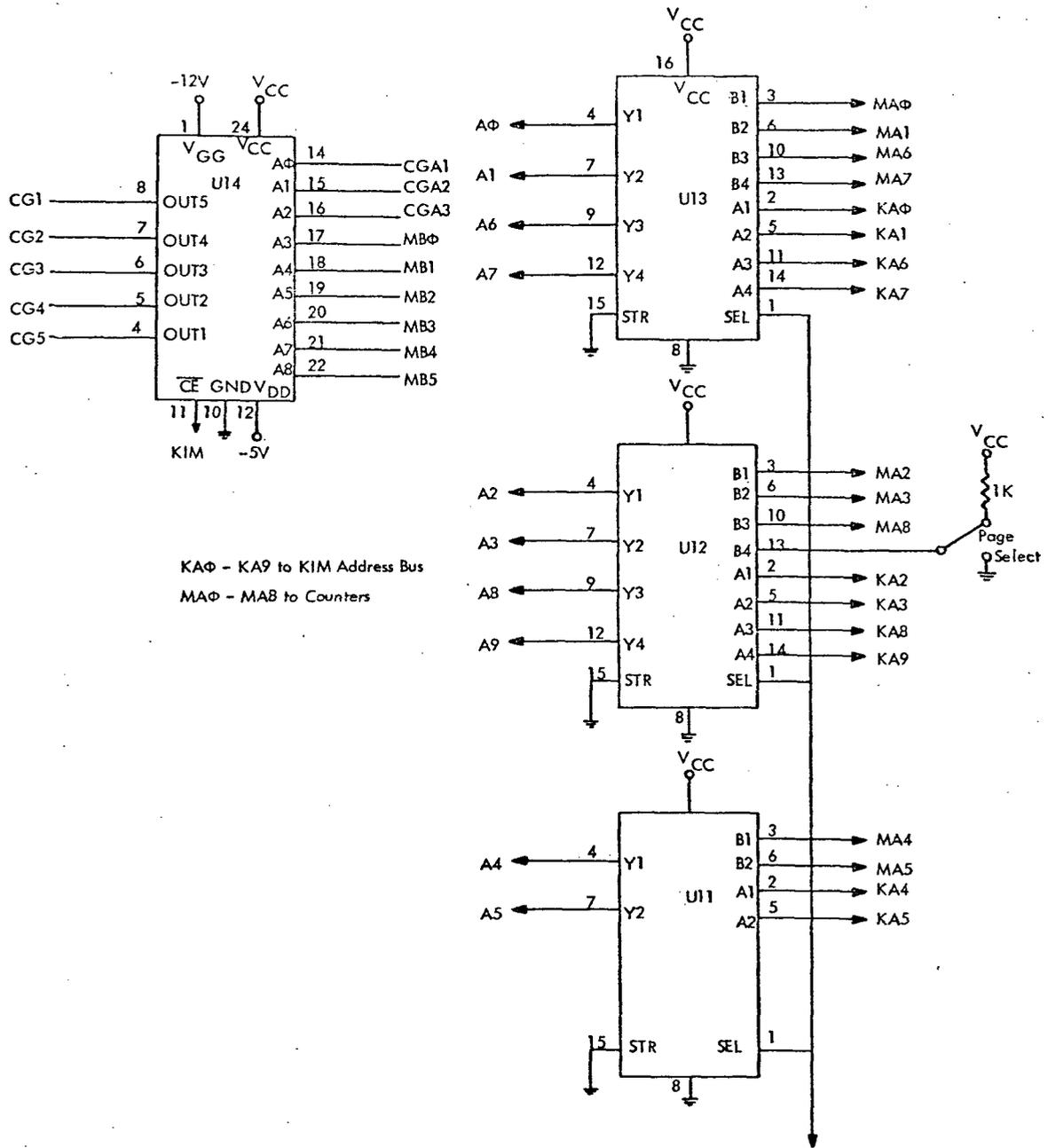


Figure 5. Schematic of Video Interface (Cont.)

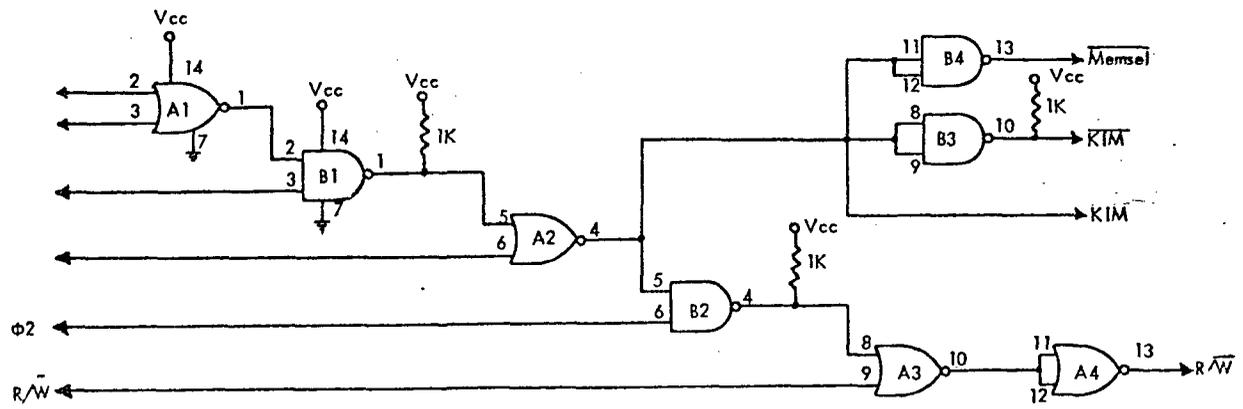
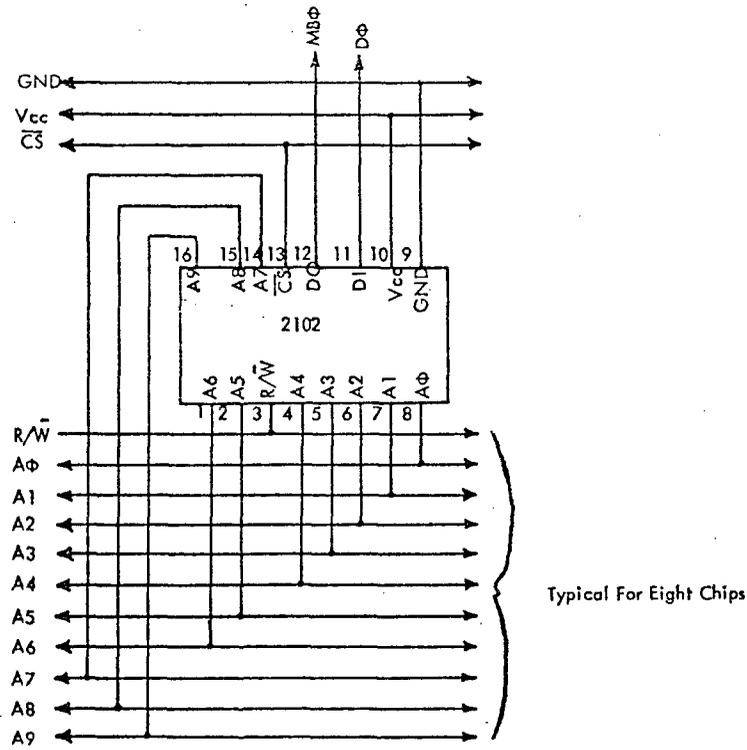
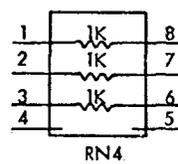
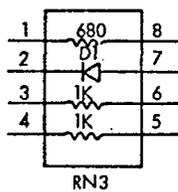
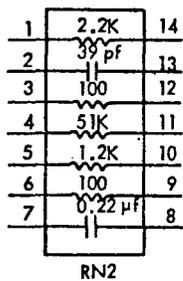
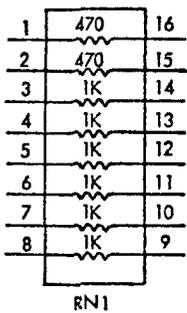
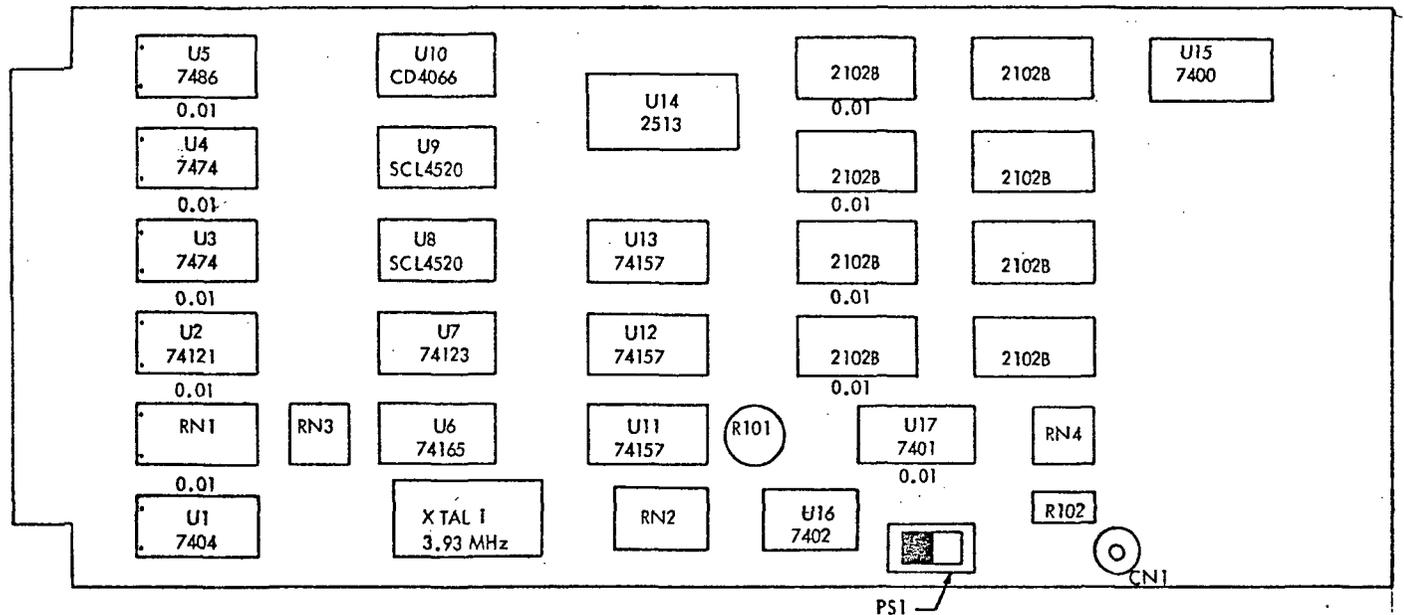


Figure 6. Schematic of Memory and Address Decoding.



- R101 (50K) - Vertical Sync
- R102 (.5K) - Horizontal Sync
- PS1 - Page Select
- CN1 - Composite Video Out (BNC Connector)
- 0.01 - Represent 0.01 μ F bypass capacitors from V_{cc} to GND (Total of 10)

Figure 7. Layout of Circuit Components.

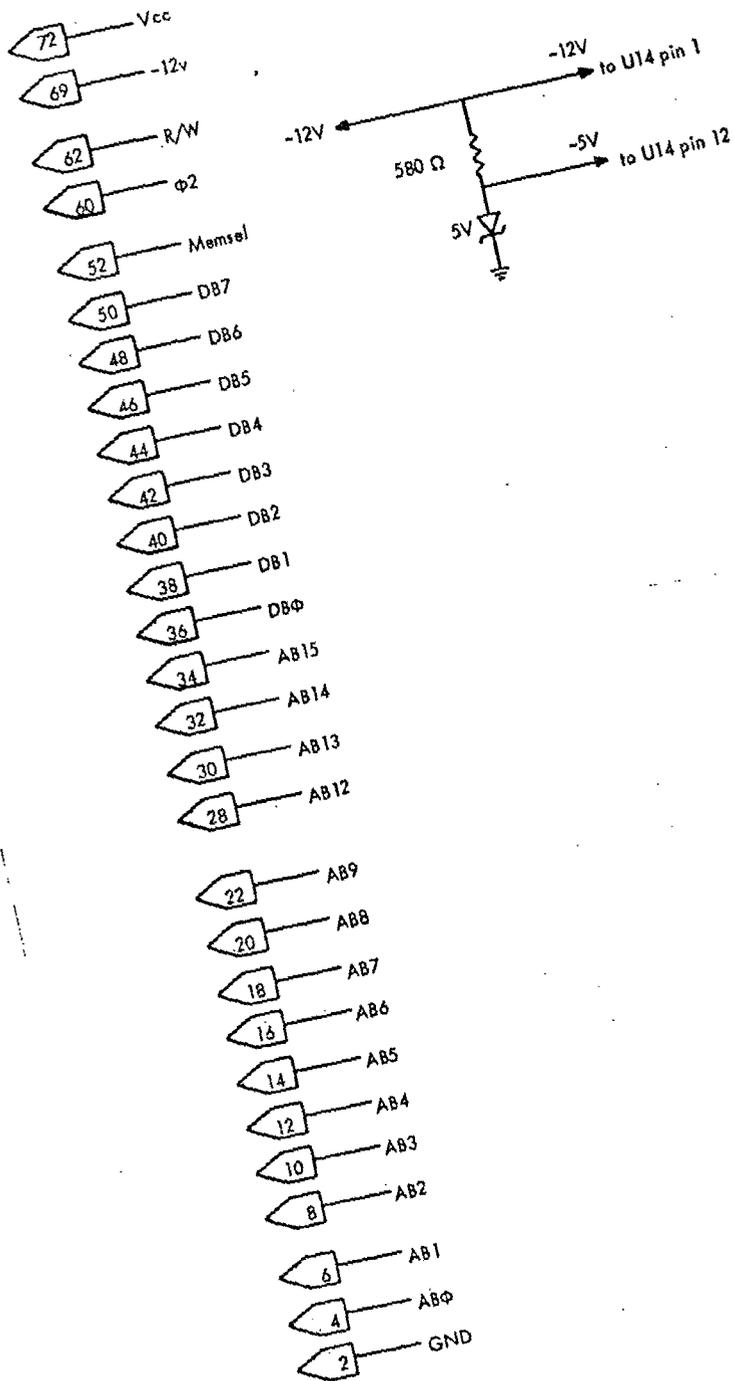
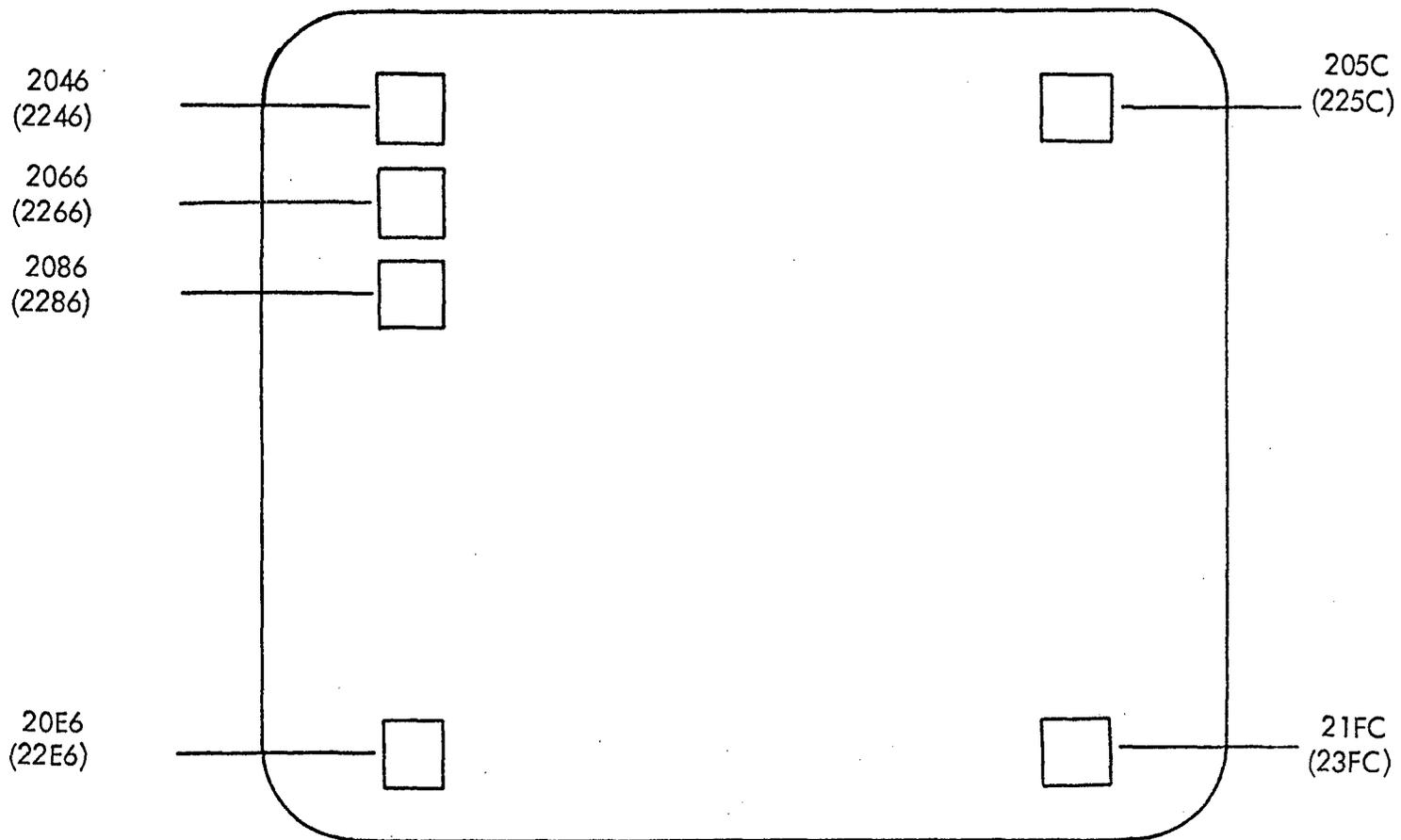


Figure 8. Edge Board Connector and Minus Power Supply.



Note: Addresses are in Hexidecimal
Addresses Enclosed by Parentheses
Refer to Page two addresses

Figure 9.. Format of Address Locations on Screen.

VII. BIBLIOGRAPHY

- [1] TV Typewriter Cookbook, Don Lancaster, Howard W. Sams and Company, Inc., Indianapolis, 1976.
- [2] Signetics Integrated Circuits Data Book, Signetics Corporation, Sunnyvale, California, 1976.
- [3] TTL Data Book, National Semiconductor Corporation, Santa Clara, California, 1976.
- [4] RCA Integrated Circuits, RCA Corporation, Somerville, New Jersey, 1976.
- [5] "Stand-Alone Development System Using a KIM-3 Microcomputer Module", NASA TM 56, J. D. Nickum, Avionics Engineering Center, Ohio University, Athens, Ohio, March 1978.