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FINAL REPORT

BASIC MECHANISMS STUDY FOR MIS SOLAR CELL STRUCTURES ON GaAs

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I. Introduction

This is a report on a largely experimental basic mechanisms study. The solar cell structure being examined is the MIS configuration on (n) GaAs. One particular system only was studied; that was the metal/ room temperature oxide/(n) GaAs materials system. Metals with electr - negativities varying from 2.4 (Au) to 1.5 (Aℓ) were used as the upper electrode. Because this was a basic mechanisms study, no attempt was made to optimize thickness for a given metal; rather the thinnest metallization that did not interfere with the measurement techniques (by introducing essentially "transmission line" series resistance problems across a device) was used. Hence, photovoltaic response was not optimized.

Putting an I layer between a metal and semiconductor can improve photovoltaic response. The immediate question is why. At first glance, it is not expected. Obviously one would expect current to be decreased with the introduction of the I layer. Superficially one would expect all current to be decreased. To be definitive, in a MIS device on n-type material the diode current (dark current) flowing conventionally from the metal to semiconductor intuitively should be reduced. The photovoltaic short circuit current flowing from semiconductor to metal should be decreased also. Performance should be reduced with the I layer's presence.

Generally, a decrease in the photovoltaic short circuit current is not seen but orders of magnitude changes are seen in many systems in the dark current. As a consequence enhanced photovoltaic performance is frequently obtained with the I layer.

Clearly photogenerated holes created in the semiconductor (n-type material) are easily crossing the I layer. The supply of these holes depends on the light, the diffusion length on the semiconductor, etc. This supply is fixed and should be the same for MS or MIS, to first order. The fact that this supply easily crosses an I layer in an MIS photovoltaic structure means that the insulator is "leaky" due to hopping from defect to defect or due to valence band (if the band model is applicable to 20 to 30Å) overlap with the semiconductor. It is also possible that the insulator is a tunnel barrier but of negligible hinderance for holes.

The fact that the dark current can change orders of magnitude with the inclusion of the I layer means one of two things: either the elections (n-type semiconductor) are having great difficulty crossing this I layer or their supply has been affected.

This physical situation was systematized into three general categories[1,2] of I layer effects: transport control, trapping on the passing of current, and barrier modification. It is within the general theoretical framework of those papers that this study is conducted. This study examines a particular materials system on (n) GaAs to determine which of these basic mechanisms is operative.

This work was originally part of an NSF-RANN sponsored joint GaAs MIS program at the Jet Propulsion Laboratory and The Pennsylvania State University. This was transferred to DOE. The work at Penn State was administered as JPL subcontract 954525.

II. Major Conclusions

1. For the materials system examined on (n) GaAs, the MIS structures are majority carrier devices. The bucking current is that of elections crossing from the semiconductor.

2. The change in open circuit voltage, from MS to the corresponding MIS solar cell structure, correlated with the Schottky barrier height change.

3. Generally Voc changes correlate well with ϕ_B(CV) changes unless leakage currents are present or device has severe hysteresis.

4. For devices where charge in the insulator shows no signs of changing slowly (i.e., no slow trapping effects) this agreement between ΔV_{oc} and $\Delta\phi_B$(CV) clearly shows that the I layer is changing the supply of available elections in the semiconductor. Clearly the $1/C^2$ measurement involves no transport across the I layer but simply measures the diffusion potential (the band bending at zero bias) in the semiconductor. This controls the supply of elections through $e^{-\phi_B/kt}$. A $1/C^2$ measurement directly yields this ϕ_B.

5. The $1/C^2$ barrier height is meaningful so long as minority carriers are unhindered.

6. Several metals examined showed appreciable hysteresis when used with the oxide employed in this study. In order of severity these are Aℓ, Ag, and Cu. Clearly Aℓ, at least, can chemically react with the oxide.

7. For Au and Pd the evolution of the barrier height ϕ and Voc with purposeful oxidation is very systematic.

8. Bare GaAs surfaces prepared with NH_4OH/H_2SO_4 produced oxide devices with higher Voc's as compared to NaOH, the alternative etch explored.

9. Copper and silver, each with electronegativity of 1.9, gave baseline MS Voc values much higher than that seen for Au (electronegativity of 2.4) and Pd (electronegativity of 2.2). This strongly implies chemical activity or at least polarization involving Cu and Ag and the NH_4OH/H_2SO_4 defined surface.

10. Disagreement between ϕ_B(PE) and ϕ_B(CV) is most severe for devices that show slow trapping.

11. Oxide just does not satisfy bonding at the Ga As surface thereby unpinning the Fermi level. The barrier height change with the introduction of this I layer does not show any strong correlation with electronegativity, at least for the range 1.9 to 2.4.

12. Photoemission studies show that this oxide does not appreciably attenuate majority carrier transport. The increase Voc is due to changing the supply of majority carriers for these materials systems explored.

13. The photoemission barrier height ϕ_B(PE) agrees reasonably well with ϕ_B(CV), the $1/C^2$ barrier height, for those metals which do not show the slow trapping effect. The trapping seems to modify electron emission from the metal when it is present.

14. It is emphasized that whichever I layer effect (transport control, trapping on passing of a current, barrier height modification) dominates will depend on the specific materials system. The overall effect of the I layer can be advantageous: for some systems it can be disadvantageous. We have observed the latter for some Si systems. For the MIS on GaAs system explored, the I layer was always advantageous.

15. These MIS GaAs solar cell structures, for the oxide used, have slow traps present for some metallizations. Fast traps are present for all metallizations. These are generally of the order of $< 10^{13}$ states $/cm^2/eV$.

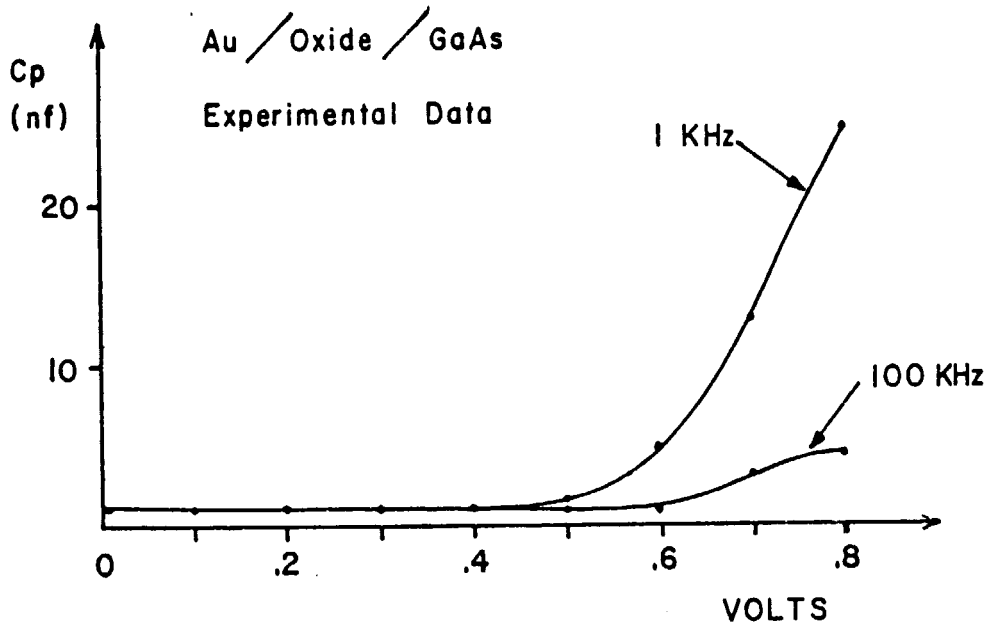
16. M-I-S devices on GaAs, for the systems examined, were found to display field shaping in forward bias. That is, charge was being stored in fast states in forward bias on the passing of a current. Capacitance, in addition to diffusion capacitance and that arising from the semiconductor space charge region, was observed. Generally the MIS forward C-V behavior was found to fall into two classes:

(a) That which showed large capacitance at 1 KHz and little capacitance at 100 KHz.

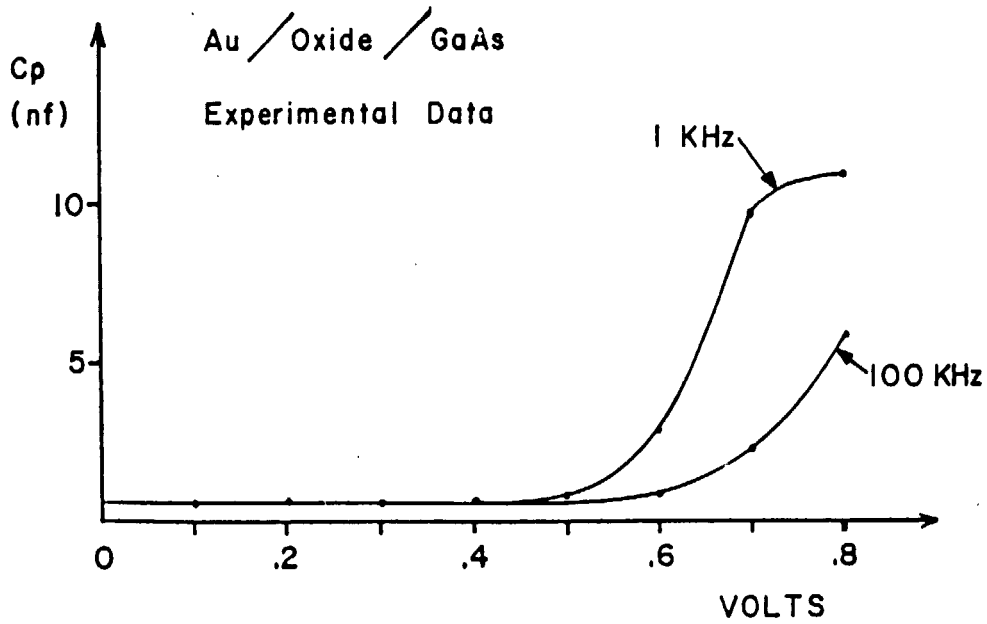
(b) That which showed little dispersion between 1 KHz and 100 KHz. In this case capacitance values were lower.

17. Baseline devices (MS) showed little capacitance in forward bias as expected (See ref. 8).

18. MIS devices with intermediate barrier heights (1.10 to 1.15 eV), as measured by reverse C-V generally showed behavior (a), variation of capacitance with frequency. A typical plot is shown below.



19. MIS devices with large barriers (>1.15 eV), as measured by reverse C-V, tended to give forward C-V curves as shown below.

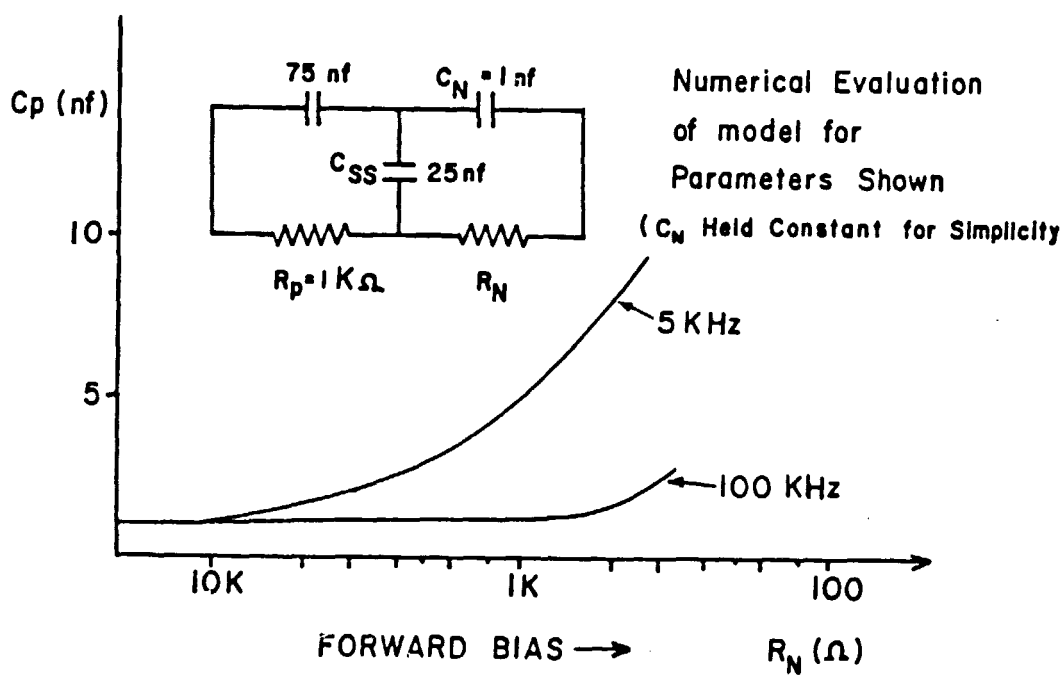


These differ from the intermediate barrier devices in that less capacitance is seen at all frequencies. Also there is less dispersion of capacitance with frequency.

20. These results outlined in (18) and (19) can be explained with the model of reference (8). Simplified versions can demonstrate what is happening (shown below together with numerial evaluations of the model)

21. From ref. 8 it is known that R_n will decrease exponentially with increasing forward bias. For the barrier heights observed R_p is relatively small. It will decrease with increasing barrier height (ref. 8).

To understand what is happening in case (a), intermediate barriers, we use this set of realistic values for R_p C_s, etc. to demonstrate the physical situation:



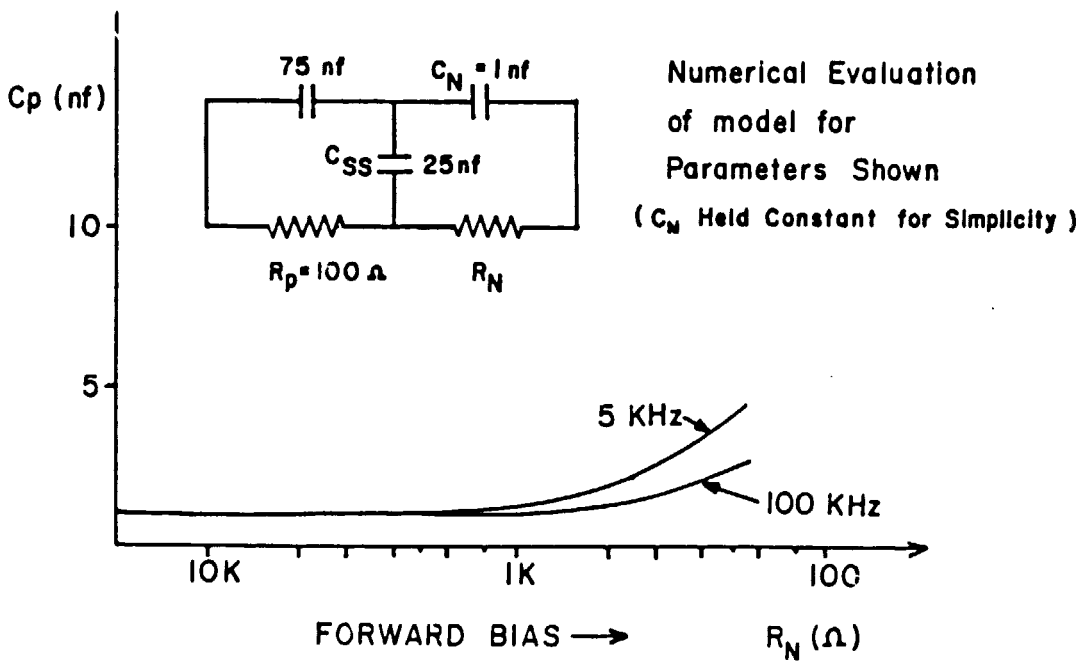
Note that as the bias increases (in forward bias) R_n decreases. For the above set of parameters, dispersion is seen. The above plot also shows that the low frequency capacitance is larger than the high frequency capacitance. Note that the difference between low frequency and high frequency capacitance ΔC is not C_s; therefore

$$N_s = \Delta C/e$$

underestimates N_s, the localized state density.

22. To understand what is happening in case (b), barriers >1.15eV, we use this same set of values as above except R_p is reduced due to the larger ϕ_B. Of course R_n would start at a higher value (compared to case (a) for zero bias; but one can just account for this by assuming zero bias is more to the left in the figure below.

The numerical model based on ref. 8 shows that this case gives little dispersion and lower capacitance at all frequencies. This corresponds to what is actually observed. Clearly, for this case (b), ΔC underestimates N_s more than for case (a).



23. Variations in forward bias capacitance between devices processed differently can largely be explained in terms of barrier height differences only. It is difficult to relate surface state densities to the material processing, directly, since the barrier height also changes with material processing. Devices with intentionally grown oxides show evidence of surface state densities $\gtrsim 10^{12}$/ev cm^2. Baseline devices have surface state densities at least an order of magnitude below this.

III. Fabrication and Characterization Used in This Experimental Study

A. Device Fabrication

1. Ohmic Contact Formation

For the studies of this report n/n+ GaAs of (100) or (111) orientation were used to fabricate both MS and M-I-S photovoltaic structures. After being cut into chips, the GaAs (single crystal material only was used) was first always given a "new material" clean. This clean consisted of the following: (1) rinse in trichloroethylene; (2) rinse in acetone; (3) rinse in isopropyl alcohol; (4) de-ionized water rinse; (5) five-minute agitation in acetone, rinse; (6) five-minute agitation in isopropyl alcohol, rinse; (7) 15-minute boil in trichloroethylene; (8) acetone rinse; (9) isopropyl rinse; and (10) then blown dry in N_2. The material was subsequently etched ($H_2SO_4/H_2O_2/H_2O$ [1:1:50] and Au-Ge eutectic was evaporated for the back, Ohmic contact. Sintering at 500°C in N_2 was then done for 5 minutes and, finally, 1000Å of Au was evaporated over the Au-Ge layer.

The resistance of these back contacts was always monitored prior to storage of the chip for future use. This could easily be done since the back contact was evaporated in an island configuration; i.e., there were two isolated Ohmic contact areas. Back contact resistance was always negligible. This was absolutely necessary for this basic studies work as is discussed in Section III.B.2.b.

2. Semiconductor Surface Preparation

In this study GaAs baseline devices (semiconductor surface etched and then immediately metalized) and GaAs conducting metal-oxide-semiconductor devices were fabricated and characterized. The first structure may be thought of as an M-S device and the second structure as a conducting MIS device. The base GaAs surface used for either structure was prepared when this work first began by using a Bromine-methanol etch. However, use of this etch system was found to be an unreliable way of defining the bare GaAs surface needed for subsequent processing. Recent work at Bell Laboratories on GaAs etches has underscored the difficulties involved in Br-methanol etch.[3]

Because of these problems with Br-Methanol, the following procedure evolved for preparing the semiconductor surface in the final etch which defined the base GaAs surface: first chips which were in storage (see Ohmic contacts, Section III.A.1) were soaked in isopropyl alcohol, rinsed in isopropyl alcohol and then blown dry in N_2. Then one of two etches was used. These final etches (an etch was used in the Ohmic contact processing, see Section III.A.1) systems used are referred to as either basic (one minute using $NaOH/H_2O_2/H_2O$ [5:7:90]) or acidic[4] (fifteen seconds using $NH_4OH/H_2O_2/H_2O$ [10:1:1]; then one minute using $H_2SO_4/H_2O_2/H_2O$ [10:1:1]). The freshly etched chips were then rinsed in running de-ionized water for 10 to 15 minutes. Baseline devices (MS) devices were fabricated by immediately metalizing these bare, freshly defined surfaces. The conducting M-I-S devices were fabricated by oxidizing these etched GaAs surfaces; for the MIS structure metallization was subsequent to this purposeful oxidation.

Since the main objective of this study was to gain insight into basic mechanisms operating in M-I-S solar cell structures fabricated using GaAs, well-defined, repeatable procedures had to be employed at every step. Consequently great care was taken to avoid any contamination during this process of defining the bare GaAs surface. All "electronic grade" chemicals were used; precautions were taken to avoid dust, etc.

3. Oxidation Procedure Used for MIS Structures

Because of funding limitations, we had the opportunity of using only one oxidation procedure for this study. That procedure was to employ room temperature oxide growth using a water bubbled O_2 ambient[4]. Hence it must be noted that all results of this work apply to MIS on GaAs systems employing <u>this specific</u> I layer.

This room temperature oxide layer was grown in a glass tube using zero grade O_2. The tube was periodically given a precautionary cleaning as follows: (1) 30 minute immersion in Aqua Regia; (2) rinse with copious amounts of DI water; (3) 5 minute immersion in HF/DI water (50:50) and then (4) rinse with copious amounts of DI water. The tube was dried after such a cleaning by passing N_2 through. When the tube was not being used for oxidation, this same N_2 streaming (zero grade N_2) was used.

All gas lines to the oxidation tube were teflon. Flow meters, as normally found in electronic devices processing, were used for gas flow rate control.

The M-I-S solar cell structures were fabricated using this equipment to produce the I layer of this study. In all cases the purposeful oxidation employed in the MIS configurations was done by inserting the freshly etched chips (discussed in Section III.A.2) into the environment of the oxidation tube. Water-bubbled O_2 (flowing at 0.5 SLPM) was always used in the tube, at room temperature.

4. Metallizations Used

The metals used in this work were Au, Pd, Ag, Cu, and Aℓ. These metals are listed according to their Pauling electronegativities which are[5] 2.4, 2.2, 1.9, 1.9 and 1.5, respectively. They were chosen because they give a spread in electronegativities. This spread extends over that available for convenient, usable metals, i.e. from Aℓ to Au. Hence, although specific work function data is in doubt, this study has used metals whose work functions span from that of Aℓ (about the lowest of usable metals) to that of Au (about the highest of usable metals).

Metallizations were performed immediately after etching for M-S devices and immediately after oxidation for M-I-S devices. The metallizations were performed in an oil-less Varian vacuum system using a Vac-Sorb and a Vacion Titanium Sublimation pump to achieve a vacuum in the 10^{-8} torr range.

B. Device Characterization

1. Information Needed for Characterizing MIS Solar Cell Structures

It is clear that photovoltaic data for an MIS device is of primary consideration. More information is needed, however, to determine physically how a given MIS solar cell operates. To fundamentally understand MIS solar cell device operation for a given materials system (by a materials system is meant the particular metal, the particular I layer, and the semiconductor including the particular surface treatment used), one must be able to show experimentally the origins of the enhanced behavior. One must be able to determine why the performance is enhanced for the MIS solar cell structure over the corresponding MS structure. This work experimentally demonstrates the role of the I layer in a particular MIS system; that system studied is of the general form metal/room temperature grown oxide/(n) GaAs.

The I layer need not always enhance the performance of the MIS structure over the corresponding MS structure. In fact, we have demonstrated this for Si[6] where, for one specific materials system, the MIS configuration dark I-V gives <u>higher currents</u> than the corresponding dark I-V for the MS device. As a photovoltaic structure the MIS device for this system is out-performed by the MS device. At first it seems strange that the structure with an I layer passes more dark current, but for this system the effect has a chemical origin.

The point is the I layer can be advantageous; it can be disadvantageous. It depends on the system. This was incorporated in the general theory of the role of the interfacial layer in MIS solar cells.[1] It was shown that the introduction of an I layer opens the door to three general categories of effects which can then occur in solar cell structure.[1,2] These can, independently, occur in an advantageous or disadvantageous manner. A great deal of detailed modeling has been done since that general paper; however, the broad categories delineating what the I layer physically can do have only been substantiated. Given an MIS solar cell structure one clearly would like to determine which of these possible effects are present, which are acting advantageously, and which are acting disadvantageously.

These three effects possible in the MIS solar cell configuration can be categorized as [1,2] (1) transport attenuation by the I layer (in the MIS configuration, transport between the metal and semiconductor--and the reverse--must take place by hopping or some tunneling process across the I layer), (2) trapping of charge on the passing of a current (field shaping effect; one reason why the diode ideality factor n can be >1.0), and (3) Schottky barrier height modification. When one or more of these occurs in an advantageous manner, enhanced solar cell performance is observed. These categories serve as a "check-off list" in examining an MIS solar cell structure to determine the origins of its physical behavior.

Having physically categorized the possible effects present in the MIS structure, it remains to determine what approaches will be used to examine for them. To establish this some theoretical discussion is necessary. It can begin with the device dark current density (dark IV). This is the bucking current or closely related to it (light may modify ϕ_B or n).

The current may be viewed as being composed of three components. For n-type material these take the form:[1,2]

$$J_D = \tau_e A^* T^2 e^{-\phi_B/kt} \left[e^{V/nkT} - 1\right] + \tau_h \frac{eD_p P_{no}}{L_p} \left[e^{V/kT} - 1\right] + J_{recombination} \quad (1)$$

This relatively simple equation points out physically what is happening in an M-I-S structure. It avoids the specific system-dependent details needed in numerical modeling. The τ prefactors are, in general, voltage dependent. They characterize the effects of transport across any interfacial layer (I layer) present.[1,2]

The first component of Eq (1) is the majority carrier contribution. It is a thermionic emission term which is strongly controlled by the barrier ϕ_B. It may be reduced if the thermionically emitted electron supply is attenuated by the I layer. This is characterized by the τ_e prefactor.

The quantity S defined by

$$S = A^* T^2 e^{-\phi_B/kT} \left[e^{V/nkT} - 1\right] \quad (2)$$

gives the supply potentially available for crossing from the conduction band of the semiconductor to the metal; τ_e gives the probability that these electrons do indeed cross the I layer. The quantity τ_e is such that $0 \leq \tau_e \leq 1.0$.

The attenuation τ_e, in a given system, may physically arise because the electrons must hop from defect to defect across the I layer. In another system it could arise from direct or indirect tunneling. Fortunately, some observations concerning τ_e can be made without recourse to specific models. These observations will help us to experimentally understand a given MIS system.

The first point to be made is an important one: attenuation of the supply S (Eq (2)) by τ_e physically cannot give rise itself to a voltage drop across the I layer. The reason lies in Gauss' Law. For a given supply S there is a specific band bending configuration in the semiconductor. Hence a specific electric field configuration throughout the semiconductor. If the I layer only acts as a "filter" allowing some of S to cross and does not cause charge to be trapped, on the passing of a current, at or near the I layer, then τ_e causes no voltage drop across the I layer. The electric flux lines that are crossing I are still dictated by the semiconductor configuration; i.e., Gauss' Law. Hence the presence of a $\tau_e < 1.0$ alone cannot change the electric field configuration in the I layer from that which would be present if $\tau_e = 1$. Then varying τ_e alone cannot change the voltage drop existing across the I layer, for a given configuration in the semiconductor or, equivalently, for a given supply S. The value of τ_e does not affect the electric field configuration in the I layer or in the semiconductor for a given supply S. It simply reduces the amount of that supply S which can cross to the metal. By itself it cannot influence capacitance measurements.

A second point can be made concerning τ_e which will influence our interpretation of the data. If τ_e is present in a majority carrier device (i.e., the first term of Eq (1) dominates) but not specifically accounted for, then there are two ways in which it will influence experimental data: (1) If τ_e is constant, being unaware of its presence will lead to a barrier height determination from dark I-V data that is higher than the true value. (2) If τ_e is a function of S (and, therefore, of voltage), then being unaware of its presence will lead to n factors (even without field shaping or recombination) that are greater than unity. A dependence of τ_e on S is possible if, for example, transport across the I layer is by hopping from defect to defect.

Clearly there is a need to independently measure τ_e and ϕ_B. The latter quantity, of course, controls the supply S as is seen in Eq (2). In principle τ_e can be independently determined in a photoresponse measurement in which electrons in the metal, once excited by light, cross the I layer, and are collected by the electric field in the semiconductor. The barrier height can be obtained, in principal, also from photoresponse or from $1/C^2$ data. These are all discussed below.

A further complication can arise in the first component of Eq (1). As has been mentioned, charge may be stored in the I layer when a current flows. This would redistribute the voltage V across the device. There would be a voltage drop across the I layer in this case. Thus the n factor of this first term can be 1.0 for a reason completely different than that discussed above. It can

be >1.0 because the supply of available electrons in the semiconductor, which can be thermionically emitted, follows a voltage less than V.[1,2] That is, the applicable Boltzmann factor in this case if $e^{V/nkT}$ not $e^{V/kt}$. In principle such a redistribution of voltage is detectable by a forward bias capacitance measurement.[8]

If the first component of J_D in Eq (1) dominates, the Schottky barrier-type structure is a majority carrier device and the dark I-V characteristic must be correlated to barrier height. Summarizing, in ln J_D versus V plot can yield an n factor greater than unity even if there are no recombination currents (1) because of voltage dependent attenuation of the transport across the I layer of the thermionically emitted electrons or (2) because of redistribution of the voltage across the device due to the presence of trapped charge on the passing of a current. The trapping is in the interfacial layer or at the interfacial layer/semiconductor boundary. The former would give n >1.0 since determining n factors from ln J_D versus V plots implicitly ignores any voltage dependent τ_e prefactor. That is, one is interpreting the I-V characteristic in terms of $A^*T^2e^{-\phi_B/kT}$ $(e^{V/nkT} - 1)$. The second would give an n >1.0 since the applicable Boltzmann factor is $e^{V/nkT}$.

When considering experimental data, it must be realized also that the majority carrier components of Eq (1) can be suppressed entirely in Schottky barrier-type devices by the addition of a properly chosen I layer. If this has occurred clearly the dark I-V characteristic would not correlate with barrier height. Photovoltaic performance would not correlate with barrier height. As seen from Eq (1) a minority carrier device on an n-type semiconductor could have its dark I-V controlled by hole transport across the I layer. This transport is characterized by τ_h. Alternatively the hole transport could be controlled by diffusion in the semiconductor.[1,2] In the former case the Photovoltaic short circuit current would be suppressed.[1]

From this above discussion of the three possible effects present in the MIS solar cell configuration, it is seen that a series of measurements and correlations is needed to experimentally examine a device. To examine for effect (1), transport control, and independent probe is required to monitor electron transport from the metal, across the I layer, to the semiconductor and the reverse. A probe is also needed to monitor hole transport (the minority carrier in this work) from the metal to the insulator and reverse. In principal a photoemission experiment can be used to independently examine electron transport across the I layer. Hole transport is easily checked by observing the photovoltaic short circuit current.[1]

To examine for effect (2) one must realize that there can be slow trapping and fast trapping. For slow trapping, one must look for hysteresis in the dark I-V and light I-V (performance under light). This would show up gross effects only as the traps fill. Further, slow traps, if they stayed filled, would then show up as a ϕ_B change, employing forward bias C-V (as a function of frequency) measurement If there is meaningful bias developed across the I layer, <u>it must</u> show up in a forward C-V measurement.

To examine for modification of the Schottky barrier height (effect 3) three techniques can be used to measure the barrier height ϕ_B. The best is to use reverse C-V ($1/C^2$ plots) to determine the diffusion potential.[9,10] Determining the diffusion potential will then yield the barrier ϕ_B since the doping will be known. Such a barrier height determination is independent of transport across the I layer. Another technique is photoemission. Use of the Fowler plot is required and transport across the oxide by the electrons (for the n-type GaAs considered here) is convoluted into the measurement.[9] However, this can be an informative, independent technique. Some practical problems will be discussed below. The third technique is to use dark I-V data and <u>assume</u> Eq (2), along with assuming $\tau_e = 1$ or $\tau_e = \tau_e(V)$ (such that this voltage dependence can be incorporated into n.) This last technique has errors introduced by leakage currents and recombination currents. This use of ln I versus V plots does, however also allow determination of n which can be correlated with other measurements.

2. Approaches Used

a. Reverse C-V Technique

The reverse bias capacitance $1/C^2$ technique provides one method to determine the Schottky barrier height, ϕ_B (CV), which does not involve the transport of majority carriers through the interfacial oxide. In this sense the attenuation properties of the oxide film, if any, do not affect the determination of the diffusion potential. However, the effects of charge redistributions due both to the surface oxidation and metalization are reflected in the space charge region of the semiconductor and in turn in the measured diffusion potential. Further, if the reverse $1/C^2$ plot is linear, it represents a meaningful technique for obtaining device barrier heights.[8,9,10]

In this work the reverse C-V was extensively used; $1/C^2$ plots were employed to determine the Schottky barrier height. The notation ϕ_B (C-V) is used for a barrier height obtained from a $1/C^2$ plot. This information also provided an independent measure of the semiconductor chip doping.

In this work reverse C-V data was generally measured at 100 KHz. The apparatus used is discussed in the section on forward bias C-V measurements.

b. Forward Bias C-V Measurements

If there is significant voltage dropped across the I layer in a given system, this will show up in a forward C-V measurement. For such a voltage to develop on the passing of current there must be charge trapped in the I layer or at the I layer/semiconductor boundary or both when the current flows. As discussed in reference 8, theoretical work done partially under the sponsorship of this contract, forward C-V can yield characteristic times for the trap sites. Most importantly such data can give an estimate of N_T, the trap site density involved, since

$$N_T \simeq \Delta C/e$$

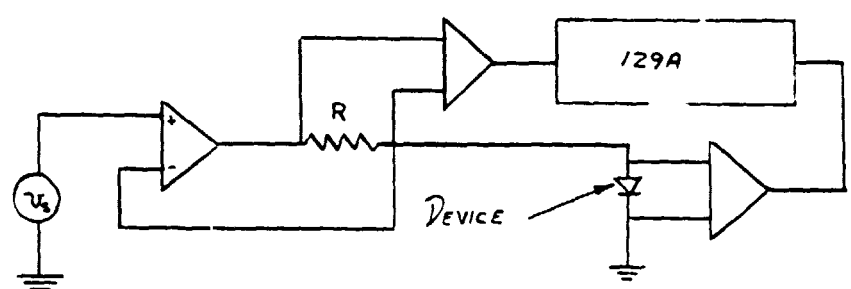
where N_T is in $(eVcm^2)^{-1}$ and ΔC is the excess capacitance coming from the fast traps (defined by the lowest frequency that can be used) per cm^2. It can be shown that this only gives a lower bound for N_T.[8]

To obtain this forward C-V data, great care must be taken to avoid spurious data. Back contacts must have negligible resistance; otherwise, when the solar cell forward current turns on, the back contact can significantly affect the data. The apparatus must be carefully designed and set up. The specific design, as well as discussion of the evolution of the system, is to be found in monthly reports and the semi-annual report submitted to JPL.

In brief, the apparatus set-up was designed for use with M-S and M-I-S devices. Since these structures are conducting in forward bias, measurement of their equivalent parallel capacitance can be difficult. Stray impedances, harmonics of the applied frequency (generated by the diodes non-linear IV) and "ohmic" contact impedances, can cause large errors in the measured capacitance, as the diode is forward biased. The apparatus in use was designed to minimize these sources of errors.

Two systems are used to obtain forward bias CV data. One is based around a General Radio 1608A bridge, and is used at low frequencies (<20 KHz). A Princeton Applied Research (PAR) 129A lock-in amplifier (LIA) is used as a detector with a PAR 124A LIA used as a preamplifier, in the bandpass mode. This combines the advantages of a tuned detector (high harmonic rejection) with that of the LIA (high rejection of non-coherent signals, separate in-phase and quadrature nulling). The bridge can be accurately balanced with less than 1 mv (rms) across the diode, which reduces errors due to harmonics.

At high frequencies (>5 KHz) the 129A lock-in is used as part of a phase detection system. A block diagram of this is shown below:



An operational amplifier connected as a voltage follower is used to apply a signal to the diode. Since the feedback for the op amp is taken after the resistor, R, the diode is driven by a near ideal voltage source with an output impedance <1Ω. This insures that the voltage across the diode will have a negligible harmonic content. This voltage is amplified, and applied to the reference input of the lock-in amplifier. The voltage across R, which is proportional to the current through the diode, is applied to the LIA's input. The LIA then determines the components of the current which are in phase, and 90°out of phase with the reference voltage,

and hence the real and imaginary components of the diodes admittance. The four terminal connection of the diode eliminates the effects of series inductance and resistance in the cables. Excitation levels of less than 1 mv rms are used to minimize the effect of the harmonics. This system and the bridge described previously, are in good agreement at intermediary frequencies (5 to 20 KHz).

c. Internal Photoemission

The Schottky barrier height may be independently determined, in principle, by an infared photoemission experiment. In this experiment an electron near the Fermi level in the metal is excited to a state above the Fermi level and travels across the interface (by tunneling, or hopping in the case of an M-I-S structure) into the semiconductor. The photoresponse is described ideally by the Fowler theory and is given by $R \doteq$ constant $(h\nu - \phi_B)^2$. A plot of the $\sqrt{R}$ versus $h\nu$ yields ideally an intercept equal to the Schottky barrier height, ϕ_B(P.E.).

Photoemission experiments of this kind have a long established history in the study of M-S contacts. However, the extension of this technique to the study of M-I-S structures requires a careful consideration of the effects of the interfacial oxide. In this type of experiment for the M-I-S structure, the barrier height determination is complicated by the transport properties of the thin oxide film. The barrier height changes may be indicated in data but attenuation of the electron current across the I-layer may also be indicated. It is clear that care must be used in interpreting photoemission data obtained for M-I-S solar cell structures.

In our work the photoemission appartus consisted of the following: A Bausch and Lomb ($.70\mu \rightarrow 1.60\mu$) monochrometer with a Bausch and Lomb tungsten light source are used in conjunction with a double lens colluminating optical system. The columinating and focusing lenses enable the focusing of the infrared beam to a spot $<.2cm^2$. This focusing allows one to select the beam width of the monochrometer output to be less than the device area thereby eliminating possible edge effects.

A PAR chopper (33 Hz) sets up a reference signal for a 129A PAR-LIA. The short circuit photocurrent is sent to a current sensitive pre-amp whose input impedance is less than $.1\Omega$. The low input impedance assures an accurate measure of the device short circuit current. The amplified photoemission signal is then sent to the PAR-LIA, where the magnitude of the response is determined.

d. Dark I-V Measurements

Dark current-voltage data is very informative since it shows the solar structure functioning as a diode. The current flowing is composed of the contributions of Eq (1). When the structure is functioning as a solar cell, the strength of the bucking current determines performance. The bucking current is the dark I-V or is closely related to it. (With light present the ϕ_B, n, and even τ's of Eq (1) could be modified if trapping is involved

in the structure.) As discussed in Section III B1, dark I-V data may be interpreted to yield n and ϕ_B values.

Dark I-V data should be taken by ramping up and down to look for hysteresis effects. This approach was used in all data reported here.

e. Photovoltaic Response

Simulated AMI conditions were established using ELH bulbs. All devices were examined for photovoltaic response at 28°C. This temperature was established and monitored using a Peltier plate. Light intensity was calibrated using a NASA standard Si cell. Characteristics in the fourth quadrant (power quadrant) were swept back and forth to look for any possible hysteresis effects.

Besides its obvious use, photovoltaic response can show if minority carriers are having difficulty crossing the I layer. If they are, the short circuit current will fall.[1] This is a very important application of photovoltaic response from the point of view of examining for specific effects in a given device.

IV. Experimental Results and Discussion

In the course of this study a number of devices were fabricated. Table I lists some specific examples. It must be remembered that these devices were fabricated to examine basic mechanisms. Hence the oxidation procedure and the metallization were not optimized for solar cell performance. From this table it is clear that every measure of barrier formation shows that this purposeful oxide (grown as indicated) increases the barrier for the systems studied. This is the basic origin of the increased performance seen in these GaAs MIS devices. This possible effect was category (3) in Section III B1.

If purposefully inserted oxide did not play some active role in barrier formation (through chemical interaction, trapping), its presence could only reduce the device barrier height below the baseline value.[1,2] That is, if the inserted oxide only served to separate further the metal and GaAs, the barrier height would be reduced.[1,2] Such is not the case. This I layer, produced as described, is playing an active role; all the devices using these materials systems had increased ϕ_B values.

The oxide could change the barrier ϕ_B by satisfying the bonding requirements at the GaAs surface, a simple chemical effect. Thus with the oxide present the Fermi level at the surface of the semiconductor would be unpinned allowing the barrier height to reflect the metal -- GaAs work function difference. This does not seem to be the general case as will be discussed below. The barrier change is certainly related to trapping, at least for Ag, Cu and Al on this grown oxide. Devices fabricated using these metals showed significant charge trapping in the oxide. Also fast interface states were seen for these metals and even for Au devices in MIS structures using the oxidized surface employed in this study. Figure 1 presents some examples. This forward C-V data show the filling of fast interface states in forward bias.[8]

TABLE I

FABRICATION AND ELECTRICAL PARAMETERS FOR VARIOUS CONDUCTING METAL-OXIDE-(n) GaAs DEVICES.
Asterisk Indicates Parameter Which May Vary Due to Trapping.

Etch	(No Optimization) Oxidation Parameters	(No Optimization) Metallization	Orientation	Photoresponse Barrier (ev)	C-V Barrier (ev)	Dark I-V Barrier (ev)	Photovoltaic Open Circuit Voltage (ev)	Device Number	Comments
NaOH	Baseline	Au (125A)	(100)	1.01	.99	.93	.47	G-19	See G-21; very similar
NH_4OH/H_2SO_4	Baseline	Au (125A)	(100)	--	1.02	.93	.49	G-60	See G-21; very similar
NaOH	48 hrs; 0.5 SLPM O_2	Au (125A)	(100)	--	1.12	.98	.58	G-3	
NH_4OH/H_2SO_4	48 hrs; 0.5 SLPM O_2	Au (125A)	(100)	--	1.20	1.10	.66	G-12	
NH_4OH/H_2SO_4	Baseline	Ag (200A)	(100)	.94*	1.07*	.99*	.54*	G-26	Compare to G-19, G-60, G-21; Ag reacts with surface
NaOH	48 hrs; 0.5 SLPM O_2	Ag (200A)	(100)	1.17*	1.14*	.99*	.59*	G-25	Hysteresis in light IV
NH_4OH/H_2SO_4	48 hrs; 0.5 SLPM O_2	Ag (125A)	(111)	1.16*	1.16*	1.08*	.71	G-68	Hysteresis in light IV
NaOH	Baseline	Pd (125A)	(100)	.97	1.00	.91	.46	G-21	Very similar to G-19 and G-60
NaOH	48 hrs; 0.5 SLPM O_2	Pd (125A)	(100)	1.21	1.23	.97	.60	G-31	Leakage current
NH_4OH/H_2SO_4	48 hrs; 0.5 SLPM O_2	Pd (125A)	(111)	1.15	1.23	1.08	.71	G-66	
NaOH	Baseline	Al (125A)	(100)	1.02	.73	.68	.21	G-10	
NaOH	48 hrs; 0.5 SLPM O_2	Al (125A)	(100)	1.14*	.79*	.76*	.35*	G-41	Hysteresis in light IV
NH_4OH/H_2SO_4	Baseline	Cu (1-5A)	(111)	1.08*	1.11*	1.08*	.65	G-65	Interaction with surface by Cu
NH_4OH/H_2SO_4	48 hrs; 0.5 SLPM O_2	Cu (135A)	(111)	1.16*	1.16*	1.17*	.73	G-78	Hysteresis in light IV

For these material systems presented in Table I the enhanced performance of the M-I-S solar cell compared to the corresponding MS device is due principally to increased barrier height. The evolution of the barrier formation with the introduction of the purposeful oxide used in this study is believed to be related to trapping for some metals. For some metals, chemical interaction between the metallization and the oxide is apparent. These points are discussed in detail below.

A. Au MIS and MS Devices on GaAs

Figure 2 shows $1/C^2$ data for the Au Schottky barrier-type devices of Table I. The increase of the barrier height ϕ_B (CV), as measured by C-V, with oxidation is evident. The doping variation indicated is small and consistent with that expected from wafer to wafer for this material. The $1/C^2$ plots are found to be ideal straight lines for both baseline (M-S) and oxide (M-I-S) devices.

Extensive forward bias C-V work was done for Au M-I-S devices since they were so stable (no slow trapping). As mentioned fast states were present for all metals, including Au (Figure 1). Because there is this excess capacitance ΔC present in forward bias (over that of any diffusion capacitance), there is field shaping in these devices.[1,2] The theory of Reference 8 was used to interpret forward C-V data. Due to shunting resistance (see Ref. 8 and Section II), the trapping state density can be higher than that estimated from $\Delta C/e$. The detailed information obtained and its relation to overall device behavior has already been discussed in Section II.

Dark I-V data typically seen for Au devices are shown in Fig. 3. The n or ideality factors are close to unity. The barrier height ϕ_B (IV) obtained from the dark current-voltage data evolves in the same way as ϕ_B (CV) with purposeful oxidation. In general there is reasonable agreement between the various measures of the barrier height: $1/C^2$, dark I-V, and photoresponse. These device characterization parameters are stable.

The photovoltaic behavior (no opitmization) of these Au devices of Table I is presented in Fig. 4. Again the evolution of the device with oxidation is observed. In fact for these devices the change in open circuit voltage is the change in barrier height as measured by $1/C^2$ data.

It must be noted that data for devices fabricated on two different baseline surfaces and two different oxide surfaces have been presented for Au. The difference lies in the etches used to define the baseline surface of GaAs. This is pointed out in Table I. These different etches could possibly leave surfaces containing different ions. It is noticed that NH_4OH/H_2SO_4 etching results generally in a higher barrier and a correspondingly higher Voc under AMI. For all metallizations except Al (and, therefore, for a range of electronegativities from 1.9 to 2.4), a 48 hour oxide gave a $V_{oc} \sim .7$ if NH_4OH/H_2SO_4 was used. This result was also independent of orientation as Table I shows.

B. Pd MIS and MS Devices on GaAs

Palladium Schottky barrier-type devices were fabricated in this study. Figure 5 shows that the purposeful oxidation process used again caused an increase in the barrier height over that of baseline devices. Figure 6 presents the dark I-V curves. Ideality factors were near unity for Pd devices. As would be expected for such thin metallizations, series resistance is more of a problem in the Pd structures.

Figure 7 gives light I-V data for Pd devices. The baseline behavior (as well as barrier heights) is essentially the same as found for Au baseline devices. For the M-I-S structure the behavior is also similar to that of Au devices. As was seen for gold, the change in V_{oc} for Pd devices from baseline to oxide structure is equal to the change in ϕ_B (CV) for these $n \approx 1$ structures. These devices are majority carrier solar cells whose enhanced performance in the MIS configuration is due to the increase in ϕ_B. This is again effect (3) of Section III B1 as was the case for Au.

There was no obvious hysteresis for either Au or Pd in any characteristic; e.g., dark IV, light IV, etc. Therefore, no slow trapping sites were significant in the I layer or at the I layer/GaAs interface. There are fast states present in these structures as the typical data of Fig. 1 shows. These fast states on filling give field shaping (Section III L1); that is why they contribute to the forward C-V of Fig. 1. This field shaping is one reason why the ideality factor n can be $n > 1.0$ (see Section III B1 for full discussion).

The data of Fig. 1 can be used to estimate n from [11]

$$n \approx 1 + C/C_i \tag{4}$$

where C_i is the interface layer capacitance. This must be estimated; $C_i \approx 100$ nf seems reasonable. Then from Fig. 1 n values of ~1.2 would be expected. Generally for Au and Pd $n \lesssim 1.2$.

C. Ag MIS and MS Devices on GaAs

Silver devices on GaAs were observed to be sensitive to device history. Trapping phenomena were clearly observed on M-I-S devices. This charge storage in the interfacial region was found to be erasable.

Figure 8 shows a baseline device and a device with a purposeful oxide. From the barrier heights it is seen that apparently the native oxide on the baseline surface is important for silver metallizations. However, it was found that, in the case of a purposefully oxidized surface, the barrier height could be further increased by subjecting Ag devices to a forward bias pulse. The pulses used were 50 mA/cm^2 for two minutes. Such pulses inject negative charge. This can arise since electrons cross the oxide in forward bias and some of these electrons may be trapped. Trapped negative charge in the interface layer necessitates further shielding by the semiconductor. Hence the increased barrier height seen experimentally in Fig. 8 results.

The dark I-V data also shows slow trapping (Fig. 9) for Ag devices on GaAs. Again forward bias puts negative charge in the interfacial layer when sweeping through higher voltages. This results in the higher barrier observed when sweeping back to lower voltages. The light I-V data collaborates this model.

Figure 10 shows this. Forward pulsing the Ag devices increases the barrier height (as seen in Figs. 8 and 9) and increases the photovoltaic open circuit voltage V_{oc}. Figure 10 further shows that passing a reasonably strong current in the opposite direction to the forward pulse, as occurs under light, erases the charge trapped -- at least partially. This is discussed in more detail later.

Table I shows that for Ag devices ϕ_B, as measured by photoemission, can differ markedly from ϕ_B as measured from C-V. This also shows up for Al. Both systems, using the oxide of this study, showed considerable slow trapping effects.

D. Cu MIS and MS Devices on GaAs

Table I shows the results seen using Cu as the metallization in the system under study. From the metals considered so far, it is apparent that, although the metal electronegativities have varied from 2.4 (Au) to 1.9 (Cu and Ag), the V_{oc} attainable with a 48 hour oxide has not varied correspondingly. Hence, it does not seem possible to attribute the barrier height change seen in the metals considered to this point simply in terms of the oxide unpinning the Fermi level (Section III B1).

The light I-V for Cu devices (MS and MIS) appears in Fig. 11. The photoemission response, or rather its square root as dictated by the Fowler plot approach, is seen in Fig. 12. These photoemission plots are typical of that seen for all metals (they are shifted, of course, for other metals); hence, they can be used to point out some general observations.

As discussed in Section III B1, if there were a voltage (or energy) dependent τ_e for electrons (see Eq (1)), then there would be no linear Fowler region from which the barrier height could be extrapolated using $R^{\frac{1}{2}} \sim (h\nu - \phi_B)$. If the oxide introduced a constant attenuation, then the slope of the Fowler region of Fig. 12 would be different for baseline and oxide. It is not; nor is it for any of the other metals that were used.

The picture that is emerging, then, is that the oxide just does not satisfy bonding at the semiconductor surface unpinning the Fermi level. The barrier height change shows no strong correlation with electronegativity at least for the range 1.9 to 2.4. The principal enhancement of V_{oc} is due to this change in ϕ_B. There are trapping sites present -- fast sites in all systems and, for some (Ag, Cu, Al) slow sites. Further the oxide does not appreciably attenuate majority carrier transport. Also there is no evidence for any minority carrier attenuation by the oxide. Transport across this oxide is probably by a hopping mechanism from one defect to another.

E. Al MIS and MS Devices on GaAs

Aluminum Schottky barrier-type devices fabricated in this study generally were unstable. Figure 13 gives $1/C^2$ data for two devices. Oxidation does tend to increase the barrier height, but as Fig. 14 shows there are hysteresis effects in the dark I-V arising from slow traps in the interfacial region. The $1/C^2$ barrier heights agree reasonably well with those obtained from the dark I-V; however, photoresponse barrier heights are much higher. This apparently is related to trapping of the photoexcited electrons coming from the metal in this measurement.

Figure 15 shows the enhanced photovoltaic response (increased V_{oc}) seen for Al-oxide structures over Al-baseline devices on GaAs. Again trapping in the interfacial region is evident. This behavior of Al devices is similar to that seen for Ag devices on the same water-bubbled, O_2 grown oxide. As seen in the insert in Fig. 15, forward biasing can put negative charge into the interfacial layer since electrons must cross that region. Under light, when operating as a photovoltaic device, the biasing configuration of the device is similar to forward bias but the current is flowing in the opposite direction. In fact for an n-type device it must be carried by holes across the interfacial region.[1] These holes can erase -- at least partially -- the stored negative charge. Reverse biasing the device, in the dark, is essentially unable to erase the charge due to the low saturation current.

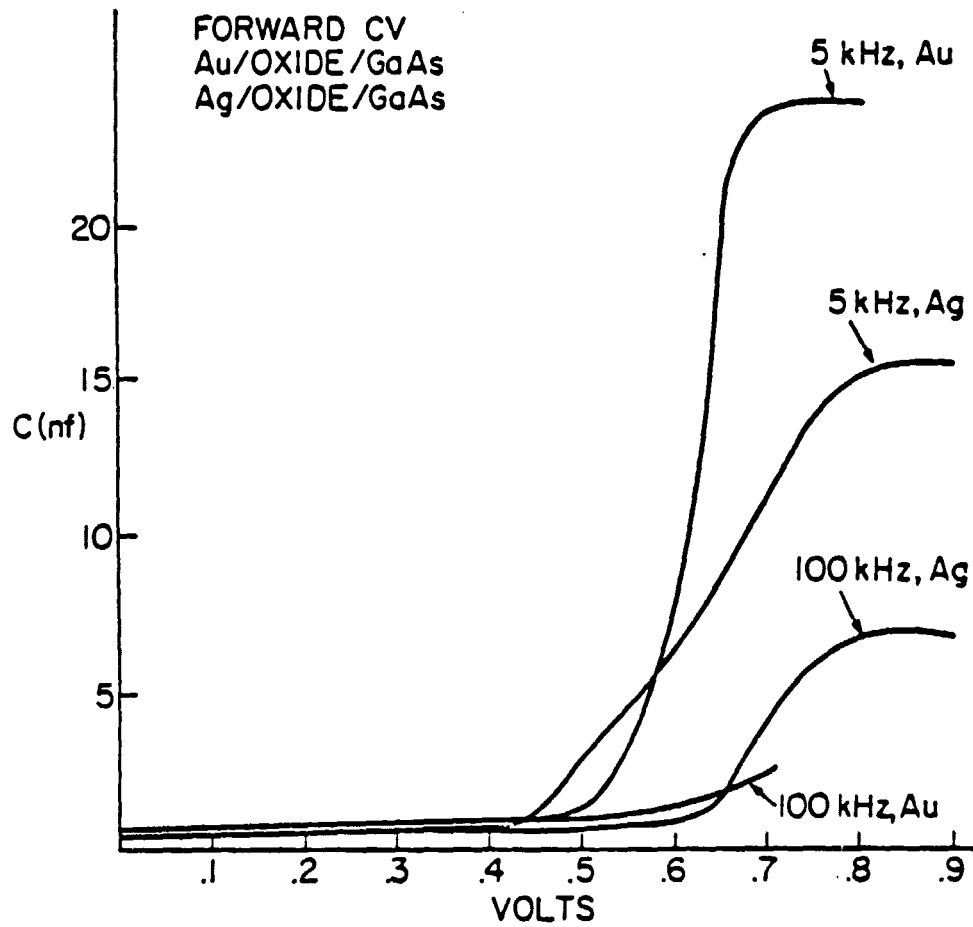


Fig. 1. Equivalent parallel capacitance vs. forward bias for typical Au and Ag devices.

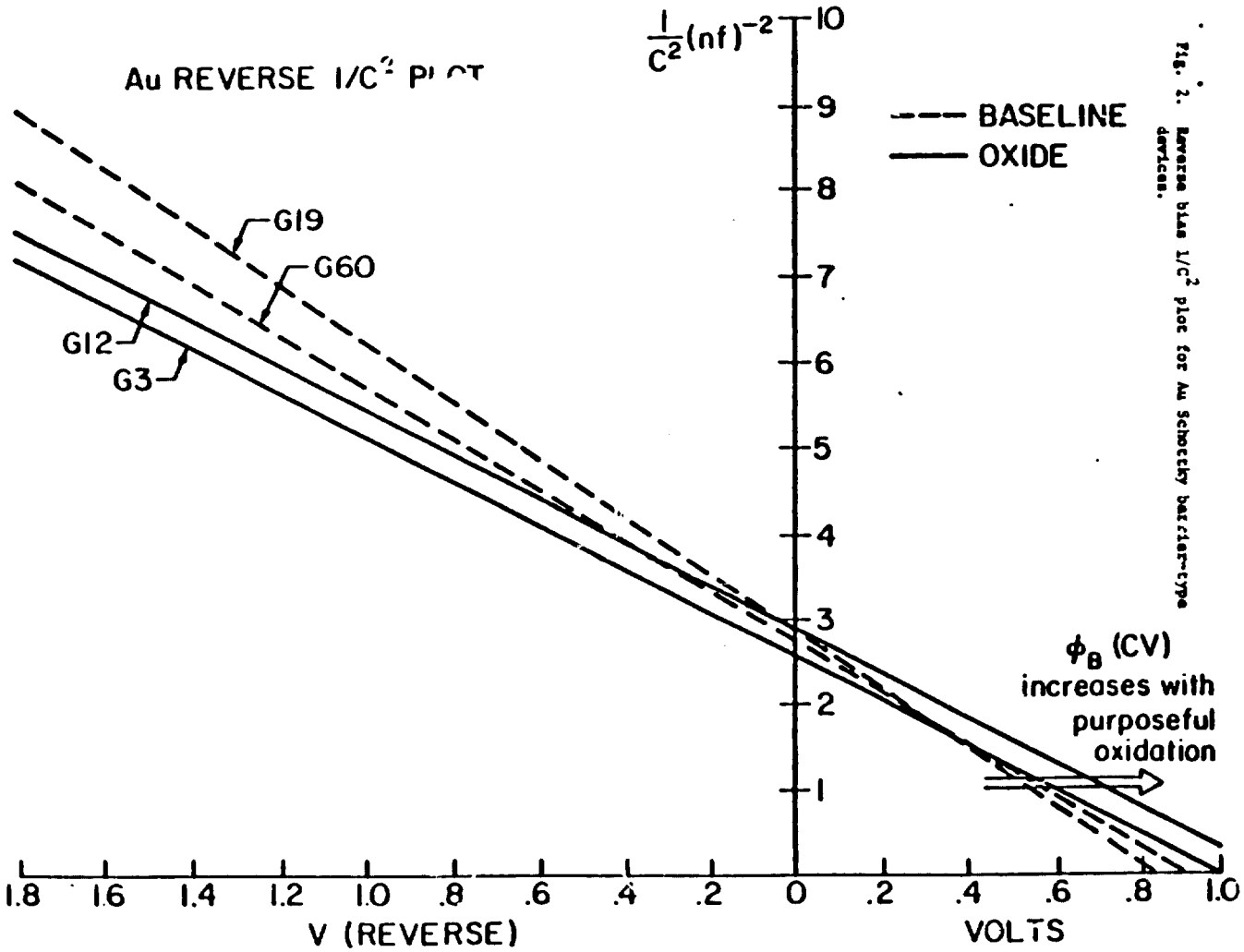


Fig. 2. Reverse bias $1/C^2$ plot for Au Schottky barrier-type devices.

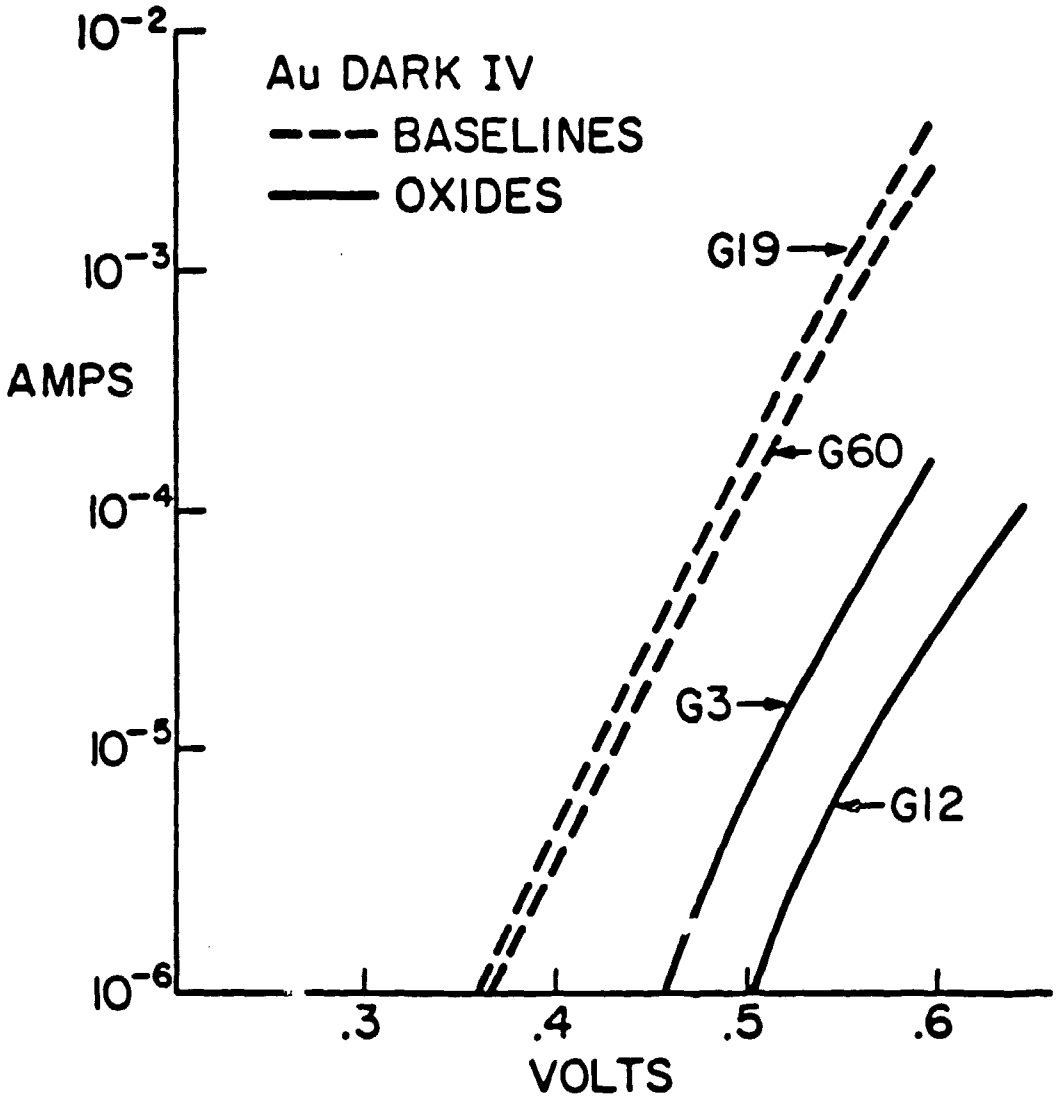


Fig. 3 Dark IV for Au Schottky barrier-type devices.

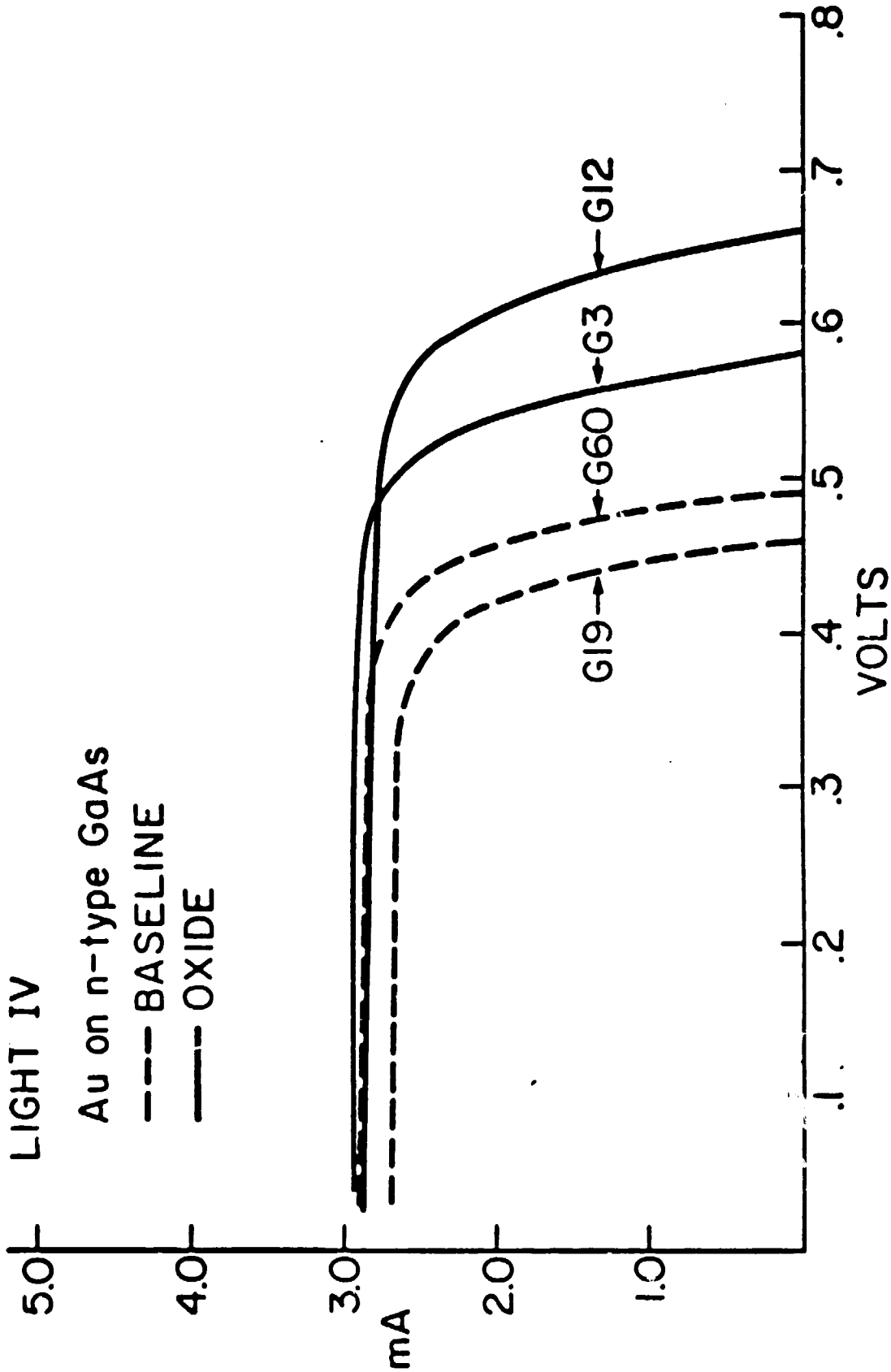


Fig. 4 Light IV for Au Schottky barrier-type devices.

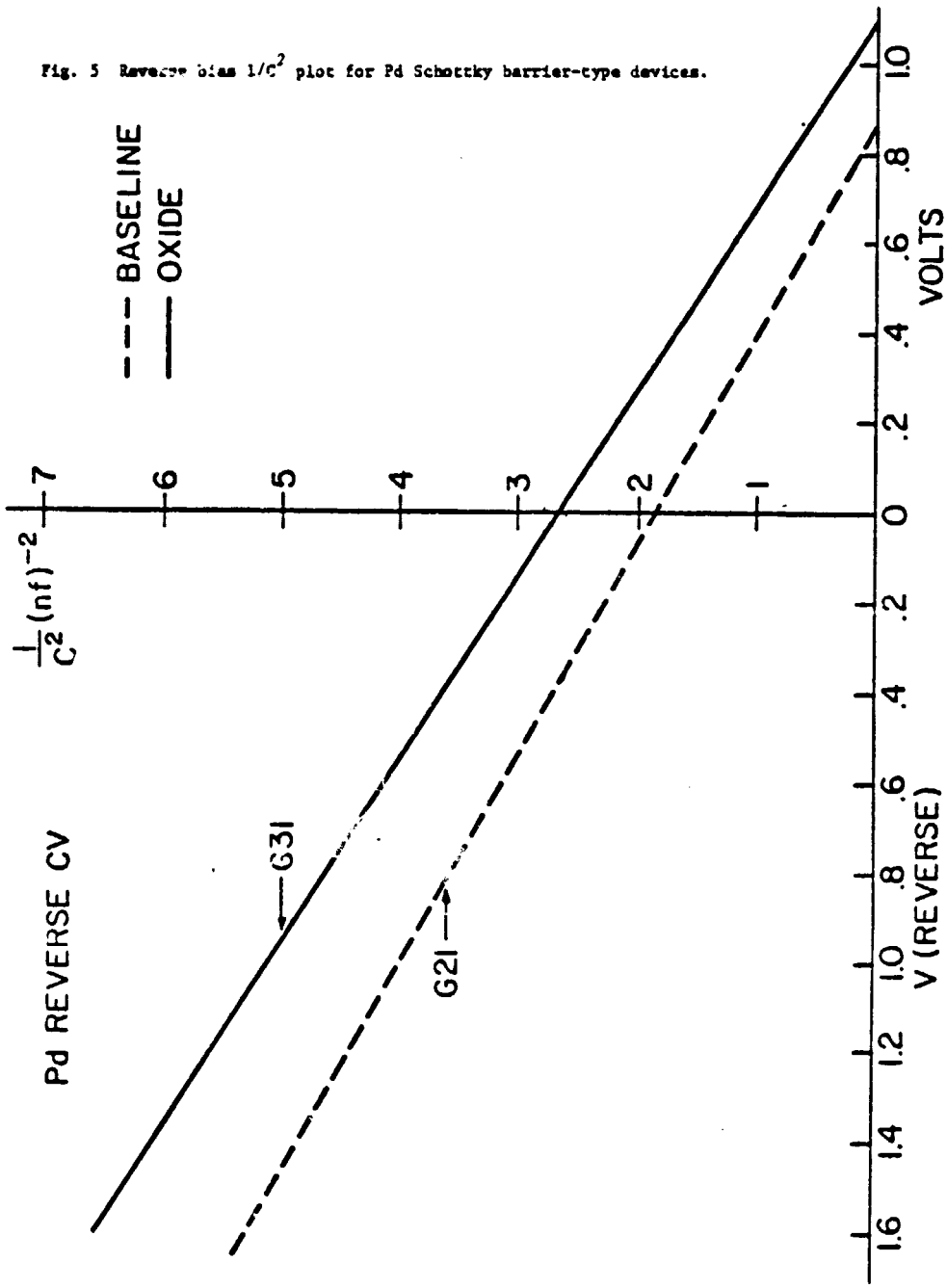


Fig. 5 Reverse bias $1/C^2$ plot for Pd Schottky barrier-type devices.

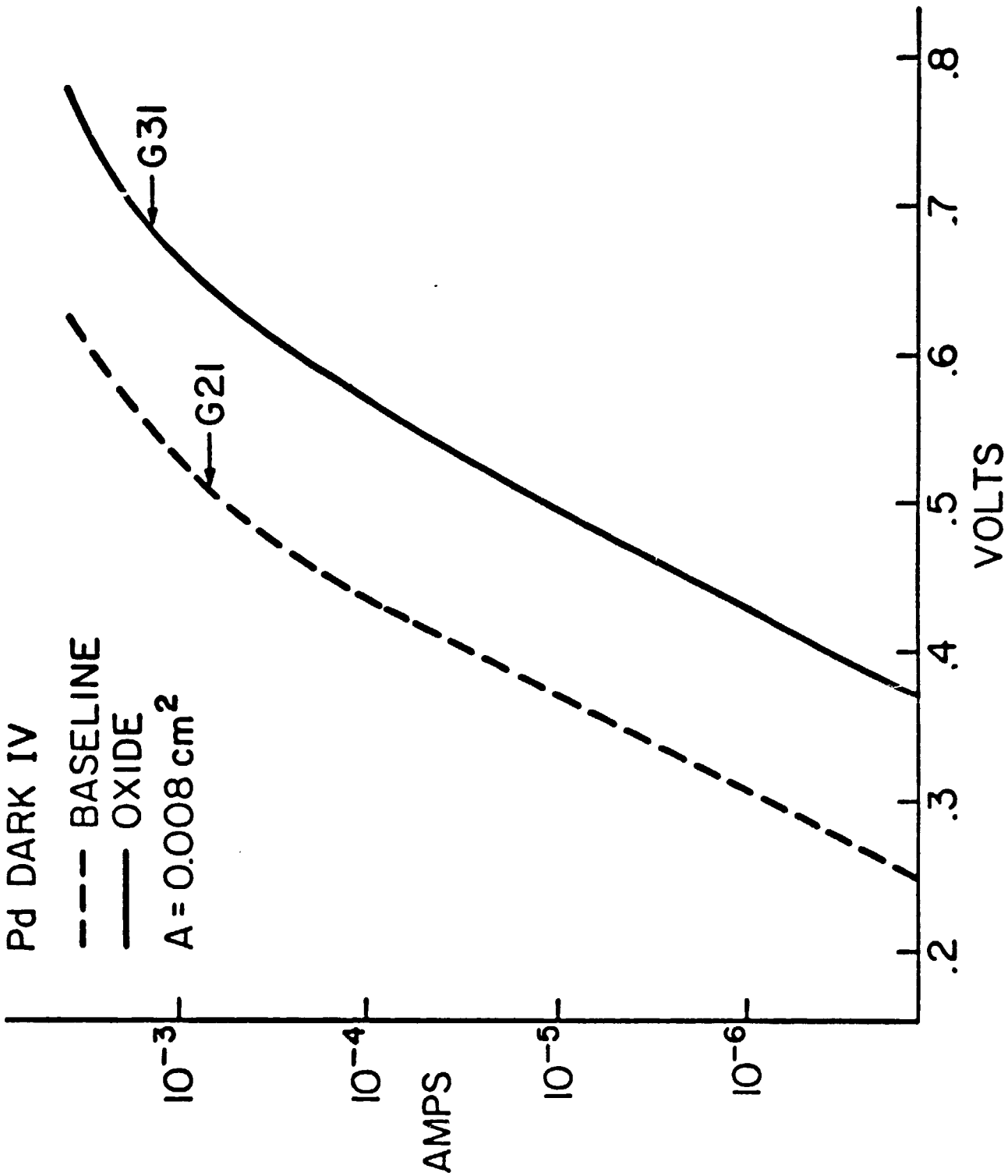


Fig. 6 Dark IV for Pd Schottky barrier-type devices.

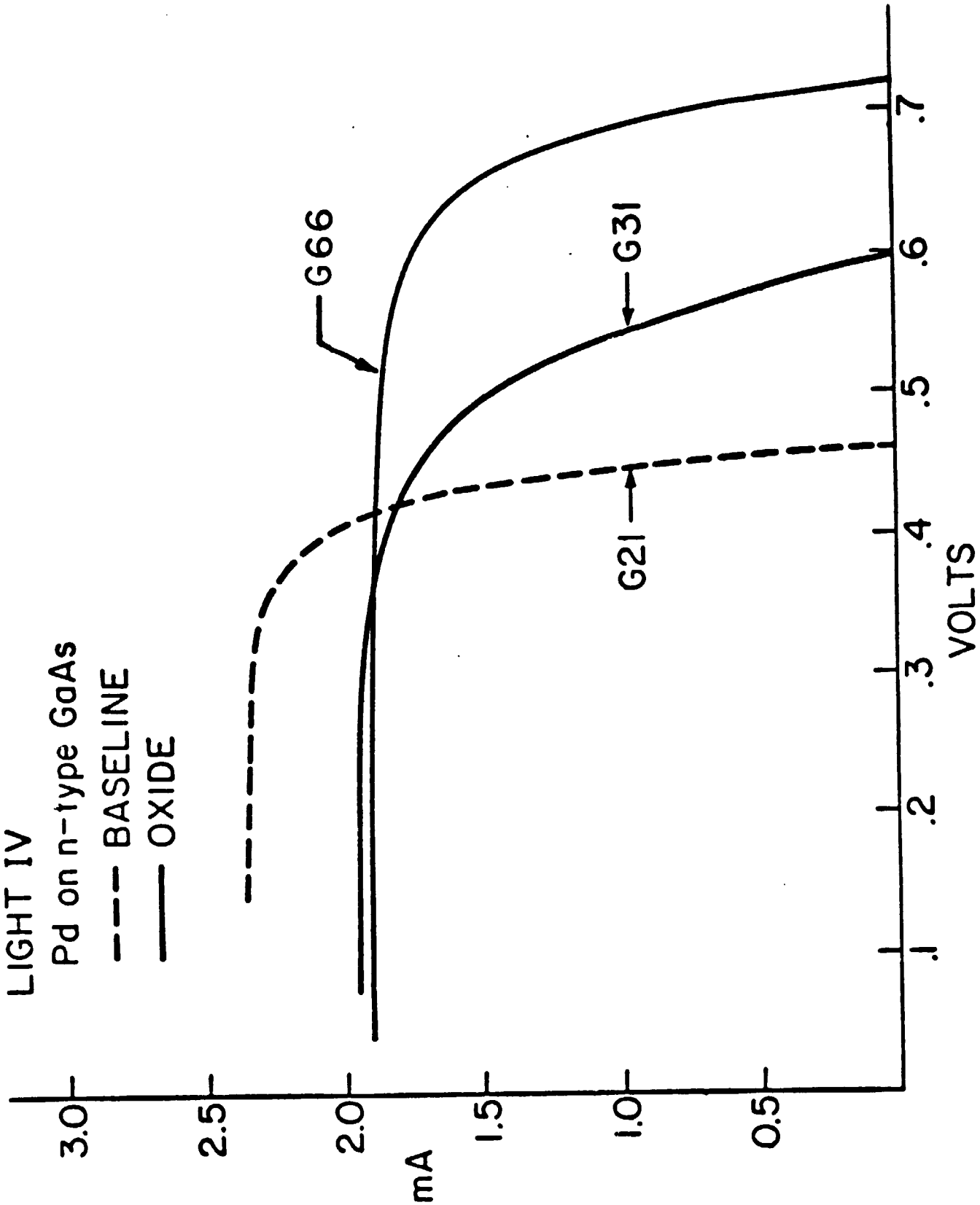
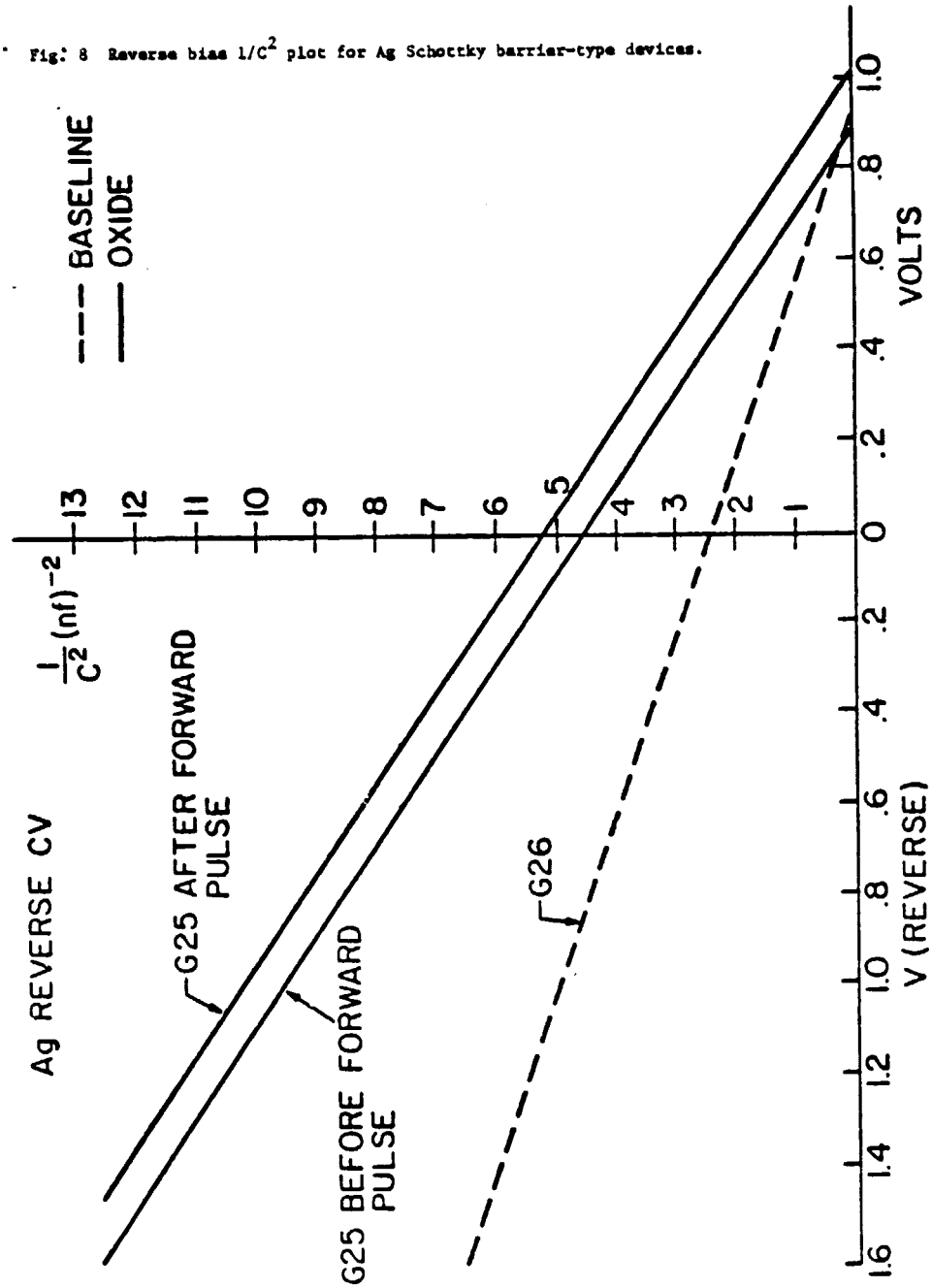


Fig. 7 Light IV for Pd Schottky barrier-type devices.

Fig. 8 Reverse bias $1/C^2$ plot for Ag Schottky barrier-type devices.



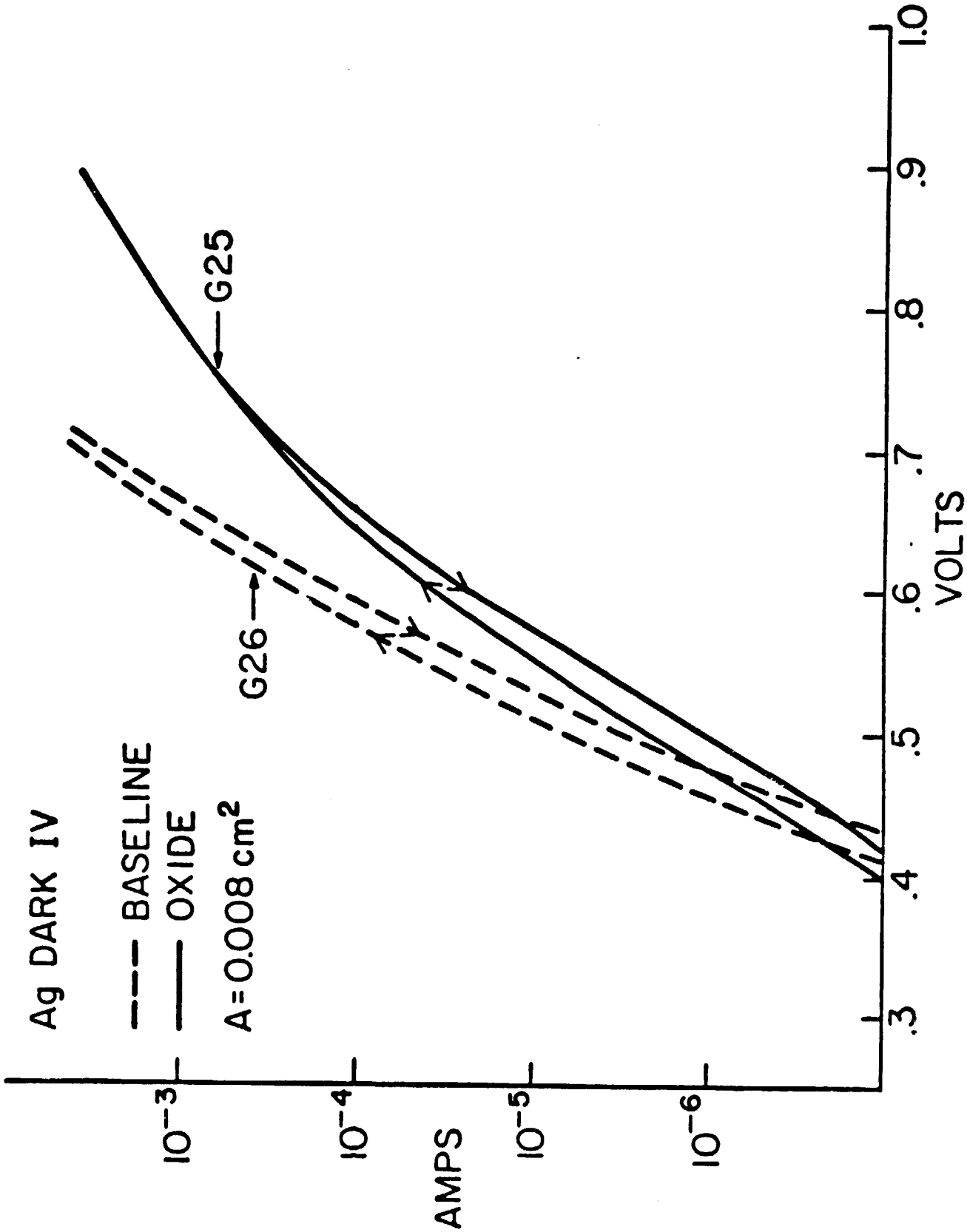


Fig. 9 Dark IV for Ag Schottky barrier-type devices.

Fig. 10 Light IV for Ag Schottky barrier-type devices.

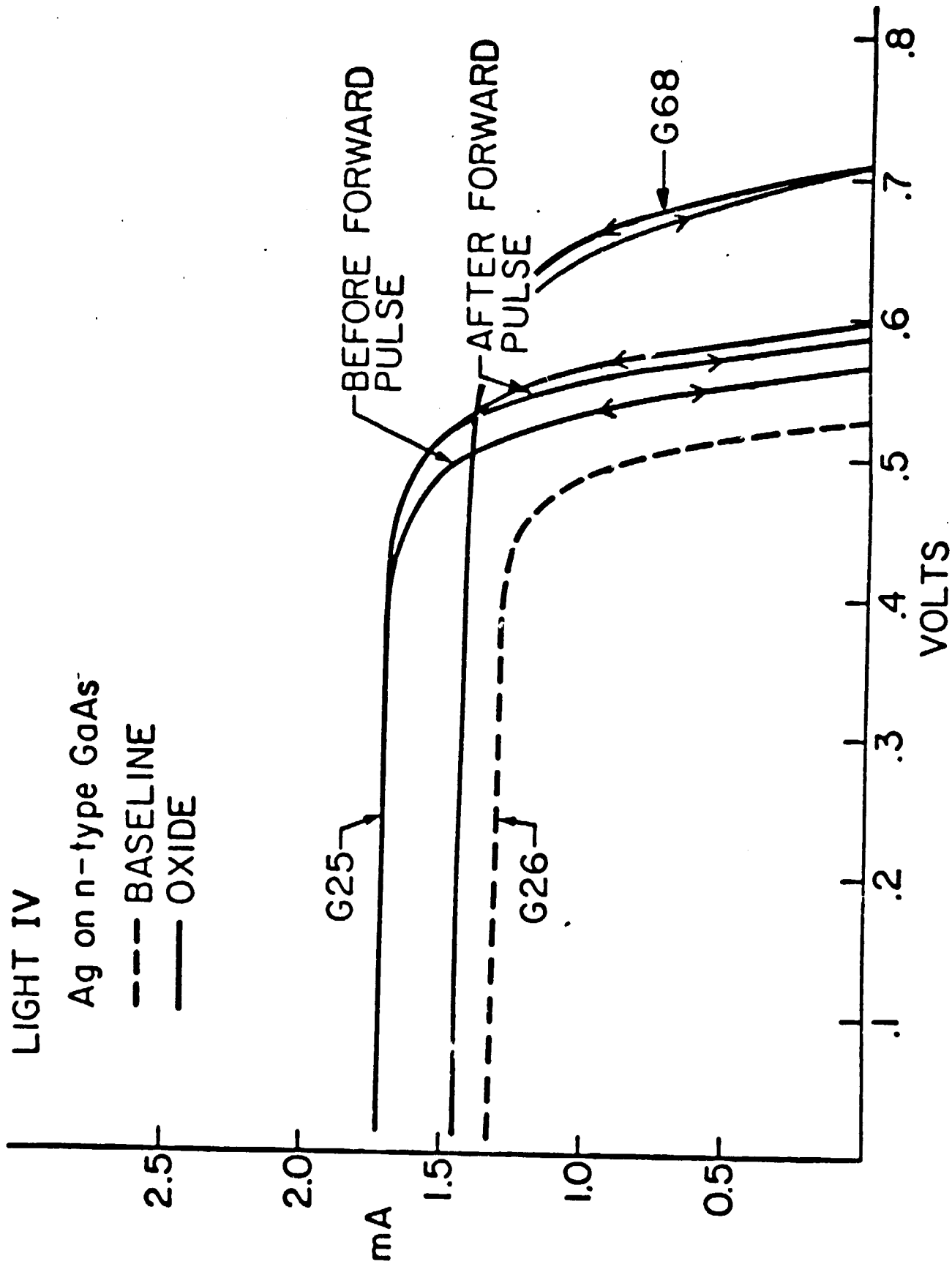
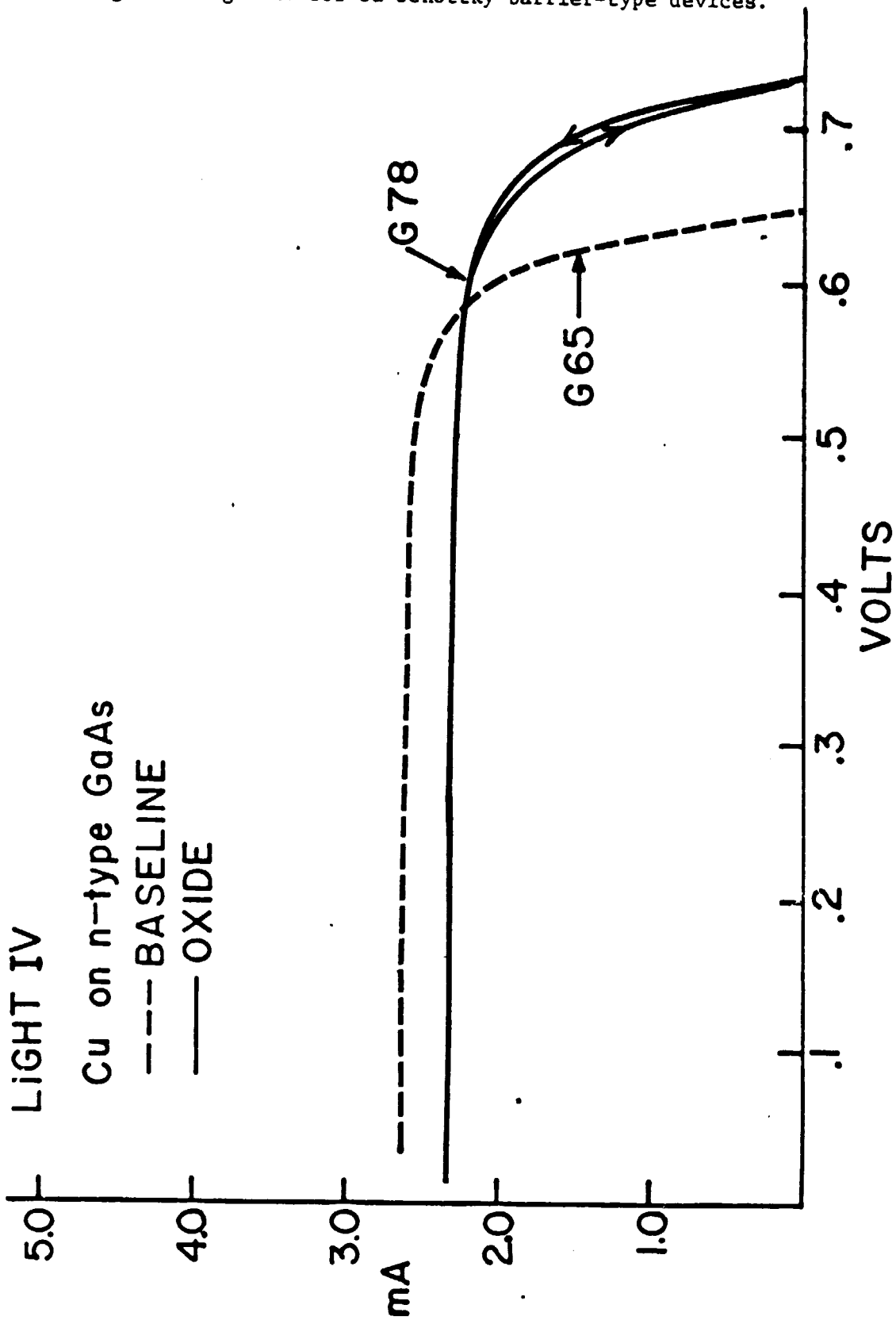


Fig. 11 Light IV for Cu Schottky barrier-type devices.



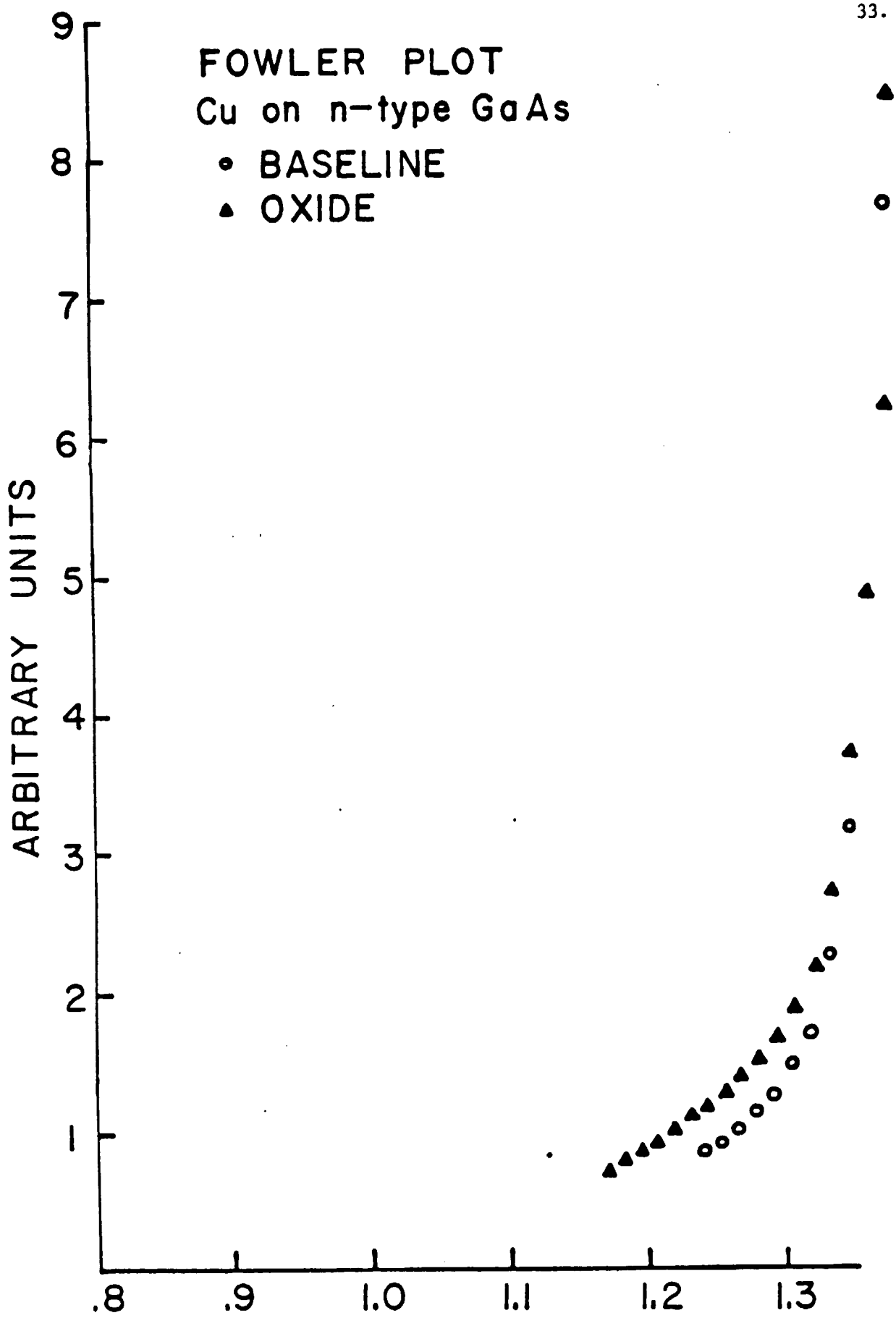
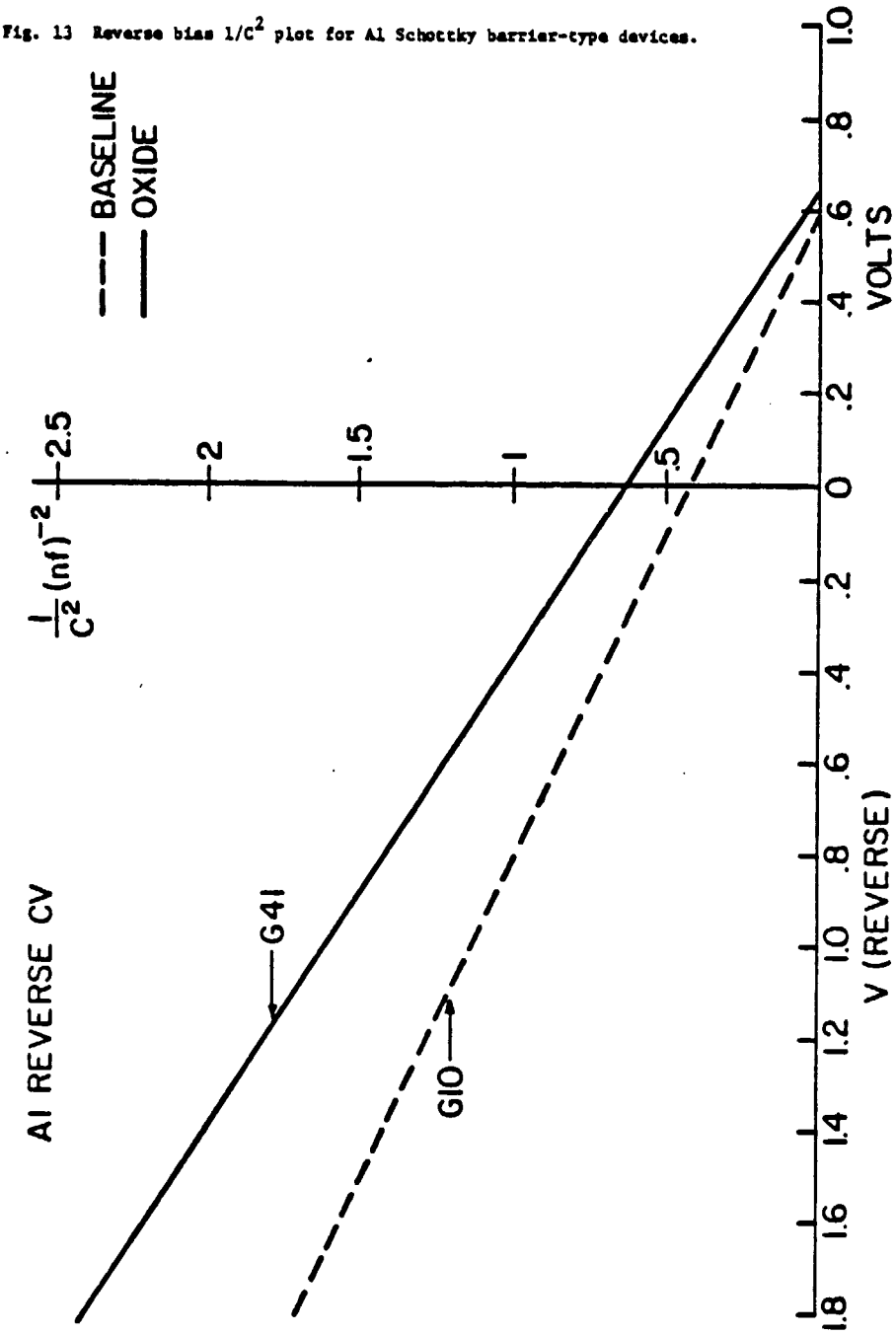


Fig. 12 Photoemission for Cu Schottky barrier-type devices.

Fig. 13 Reverse bias $1/C^2$ plot for Al Schottky barrier-type devices.



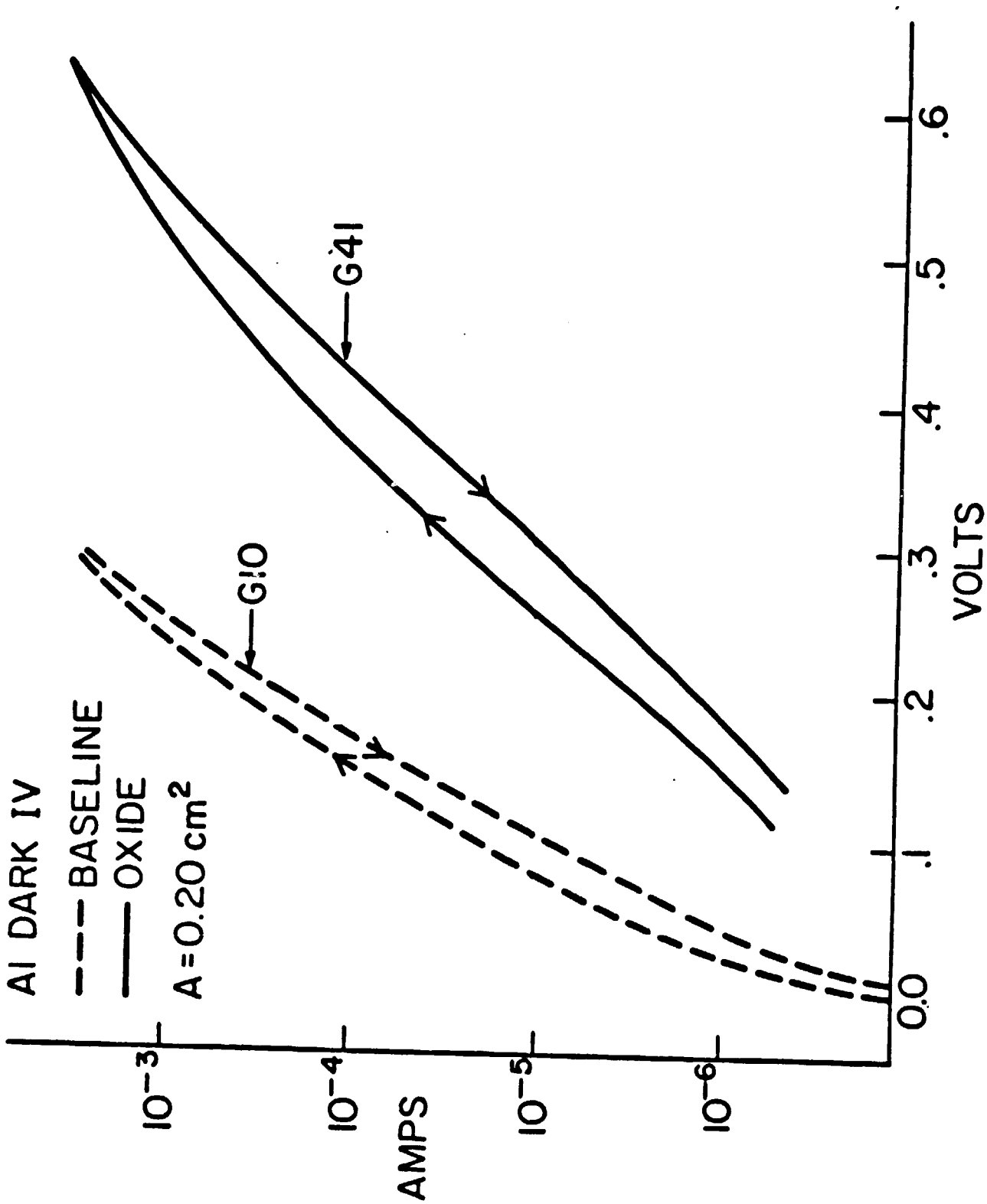


Fig. 14 Dark IV for Al Schottky barrier-type devices.

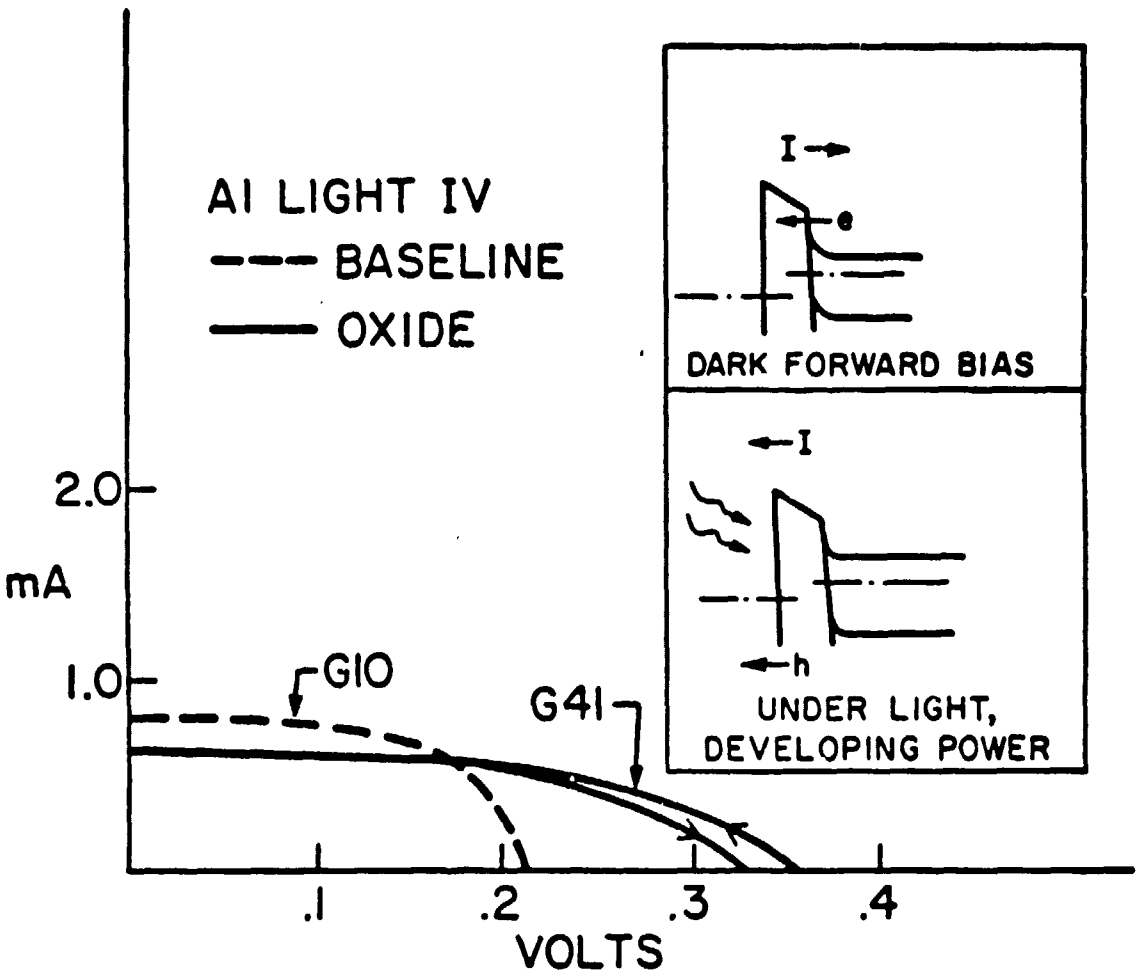


Fig. 15 Light IV for Al Schottky barrier devices. Inset shows mechanism for introduction and erasure of charge.

V. References

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VI. Publications Supported in Part or Entirely by this Contract

1. R. Childs, J. Fortuna, J. Geneczko, and S. J. Fonash, Proceedings of 12th IEEE Photovoltaic Specialists Conf. 862 (1976)

2. S. Fonash, J. Appl. Phys. 48, 3953 (1977).

3. R. Childs, J. M. Ruths, T. E. Sullivan, S. J. Fonash, J. Vac. Sci and Technol., to be published.

4. S. Fonash, T. Sullivan, R. Childs and J. Ruths, Proceedings of 13th IEEE Photovoltaic Specialists Conf. (1978), to be published.