NASA-CR-152, 169

FINAL TECHNICAL REPORT
August 1978

ASSESSMENT STUDY OF INFRARED DETECTOR ARRAYS FOR LOW-BACKGROUND ASTRONOMICAL RESEARCH

(NASA-CR-152169) ASSESSMENT STUDY OF INFRARED DETECTOR ARRAYS FOR LOW-BACKGROUND ASTRONOMICAL RESEARCH Final Technical Report (Analytical Decisions, Inc.) 98 p HC A05/MF A01 CSCL 03A G3/89

N79-10971

Unclas 36054

Contract No. NAS2-9858

For: National Aeronautics and Space Administration
Ames Research Center
Moffett Field, California 94035

NOV 1978
RECEIVED
NASA STI FACILITY

ANALYTIC DECISIONS INCORPORATED
1401 Wilson Boulevard
Suite 200
Arlington, Virginia 22209

NASA-CR-152, 169

ANALYTIC DECISIONS INCORPORATED
1401 Wilson Boulevard
Suite 200
Arlington, Virginia 22209

FINAL TECHNICAL REPORT

ASSESSMENT STUDY OF INFRARED DETECTOR ARRAYS FOR LOW-BACKGROUND ASTRONOMICAL RESEARCH

Contract No. NAS2-9858

For

National Aeronautics and Space Administration
Ames Research Center
Moffett Field, CA 94035

1 August 1978

Prepared by K. J. Ando
K. J. Ando
Senior Scientist

TABLE OF CONTENTS

Section or Paragraph	Title	Page
I	INTRODUCTION	1
	BACKGROUND AND STUDY GOALS	1
II	MONOLITHIC EXTRINSIC FOCAL PLANE ARRAYS	4
2.1	DOPANT CONSIDERATIONS FOR MONOLITHIC EXTRINSIC FOCAL PLANE ARRAYS	6
2.2	SPECTRAL RANGE AND QUANTUM EFFICIENCY	11
2.3	RESPONSIVITY	15
2.4	DETECTIVITY AND NEP	23
2.5	Si:X CHIP DESIGN AND OPERATION	29
2.6	Si:X CHIP PERFORMANCE	32
III	MONOLITHIC INTRINSIC FOCAL PLANE ARRAYS	39
3.1	InSb CCD	40
3.2	InSb CCD PERFORMANCE CHARACTERISTICS	42
3.3	MULTILAYER MONOLITHIC INTRINSIC ARRAYS	47
IV	CHARGE INJECTION DEVICE (CID)	51
V	HYBRID FOCAL PLANE ARRAYS	63
5.1	HYBRID FOCAL PLANE CONFIGURATIONS	64
5.2	DETECTOR TYPES FOR HYBRID ARRAYS	68
5.3	DETECTOR/CCD COUPLING	78
VI	CONCLUSIONS	88
REFERENCES		91

TITLES OF FIGURES

Figure Number	Title	Page
2.1	Impurity levels in silicon	9
2.2	Quantum yield versus absorptance (αL) for a longitudinal detector	12
2.3	Quantum efficiency versus detector thickness and doping concentration for Si:In	14
2.4	Spectral absorption coefficient of Si:X	16
2.5	Photoconductive spectrum at 20K for sample of Si:In	17
2.6	Si:Ga spectral response	18
2.7	Responsivity and noise of Si:In detector as a function of temperature	20
2.8	Responsivity versus temperature and bias for a Si:Ga detector	21
2.9	Responsivity as a function of frequency for a Si:In discrete detector	24
2.10	Detectivity of Si:In as a function of temperature	27
2.11	Si:Ga D* as a function of temperature for various background photon flux densities	28
2.12	Circuit diagram of the 2x32 2096 array	30
2.13	Si:X chip cross-section	31
2.14	NEP versus integration time for a Si:X chip	38
3.1	Photomicrograph of a 20-element InSb CCD	42
3.2	Schematic diagram of 4ϕ overlapping gate 20-element imager: 8585 design	42
3.3	Theoretical reduction of dark current with temperature for InSb	46
3.4	Multilayer monolithic intrinsic structure	48
4.1	Schematic diagram of a two-dimensional InSb CID focal plane array configuration	52
4.2	Representative CID noise equivalent circuit	56
4.3	Calculated noise equivalent carriers of all noise sources versus background photon flux for a 16x24 InSb CID array	59

Figure Number	Title	Page
4.4	Measured RMS noise carriers of all noise sources vs. background photon flux for a 32-element InSb CID line array	59
4.5	Calculated maximum integration time vs. incident background flux for a InSb CID array	62
5.1	Detector material compatibility with silicon: Percent contraction from 300K	65
5.2	Hybrid structure employing direct epoxying of detector array to CCD	66
5.3	Hybrid structure using flip-chip bonding of detector array to CCD	66
5.4	Performance data on a recently measured backside-illuminated InSb array	70
5.5	Measured quantum efficiency vs. wavelength for backside-illuminated InSb detectors	71
5.6	Backside-illuminated device design	73
5.7	Experimentally measured absolute spectral response curves for three different backside-illuminated InAsSb devices	74
5.8	Relative spectral response at 85K for $Pb_{0.8}Sn_{0.2}Te/PbTe$ and $Pb_{0.76}Sn_{0.24}Te/PbTe$ diodes	75
5.9	D* as a function of R_oA product for an $InAs_{.85}Sb_{.15}$ detector at 77K	77
5.10	Zero-bias R_oA product as a function of temperature for two $InAs_{1-x}Sb_x$-InAs detectors	80
5.11	Direct injection (source input) interface circuit	82
5.12	Gate modulation input circuit with buffer amplifier	82
5.13	AC-equivalent circuit of the direct injection input	83
5.14	Injection efficiency as a function of g_m for $R_D = 10^8$ and 10^9 ohms	86

I. INTRODUCTION

BACKGROUND AND STUDY GOALS

This report will present the results of a study, "Assessment Study of Infrared Detector Arrays for Low-Background Astronomical Research," performed by Analytic Decisions Incorporated, Arlington, Virginia, for the NASA-Ames Research Center under Contract NAS 2-9858. The basic purpose of this report was to survey and assess the current state-of-the-art of infrared detector arrays employing CCD or CID readout and determine the applicability, limitations and potentials of such arrays under the low-background astronomical observing conditions of interest for SIRTF.

Cryogenically cooled shuttle-borne telescopes, such as the Shuttle Infrared Telescope Facility (SIRTF) will provide a unique opportunity for high sensitivity and high resolution observations of faint astronomical objects. A preliminary design study has been completed for SIRTF[1] and the Focal Plane Instruments and Requirements Science Team (FIRST) has been engaged in the definition and conceptual design of the photometric and spectroscopic instruments for SIRTF.[2]

Many of the instruments currently being defined by the FIRST group will require arrays of detectors rather than discrete detectors. Historically, past probe and spaceborne instruments for long wavelength infrared (LWIR) celestial survey and background measurements have employed discrete detectors in staggered linear or linear arrays. The infrared survey arrays, currently under development for IRAS, are examples of this approach. Arrays of this type, which incorporate extrinsic doped germanium and silicon detectors, have provided excellent performance at low background. The cost of these arrays, however, on a per detector channel basis has been high, reflecting the

low yields associated with detector fabrication, number of associated parts, and the critical hand wiring involved. Additionally, as the requirement for the number of detectors increases, this approach is ultimately limited in performance by the relatively large size of discrete detectors, interconnect complexity, and power dissipation. One approach to overcome this limitation has been to adapt the microelectronic batch processing techniques to fabricate integrated arrays of detectors, load resistors, and MOSFET preamplifiers. The general characteristics of a Si:As integrated array based upon this approach were recently reported.[3]

A second and more powerful and versatile approach to integrate the detector and signal processing functions on-chip has evolved in recent years. This approach, based upon the charge transfer concept, has made possible for the first time the realization of practical high density self-scanned infrared arrays with integral low noise readout. The use of charge transfer devices allow signals from a large number of detectors to be multiplexed on-chip and read out through a single output amplifier, thereby reducing the parts count and interconnect complexity and making possible detector arrays with many thousands of individual detectors. This study will review the state of the art of such detector arrays.

Four general classes of infrared CCD detector arrays will be reviewed in this report. Section II will review the state of the art of monolithic extrinsic arrays. In monolithic extrinsic arrays, an extrinsic substrate provides the infrared sensitivity. The resultant signal charge is injected into a lightly doped epitaxial layer for charge transfer multiplexing and readout.

Section III will review the state of the art of monolithic intrinsic arrays. A monolithic intrinsic array is the IR analog of the visible imager CCD. IR detection occurs in a narrow

bandgap semiconductor such as InSb. Charge transfer and readout occurs either in the same material or signal charge is transferred to a wider bandgap layer for CCD readout.

Section IV will review charge injection devices (CID). Charge injection devices are monolithic intrinsic arrays which employ surface charge transfer to achieve X-Y address capability for area arrays. Signal readout occurs by a sequential injection of the stored charge into the substrate and detection of the resulting substrate current.

Section V will review hybrid arrays. Hybrid arrays employ separate sensing and charge transfer media. The detector array, fabricated in the photosensitive medium, is electrically and mechanically coupled to a silicon CCD multiplexer.

Section VI will compare the relative suitability and potentials of the various approaches for the low-background astronomical conditions of interest and summarizes the conclusions of this study.

II. MONOLITHIC EXTRINSIC FOCAL PLANE ARRAYS

The state of the art of infrared focal planes prior to the advent of charge transfer devices was based upon discrete detector arrays with individual load resistors and preamplifiers. The introduction of the charge coupling principle in 1970 led quickly to the investigation of the feasibility of extrinsic focal plane arrays.

A number of test chips, such as the CCD 2063,[4] were developed to test and validate the basic detector/CCD structure in monolithic form. This chip incorporated 8, 16, and 32 detector element linear arrays with integral CCD readout registers. CCD readout of extrinsic gallium doped silicon (Si:Ga) detectors was successfully demonstrated with this chip. Tests on this chip and other chips showed that reasonable charge transfer efficiencies could be obtained at operating temperatures as low as $8^{\circ}K$ in the conventional inversion mode of operation. Inversion or depletion mode of operation was made possible by the deposition of lightly doped epitaxial layer on the extrinsic substrate. The simpler accumulation mode of operation, in which signal charge is transferred as majority carriers in the photoconductive substrate, was also tried in the CCD 2063 and other test devices, but abandoned in favor of the inversion mode of operation due to poor charge transfer efficiency at the low temperatures of interest.

A number of extrinsic detector coupling schemes and features such as bucket overload protection (BOP) on each detector input and bucket background subtraction (BBS) circuit were also tested on the CCD 2063.

Experience gained in the design, fabrication, and evaluation of chips such as the CCD 2063 led to the development of a second generation extrinsic silicon test chip, the CCD 2096.[5]

The CCD 2096 provided a test vehicle for testing and evaluating a number of direct and indirect injection CCD readout structures. Additionally, the CCD 2096 incorporated monolithic 4x4 and 2x32 arrays with CCD readout and demonstrated for the first time the feasibility of two dimensional mosaic staring arrays.

Development of the CCD 2096 chip was sponsored by the Defense Advanced Research Project Agency (DARPA), the Air Force, and the Army. Extensive development and evaluation of the test structures of the CCD 2096 were conducted for these sponsors. The most extensive of these efforts was the DARPA CCD^2 program.

Specific applicable devices on the CCD 2096 were also tested under an Air Force program.[6] The objective of this program was to investigate monolithic Si:Ga detector arrays for 8 to 14 μm infrared imaging with on-chip signal processing. The results were used to design a Si:Ga time delay and integration (TDI) chip. Si:In TDI arrays on the CCD 2096 chip were also evaluated in the direct injection mode under the Army's MOSIS program. Finally, the CCD 2096 has been evaluated at low backgrounds for LWIR staring applications under Army sponsorship. A CCD 2096 process compatible with a Si:As substrate was developed and evaluated.

In parallel with the development of the CCD 2096, a Si:Ga monolithic array for low background applications was developed under DARPA/Air Force sponsorship. The design of the chip was very simple for high yield and incorporated a unique injection scheme for efficient detector/CCD coupling at low backgrounds.

The successful fabrication and demonstration of extrinsic silicon focal plane chips would not have been possible without

the advances made in the growth and fabrication of quality extrinsic silicon materials. Extensive materials development work to dope and grow high quality silicon crystals during this period brought extrinsic detector materials such as Si:In and Si:Ga to the stringent quality levels required for focal plane arrays.

DOD development efforts continue to advance the state of the art of extrinsic focal plane chips and materials technology. New generations of test chips and arrays incorporating larger numbers of detectors and on-chip functions involving more sophisticated fabrication processes are currently in development. Several significant milestones which reflect the relative maturity of this technology have been recently achieved. Under DARPA sponsorship, a 12 chip mosaic focal plane, complete with drive and readout electronics and an integral dewar, was delivered to a contractor for integration into a flight sensor. This represents the first transition of this technology into practical hardware.

2.1 DOPANT CONSIDERATIONS FOR MONOLITHIC EXTRINSIC FOCAL PLANE ARRAYS

Monolithic extrinsic arrays use an extrinsic substrate as the infrared detector. The substrate is biased such that the detectors operate in the photoconductive mode. Although intrinsic photoconductivity in silicon is limited to 1.1 μm, infrared response can be obtained by extrinsic photoconductivity. Extrinsic photoconductivity occurs when specific impurities occupy localized energy levels within the bandgap. Extrinsic photoconductivity is associated with transitions from these levels to the band continuums. Measured impurity ionization energies in silicon range from 0.033 eV (Li donor level) to 0.55 eV (Zn acceptor level).[7] The corresponding cutoff wavelengths range from 2 μm (Si:Zn) to 38 μm (Si:Li). Longer wavelength cutoffs can be obtained with germanium where impurity ionization energies as low as 0.01 eV (Ge:Ga, Ge:B) have been observed. The

technology of germanium doped extrinsic discrete detectors was developed during the past 20 years to a high level of maturity and remains the highest performance approach for long infrared (50-120 μm) applications. Detailed information on impurity photoconduction in germanium and silicon can be found in the recent comprehensive review paper by Bratt.[8]

Monolithic extrinsic focal plane array development, however, has concentrated on impurity doped silicon because of its important advantages over germanium as a host crystal. The major practical reason has been the availability of a well developed CCD and LSI device technology in silicon. High interface state densities and the lack of a suitable passivation process are the major obstacles which prevent viable CCD operation in germanium. Secondary advantages of silicon are the higher practical doping concentrations resulting in thinner substrates and a lower dielectric constant which results in shorter detector time constants. Table I is a summary of the available properties of extrinsic silicon detectors.[9] Figure 2.1 summarizes the ionization energies and cutoff wavelengths λ_c for these dopants. Detailed performance data on some of the detectors in Table I can be found in References 12 and 13.

Of the detector materials listed in Table I, only a few have been developed into monolithic focal plane arrays. The number of applicable dopants for viable focal planes in a monolithic structure is limited because of a number of important requirements which it must satisfy simultaneously:

1. The dopant must be electrically active from a single dominant impurity level in the temperature range of interest. Many dopants can exist in more than one level because of multiple charge states or the formation of complexes with other types of impurities in the host lattice. Compensation of such multiple level

TABLE I. EXTRINSIC SILICON DETECTOR PARAMETERS

Detector	Type	ΔE eV	λpk μ	λ½ μ	A(λpk) $10^{-15}cm^2$	m*/m	g	B cm^3sec^{-1}	Solubility 10^{19}atoms/cm^3	Distribution Coefficient
Si.Tm	n	0.49	--	--	--	1.08	2	--	--	--
Si Yb	n	0.33	--	--	--	1.08	2	--	--	--
Si Zn	P	0.33	3.0	3.7	0.2	0.59	4	$4.5x19^{-8}$(80-200°K)	0.006	$1.1x10^{-5}$
Si Ni	P	0 23	2.0	3 6	--	0.59	4	--	--	--
Si Te	P	0 2	--	4.8	--	--	-	--	--	0.01
Si Cu	P	0 25	3.75	4 9	0.005	0.59	4	--	--	--
Si:Te	P	0 26	3 5	4.2	--	0.59	4	--	--	--
Si·Ni	P	0.23	--	5.4	--	--	-	--	--	0 6
Si Be	P	0.191 0.145	6.0	7 4	0.0051	0.59 0.59	4 4	-- --	-- --	-- $<1.6x10^{-7}$
Si S	n	0.18	--	6.9	--	--	-	--	0.003	--
Si In	P	0.155	5.2	8 0	0.033	0.59	-	$1.3x10^{-6}$78°K $2x10^{-6}$(70-100°K)	--	$4.1x10^{-4}$
Si.Te	n	0.14	--	8.9	--	--	-	--	>0 003	--
Si:Mg	n	0.11	--	11.2	--	--	--	--	>0.0002	--
Si:Bi	n	0 069	16.5	18.6	0.7	1.08	2	$1.4x10^{-5}$(1-4°K)	0.082	$7\ 1x10^{-4}$
Si:Ga	P	0 065	15.01	17 0	0.56	0.59	4	$1\ 5x10^{-6}$30°K	4.0	0.008
Si.Al	P	0 057	14.6	18.2	0.85	0.59	4	--	2.0	0 002
Si:As	n	0 055	22 5	24.2	1 5	1 08	2	$5\ 2x10^{-6}$(1-4°K)	190	0.3
Si B	P	0.045	23 5	27.8	1 8	0 59	4	$1\ 0x10^{-5}$(1-20°K)	60	0.8
Si P	n	0.044	26.0	29 4	2.2	1 08	2	$6.9x10^{-6}$(1-4°K)	130	0.35
Si:Sb	n	0.039	28.8	31.5	7.2	1 08	2	$1.8x10^{-6}$(1-4°K)	6.8	0.023

ORIGINAL PAGE IS
OF POOR QUALITY

ORIGINAL PAGE IS
OF POOR QUALITY

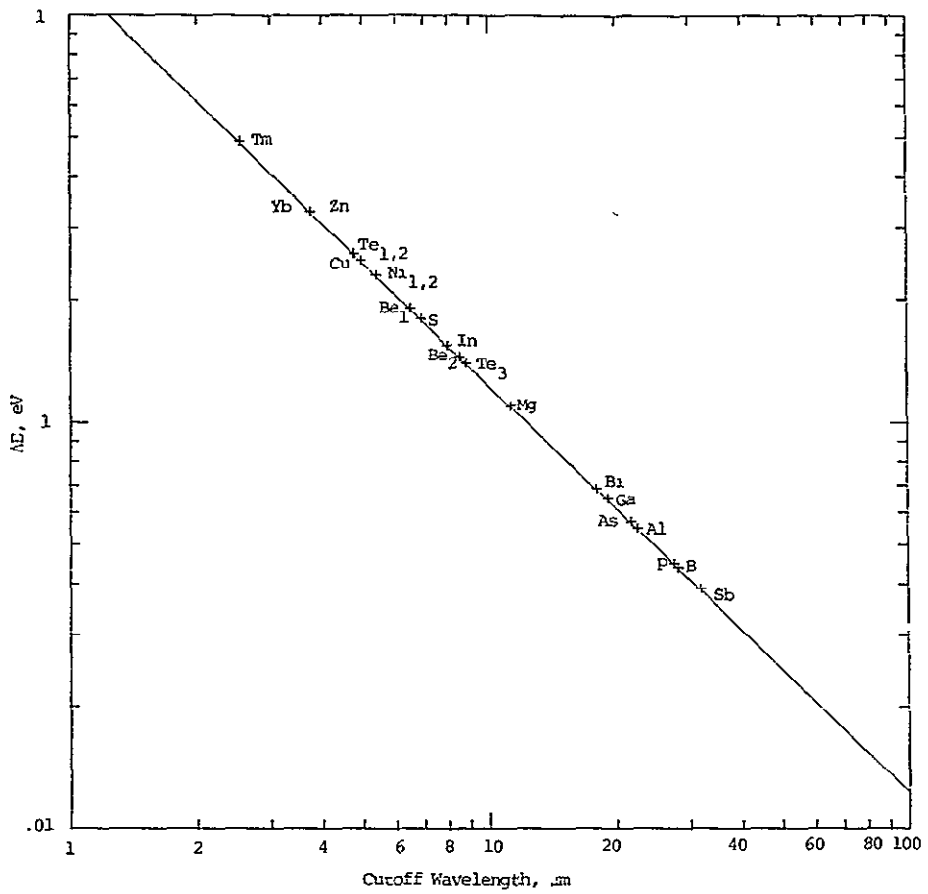


Figure 2.1 Impurity levels in silicon

dopants is difficult and resultant excess free carrier generation can reduce the operating temperature for background limited performance.

2. The solid solubility and photoionization cross section must be high and its segregation coefficient and other growth parameters must be favorable so that the dopant can be incorporated in the host crystal in concentrations near the solubility limit for high quantum efficiency in layers of minimum thickness. Detector substrates for focal plane arrays must as a rule be thinner than discrete detectors to minimize crosstalk between detectors. Additionally, for some dopants, the maximum impurity concentration is limited to values lower than the solubility limit due to impurity band conduction. A case in point is Ga, where the impurity conduction limit is about $5 \times 10^{16}/cm^3$ compared to a maximum solid solubility of $4 \times 10^{19}/cm^3$.

3. The dopant must be compatible with the CCD device processing. CCD processing involves a number of high temperature processing steps. These steps tend to deplete the dopant from the silicon substrate. This makes it necessary to choose a dopant that is a slow diffuser.

To date, In, Ga, and As have been found to reasonably satisfy the criteria listed above and have been utilized in monolithic focal plane arrays. Other dopants have been tried but with less success. The search continues for alternate focal plane compatible dopants. The prime goal has been to find new deep level dopants that will operate at temperatures above 50K for greater flexibility in operating temperature and wavelength selection.

2.2 SPECTRAL RANGE AND QUANTUM EFFICIENCY

The spectral response characteristics of an impurity doped detector is determined primarily by the photoionization cross section σ_o, the detector thickness ℓ in the direction of incident radiation, and N the density of absorbing impurity atoms. The quantum efficiency of an extrinsic detector can be calculated from these parameters by the familiar expression,

$$\eta = \frac{(1-R)(1-e^{-N\sigma_o \ell})}{(1-Re^{-N\sigma_o \ell}} \tag{2.1}$$

where R is the reflection coefficient of the front surface ($R \sim .3$ for Si), $\alpha = \sigma_o(N_A - N_D)$ is the absorption coefficient. and $N_A - N_D$ is the net density of the majority dopant. This relation is applicable to both transverse detectors (bias applied perpendicular to the incident flux) and longitudinal detectors (bias parallel to the incident flux) for $N\sigma_o \ell \leq 1$. The longitudinal bias case is the one encountered in monolithic arrays. For large absorptances ($N\sigma_o \ell >> 1$), the quantum yield η_E differs for the two modes due to differences in the photocarrier generation profiles. The quantum yield for longitudinal detectors is given by[9]

$$\eta_E = \left[\frac{(\alpha L)^2(1-R_1)e^{-\alpha L}(R_2)^{\frac{1}{2}}}{(1-R_1R_2e^{-2\alpha L})\left[\tan^{-1}(R_2)^{\frac{1}{2}}-\tan^{-1}(R_2^{\frac{1}{2}}e^{-\alpha L})\right]}\right] \tag{2.2}$$

where R_1 and R_2 are the reflectivity of the front and rear surfaces of the detector. This equation takes into account the situation where reflections from the rear surface can increase the apparent absorption length. The quantum yield is shown for the longitudinal bias case for a number of R_1 and R_2 values in Figure 2.2. Note that the maximum value is obtained for $\alpha L \approx 1.5$.

Because extrinsic photoconductivity is associated with weak transitions, absorption coefficients for extrinsic detectors are low. Typically α ranges from 10 to 50 cm^{-1} compared to

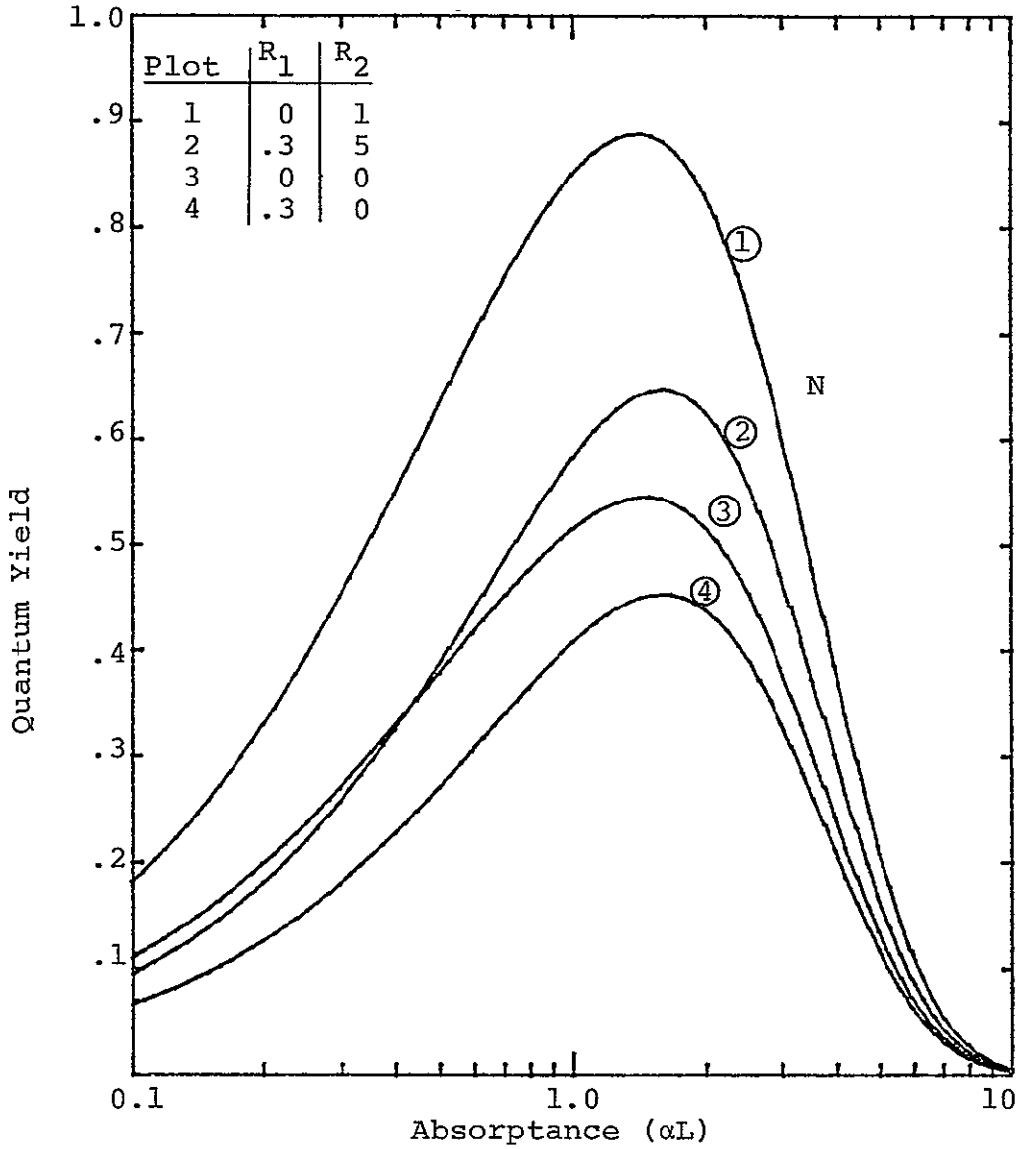


Figure 2.2 Quantum yield versus absorptance (αL) for a longitudinal detector

$\approx 10^4$ cm^{-1} for intrinsic semiconductors such as silicon in the visible and InSb in the 3-5 μm range. Long detector absorption lengths must therefore be utilized for reasonable quantum efficiency operation. Figure 2.3 shows the dependence of the quantum efficiency η on detector thickness and doping density N specifically for Si:In detectors.

While an absorptance value near 1.5 is desirable for maximum quantum efficiency, the choice of a detector thickness for monolithic focal planes is a complex trade involving the maximum solubility of the dopant, onset of impurity conduction, optical crosstalk, radiation susceptibility, and the thermal equilibrium density of carriers. The maximum solubility of In, for example, in silicon is about $1 \times 10^{18}/cm^3$, with an In concentration of about $5 \times 10^{17}/cm^3$ being the current practical limit for crystals grown by the Czochralski and float zone methods. A detector thickness of 0.05 cm has been found to be a reasonable compromise between quantum efficiency and optical crosstalk and is currently the preferred thickness for Si:In focal plane arrays. This corresponds to a $N\sigma\ell$ value of .33 and $\eta \approx .25$.

The spectral response of an extrinsic detector is determined by the wavelength dependence of the absorption coefficient σ. Theoretical photoionization cross sections have been derived for deep impurity levels based upon a delta function potential by Lucovsky.[10] The theoretical expression for the spectral shape of σ_o given by this model is,

$$\sigma_o = \frac{16\pi e^2}{3nm^*c}\left(\frac{\varepsilon_{eff}}{\varepsilon_o}\right)^2 \left[\frac{\Delta E^{\frac{1}{2}}(1.24/\lambda - \Delta E^{3/2}}{(1.24/\lambda)^3}\right] \qquad (2.3)$$

where n is the refractive index, m* is the scalar for the effective mass in the valence or conduction band, and $\varepsilon_{eff}/\varepsilon_o$ is a factor by which the electric field differs from the average value in the semiconductor. The spectral shape of σ_o depends upon

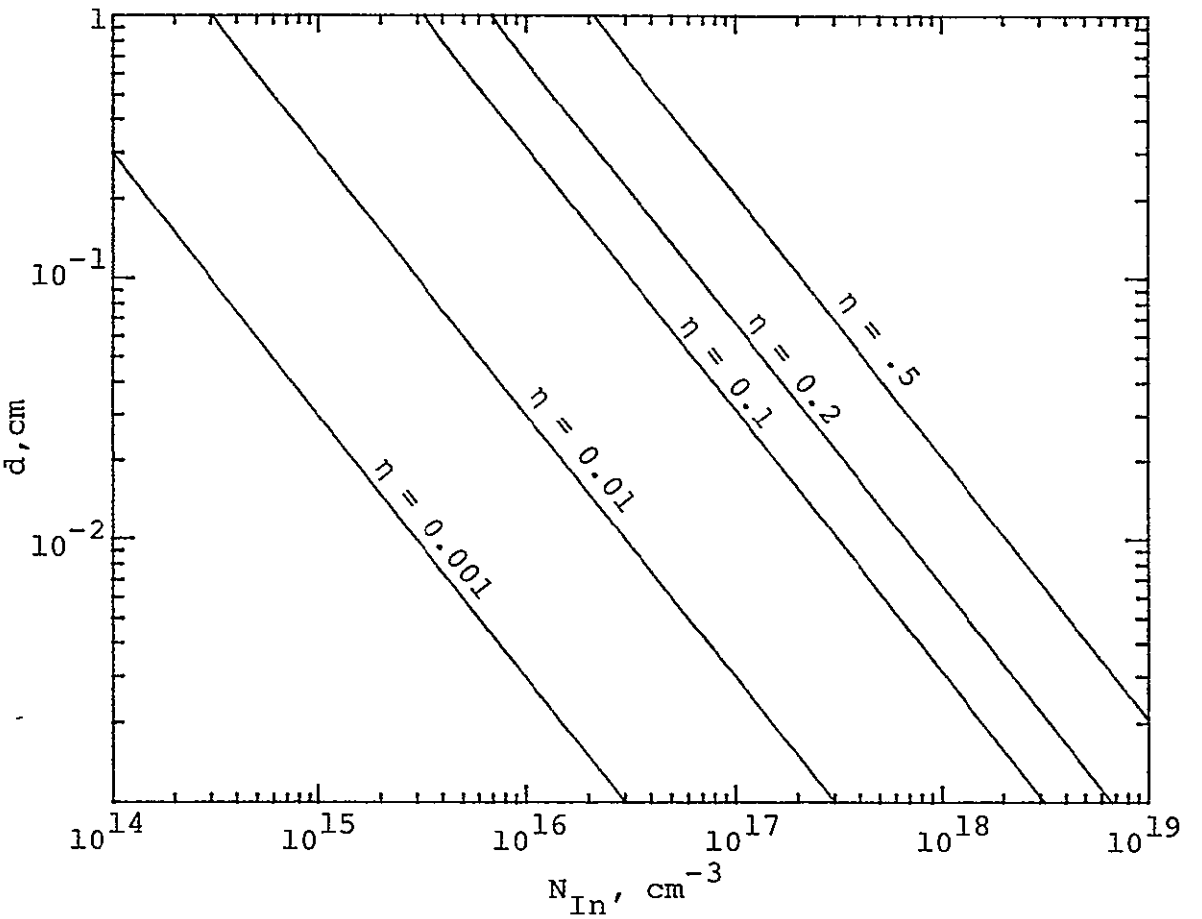


Figure 2.3 Quantum efficiency vs. detector thickness and doping concentration for Si:In (σ_o = $3.3 \times 10^{-17} cm^2$ at 4.1 μm)

whether the dopant is a shallow or deep level. Dopants with shallow levels have spectral responses with the peak absorption located near the absorption edge, $\lambda_p \approx \lambda_c$. On the other hand, dopants with deep levels have their peaks at $\lambda_p \approx \lambda_c/2$. This is illustrated in Figure 2.4 where the theoretical photoionization cross section is fitted to experimental spectral response data for Si:In (λ_c = 8 μm) and Si:Ga (λ_c = 17 μm).

Extensive spectral response data has been obtained on these two dopants in the course of the development of these materials for focal plane arrays. Figure 2.5 shows a detailed photoconductive spectrum of a Si:In detector at 20°K.[11] These measurements have revealed the presence of a second acceptor level at 0.111 eV which extends the response out to 11.2 μm. Additionally, photoconductivity beyond 11 μm is observed due to excited state photoconductivity from the In centers. Although not significant from a spectral response standpoint since these contributions are small (< 1% of the peak In response), the presence of the .111 eV level is of importance for the operation of Si:In detectors since it can significantly reduce the maximum temperature at which background limited performance is obtained.

Figure 2.6 shows the spectral response of a Si:Ga monolithic detector.[6] Monolithic detectors are individual test detectors incorporated in CCD test chips which permit on-chip evaluation of detector performance without the complexities of CCD readout. The peak response is at about 14 μm. The dip at 3 μm is probably due to H_2O absorption. Spectral response data on a number of other dopants can be found in the reviews by Bratt[8] and Sclar.[12,13]

2.3 RESPONSIVITY

The responsivity of an infrared detector is given by

$$R = \frac{I_s}{A_d H} \tag{2.4}$$

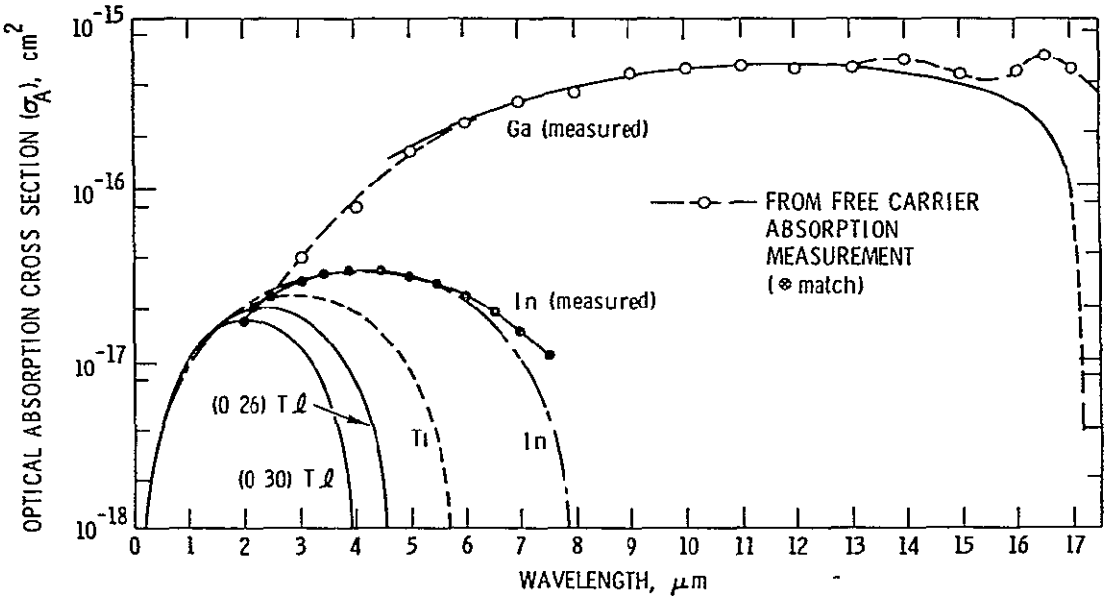


Figure 2.4 Spectral Absorption Coefficient of Si:X

ORIGINAL PAGE IS
OF POOR QUALITY

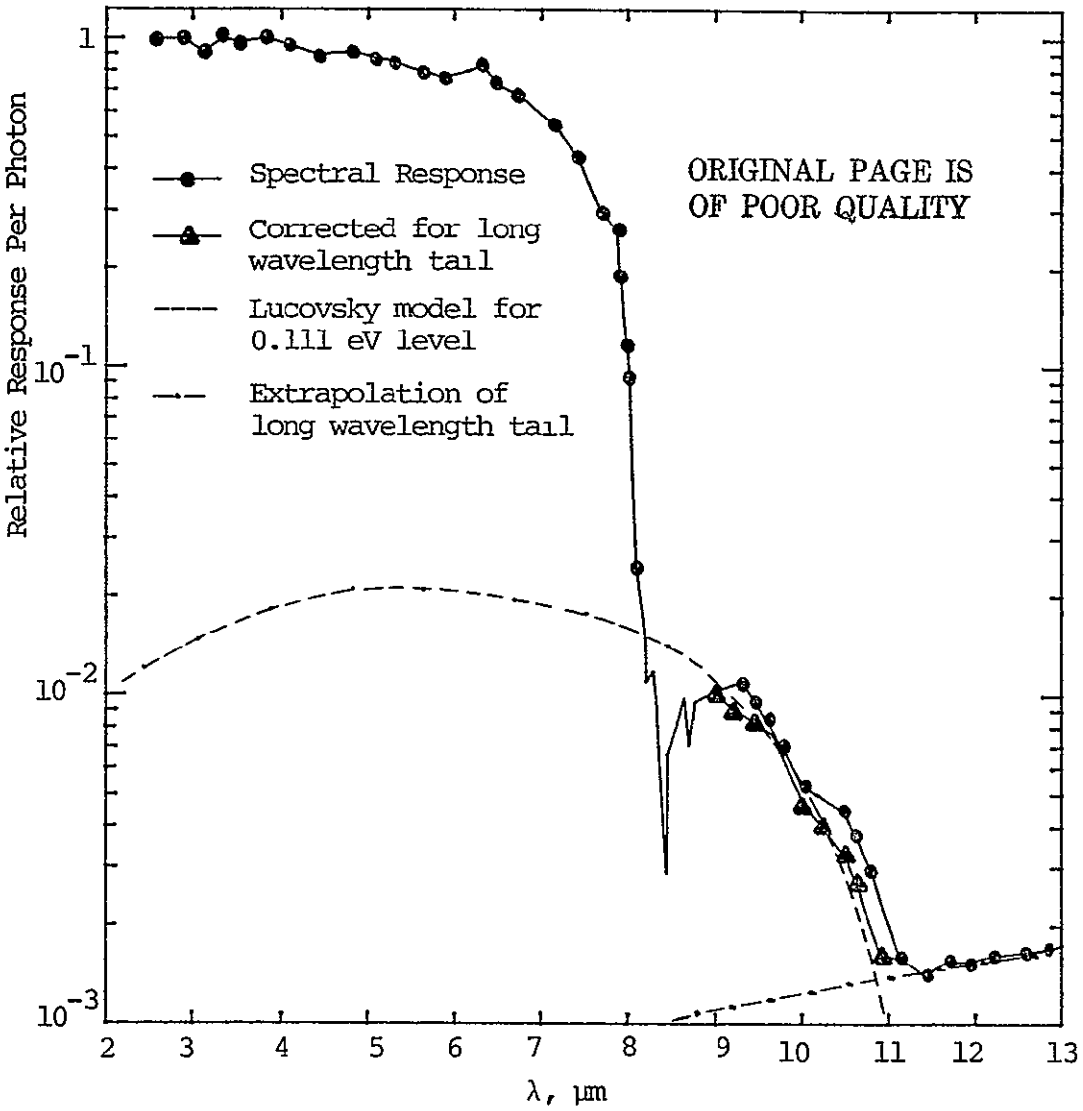


Figure 2.5 Photoconductive spectrum at 20K for sample of Si:In (FZ grown) in a 300K, 30° FOV background

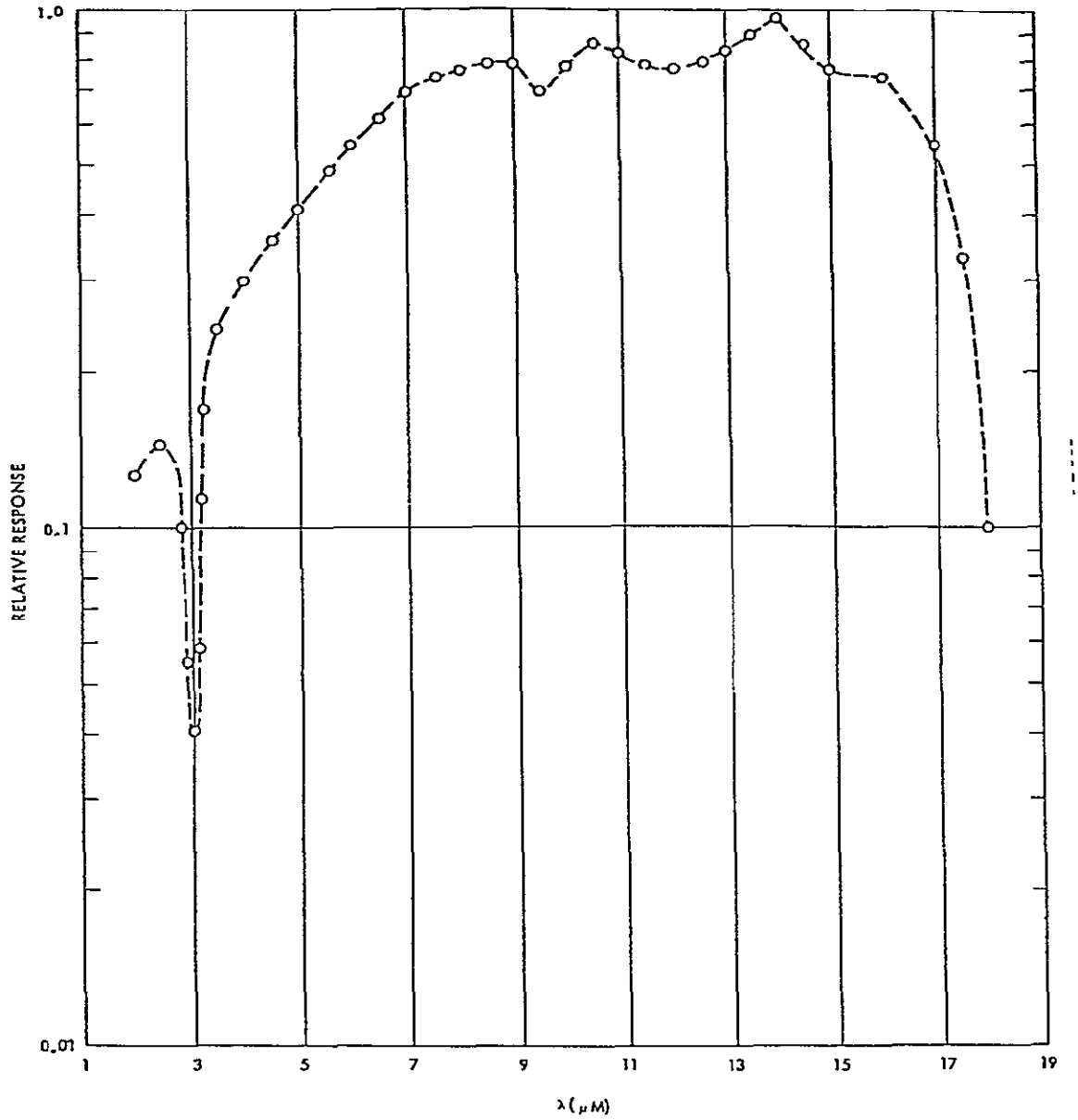


Figure 2.5 Si:Ga spectral response (2096-10/4 monolithic detectors)

where H = RMS irradiance

I_s = RMS signal current

A_d = detector active area.

At low frequencies, the responsivity of an extrinsic detector can be expressed as

$$R = \frac{q\eta\lambda}{hc} (N \sigma_o) G_o \ell = \frac{q\eta\lambda}{hc} G_o = .80\lambda\eta G_o \tag{2.5}$$

and

$$G_o = \frac{V\mu\tau}{\ell^2} = \frac{\tau}{\tau_R} \tag{2.6}$$

where ℓ = detector thickness

G_o = DC photoconductive gain

τ = majority carrier lifetime

τ_R = hole transit time

V = bias voltage

μ = majority carrier mobility.

Figure 2.7 shows the responsivity and noise of a Si:In detector as a function of temperature.[14] Note that the responsivity is a strong function of temperature with a peak value of 20 A/W at 60K. This rapid increase is due to a highly temperature dependent hole lifetime since η is independent of temperature and μ increases only slightly with temperature. More recent data has shown that the responsivity becomes less temperature dependent at higher bias.[15]

The responsivity of Si:Ga, on the other hand, as seen in Figure 2.8 is relatively constant in its operating temperature range. Figure 2.8 shows the responsivity versus temperature and background photon flux for three different concentrations of compensating phosphorous.[16] A strong bias voltage dependence

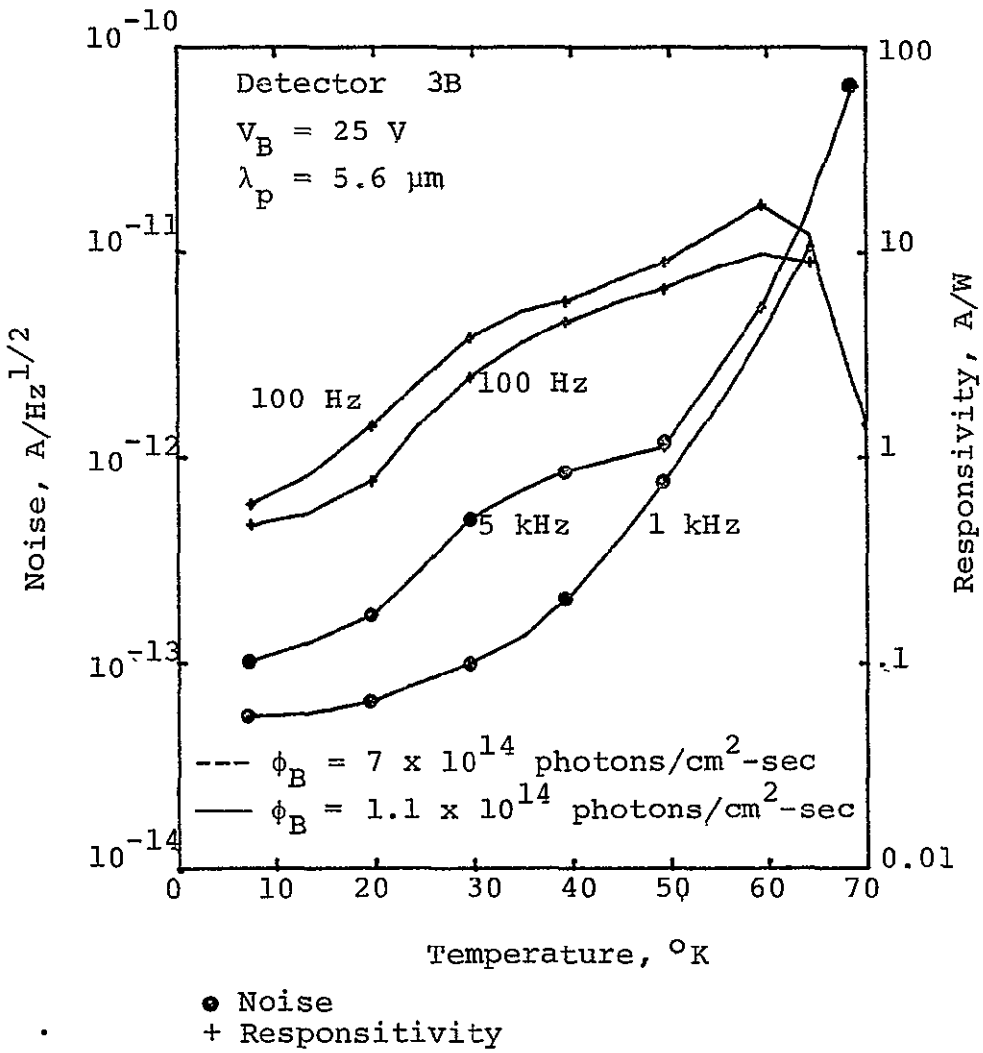


Figure 2.7 Responsivity and noise of Si:In detector as a function of temperature. Detector thickness - 0.04 in., N_{In} = 3.3 x 10^{17} cm^{-3} (g=4), $N_{"x"}$ = 1.6 x 10^{15} cm^{-3} and $N_{Donors} - N_B$ = 7.6 x 10^{13} cm^{-3}.

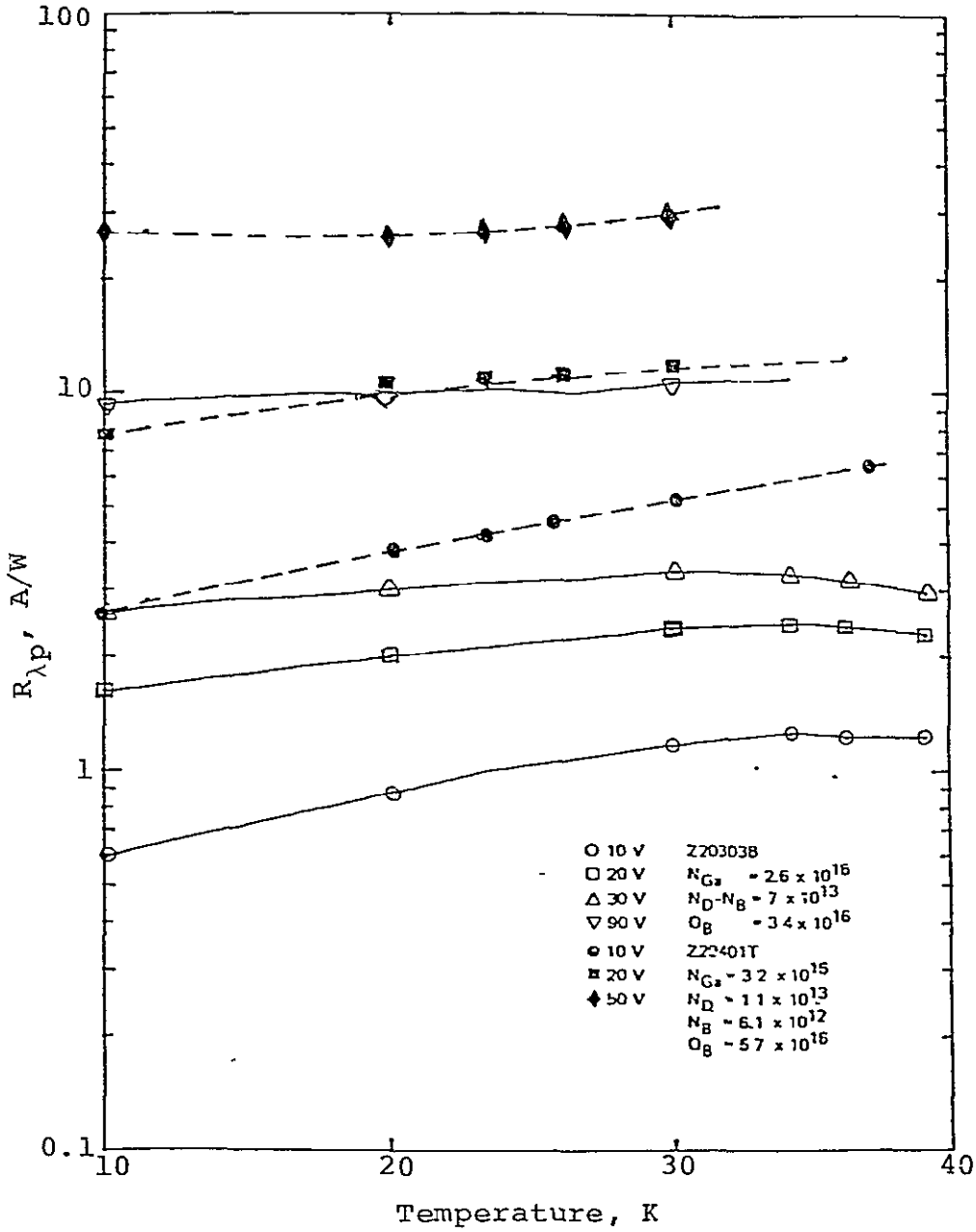


Figure 2.8 Responsivity versus temperature and bias for a SI:Gi detector

and a relatively weak temperature dependence can be seen.

The responsivity of a p type extrinsic detector material such as Si:In and Si:Ga is primarily limited by the residual boron which is present as an impurity in all silicon. Boron introduces shallow acceptor levels from which holes can be easily thermally excited. In order to inactivate the boron levels, it is necessary to compensate them with a n type impurity such as phosphorous or antimony. Compensation, however, negatively charges the boron atoms and some of the desired dopant atoms. These sites become centers for recombination and reduce the lifetime and responsivity. The lifetime for an extrinsic detector can be approximated by the expression,

$$\tau = (BN_p)^{-1} \tag{2.7}$$

where B = recombination coefficient, cm^3/sec

N_p = number of negatively ionized trapping centers per cm^{-3} ($\approx$ compensating phosphorous density)

Typical observed values of τ for Si:In and Si:Ga detectors range from 10 to 100 nanoseconds, corresponding to N_p values in the $5x10^{12}$ to 10^{14} range. Precise and repeatable compensation to the 10^{13} cm^{-3} or lower range for maximum responsivity has been difficult to achieve. Additionally, for the focal plane arrays, temperature variations in the crystal growth process and the high temperature processing utilized in chip fabrication is thought to induce spatial non-uniformities in the compensation. This appears to be the major source of the responsivity non-uniformity observed in focal plane arrays.

Precise compensation is also required to minimize the responsivity rolloff with frequency. The basic frequency response limitation associated with the detector responsivity results from the dielectric relaxation time and is given by,

$$\tau_\rho = \varepsilon_o \varepsilon \rho = \frac{\varepsilon_o \varepsilon d}{q \mu \eta \phi_B \tau} \tag{2.8}$$

where ε_o = dielectric constant of free space

ε = relative dielectric constant ($\approx$ 12 for silicon)

ρ = resistivity

τ = hole lifetime

d = detector length in the direction of the incident flux.

The corresponding frequency rolloff due to the dielectric relaxation is given by

$$F(w) = \frac{1}{\left[1 + (\tau_\rho \omega)^2\right]^{\frac{1}{2}}} \tag{2.9}$$

Figure 2.9[14] shows the responsivity rolloff due to dielectric relaxation for a Si:In discrete detector for a background ϕ_B of 1.1×10^{14} p/cm^{2}sec. Note that Figure 2.9 and Equation (2.8) suggests that discrete detector frequency response should be limited to less than 100 Hz at low backgrounds ($\phi_B < 10^{10}$ p/cm^{2}sec). This behavior may, however, be slightly altered at higher biases by the apparent decrease in detector time constants due to possible space charge injection effects.

2.4 DETECTIVITY AND NEP

The detectivity of a detector is given by

$$D^* = \frac{R A_d^{\frac{1}{2}}}{I_n} \tag{2.10}$$

where R is the responsivity, A_d is the detector area, and I_n is the total noise current (A/Hz$^{\frac{1}{2}}$). D* is the signal to noise ratio per unit radiant flux and is customarily expressed in unit of cm Hz$^{\frac{1}{2}}$/watt.

ORIGINAL PAGE IS
OF POOR QUALITY

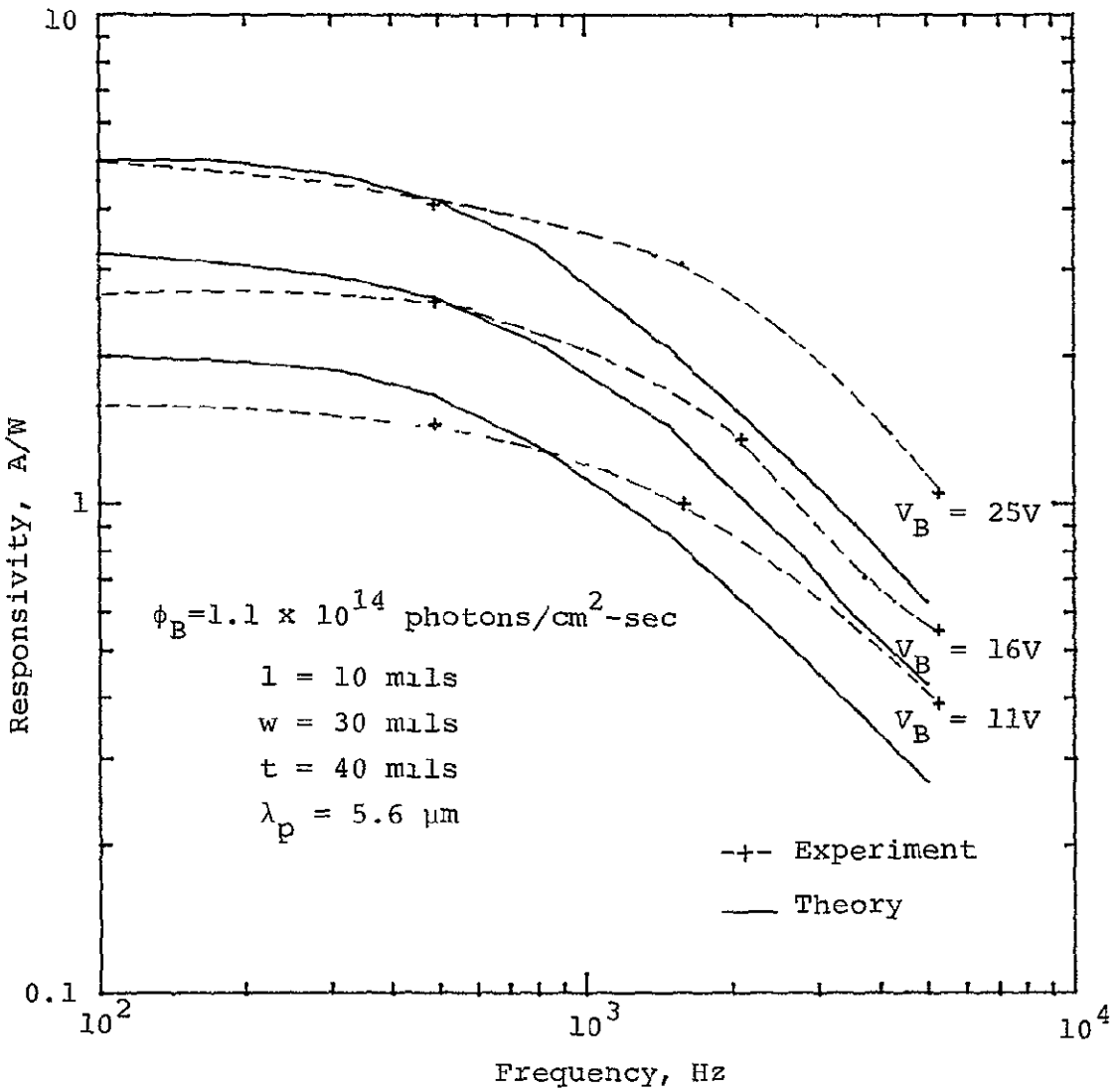


Figure 2.9 Responsivity as a function of frequency for a SI:In discrete detector

The noise equivalent power, NEP, is related to the D* by

$$NEP = \frac{A_d^{\frac{1}{2}}}{D^*} \tag{2.11}$$

The NEP is the radiant flux necessary to give an output equal to the detector noise and is given in units of $w/Hz^{\frac{1}{2}}$. Note that both D* and NEP are functions of wavelength since D* is defined in terms of signal to noise ratio per watt rather than per unit photon flux.

For extrinsic detectors, the dominant noise source is the generation-recombination noise current, which for low frequencies is given in terms of the carrier concentrations by

$$I_{gr} = 2Eq\mu(p\tau)^{\frac{1}{2}} \left(\frac{dw}{\ell}\right)^{\frac{1}{2}} \tag{2.12}$$

where $p = p_o + p_e$

p_o = concentration of thermally generated carriers
$= \phi_{th}\tau d$

p_e = concentration of background generated carriers
$= \eta\phi_B\tau/d$

E = applied field

d = detector thickness

w = detector width

ℓ = detector length

P_o, the concentration of thermally generated carriers is given by

$$p_o = \frac{[N_A - N_D]N_V}{gN_D} \; e^{-(\Delta E/kT)} \tag{2.13}$$

where N_A is the density of acceptors, N_D is the density of donors, g is the degeneracy of the level, and N_V is the effective density of states in the valence band (for a p type photoconductor) given by

$$N_V = 2\left(\frac{2\pi m_o kT}{h^2}\right)^{3/2}\left(\frac{m^*}{m_o}\right)^{3/2} = 4.8296\text{x}10^{15}\left(\frac{m^*}{m_o}\right)^{3/2} T^{3/2} \qquad (2.14)$$

where m^*/m_o is the effective mass ratio in the valence band. Equations (2.12) through (2.14) can be utilized to express the detectivity D* with its explicit temperature dependence as

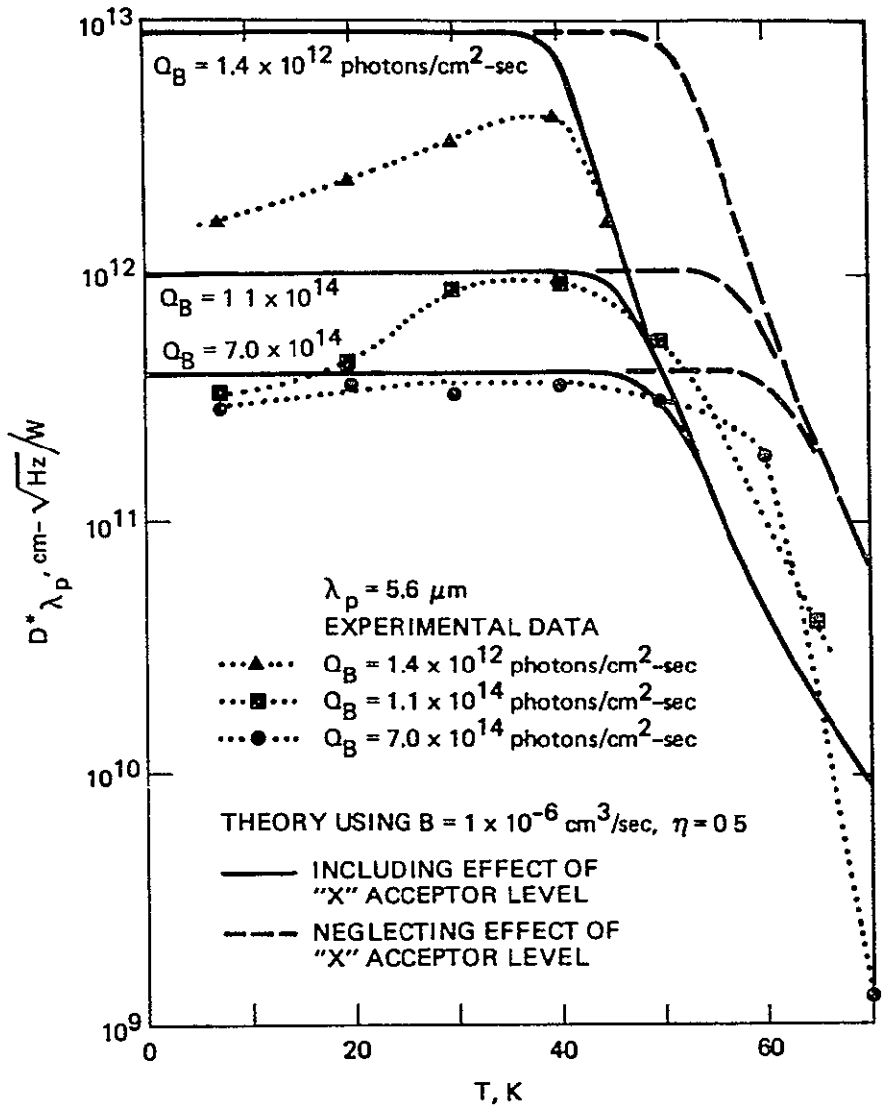
$$D^* = \frac{\eta\lambda}{2hc}\left[\eta\phi_B + \frac{2d\ [N_A - N_D]}{gN_D}\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} e^{-(\Delta E/kT)}\right]^{-\frac{1}{2}} \qquad (2.15)$$

At temperatures or backgrounds where $\phi_B >> \phi_{th}$ Equation (15) reduces to the familiar background limited D*,

$$D^* = \frac{\lambda}{2hc}\left(\frac{\eta}{Q_B}\right)^{\frac{1}{2}} \qquad (2.16)$$

Typical data for Si:In detectors as a function of temperature are shown in Figure 2.10.[14] Theoretical D* curves are also plotted. Figure 2.10 shows that the D* rolloff occurs at a lower temperature than one anticipates on the basis of the In level alone. This has been attributed to the presence of the additional acceptor level at .111 eV observed in the spectral response measurements. Free carrier concentrations determined by Hall measurements have confirmed the existence of this "X" level in Si:In crystals and suggest that its concentration is correlated with the In concentration.[11] Recent improvement in the growth techniques of Si:In crystals, however, have reduced the "X" level concentration to the point where performance dominated by the In ionization energy have been achieved.

Figure 2.11 shows the D* as a function of temperature for Si:Ga detectors for three different phosphorous compensating densities and at three background levels.[6]



ORIGINAL PAGE IS
OF POOR QUALITY

Figure 2.10 Detectivity of Si:In as a function of temperature. Detector thickness = 0.04 in., $N_{In} = 3.3 \times 10^{17}$ cm^{-3} (g = 4), $N_{"x"} = 1.6 \times 10^{15}$ and $N_{Donors} = N_B = 7.6 \times 10^{13}$ cm^{-3}.

ORIGINAL PAGE IS
OF POOR QUALITY

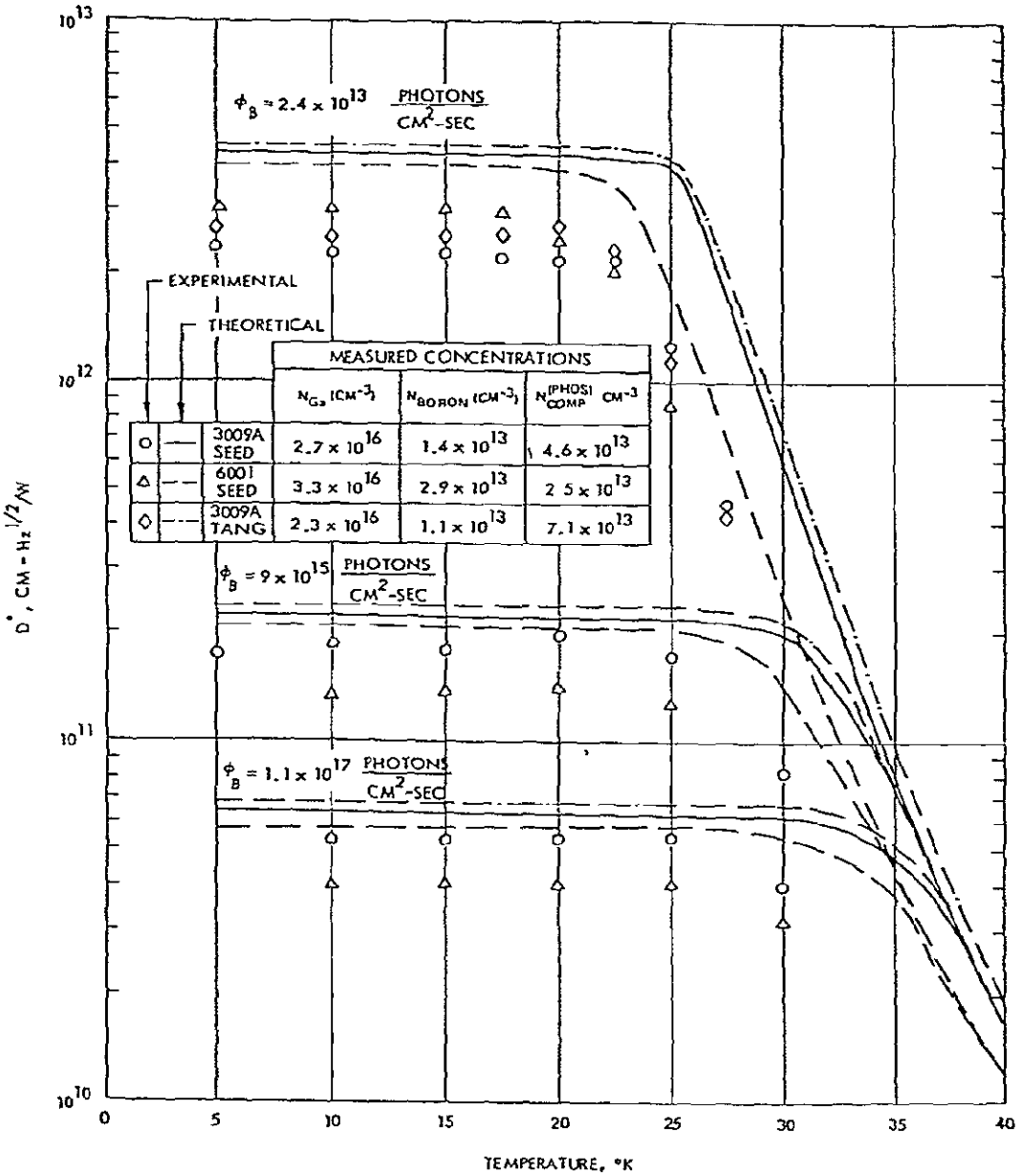


Figure 2.11 Si:Ga D* as a function of temperature for various background photon flux densities

2.5 Si:X CHIP DESIGN AND OPERATION

The design and layout of Si:X chips are very similar to the interline transfer visible CCD imagers with a set of parallel inputs along the channel and a serial output multiplexer. The design and configuration of the 2 x 32 array circuit of the 2096 chip is shown in Figure 2.12. Also shown is a cross section of the unit cell. Each unit cell contains an input circuit, storage gate, bucket overload protection circuit, transfer gate and four bits (analog) of CCD readout. Four bits of CCD register are utilized in each unit cell to minimize the gate length in the direction of charge flow for high transfer efficiency. Signal charge is loaded into alternate bits to provide isolation between signal charges to minimize electrical crosstalk. Both rows of 32 detectors are read out by conventional on-chip resettable floating diffusion MOS amplifiers.

The CCD register, which provides the charge storage, overload protection, and charge transfer, is fabricated in the lightly doped epitaxial layer. Detector bias is applied between the common p+ contact and a direct or indirect contact on the epi side. The detector contact area and the field lines delineate the active detector volume. The optical input can be introduced through the CCD structure side (front illumination) or from the substrate (back illumination). Because of the low absorptance of extrinsic substrates and the bias field delineation of the detector volume, both modes yield comparable responsivities.

Another chip design involving less complex unit cell architecture is shown in Figure 2.13. Simpler design features and an operational implementation of isolation between cells permit a smaller unit cell and potentials for high yield and producibility for this chip. A novel injection mode minimizes the input time constant at low backgrounds. Si:In and Si:Ga chips incorporating these design features are currently under development.

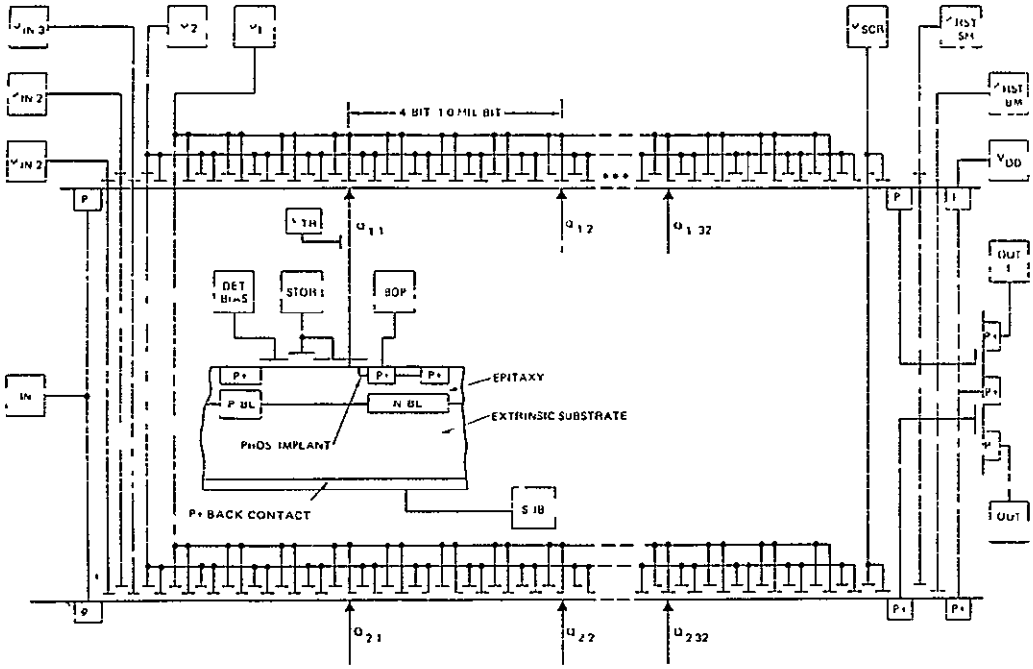


Figure 2.12 Circuit diagram of the 2x32 2096 array

ORIGINAL PAGE IS
OF POOR QUALITY

ORIGINAL PAGE IS
OF POOR QUALITY

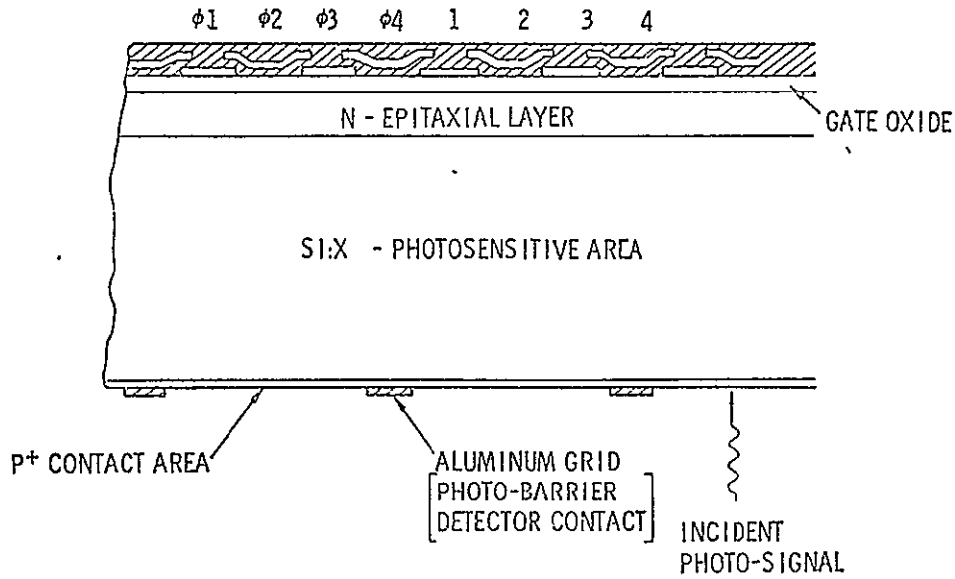


Figure 2.13 Si:X chip cross-section

2.6 Si:X CHIP PERFORMANCE

The performance characteristics of a Si:X chip are determined by the CCD register and the associated input circuits in the epitaxial layer and the detector properties of the substrate. Performance characteristics determined by the CCD register, such as charge storage capacity, signal linearity, electrical cross-talk, charge transfer efficiency and noise are similar to visible CCD imagers since the fabrication and design of Si:X chip is based upon the same CCD technology.

Charge Storage Capacity and Dynamic Range

The dynamic range is the ratio of the CCD charge storage capacity and the CCD noise level. The maximum charge which can be stored is given by

$$n_{max} = \frac{n_c C_{ox} A \Delta V_g}{q} \tag{2.17}$$

where
- n_c = number of gates used for storage (1)
- A_g = gate area (1.5 mil^2)
- C_{ox} = oxide capacitance ($2x10^{-8} F/cm^2$)
- ΔV_g = storage gate voltage (5 V)
- q = Electronic charge.

Using the numbers listed in the parentheses, $N_{max} = 9x10^6$ electrons. For a noise level of 1000 electrons, the dynamic range is $9x10^3$. The dynamic range can be increased over this value by using more than one gate for signal storage in the unit cell.

Maximum Integration Time

For astronomical applications, long integration times are desirable for maximum detectivity. The maximum integration time is limited by the charge storage capacity of the storage gate and the thermally and background generated charge carriers. The maximum integration time can be approximated by

$$T_{max} = \frac{\alpha C_{ox} \Delta V_g}{q\ (J_B + J_T)} \qquad (2.18)$$

where J_B = background generated charge flux (carriers/cm^{2}sec)
J_T = thermally generated charge flux (carriers/cm^{2}sec)
α = fraction of the unit cell used for charge storage ($\approx$ 10%)

Using J_T derived from dark Hall measurements of the carrier concentration versus temperature, Equation 2.18 predicts large T_{max} for low backgrounds. For example, for T = 20K and J_B = 10^5 carriers/cm^{2}sec, T_{max} is about 625 seconds. Current Si:In chips, however, exhibit charging times which are about an order of magnitude lower, due to extraneous currents in the Si:In chip structure that are not suppressed by cooling. Process improvements and improvements in the quality of the extrinsic substrate are expected to substantially reduce these sources.

Linearity

The linearity of response to an increasing optical input has been tested on the CCD 2096. The input signal to the CCD was varied by changing the integration time. The response for the CCD 2096 remained linear as the signal was increased from 1 percent of bucket capacity to about 60 percent of bucket capacity. Above 60 percent of bucket capacity, the signal response became non-linear due to the onset of saturation. Linearity over similar ranges have been verified for other similar chips. Although difficult to verify except under narrow bandwidth conditions, linearity can be expected to be maintained below 1 percent down to the CCD noise level.

Crosstalk

Crosstalk between elements can arise from two sources in an extrinsic MFPA. The first source is the optical crosstalk

due to the geometry of the chip. Optical crosstalk was originally considered to be a significant drawback of the extrinsic approach due to the low absorption cross section and thick subsbtates. However, the incoming optical cone coverage in the silicon substrate because of the large change in the refractive index. Additionally, it was found that detector bias effects play an important role in the delineation of the collection area, independent of the unit cell size. Both factors minimize the optical crosstalk. The second source of crosstalk is electrical and is due to charge spillover resulting from charge transfer inefficiency. A typical measured charge transfer efficiency for the Si:X chip is .99975. The corresponding electrical crosstalk is about 0.2 percent which for all practical purposes is negligible.

Spot scan measurements at various detector locations have been conducted on the CCD 2096 and other chips. These measurements have shown that the optical crosstalk can be kept to less than 10 percent at typical f/numbers of f/3 and greater. The spot scan measurements also indicate that independent of the size and specific geometry of the detector contact, an effective detector area that is about 80 percent of the detector element area can be achieved.

D* and NEP

The D* and NEP of Si:X chip are limited by the noise characteristics of the CCD readout multiplexer. The noise in CCD has been modeled quite extensively.[17,18] Based upon these models, basic performance equation for Si:X chips can be derived. Table II lists the basic equations for D* and NEP and noise sources as derived from such a model.[19]

The noise sources listed in Table II basically fall into three categories: 1) detector shot noise associated with the

background; 2) channel noise associated with the input MOS channel; and 3) CCD readout noise. Note that the photon and channel noise are sample time (integration time) dependent, whereas the CCD noise sources are independent of sample time.

At low sampling rates, the noise spectral density shapes are not important because CCD noise is folded back into the detector bandwidth (noise aliasing) by the CCD readout process. For this reason, at frequencies above the 1/f corner frequency, the noise spectral density can be assumed to be flat and the NEP can be calculated by summing the noise variances.

Detailed test data on Si:In chips have shown that the dominant noise source for backgrounds less than 10^{12}/mcm^{2}sec is the fast interface state (FIS) noise. FIS noise arises from the fluctuations associated with the filling and emptying of the interface states N_{ss} as the signal charge is transferred along a CCD register. N_{ss} is the number of interface states per unit area per unit of energy in the bandgap and considered constant across the gap. Typical FIS noise values for current Si:In chips are in the 800 to 2000 noise carriers (RMS) range implying N_{ss} values of about 10^{11} states/cm^2-eV. This N_{ss} value is an order of magnitude higher than for comparable surface channel CCD devices on bulk substrates. MOS/CCD process refinements are being made currently to reduce the N_{ss} for Si:X chips.

The NEP given in Table II can be expressed in the more curtomary units of W/Hz$^{1/2}$ as

$$\mathrm{NEP}\left(\frac{W}{Hz^{\frac{1}{2}}}\right) = \frac{hc}{\lambda \eta G T_s}\left(\frac{\mathrm{Var}N_T}{\Delta f}\right)^{\frac{1}{2}} \tag{2.19}$$

TABLE II. Si:X Chip Noise Variance and Performance Equations and Symbols Listing

Photon Noise

$$\mathrm{Var}\ N_p = 2\eta Q_B A_d G^2 \left(\frac{g_m R_d}{1 + g_m R_d}\right)^2 T_s \left\{1 - \frac{\tau}{T_s}\left[1 - \exp(-T_s/\tau)\right]\right\}$$

Channel Noise

$$\mathrm{Var}\ N_{ch} = \frac{1}{(1 + g_m R_d)^2} \frac{4kTg_m}{3e^2} T_s \left\{1 - \frac{\tau}{T_s}\left[1 - \exp(-T_s/\tau)\right]\right\}$$

$$+ \frac{4kTg_m}{3e^2} \tau \left[1 - \exp(-T_s/\tau)\right]$$

Fat Zero Noise

$$\mathrm{Var}\ N_{FZ} = \frac{2kTC_{in}}{3e^2}$$

Fast Interface State Noise

$$\mathrm{Var}\ N_{FIS} = 69 \frac{kT}{e} A_{CCD} N_{SS}$$

Reset Noise

$$\mathrm{Var}\ N_{RST} = \frac{2kTC_{out}}{3e^2}$$

Output Device Noise

$$\mathrm{Var}\ N_{out} = \left(\frac{V_1 C_{out}}{e}\right)^2 \ln\left(\frac{1}{f_c}\right)$$

Input Transconductance (weak inversion)

$$g_m = \frac{\eta A_d Q_B G e^2}{2kT}$$

Input Time Constant

$$\tau = C_d/g_m$$

Noise Equivalent Power

$$\mathrm{NEP} = (\mathrm{Var}\ N_{TOT})^{1/2} \frac{hc}{G\eta\lambda T_s}$$

Detectivity

$$D' = \frac{(A_d/2T_s)^{1/2}}{\mathrm{NEP}} \mathrm{sinc}\ (\pi f T_s) \left[\frac{1}{1 + (2\pi f\tau)^2}\right]^{1/2}$$

Symbol	Parameter
$\mathrm{Var}\ N_p$	Photon Noise Variance
$\mathrm{Var}\ N_{ch}$	Channel Noise Variance
$\mathrm{Var}\ N_{FZ}$	Fat Zero Noise Variance
$\mathrm{Var}\ N_{FIS}$	Fast Interface State Noise Variance
$\mathrm{Var}\ N_{RST}$	Reset Noise Variance
$\mathrm{Var}\ N_{out}$	Output Noise Variance
$\mathrm{Var}\ N_{tot}$	Total Noise Variance
g_m	Input Circuit Transconductance
τ	Input Circuit Time Constant
η	Quantum Efficiency
A_d	Detector Area
A_{CCD}	Area of CCD Register
R_d	Detector Resistance
T_s	Sample Time of Detector
T_c	Clock Period
T	Temperature
G	Photoconductive Gain
N_{SS}	Surface State Density
C_{in}	Capacitance of Input Device
C_{out}	Capacitance of Output Device
C_d	Detector Capacitance
λ	Wavelength
V_1	Noise at 1 Hz (output device 1/f)
Q_B	Background Photon flux at MFPA
i_p	Photon Current
N_{max}	Maximum Number of Transfers in MFPA
k	Boltzman Constant
e	Electronic Charge

ORIGINAL PAGE IS OF POOR QUALITY

which for $\Delta f = 1/2T_s$ becomes

$$NEP\left(\frac{W}{Hz^{\frac{1}{2}}}\right) = \frac{hc}{\lambda\eta G}\left(\frac{2VarN_T}{T_s}\right)^{\frac{1}{2}} \tag{2.20}$$

At high backgrounds or where high photoconductive gains are obtained, the shot noise of the background will dominate over the fixed CCD noise and the Si:X chip performance will be BLIP limited. Under these conditions D* is independent of the integration time since Var N_T will be directly proportional to T_s and the explicit T_s dependence will cancel out. On the other hand, at low backgrounds Var N_T will be constant (FIS noise limited) and the NEP and D* will be inversely and directly proportional to $T_s^{1/2}$, respectively. Figure 2.14 shows the NEP limits as a function of T_s at low backgrounds. A gain, G, of unity was assumed. Responsivity data on Si:In and Si:Ga discrete detectors show that gains in excess of 10 can be obtained.[15,16] Gains greater than unity, however, are difficult to realize in Si:X chips due to operating bias limitations.

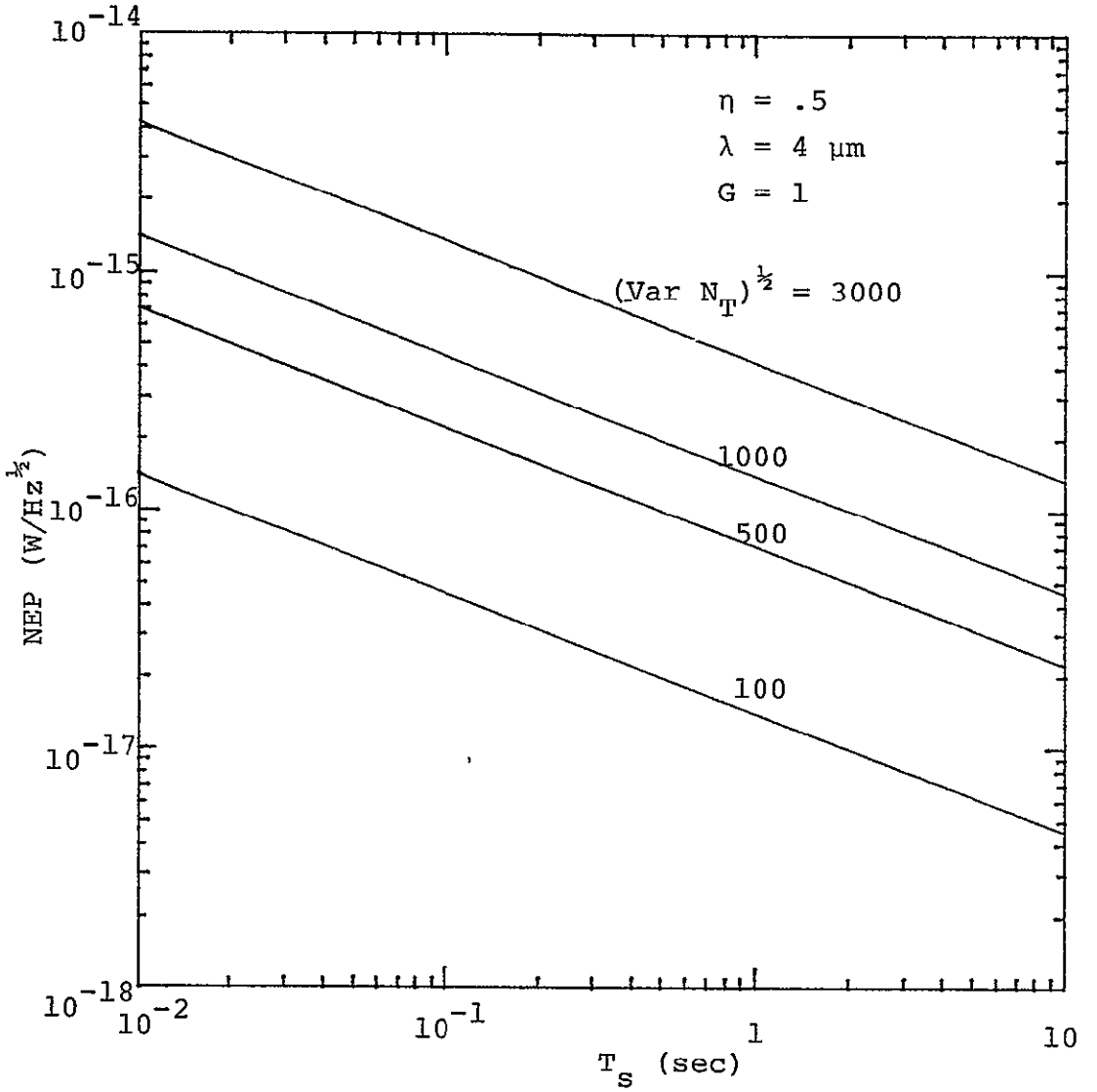


Figure 2.14 NEP Versus Integration Time for a Si:X Chip

III. MONOLITHIC INTRINSIC FOCAL PLANE ARRAYS

Since the development of high performance silicon CCD and CID imagers, a number of approaches have been investigated to fabricate high density monolithic arrays in materials other than intrinsic or extrinsic silicon. One such approach is to fabricate CCD or CID structures on a narrow bandgap semiconductor to extend the spectral response into the infrared region.

A monolithic intrinsic infrared focal plane array fabricated in the appropriate narrow-band semiconductor represents in many ways the ultimate solution for realizing an infrared focal plane array. The absorption coefficient of an intrinsic narrow-band semiconductor is high. Therefore, high quantum efficiency can be realized in thin detector layers. The high absorption coefficient minimizes crosstalk effects. The higher permissable operating temperatures of an intrinsic material can also be a significant advantage in many space applications where cooling to low temperatures may be impractical.

A number of narrow bandgap semiconductor materials have been investigated for CCD array feasibility.[20,21] The lack of a mature MIS (metal insulator semiconductor) technology, similar to that which exists for silicon, and the low minority carrier lifetimes and breakdown voltages compared to silicon, however, have limited the choice for development to only a few promising candidates, namely, InSb and some of the III-V and II-VI tenary alloy systems.

During the past several years, significant progress has been made on InSb MIS technology. Both CCD[22] and CID[23] operation have been demonstrated at 77K. Significant progress has also been made in the MIS technology of the III-V tenary alloy system.[24] Additionally, monolithic (Hg,Cd)Te CCD arrays are being

developed under the tri-service MIDAS program. CCD operation in (Hg,Cd)Te was recently demonstrated for the first time. A charge transfer efficiency of 0.999 was measured for a 16 bit CCD register.

Another approach currently under development is based upon epitaxially grown layers of III-V ternary alloys in a multilayer structure in which detection and CCD readout occur in separate layers. The technology required to fabricate such structures is being developed under the DARPA HALO Program.

3.1 InSb CCD

The development of InSb CCDs has proceeded for a number of years under NASA sponsorship.[25] Under this effort, a number of InSb test chips were designed, fabricated, and evaluated. Significant progress was made both in performance and device processing parameters for an InSb CCD. Progress on this effort led to the design of a 9-bit CCD mask set (8580) complete with other test structures for process control. The important milestone of charge transfer with proper time delay was achieved. A charge transfer efficiency (CTE) of 0.90, which was low due to the long gate lengths of the 8580 design, was measured.

A new mask set, the 8582 was designed. This design incorporated a 2-bit structure and a 9-bit CCD imager with gate lengths of 25 μm (1 mil), reduced from the 50 μm (2 mil) value of the 8580 test chip. The 2-bit structure was successfully operated and an improved CTE value of 0.97 was demonstrated. Design flaws in the 8580 mask set and metal clock lines step coverage problems precluded a similar demonstration of the 9-bit coverage.

Experience gained with the 8582 identified a number of design and processing problems limiting device yields and led to the design of a completely new design, the 8585. Fabrication of the 8585 is based upon a total etch technology, which potentially

should overcome the problems of the 8582 design. This new chip is currently under NASA sponsored development and incorporates 1) a 20-element linear imager with 12.5 μm gate lengths; 2) a 4-bit element 4-phase TDI array and a 4-element 2-phase linear imager with 12.5 μm gate lengths; 3) a 2-element 4-phase linear imager with 10 μm gate lengths; 4) a monolithic gated charge integrator circuit for on-chip signal processing; and 5) an assortment of test devices.

The 20-element linear image is shown in Figure 3.1. Figure 3.2 shows schematically the design of this 20-element imager. The 20 detectors are MIS capacitors with thin ($\approx$ 0.0075 μm) titanium serving as the transparent metal gates. The imager is a 4-phase surface channel overlapping gate design with 12.5 μm gates. A "fill and spill" input circuit consisting of: 1) input (ID) diode, 2) signal (B) gate, 3) surface control (SC) gate, and 4) a storage gate, which is also the first phase-2 well, is incorporated into this design. This input structure allows the introduction of a low noise "fat zero" bias charge for efficient charge transfer.

A number of 8585 chips have been fabricated and evaluated. A CTE of 0.995 was measured for the 2-element test device. The 20-element linear imager was also operated and is currently in evaluation.

Significant improvements have been made in the MIS properties and the process technology necessary for InSb CCDs. Planar p-n diodes have recently been fabricated on InSb using ion-implantation of beryllium ions. The requisite gate insulator technology has also shown rapid improvement with insulators possessing flat-band voltages of approximately -0.5 volt (n-type InSb substrates), interface state densities of $2 \times 10^{11}/cm^2$-eV at mid-gap, and negligible hysteresis. Progress has also been made toward developing a fully planar channel stop structure. The approach chosen for development utilizes ion-implantation to form a heavily doped n^+ layer overlying the n-type InSb substrate.

ORIGINAL PAGE IS
OF POOR QUALITY

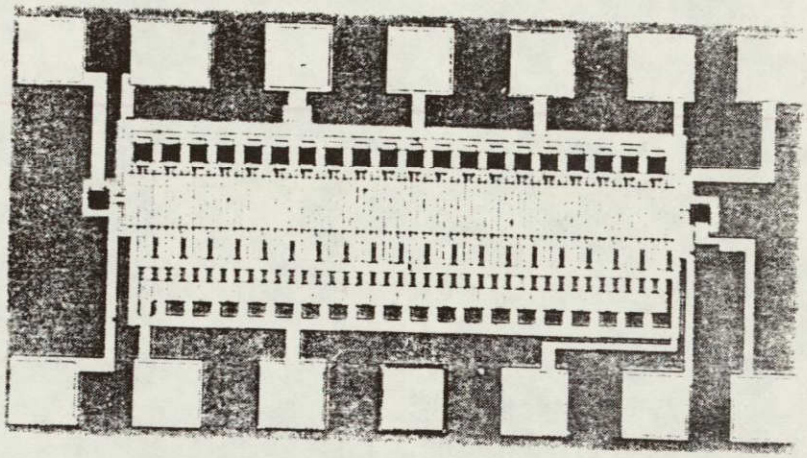


Figure 3.1 Photomicrograph of 20-element InSb CCD

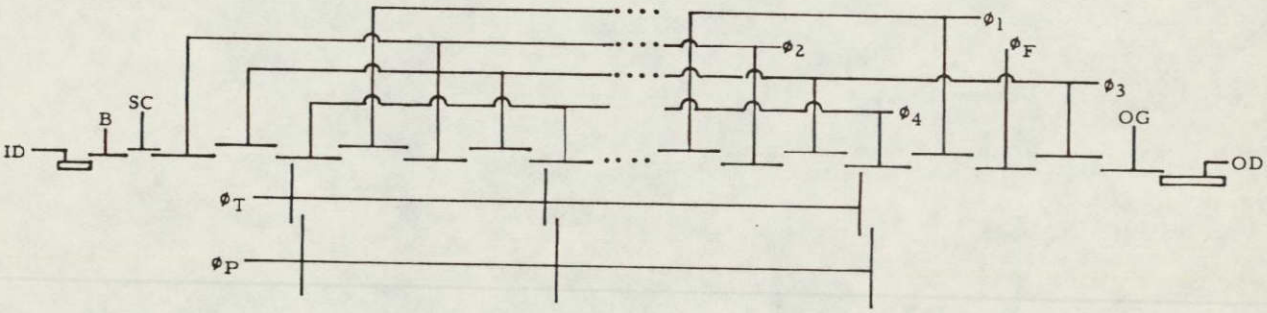


Figure 3.2 Schematic Diagram of 4ϕ Overlapping Gate 20-Element Imager: 8585 Design

$$J_G = qn_i \left(\frac{n_i L_p}{N_D \tau_p} + \frac{W_d}{2\tau_d} + \frac{S}{2} \right) \tag{3.2}$$

where the first term is the dark current due to minority carriers generated in the neutral bulk which diffuse to the depletion region, the second due to carriers generated in the depletion region of width W_d, and the third due to generation at the surface with surface recombination velocity S. n_i is the intrinsic carrier concentration, N_D is the impurity concentration, $L_p = (D\tau p)^{1/2} = (\mu\tau pkT/q)^{1/2}$ is the diffusion length and τ_p the minority carrier lifetime.

Representative values for state of the art InSb CCDs at 77 are[22]

$N_D = 10^{15}/cm^2$
$n_i = 2.7x10^9/cm^3$
$\tau_p = .1\ \mu sec$
$\mu_p = 9x10^3\ cm^2/Vsec$
$L_p = 25\ \mu m$
$C_s = 1.5\ pF/cm^2$
$C_o = 3x10^{-8} F/cm^2$
$\Delta\phi_s = 2.5$ volts.

Using these values, the estimated dark current components at 77K are:

J_G (bulk diffusion)	$0.02\ nA/cm^2$
J_G (g-r current from depletion region)	$300\ nA/cm^2$
J_G (surface)	$(0.2)S\ nA/cm^2$

Assuming "low S" surfaces, it can be seen that the dominant source of dark current will be the bulk generation from the depletion region. Note that the dark current for InSb at 77K is large in comparison to silicon devices even at room temperature where dark

currents in the 5-10 nA/cm^2 range are typical. This is due to the longer lifetimes in silicon (≈100 μsec) and the substantially higher intrinsic carrier concentrations at a given temperature for low bandgap materials such as InSb.

From Equation (3.1) and the estimated dark currents, the expected bulk-limited storage time is on the order of .25 sec. Experimentally, InSb MIS storage times up to .5 seconds have been measured at 77K. C-T measurements by Kim[23] have also shown that the storage time is of the order of .3 sec at 77K for InSb MIS capacitors.

The measured dark currents and storage times for InSb at 77K are not favorable for low background astronomical applications where long integration times are desirable for maximum detectivity. In order to increase the storage time capability, it will be necessary to operate InSb at temperatures substantially lower than 77K to reduce the dark current.

The temperature dependence of the dark current will be dominated by the temperature dependence of n_i and is given by the expression,

$$J_G = \alpha T^{3/2} e^{-(E_g/2kT)} \tag{3.3}$$

where E_g is the energy gap. The $T^{3/2}$ reflects the density of states effect and the activation energy is $E_g/2$ since the states that contribute to thermal generation are near mid bandgap. A normalized plot of this equation is given in Figure 3.3. A reduction of about $2x10^4$ is predicted between 77K and 50K. Dark current reductions of this magnitude, however, may not be achievable in actual InSb CCDs since substrate leakage and other fixed leakage currents may dominate the thermal generation at low temperatures.

The spectral response of InSb MIS detectors and CID arrays

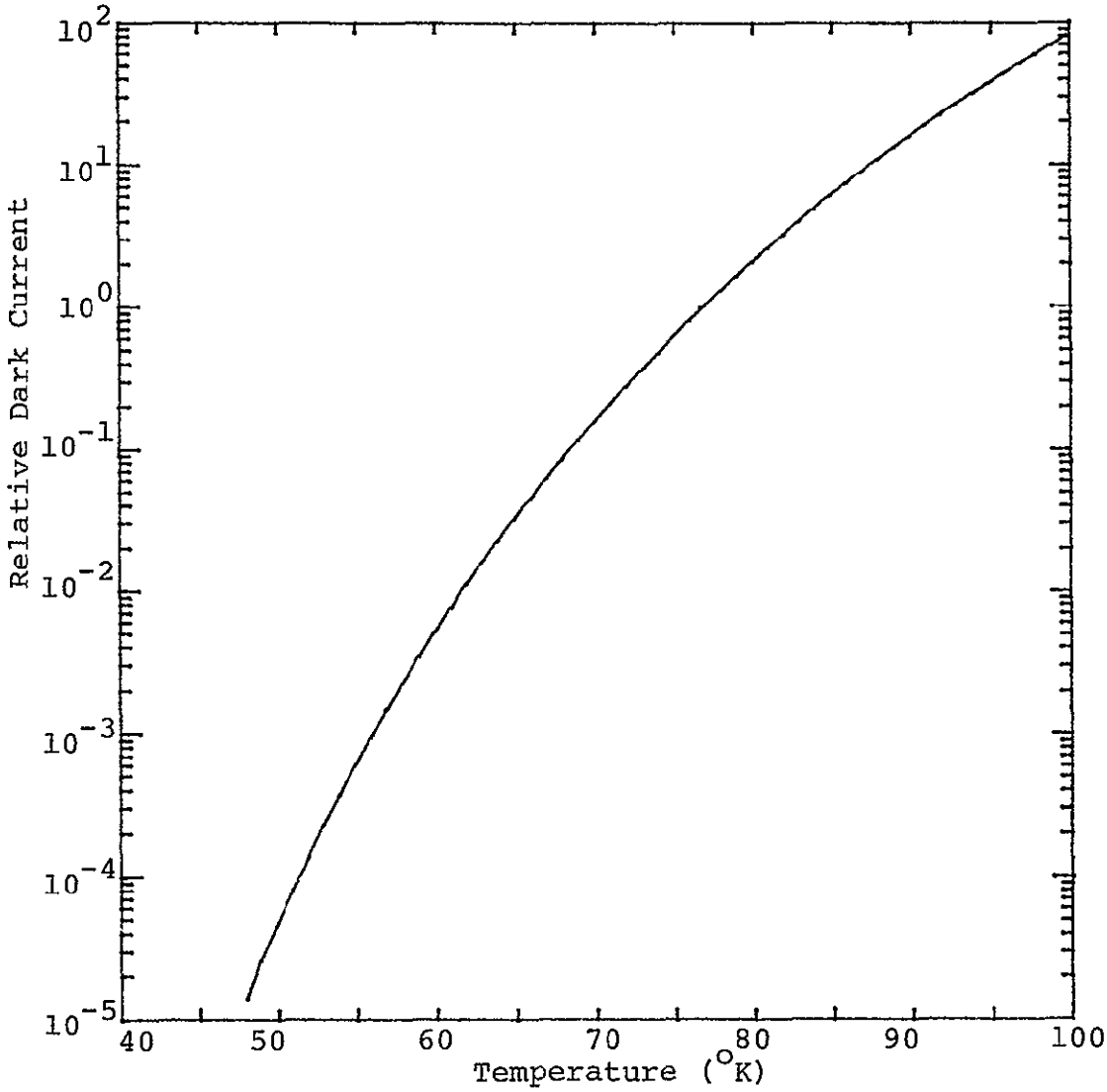


Figure 3.3 Theoretical Reduction of Dark Current with Temperature for InSb (E_g = 0.225 eV)

ORIGINAL PAGE IS
OF POOR QUALITY

have been measured and have been found to show a spectral response identical to that of a photovoltaic InSb discrete detector. The spectral response of an InSb CCD should also be similar with the characteristic bandgap defined cutoff of about 5.4 μm.

D*, NEP and other CCD performance data do not as yet exist due to the developmental nature of the existing devices. At low backgrounds ($\leq 10^{10}$ p/cm^{2}sec) and low temperatures, D* can be expected to be limited by the CCD noise. CCD noise of existing InSb arrays is dominated by the fast interface state noise because of the high interface state densities. As the processing technology matures, the interface state densities can be expected to improve to the point where the CCD noise characteristics can be expected to be similar to a silicon surface channel CCD with a comparable number of elements.

3.3 MULTILAYER MONOLITHIC INTRINSIC ARRAYS

Another fully monolithic approach which is currently under development is the representative monolithic intrinsic structure shown schematically in Figure 3.4. The structure is fabricated utilizing the liquid-phase-epitaxy method similar to that developed for high performance backside illuminated photodiodes in $InAs_{1-x}Sb_x$.[26,27] The basic structure consists of a number of $InAs_{1-x}Sb_x$ epitaxial layers of different composition and thicknesses grown successively on a transparent substrate. The detector layer is selectively doped to form a p-n junction contact or alternatively, interlayer contacts are made to delineate the individual photodiodes and interconnects to the CCD register. A separate CCD layer is epitaxially grown on top of the detector layer to form the composite structure. Buffer layers are compositionally step graded between the substrate and detector layers to relieve the lattice strain caused by lattice mismatch.

This approach has several attractive features. Since the detector layer is back illuminated and not obscured by the CCD structure, detector fill factors approaching unity can be obtained.

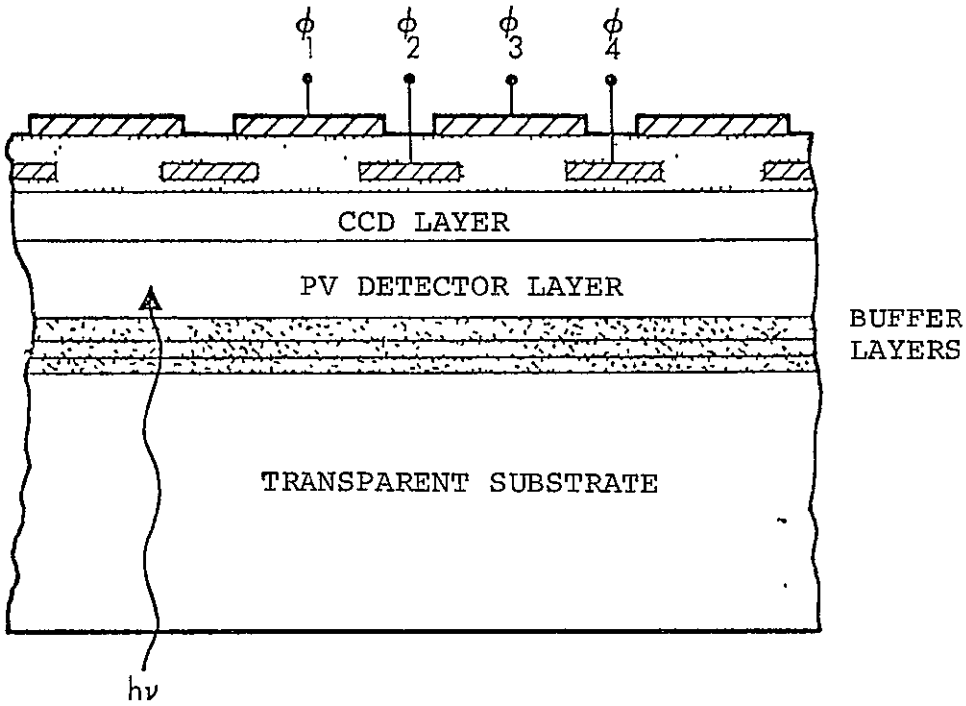


Figure 3.4 Multilayer Monolithic Intrinsic Structure

ORIGINAL PAGE IS OF POOR QUALITY

The spectral response of the detector layer is tunable since the bandgap of the $InAs_{1-x}Sb_x$ ternary alloy system is a function of the alloy composition. The long wavelength response of $InAs_{1-x}Sb_x$ has been tuned compositionally from 3.1 μm ($x \approx 0.0$) to 7.0 μm ($x \approx 0.4$) and is potentially capable of operation out to 9.0 μm ($x \approx 0.6$) at 77K.

Another attractive feature is the separation of the detector and CCD readout function into two distant layers. The CCD can be fabricated in a wider bandgap alloy material such as GaInSb. A storage time of about 6 seconds at 77K has been observed for p-$Ga_{.85}In_{.15}Sb$ MIS devices,[24] making it an attractive material for the CCD layer.

While this approach offers many attractive features, it is the least developed of the focal plane approaches. Formidable materials technology problems must be overcome to make this a viable approach. The DARPA sponsored HALO monolithic intrinsic detector array program has directly addressed these problems and is developing the base technology necessary to establish device viability.

A liquid phase epitaxy growth process which yields alloy layers possessing the morphology, donor levels, and dislocation density necessary for multilayer lattice matched structures has been demonstrated for structures similar to that shown in Figure 3.4. An extensive effort is in progress to improve basic MIS properties of the CCD layer. Significant MIS milestones which have been achieved are: 1) the development of a SiO_2 gate oxide growth technique which yields exceptionally low fast interface state densities, 2) successful growth of liquid phase epitaxy InSb layers with MIS properties superior to existing bulk InSb, and 3) a successful demonstration of CCD operation in GaInSb.

Several ion implantation approaches to form efficient detector contacts and planar diodes required in the CCD input/output circuits have been developed. The ion implantation diodes were found

to have leakage currents sufficiently low to meet the device requirements and were found to be superior to the planar diffused diodes.

While many components of the base technology have been established, considerable development will be required before the viability of this approach can be established. This approach certainly has long term potential since the limitations at this time appear more technological than fundamental. A key milestone for this technology will be the fabrication and demonstration of the first test array.

IV. CHARGE INJECTION DEVICE (CID)

The charge injection principle is an alternate approach to solid state imaging which has received considerable development attention in the past few years. Charge injection devices (CIDs) are self-scanned focal plane arrays that employ surface charge transfer between two closely spaced MOS capacitors per element to achieve a full X-Y address capability for area arrays. CIDs are capable of both conventional sequential raster scan and random address. Additionally, CIDs can be operated in a unique nondestructive readout mode. This readout mode appears to provide a very powerful approach for increasing the signal to random noise level through repeated readouts which are summed.[28] Visible imager CID array technology has progressed considerably and 244x248 arrays are commercially available.

During the past few years the CID approach has also been applied to InSb. The pioneering work of Kim[23,29] in InSb MIS technology led to the successful development of CID arrays. Under DoD sponsorship, a 32-element linear array was successfully fabricated and evaluated. The key to the successful fabrication of these arrays was the development of a metal-SiON-InSb MIS multilevel overlapping gate process.

A charge injection device is conceptually simple. It is basically an array of MOS capacitors which are sequentially scanned by silicon MOS shift registers. Each unit cell consists of two closely coupled MOS capacitors so that charge can be readily transferred between the two storage sites. Figure 4.1 shows the layout of an CID area array and illustrates the principles of operation. During the integration period, photogenerated charge is stored in both the row and column gates at each sensing site. When the vertical scan generator selects a row line, the signal charge at every gate in that line is transferred

ORIGINAL PAGE IS
OF POOR QUALITY

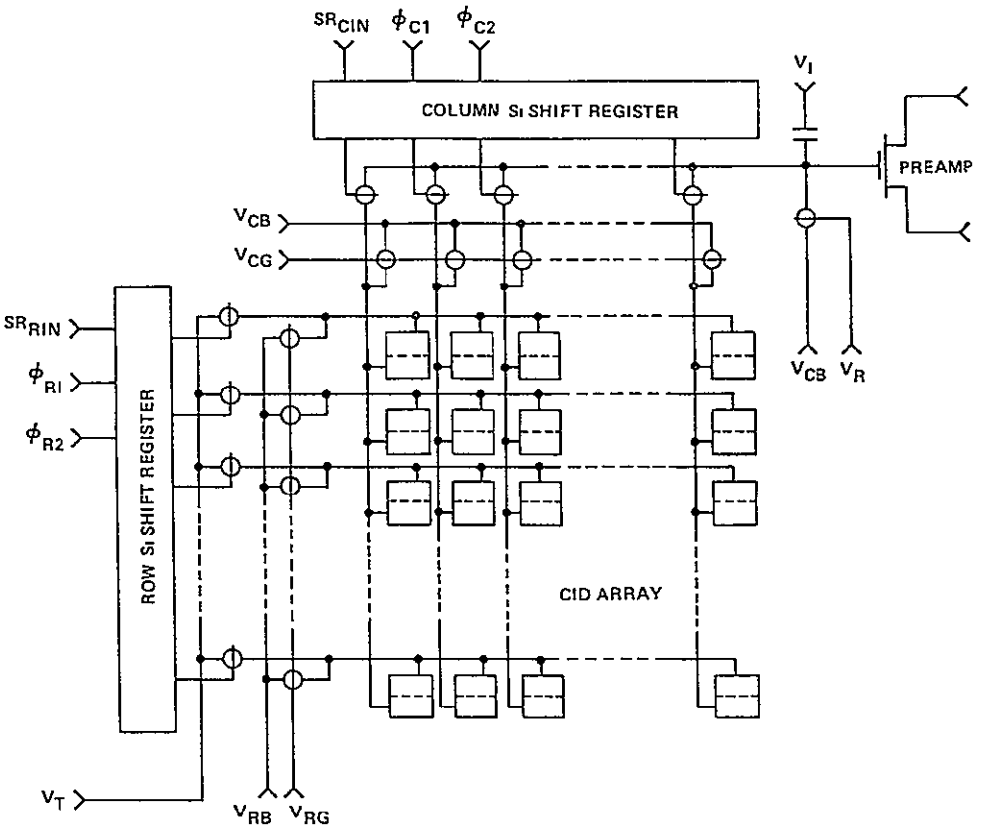


Figure 4.1 Schematic Diagram of Two-Dimensional CID Focal Plane Array Configuration, Used in a Staring Mode of Operation

to the corresponding column gate by setting its voltage to the low state. Charge at the selected site is injected into the substrate by applying an injection pluse through the selected column line. At the same time, any charge in the unselected elements of that column must be transferred into the corresponding row gates to avoid injection. For the selected element, charge injected into the substrate and the resultant displacement current is sensed as the signal. The charge in the unselected lines must simultaneously be transferred to avoid injection. This mode of readout is called the sequential injection technique. Readout may also be accomplished by a parallel injection technique, the charge is not injected until all of the elements of the selected row have been read out. All of the charge in the selected line can be injected simultaneously by driving all column voltages to zero. The parallel injection approach is useful where high speed readout is required.

Since charge must be transferred back and forth between row and column gates in each resolution element, close copuling between gates is necessary in an area array. Under Navy sponsorship, a number of gate structures were investigated for area array applications. Several of the gate structures were found to provide good coupling with potentials for reasonable yields. Several 16x24 arrays were subsequently fabricated utilizing several of the alternate gate structures. The size of the resolution elements was 2x2 mils spaced on 3 mil centers in one direction. Row and column silicon shift registers were mounted on the same substrate as the array and wire bonded to the row and columns of the array. CV characteristics of these 16x24 InSb arrays were evaluated at 77K as a screening procedure and a check on array uniformity. These results indicated uniform CV characteristics for all the rows and columns after array processing. Raw video displays of single-element response and image displays of "word" test patterns were also obtained demonstrating

for the first time raster scanned operation of an InSb area array in the staring mode.[30]

Very little quantitative performance data, however, has been reported for these arrays. Projection of area array performance for astronomical applications must therefore be based upon the more extensive data available from the evaluation of the linear arrays and the theoretical analysis of InSb CID array performance. InSb linear array performance has been measured in the temperature range from 77K to 4.2K.[31] It was found that the dark current and noise decreased several orders of magnitude as the array temperature was lowered from 75K down to about 30K, below which no measurable decrease was observed. Theoretical analysis of InSb arrays to assess their ultimate performance have been performed by a number of investigators.[30,32] These analyses have identified the major noise sources and combined with existing linear array data, can provide performance projections for InSb area arrays.

Figure 4.2 is the noise equivalent circuit of the CID. The noise sources are: 1) the kTC noise associated with the setting of the reference voltage across the total input shunt capacitance; 2) Johnson noise of the column selection switch and distributed resistance of the array column; 3) amplifier noise; 4) dark current shot noise, and 5) the shot noise associated with the background. Table III is a summary of these noise sources with appropriate expressions to calculate their magnitudes.

CIDs employ integrator reset switches (DC restore) which act to reset frequencies less than the clock frequency, and the high frequency signals are attenuated by the sampling effect to provide a bandpass filter for the noise. The effective low cutoff is the sampling rate f_s and the upper cutoff frequency is determined by the minimum bandwidth required $\Delta f = 2 f_s$. The

TABLE III. NOISE SOURCES FOR A CID ARRAY[33]

KTC Noise	$\bar{N}_{eqC} = \sqrt{kTC_T}/q$
Selection Switch Thermal Noise	$\bar{N}_{eqR} = C_{col}\sqrt{4\ kTR_{so}\Delta f}/q$
Amplifier Noise	$\bar{N}_{eqA} = C_T \dfrac{\sqrt{(8\ kT\Delta f/3g_m) + 10^{-13}\ \ell n3}}{q}$
Dark Current Shot Noise	$\bar{N}_{eqD} = \sqrt{8x10^{11}A_dT_I}$
Background Shot Noise	$\bar{N}_{eqB} = \sqrt{\eta\phi_B A_d T_I}$

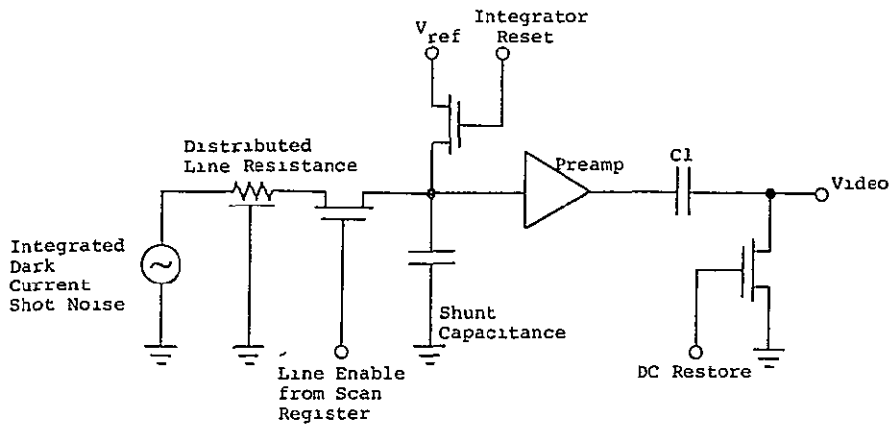


Figure 4.2 Representative CID Noise Equivalent Circuit

ORIGINAL PAGE IS
OF POOR QUALITY

expression in Table II was derived by integrating the noise power spectral density between these two limits.

Figures 4.1 and 4.2 illustrate one of the major limitations of the CID approach. Note that the sensing of an individual element, the shunt capacitance loading of the output amplifier includes the line capacitances of the selected row and column, if all others are assumed to be floating, the input capacitance of the MOS input device, and the injection coupling capacitance. For the 12 x 16 array, the total shunt capacitance C_T is estimated to be about 15 pf. The responsivity of the output amplifier is given by

$$R_c = \frac{q}{C_T} \times 10^6 \ \mu V/\text{election} \tag{4.1}$$

For C_T of 15 pf, R_c = .011 μV/e, i.e., a signal charge of 10^6 electrons results in an output of 11 mV. As the number of array elements increase, the responsivity will further decrease due to the increase of C_T. On the other hand, the output capacitance of a CCD array is the capacitance of a reverse biased diode and is of the order of .1 pf, independent of the size of the array.

Table IV summarizes the calculated number of noise carriers for the noise sources listed in Table III for an integration time of 5×10^{-3} sec. As seen from Table IV, the kTC noise is the dominant noise. Fortunately, this source of noise can be completely eliminated by AC coupling followed by DC restoration as shown in Figure 4.2, i.e., by the double correlated clamping technique. Note that even for an integration time of 5×10^{-3} sec, the shot noise due to the dark current dominates.

Figure 4.3 is a plot of the total CID noise at 77K for an integration time of 1.5 msec, as a function of the background photon flux. As expected, at high background flux, the noise is dominated by the shot noise in the background with background limited performance at about 10^{13} photons/cm^{2}sec. At lower backgrounds, shot noise due to the integrated dark current predominates. The number of noise carriers in this region is about 320.

TABLE IV. Calculated Noise Levels for the 16x24 InSb CID

KTC Noise ($\bar{N}_{eqC}$)	800 carriers (removed by double correlated sampling)
Selection Switch Termal Noise ($\bar{N}_{eqR}$)	180 carriers
Amplifier Noise ($\bar{N}_{eqA}$)	144 carriers
Dark Current Shot Noise ($\bar{N}_{eqD}$)	320 carriers
Background Shot Noise ($\bar{N}_{eqB}$)	25 carriers for $\phi_B = 10^{10} p/cm^2 sec$

$t_{int} = 5x10^{-3} sec$
$T = 77^{o}K$
$A_d = 2.58x10^{-5} cm^2$
$C_T = 15$ pf
$C_{col} = 7$ pf
$\Delta f = 4$ MHz

ORIGINAL PAGE IS
OF POOR QUALITY

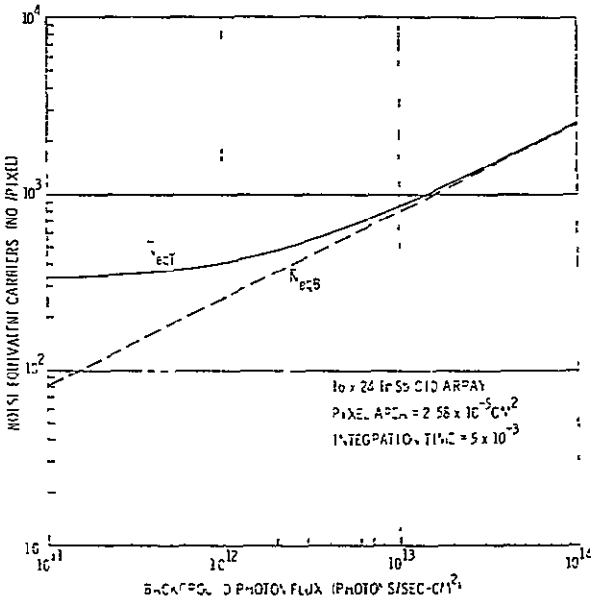


Figure 4.3 Calculated Noise Equivalent Carriers of All Noise Sources vs. Background Photon Flux for an Integration Time of 5×10^{-3} sec.

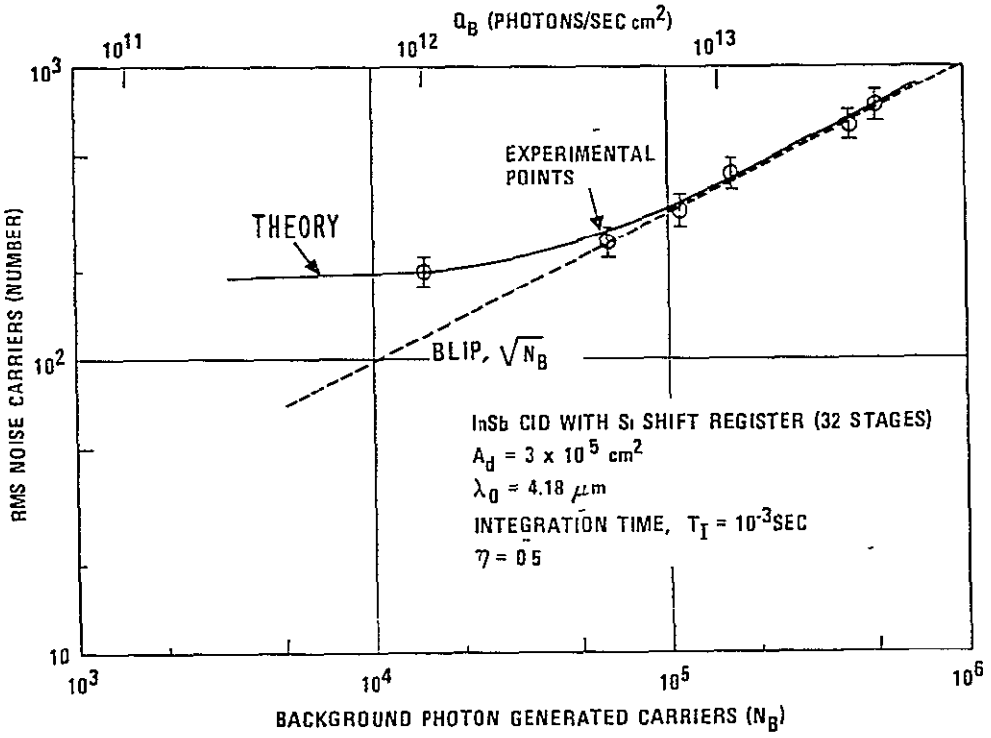


Figure 4.4 Measured RMS Noise Carriers of All Noise Sources vs. Background Photon Flux for a 32-Element InSb CID Line Array

Figure 4.4 shows a comparison of the noise model with measured data for a 32 element line array. The solid line is a plot of the calculated noise of all noise sources based upon the array noise model for the 32-element line array. It can be seen that the array performance model compares faborably with the experimental data.

For low background astronomical applications, the shot noise due to the dark current can be made negligible by simply operating at temperatures below the nominal $77^{o}K$ operating temperature. The dark current reduction due to the exponential decrease in the intrinsic carrier concentration with temperature is given by Equation 2.3. Dark current reductions comparable to the values in Figure 2.3 should be possible for InSb CID arrays. Operation at low temperatures will also increase the maximum permissible integration time. Dark charge, during the integration period, is collected under both gates of a CID element, and charge saturation occurs when each gate is half filled, i.e., $N_{SAT} \approx 1/2(C_{ox}V_{eff}/q)$. For InSb CID, $N_{SAT} \approx 2x10^{11}$carriers/$cm^2$. Utilizing this typical value and including the exponential temperature dependence of the intrinsic carrier concentration n_i, the maximum integration time can be calculated. The results are show in Figure 4.5.

Note that integration times limited only by the background flux should be realizable by cooling to $50^{o}K$ or less. Under these conditions, array performance should become amplifier noise limited. However, with present state of the art InSb CIDs, ultimate detectivity at low backgrounds is not limited in practice by amplifier noise, but rather by the degree to which the fixed pattern noise can be rejected. Fixed pattern noise effects, in general, are more dominant at low backgrounds for CIDs than for CCDs due to the variations introduced by the line column, and switch capacitances, and the lower signal responsivity of the output amplifier. Considerable development will be

required in the device processing to obtain amplifier noise limited performance at low backgrounds.

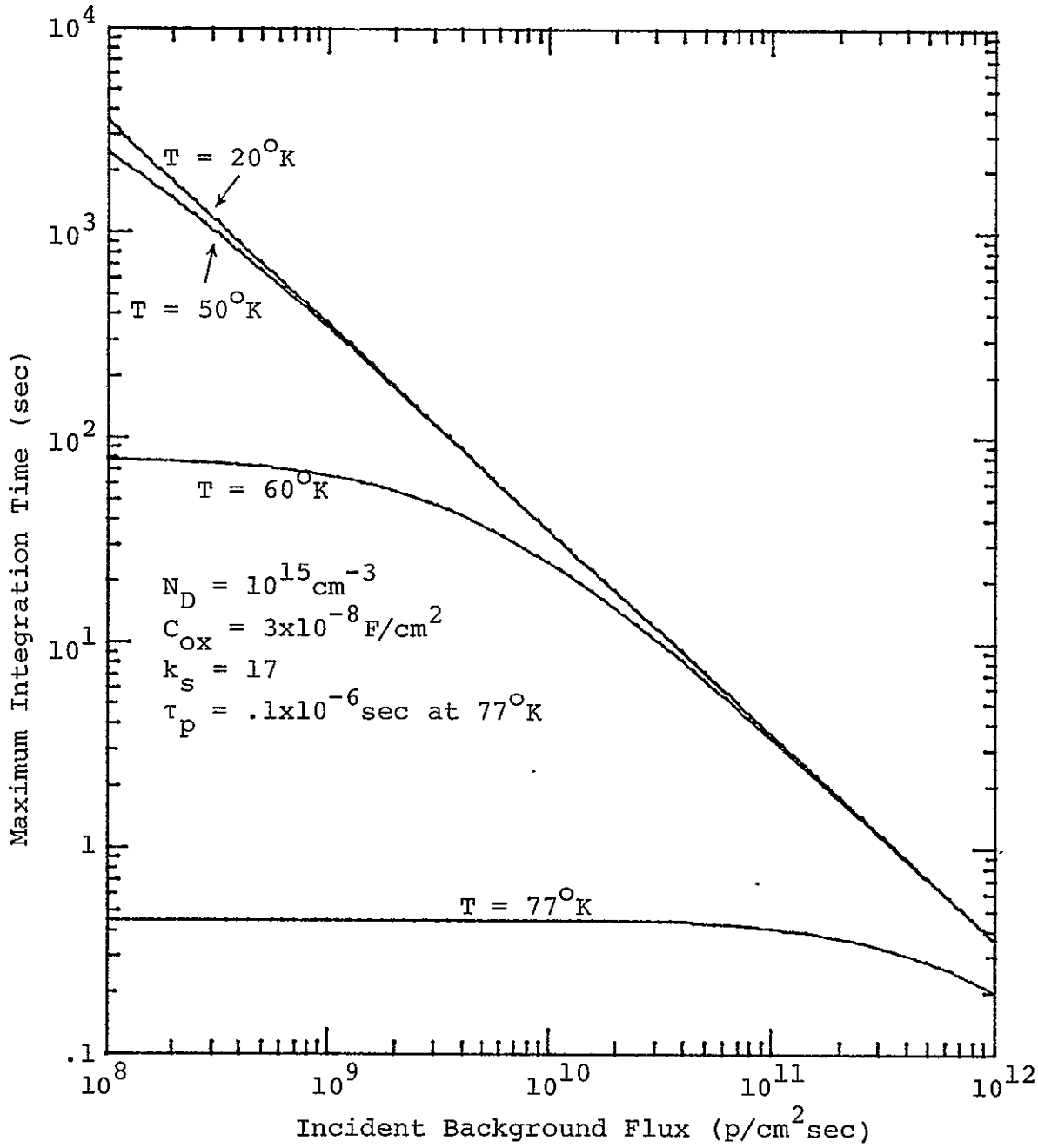


Figure 4.5 Calculated Maximum Integration Time vs. Incident Background Flux for a InSb CID Array

V. HYBRID FOCAL PLANE ARRAYS

Hybrid focal planes represent a pragmatic approach to a high density focal plane in which a photodetector array is electrically and mechanically coupled to a silicon readout multiplexer. This approach combines the best of a mature detector technology with the well-developed silicon CCD technology.

The hybrid approach is the most versatile and flexible of the focal plane approaches currently under development. The versatility and advantages of the hybrid approach arise principally from the ability to select and optimize independently the photodetector array and readout multiplexer. A single "universal" CCD multiplexer, for example, can be designed, fabricated and used for a variety of detector arrays.

The separation of the sensing and readout media allows the benefits of CCD readout to be realized in a number of intrinsic detector materials whose MIS properties make it difficult to achieve viable CCD operation. The benefits of intrinsic detectors, i.e., high operating temperatures, high quantum efficiency, and low crosstalk are also realized. The hybrid approach can also be used to fabricate focal planes of extrinsic detectors incorporating dopants that are not compatible with the high temperature processing requirements of silicon, since the silicon and detector media can be processed separately.

Another significant advantage is the increased silicon chip area due to the separation of the detector and multiplexing functions. This makes possible greater flexibility in the CCD design and potentials for the incorporation of more sophisticated on-chip signal processing functions than a fully monolithic design.

The hybrid approach, however, does have its disadvantages and introduces a number of critical issues. Of critical importance from the standpoint of yield, reliability, and performance is the

mechanical and electrical interface which a hybrid structure requires to couple the detector array and the silicon multiplexer. The number of interconnects required can be large since a detector/multiplexer interconnect is required for each element. Difference in the thermal expansion coefficient between the detector array material and the silicon multiplexer can result in significant mechanical stress and poor reliability after temperature cycling of the arrays. The thermal expansion mismatch between the detector substrate and the silicon multiplexer thus may place a limitation on hybrid array size.

An efficient input circuit is also needed to inject the detector signal into the CCD multiplexer. Direct injection circuits are simple, but are sensitive to gate threshold non-uniformities. Input circuits have been proposed and demonstrated which reduce the effects of gate threshold non-uniformity but at the expense of increased circuit complexity and power dissipation. Resolution of the gate threshold non-uniformity problem remains one of the critical issues for hybrid focal planes.

5.1 HYBRID FOCAL PLANE CONFIGURATION

A number of hybrid focal plane configurations are currently under development. The critical problem for a hybrid is the thermomechanical compatibility of the detector material and the silicon CCD. Since the detector materials of interest will in general contract more than the silicon, cracking and delamination of the detector material can occur with temperature cycling. The magnitude of the contraction can be calculated from the known thermal expansion coefficients and the results are shown in Figure 5.1. The III-V semiconductors and (Hg,Cd)Te have reasonable expansion mimatches to silicon. On the other hand, the large mismatch for PbSnTe is a deterrent to fabricating large PbSnTe hybrid arrays.

Two of the most widely employed hybrid focal plane structures are shown in Figures 5.2 and 5.3. In the structure of Figure 5.2, the detector layer is directly epoxied onto a silicon CCD multi-

ORIGINAL PAGE IS
OF POOR QUALITY

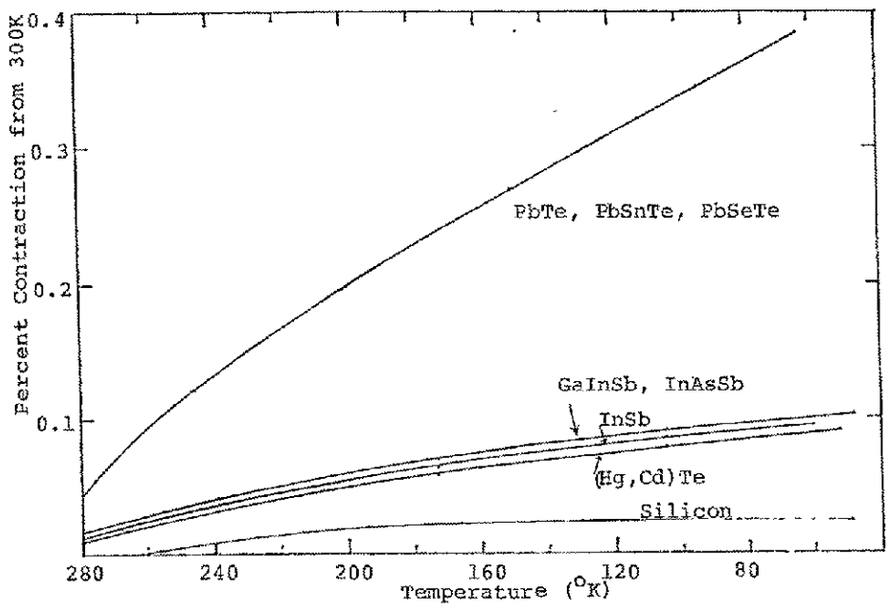


Figure 5.1 Detector Material Compatibility with Silicon: Percent Contraction from 300K

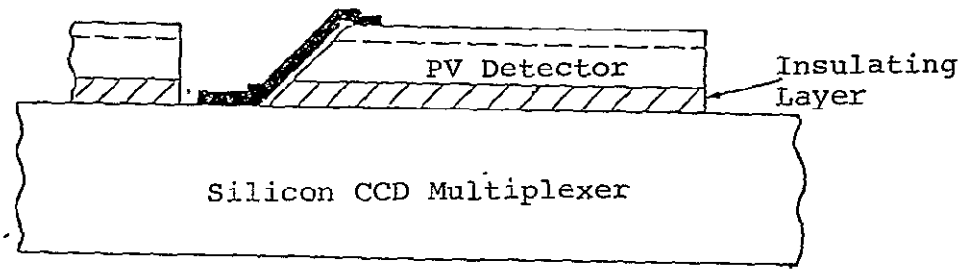


Figure 5.2 Hybrid Structure Employing Direct Epoxying of Detector Array to CCD

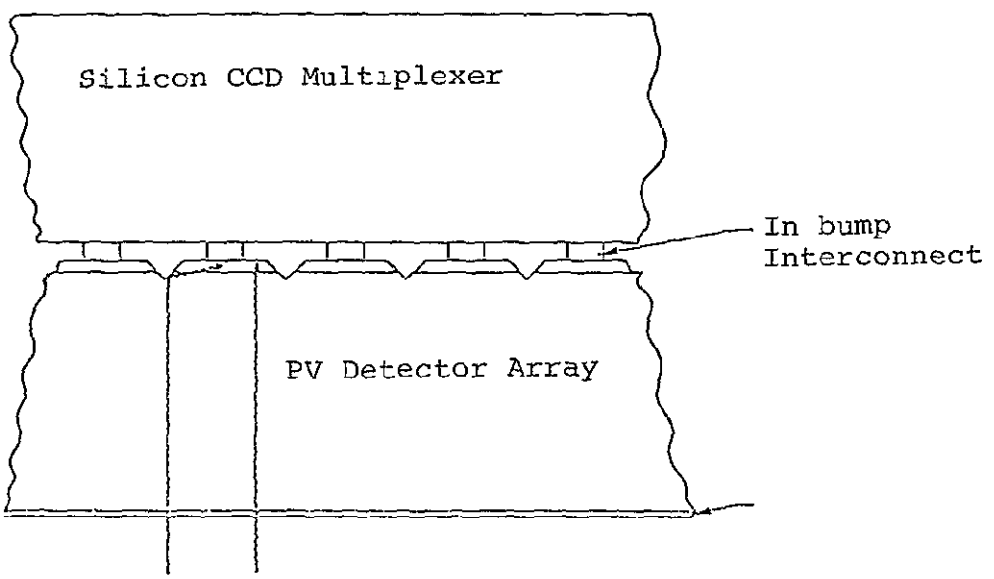


Figure 5.3 Hybrid Structure Using Flip-Chip Bonding of Detector Array to CCD

plexer. The thermal expansion coefficient of the detector material must closely match that of silicon. The insulating epoxy must also remain ductile during the temperature cycling to relieve the mechanical stress due to the differential contraction during temperature cycling. This structure is not a high density structure because of the space that the detector/CCD metallization requires. Additionally, optical fill factors of greater than 50 percent are difficult to achieve for the same reason.

The second design, shown schematically in Figure 5.3 is the flip-chip solder bump cold weld approach. Indium is the preferred material for the solder bumps due to its low-yield stress even at cryogenic temperatures. This approach has a number of significant advantages with respect to yield, performance and detector compatibility. As shown in Figure 5.3, this approach is ideally suited for transparent backside illuminated detector arrays. Because the metallization is on the bump side of the array, no obscuration of the active detector array occurs and high fill factors can be achieved. The utilization of a thick transparent substrate also adds mechanical rigidity to the structure. Since the CCD and detector array can be screened and tested prior to bump interconnection, the potential for high yields exist. Finally, the use of In as the bump material with its favorable deformation properties and adjustable aspect ratio can accommodate larger thermal expansion mismatches than the epoxied structure shown in Figure 5.2.

Significant progress in flip-chip In bump bonding technology has been made in the last few years. A InAsSb detector array with elements on 4 mil centers was successfully mated to a FET switch array.[34,35] An interconnect yield of 98 percent was obtained and maintained through 12 temperature cycles down to 77K. A mated PbSnTe/FET multiplexer has also been demonstrated. Thermal cycling experiments with this structure showed that only limited size arrays were possible because of large thermal expansion

coefficient mismatch between PbSnTe and silicon.[35] Photovoltaic InSb detectors have also been successfully flip-chip bonded to silicon test substrates having metallized lead patterns.[36] A process was developed in which InSb diode arrays could be In bump connected to silicon CCD multiplexers and the resulting structure thinned to the required thickness.

Significant progress continues to be made in the design and fabrication of CCD multiplexers for hybrid application. Several new direct injection CCD multiplexer designs have evolved and are in the early stages of fabrication. These CCD multiplexer chips can be utilized for hybrid readout or can be processed on extrinsic substrates to yield monolithic extrinsic arrays.

Similar progress has been reported on the hybrid approach employing direct epoxying of the detector material to the CCD substrate.[37] Two slabs of (Hg,Cd)Te on which 32-detector elements were fabricated were epoxied to a CCD signal processor. This array was repeatedly cycled from 300K to 110K with no failures. An electrical evaluation of the 32 element array demonstrated minimal loss of signal to noise ratio due to the CCD readout of the PV detectors.

52. DETECTOR TYPES FOR HYBRID ARRAYS

Hybrid focal plane arrays can, in principle, be fabricated in all extrinsic semiconductors. The hybrid approach can also be extended to include both extrinsic silicon and germanium detector arrays. Thermal expansion mismatch problems, would, of course, be absent for these materials.

Hybrid technology, however, has concentrated on only a few of the most developed and promising of the compounds from the III-V, IV-VI, and II-VI material systems. An excellent compilation of the properties of these materials can be found in the review article by Longo, et al.[35]

Theoretically, both photoconductive and photovoltaic intrinsic detectors are suitable for hybrid arrays. The development efforts in recent years, however, have focused on photodiodes operated at near zero bias. Photodiodes are preferable for focal plane arrays because their impedances are comparable to the input impedance of a CCD so that direct coupling into the CCD is possible. Low impedance photoconductors such as (Hg,Cd)Te require a buffer state to provide current gain to couple into a CCD. The higher impedance of photodiodes also minimizes on-chip power dissipation, and important consideration of large high density mosaic focal planes operating in the staring mode.

Two of the most promising of the detector materials for hybrids are the III-V semiconductors InSb, and the ternary alloy $InAs_{1-x}Sb_x$. InSb is an attractive candidate for hybrids because of the maturity of InSb photodiode technology and the availability of large, high quality InSb bulk substrates. InSb photodiode arrays are currently under development for both staring and TDI scanning systems. The D* and responsivity of InSb photodiode arrays have been shown to be comparable to discrete InSb detectors. This point is illustrated in Figure 5.4 for a back illuminated InSb array.[36] In addition, a significant advance for InSb arrays was the development of a low S (surface recombination velocity) back surface passivation process which yields repeatedly, detectors with the response shown in Figure 5.5. The high quantum efficiency at the short wavelengths demonstrates the success of the passivation process for the low S input surface.

The $InAs_{1-x}Sb_x$ alloy system offers greater flexibility than InSb in a number of respects. First of all, the spectral bandwidth and the long wavelength cutoff of the alloy can be tailored to fit the desired spectral range. Response out to 9 μm is, in principle, possible. Secondly, the thick transparent substrate provides mechanical strength to the structure, an important feature during the hybrid bump mating process. Finally, thinning

ORIGINAL PAGE IS
OF POOR QUALITY

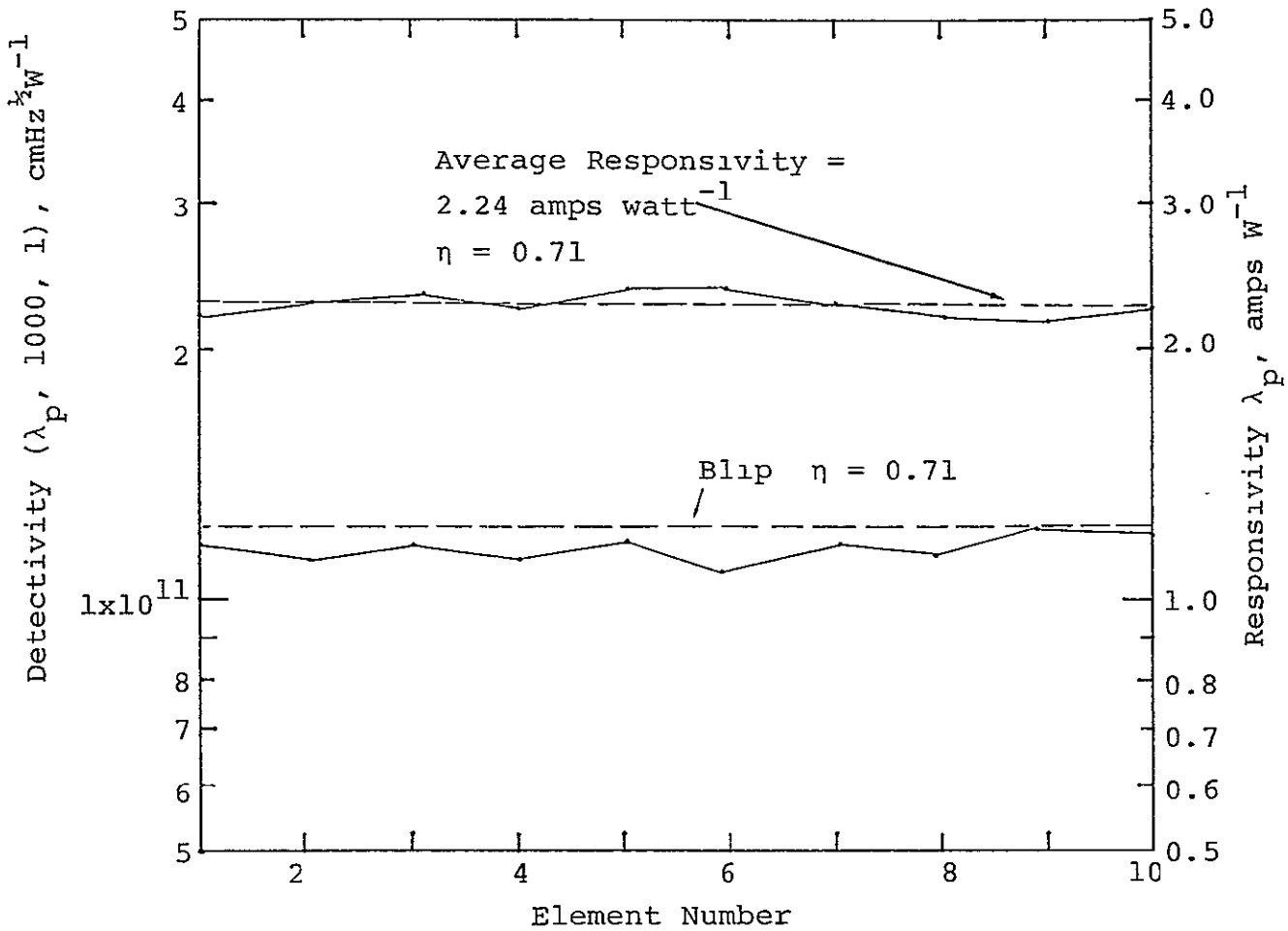


Figure 5.4 Performance Data on a Recently Measured Backside-Illuminated InSb Array (Q_B = 1x10^{16} Photons/sec-cm^2; T = 77K)

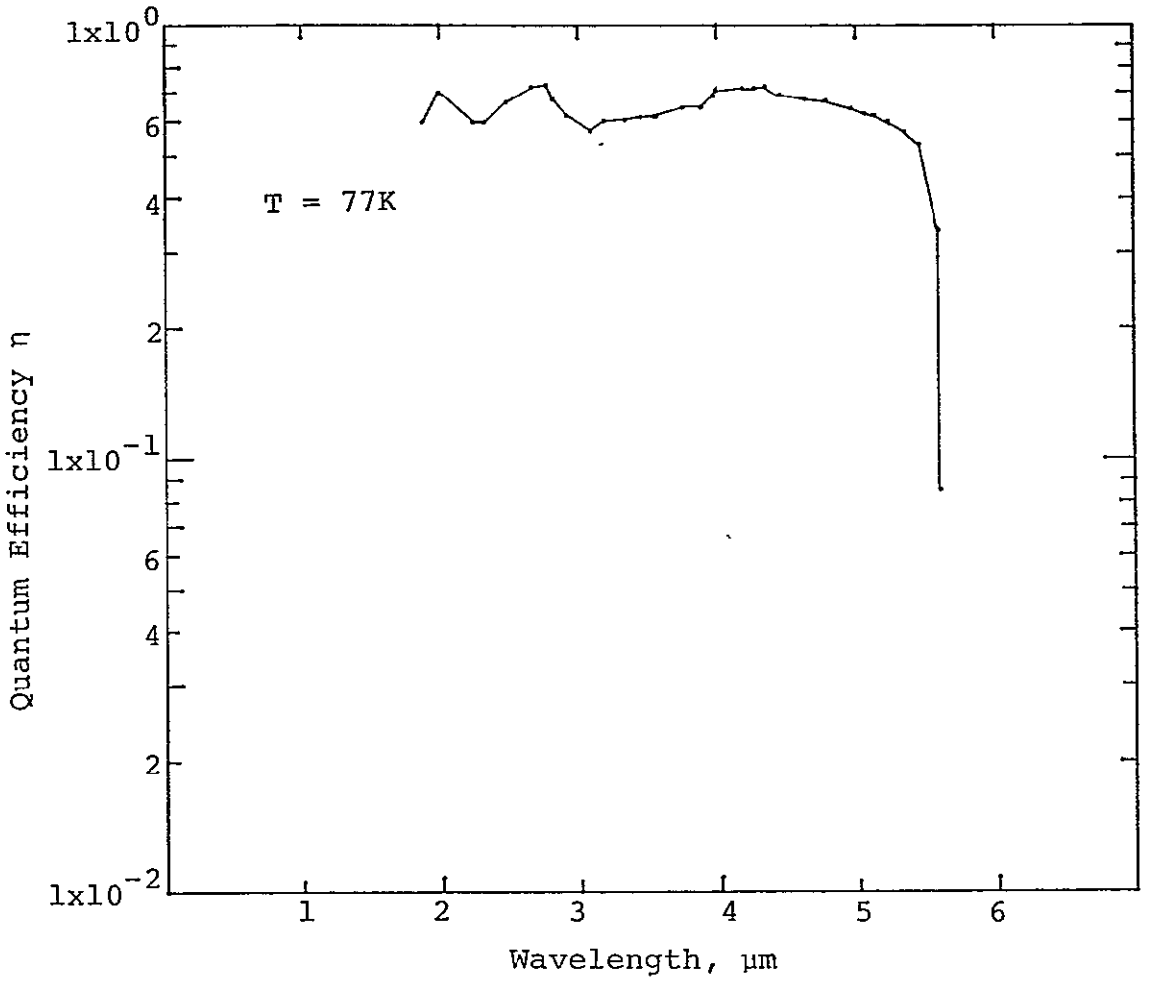


Figure 5.5 Measured Quantum Efficiency Versus Wavelength for Backside-Illuminated InSb Detectors

ORIGINAL PAGE IS
OF POOR QUALITY

is not required after mating since the substrate is transparent. On the other hand, advanced growth technique involving liquid phase epitaxy are required for fabrication.

Figure 5.6 shows the basic structure for a backside illuminated $InAs_{1-x}Sb_x$ photodiode.[27] This multilayer detector is produced by a liquid epitaxy growth method. The device consists of four different regions: 1) active layer; 2) filter layer; 3) buffer layers; and 4) transparent substrate. The incident radiation enters at the bottom of the structure through a substrate that is transparent in the region of interest. Further filtering is provided by the filter layer, while the desired radiation is absorbed in the active layer. The buffer layers serve to relieve the lattice mismatch between the InAs substrate and the $InAs_{1-x}Sb_x$ detector layer.

The measured spectral response of three typical $InAs_{1-x}Sb_x$ photodiodes with different Sb composition in the active and filter layers are shown in Figure 5.7.[27] Internal quantum efficiency of 90% and a R_oA product of $2x10^7$ ohm-cm^2 have been obtained at 77K for these detectors.

Another detector material which shows potential for application to hybrids where longer wavelength cutoffs are desired is the $Pb_{1-x}Sn_xTe$ alloy system. Backside illuminated $Pb_{1-x}Sn_xTe$ heterojunction alloy photodiodes, similar in structure to the $InAs_{1-x}Sb_x$ photodiodes have been fabricated.[38,39] Figure 5.8 shows the spectral response at 85K for two compositions. The sharp cutoff below 6 μm is due to the PbTe substrate. The long wavelength cutoff is determined by the Sn content of the active layer and the operating temperature. The Pb SnTe alloy systems exhibit large Burnstein-Moss shifts in the bandgap with temperature due to the extremely low values of effective mass. The 50% cutoff of the $Pb_{0.8}Sn_{0.2}Te/PbTe$, for example, shifts from 11.5 μm at 85°K to 14.5 μm at 15K.

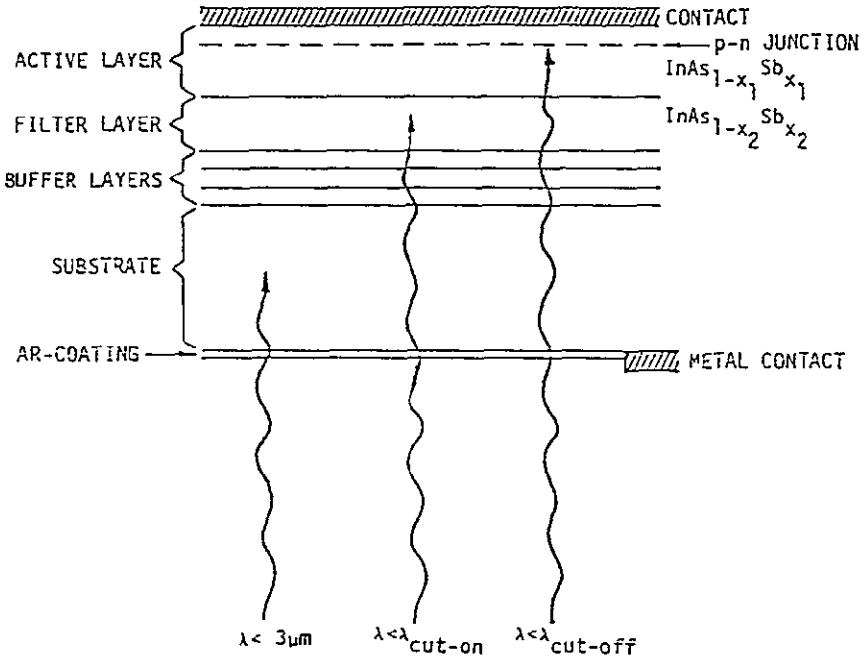


Figure 5.6 Backside-Illuminated Device Design

ORIGINAL PAGE IS
OF POOR QUALITY

ORIGINAL PAGE
OF POOR QUALITY

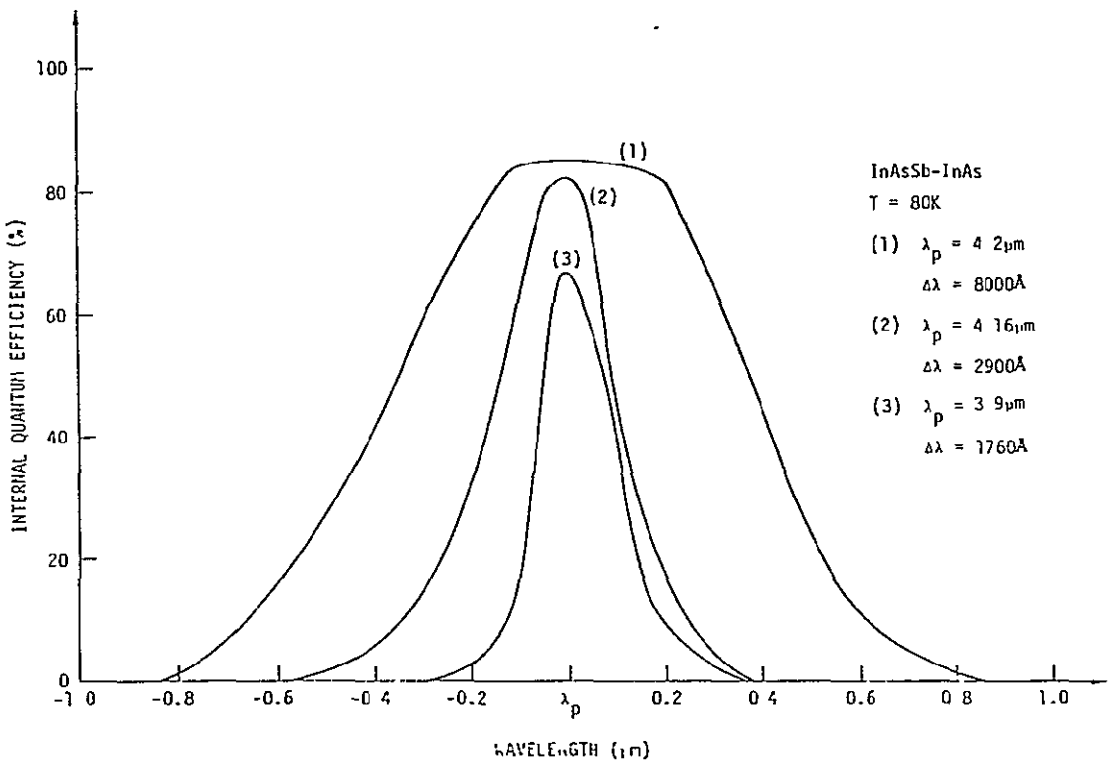


Figure 5.7 Experimentally Measured Absolute Spectral Response Curves for Three Different Back-side-Illuminated InAsSb Devices. (The Sb composition difference between the active layer and the filter layer are ∿2.3% for device 1, ∿1.3% for device 2, and ∿0.5% for device 3.)

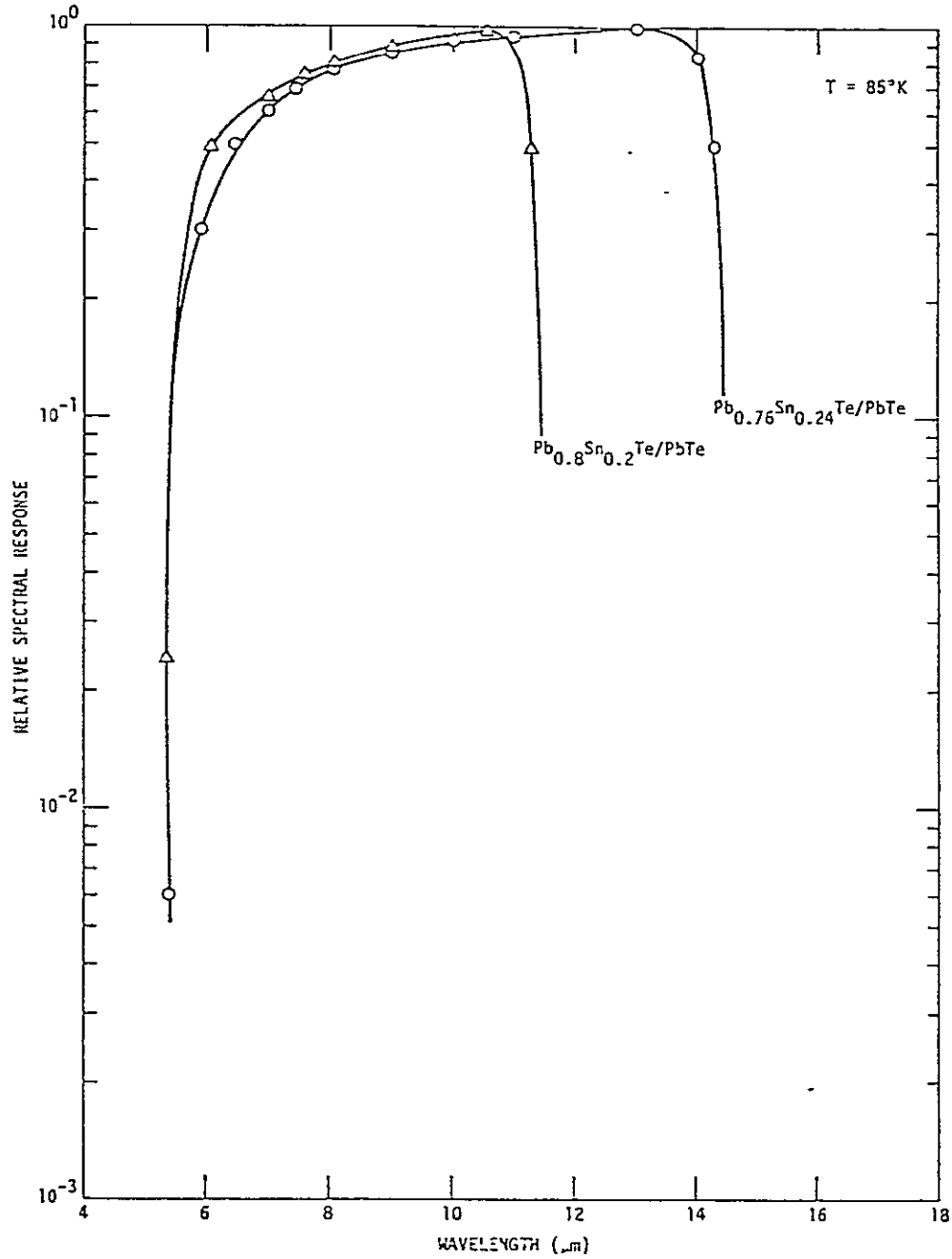


Figure 5.8 Relative Spectral Response at 85°K for $Pb_{0.8}Sn_{0.2}Te/PbTe$ and $Pb_{0.76}Sn_{0.24}Te/PbTe$ Diodes

ORIGINAL PAGE IS
OF POOR QUALITY

Performance parameters and figure of merits typically quoted for these photodiodes are their D* and R_oA products. D* for a photodiode is determined by the thermal noise source of the detector resistance and the background photon noise. Photodiodes provide near maximum signal to noise ratio at zero bias. The D* for the zero bias condition is given by the familiar expression,

$$D^*_\lambda = \eta\lambda \frac{q}{hc} \left[\frac{4kT}{R_oA} + 2q^2\eta\phi_B \right]^{-\frac{1}{2}} \tag{5.1}$$

where R_oA is the zero-bias resistance-area product,

T is the detector temperature,

η is the internal quantum efficiency.

Equation 5.1 is plotted in Figure 5.9 as a function of background photon flux and R_oA product at 77^oK.

At low backgrounds, D* is limited by the thermal noise of the detector which is directly related to the R_oA product, and reduces to

$$D^* = \frac{\lambda\eta q}{hc} \left(\frac{R_oA}{4kT} \right)^{\frac{1}{2}} = 1.08\text{x}10^{11} \lambda\eta \left(\frac{R_oA}{T} \right)^{\frac{1}{2}} \tag{5.2}$$

where R_oA is the unit of ohm-cm^2 and λ is in μm

The R_oA of a photodiode is defined as

$$R_oA = \left[\frac{\partial J}{\partial V} \Big|_{V=0} \right]^{-1} \tag{5.3}$$

where J is the total thermal current density and is the sum of the diffusion current, depletion layer generation-recombination current, surface leakage (shunt) currents, and tunnel currents. Diffusion current is due to the diffusion of thermally generated minority carriers from the n and p sides of the semiconductor to the depletion layer at the junction interface and is only significant at high temperatures. Generation-recombination (g-r) current is due to the thermal generation and recombination of carriers in the depletion layer.

ORIGINAL PAGE IS
OF POOR QUALITY

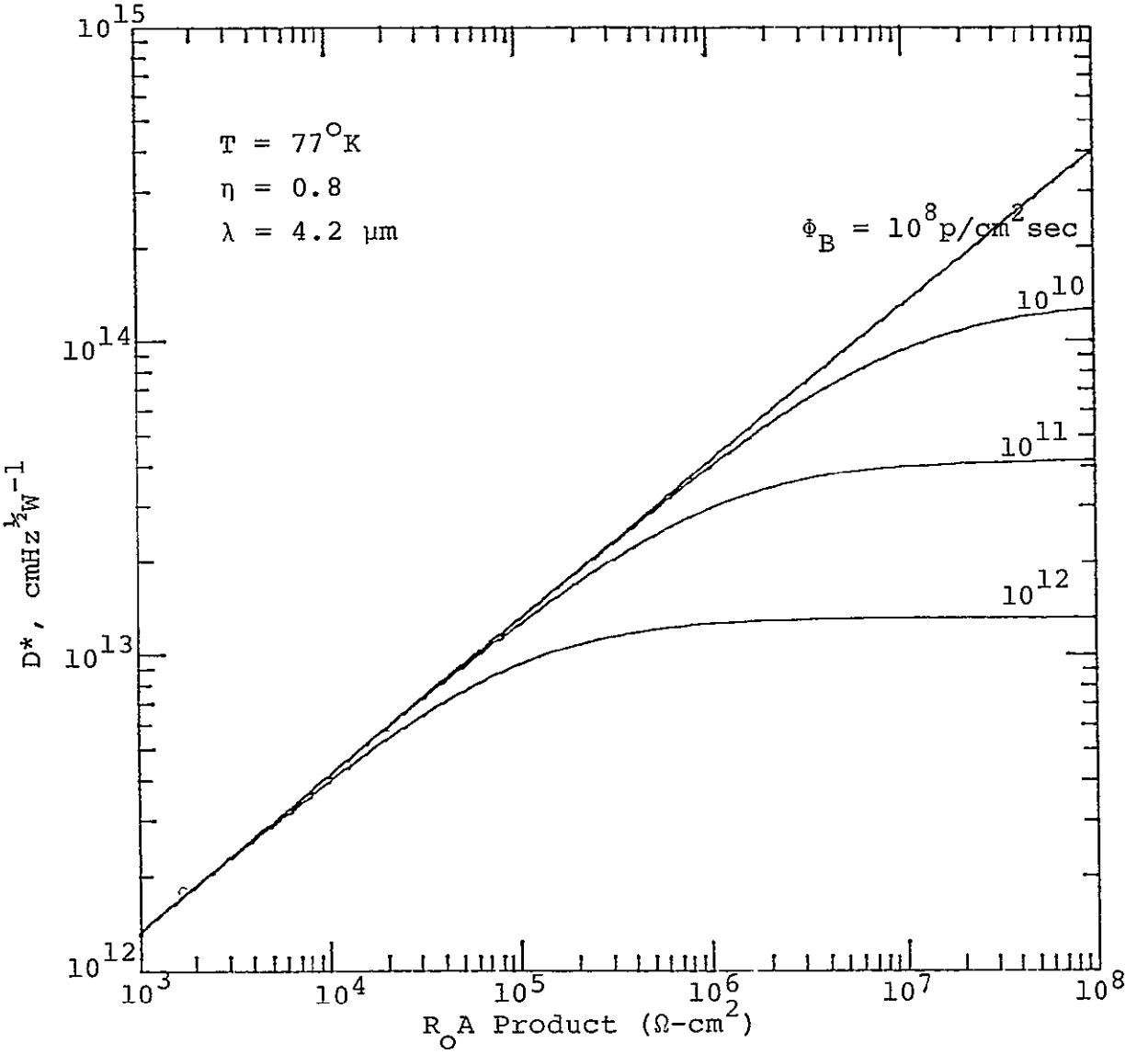


Figure 5.9 D* as a Function of R_oA Product for an $InAs_{.85}Sb_{.15}$ Detector at 77K

Equation 5.3 can be rewritten as

$$R_oA = \left[\frac{\partial}{\partial V}(J_D + J_{GR} + J_T + J_s)\Big|_{V=0}\right]^{-1} \tag{5.4}$$

$$= \left[\frac{1}{R_oA_D} + \frac{1}{R_oA_{G-R}} + \frac{1}{R_oA_T} + \frac{1}{R_oA_s}\right]^{-1}$$

where R_oA_D, R_oA_{G-R}, R_oA_T and R_oA_s are the R_oA products due to diffusion, generation-recombination, bulk tunneling, and surface leakage respectively. Expressions for R_oA_D, R_oA_{G-R} and R_oA_T have been derived for abrupt p^+n junction.[40] The expressions are listed in Table V. The R_oA product is dominated at high temperatures by diffusion current since $R_oA_D \alpha (1/n_i^2)$. As the temperature is decreased, the photodiode will become dominated by the g-r noise since $R_oA_{G-R} \alpha (1/n_i)$. At some lower temperature, the shunt leakage and tunnel currents will dominate and the R_oA product will become independent of temperature.

R_oA products have been measured for the $InAs_{1-x}Sb_x$ and $Pb_{1-x}Sn_xTe$ alloys as a function of temperature and are in general agreement with theory. Figure 5.10 shows the experimental determined R_oA products for representative $InAs_{1-x}Sb_x$ diodes sampled from a 32x32 diode array.[41] Also shown is the theoretical value for R_oA_{G-R} calculated for $\tau = 0.5$ μsec. Note that at temperatures above 120 K, the curves fit the g-r model. At lower temperatures, the R_oA is dominated by leakage currents. At low temperatures, considerable variation in the R_oA products are found since the surface leakage is highly processing dependent. R_oA products have also been measured for $Pb_{1-x}Sn_xTe$ diodes (x = .27) sampled from a 12x16 array. The average R_oA product was found to be 2.2 ohm-cm^2 at 92°K with the leakage being diffusion dominated at this temperature. The value increases to about 16 ohm-cm^2 at 77°K.

5.3 DETECTOR/CCD COUPLING

In an intrinsic CCD imager, such as the InSb CCD and silicon visible imager CCDs, detection and collection of the signal current occurs in the same medium. The photo-generated minority carriers

TABLE V. R_oA PRODUCTS

$$R_oA = \left[\left(\frac{1}{R_oA}\right)_D + \left(\frac{1}{R_oA}\right)_{G-R} + \left(\frac{1}{R_oA}\right)_T\right]^{-1}$$

$$R_oA = \left(\frac{kT}{q}\right)^{\frac{1}{2}}\left(\frac{\tau_e}{\mu_e}\right)^{\frac{1}{2}} \frac{N_A}{qn_i^2}$$

$$R_oA_{G-R} = \left(\frac{N_A kT}{2\varepsilon\varepsilon_o} \ln \left\{\frac{N_A N_D}{n_i^2}\right\}\right)^{\frac{1}{2}} \frac{\tau_o}{qn_i}$$

$$R_oA_T = \frac{8\pi^2 h^3 kT}{m^* q^2 E_p^2} \exp\left[\frac{\pi}{3qh}\left(\frac{m^*\varepsilon_s}{N_D}\right)^{\frac{1}{2}} E_g\right]$$

R_oA_s is temperature independent

ORIGINAL PAGE IS
OF POOR QUALITY

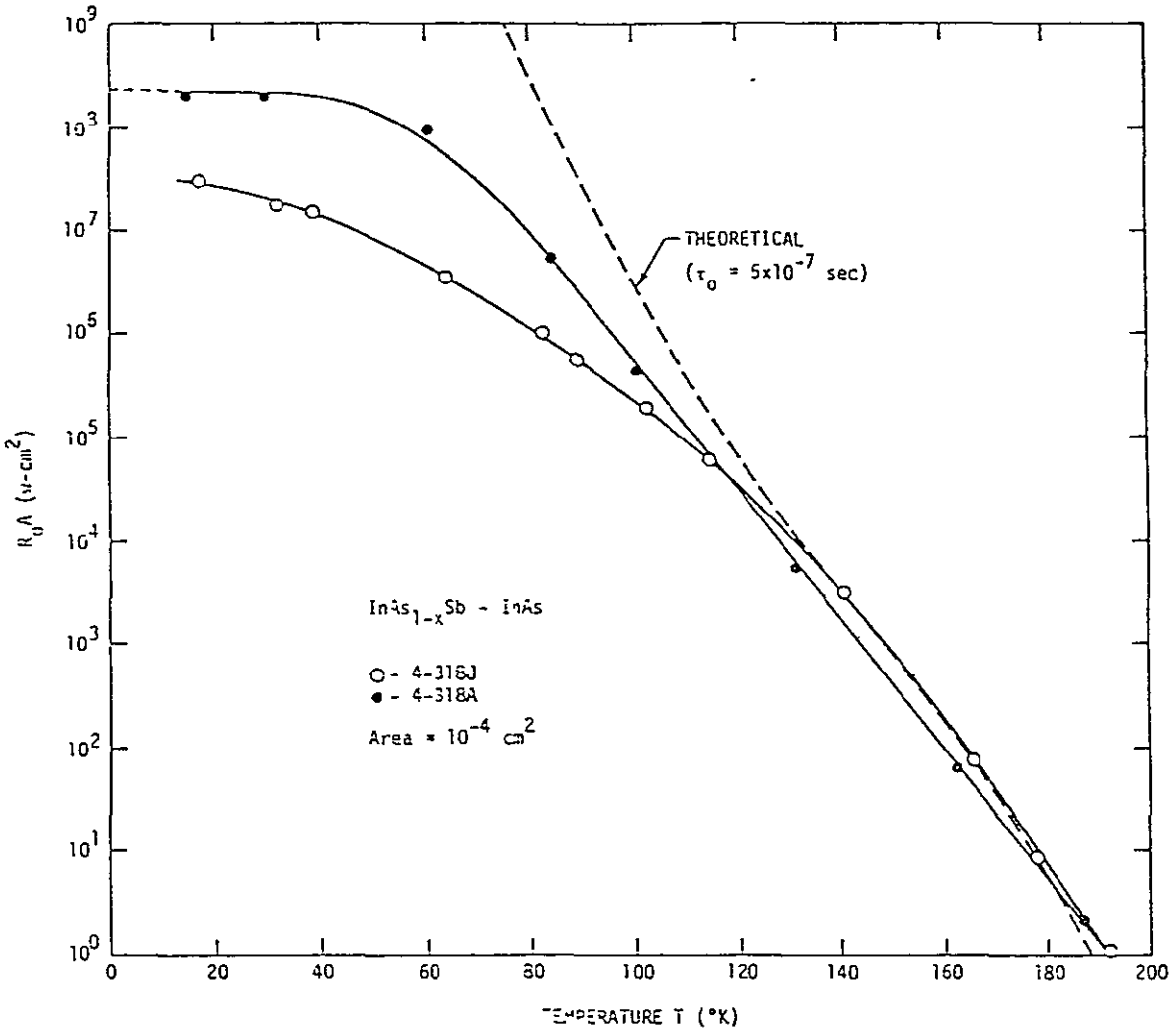


Figure 5.10 Zero-Bias R_oA Product as a Function of Temperature for Two $InAs_{1-x}Sb_x$-InAs Detectors

are directly collected by the depletion regions underneath the charge storage gates with high efficiency. Input time constants are also short since the injection collection process is only limited by the drift and diffusion times of the carriers.

In the case of a hybrid focal plane, a detector/CCD coupling circuit is required since the photo-current from the detector must be transferred to the silicon multiplexer. The key performance requirement for such a circuit is to convert the detector current to an equivalent CCD current with high efficiency and minimal added noise such that the signal to noise ratio is limited only by the detectivity of the detector. The complexity of the detector/CCD circuit is severely limited by the available area at each pixel site and to date only the simplest coupling circuits have been investigated for hybrids. These coupling circuits can be divided into direct and indirect injection.

The two basic injection schemes are shown in Figure 5.11 and 5.12. The direct injection scheme shown in Figure 5.11 and related variants on this scheme are most often employed because of their inherent simplicity and compatibility with the dimensions of the unit cell. In Figure 5.11, referred to a direct injection or source modulation, the signal current from the detector is used to modulate the source of the MOSFET input. The MOSFET gate is G_1, and is biased at DC while the source is floating. The potential well under G_2 acts as an induced drain into which the current from the detector is injected and integrated before transferring to the CCD multiplexing channel and ϕ_1. In Figure 5.12, referred to as gate modulation or indirect injection, the signal current from the detector converted to a voltage signal via a load resistor or buffer amplifier. The resultant voltage swing is directly applied to the gate and modulates the channel current.

The AC equivalent circuit for the direct injection scheme is shown in Figure 5.13. The injection efficiency, i.e., the

ORIGINAL PAGE IS
OF POOR QUALITY

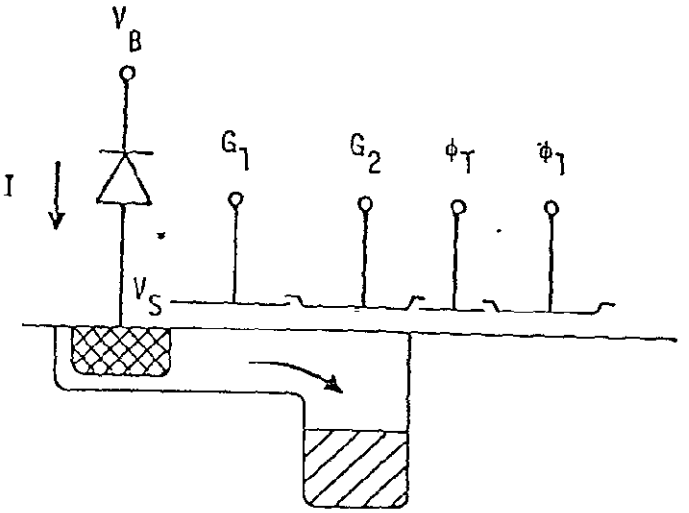


Figure 5.11 Direct Injection (Source Input) Interface Circuit

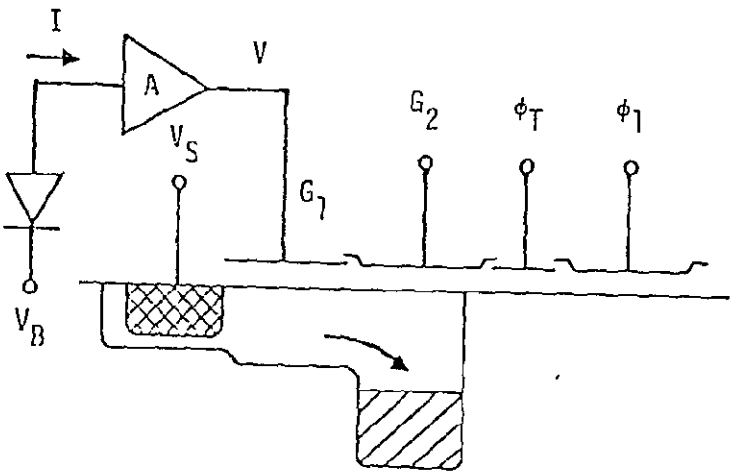


Figure 5.12 Gate Modulation Input Circuit with Buffer Amplifier

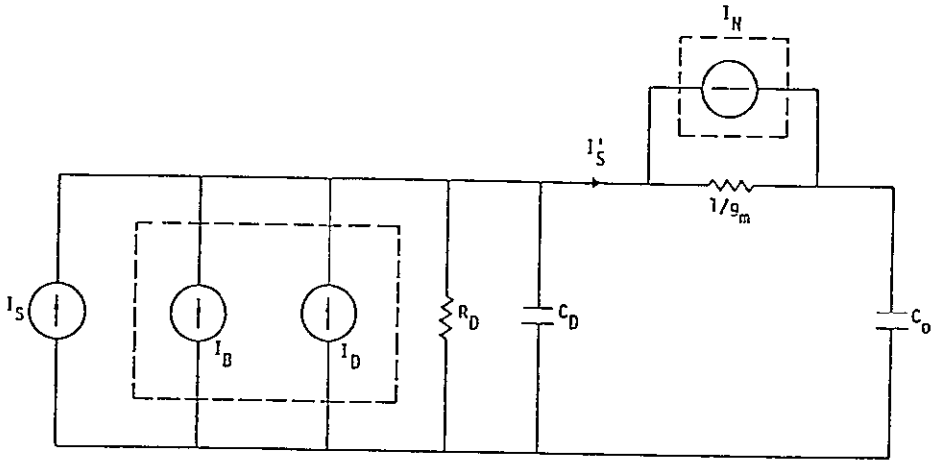


Figure 5.13 AC-Equivalent Circuit of the Direct Injection Input. (I_S is the detector signal current, I_S' is the signal current injected into the input, I_B, I_D and I_N are the noise current sources corresponding to background shot current, detector thermal noise, and input MOSFET noise including channel thermal noise and 1/f noise.)

fraction of signal current injected into the CCD channel is easily derived and is given by[42,43,44,35]

$$\eta_{INJ} = \frac{I_s'}{I_s} = \frac{g_m R_D}{1+g_m R_D}\left[\frac{1}{1 + \frac{j\omega C_D R_D}{1+g_m R_D}}\right] \tag{5.5}$$

where R_D is the detector resistance and C_D is the detector junction capacitance. At low frequencies, η_{INJ} is reduced to $g_m R_D/(1+g_m R_D)$. The injection efficiency I_s'/I_s increases monotonically as the $g_m R_D$ product increases until it is very nearly unity for $g_m R_D >> 1$. The injection efficiency rolls off at high frequencies with a time constant given by

$$RC = \frac{R_D C_D}{1+g_m R_D} \tag{5.6}$$

Note that the condition for high injection efficiency and wide bandwidths is $g_m R_D >> 1$, i.e., the detector resistance R_D and g_m, the transconductance of the CCD channel, must be high. The detector resistance R_D depends on the type of detector used, the operating temperature and the bias point of a photodiode. For most applications, these parameters are relatively fixed. The injection efficiency therefore depends primarily on the transconductance of the CCD input MOSFET. The transconductance of a MOSFET is given by

$$g_m = \frac{Z}{L}\,\mu C_{ox}\left(\frac{kT}{q}\right)\left[\left(1 + \frac{2I_s'}{\frac{Z}{L}\,\mu C_{ox}}\left(\frac{q}{kT}\right)^2\right)^{\frac{1}{2}} - 1\right] \tag{5.7}$$

where Z/L is the CCD input gate aspect ratio, μ the minority carrier, C_{ox} is the oxide capacitance per unit area and I_s' is the channel current. The small current limit such that

$$I_s' << \frac{Z\mu C_{ox}}{2L}\left(\frac{kT}{q}\right)^2 \tag{5.8}$$

is known as the subthreshold region and g_m reduces to

$$g_m = \frac{qI_s'}{kT} \tag{5.9}$$

CCDs, except at the highest backgrounds, operate in the subthreshold region, where the detector current due to background and thermally generated reverse bias currents provide the channel bias current. A plot of the injection efficiency as a function of channel bias current and g_m is shown in Figure 5.14 for two detector resistances. At low backgrounds, the detector background currents will be small ($\approx 10^{-13}$Amp for $\phi_B = 10^{10}$p/cm^{2}sec, $A_D = 10^{-4}$cm), and insufficient for high injection efficiency and wide bandwidths. The injection efficiency can be improved, of course, at low backgrounds by injecting a DC bias current to increase the g_m of the CCD input stage. However, the added bias current will introduce additional shot-noise and background limited performance can never be achieved by this technique. Increasing the Z/L ratio of the CCD input stage to increase g_m is also not effective since g_m is essentially independent of device geometry in the subthreshold region.

Another problem associated with the simple direct injection scheme is the detector to detector responsivity non-uniformity arising from the spatial variation of the gate threshold voltage. In the direct injection input shown in Figure 5.11, the bias across the photodiode is applied through gate G_1. The bias across the photodiode for a fixed gate bias V_{G1} and back-bias V_B is

$$V_{det} = V_S - V_B \approx V_{G1} - (V_T \pm \Delta V_T) - V_B \tag{5.10}$$

where $\pm \Delta V_T$ is the gate threshold variation for the input gate. The gate threshold variation ΔV_T will result in the bias on detectors on the focal plane to vary over a range of about $2\Delta V_T$. The resultant variation in bias current between detectors will cause the injection efficiency to vary from element to element.

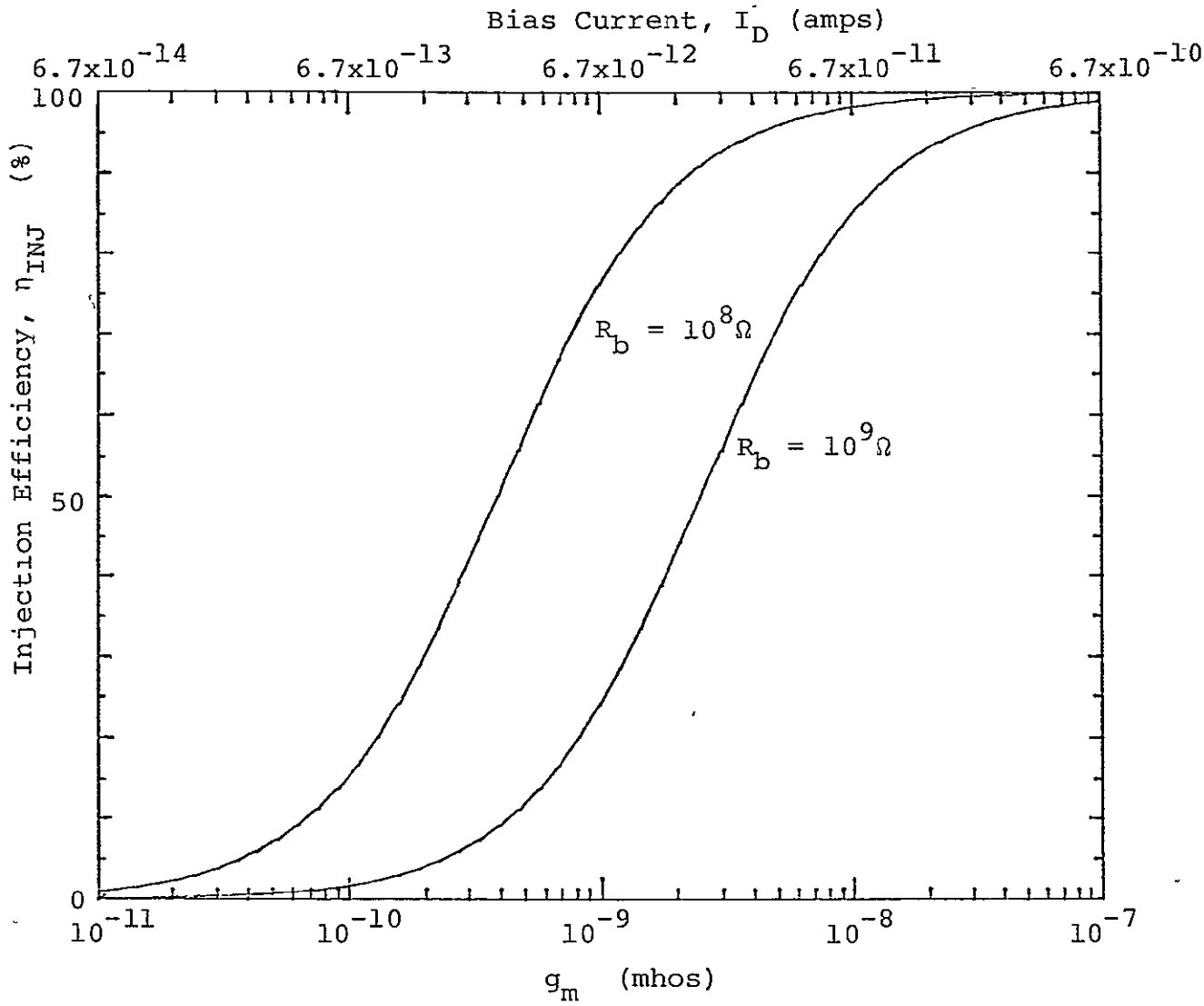


Figure 5.14 Injection Efficiency as a Function of g_m for $R_D = 10^8$ and 10^9 ohms

ORIGINAL PAGE IS
OF POOR QUALITY

Current state of the art gate threshold uniformity for commercial MOS devices is of the order of $\pm$ 150 mV. Since photodiodes are operated at or near zero bias to minimize 1/f noise, spatial variations in the gate threshold of this magnitude represent a significant problem for arrays with large numbers of photodiodes. A number of approaches to minimize the gate threshold variation problem are currently being investigated. These approaches fall into three catagories: 1) improved MOS/CCD processing for low ΔV_T; 2) improved detector reverse bias characteristics; and 3) active on-chip compensation circuits. Progress has been reported utilizing approaches 1) and 3). ΔV_T of $\pm$ 15 mV have been reported for CCD inputs fabricated utilizing special processing techniques. Several operational implementations that reduce the ΔV_Ts to the $\pm$ 5 mV range have been demonstrated, making direct injection coupling in hybrids practical. Further work, however, will be necessary to reduce the complexity of the circuits and in the long term, improved MOS/CCD processing will be the key to a satisfactory solution.

The detector signal can also be coupled to the multiplexer by modulating the channel current as shown in Figure 5.11. The CCD input MOSFET is then basically in the grounded source configuration. Because a photodiode is a high impedance current source, in order to maximize the output signal voltage, a bias resistor or a buffer amplifier with a load resistor is required for each element. Both bipolar devices, with their low gate threshold ($\pm$ 5 mV) and high current gains, and process compatible MOSFETs have been employed as buffer amplifiers. Response non-uniformity is, in general, more severe for this circuit because in addition to the inherent gate threshold variations, additional non-uniformities are added by the monolithic resistors and buffer amplifiers. For this reason, and because of the additional complexity of gate modulation, direct injection is more widely used for hybrid multiplexers.

VI. CONCLUSIONS

Focal plane array technology has progressed rapidly in the past few years, due in large part to the sizable DoD development efforts in this area.

At the present time, the monolithic extrinsic approach is the most advanced of the focal plane approaches and is the best candidate for near-term astronomical applications. As shown in Section II, considerable device maturity has been achieved, in particular for Si:In and Si:Ga arrays. Si:In and Si:Ga arrays are currently being produced and utilized on a number of DoD IR measurement programs. These arrays should become available for astronomical applications in the near future. As shown in Section 2.6, these arrays should be capable of long integration times when cooled to sufficiently low temperature

Hybrid CCD arrays represent an attractive alternative approach. Significant advances have been made both in the development of intrinsic photovoltaic detector arrays of InSb, InAsSb, PbSnTe, HgCdTe and the requisite interconnect technology. A new generation of high density CCD multiplexers, to which these arrays will be coupled, will be available in the near future. For astronomical applications where a variety of detector materials may be necessary to cover an extended spectral region, the hybrid may be the optimum and lowest cost approach.

The monolithic intrinsic approach remains a technology with long-term potential, but limited by the lack of a mature materials technology and remains the least developed of the approaches. The current NASA sponsored development effort to fabricate and develop InSb CCD technology is addressing a number of the critical materials problems. Progress, however, is expected to be slow reflecting the formidable materials and processing issues. Small two-dimensional InSb TDI arrays with a few hundred elements may become

available in a few years. Unless N_{ss} values can be significantly reduced from present values, it remains doubtful whether these arrays will be useful for astronomical applications where high detectivities are desired.

Small two-dimensional CIDs remain a competitive candidate for astronomical applications. Significant performance improvements should be realizable with cooling since the dominant noise source at 77K is the integrated dark shot noise. The CID approach, however, has limited potential for arrays larger than 32x32 because of the output capacitance limitations.

REFERENCES

1. "Shuttle Infrared Telescope Facility, Preliminary Design Study," Final Report for Contract NAS 2-8494, August 1976

2. Interim Report and Appendices, Shuttle Infrared Telescope Facility, Focal Plane Instruments and Requirements Science Team, April 14, 1978

3. N. Sclar, R. L. Maddox and R. A. Florence, "Silicon Monolithic Infrared Detector Array," Appl. Optics Vol. 16, p. 1525, June 1977

4. J. C. Fraser, D. H. Alexander, R. M. Finnila and S. C. Su, "An Extrinsic Silicon Charge Coupled Device for Detecting Infrared Radiation," International Electron Devices Meeting, Washington, D. C., Technical Digest, December 1974, p. 442

5. K. Nummedal, J. C. Fraser, S. C. Su, R. Baron and R. M. Finnila, "Extrinsic Silicon Monolithic Focal Plane Array Technology and Applications," Proc. 1975 Int. Conf. on the Application of Charge-Coupled Devices, 29-31 October 1975, p. 442

6. "Low-Cost Arrays for Detection in Infrared (LADIR)," AFAL-TR-76-70, September 1976

7. S. M. Sze, "Physics of Semiconductor Devices," Wiley Interscience, 1969, p. 30

8. P. R. Bratt, "Impurity Germanium and Silicon Infrared Detectors" in Semiconductors and Semimetals, Vol. 12, ed. by R. K. Willardson and A. C. Beer, Academic Press, 1977

9. R. D. Nelson, "Infrared Charge Transfer Devices--The Silicon Approach," Optical Eng. 16, #3, p. 275, May-June 1977

10. G. Lucovsky, "On the Photoionization of Deep Impurity Centers in Semiconductors," Solid State Commun. 3, 299 (1965)

11. R. Baron, M. H. Young, J. K. Neeland and O. J. Marsh, "A New Acceptor Level in Indium Doped Silicon," Appl. Phys. Letters, 30, 594 (1977)

12. N. Sclar, "Extrinsic Silicon Detectors for 3-5 and 8-14 μm," Infrared Phys. 16, 435 (1976)

13. N. Sclar, "Survey of Dopants in Silicon for 2-2.7 and 3-5 μm Infrared Detector Application," Infrared Phys. 17, 71 (1977)

14. N. Y. Pines and R. Baron, "Characteristics of Indium Doped Silicon Infrared Detectors," International Electron Device Meeting, Washington, D.C., Technical Digest, December, 1974, p. 446

15. R. Baron, M. H. Young, J. P. Baukus, O. J. Marsh and J. M. Sheets, "Properties of Indium-Doped Silicon as an Extrinsic Detector Material," Proc. IRSI Detector Specialty Meeting, March 22-23, 1977

16. J. P. Baukus, M. H. Young, R. Baron, M. J. Sheets and O. J. March, "Characterization of Gallium-and-Aluminum-Doped Silicon Detectors," Proc. IRIS Detector Specialty Meeting, March 22-23, 1977

17. J. E. Carnes and W. F. Kosonocky, "Noise Sources in Charge-Coupled Devices," RCA Review 33, p. 327, (1972)

18. D. M. Erb and K. Nummedal, "Buried Channel Charge Coupled Devices for Infrared Applications," Proc. of the CCD Applications Conf., San Diego, 18-20 September 1973, p. 157

19. D. Aviv, "Technology Assessment and New Opportunities," Study 203, Aerospace Report #ATR-76(7374)-2, Vol. II, Dec. 1976

20. A. J. Steckl, R. D. Nelson, B. T. French, R. A. Gudmundsen and D. Schechter, "Application of Charge-Coupled Devices to Infrared Detection and Imaging," Proc. IEEE 63, p. 67, (1975)

21. T. F. Tao, J. R. Ellis, L. Kost, and A. Coshier, "Feasibility Study of PbTe and $Pb_{0.76}Sb_{0.24}Te$ Infrared Charge Coupled Imager," Proc. CCD Applications Conf. p. 295, September 1973

22. R. D. Thom, R. E. Eck, J. D. Phillips, and J. B. Scorso, "InSb CCDs and Other MIS Devices for Infrared Applications," Proc. CCD Applications Conf., p. 31, October 1975

23. J. C. Kim, "InSb MOS Detector," Final Technical Report, Army Night Vision Laboratory Contract No. DAAK02-73-C-006, February 1975

24. D. T. Cheung, W. E. Tennant, E. E. Barrowcliff, J. P. Rode, E. R. Gertner and A. M. Andrews, "MIS Studies on Narrow Bandgap III-V Compounds," Proc. IRIS, July 1976

25. Final Report, "Further Development of an Indium Antimonide (InSb) Charge-Coupled Infrared Imaging Device (CC IRID), 20-Element Linear Imager," Contract +NAS1-14395, NASA Report #CR-145204, April 1977

26. A. M. Andrews, D. T. Cheung, E. R. Gertner and J. T. Longo, "Liquid Phase Epitaxial Growth of Stepwide-Graded $InAs_{1-x}Sb_x$-InAs Heterostructures," J. Vac. Sci. Tech.13, p. 961 (176)

27. D. T. Cheung, A. M. Andrews, E. R. Gertner, G. M. Williams, J. E. Clarke, T. G. Pasko and J. T. Longo, "Backside Illuminated $InAs_{1-x}Sb_x$-InAs Narrow-Band Photodetectors," Appl. Phys. Letters 30, p. 587 (1977)

28. R. S. Aikens, C. R. Lynds and R. E. Nelson, "Astronomical Applications of Charge Injection Devices," Proc. of the SPIE 78, Low Light Level Devices, p. 65, (1976)

29. J. C. Kim, "InSb MIS Technology and CID Devices," Proc. CCD Applications Conf., p. 1, October 1975

30. J. C. Kim, W. E. Davern and D. Colangelo, "Continued Development of Indium Antimonide CID Arrays," Final Technical Report, Naval Research Laboratory Contract N00173-76-C-0128, May 1977

31. R. S. Aikens, J. P. Brett and F. C. Gillett, "InSb CID Element Evaluation," KPNO Internal Report, Kitt Peak National Observatory, September 1977

32. P. E. Howard, J. C. Kim and J. M. Hooker, "Theoretical Analyses and Performance Projections for InSb Charge Injection Device Focal Plane Arrays," Proc. of the 1976 National IRIS Symposium, July 1976

33. J. C. Kim, "InSb Charge-Injection Device Imaging Array," IEEE Trans. Electron Devices, ED-25, p. 232 (1978)

34. A. M. Andrews, E. R. Gertner, J. E. Clarke, G. M. Williams, J. G. Pasko, J. M. Tracy, D. E. Olson and J. T. Longo, "$InAs_{1-x}Sb_x$ Diode Arrays for Hybrid Focal Planes," Proc. IRIS Detector Specialty Group Meeting, Colorado Springs, Colo., 1977

35. J. T. Longo, D. T. Cheung, A. M. Andrews, C. C. Wang and J. M. Tracy, "Infrared Focal Planes in Intrinsic Semiconductors," IEEE Trans. on Electron Devices, ED-25, p. 213 (1978)

36. J. D. Phillips, J. B. Scorso and R. D. Thom, "InSb Arrays with CCD Readout for 1.0-5.5 μm Infrared Applications," Proc. Conf. on Charge-Coupled Device Technology and Applications, Washington, D.C., December 1976

37. R. Broudy, M. Gurnee, S. Iwasa, T. Treadwell and J. White, "IR/CCD Hybrid Focal Planes," Proc., SPIE 132, Utilization of IR Detectors, Los Angeles, Calif., January 1978

C-2

38. A. M. Andrews, J. T. Longo, J. E. Clarke and E. R. Gertner, "Backside-Illuminated $Pb_{1-x}Sn_xTe$ Heterojunction Photodiodes," Appl. Phys. Letters 26, p. 428 (1975)

39. M. R. Johnson and R. A. Chapman, IRIS Specialty Group on Infrared Detectors, March 1974, p. 101

40. C. C. Wang, J. M. Tracy, M. H. Kalisher and M. D. Ewbank," PbSnTe/Si Hybrid Focal Plane Development for FLIR Applications," Proc. IRIS Detector Specialty Group Meeting, Colorado Springs, Colo., March 1977

41. A. J. Steckl, "Injection Efficiency in Hybrid IRCCDs," Proc. CCD Application Conf., San Diego, Calif., p. 85, 1977

42. R. Balcerak, P. W. Van Atta, J. T. Hall and W. Grant, "Signal Processing Interface for 3-5 μm Intermediate Temperature Photovoltaic Detectors," Proc. IRIS Detector Specialty Meeting, San Diego, Calif., 1976

43. N. Bluzer and R. Stehlik, "Buffered Direct Injection of Photocurrent into Charge-Coupled Devices," IEEE Trans. Electron Devices, ED-25, No. 2, p. 160, (1978)