NST-44

TO: XXX/Scientific & Technical Information Division
    Attn: Miss Winnie M. Morgan

FROM: GP/Office of Assistant General
      Counsel for Patent Matters

SUBJECT: Announcement of NASA-Owned U.S. Patents in STAR

In accordance with the procedures agreed upon by Code GP and Code KSI, the attached NASA-owned U.S. Patent is being forwarded for abstracting and announcement in NASA STAR.

The following information is provided:

U.S. Patent No.: 3860946

Government or Corporate Employee: Caltech/JPL

Supplementary Corporate Source (if applicable): Pasadena, CA

NASA Patent Case No.: N90-13064-1

NOTE - If this patent covers an invention made by a corporate employee of a NASA Contractor, the following is applicable:

YES ☒ NO

Pursuant to Section 305(a) of the National Aeronautics and Space Act, the name of the Administrator of NASA appears on the first page of the patent; however, the name of the actual inventor (author) appears at the heading of column No. 1 of the Specification, following the words "...with respect to an invention of ..."

Bonnie L. Henderson

Enclosure

(NASA-Case-NPO-13064-1)
SPACE-CHARGE-LIMITED SOLID-STATE TRIODE Patent (NASA) 7 p CSCL 09A

Unclas 00/33 37222
A solid-state triode is provided from a wafer of near-intrinsic semiconductor material sliced into filaments of rectangular cross section. Before slicing, emitter and collector regions are formed on the narrow sides of the filaments, and after slicing gate regions are formed in narrow strips extending longitudinally along the midsections of the wide sides of the filaments. Contacts are then formed on the emitter, collector and gate regions of each filament individually for a single filament device, or in parallel for an array of filament devices to increase load current.
**FIG. 4**

![Graph with voltage and current readings.](image)

**FIG. 5**

![Diagram with labeled parts.](image)
SPACE-CHARGE-LIMITED SOLID-STATE TRIODE

ORIGIN OF THE INVENTION

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, Public Law 85-568 (72 Stat. 435; 42 USC 2,457).

BACKGROUND OF THE INVENTION

This invention relates to a solid-state triode, and more particularly to a space-charge-limited solid-state triode.

A space-charge-limited solid-state triode (SCLT) that is similar in operation to the vacuum-tube triode is highly sought after because, having some characteristics like those of a field-effect transistor (FET), particularly a high input impedance, the SCLT has the following advantages: lower noise figure, larger power capability, higher operating temperatures, tolerant, higher radiation resistance, and higher frequency response.

A basic difference between the SCLT and the FET is that the FET operates on the ohmic current through the channel, while the SCLT operates on the space-charge current. Consequently, to achieve the SCLT in a solid-state device, and its attendant advantages, the base material must be near-intrinsic, and the base must be maintained as pure as possible throughout the fabricating steps.

A number of solid-state triodes have been devised. One of these is found described in a U.S. Pat. No. 3,056,888 to M. M Atalla. The device described therein comprises a near-intrinsic silicon wafer (n-type) which includes a high resistivity base portion. These spaced surface portions are on one surface of the wafer. Ohmic contacts are made to the two spaced surface portions to provide emitter and collector electrodes. The area between these two spaced surface portions is covered with a thin film of dielectric material. A gate electrode is then deposited on this dielectric film to provide an arrangement similar to an insulated-gate FET. The electric field produced in response to a potential applied to the gate is effective as a space-charge-limited current control means only to a shallow depth in view of the geometry. The fabrication techniques require very careful processing to establish both the depth of diffusion of the low resistivity spaced surface portions as well as their geometry and spacing. Furthermore, a dielectric film must be used to separate the gate electrode from the near-intrinsic base portion, thereby limiting high frequency response.

Another solid-state triode is disclosed in U.S. Pat. No. 3,269,533 by G. T. Wright. Several embodiments are shown using a ferroelectric crystal such as lead zirconate, or high permittivity para-electric crystal such as cadmium sulphide, zinc sulphide or the like, for the base material. Basically, the arrangement in each embodiment is one wherein the gate (control electrode) and the emitter (anode) are on one surface of the semiconductor wafer and the collector (cathode) is on the other surface of the semiconductor wafer. This places the controlling field adjacent the anode, and again makes for difficult manufacturing techniques because of the close attention that must be paid to geometry or spacing. Also, for best results the device requires insulating crystalline material for the base with a resistivity between $10^5$ and $10^6$ ohm cm. It is difficult to find materials of that resistivity to be relatively trap free.

In U.S. Pat. No. 3,250,367 to A. Rose, a solid-state triode is disclosed which comprises emitter and collector portions of a bandgap material that make abrupt blocking contacts to opposite sides of a common thin conducting layer or grid, made of a metal or a degenerate semiconductor. A thin layer of an insulator (substantially intrinsic material) is interposed between the emitter and the grid. It is difficult to obtain reliable thin insulating layers and thin grids that are transparent to injected carriers.

Jerome Kurshan discloses in U.S. Pat. No. 2,820,154 a device including a body of substantially intrinsic germanium or silicon having slots formed therein with emitter electrodes of a given conductivity type formed on the projections between the slots and a collector electrode of the same conductivity type formed on the other side of the body opposite emitter electrodes. A control electrode of opposite conductivity type is formed in the body of the intrinsic material across the bottom of each of the slots.

An improvement over that structure of Kurshan, made by the present inventor, has been reported in Electronic Design, Vol. 10, No. 6, on Mar. 14, 1968, at pages 38 and 40. That improvement consists of forming control (gate) electrodes at only the corners of the slots. To accomplish that, narrow strips of material of the opposite conductivity type are alloyed to both sides of the devices at the very bottom of the groove. The control electrodes are thus placed more in the active region between emitter and collector electrodes for a direct effect on current flow between the emitter and collector electrodes than if the control electrodes were to be placed on the bottom of the slots between the projections.

The improved device utilizes the space-charge-limited current phenomenon and is characterized by high input impedance (comparable to that of a reverse-biased p-n junction), relatively high voltage operation, and a high amplification factor. In addition, the device has a low noise figure, low susceptibility to radiation effects and low sensitivity to temperature changes. However, fabrication of the device is difficult, primarily because the control electrodes require an elaborate masking procedure to produce extremely narrow grooves (preferably not more than 1 mil wide) in the corners of the slots because the corners are, in practice, curved surfaces. The grooves are necessary to place the material selected for the control electrodes in position for proper alloying into the body of the device. What is desired is a more readily fabricable configuration for the same improved device.

SUMMARY OF THE INVENTION

In accordance with the present invention, a wafer of near-intrinsic material is prepared with broad emitter and collector regions on opposite sides. The wafer is then cut into filaments of rectangular cross section, leaving the emitter and collector regions on opposite narrow sides. Gate regions are then formed in narrow strips extending longitudinally along the midsections of the remaining opposed sides of each filament. Each filament constitutes a triode when ohmic contacts are made to the emitter and collector regions, and a common ohmic contact is made to the two gate regions. A
driver and as a mixer, as well as a general purpose ampli-
ifier with a relatively high input impedance and a high
amplification factor. It is particularly suitable for use in
hostile environments as it is relatively insensitive to the
effects of radiation.

A preferred method for forming these triodes begins
with a wafer of near-intrinsic semiconductor material
approximately 0.15 mm thick. Emitter and collector
diffusion is then accomplished on opposite faces of the
wafer with appropriate geometry for the diffusion on
one side vis-a-vis the diffusion on the other side to
allow space for ultimately providing the gate contacts.
Another method would have identical diffusions for
emitter or collector followed by an etch to remove that
diffused portion reserved for the gate contacts. The
wafer is then sliced into filaments approximately 0.06
mm wide. Masking is applied to the broad sides of each
filament, and gates are diffused. Device contacts are
finally connected, as by metallizing contact areas and
then brazing the contacts.

An alternate technique for forming the gate regions
is by alloying thin strips of suitable material into oppo-
site wide sides of the device by use of laser energy. The
sides of the filament may first be masked to receive the
strip of material to be alloyed. A focused laser beam is
then scanned along the strip with the laser spot span-
ing the strip with sufficient overlap to form a 0.06 mil
wide gate region.

In fabricating devices according to the present inven-
tion, the selected spacing (L) between the emitter and
the collector, i.e., the thickness of the starting wafer,
will depend upon the desired triode characteristic, e.g.,
higher voltage capability. Another consideration is the
diode current (I) capacity (i.e., capacity before gates
are added) given by the equation

$$I = k V^{3/2} L^3$$

where $k = 9/8 \epsilon \mu$

$A = \text{area of emitter region}$

$\epsilon = \text{dielectric constant for base material}$

$\mu = \text{mobility of injected carrier}$

$V = \text{applied voltage}$

For control of the device amplification factor, the
gates are provided with a selected distance $d_1$ from the
emitter and a selected distance $d_2$ between the gate re-
gions. Increase of $d_1$ and decrease of $d_2$ will increase the
amplification factor, although quite obviously neither can
be changed without limit. In practice, the dimen-
sions $L$ and $d_2$ are chosen and the value of $d_1$ is selected,
usually equal to approximately half of $L$, such that the
desired value of the amplification factor is obtained.

The spacing $L$ is smaller than the corresponding spac-
ing between source and drain normally used for con-
struction of FET devices, and in practice is made as
small as possible for increased current capacity. In an
FET, that spacing does not appreciably affect current
capacity and is therefore made large for convenience in
fabricating the gates.

To offset any limitation of current in devices of the
present invention resulting from an increase in the
spacing $L$, necessary for the gates, the area of the emi-
ter region can be significantly increased by starting
with a larger wafer from which the filaments are cut.

The amplification factor desired is then provided by
proper selection of the distance $d_1$ of the gate regions
from the emitter region, the last remaining variable pa-
rameter after thickness of the wafer is set and the thick-
ness for the filaments is selected. Increasing the dis-
tance $d_1$ increases the amplification factor. Decreasing
the thickness of the filaments sliced from the wafer, to
decrease the distance between the gate regions, will
also increase the amplification factor, but that distance
is, in practice, selected more from the practical consid-
7erations of slicing the filaments, leaving the selection of
the gate distance from the emitter as the final control
parameter for the amplification factor.

Other semiconductor materials, besides silicon and
germanium could be used, but these mentioned are the
most readily available in the required purity. And of
these, silicon is preferred because of its highly ad-
vanced technology, such as diffusion, and its wider
band gap. Once the base material is selected, the device
can be formed with the geometry substantially as
shown and described using all manner of techniques
known for providing the abrupt junction between the
body and the emitter, collector and gate regions.

While the device described was considered to have a
silicon body of the $n$-type (near-intrinsic $n$-type) of
semiconductor material, it can be of the $p$-type (near
intrinsic $p$-type). In that event, the emitter and collec-
tor are made $n^+$ such as by alloying or diffusing anti-
mony, and the gates are made $p^+$, such as by alloying
aluminum. If the body were germanium, then still other
choices of materials would be made as the source of im-
purities.

What is claimed is:

1. A space-charge-limited solid-state triode compris-
ing:

- a filament of semiconductor of near-intrinsic mate-
rial, said filament having a substantially rectangular
cross section,

- an emitter region of a selected type of conductivity,
said region being formed with a high concentration of
impurities distributed along one narrow side of said
filament,

- a collector region of the same type of conductivity as
said emitter region, said collector region being
formed with a high concentration of impurities distri-
buted along a narrow side of said filament oppo-
site said narrow side,

- separate ohmic contacts made to said emitter and
collector regions,

- gate regions of a conductivity type opposite said one
type, said gate regions being formed with high con-
centration of impurities distributed in narrow strips
extending longitudinally along the midsections of
both wide sides of said filament,

- ohmic contacts made to said gate regions, and

means for connecting said gate contacts together to
form a single control electrode.

2. A space-charge-limited solid-state triode as de-
defined in claim 1 having a plurality of like filament
structures, each with emitter, collector and gate regions,
said filament structures being arranged in an array with
a common contact to said emitter region of every struc-
ture, a common contact to said collector region of
every structure, and a common contact to said gate re-
gions of every structure, thereby providing a plurality of
space-charge-limited triodes in parallel for increased
current capacity.

3. A space-charge-limited solid-state triode as de-
defined in claim 2 wherein one of said emitter and collec-
tor contacts is at least as wide as said array and at least
as long as each filament to provide a supporting base
for said array, and wherein each of the remaining