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(NASA-CR-157439) ANALYSIS OF THE EFFECTS OF  
IMPURITIES IN SILICON Quarterly Report, 19  
Jan. - 30 Apr. 1979 (Solarex Corp.,  
Rockville, Md.) 36 p HC A03/MF A01 CSCI 10A

N79-24456

Unclas  
G3/44 22166

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IN SILICON

FIRST QUARTERLY REPORT

FOR PERIOD COVERING  
19 JANUARY 1979 to 30 APRIL 1979

BY

J. H. WOHLGEMUTH

JPL CONTRACT NO. 955307

SOLAREX CORPORATION  
1335 PICCARD DRIVE  
ROCKVILLE, MD 20850



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" The JPL Low - Cost Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

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## ABSTRACT

The purpose of this program is to conduct a solar cell fabrication and analysis program to determine the effects on the resultant solar cell efficiency of impurities intentionally incorporated into silicon. The program will employ "flight-quality" technologies and quality assurance to assure that variations in cell performance are due to the impurities incorporated in the silicon.

The initial program quarter was dedicated to 1) preparation of the detailed Program Plan including a detailed Quality Assurance Plan, 2) the identification and ordering of the processing equipment and materials required for handling of impure wafers, 3) the training of processing personnel to familiarize them with the process sequence and Q.A. requirements, 4) the set-up and check out of all process equipment and process parameters, 5) the development of various control log books and data sheets, and 6) processing of verification cells to serve as a data base for all experimental work. The initial verification runs have resulted in an average AM0 cell efficiency of 12.8% at 25°C (In excess of 15% AM1 at 25°C). Test runs will begin upon completion of six verification runs and JPL approval of the program plan.

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## INTRODUCTION

One of the major costs of a silicon solar cell is the cost of the high purity silicon that is used as the substrate. There has been a great deal of work done in attempting to define the silicon purity actually required to produce high efficiency solar cells. Silicon crystals with intentionally added impurities have been grown by both Westinghouse /Dow Corning<sup>1</sup> and Monsanto<sup>2</sup>. This material has been studied for impurity content and lifetime. Solar cells have been processed from this material, but most of this work has not been performed by an experienced solar cell manufacturer. This fabrication should be performed using a process sequence that has been proven in large scale production (preferably one that has application to the production of terrestrial solar cells) and with stringent quality control procedures.

The purpose of this program is to conduct a solar cell fabrication and analysis program to determine the effects on the resultant solar cell efficiency of impurities intentionally incorporated into silicon. A "flight-quality" solar cell process is to be employed with a stringent quality assurance program. The Solarex program has been formulated under the following requirements:

- 1) Assurance must be made that lots do not get misplaced. Only one lot will ever be in process at any given time. Control and test wafers will be distinguished by size.

- 2) The processes must be well controlled and documented to assure that the results are not process dependent. A cell process sequence has been selected that has been employed in large scale production. Important process parameters have been identified and an in-line Q.A. procedure developed as part of the overall Q.A. Plan.
- 3) Decontamination procedures must be incorporated to assure that the lots do not cross-contaminate each other. A cleaning procedure has been established. A monitor run will be performed before each test run to assure the cleanliness of the process equipment.
- 4) Finished cells must be subjected to sufficient measurement techniques that the mechanism of impurity effects on cell behavior can be identified. A number of measurement techniques have been chosen for use and decisions made on which technique will be performed on all cells and which will be performed on selected samples. A data base for all measurements will be established using control wafers during initial verification runs. Then test measurements will be compared to this data base.

During the first quarter the Program Plan including the detailed Quality Assurance Plan was developed and submitted to JPL for approval. Various equipment and tooling required

for handling and decontaminating the cell processing equipment was identified, ordered and installed. The personnel responsible for cell fabrication were educated in the process sequence procedures controls and required measurements. Finally, the initial verification runs using control or standard silicon were begun.

## 2. Program Description

### 2.1 Identification

During the course of the program four different types of cell lots will be processed. These cells will be identified as:

- Verification Cells - These cells will be processed during the first few weeks of the program using control silicon. These runs are designed to verify that cell processes are being performed correctly, familiarize the staff with all processes, control procedures and the Q.A. plan and finally establish a baseline for all solar cell parameters. The verification runs will employ 3-inch diameter wafers, that will be cut into 2 cm x 2 cm cells.

The verification runs are designed to acquaint the operators with the processing sequence, controls and Q.A. procedures as well as to serve as a data base for comparison of future results. To serve as a data

base a minimum number of in specification verification runs are required. This minimum number has been set at 6 such verification runs. This, however, does not mean that only 6 verification runs will be performed, since it is expected that minor variations in parameters and specifications may be necessary during the early runs. Therefore, the verification runs will be continued until 6 successful runs have been completed using identical process parameters.

- Test Cells - These are cells fabricated from the test wafers supplied by JPL containing known quantities of impurities. (At the time of processing Solarex personnel will not know the impurity content of the wafers.) The test wafers will be cut into 2 cm x 2 cm cells.
- Control Cells - These cells are co-processed with the test cells on control silicon. They are used to assure that the processing of each test lot is correct. The control runs will employ 3-inch diameter wafers, that will be cut into 2 cm x 2 cm cells.
- Monitor Cells - These cells will be processed using control silicon after the decontamination procedure has been completed. Before each test lot is run, a monitor lot will be run and the results analyzed to assure that the equipment is not contaminated. The

monitor runs will employ 3-inch diameter wafers, that will be cut into 2 cm x 2 cm cells.

## 2.2 Program Organization

The initial processing efforts will entail the use of control silicon during verification runs. The cells in each lot will be processed using the standard process sequence (see section 2.3) and then the various measurements (see section 2.6) performed on the finished cells. Upon completion of the processing and testing of all the cells in one verification lot, the results will be analyzed. If the processing has proved satisfactory and within all specifications more verification lots will be run using identical processing. If the cells are not within specification and possibly the cell performance not satisfactory, the processing sequence or parameters will be altered before continuing with the next verification run. The verification runs will be continued until six (6) identically processed, satisfactory runs have been completed. The data from these 6 runs will be used as a data base for comparing all subsequent processing.

Upon completion of the verification runs, monitor and experimental lots will be started. A monitor lot using control silicon will be processed before each experimental lot. If the monitor lot performance matches the verification lots, an experimental lot will be run using test and control silicon. At the completion of each experimental run the equipment will be decontaminated. Then the next monitor lot will be run. If

at anytime the results of a monitor lot indicates continued contamination, the decontamination procedure will be repeated and then another monitor lot processed. An experimental lot will never be run until after the successful completion of a monitor lot.

### 2.3 Process Sequence

The processing of the cells for this program must be performed by a process sequence that is:

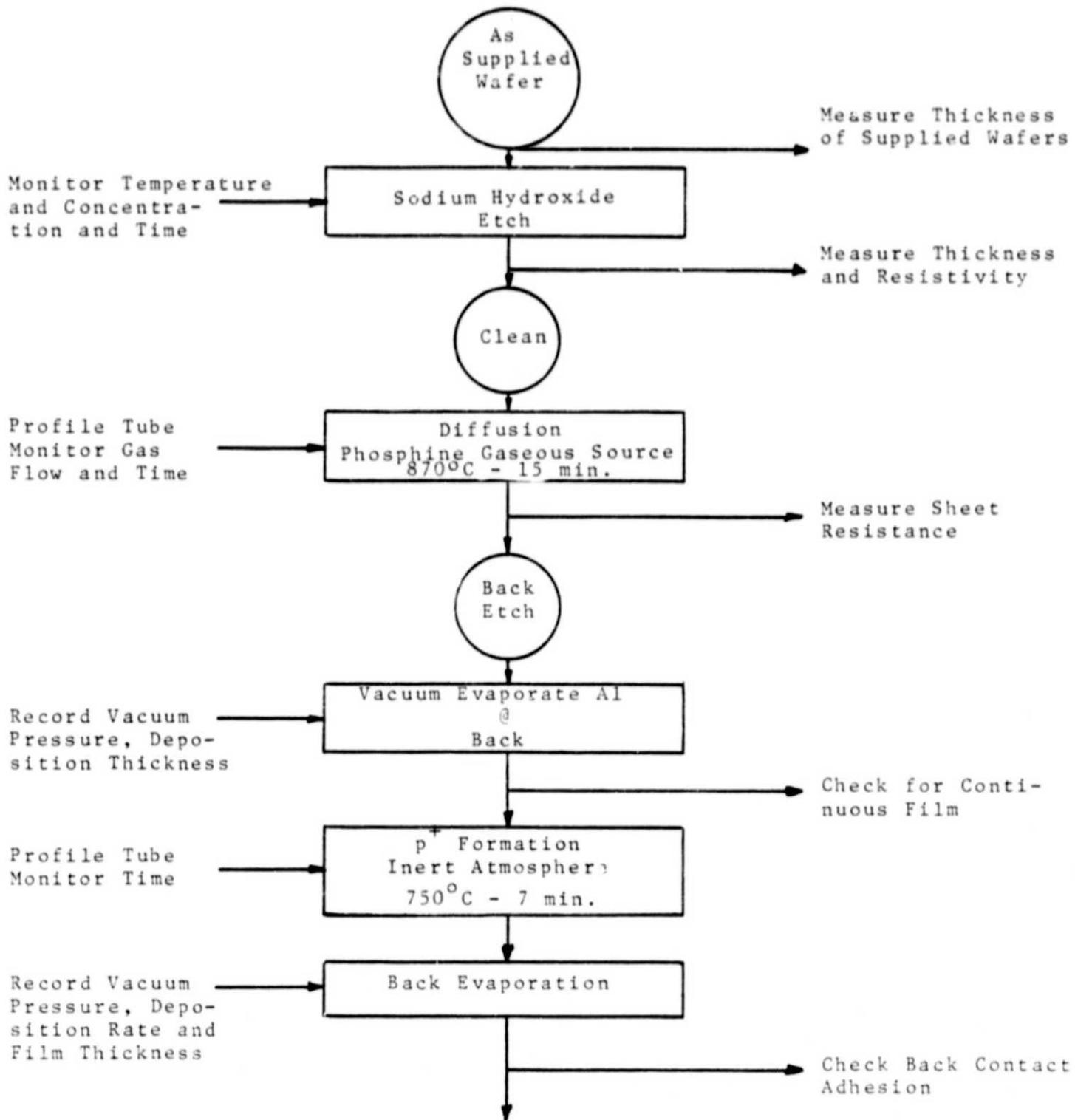
- reproducible with minimum batch-to-batch variation.
- tolerant of small (unavoidable and/or statistical) variations.
- indicative of results expected from "typical" terrestrial cell production.

Under these constraints, Solarex has chosen a process sequence as shown in the flow chart in Figure 1. This is a process sequence that has been employed for the fabrication of a large number of cells including the fabrication of thin cells for the NASA OAST pilot line, with stringent controls over the process parameter.

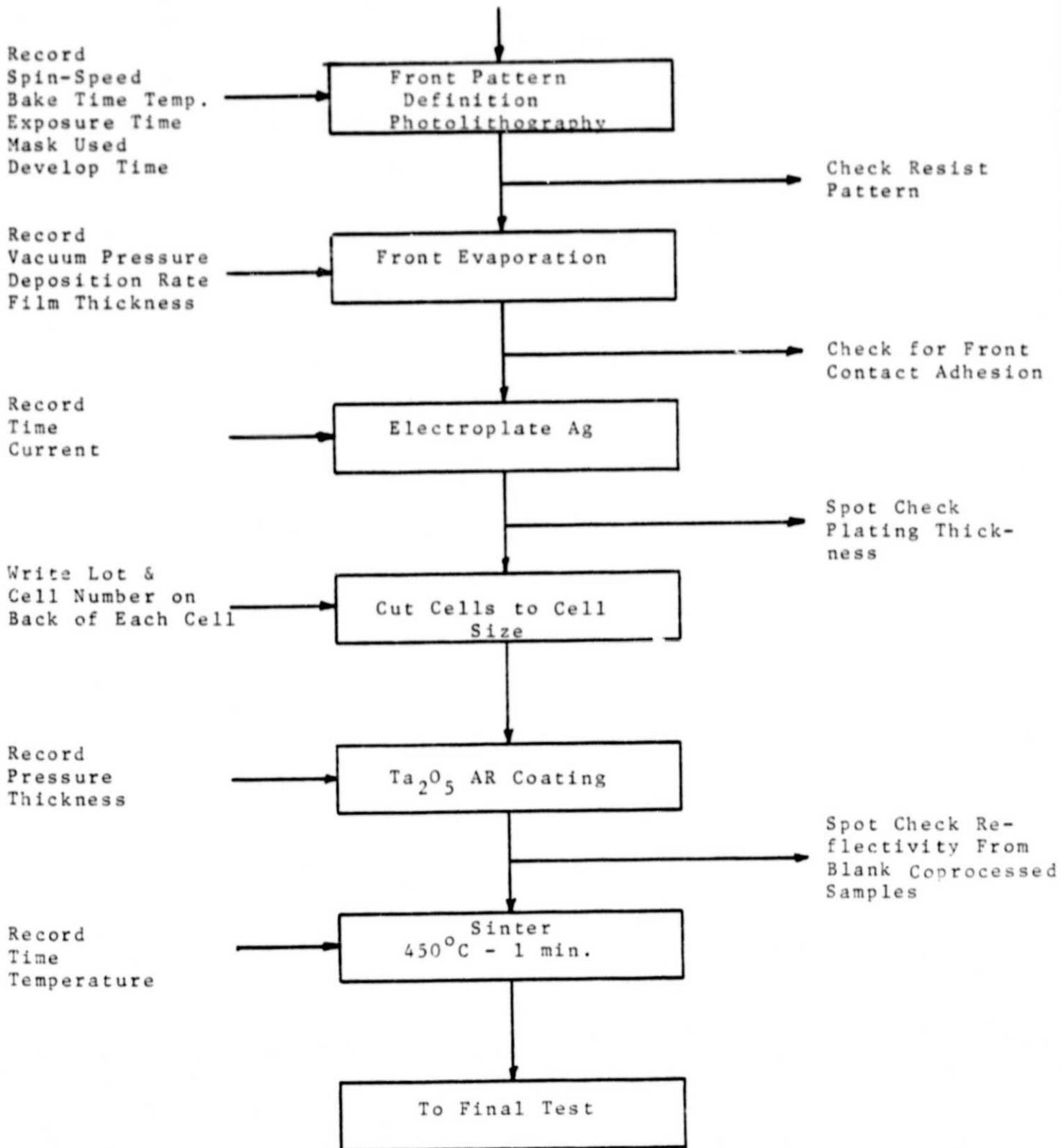
### 2.4 Decontamination Procedures

Cross-contamination of one impurity-containing group by another will be prevented by proper cleaning and checked by the use of monitor lots. After one contaminated lot has been run, the diffusion and alloy tubes and boats will be steam

FIGURE 1  
PROCESS SEQUENCE



continued on next page



cleaned by gaseous HCl while in place at elevated temperatures. Then they will be cooled, removed from the furnace and etched in HF to remove the outer layer. In addition, all etchant and cleaning baths will be changed with the containers being rinsed in deionized water. Between all steps the wafers or cells will be cleaned in deionized rinsing systems with the conductivity of the water monitored.

After the cleaning process has been accomplished, a monitor lot will be run using control silicon. No JPL impurity wafers will be run until these monitor cells have been completed and the test results show no contamination of the equipment.

## 2.5 In-Line Quality Assurance

During cell processing various quality control measurements are performed. The required in-line measurements of cell parameters are listed below.

1. Thickness measurements will be performed on etched wafers.
2. Resistivity measurements will be taken on approximately 10% of each lot after etching.
3. Each run shall have the diffused sheet resistance measured on three control wafers, choosing a cell from the center and one from each edge of the diffusion tube. The center wafer shall be measured in five locations (wafer center and four equidistant

points at a radial distance of one-inch from the wafer center).

4. Probe measurements of the sheet resistance of the front metal contacts after Ag plating shall be made for 10% of the cells in each lot. These values will be correlated by means of optical measurements of contact thicknesses on sample cells.
5. Reflectance of a control wafer (having no metal pattern) shall be measured for every test run.

In addition to these in-line cell measurements, the following shall be recorded during processing:

- temperature of NaOH bath
- etch time
- temperature profile of diffusion tube
- diffusion time
- pressure during Al evaporation
- thickness of Al film
- temperature profile of alloy tube
- alloy time
- pressure during back evaporation
- spin and speed of photoresist spin-on
- bake time during photolithography
- bake temperature during photolithography
- exposure time
- development time

- pressure during front evaporation
- silver plating time
- pressure during AR coating
- monitor frequency shift during AR coating
- sinter time
- sinter temperature

While all of these values will be measured, the rejection-acceptance criteria will be restricted to those parameters that can adversely effect final cell performance. These in-line rejection-acceptance criteria are listed below.

- 1) Raw material for verification, monitor and control wafers shall be rejected if  $\rho < 1.00$  ohm-cm or if  $\rho > 3.0$  ohm-cm.
- 2) Etched thickness of verification, monitor, control and test wafers shall be between 10 and 12 mils.
- 3) A prediffusion profile of the furnace with tube in place shall show the active diffusion zone to be  $870^{\circ}\text{C} \pm 5^{\circ}\text{C}$ . The furnace heating element controls shall be adjusted to achieve this temperature.
- 4) The diffused sheet resistance of monitor runs and verification runs shall be  $\geq 50 \Omega/\square$  and  $\leq 90 \Omega/\square$ . The diffused sheet resistance of control cells for test runs shall be  $\geq 45 \Omega/\square$  and  $\geq 95 \Omega/\square$ .
- 5) The deposited thickness of aluminum metal shall be between 6,000 and 10,000 Å. A profile of the diffusion tube made before formation of the  $p^+$  layer shall

show the active area to be  $750^{\circ}\text{C} \pm 5^{\circ}\text{C}$ . The furnace heating element controls shall be adjusted to achieve this temperature.

- 6) The deposited back contact shall be examined for adherence integrity. Areas of bubbling, delamination on bare silicon exceeding  $1/2$  sq. cm. on the wafer shall constitute rejection. If two wafers out of the run are rejectable, the run is rejected. A tape test is performed on a sample from each lot with metal lift-off constituting rejection of the lot. Rejected runs may have the contact metal removed and a fresh contact metal deposited. This must be recorded on the lot follower, the QC log and brought to the attention of the program manager.
- 7) The photolithography inspection shall verify that the front metal contact pattern is free of resist areas and that the line width is correct to  $\pm 25\%$ .
- 8) The front contact pattern shall be inspected for severance, bubbling and delamination and a sample tape tested. If the major buss bars are severed (near the contact pads) or if a large number ( $>15$ ) of the "fingers" are severed or missing, the cell is a reject. If three or more test cells are rejected or if less than ten control cells are accepted, or if the sample fails the tape test the run is rejected.

- 9) Plating thickness shall be a minimum of six microns. This will be measured by means of both a four point probe measurement and correlated with an optical measurement of the plating thickness. Either 10% of each lot or a minimum of 3 cells shall be measured. If any of these cells are underplated, the whole lot shall be checked and all underplated cells returned to the plating tank until the minimum acceptable thickness is reached.

## 2.6 Testing

Every finished cell including all test, control, monitor and verification runs would be measured to yield the following data taken at AMO and 25°C (standardized using a flight calibrated cell from NASA;Lewis):

- I-V curve
- $I_{sc}$
- $I_{sc}$  blue with Corning Filter #9788
- $I_{sc}$  red with Corning Filter #2408
- $V_{oc}$
- $P_{max}$
- $I_{mp}$
- $V_{mp}$

The following measurements will be performed on a sample basis, typically on at least one control cell and on one average performance test cell.

- reflections versus wavelength to assure proper AR coatings and to factor the reflectivity dependence out

of the spectral response data. A value for the absorption and the wavelength of minimum reflectance will be reported.

- quantum yield measurements
- dark I-V curve
- $I_{sc}$  vs  $V_{oc}$  curve
- junction capacitance
- junction conductance
- series resistance
- diode factor  $n$  from  $I_{sc}$  vs  $V_{oc}$
- $I_0$  from  $I_{sc}$  vs  $V_{oc}$

## 2.7 Analysis

The analysis will be performed using the cell measurements described above. The average with standard deviation of various parameters will be plotted as a function of impurity concentration. In order to understand the actual loss mechanisms, comparisons will be made on a large number of parameters including:

- |   |                     |
|---|---------------------|
| • $P_{max}$   | • $I_{sc}$ red      |
| • $I_{sc}$  | • $I_{sc}$ blue     |
| • $I_{mp}$  | • $I_{sc} - I_{mp}$ |
| • $V_{mp}$  | • $V_{oc} - V_{mp}$ |
| • $V_{oc}$  | • $n$               |
| • Collection efficiency<br>as a function of<br>wavelength | • $I_0$ .           |

These measurements will be performed to the degree necessary to understand the mechanisms at work in the cells. This means obtaining enough information to ascertain what fraction of degradation in output power is due to:

- loss in short circuit current due to bulk degradation
- loss in open-circuit voltage due to junction degradation (n factor)
- loss in fill factor due to shunting by the impurities or due to an increase in  $I_0$
- loss in fill factor due to series resistance.

These measurements will be of vital importance in the analysis of exactly how each impurity degrades cell performance.

### 3.0 Progress and Results

The initial program efforts entailed the identification and procurement of special handling supplies and materials required to prevent cross-contamination. This equipment was set-up, personnel trained in its use and familiarized with the Program Plan and Quality Assurance Plan and various process parameters determined. Various log and data sheets were created to aid in the identification of lots, the performance and recording of processing steps and the recording of all test measurements. Upon completion of this set-up and training period, verification runs were begun.

The initial verification runs were fabricated using a diffusion temperature of 860°C. These wafers had a sheet resistance on the high end of the acceptable level and somewhat low output power (65mW for a 2 x 2 cell at AM0 and 25°C). We did not wish to use a process sequence that results in any accept-reject parameters being uncomfortably close to the reject limit. Therefore, as of verification run 4 the diffusion temperature was raised to 870°C. All subsequent runs have been performed using this temperature and have yielded satisfactory results.

Appendix A summarizes the AM0 I-V measurements made on Verification Lots 4, 5, 6, and 7. The average efficiency of these cells is 12.8% (AM0 at 25°C), which translates to greater than 15% (AM1 at 25°C). Table #1 summarizes the results of I-V measurements on these 4 verification runs. The values show good consistence within each run and from run to run.

TABLE I

## SUMMARY OF VERIFICATION RUNS V-4, V-5, V-6

Lots	I <sub>SC</sub> (mA)	V <sub>OC</sub> (mV)	P <sub>max</sub> (mW)	I <sub>mp</sub> (mA)	V <sub>mp</sub> (mV)	I <sub>SC</sub> Blue (mA)	I <sub>SC</sub> Red (mA)	Fill Factor (%)
V-4 AVG.	148.9	595.7	69.0	139.1	496.0	39.9	82.5	
σ	1.72	1.95	2.00	3.44	7.43	1.57	1.30	77.8
Coef. Var.	.012	.003	.029	.025	.015	.039	.016	
V-5 AVG.	149.1	595.5	68.9	138.8	496.1	39.2	83.3	
σ	1.46	1.28	2.38	4.58	10.85	1.12	0.93	77.6
Coef. Var.	.010	.002	.035	.033	.022	.029	.011	
V-6 AVG.	152.4	597.7	71.1	143.1	497.6	40.7	83.2	
σ	1.10	1.53	1.34	2.41	5.10	1.34	0.99	78.2
Coef. Var.	.007	.003	.019	.017	.010	.033	.012	
V-7 AVG.	149.3	595.7	69.6	140.0	496.9	37.6	84.7	
σ	1.70	2.06	1.33	2.67	4.83	1.39	1.06	78.2
Coef. Var.	.011	.003	.019	.019	.010	.037	.013	
AVG. VALUE (V-4, -5, -6, -7)	149.9	596.2	69.7	140.3	496.7	39.4	83.4	78.0

The other measurements that are made on a sample basis are summarized in Table 2. As can be seen, these values are also in general consistent. However, variations in conductance and shunt resistance especially for the sample cell from V-5 indicate that it will be necessary to measure more than one sample cell to obtain a good estimate of an average or typical shunt value for a specific lot.

TABLE 2

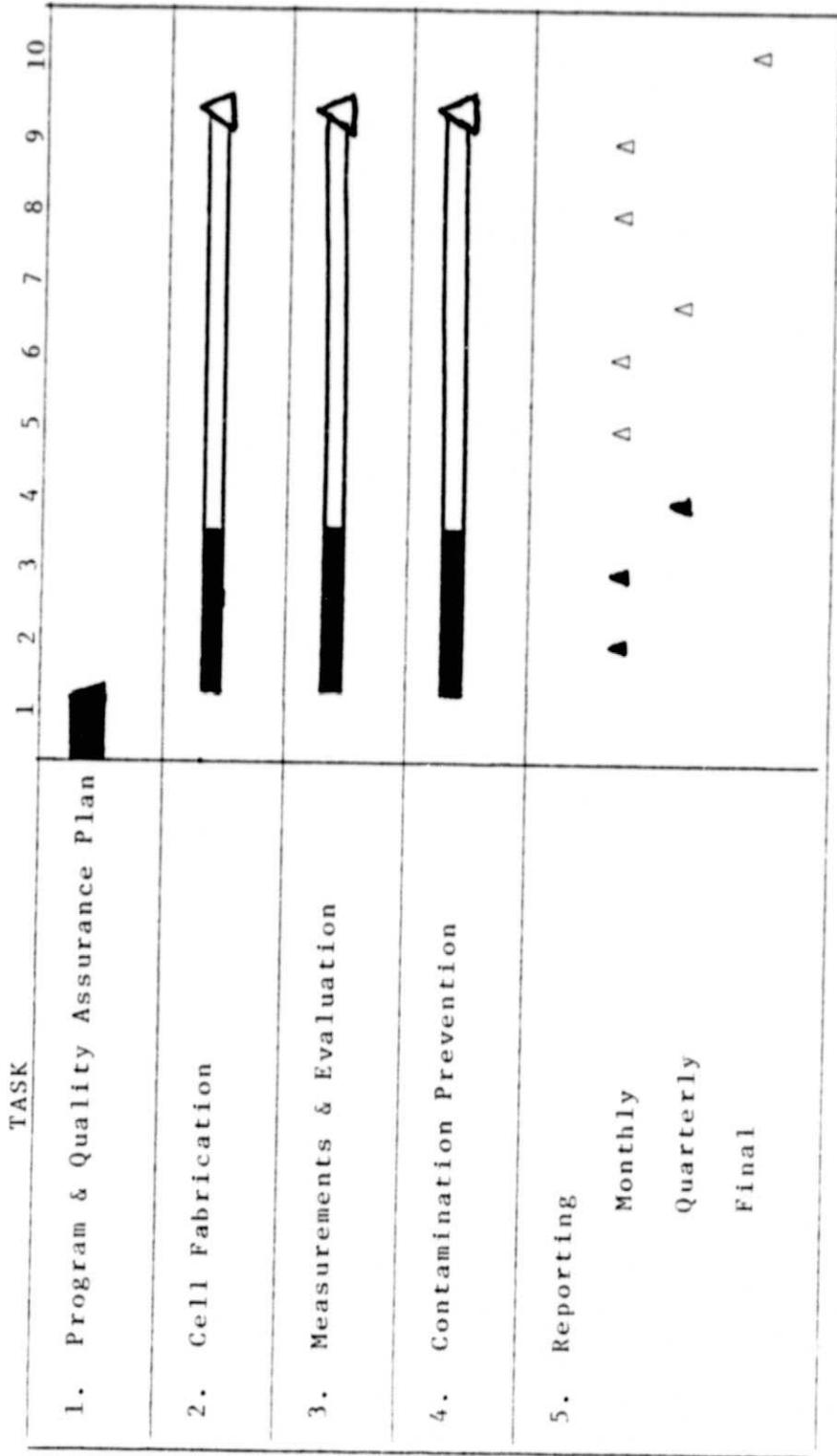
Lot No.	$P_{\max}$	Absorption Efficiency $\alpha$ in %	Quantum Yield % at max $\lambda$ max ( $\mu$ )	Carriers Collected per absorbed photon	Junc. Cap $\mu\text{f}$	Junc. Cond. $\text{m}\Omega$	$R_{\text{series}}$ $\Omega$	$R_{\text{shunt}}$ $\text{K}\Omega$	Diode Factor $n$	$I_0$ $\text{MA}$
4	69.0	.91	.6	.82	.115	.03	.0741	50.8	1.02	$3 \cdot 10^{-8}$
5	68.9	.91	.6	.83	.112	2.96	.041	0.345	1.05	$3 \cdot 10^{-8}$
6	71.1	.91	.6	.83	.116	.24	.061	4.71	1.05	$3 \cdot 10^{-8}$
7	69.6	.91	.6	.84	.093	.29	.0893	11.6	1.02	$3 \cdot 10^{-8}$

#### 4.0 Planned Activities

During the coming months the verification runs will be completed and then the monitor and test lots begun. Once the results of JPL supplied test cells have been obtained, the analysis phase of the program will begin. At this time the schedule calls for running 45 different impurity lots and performing the decontamination procedure after each experimental lot. An update program milestone chart is included as Figure 2.

FIGURE 2 . PROGRAM PLAN

MILESTONE CHART



## REFERENCES

1. R. H. Hopkins, et al, "Silicon Materials Task of the Low Cost Solar Array Project (Part 2), 9th Quarterly Reports. ERDA/JPL-954331-78/1, 1978.
2. H. W. Gutsche and D. E. Hill, "Determination of a Definition of Solar Grade Silicon", Final Report, No. ERDA/JPL-954338-76.

Appendix A

Verification Lot Results

Cell #	$I_{sc}$ (mA)	$V_{oc}$ (mV)	$P_n$ (mW)	$I_{mp}$ (mA)	$V_{mp}$ (mV)	$I_{sc\ blue}$ (mA)	$I_{sc\ red}$ (mA)
1	148	595	69	141	490	41	81
2	149	595	70	140	500	41	81
3	151	596	72	144	500	41	82
4	148	595	69	139	495	40	81
5	150	595	68	138	495	41	82
6	147	595	71	143	495	41	83
7	144	594	66	133	495	39	80
8	148	595	70	140	500	40	82
9	149	595	69	140	495	41	81
10	148	596	69	138	500	40	81
11	149	596	70	142	495	40	83
12	149	594	70	143	490	40	83
13	151	597	69	140	495	41	84
14	148	595	68	137	470	40	82
15	151	597	72	137	480	41	83
16	151	597	66	135	490	40	84
17	147	598	70	142	495	42	83
18	147	590	64	130	490	37	83
19	150	593	68	138	495	40	82
20	151	596	71	142	500	40	83
21	151	599	72	140	510	41	83
22	151	598	66	138	498	42	81
23	150	597	71	144	500	42	81
24	152	599	71	142	500	42	83
25	147	593	68	141	498	36	84
26	149	593	69	139	500	37	86
27	147	595	68	140	510	38	83
28	148	595	70	141	498	37	84



Cell #	$I_{sc}$ (mA)	$V_{oc}$ (mV)	$P_m$ (mW)	$I_{mp}$ (mA)	$V_{mp}$ (mV)	$I_{sc\ blue}$ (mA)	$I_{sc\ red}$ (mA)
1	149	596	70	141	500	40	84
2	150	597	70	140	500	42	82
3	149	596	69	137	505	41	82
4	148	596	70	140	500	39	83
5	149	596	69	139	500	40	84
6	148	596	70	134	490	39	83
7	149	596	69	140	490	39	83
8	150	596	70	140	500	40	84
9	149	596	67	148	438	38	82
10			R E J E C T				
11	148	592	60	122	495	38	83
12			R E J E C T				
13	147	593	63	128	495	38	83
14	148	595	69	139	500	38	84
15	149	595	68	138	495	39	84
16	149	595	70	141	495	38	85
17	148	594	70	140	500	38	84
18	148	595	68	139	490	38	84
19	144	595	67	135	495	38	81
20	148	595	64	130	490	38	84
21	151	595	69	139	495	41	83
22	152	597	71	144	495	41	84
23	150	597	70	141	495	40	84
24	150	596	70	140	500	39	84
25	151	596	71	143	495	41	84
26	149	596	70	140	500	38	83
27	150	597	71	141	505	40	83
28	151	592	69	142	490	38	85



Cell #	$I_{sc}$ (mA)	$V_{oc}$ (mV)	$P_m$ (mW)	$I_{mp}$ (mA)	$V_{mp}$ (mV)	$I_{sc\ blue}$ (mA)	$I_{sc\ red}$ (mA)
1	153	597	69	139	495	43	82
2	154	599	72	147	490	41	83
3	153	599	72	144	500	41	84
4	152	599	70	142	490	40	84
5	154	598	71	144	495	41	84
6	152	599	70	140	500	43	81
7	154	596	70	144	485	43	82
8	152	600	72	144	500	42	82
9	153	599	70	140	500	43	82
10	153	598	72	143	505	42	83
11	153	598	71	145	490	41	83
12	153	598	72	144	495	41	83
13	153	598	72	145	495	40	84
14	151	598	71	144	495	41	83
15	152	597	72	145	495	40	84
16		B R O K E N					
17	151	597	72	143	500	41	83
18		B R O K E N					
19	153	597	72	145	495	41	83
20	153	592	71	145	490	43	82
21	152	597	71	142	500	40	84
22	153	599	73	145	500	39	85
23	152	599	72	143	505	39	84
24	152	599	69	140	495	40	84
25	153	599	70	143	490	41	84
26	153	597	72	144	500	39	85
27	154	598	73	145	500	41	85



Cell #	$I_{sc}$ (mA)	$V_{oc}$ (mV)	$P_n$ (mW)	$I_{mp}$ (mA)	$V_{mp}$ (mV)	$I_{sc}$ blue (mA)	$I_{sc}$ red (mA)
1	150	595	71	140	505	39	85
2	150	597	70	140	500	38	86
3	149	598	71	140	505	38	84
4	149	597	67	141	490	37	85
5	149	598	70	142	495	38	84
6	150	597	68	137	495	37	86
7	151	597	68	138	490	39	84
8	152	598	71	143	495	39	86
9	148	598	70	140	500	39	83
10	148	597	69	140	495	40	82
11	151	597	71	141	505	39	85
12	149	597	70	143	490	38	85
13	148	595	70	140	500	36	85
14	147	595	70	140	500	36	84
15	148	595	69	140	490	36	85
16	146	593	66	134	490	36	84
17	146	594	68	138	495	35	85
18		BROKEN					
19	147	594	69	132	500	36	85
20	149	596	70	140	500	37	85
21	150	597	71	143	500	39	84
22	149	596	70	140	500	38	84
23		BROKEN					
24	151	596	70	140	500	39	85
25		BROKEN					
26	150	597	70	140	500	38	84
27	150	592	70	141	495	38	86
28	153	595	72	145	495	39	86
				30			

