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ELECTRICAL CHARACTERIZATION OF HUGHES HCMP 1852D AND RCA CDP1852D 8-BIT, CMOS, I/O PORTS

JUNE 1979

(NASA-CR-162159) ELECTRICAL CHARACTERIZATION OF HUGHES HCMP 1852D AND RCA CDP1852D 8-BIT, CMOS, I/O PORTS Final Report (Hughes Aircraft Co.) 48 p

HC A03/MP A01

CSCL 09B G3/60 31900

AEROSPACE GROUPS

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA
ELECTRICAL CHARACTERIZATION OF
HUGHES HCMP 1852D and RCA CDP1852D
8-BIT, CMOS, I/O PORTS

FINAL REPORT
June 1979

Contract Number JPL 954789, Modification 1

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TEST ABSTRACT

Twenty-five Hughes HCMP 1852D and 25 RCA CDP1852D 8-bit, CMOS, I/O-port microcircuits were subjected to electrical characterization tests. All electrical measurements were performed on a Tektronix S-3260 Test System at the Hughes Aircraft Company Technology Support Division in Culver City, California. Before electrical testing, the devices were subjected to a 168-hour burn-in at 125°C with the inputs biased at 10V. The burn-in was performed at the JPL facilities in Pasadena, California.

Four of the Hughes parts became inoperable during testing. They exhibited functional failures and out-of-range parametric measurements after a few runs of the test program.
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1.0 INTRODUCTION

This report documents the results of electrical characterization tests performed to determine the electrical performance characteristics of 25 RCA CDP1852D and 25 Hughes HCMPS 1852D CMOS integrated circuits. The performance characteristics were measured under various electrical conditions at five temperatures. The data was analyzed and tabulated to show the effect of operating conditions on performance and to indicate parameter deviations among the devices in each group. This information can be used in evaluating typical device performance and in determining specification limits. Accuracy was given precedence over time-efficiency where practical, and tests were designed to measure worst-case performance.

The tests were divided into three categories: functional, AC parametric, and DC parametric. The functional tests were performed on a pass/fail basis to verify that the device under test (DUT) was logically correct. All voltage and timing conditions (except supply voltage) were set to nominal values to distinguish between functional failures and statistically unusual devices. The AC parametric tests consisted of propagation delays, transition times, setup times, hold times, and pulse widths. These were measured either by a one-shot technique or by a moving-strobe method, depending on the nature of the measured parameter. The DC parametric tests were simple static measurements made by forcing specified conditions on the DUT and measuring a voltage or current.

All of these tests were performed under computer program control on a Tektronix S-3260 Automated Test System. All devices were subjected to the full set of tests at ambient temperatures of -55°C, -20°C, 25°C, 85°C, and 125°C. The temperature environment was provided by a Temptronic thermal airstream unit (TP450A) under program control.
Twenty-five devices from each manufacturer (RCA and Hughes) were tested. The data was tabulated and analyzed separately for each lot. There were no functional failures or significantly deviant devices in the RCA lot. In the Hughes lot, four devices failed the functional tests and yielded out-of-range or abnormal parametric values. These failures are discussed in detail in Section 4.0.
2.0 DEVICE DESCRIPTION

The RCA CLP1852D and Hughes HCMY 1852D are 8-bit, mode-programmable, parallel input/output ports for use in 1800-series microprocessor systems. They are capable of interfacing directly with the 1802 microprocessor without additional components. They use static silicon-gate CMOS circuitry and are compatible with 4000-series microcircuits. They are supplied in 24-lead, hermetic, dual-in-line, ceramic packages.

A brief functional description of the 1852 device is given in Paragraph 2.2. Pin connections are shown in Figure 1, and a functional diagram appears in Figure 2.

```
<table>
<thead>
<tr>
<th>CS1</th>
<th>1</th>
<th>24</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODE</td>
<td>2</td>
<td>23</td>
<td>SR</td>
</tr>
<tr>
<td>D10</td>
<td>3</td>
<td>22</td>
<td>D17</td>
</tr>
<tr>
<td>D00</td>
<td>4</td>
<td>21</td>
<td>D07</td>
</tr>
<tr>
<td>D11</td>
<td>5</td>
<td>20</td>
<td>D16</td>
</tr>
<tr>
<td>D01</td>
<td>6</td>
<td>19</td>
<td>D06</td>
</tr>
<tr>
<td>D12</td>
<td>7</td>
<td>18</td>
<td>D15</td>
</tr>
<tr>
<td>D02</td>
<td>8</td>
<td>17</td>
<td>D05</td>
</tr>
<tr>
<td>D13</td>
<td>9</td>
<td>16</td>
<td>D14</td>
</tr>
<tr>
<td>D03</td>
<td>10</td>
<td>15</td>
<td>D04</td>
</tr>
<tr>
<td>CLOCK</td>
<td>11</td>
<td>14</td>
<td>CLEAR</td>
</tr>
<tr>
<td>VSS</td>
<td>12</td>
<td>13</td>
<td>CS2</td>
</tr>
</tbody>
</table>
```

Figure 1. 1852 Pin Connections.
2.1 PIN DESCRIPTIONS

2.1.1 Mode Control Input (Mode)

The mode control input programs the device as an input port (MODE = 0) or an output port (MODE = 1).

2.1.2 Clock Input

The clock input enters data into the data register (see Figure 2) and affects the SR output.

2.1.3 Chip Select Inputs (CS1, CS2)

The chip select inputs enable or disable the tristate data outputs and affect the SR output and entry of data into the register.

2.1.4 Clear Input

The clear input clears the data register and resets the SR output.
2.1.5 **Data Inputs (DI0 through DI7)**

The data inputs provide the eight bits of data for the register.

2.1.6 **Data Outputs (DO0 through DO7)**

The data outputs are three-state (logic "1", logic "0", high-impedance) output drivers.

2.1.7 **Service Request Output (SR)**

The service request output provides the signal to the processor or output device. The output provides positive logic in the output mode and negative logic in the input mode.

2.2 **OPERATION**

2.2.1 **Operation as Input Port**

The data at the inputs is strobed into the data register when the clock pin is high (logic "1"). The data outputs are enabled when both chip selects are high (CS1 CS2 = 1). The service request output is set (SR = 0) by negative (high-to-low) transition of CLOCK. The service request output is reset (SR = 1) by negative transition of CS1, CS2 or negative transition of CLEAR. The data register is cleared (set to logic "0") when CLEAR = CLOCK = 0.

2.2.2 **Operation as Output Port**

The data is strobed into the register when CS1 CS2 CLOCK = 1. Data outputs are enabled at all times. The service request is set (SR = 1) by the negative transition of CS1, CS2. The service request is reset (SR = 0) by the negative transition of CLOCK or the negative transition of CLEAR. The data register is cleared when CLEAR = CLOCK = 0.
3.0 DESCRIPTION OF TESTS

Testing any parameter of an 1852 device involves applying stimuli to the device and observing its response. The details of these two actions define the specific test or measurement. Microcircuit tests can be divided into functional tests, AC parametric tests, and DC parametric tests. The following are brief explanations of the methods used with the Tektronix S-3260 to perform these tests.

3.1 FUNCTIONAL TESTS

Functional tests are performed on a pass/fail basis using a pattern of logical "1"s and "0"s. The pattern defines a series of stimuli to be presented at the DUT inputs and a series of results to be expected at the outputs. The input levels are provided by drivers whose voltage levels can be programmed individually for each input and whose state (1, 0, or inhibited) is controlled by the pattern. The expected DUT output levels are checked by comparators which are also individually programmable and under pattern control. The comparators are strobed so that the output is sampled only during a specific time interval. An error is detected under the following conditions:

1. During comparison for a 1, if the DUT output is less than the logic "1" compare level at any time during the compare window
2. During comparison for a 0, if the DUT output is greater than the logic "0" compare level at any time during the compare window (see Figure 3).

The placement and width of the compare window and the frequency at which the pattern is run are under program control.
The functional tests were performed using the pattern shown in Table 1. The test conditions are shown in Table 2.

3.2 AC Parametric Tests

AC parametric tests performed on the 1852 device include propagation delays, transition times, and input timing tests. The propagation delays were measured using a one-shot (real time) technique which makes a direct measurement of the time between two transitions. The trigger levels at which the measurement clock starts and stops are determined by comparator settings and are programmable.

Transition times are measured indirectly. Propagation delays are measured to the output-under-test at two trigger levels (usually 10 percent and 90 percent of output swing). The difference between the two delays is the transition time between the two levels.

Input timing is controlled on the S3260 by a number of programmable clock phases. An input may be programmed to assume one level (determined by the pattern ...rivers) for an entire clock cycle or to appear as a pulse within the cycle. The start time and duration of this pulse are programmable, and several inputs can be pulsed differently within a clock cycle. This allows input timing conditions to be varied over a wide range so that their effect on device performance may be determined. Minimum timing conditions for proper device operation, such as set up and hold times, are measured by moving the pulse edges relative to one another while repeatedly running a functional test pattern (see Paragraph 3, 1). If the parameter of interest is varied from a failing condition (for example, very short setup time) to a passing condition, the value at which the device first functions properly is the minimum. To ensure isolation of the parameter under test, the other timing conditions are greatly relaxed.

The following AC parameters were measured at VDD voltages of 5V and 10V (refer to Table 3 for test conditions):

Input Mode Propagation Delays
1. Clear to data outputs (TCLR, Figure 3)
2. Chip select to output on, low (TCAO, Figure 4)
(Table 1, continued)

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin</th>
<th>Time Slot</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60</td>
</tr>
<tr>
<td>CS1/CSI</td>
<td>1</td>
<td>1 1 1 1 1 0 0 0 0 0 1 0 1 1 1 0 0 0 0 0 0 0 0 1</td>
</tr>
<tr>
<td>CS2</td>
<td>13</td>
<td>1 1 1 1 1 0 0 0 0 0 0 0 1 0 1 1 1 0 0 0 0 0 1 1 0</td>
</tr>
<tr>
<td>MODE</td>
<td>2</td>
<td>0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>CLOCK</td>
<td>11</td>
<td>1 1 1 1 0 1 0 0 0 0 0 0 0 0 1 0 0 1 0 0 1 0 0 0 0 1 1 0</td>
</tr>
<tr>
<td>CLEAR</td>
<td>14</td>
<td>1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>Inputs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DI 0</td>
<td>3</td>
<td>0 0 1 1 0 1 1</td>
</tr>
<tr>
<td>DI 2</td>
<td>5</td>
<td>0 1 0 1 0 1 1</td>
</tr>
<tr>
<td>DI 3</td>
<td>9</td>
<td>0 0 0 1 0 1 1</td>
</tr>
<tr>
<td>DI 4</td>
<td>16</td>
<td>0 0 0 1 0 1 1</td>
</tr>
<tr>
<td>DI 5</td>
<td>18</td>
<td>0 0 0 1 0 1 1</td>
</tr>
<tr>
<td>DI 6</td>
<td>20</td>
<td>0 0 0 1 0 1 1</td>
</tr>
<tr>
<td>DI 7</td>
<td>22</td>
<td>0 0 0 1 0 1 1</td>
</tr>
<tr>
<td>Outputs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DO 0</td>
<td>4</td>
<td>0 0 1 1 X X 0 1 1 1</td>
</tr>
<tr>
<td>DO 1</td>
<td>6</td>
<td>0 1 0 1 X X 0 1 0 0</td>
</tr>
<tr>
<td>DO 2</td>
<td>8</td>
<td>1 0 0 1 X X 0 1 1 1</td>
</tr>
<tr>
<td>DO 3</td>
<td>10</td>
<td>0 0 0 1 X X 0 1 0 0</td>
</tr>
<tr>
<td>DO 4</td>
<td>15</td>
<td>0 0 0 1 X X 0 1 1 1</td>
</tr>
<tr>
<td>DO 5</td>
<td>17</td>
<td>0 0 0 1 X X 0 1 0 0</td>
</tr>
<tr>
<td>DO 6</td>
<td>19</td>
<td>0 0 0 1 X X 0 1 1 1</td>
</tr>
<tr>
<td>DO 7</td>
<td>21</td>
<td>0 0 0 1 X X 0 1 0 0</td>
</tr>
<tr>
<td>SR/SR</td>
<td>23</td>
<td>0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1</td>
</tr>
</tbody>
</table>
### TABLE 2. FUNCTIONAL TEST CONDITIONS

<table>
<thead>
<tr>
<th>Condition</th>
<th>At 3V</th>
<th>At 15V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drivers, High (Logic &quot;1&quot;)</td>
<td>3V</td>
<td>15V</td>
</tr>
<tr>
<td>Drivers, Low (Logic &quot;0&quot;)</td>
<td>0V</td>
<td>0V</td>
</tr>
<tr>
<td>Comparators, High</td>
<td>1.5V</td>
<td>7.5V</td>
</tr>
<tr>
<td>Comparators, Low</td>
<td>1.5V</td>
<td>7.5V</td>
</tr>
<tr>
<td>Cycle Time, (Period)</td>
<td>16µs</td>
<td>16µs</td>
</tr>
<tr>
<td>Compare Window: Start</td>
<td>15.95µs</td>
<td>15.95µs</td>
</tr>
<tr>
<td>Duration</td>
<td>8ns</td>
<td>8ns</td>
</tr>
</tbody>
</table>

### TABLE 3. AC-PARAMETRIC TEST CONDITIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>At VDD = 5V</th>
<th>At VDD = 10V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drivers, High</td>
<td>5V</td>
<td>10V</td>
</tr>
<tr>
<td>Drivers, Low</td>
<td>0V</td>
<td>0V</td>
</tr>
<tr>
<td>Comparators:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delays to On/Off:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>3.75V</td>
<td>7.5V</td>
</tr>
<tr>
<td>Low</td>
<td>1.25V</td>
<td>2.5V</td>
</tr>
<tr>
<td>Other Delays:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>2.5V</td>
<td>5V</td>
</tr>
<tr>
<td>Low</td>
<td>2.5V</td>
<td>5V</td>
</tr>
<tr>
<td>Input Timing:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>2.5V</td>
<td>5V</td>
</tr>
<tr>
<td>Low</td>
<td>2.5V</td>
<td>5V</td>
</tr>
<tr>
<td>Transition Time:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>4.5V</td>
<td>9V</td>
</tr>
<tr>
<td>Low</td>
<td>0.5V</td>
<td>1V</td>
</tr>
<tr>
<td>Cycle Time</td>
<td>5µs</td>
<td>5µs</td>
</tr>
<tr>
<td>Output Loads:</td>
<td>Figure 6</td>
<td>Figure 6</td>
</tr>
<tr>
<td>On/Off</td>
<td>Figure 7</td>
<td>Figure 7</td>
</tr>
</tbody>
</table>
Figure 3. Input-Port/Output-Port Timing

Figure 4. Input-Port Timing
3. Chip select to output on, high (TCA1, Figure 4)
4. Chip select to output off, low (TCB0, Figure 4)
5. Chip select to output off, high (TCB1, Figure 4)
6. Clock to service request (TSR0, Figure 3)
7. Chip select to service request (TSR1, Figure 4)
8. Clear to service request (TSR2, Figure 3)

Output Mode Propagation Delays
1. Clear to data outputs (TCLR, Figure 3)
2. Clock to data outputs, high (TOD1, Figure 3)
3. Clock to data outputs, low (TOD0, Figure 3)
4. Clock to service request (TSR0, Figure 3)
5. Chip select to service request (TSR1, Figure 4)

Input Mode Input Timing
1. Minimum clock pulse width (TWS, Figure 4)
2. Minimum data setup time (TDS, Figure 4)
3. Minimum data hold time (TDH, Figure 4)
4. Minimum time from clock 0 to chip select 0 to 1 (TCS, Figure 4)

Output Mode Input Timing
1. Minimum clock pulse width (TWS, Figure 4)
2. Minimum data setup time (TDS, Figure 4)
3. Minimum data hold time (TDH, Figure 4)

Transition Times
1. Output, low to high (TTLH, Figure 5)
2. Output, high to low (TTHL, Figure 5)

Figure 5. Transition Time
The input timing parameters TWS, TDS, and TDH were measured using time slots 9 through 38 of the functional test pattern (refer to Table 1). The parameter under test was varied in 1-nanosecond increments as shown in Table 4. The TCS parameter had no effect on the proper functioning of the device.

3.3 DC PARAMETRIC TESTS

Most of the DC parametric tests were performed in a straightforward manner. Input conditions were applied using the drivers as in the functional and AC tests, and the pin under test was forced with a regulated voltage or current supply (depending on the specific parameter). The desired parameter was then measured and recorded.
The exceptions were the VIH (minimum logic "1" input voltage) and VIL (maximum logic "0" input voltage) tests. These were similar to the input timing tests, except that the input voltages were varied instead of the timing.

In the VIH test, all inputs except the one under test had drive levels of VDD and 0V. Timing conditions were nominal. The logic "0" level of the input under test was set at 0V, and the logic "1" level was set to a voltage low enough to ensure that the device would fail to function properly. The functional test was run repeatedly, with the logic "1" level on the input under test raised each time, until the device passed. The voltage at which the device first passed was the minimum logic "1" level for the input under test. The VIL test was performed in a similar manner.

Table 5 lists the DC parameters measured, with the exception of VIH and VIL. These two parameters were measured using the functional test pattern of Table 2. The timing conditions were the same as those for functional tests (refer to Paragraph 2.2). The input voltages were varied in 0.1-volt increments as shown in Table 6. Each input was tested separately at each voltage.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Name</th>
<th>Pin</th>
<th>Voltage/Current Forced</th>
<th>VDD-VSS (V)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>VICP</td>
<td>Positive input clamp voltage</td>
<td>Each input</td>
<td>1 mA</td>
<td>0</td>
<td>VDD and VSS tied to ground</td>
</tr>
<tr>
<td>VICN</td>
<td>Negative input clamp voltage</td>
<td>Each input</td>
<td>-1 mA</td>
<td>0</td>
<td>VDD and VSS tied to ground</td>
</tr>
<tr>
<td>I1H</td>
<td>Input current, high</td>
<td>Each input</td>
<td>15 V</td>
<td>15</td>
<td>0V on other inputs</td>
</tr>
<tr>
<td>I1L</td>
<td>Input current, low</td>
<td>Each input</td>
<td>0 V</td>
<td>15</td>
<td>15V on other inputs</td>
</tr>
<tr>
<td>IOH</td>
<td>Output current, low</td>
<td>Each input</td>
<td>4.6 V</td>
<td>5</td>
<td>Output under test is in high (logic &quot;1&quot;) state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4.5 V</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>9.5 V</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>9.0 V</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10.5 V</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>I0L</td>
<td>Output current, low</td>
<td>Each output</td>
<td>0.4 V</td>
<td>5</td>
<td>Output under test is in low (logic &quot;0&quot;) state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.5 V</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.5 V</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.0 V</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.5 V</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>IOZH</td>
<td>High-impedance output current, high</td>
<td>Each data output</td>
<td>12 V</td>
<td>12</td>
<td>0V on all inputs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>15 V</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>IOZL</td>
<td>High-impedance, output current, low</td>
<td>Each data output</td>
<td>0 V</td>
<td>12</td>
<td>0V on all inputs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 V</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>I1S</td>
<td>Quiescent supply current</td>
<td>VSS</td>
<td>0 V</td>
<td>10</td>
<td>Precondition by running functional test (Table 1) to vectors 1, 5, 7, 9, 21, 40, 44 and 51. Logic &quot;1&quot; = VDD-VSS, Logic &quot;0&quot; = 0V. Outputs open. Eight tests at each of two voltages.</td>
</tr>
<tr>
<td>Parameter</td>
<td>From (V)</td>
<td>To (V)</td>
<td>VIH (5V)</td>
<td>VIL (5V)</td>
<td>VIH (10V)</td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>-------</td>
<td>----------</td>
<td>----------</td>
<td>-----------</td>
</tr>
<tr>
<td>VIH</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>VIL</td>
<td>0</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Other Pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compare Levels</td>
<td></td>
<td></td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
</tr>
</tbody>
</table>

**TABLE 6. VIH AND VIL TEST CONDITIONS**
4.0 TEST RESULTS

4.1 SUMMARY

Three of the Hughes parts (serial numbers 31, 38, and 46) became inoperable during testing. They each performed normally through one or two runs of the test programs, then began to yield out-of-range values. Serial number 31 was the only device to fail both functional tests repeatedly. The other devices passed the functional test but yielded no reading on numerous parametric tests, particularly those performed at high voltages. Serial number 42 exhibited similar characteristics, beginning with the first iteration of the test program, and remained stable through subsequent runs.

None of the RCA parts failed the functional tests or yielded abnormal data.

4.2 DATA TABULATION

For each parameter, the data was tabulated by device serial number and temperature. The sign "<\(^\ast\)" to the right of a value was used to indicate an out-of-range measurement. The minimum, maximum, mean, standard deviation, and median values were listed at the bottom of each temperature column. Out-of-range measurements were excluded from the statistics.

The RCA parts were numbered 3 through 27; the Hughes parts were numbered 28 through 52. The statistics for each group were calculated separately. Serial numbers 31, 38, 42, and 46 were excluded from the tabulations.
In addition to the printed data, histograms of some parameters were provided. Each histogram displays data for one or more parameters at all five temperatures, in ascending order (-55°C, -20°C, 25°C, 85°C, 125°C). The histograms illustrate clearly both the effect of temperature and the distribution of devices for each parameter. RCA and Hughes parts were plotted separately. Table 7 is a list of the parameters plotted. The histograms are provided in Appendix A.

**TABLE 7. LIST OF HISTOGRAMS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISS</td>
<td>VDD = 15V</td>
</tr>
<tr>
<td>IOH</td>
<td>VDD = 5V, VO = 4.6V</td>
</tr>
<tr>
<td></td>
<td>VDD = 10V, VO = 9.5V</td>
</tr>
<tr>
<td>IOL</td>
<td>VDD = 5V, VO = 0.4V</td>
</tr>
<tr>
<td></td>
<td>VDD = 10V, VO = 0.5V</td>
</tr>
<tr>
<td>TCA0 and TCA1 together</td>
<td>VDD = 5V</td>
</tr>
<tr>
<td>TCB0 and TCB1</td>
<td>VDD = 5V</td>
</tr>
<tr>
<td></td>
<td>VDD = 10V</td>
</tr>
<tr>
<td>TOD0 and TOD1</td>
<td>VDD = 5V</td>
</tr>
<tr>
<td></td>
<td>VDD = 10V</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS OF
HUGHES HCMP 1852D and RCA CDP1852D
8-BIT, CMOS, I/O PORTS

FINAL REPORT

APPENDIX A
HISTOGRAMS
REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
DATW FOR 10H1

FREQ. OF OCCURRENCE

READINGS:
MAXIMUM:
MEAN:
MINIMUM:
STD DEV:

# OF CELLS 50
CELL SIZE 100.0U

25 MAY 79
Reproducibility of the original page is poor
S-3260  DATA FOR IOL1

IOL: VDD=5V  V0=0 4V

25 MAY 79

# OF CELLS  50
CELL SIZE  200.0U

READINGS:
MAXIMUM  10.60M  9.160M  7.640M  6.555M  6.189M
MEAN  6.947M  6.240M  5.583M  4.682M  4.270M
MINIMUM  4.955M  4.960M  4.640M  4.085M  3.440M
STD DEV  1.093M  785.8U  609.3U  787.3U  852.6U
<table>
<thead>
<tr>
<th># OF CELLS</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>CELL SIZE</td>
<td>4 0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>READINGS</th>
<th>336</th>
<th>336</th>
<th>336</th>
<th>336</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAXIMUM</td>
<td>193 ON</td>
<td>205 ON</td>
<td>235 ON</td>
<td>270 ON</td>
</tr>
<tr>
<td>MEAN</td>
<td>148 ON</td>
<td>169 ON</td>
<td>192 ON</td>
<td>217 ON</td>
</tr>
<tr>
<td>MINIMUM</td>
<td>101 ON</td>
<td>113 ON</td>
<td>133 ON</td>
<td>147 ON</td>
</tr>
<tr>
<td>STD DEV</td>
<td>36 36N</td>
<td>23 57N</td>
<td>27 43N</td>
<td>32 19N</td>
</tr>
</tbody>
</table>

A-6
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

A-7
# OF CELLS 50
CELL SIZE 4.000N

READINGS 236 336 336 336 336 336
MAXIMUM 237.5N 215.5N 340.5N 360.5N 294.5N
MEAN 254.1N 227.2N 296.3N 316.4N 334.3N
MINIMUM 232.0N 230.0N 233.5N 249.4N 259.0N

25 May 79

A-8
DATA FOR T001RH

25 MAY 79

FREQ OF OCCURRENCE

SECONDS

50.00N

250.00N

220.00N

210.00N

150.00N

130.00N

110.00N

90.00N

70.00N

50.00N

# OF CELLS 56
CELL SIZE 4.008N

RECORDS

336

336

336

336

MAXIMUM
199.0N
166.5N
189.0N
21.5N
241.0N

MEAN
126.3N
141.9N
161.3N
193.3N
202.3N

MINIMUM
91.40N
106.5N
114.5N
127.0N
139.5N

STD DEVI
12.24N
13.91N
16.05N
16.80N
20.94N

A-10
S-3360  DATA FOR TD01B  TOD0, TOD1: VDD=10V

25 MAY 79

# OF CELLS  50
CELL SIZE  2000N

READINGS:  336  336  336  336  336  336
MAXIMUM:  56.35N  62.28N  70.80N  82.05N  92.00N
MEAN:  49.12N  54.56N  62.24N  71.18N  80.35N
MINIMUM:  38.70N  42.56N  48.05N  53.65N  56.55N
STD DEV:  3.145N  5.662N  4.260N  5.136N  5.881N

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

A-11
**S-3260**  
DATA FOR ISS  
ISS: UDO=15U  

<table>
<thead>
<tr>
<th>READINGS</th>
<th>MAXIMUM</th>
<th>MEAN</th>
<th>MINIMUM</th>
<th>STD DEV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 000</td>
<td>-2.137N</td>
<td>-28.85N</td>
<td>4.831N</td>
</tr>
<tr>
<td></td>
<td>0 000</td>
<td>-3.406N</td>
<td>-33.95N</td>
<td>7.296N</td>
</tr>
<tr>
<td></td>
<td>0 000</td>
<td>-7.107N</td>
<td>-55.00N</td>
<td>17.15N</td>
</tr>
<tr>
<td></td>
<td>176</td>
<td>-2 200N</td>
<td>-22.55N</td>
<td>54.29N</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>-35.45N</td>
<td>-16.78N</td>
<td>161.9N</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>-955 0N</td>
<td>-516.8N</td>
<td>-161.9N</td>
</tr>
</tbody>
</table>

**DATA EDITED**  
# OF CELLS 100  
FREQ OF OCCURRENCE  

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
S-126J  DATA FOR IOH1
IOH  UDD=5V  VD=4.6V

25 MAY 79

# OF CELLS  50
CELL SIZE  100  AU

FREQ OF OCCURRENCE

READINGS:
MAXIMUM:  425  425  425  425
MEAN:  417.3  417.3  417.3  417.3
MINIMUM:  417.3  417.3  417.3  417.3
STD DEVI.:  417.3  417.3  417.3  417.3

A-14
# OF CELLS: 50
CELL SIZE: 200 mV

READINGS:

MAXIMUM: -8.760M -7.600M -6.420M -5.250M
MEAN: -10.45M -9.849M -8.862M -7.814M
MINIMUM: -12.35M -10.75M -9.570M -8.575M
STD DEV: 953.30 826.20 743.90 652.20

FREQ. OF OCCURRENCE

25 MAY 79

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

A-15
5-3360 DATA FOR IOL1
IOL: UDD=5U UG=6.4U

25 MAY 79

# OF CELLS 50
CELL SIZE 200 8U

FREQ. OF OCCURRENCE

READINGS:
MAXIMUM: 225 225 225 225 225 225
MINIMUM: 6.830M 5.810M 4.800M 3.790M 2.780M 1.770M
STD DEVI: 816.6U 730.7U 652.9U 567.4U 482.1U 396.8U

A-16
REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
S-3260  DATA FOR TAB 1A  TCA0,TCA1: VDD=5V

25 MAY 79

# OF CELLS  50
CELL SIZE  5.000N

READINGS:  400  400  400  400  400
MAXIMUM:  160.0N  182.0N  210.0N  232.0N  263.5N
MEAN:  110.0N  125.0N  144.3N  163.7N  181.9N
MINIMUM:  71.00N  79.45N  90.60N  104.0N  114.5N
STD DEVIATION:  23.90N  27.36N  31.44N  35.80N  40.42N
S-325B DATA FOR TAB1B
TCA0, TCA1: VDD=10V
25 MAY 79

<table>
<thead>
<tr>
<th># OF CELLS</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>CELL SIZE</td>
<td>2.000N</td>
</tr>
</tbody>
</table>

### READINGS
- MAXIMUM: 65.50N, 74.00N, 85.30N, 96.95N, 110.00N
- MEAN: 47.45N, 53.19N, 60.59N, 68.86N, 76.90N
- MINIMUM: 32.75N, 36.05N, 40.50N, 48.80N, 58.30N
- STD DEVI: 8.37N, 9.73N, 11.63N, 13.59N, 15.82N

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR
S-3.250  DATA FOR TC01A  TCB0, TCB1: VDD=5V

FREQ. OF OCCURRENCE

25 MAY 79

SECONDS

360 ON
350 ON
340 ON
330 ON
320 ON
310 ON
300 ON
290 ON
280 ON
270 ON
260 ON
250 ON
240 ON
230 ON
220 ON
210 ON
200 ON
190 ON
180 ON

# OF CELLS  50
CELL SIZE  4.000N

READINGS:
MAXIMUM:  400  400  400  400  400
MEAN:     295.5N  302.5N  327.0N  349.0N  376.0N
MINIMUM:  198.5N  194.0N  203.0N  221.2N  236.8N
STD DEVI:  20.38N  23.57N  27.90N  32.27N  36.65N

A-20
S-3260  DTH FOR TD01A  TDD00, TDD1: UDD=SU

25 MAY 79

# OF CELLS  50
CELL SIZE  4.000N

MEASUREMENTS:

MAXIMUM:  400  400  400  400  400
MEAN:  135.5N  153.6N  174.5N  196.5N  219.5N
MINIMUM:  73.00N  81.60N  92.10N  104.5N  115.00N
STD DEVIATION:  16.04N  18.39N  21.22N  24.03N  27.19N

A-22
REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR