

**THE JET PROPULSION LABORATORY/
CALIFORNIA INSTITUTE OF TECHNOLOGY
BLOCK II VLBI PROCESSOR**

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ABSTRACT

The very long baseline interferometry (VLBI) groups at the Jet Propulsion Laboratory (JPL) and the California Institute of Technology are jointly constructing a multistation, multi-channel cross-correlation processor using the 250 kbit to 4 Mbit recording format developed for the Goddard/Haystack Mark III VLBI system. The design is modular, using bit-sliced micro-processors to perform the routine calculations for phase and delay on a per station basis, as well as for fractional bit-shift correction and Fourier transformation of the correlation coefficients on a per baseline basis. Plans call for completion in 1981 of a three station 28 channel processor that will easily expand to 10 stations, 28 channels.

- PERSONNEL
 - HARDWARE MARTY EWING, JOHN PETERSON, JIM DILLON
 - SOFTWARE DAVE ROGSTAD, WAYNE HAMMOND
- GOALS
 - BLOCK I - 500 KBIT NEAR-REAL-TIME OPERATIONAL SYSTEM ON DSN FOR TIME SYNC, UT1 AND POLAR MOTION, Δ VLBI
 - BLOCK II - MARK III COMPATIBLE SYSTEM FOR CATALOG MAINTENANCE, SOURCE STRUCTURE, DSN BASELINE DETERMINATION, GEODESY
- PRINCIPAL PROCESSOR CHARACTERISTICS
 - HARDWARE DELAY
 - PHASE ROTATION IN STATIONS
 - DELAY AND PHASE UPDATES IN MICROPROCESSORS
 - 16 LAG CHANNELS PER CORRELATOR
 - FFT AND FRACTIONAL BIT SHIFT CORRECTION IN MICROPROCESSORS
 - MULTILEVEL TONE DETECTOR PER STATION
 - 28 FREQUENCY CHANNELS, 3 STATIONS (EXPANDABLE) FOR BLOCK II

Figure 1. Block I/II VLBI processors.

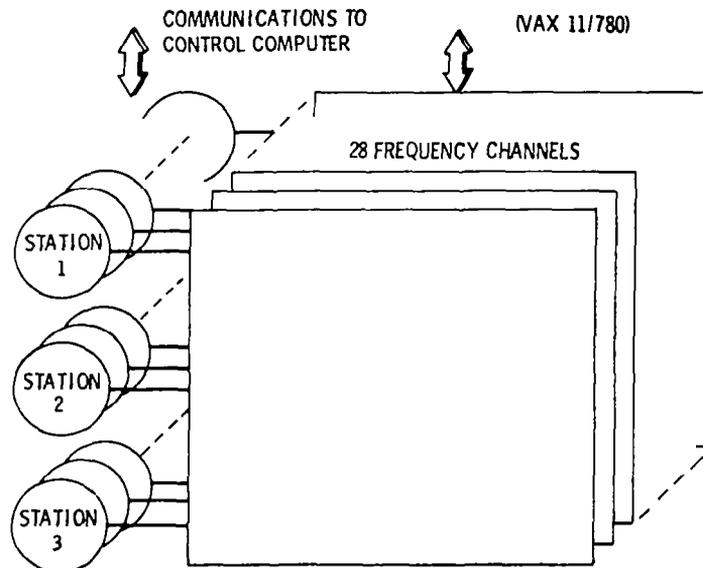


Figure 2. Schematic diagram of Block II VLBI processor.

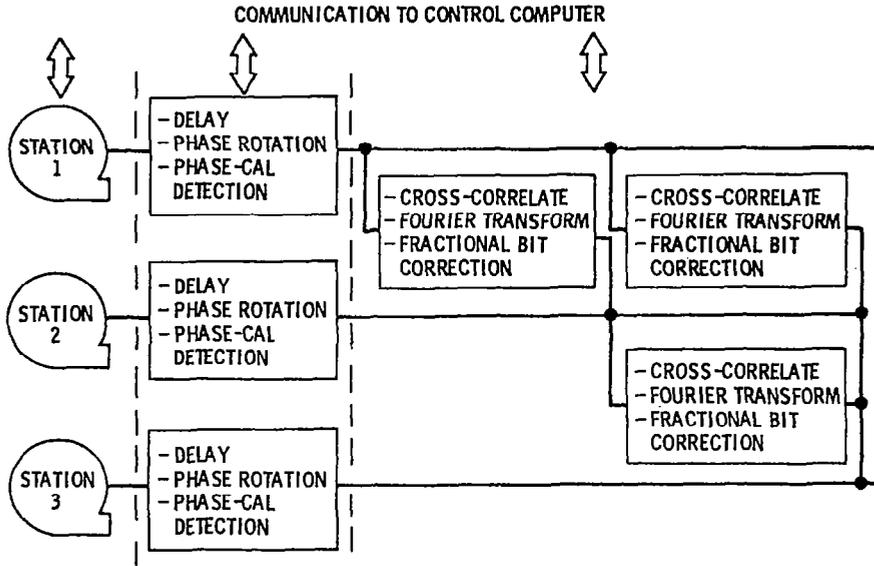


Figure 3. Block diagram of Block II VLBI processor single frequency channel.

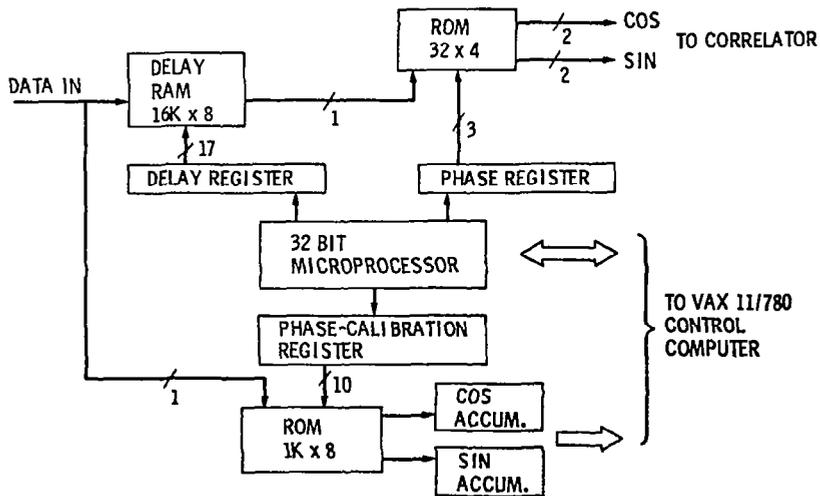


Figure 4. Schematic diagram of station module.

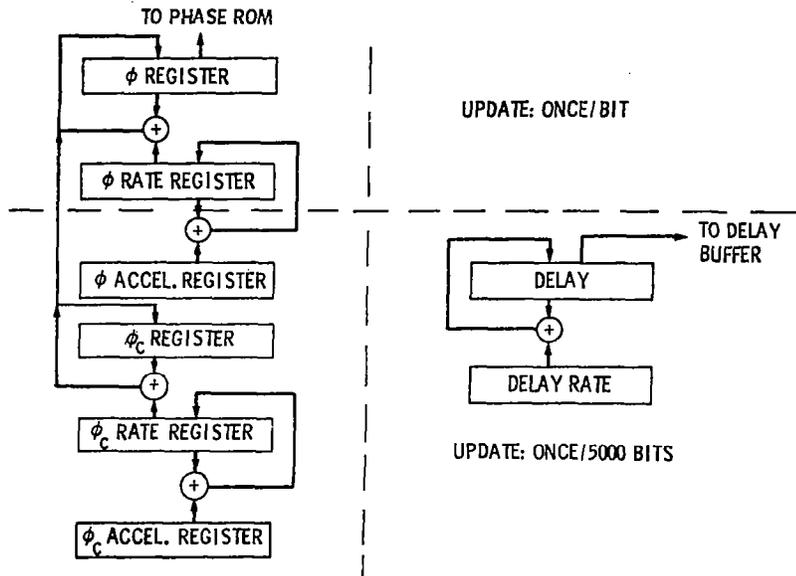


Figure 5. Station module update algorithms.

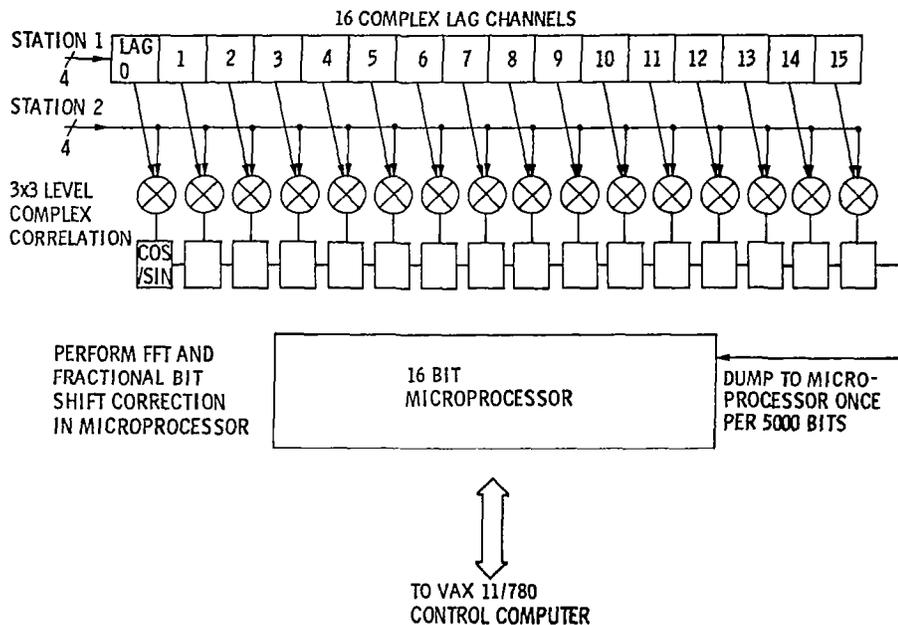


Figure 6. Schematic diagram of correlator module.