A TRANSLATOR WRITING SYSTEM FOR
MICROCOMPUTER HIGH-LEVEL LANGUAGES AND ASSEMBLERS

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NASA LaRC uses many dedicated microprocessors in aerospace research. Few software tools are available for these machines, and in particular, very few have any form of high-level language facility. Since the Langley environment involves considerable experimentation, a great deal of software is experimental and may change frequently. It has to be prepared relatively quickly and at low cost.

In order to implement high-level languages whenever possible, a Translator Writing System of advanced design has been developed. It is intended for routine production use by many programmers working on different projects. As well as a fairly conventional parser generator, it includes a system for the rapid generation of table driven code generators. This code generation system is the result of research performed at the College of William and Mary under NASA sponsorship. The parser generator was developed from a prototype version written at the College of William and Mary.

The Translator Writing System includes various tools for the management of the source text of a compiler under construction. In addition, it supplies various "default" source code sections so that its output is always compilable and executable. The system thereby encourages iterative enhancement as a development methodology by ensuring an executable program from the earliest stages of a compiler development project.

This presentation will describe the Translator Writing System and some of its applications. These include the PASCAL/48 compiler, three assemblers, and two compilers for a subset of HAL/S. PASCAL/48 is a Pascal-like language for the Intel-8748 microcomputer. The assemblers which have been built are for assembly language subsets for the Intel-8080, the Motorola M68000, and the NSSC-II. The HAL/S subset was implemented for the Intel-8080 and the GE 703. Detailed measurements of the use of the system to build the code generators for the HAL/S compilers will be given.

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**THE PROBLEM**

- NEED HIGH-LEVEL LANGUAGES, HENCE COMPILERS
- NEED ASSEMBLERS
- ONE SOLUTION IS A TWS

**TWS CRITERIA**

- ENCOURAGE ITERATIVE ENHANCEMENT
  - EARLIEST POSSIBLE EXECUTION
  - TEXT MANAGEMENT TO RELIEVE TEDIOUM
- FLEXIBILITY IN ITS USE
- TRANSPORTABLE IMPLEMENTATION

**TRANSFORMER WRITING SYSTEM**

[Diagram showing the process of transforming a specification into a compiler.]
USE OF TWS

1. IF PARSER NEEDED, RUN PARGEN, EXECUTE RESULTING COMPILER TO TEST.

2. CHANGE GRAMMAR AS NECESSARY, RERUN PARGEN.

3. ADD SEMANTICS USING EDITOR.

4. RECOVER GRAMMAR AND SEMANTICS WITH GRAMGEN IF NECESSARY TO RERUN PARGEN.

5. IF CODE GENERATION NEEDED, PREPARE CGGL SPECIFICATION AND RUN CODGEN.

6. MODIFY CGGL AS NEEDED.

7. ITERATE THROUGH ABOVE STEPS ADDING LANGUAGE FEATURES AS DESIRED.

PARGEN

• INPUTS
  - GRAMMAR IN STANDARD BNF
  - SEMANTICS IN PASCAL
  - SKELETON OR OLD COMPILER

• OUTPUT IS AN EXECUTABLE COMPILER INCLUDING
  - SCANNER
  - LALR (1) PARSER
  - SEMANTICS ROUTINE

• TEXT MANAGER PRESERVES PROGRAMMER'S CONTRIBUTION TO COMPILER E.G., SYMBOL TABLE ROUTINES
CODGEN

- INPUTS
  - CGGL SPECIFICATION
  - SKELETON OR OLD COMPILER

- OUTPUT IS AN EXECUTABLE COMPILER INCLUDING A CODE GENERATOR.

- CGGL IS A NON-PROCEDURAL LANGUAGE FOR DESCRIBING THE CODE-
  GENERATION PROCESS.

- TEXT MANAGER PRESERVES PROGRAMMER'S CONTRIBUTION TO COMPILER
  E.G., MACHINE LANGUAGE FORMATTER.

PASCAL/48

- INTL-8748
  - MICROCOMPUTER
  - 8-BIT CPU
  - 64 WORD RAM
  - 1024 WORD ROM
  - 27 I/O LINES

- PASCAL/48
  - PASCAL DERIVATIVE FOR 8748
  - EXTENSIONS TO ALLOW CONTROL OVER GENERATED CODE
  - RESTRICTIONS TO PROHIBIT INEFFICIENT FEATURES
  - COMPILER AVAILABLE ON CDC CYBERS
ASSEMBLERS

• CUSTOMIZED SKELETON FOR ASSEMBLERS
  - TWO PASSES
  - STANDARD LISTING BY DEFAULT
  - FLEXIBLE INPUT FORMAT CONVENTIONS
  - HANDLES MACROS WITHOUT PARAMETERS

• COMPARED TO META-ASSEMBLER, ASSEMBLER BUILT FOR NSSC-II
  - WAS PRODUCED MORE QUICKLY
  - EXECUTES 5 TIMES FASTER
  - USES ONE FOURTH THE SPACE

EXAMPLE PASCAL/48 PROGRAM

```
VAR
  I[2]: INTEGER;
  A[16..300, PDM]: ARRAY [100] OF INTEGER;

VALUE A = (99 OF 0, 1);

PROCEDURE GET_INPUT;
BEGIN
  REPEAT
    UNTIL PORT1 BIT 3
  END; (* GET_INPUT *)

BEGIN (* PROGRAM FOR_YOU *)
  FOR I := 100 DOWNTO 1 DO
    BEGIN
      GET_INPUT;
      PORT1 := PORT1 AND 2.11100011)
      PORT2 := A[I] + PORT1 XOR I
    END (* FOR I := 100 DOWNTO 1 DO BEGIN *)
END. (* PROGRAM FOR_YOU *)
```
GENERATED CODE FOR EXAMPLE PROGRAM

GENERATED CODE FOR EXAMPLE PROGRAM

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>JMP</td>
<td>L009</td>
</tr>
<tr>
<td>NOP</td>
<td></td>
</tr>
<tr>
<td>JMP</td>
<td>L063</td>
</tr>
<tr>
<td>NOP</td>
<td></td>
</tr>
<tr>
<td>JMP</td>
<td></td>
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<tr>
<td>NOP</td>
<td></td>
</tr>
<tr>
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<td>L007</td>
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<tr>
<td>JMP</td>
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<td>CLR</td>
<td>A</td>
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<tr>
<td>MOV</td>
<td>PSW,A</td>
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<tr>
<td>JMP</td>
<td>L012</td>
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<tr>
<td>L007:</td>
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<tr>
<td>JMP</td>
<td></td>
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<tr>
<td>CLR</td>
<td>A</td>
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<tr>
<td>MOV</td>
<td>PSW,A</td>
</tr>
<tr>
<td>JMP</td>
<td>L012</td>
</tr>
<tr>
<td>L009:</td>
<td></td>
</tr>
<tr>
<td>IN</td>
<td>A,P1</td>
</tr>
<tr>
<td>CPL</td>
<td></td>
</tr>
<tr>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>JB3</td>
<td>L000</td>
</tr>
<tr>
<td>RET</td>
<td></td>
</tr>
<tr>
<td>L00D:</td>
<td></td>
</tr>
<tr>
<td>MOV</td>
<td>R2,#99</td>
</tr>
<tr>
<td>CALL</td>
<td>L000</td>
</tr>
<tr>
<td>L012:</td>
<td></td>
</tr>
<tr>
<td>ANL</td>
<td>P1,#227</td>
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<tr>
<td>IN</td>
<td>A,P1</td>
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<tr>
<td>MOV</td>
<td>P1,A</td>
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<tr>
<td>MOV</td>
<td>A,P2</td>
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<tr>
<td>MGVP3</td>
<td>A,P2</td>
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<td>ADD</td>
<td>A,P2</td>
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<tr>
<td>XRL</td>
<td>A,R1</td>
</tr>
<tr>
<td>OUTL</td>
<td>P2,A</td>
</tr>
<tr>
<td>DJNZ</td>
<td>R2,L014</td>
</tr>
</tbody>
</table>

SEPARATE CODE GENERATION
USING CGGL

LANGUAGE: HAL/S

INTERMEDIATE CODE LANGUAGE: HALMAT

--- 178 OPERATORS TOTAL
--- 30 OPERATORS IMPLEMENTED
--- 25 GENERATE CODE
--- BASICALLY AN INTEGER SUBSET WITH SIMPLE CONTROL STRUCTURES

CODE GENERATORS
--- ONE PASS
--- NO PRE-OPTIMIZATION PASS
--- NO PEEPHOLE OPTIMIZATION
--- INTEL 8080, GE 703
IMPLEMENTATIONS

INTEL 8080

- 8 BIT MACHINE
- SINGLE ACCUMULATOR
- NO INDEX REGISTER
- 1, 2, 3 BYTE INSTRUCTIONS
- HARDWARE STACK
- ONLY INTEGER ADD, SUBTRACT
- 16 BIT ADDRESSES

GE 703

- 16 BIT MACHINE
- SINGLE ACCUMULATION
- INDEX REGISTER
- ONE WORD INSTRUCTIONS
- NO HARDWARE STACK
- INTEGER ADD, SUBTRACT, MULTIPLY, DIVIDE
- ONLY ADDRESS CURRENT PAGE, PAGE ZERO
- PAGE: 256 WORDS

703 Code Generator

<table>
<thead>
<tr>
<th>TASK</th>
<th>TIME (DAYS)</th>
</tr>
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<tbody>
<tr>
<td>READING MANUAL</td>
<td>.5</td>
</tr>
<tr>
<td>CGGL PROGRAM</td>
<td>1.5</td>
</tr>
<tr>
<td>WRITING PASCAL ROUTINES</td>
<td>1.5</td>
</tr>
<tr>
<td>DEBUGGING</td>
<td>1.0</td>
</tr>
</tbody>
</table>

4.5 DAYS

NOTES:

1. ALL PROGRAMS WERE CODED AND KEYED BY NOONAN.

2. SOME OF DEBUGGING TIME WAS USED IN CLEANUP.

3. ONE DEBUGGING RUN WAS USED TO FIX A BUG INTRODUCED BY CLEANUP.

4. A TOTAL OF 6 RUNS (EXECUTION) WERE USED.

5. ONE CGGL BUG.
703 IMPLEMENTATION

<table>
<thead>
<tr>
<th>Source of Code</th>
<th>No. Procedures</th>
<th>% Lines</th>
<th>% Instr. Storage</th>
</tr>
</thead>
<tbody>
<tr>
<td>8080 IMPE.</td>
<td>46</td>
<td>58%</td>
<td>58%</td>
</tr>
<tr>
<td>MODIFIED 8080</td>
<td>4</td>
<td>8%</td>
<td>6%</td>
</tr>
<tr>
<td>NOONAN</td>
<td>9</td>
<td>10%</td>
<td>10%</td>
</tr>
<tr>
<td>CGGL</td>
<td>1</td>
<td>24%</td>
<td>26%</td>
</tr>
</tbody>
</table>

Notes:

1. CGGL PROGRAM: 292 LINES
2. PASCAL PROGRAM: 890 LINES
3. FOR AN EARLIER NON-TABLE-DRIVEN IMPLEMENTATION, CGGL ACCOUNTED FOR 83% OF LINES AND 77% OF STORAGE.