The Microcomputer Array Processor System (MAPS) is a programmable multiprocessor computer system designed for Electronic Warfare applications for the Air Force Avionics Laboratory (AFAL). The system architecture retains many of the classic multiprocessor design concepts including a master-slave relationship among its microprocessors under the control of a single operating system in a tightly coupled structure. Each processor is a 32-bit programmable computer with its own dedicated memory and a capability to execute approximately 4 million instructions a second. In addition to the dedicated memory, each processor can communicate with numerous banks of common memory (referred to as global memory). The various global memory modules and their communication structure serve to tie the individual processors together in a symmetrical multiprocessor computer architecture. The multiprocessor system is modular and can contain as few as 2 and as many as 8 processors coupled with from 1 to 16 banks of global memory and executes 32 million instructions per second. Expansions beyond these limits are possible if every processor does not have to have access to every global memory module. Currently, a 4 processor system (with 3 banks of global memory) is installed at Wright Patterson Air Force Base for use by AFAL. This system will be expanded to 6 processors during 1980. This multiprocessor subsystem is approximately 1.6 cubic feet and consumes under 400 watts of power.
MULTIPROCESSOR SYSTEM ATTRIBUTES

- TASK
- SYMMETRY
- COMMUNICATION
- PROCESSOR INTELLIGENCE
MAP PROCESSING FUNCTIONS

- Establishes file of active emitters
  - Determines PRI
  - Reports presence of new emitters.
- Tracks established emitters
  - Tracks in time and angle
- Deletes inactive emitters
- Capability for
  - Scan rate determination
  - Emitter type identification
  - Receiver control
  - Power management

PDS SYSTEM

0.1 - 19 GHz

PROCESSING SYSTEM

RECEIVER

DIGITIZER

PRE PROCESSOR

MAP

DISPLAY CONTROL

DISPLAY

INTERCEPT PROCESSING

EMITTER ESTABLISHMENT

SYSTEM PROCESSING

RECEIVER CONTROL
MAP ARCHITECTURE

MICROPROCESSOR-1

PROGRAM MEMORY

CPU

PORT

PORT

PORT

EXPANSION

PROGRAM MEMORY

CPU

PORT

PORT

PORT

PROGRAM MEMORY

CPU

PORT

PORT

PORT

PROGRAM MEMORY

CPU

PORT

PORT

PORT

EXPANSION

POSP

GLOBAL MEMORY

BANK-1

BANK-2

BANK-3

MINI-COMPUTER

EXPANSION
PROCESSOR

TIMING & CONTROL

INTERRUPTS

PCU

PM 4K x 32

PIPECLINE

ALU

BUS TRANSCEIVER

EXTERNAL DEVICES

PCU

CONDITION DECODE

OPCODE DECODE

BRANCH ADDRESS

PIPELINE

PCU (PROGRAM CONTROL UNIT)

PC STACK

NEXT INSTRUCTION CONTROL

REPEAT COUNTER

PM ADDR

INTERRUPT CONTROL UNIT

STATUS REGISTER

MASK REGISTER

BUS

268
MICROPROCESSOR SLICE BLOCK DIAGRAM

CLOCK

A ADDRESS
B ADDRESS

DIRECT INPUT

MICRO-CODE

MICRO-INSTRUCTION DECODE

MULTIPLEXER

OUTPUT CONTROL

OUTPUT

RAM SHIFT

Q SHIFT

Q REGISTER

16 X 4 RAM READ A & B WRITE B

SELECTOR

SELECTION DECODE

ALU

F

OVR

CIN

G

F3

Cn+4

C

R

S

W

F

0

1
<table>
<thead>
<tr>
<th>TYPE</th>
<th>INSTRUCTION</th>
<th>EXECUTION (nSec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>REGISTER/REGISTER</td>
<td>.250 or 325</td>
</tr>
<tr>
<td>1</td>
<td>INPUT/OUTPUT</td>
<td>350 OUTPUT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 INPUT</td>
</tr>
<tr>
<td>2</td>
<td>REGISTER/IMMEDIATE</td>
<td>350</td>
</tr>
<tr>
<td>3</td>
<td>READ/WRITE PROGRAM MEMORY</td>
<td>525 READ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>650 WRITE</td>
</tr>
<tr>
<td>4</td>
<td>EXTERNAL FUNCTION CONTROL</td>
<td>350</td>
</tr>
<tr>
<td>5</td>
<td>INTERRUPT CONTROL</td>
<td>400</td>
</tr>
<tr>
<td>6</td>
<td>PC STACK CONTROL</td>
<td>300</td>
</tr>
<tr>
<td>7</td>
<td>CONDITIONAL BRANCH</td>
<td>200 NO BRANCH</td>
</tr>
<tr>
<td></td>
<td></td>
<td>300 BRANCH</td>
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</table>
# Comparison of μProcessors

<table>
<thead>
<tr>
<th></th>
<th>AMD AM2901</th>
<th>MMI MM6701</th>
<th>Intel 3002</th>
<th>TI SBP0400</th>
<th>Motorola M10800</th>
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<tbody>
<tr>
<td><strong>Slice Width</strong></td>
<td>4 bits</td>
<td>4-bits</td>
<td>2-bits</td>
<td>4-bits</td>
<td>4-bits</td>
</tr>
<tr>
<td><strong>Cycle Time</strong></td>
<td>100ns</td>
<td>200ns</td>
<td>150ns</td>
<td>1000ns</td>
<td>55ns</td>
</tr>
<tr>
<td>(Register to register; Read, Modify, Write)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Power Dissipation</strong></td>
<td>0.92W</td>
<td>1.12W</td>
<td>1.45W</td>
<td>0.13W</td>
<td>1.3W</td>
</tr>
<tr>
<td>(4 bits)</td>
<td></td>
<td></td>
<td>(2 x 0.73)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Addressable Registers</strong></td>
<td>16</td>
<td>16</td>
<td>11</td>
<td>8</td>
<td>1 (External 4-256)</td>
</tr>
<tr>
<td><strong>Register Addressing Mode</strong></td>
<td>Two-Address</td>
<td>Two-Address</td>
<td>Single-Address</td>
<td>Single-Address</td>
<td>Single-Address</td>
</tr>
<tr>
<td><strong>Number of Microcode Control Inputs</strong></td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>9</td>
<td>16</td>
</tr>
<tr>
<td><strong>Primary Arithmetic Functions</strong></td>
<td>R + S</td>
<td>R + S</td>
<td>R + S</td>
<td>R + S</td>
<td>R + S</td>
</tr>
<tr>
<td><strong>Primary Logic Functions</strong></td>
<td>R - S</td>
<td>R - S</td>
<td>R - S</td>
<td>R - S</td>
<td>R - S</td>
</tr>
<tr>
<td><strong>Possible Source operand Combination to ALU</strong></td>
<td>203</td>
<td>203*</td>
<td>24*</td>
<td>33*</td>
<td>6 - 262</td>
</tr>
<tr>
<td><strong>Possible ALU Destination Registers</strong></td>
<td>17</td>
<td>17</td>
<td>12</td>
<td>10</td>
<td>2 - 258</td>
</tr>
<tr>
<td><strong>Flags</strong></td>
<td>Carry</td>
<td>Carry</td>
<td>Carry</td>
<td>Carry</td>
<td>Carry</td>
</tr>
<tr>
<td></td>
<td>Overflow</td>
<td>Overflow</td>
<td>Overflow</td>
<td>Overflow</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Zero</td>
<td>Zero</td>
<td>F=1111</td>
<td>Zero</td>
<td></td>
</tr>
</tbody>
</table>
| *Not all functions can be performed on all operand pairs.*
DISTINCTIVE CHARACTERISTICS

- Two-address architecture —
  Independent simultaneous access to two working
  registers saves machine cycles.
- Eight-function ALU —
  Performs addition, two subtraction operations, and
  five logic functions on two source operands.
- Flexible data source selection —
  ALU data is selected from five source ports for a
  total of 203 source operand pairs for every ALU
  function.
- Left/right shift independent of ALU —
  Add and shift operations take only one cycle.
- Four status flags —
  Carry, overflow, zero, and negative.
- Expandable —
  Connect any number of Am2901's together for longer
  word lengths.
- Microprogrammable —
  Three groups of three bits each for source operand,
  ALU function, and destination control.

MAP PERFORMANCE
(42 Emitter Environment)

PROCESSING TIME (MSEC)

PULSE RATE = 31,800

NUMBER OF SLAVE PROCESSORS