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ANALYSIS OF SPACE TELESCOPE DATA COLLECTION SYSTEM

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by

Frank Ingels - Principal investigator
W. O. Schoggen - Associate Investigator



Mississippi State University
Mississippi State, MS 39762

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DATA COLLECTION SYSTEM

INTERIM
FINAL REPORT
COVERING
THE PERIOD
JULY 1, 1979
to
OCTOBER 31, 1980

Submitted
by

Frank Ingels - Principal Investigator
W. O. Schoggen - Associate Investigator

Mississippi State University
Electrical Engineering
Mississippi State, MS 39762

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TABLE OF CONTENTS

Chapter	Page
LIST OF FIGURES	iii
LIST OF TABLES	v
LIST OF SYMBOLS	vi
SUMMARY OVERVIEW	ix
1. INTRODUCTION	1
1.A Command Function and Forward Communication Link	1
1.B Data Function	5
1.B.1 Engineering Data	5
1.B.2 Science Data	6
1.C Return Communication Links	8
2. THE SPACE TELESCOPE S-BAND SINGLE-ACCESS SYSTEM	12
2.A Space Telescope Orbiting Observatory	12
2.A.1 Scientific Instruments	13
2.A.2 Control Unit/Science Data Formatter	13
2.A.2.a Science Data Formatter	16
2.A.2.b 255 PN Encoder	20
2.A.2.c Reed/Solomon Encoder/ Interleaver	21
2.A.3 Support System Module	24
2.A.3.a Data Management Subsystem	24
2.A.3.b Instrumentation and Communications System	34
2.B Tracking and Data Relay Satellite System	35

TABLE OF CONTENTS (Continued)

Chapter	Page
2.B.1 Return Channel Link Model	35
2.B.2 Ground Station	36
2.C NASA Communications Network	40
2.D Assumptions	41
3. ANALYSIS OF THE PERFORMANCE OF THE SSA RETURN LINK	42
3.A Probability of Error for Concatenated Code	42
3.A.1 Transparency of the DOMSAT Link	45
3.A.2 Probability of a Burst	47
3.B Probability of Error on the Inner Channel (Output of the 255 PN Encoder Sequence to Output of Viterbi Decoder	53
3.C 255 PN Sequence	72
4. RECOMMENDATIONS AND RESULTS	75
5. APPENDICES	82
5.A Example of a Reed/Solomon Encoder/Interleaver	83
5.B Delay Modulation	85
5.C Example of a Concatenated Code	88
5.D Affect of PSK Demodulator Carrier Slip on Differential Encoded Data with/without Interleaving	92
6. REFERENCES	95

LIST OF FIGURES

Figure		Page
1.1	The Space Telescope System	2
1.2	DMS and SI C&DH Command Formats	4
1.3	ST Data Transmission Flow	9
2.1a	Science Data Flow Through the ST	14
2.1b	Encoding Summary for the Science Data	15
2.2	General Data Packet Format for ST Science Data	18
2.3	Matrix Visualization of the R/S Encoder	23
2.4a	Differential Encoder with Truth Table	30
2.5	Convolutional Encoder with PCI and Cover Sequence	31
2.6	Periodic Convolutional Interleaver and Deinterleaver	33
2.7	Synchronization Strategy for the Periodic Convolutional Deinterleaver	39
3.1	Generalized ST/TDRSS Concatenated Coding Concept	43
3.2	Probability of an Error Burst Longer than L Versus Burst Length for Rate 1/3 Viterbi Decoding with BER = 10^{-5}	48
3.3	Average Burst Length Statistics for Rate 1/2 and 1/3 Viterbi Decoded Errors	49
3.4	Concatenated Coding BER Versus Inner Coding E_b/N_o for A R/S Outer Code with J = 8	52
3.5	Costas Loop	65

LIST OF FIGURES (Continued)

Figure		Page
4.1	Probability of Error Versus Energy Per Bit to Noise Density Ratio for 1/3 Soft Decision Viterbi Decoding with $K = 7$	80
4.2	Concatenated Coding BER Versus TDRSS Channel Viterbi Decoded BER For R/S ($J=8$)	81
B.1	NRZ-1 and Delay Modulation Binary Signal Waveforms	87
C.1	Concatenated Code	89

LIST OF TABLES

Table		Page
3.1	Data Loss Estimate Due to Sync Loss	63
3.2	Excepted Bit Error Rate for the SSA Return Link Due to RFI and Bit Slip	73
4.1	TDRSS EIRP Requirements for the SSA Return Link	77
5.2	SSA Predicted Performance	79

LIST OF SYMBOLS

BER	Bit Error Rate
BCU	Bus Coupler Unit
BPSK	Bi-phase Shift Keying
BSR	Bit Slip Rate
CCIR	International Radio Consultative Committee
CDI	Command Detector Interface
C.E.	Convolutional Encoder
CU/SDF	Control Unit/Science Data Formatter
DIU	Data Interface Unit
DMS	Data Management Subsystem
DMU	Data Management Unit
DOMSAT	Domestic Satellite System
E	Number of Correctable Symbol Errors per R/S Block
EIRP	Effective Isotropic Radiated Power
ESTR	Engineering/Science Tape Recorders
FGS	Fine Guidance Sensor
GSFC	Goddard Space Flight Center
HGA	High Gain Antenna
Hz	Hertz
I	In-phase
IC	Integrated Circuits
I&C	Instrumentation and Communications Subsystem
J	Number of Bits Per R/A Symbol

LIST OF SYMBOLS (Continued)

Kbps	Kilobits Per Second
LGA	Low Gain Antenna
MA	Multiple Access
MDPS	Megabits Per Second
MDB	Multiplexed Data Bus
MHz	Megahertz
MSB	Most Significant Bit
N_{\max}	Maximum Number of Output Symbols of the Convolutional Encoder w/o a Transition
NASCOM	NASA Communications Network
NRZ-L	Non-Return-to-Zero-Level
NSSC-I	NASA Standard Spacecraft Computer, Model I
OTA	Optical Telescope Assembly
$P_1(E)$	The R/S Input Symbol Error Probability
$P_2(e)$	The Output Probability of the R/S Decoder/Deinterleaver
$P_b(e)$	Probability of a Bit Error Occurring on the Inner Channel
$P_{R/S}(E)$	Symbol Error Probability Out of the R/S Decoder/Deinterleaver
$P_T(e)$	Overall Bit Error Probability
$P_{VD}(E)$	Bit Error Rate Out of the Viterbi Decoder
$P_{WS}(E)$	Average Bit Error Rate of the TDRSS Link
PCI	Periodic Convolutional Interleaver
PCU	Power Control Unit
PIT	Processor Interface Table

LIST OF SYMBOLS (Continued)

PN	Pseudo Noise
PSK	Phase Shift Key
Q	Quadrature-phase
RF	Radio Frequency
RFI	Radio Frequency Interference
RM	Remote Module, Resource Monitor
R/S	Reed-Solomon
SDF	Science Data Formatter
SI	Scientific Instrument
SI C&DH	SI Control and Data Handling (Subsystem)
SNR	Signal to Noise Ratio
SSA	S-band Single Access
SSM	Support Systems Module
ST	Space Telescope Orbiting Observatory
STINT	Standard Interface for Computer
STOCC	Space Telescope Operations Control Center (at GSFC)
ST Sci	Space Telescope Science Institute Contractor
T	Interval of Heavy RFI
TDRS	Tracking and Data Relay Satellite
TDRSS	Tracking and Data Relay Satellite System
VCO	Voltage Control Oscillator

ANALYSIS OF SPACE TELESCOPE

DATA COLLECTION SYSTEM

SUMMARY OVERVIEW

Each task of the Statement of Work is listed and its portion of report is indicated. By each task is an indication of which monthly progress report addresses this task and a short summary of the results is indicated. Receipt of some recent documentation (the DOMSAT SRI Final Report and a revised TDRSS manual) as well as new developments which have arisen in the last year, have pointed up several work tasks that need to be addressed and these are mentioned at the end of this overview.

It is worth mentioning that several items of interest arose during the span of this contract and these items were addressed upon request even though they may not have been a specific part of the statement of work.

Finally, Table 3.2 and Section 4 summarizes the expected performance of the SSA Link under various conditions.

TASK A: Analyze the effects of frame synchronization loss. This task is addressed in Section 3.B and Section 4. A few remarks at this point would be in order.

A frame sync loss will create loss of data for the frame in which it occurs (since one would not know whether the preceding

data was properly in sync or not) and during search from frame sync the system would of course be losing data. The search mode for reacquisition utilizes multiple search procedures, see Figure vi.1.

The monthly progress reports of October 1979 and November 1979 discuss this Task in greater detail, however a summary statement may be made as follows:

For a bit synchronizer slip, if we assume the minimum data is lost, then 200 bits are lost per a 30 PN sequence state searched. For the 30 bit PN sequence we expect well over 10 states to be searched (This depends upon the type of search protocol used. See the November 1979 monthly report for a discussion of the number of search states expected to be searched), but for a conservative agreement assume 10 states are searched. Then 2000 bits (or an absolute minimum of 600 bits for 3 states searched) should be high in error content and we lose that block of Reed/Solomon data regardless of the interleaver. As a result it is likely that frame sync would drop out during this period and that the next frame of data would also be lost. If the bit synchronizer will perform to the 10^{-11} specification which has been tendered by NASA/GSFC, then the average Bit Error Rate expected due to bit synch loss resulting in frame sync loss would be approximately 4.5×10^{-7} on a 20 hour basis (See November 1979 monthly report).

Assuming bit sync lock but a 30 bit PN sequence lock loss the Viterbi decoder will again lose anywhere from 200 to 500 information bits per state searched. Since there are 30 states that could be searched it is possible to lose 15,000 bits of information

while reacquiring sync, however, if even 3 states are searched a loss of 600 bits minimum would occur which would result in loss of an R/S block of data since the R/S code cannot decode that many errors. A discussion with Dr. Odenwalder of Linkabit, Corporation to discover an average number of states to be searched was not fruitful since the question is a difficult question to answer.

If bit sync and frame sync are locked up correctly and if the 30 bit PN generator for the Viterbi decoder is locked up correctly then we must consider the case of a mistake occurring in the 255 PN sequence generator synch, which is reset by the frame sync word which occurs once in each 1024 segment. For this specific sync loss approximately 1024 bits would be in error one fourth of the time, 769 bits in error one fourth of the time, 514 bits in error and 255 bits in error one fourth of the time. Thus we could experience a full R/S matrix (block) of data loss three out of four times that sync with the 255 PN sequence is lost.

TASK B: Analyze System Parameters pursuant to encoding, decoding interleaving/deinterleaving and spectrum spreading to meet flux density requirements.

An analysis has been made of the bit transition density which should result from the Space Telescope Data Collection Systems (STDCS) for the science data SSA telecommunications link (Section 3.P.a). Originally the last operation before transmission of the science data involved a rate $\frac{1}{2}$ convolutional encoding with channel interleaving to 116 symbol separation and an alternate symbol interleaver. This operation would provide a randomized bit stream

that should have a low flux density of radiated power levels when incident on earth. (See also Section 3.C).

A discussion by Magnavox illustrated the fact that the 255 PN sequence generator which is in the system for meeting CCIR requirements was in reality not necessary with an exception of a few very rare data sequences. Furthermore the power flux density would exceed CCIR requirements for such a short period of time that it is very questionable that these excursions could be measured.

Since this analysis was performed the system has been changed to incorporate a rate 1/3 convolutional encoder which further randomizes the data stream to be transmitted. A review of a Lockheed Computer analysis (Section 2.A.2.b) demonstrated that it is possible that the CCIR could be exceeded by 8-13 db for approximately 10% in the 4KHz bandwidth windows when using 8 bit random and 8 bit periodic data inputs to the SCI and DH, reference 18. However the computer analysis by Lockheed also demonstrates that even with the 255 PN sequence certain data patterns create a CCIR flux density limitation for a small percentage of time.

The consensus of opinion is that the excursions of CCIR violations are so short in duration that the measuring equipment that is located on the ground will never detect the short time violations.

It is our recommendation to not use the 255 PN sequence since any difficulty in achieving or staying locked in sync with this cover sequence will cause a large loss in data since the Reed/Solomon code with pseudo interleaving will be lost for at least a full segment if not for a full packet.

TASK C: Analyze requirements for a very low bit error rate (BER) for scientific data (typically approaching a BER of 10^{-7}) in comparison to data sources with higher redundancy such as voice or housekeeping telemetry.

A review of correspondence from scientific experimenters point out the very definite need for extremely low BER for some experiments. In particular for experiments that count very rare occurrence events (such as high energy particles) the data most likely will consist of zeroes with counts occurring at less than 1 in 10^5 . As a result the experiment would suffer drastically if protection against the BER is that quoted for TDRSS to White Sands (10^{-5}). The interested reader is referred to correspondence from Dr. Edward J. Groth (Princeton University) to Dr. David S. Leckrone of NASA/GSFC, January 6, 1978. Another reference of interest is a correspondence to Mr. George M. Levin, ST Science and Operations Project Manager from Dr. David S. Leckrone of NASA/GSFC which summarizes several PI estimates of the maximum uncorrected BER which would correspond to an acceptably small degradation of their scientific data.

A summary of this correspondence indicates that a BER as high as 2.5×10^{-5} would be the maximum limit acceptable and even at that several experiments would be seriously impacted. An error rate of 10^{-7} is highly preferred.

For this reason a Reed/Solomon encoder and interleaver has been added to the science data communication system (Section 2.A.2.c). In the September-November 1979 monthly report the advisability of this additional encoding was pointed out by these investigators and

Section 3.A bounds the overall concatenated code performance.

However repeated requests to increase the interleaver depth of the Reed/Solomon interleaver have repeatedly been discouraged by these investigators for reasons explained in detail in the May 1980 monthly report.

TASK D: Analyze recommendations for various coding and communications techniques as follows:

- Coding and communication of scientific data at the instrument.
- Coding and interleaving data in the central management system.
- Incorporating spread spectrum techniques on the downlink to meet CCIR flux density requirement.

In a memorandum to Mr. Jim Atherton (September 4, 1979), then technical monitor for this contract, a discussion of a method of providing each scientific investigator with a 31,26 BCH code that would increase the performance figure from .9993502031 for average correct transmission of a 26 bit word (16 bits data plus 8 bits mode information) to a figure of .99999971 average correct transmission of a 31 bit word (the original 26 bit word plus 5 bit parity checks) was presented. This would drop the average BER from an assumed 2.5×10^{-5} BER to a much better figure of 9.678×10^{-9} BER. In this manner individual investigators would achieve excellent BER performance with essentially a zero overhead addition to the system as a whole and an overhead of 19% for the individual investigator.

The coding and interleaving data in the central management system has been addressed via the decision to add the Reed/Solomon encoder with depth 8 R/S symbol interleaver, Section 2.A.2.c and Section 3.A. These investigators participated in the design review meeting at NASA/GSFC, September 25, 1979, concerning this decision which was recommended by many personnel involved in the project, these investigators being among those in favor of the additional encoding in view of the overall system constraints.

The monthly report of April 1980 includes an analysis of the expected system performance for the SSA based upon several variables of RFI. This analysis includes the latest specifications from the TDRSS Users Guide and the most up to date SSA system configurations.

The system performance after system synchronization lockup should be better than 10^{-10} with the exception of the heavy RFI periods during which no transmission is to be allowed.

Recommendation concerning the spectrum spreading techniques on the down link to meet the CCIR flux density requirement has been discussed orally and will be mentioned in the comprehensive report to follow. *Our recommendation is to delete the 255 code.* For one thing, it is not a true spectrum spreading operation since no additional bandwidth is utilized and the Lockheed analysis points out possible CCIR violations with or without the 255 sequence, Section 2.A.2.b. A glitch in the sequence will create a loss of a minimum of a full segment of R/S data and so it appears to gain nothing to use the 255 PN code.

TASK E: Evaluate the overall impact of frame synchronization loss effect on total data loss pursuant to recovery from an error in decoding as applied to the PN sequence and deinterleaving.

This task is addressed in the report in Section 3.B.c and in a memorandum to Mr. Jim Atherton (October 8, 1979) as well as the October 1979 and November 1979 monthly reports. The bottom line is that an error in decoding created by a PN sequence slip (either the 30 bit or the 255 bit) will create a condition that calls for synch state search as mentioned in the November 1979 report. At the best, this will cause a data loss of a minimum of 200 bits per state searched for the 30 bit PN sequence and an average estimate of 2,000 bits (600 absolute minimum if only 3 states searched) of erroneous data which would effectively eliminate that block of R/S data of approximately 16,320 bits (remember the R/S can decode no more than 505 bits in error or some special cases of 512 bits in error).

As pointed out in the May 1980 monthly report increasing the interleaver depth of the Reed/Solomon interleaver would make the problem even worse with no apparent gain to be achieved with an interleaver depth.

If a 255 PN sequence error is made it goes without saying that frame sync will suffer and a block of R/S data will be lost.

Furthermore, a bit slip occurrence will create a large data loss as was analyzed in the November 1979 report as well as in the May 1980 report. In fact the average BER due to Bit Slip alone (assuming a bit synchronizer bit slip probability of 10^{-11}) is approximately 4.58825×10^{-7} .

TASK F: Investigate methods to improve science data error control encoding to improve the error characteristic to one part in ten to the seventh (10^{-7}) BER through techniques for implementing the length of code to be used, and practicality of various types of decodings.

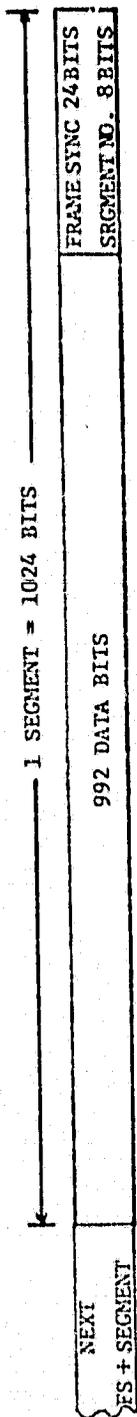
This task has been addressed indirectly throughout the course of the contract. Directly the recommendations for adding the outer code (the Reed/Solomon code with interleaving) and a proposed offering of a coding method for individual scientific investigators (memorandum to Mr. Jim Atherton, EF-22-J, September 4, 1979) concerns the improvement of the science data error control encoding. At present it is believed the system should work well even in the face of medium RFI (see the April and May 1980 monthly reports for a description and definition of RFI).

During the performance of this contract many telephone conversations were held with many contractors and subcontractors to attempt to provide a cohesive liaison between the various groups working on the Space Telescope System. Perhaps this has been one of the most important contributions of this contract effort. All calls have been documented in the monthly reports.

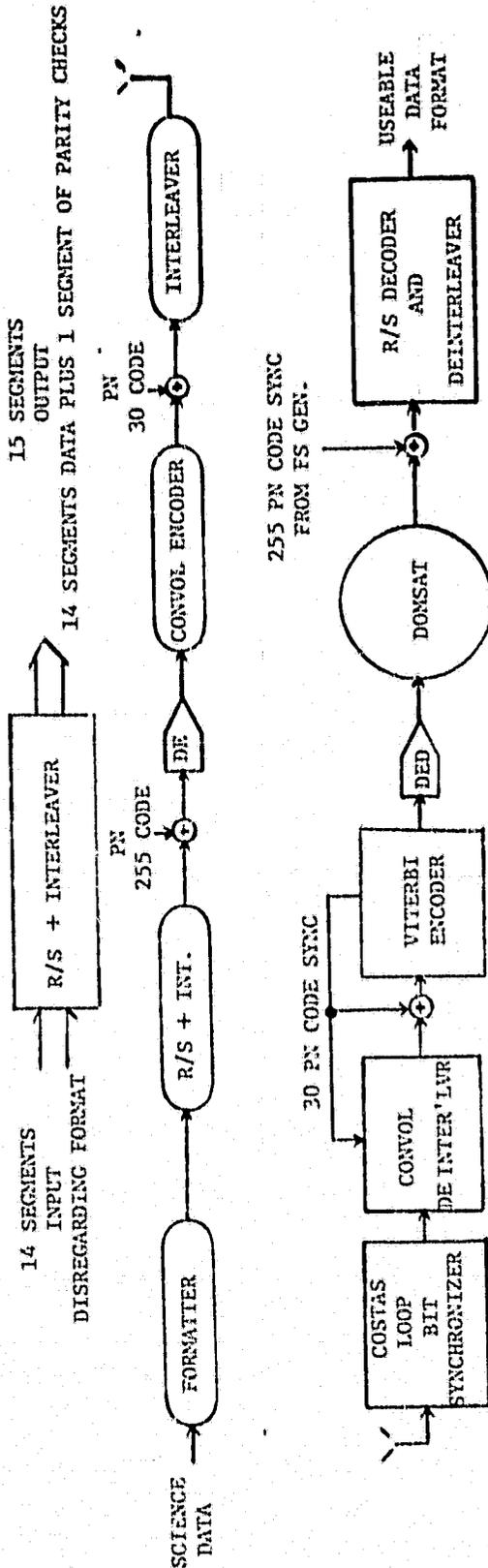
Much analysis remains to be done in connection with the Space Telescope System especially in view of the budget cuts that have been imposed.

The following points are particularly in need of further work:

- The effects of reduced data flow if the tape recorders are eliminated from the system must be carefully weighed against the cost.
- It appears from comments by Mr. R. Goddfry (NASA/GSFC) that bit jitter could be much worse than originally conceived. How this will effect the bit synchronizer bit slip probability must be considered since one of the most serious data loss situations occurs if a bit slip occurs. The data stream should be analyzed to determine the expected transition density. This knowledge will allow a worse case bit jitter to be specified, or correspondingly allow an estimate of bit slip probability to be determined.
- The command up-link should be studied. At present it appears that no commands may be sent from the ground during the heavy RFI periods. This is undesirable and perhaps unnecessary.
- The portion of the telemetry link from White Sands to GSFC via DOMSAT has been an enigma due to lack of documentation. We are at present awaiting release and receipt of the DOMSAT SRI final report.
- The 255 bit PN sequence for CCIR should be analyzed for data pattern sensitivity.
- The engineering data link should be analyzed. This link does not have sufficient error protection (in fact it is woefully weak in error protection). It is conceivable that some engineering data should be sent via the SSA link to give it better error protection.



1 segment contains 1 line of data from only 1 instrument
 16 segments or less equal 1 packet
 1 packet is from 1 instrument only in normal format
 However 1 packet can contain lines of data from up to 2 instruments



DE = Differential Encoder
 DED = Differential Decoder
 R/S+INT. = Reed/Solomon Encoder and Interleaver

Figure vi.1 Data Format and Multiple Sync Points

CHAPTER 1

INTRODUCTION

1.A Command Function and Forward (Goddard to Spacecraft) Communication Link

The Space Telescope System's primary objective is to develop and operate a large, high-quality optical telescope in low earth orbit and to provide an astronomical laboratory capability beyond the reach of earth based observatories. The Space Telescope System consists of the Space Telescope Orbiting Observatory (ST), the Space Telescope Science Institute (ST ScI), and the Space Telescope Operations Control Center (STOCC). The Space Telescope System, Figure 1.1, will be supported by the Space Shuttle, the Tracking and Delay Relay Satellite System (TDRSS), and the NASA Communications Network (NASCOM). The remainder of this section is a summary of the end-to-end ST data system.

The objective is to provide a brief description of the major ST data originators and/or recipients and to show aspects of the system that interact with the data. The intent is to illustrate how the data is generated, how it is related to the ST system and to explain pertinent data manipulations and unique ST characteristics that influence the system.

The planning and scheduling of ST missions is the responsibility of the ST ScI and the STOCC. The ST ScI primary function is to evaluate and select proposals from the scientific community and implement the selected proposals into a monthly science plan based

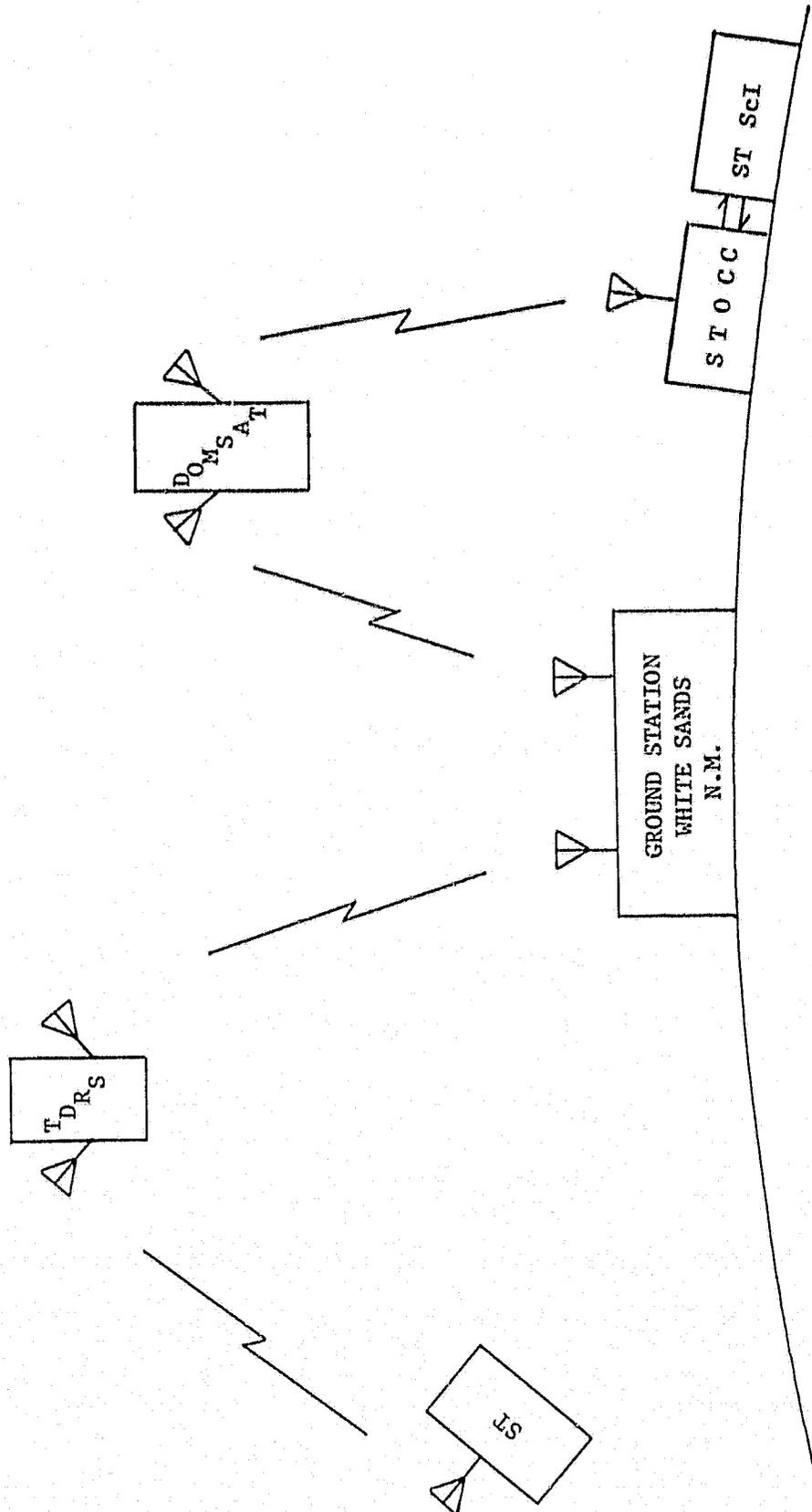


Figure 1.1 The Space Telescope System

on various constraints to receive maximum utilization of the ST. This monthly science plan is sent to STOCC where it is converted into orbit-by-orbit sequences. The STOCC is the primary and central controlling facility for performing ST mission operations.

The execution of the desired scientific observation and the operations required to maintain the ST are accomplished by the command function. The command function includes the generation, loading, verification, and execution of both real-time and stored program commands. The STOCC is responsible for the issuing of both science related commands from the daily science schedule and spacecraft related commands.

Commands are generated by the Command Management System. This system consists of off-line routines which provide for the generation of planned real-time and stored program commands, software updates to the DF 244 and NSSCI computers, and data updates. The scheduled uplinks to the ST are formatted into 48 bit command words in the off-line system. The first seven bits are the spacecraft address and the last seven bits are an error protection Hamming code which is inserted prior to transmission by the on-line system. Uplinks are assembled as single commands or in blocks up to 256 words each, Figure 1.2 The single commands are real-time, and the blocks are stored program load or data updates. The first word in each block provides memory starting address and block length for stored program commands and software updates. A data block or table number is used to replace memory locations in data updates. The ground-computed checksum is contained in the last word of each block.

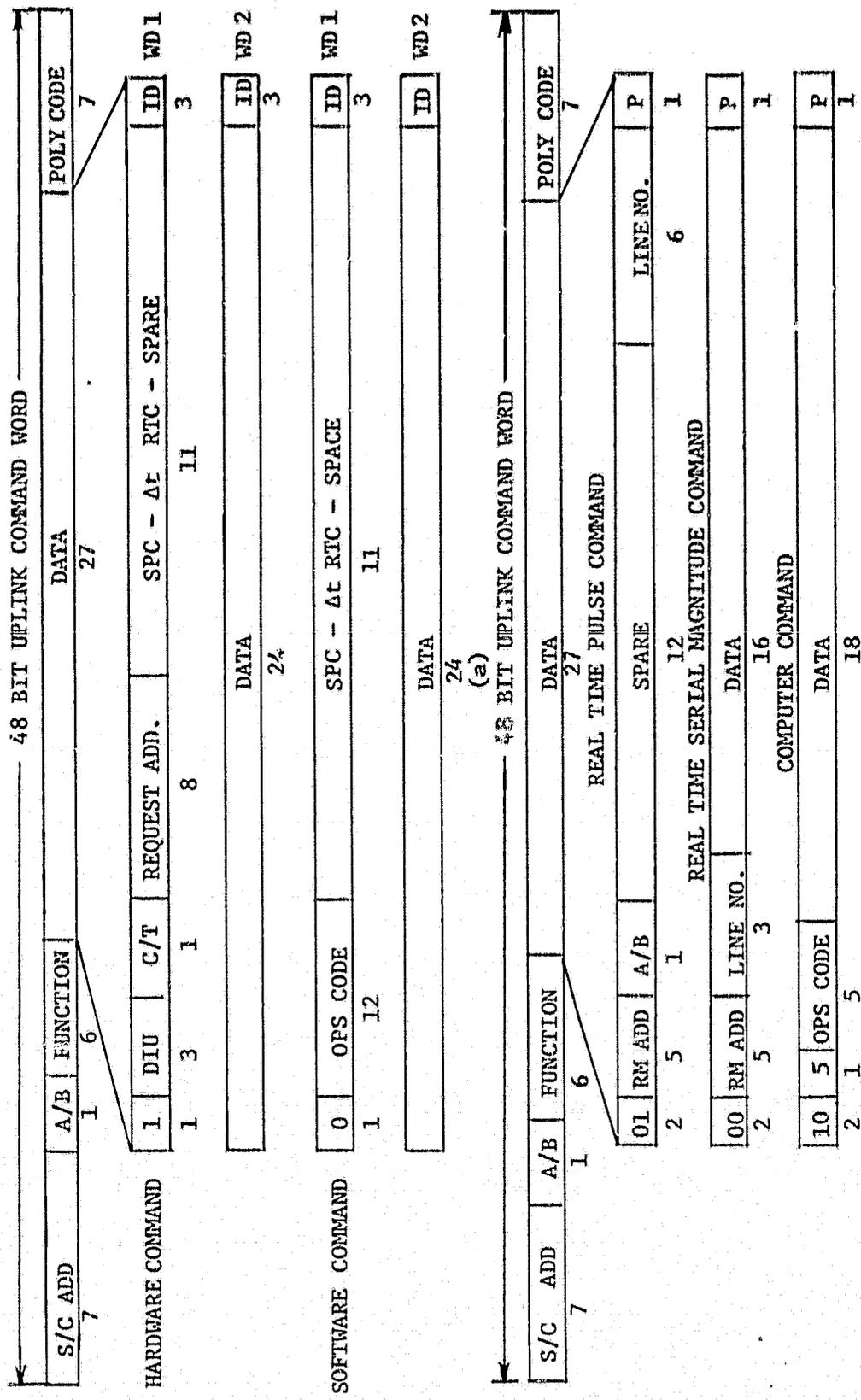


Figure 1.2 Command Formats a) DMS and b) SI CSDH

Each uplink is preceded by an acquisition sequence at 0.125 Kbps or 1.0 Kbps generated by the transponder command detector unit. Each command block is preceded by a 48-bit Command Data Interface (CDI) synchronization word. The standard 4800-bit NASCOM block format is used for all command words. Once up-link lock and data synchronization has been established, the CDI decodes the Hamming code, performs a valid bit count on each command word, decodes the address, and routes valid commands. Special commands are routed directly to the designated recipient. All other commands are routed to the Data Management Subsystem (DMS) for distribution. The commands for the Support System Module (SSM) are transmitted to the DF 224 computer and the Scientific Instruments Control and Data Handling (SI C&DH) system commands are transmitted to the Control Unit/Science Data Formatter (CU/SDF). Stored program commands are stored in temporary buffer until the last word in a block is received and then the entire block is transferred to memory.

Control and routing of commands is handled by the DMS. The DMS outputs commands via a Data Interface Unit (DIU) to the users or for special commands direct from DMS decoder to user. A 27-bit serial magnitude command interface is used to route SI C&DH commands to the CU/SDF. Real-time commands are received at either a 20.83 or 2.60 per second rate.

1.B Data Function

1.B.1 Engineering Data

All ST data is routed to the Support System Module (SSM)

where it is collected, recorded and/or transmitted to the STOCC. The data originating in the ST are grouped into two categories, engineering data and science data. Engineering data contains information on the performance and functional operation of the ST elements. Engineering data from the Scientific Instruments (SI) and the SI C&DH are collected by the CU/SDF and routed to the DIU as a composite data stream. Engineering data is routed to the Data Management Unit (DMU) via DIU. The SSM and the Optical Telescope Assemble (OTA) engineering data are combined with the SI and SI C&DH engineering data to form the composite ST engineering data rates of 0.5, 4.0, 8.0, or 32 Kbps.

The DMU arranges the data into major frames which consist of 120 or 20 minor frames. Each minor frame contains either 250 or 125 eight bit words and a 24-bit frame synchronization word. The DMU is capable of collecting and formatting the data in one of the five formats, three of which are programmable by software control and two of which are fixed by hardware control. The data are transferred to the Multiple Access (MA) system for real-time transmittal to the STOCC or to the engineering tape recorder for later transmission. The 0.5 Kbps data rate is utilized for real-time transmission only.

1.B.2 Science Data

The science data contains the observational output of one or more of the five scientific instruments (SI). The science data is routed directly from the SI or from the NASA

Standard Spacecraft Computer, Model I (NSSCI) to the DMU via the CU/SDF. The CU/SDF collects and formats the data into segments of 1024 bits. Each segment contains a 24 bit synchronization pattern, an 8 bit segment number and a 16 bit packet count. These segments are grouped into packets, each packet contains the ancillary identification information. Normally a packet contains a complete line of science data from only one SI, however, packets from two different SI may be combined and transferred to the DMU as a composite science data stream. The CU/SDF contains a Reed/Solomon (R/S) encoder which is utilized to concatenate an outer error correcting code with the science data. The R/S encoder is constructed in such a manner that the data word parity checks are interleaved, although the information words themselves are sent unaltered. The R/S encoder is utilized to give immunity to TDRSS channel degradation and to protect against burst errors. The science data are transferred to the DMU at a 4.0, 32.0, or 1024 Kbps rate for transmission in real-time to STOCC and/or recording for later transmission. The 4.0 Kbps data rate utilizes the MA system and the 1.024 Mbps utilizes the S-band Single-Access (SSA) system for real-time transmission. The 32.0 Kbps data rate is for tape recording only.

The DMU is a component of the Data Management System (DMS). The DMS, also, includes three identical magnetic tape recorders. One is allocated to the engineering data and one to the science data with the third as a spare, which may be deleted. The tape recorders are capable of recording data

at rates of 32.0, 64.0 or 1024 Kbps. The science data and engineering data rates of 4.0 and 8.0 Kbps are upconverted to 32.0 and 64.0 Kbps respectively by an 8 bit pattern, prior to being recorded. Data rates of 32.0 and 1024 Kbps are recorded at their data rates. All data rates are played back at a 1.024 Mbps rate and in reverse. The tape is not rewound prior to playback, creating a need for a reversible sync pattern on the tape.

1.C Return Communication Links

All ST data are transmitted to STOCG via the TDRSS and NASCOM utilizing the MA and SSA systems. Figure 1.3 illustrates the end-to-end ST data transmission flow. The MA system is utilized to transmit real-time engineering data at 0.5, 4.0, 8.0, or 32.0 Kbps and science data at 4.0 Kbps. Except for the 0.5 Kbps data rate, the data are transmitted to the TDRSS utilizing the transmitter portion of the transponder via the high gain antenna (HGA) system. The 0.5 Kbps data rate is transmitted in the same way except via either the HGA or the low gain antenna (LGA) system. The MA return link utilizes two simultaneous, independent channels employing spread spectrum techniques. Each channel is 1/2 convolutionally encoded and modulo-2 added to a PN code, which is unique for the ST, prior to modulating quadrature phases of a 2287.5 MHz 5 watt RF carrier. Either the In-phase (I) or the Quadrature-phase (Q) channel may be used to transmit engineering data at one of the above rates or both channel at the same rate. Only the I channel may be used to transmit the 4.0 Kbps science

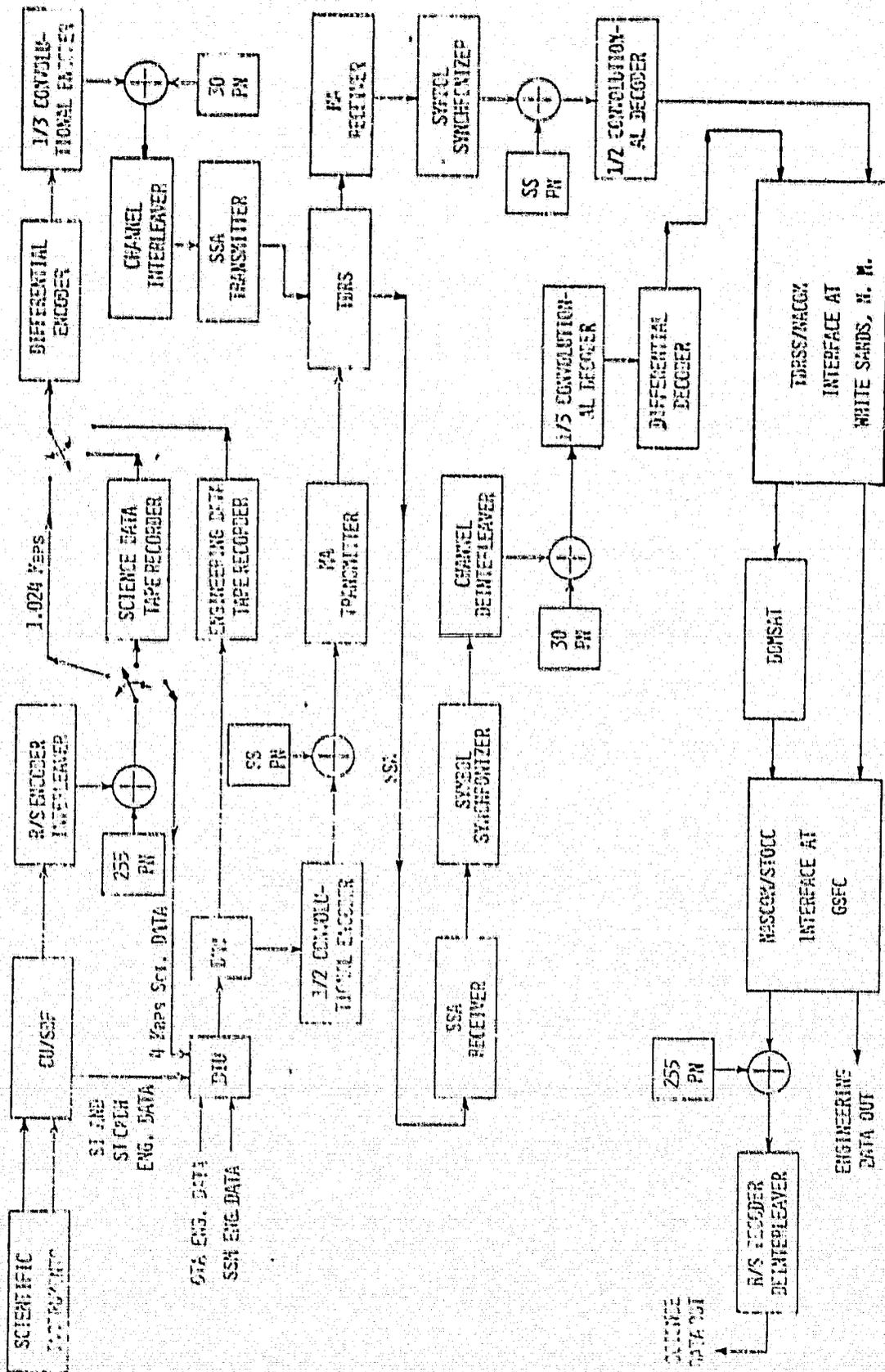


Figure 1.3 ST Data Transmission Flow

data. The data is despread, bit synchronized, and convolutionally decoded by the TDRSS ground station at White Sands, N.M. The ground station also provides individual bit-contiguous data streams at the MA transmitter input rate to NASCOM.

The SSA system is utilized to transmit real-time Reed/Solomon Encoded science data at 1.024 MBps and playback tape recorder data, both engineering and science, to the TDRSS via HGA system. The data are differentially encoded, 1/3 rate convolutionally encoded, PN coded, and optimally periodic convolutionally interleaved during high RFI periods prior to BPSK modulating a 2255.5 MHz 14 watt RF carrier. The data stream is demodulated, bit synchronized, periodic convolutionally deinterleaved, and Viterbi decoded by the TDRSS ground station. The ground station provides an individual bit contiguous data stream at the SSA transmitter input rate to NASCOM.

The NASCOM terminal accepts the bit-contiguous data stream, formats the data into discrete 4800-bit NASCOM blocks. The 4800-bit blocks are time division multiplexed with other data blocks for transmission to Goddard Space Flight Center (GSFC) via common carrier. Prior to transmission each block is appended with an error detection code. The blocks of data are demultiplexed and checked for transmission errors at the GSFC terminal. The data blocks are then routed to the STOCC. The SSA system will utilize the Domestic-Communication Satellite (DOMSAT).

The Space Telescope System must provide a bit error rate (BER) of one error in 10^6 bits on the SSA system to obtain most of its main

objectives for the current complement of SI's per Dr. D. S. Leckrone's memo of Jan. 26, 1978 to Mr. G. M. Levin. However, a BER of 10^{-7} for the SSA system is highly preferred and is more consistent with the inherent quality of the SI data (reference 20). A BER of 2.5×10^{-5} is acceptable for engineering data. The TDRSS will provide a Western Union guaranteed BER of 10^{-5} provided that the required effective isotropic radiated power (EIRP), measured in dBW, and the signal structure conditions are met by the user's signal. Obviously this does not satisfy the desired BER for the SSA system. The DOMSAT Link will provide a BER of 10^{-7} . Under these conditions, the DOMSAT Link will be viewed as transparent adding no additional noise to the TDRSS BER of 10^{-5} .

The next section is a more comprehensive description of the SSA system. This section will discuss in detail the portion of the SSA system on board the ST, the channel characteristics, and the expected overall system performance.

CHAPTER 2

THE SPACE TELESCOPE S-BAND SINGLE-ACCESS SYSTEM

The objective of this section is to provide a more in-depth view of the SSA system. The SSA system may be separated into three main subgroups for discussion purposes: The ST, the return link from the ST via TDRSS to White Sands, and from White Sands via DOMSAT to the STOCC at GSFC. The ST is presently in the design and fabrication stage and is scheduled to be operational in the early part of Fall of 1983. The TDRSS is in a similar situation; its operation date was originally November of 1980 but the date has been delayed to 1981. Therefore several assumptions concerning the SSA system must be made. These assumptions are described in the following paragraphs and listed at the end of this section.

2.A Space Telescope Orbiting Observatory

First, the portion of the SSA system which is contained on board the ST will be discussed. This portion consists of the following main groups:

- (1) Support System Module (SSM)
- (2) Scientific Instrument Control and Data Handling (SI C&DH)
- (3) Scientific Instruments (SI)

Only the portions of these main groups which pertain to the SSA system will be discussed. Further information concerning overall ST may be found in reference 1.

2.A.1 Scientific Instruments

This section will consist mainly of tracing the flow of science data through the ST, Figure 2.1. The science data originates from one of the scientific instruments (SI). The original complement of SI's consist of two imagery cameras, two spectrographs, a photometer and one of the three Fine Guidance Sensors (FGS). Each of the SI's has its own data format and data rate, but the format must be compatible with the science data format generated by the Control Unit/Science Data Formatter (CU/SDF). The data for the SI's are considered to be digitized data for this reason. All science data from the SI's are routed to the Control Unit/Science Data Formatter (CU/SDF) component of the Scientific Instrument Control and Data Handling (SI C&DH) group via dedicated six-signal interfaces.

2.A.2 Control Unit/Science Data Formatter

The SI C&DH is the interface between the SI's and the Support System Module (SSM). The SI C&DH receives, decodes, and stores and/or routes commands for the various SI's. The SI C&DH collects engineering and science data from the SI, processes this data, and transfers it to the SSM. Processing for the science data includes formatting suitable for transmission and adding the outer error correcting code. The SI C&DH provides a general computing capability to support SI control, monitoring, and data manipulation/ analysis. The SI C&DH includes the following components:

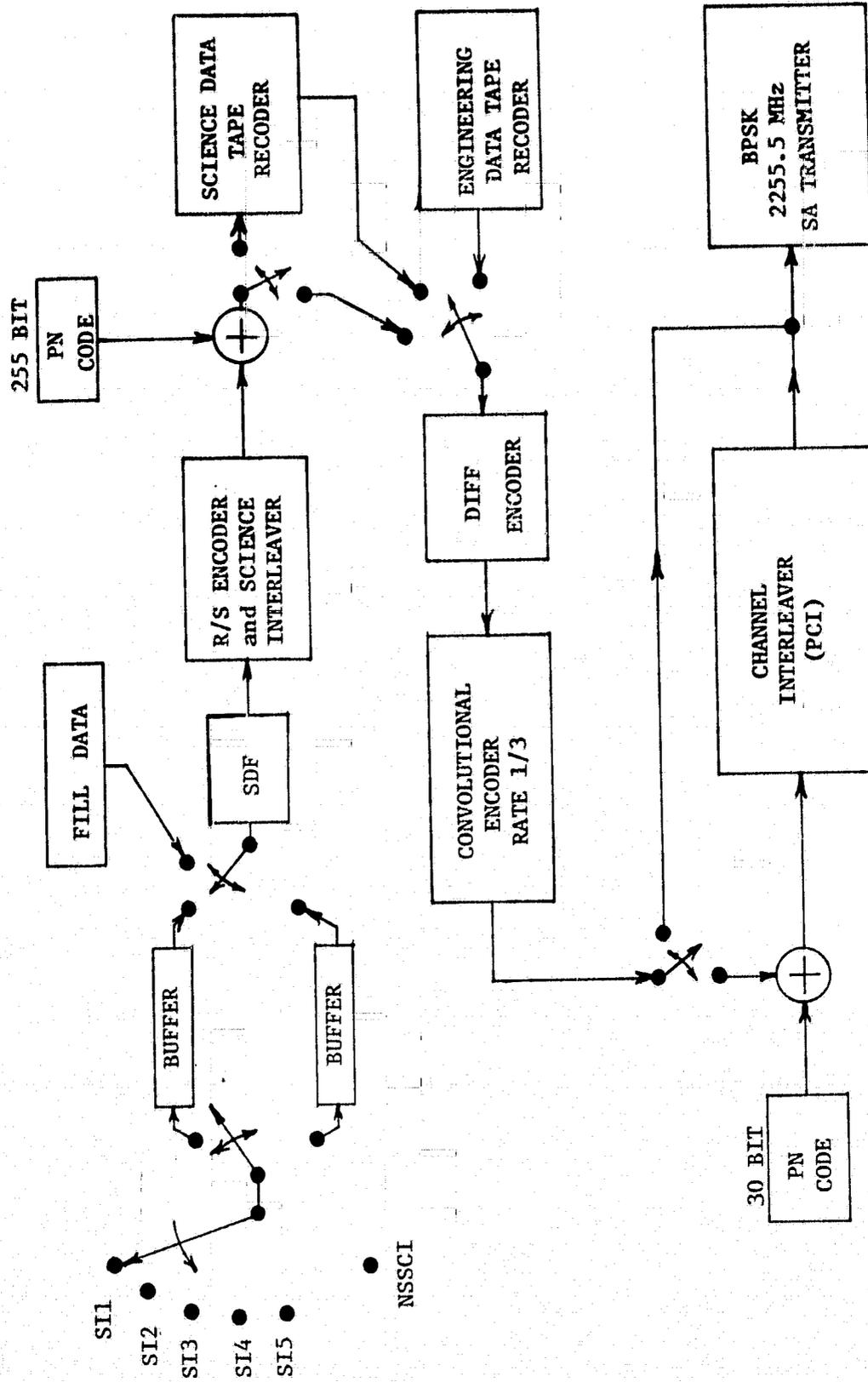


Figure 2.1a Science Data Flow Through the ST

SPACE TELESCOPE UNIT
ENCODING SUMMARY
SCIENCE DATA

This code is used to protect against errors during RFI periods
Code Properties: 1912 Information Data Bits

R/S ENCODING
AND
INTERLEAVING

+
128 Check Bits = 1 R/S Word of 2040 Bits Lengths
Overhead = $\frac{128}{1912} = 6.6945605\%$

Error Protection: In a block of 16,320 bits (containing 1024 parity check bits) any burst of 505 bits is corrected.
Problems: Any 16,320 bit block with more than 505 (512 for some special error patterns) will be decoded erroneously.

DIFFERENTIAL
ENCODING

This code provides no Error Protection.
Rather this code solves the problem of phase ambiguity of suppressed carrier coherent reception in the receiver. One problem: For an error in, two errors are emitted.

CONVOLUTIONAL
ENCODING
RATE 1/3

This code provides error protection.
Code properties: 1 Bit in Yields 3 bit outs, for an overhead of 200%
With interleaving, no group of 30 symbols will be closer than 119 symbols.
Thus, a burst of 30 symbols will be decoded correctly. With a free distance of 14 this code (without interleaving) can typically correct 6-7 errors per decoder block of 100 bits. (Assuming decoder constraint length of 5 times encoder constraint length).
Problems: Emits bursts of errors when decoder is faced with too many input errors.

PN
CODE

This code is used for synch purposes and does not add error protection.

Figure 2.1b Encoding Summary for the Science Data

- 1) Control Unit/Science Data Formatter (CU/SDF)
- 2) Multiplexed Data Bus (MDB)
- 3) Bus Coupler Unit (BCU)
- 4) Remote Module (RM)
- 5) Standard Interface for Computer (STINT)
- 6) NASA Standard Spacecraft Computer, Model I (NSSCI)
- 7) Power Control Unit (PCU)

The Control Unit/Science Data Formatter (CU/SDF) is the main hub of the SI C&DH. The CU/SDF receives, processes, and transfers commands, clock and synchronization signals from the SSM to all SI's and the NSSCI. The CU/SDF processes all communication between SSM, SI's and the NSSCI. It receives science data from the SI via the six-signal interfaces or science data, data logs, and NSSCI memory dumps from the NSSCI via STINT; formats into packets; Reed/Solomon encodes and adds a PN sequence; transferring the processed data to the SSM via a two-signal interface with the SSM. Flags in the SSM Processor Interface Table (PIT) are conditioned to indicate whether the SSM is ready to accept the data and whether the data is to be recorded or transmitted. At this point a more detailed discussion of the functions performed by the CU/SDF is required.

2.A.2.a Science Data Formatter

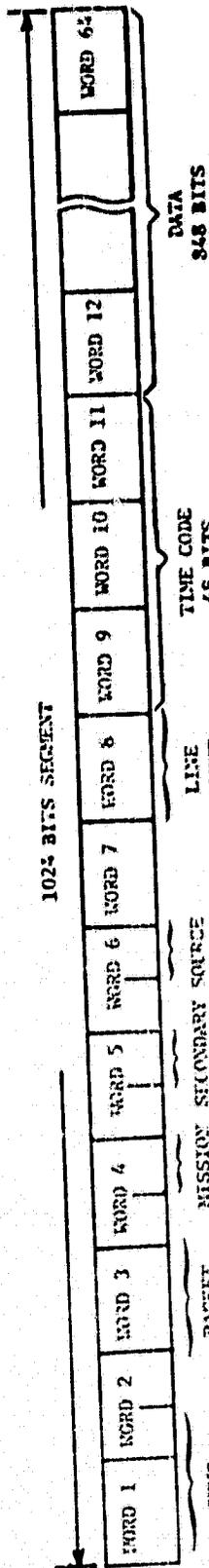
The CU/SDF receives science data from a SI in 16-bit words with the MSB first. The CU/SDF organizes the data

words into segments of sixty-four 16-bit words. The segments are in turn organized into a data packet consisting of one to sixteen segments. A packet contains a complete line of science data from only one SI. Fill data is used to complete the remaining portion of the last segment in the packet if required. The nature of the fill data has not been determined, but it may be an alternate '1', '0' sequence. Figure 2.2 illustrates a general data packet format. Packets from two different SI's may be combined and transmitted as a composite science data stream. If no science data are available, packets of dummy data are used to maintain the link.

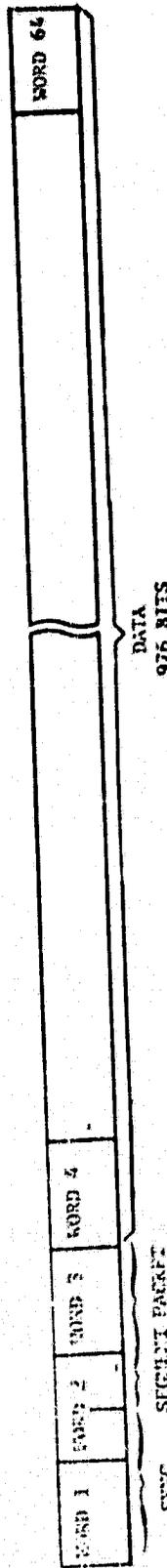
The CU/SDF is capable of transmitting science data from all five SI concurrently to either the SSM or the NSSCI. The science data from a particular SI may be routed to either the SSM or the NSSCI but not both simultaneously.

The NSSCI may receive and transmit data concurrently. Science data routed to the NSSCI is not processed through the SDF.

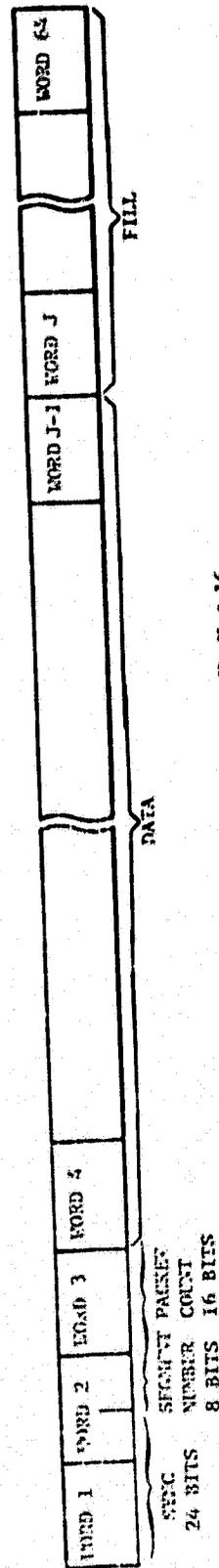
The CU/SDF transmits a continuous data stream to the SSM on command at one of the three science data rates. The CU/SDF will continue to transmit until a stop command is received. The science data are multiplexed by lines, organized into packets, R/S encoded/ interleaved, and randomized prior to transmission to the SSM. The



(a) Data Format For Segment 1



(b) Data Format For Segments 2 Thru N-1



(c) Data Format For Segment N, $N \leq 16$

Figure 2.2 General Packet Format for ST Science Data

continuous data stream is accomplished by utilizing a fill data packet when science data is unavailable. The fill data packet consists of 64 words and employs the segment one format with a fixed data pattern which is stored in memory.

The SDF utilizes two buffers to receive data from the five SI and NSSCI. These buffers accept data at various rates up to 1.024 Mbps. The read in rate is controlled by the individual sources (SI or NSSCI) and varies with the particular source. The rate at which data are read out of the buffers is controlled by the CU/SDF and is independent of the read in rate. A science data line consisting of up to 968 sixteen bit words is read in by one of the buffers. Once this buffer is filled, the SDF begins to read out the data from this buffer and organize the data into a packet consisting of one to sixteen 64 word segments. Meanwhile, a second data line is being read in by the other buffer. This second data line may originate from another source with a different data rate or from the same source at the same rate if a second source is unavailable. Since the SDF processes data at the commanded data rate, independent of the source data rate, there may be no data forthcoming from either buffer. Should this occur the fill data packet would be employed to maintain the continuous data stream.

The SDF output data is routed to the R/S encoder/interleaver. The R/S consider the incoming data stream as a succession of segments disregarding the packet structure. The R/S accepts 14 segments and generates a segment of 1024 check bits. The 14 data segments pass through the R/S undisturbed, except for a one bit delay. The 15th segment of check bits is read out following the last bit of the 14th segment of the present group and prior to the first bit of following group of 14 segments.

2.A.2.b 255 PN Encoder

The output of the R/S is modulo-2 added to the 255 PN sequence. The 255 PN sequence is generated at the same rate as the SDF data rate. The PN generator is reset to the all ones state at the beginning of each segment, including the check segment. Each segment except the check segment begins with a 24-bit sync pattern, which will be utilized to re-sync the PN generator on the ground (STOCC or ST ScI). One of the clock signals will be utilized to reset the ground PN generator to the all ones state at the beginning of the check segment.

The 255 PN sequence is employed to randomize data that may cause the output power spectrum to have too much power concentrated over too small a bandwidth in violation of the CCIR space-to-earth radiation limits. Lockheed utilized a computer simulation of the SSA system to determine the performance of the system with regards

to the CCIR limitations. Both 8-bit repeating and 8-bit random patterns were employed as input data to the SI C&DH. The Lockheed analysis indicated the CCIR limitations will be exceeded by 8 to 13 dB during 10% of the 4KHz sections, if the 255 PN coder is deleted from the system. The analysis also indicated that violation will occur for certain input sequence even when the 255 PN coder is utilized. The sequence is capable of by-passing the 255 PN coder on command. It is recommended by this author that the 255 PN sequence not be utilized due to potential data loss.

2.A.2.c Reed/Solomon Encoder/Interleaver

The Reed/Solomon (R/S) encoder/interleaver is utilized by the ST to improve the BER of the SSA, and has several unique qualities.

The R/S encoder/interleavers system appears to have an interleaver of length 8, but passes the science data format undisturbed. The system adds only an additional 1024 bits to the science data regardless of the packet length. The system uses less than 30 IC's and has a delay of only one bit. The R/S code has a block length of 16,320 bits with 1024 parity check bits. It will be able to correct any single error burst less than 505 bits per block without fail. It will not correct a burst greater than 513 bits per block. The ability to correct bursts between 505 and 513 bits per block will depend on the location of the burst within the block.

The system is capable of accepting information blocks of various bit lengths, ranging from a minimum of 64 bits to a maximum of 15,296 bits. The system will always contain 1024 check bits regardless of the number of information bits. The time required for decoding is independent of the number of information bits for this reason. Interleaving and coding is performed by the check bits which allow the information data format to remain unchanged by the R/S encoder. To understand the system one may visualize a matrix with eight columns of 8 bits each and 255 rows of 64 bits, (see Figure 2.3). Consider each column to be a separate Reed-Solomon coder, all eight codes use the same generator polynomial. The first 239 rows are reserved for information bits (science data), the last 16 rows are for the parity check bits. A science data block, consisting of up to 14 segments (14,336 bits or 896 sixteen bit words) is read into the matrix by rows and read out by rows. If the block contains less than 14 segments, the remaining bits are considered zeroes and divided between each of the eight R/S codes. These zeroes are not transmitted, the decoder will take care of the truncated data train. The science data packet may contain up to 16 segments, this is two more than the capacity of the R/S coder. In this event, the remaining segments will be consisted as part of the following packet by R/S coder.

8 COLUMNS
(8 bits per Column)

I ₆₄ ...I ₅₇	I ₄₈ ...I ₄₉	I ₄₀ ...I ₄₁	I ₃₂ ...I ₃₃	I ₂₄ ...I ₂₅	I ₁₆ ...I ₁₇	I ₈ ...I ₉	I ₁ ...I ₆₅
I ₁₂₈ ...I ₁₂₁	I ₁₁₂ ...I ₁₁₃	I ₁₀₄ ...I ₁₀₅	I ₉₆ ...I ₉₇	I ₈₈ ...I ₈₉	I ₈₀ ...I ₈₁	I ₇₂ ...I ₇₃	I ₆₅
.
.
.
I ₁₅ , 296 I							
P ₆₄ ...P ₅₇	P ₄₈ ...P ₄₉	P ₄₀ ...P ₄₁	P ₃₂ ...P ₃₃	P ₂₄ ...P ₂₅	P ₁₆ ...P ₁₇	P ₈ ...P ₉	P ₁ ...P ₆₅
P ₁₂₈ ...P ₁₂₁	P ₁₁₂ ...P ₁₁₃	P ₁₀₄ ...P ₁₀₅	P ₉₆ ...P ₉₇	P ₈₈ ...P ₈₉	P ₈₀ ...P ₈₁	P ₇₂ ...P ₇₃	P ₆₅
.
.
.
P ₁₀₂₄ ...P ₁₀₁₇							P ₉₆₈ ...P ₉₆₁

239 Rows
Reserved
for
Data

16 Rows
Check
Bits

255 Rows
64 bits
per Row

R/S Code 8
R/S Code 7
R/S Code 6
R/S Code 5
R/S Code 4
R/S Code 3
R/S Code 2
R/S Code 1

I_i - Information Bit P_i - Parity Check Bit

Figure 2.3 Matrix Visualization of the R/S Encoder

After the last row of information is read, the 16 rows of parity check bits are read out row by row. There will always be 1024 check bits regardless of the number of information bits. An example is given in Appendix A for clarification.

2.A.3 Support System Module

The data (science data plus R/S parity checks) is transferred to the SSM from the SI C&DH. The two subgroups of the SSM of interest are the Instrumentation and Communications Subsystem (I&C) and the Data Management Subsystem (DMS). The DMS will be discussed first since this is the point at which the data will enter the SSM.

2.A.3.a Data Management Subsystem

The DMS is responsible for providing the acquisition, processing, storage, and dissemination of all data, including engineering data between the SI communications and other subsystems. The DMS consists of the following components:

1. Data Management Unit (DMU)
2. DF 244 Computer
3. Command Data Interface (CDI)
4. Tape Recorders
5. Master Oscillator
6. Data Interface Unit (DIU)

(a) Data Management Unit

The DMU receives the data and clock signals from the SI C&DH at rates of 4.0, 32.0, or 1024 Kbps and routes the signals to the science tape recorder and/or the I&C for transmission. The 32.0 Kbps data rate is routed to the science tape recorder only. The 4.0 Kbps data rate is routed to the MA system for transmission to the ground in real-time, or it is up-converted to 32.0 Kbps and routed to the science tape recorder to be stored for transmission via the SSA system at a later time. The 1.024 Mbps data rate is routed either to the science tape recorder for direct recording for later transmission via the SSA system, or processed for real-time transmission via the SSA system.

The tape recorders, science and engineering, are played back at the 1.024 Mbps data rate only, regardless of the record rate. For this reason, the playback engineering data will be included in the discussion of the SSA system.

The 1.024 Mbps data rate whether playback engineering data, playback or real-time science data is processed by the DMU prior to transmission to the I&C. The signal processing function includes a differential encoder, 1/3 rate convolutional

encoder, a PN encoder, and a periodic convolutional interleaver.

(b) Tape Recorders

The DMS includes three identical tape recorders, one for the engineering and one for the science data, and one spare; which may be deleted. Both engineering and science data may be stored by any one tape record should the need arise.

Each of the three Engineering/Science Tape Recorders (ESTR) contains 2000 feet of tape, has a maximum record/playback speed of 41 inches per second, and requires 30 seconds to reach this speed when used for 1.024 Mbps rate data. Each has a recording density of 25 K bits per inch. The ESTR will be recorded at one of three rates, 32, 64, or 1024 Kbps. All recorded data is read out at a 1.024 Mbps rate only and in reverse, the tape is not rewound prior to read out. The reverse read out creates several problems. These problems are discussed in the following paragraph.

The ESTR will not accept data for recording until lock-on speed has been achieved and acknowledged by the tape. The time interval required to achieve lock-on will depend on the record rate used. The tape run during this time is referred to as the preamble. The preamble will vary in length

directly with the record rate assuming linear acceleration, 5 feet of preamble is required for the 1.024 Mbps rate. The reverse play back of all recorded data at 1.024 Mbps rate requires 5 feet of preamble and post-amble per input data stream to the ESTR. The 5 feet of post/preamble has not been incorporated into the system to date.

The Engineering/Science Tape Recorder (ESTR) accepts data rates of 4.0, 8.0, 32.0 and 1024 Kbps. Prior to recording the 4.0 and 8.0 Kbps data rates are upconverted by an 8-bit sequence to 32 and 64 Kbps rates respectively. In addition, the NRZ-L input format is converted to a Delay Modulation or Miller complement code for the purpose of improving the high density digital recording process. This conversion results in a phase ambiguity condition which results in logic states being inadvertently complemented (i.e. '1' becomes '0' and vice versa) when the data is converted back to NRZ-L prior to being read out of the ESTR. A brief discussion on Delay Modulation is included in Appendix B. The problem is compounded by the fact the read out is in reverse, the recorder is not rewound prior to playback.

Normally a specific 5 bit pattern is required to resolve the phase ambiguity, but the manufacturer of the ESTR has made internal alternation to

the units enabling a 3-bit pattern (010) to accomplish the same results. This represents a major accomplishment. Since a specific 3-bit pattern has a much higher probability of occurring naturally in the data than a specific 5-bit pattern.

Recorded data input interrupts, as well as dropouts caused by tape defects, will cause the phase ambiguity condition which will degrade the BER performance. The 3 bit pattern (010) is required to rephase the data. Each input data stream to the recorder must be preceded and followed by this 3 bit pattern. The manufacturer of the ESTR recommends 3 to 5 inches of tape between the data and both post preamble be stuffed with this 3 bit pattern to assure the correct phase for the data. They also recommend the 3 bit pattern occur periodically within the data to assure the proper phase in the event of a tape defect.

(c) Differential Encoder

The SSA system utilizes a suppressed carrier modulation/coherent carrier recovery technique, which results in a phase ambiguity problem similar to the one previously discussed. The squaring operation in a coherent carrier recovery loop acting on a suppressed carrier results in either of

two stable phase states. The results being a possible logical inversion of the output data stream. This inversion will cause extremely long error bursts, which will be beyond the error correcting capability of the R/S. The differential encoder is utilized by the DMU to solve the ambiguity. Figure 2.4 is a schematic of a typical differential encoder. The price paid for utilizing a differential encoder is that errors occur in pairs. A single error into the differential decoder results in two errors out.

(d) Convolutional Encoder

The 1/3 rate convolutional encoder, the channel interleaver, and 30 PN encoder are required to meet the constraints placed on the ST by the TDRSS. They are utilized to combat the RFI problem, returning the TDRSS channel BER to 1×10^{-5} . The 1/3 rate convolutional encoder outputs 3 symbols for 1 symbol in and has constraint length 7. Figure 2.5 shows a block diagram of the encoder. The diagram also shows that every other output symbol is inverted. This will aid the ground system with bit synchronization.

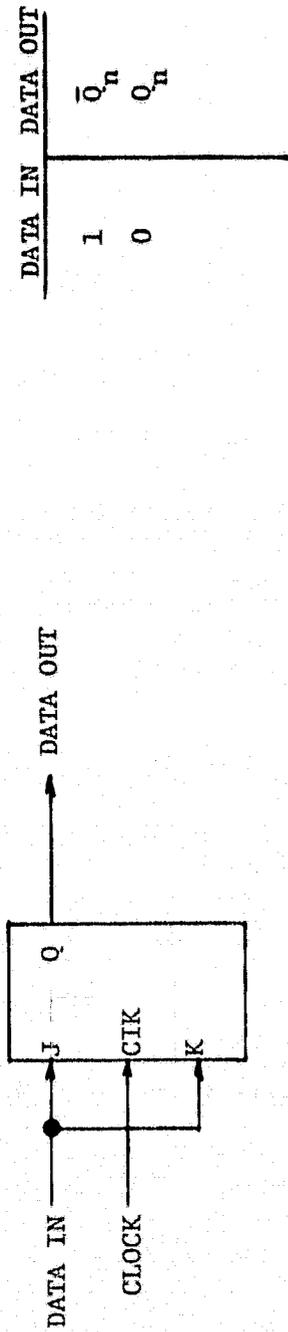
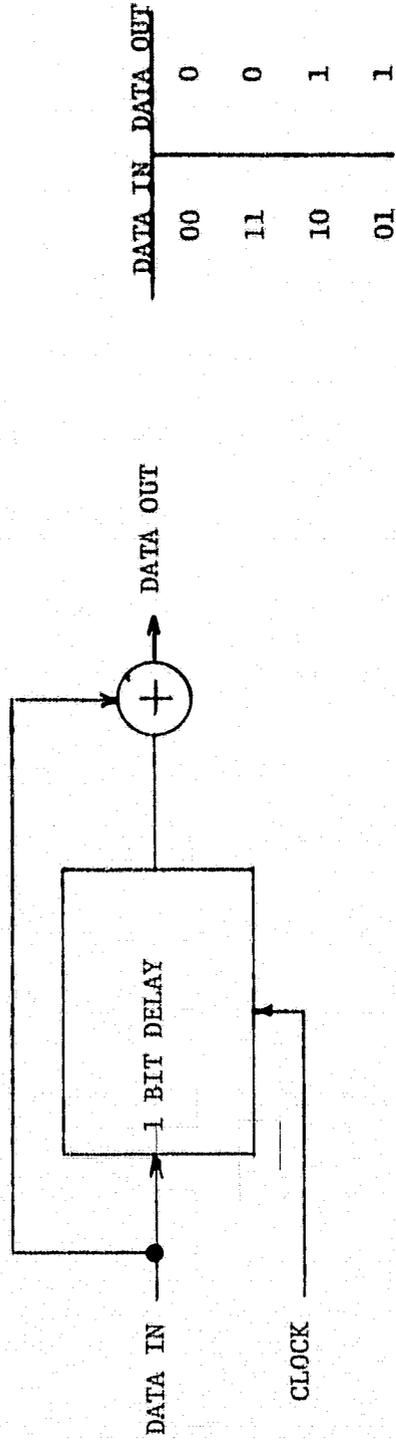


Figure 2.4a Differential Encoder with Truth Table (NRZ-M Type)

DATA IN	DATA OUT
1	\bar{O}_n
0	O_n



DATA IN	DATA OUT
00	0
11	0
10	1
01	1

Figure 2.4b Differential Decoder with Truth Table

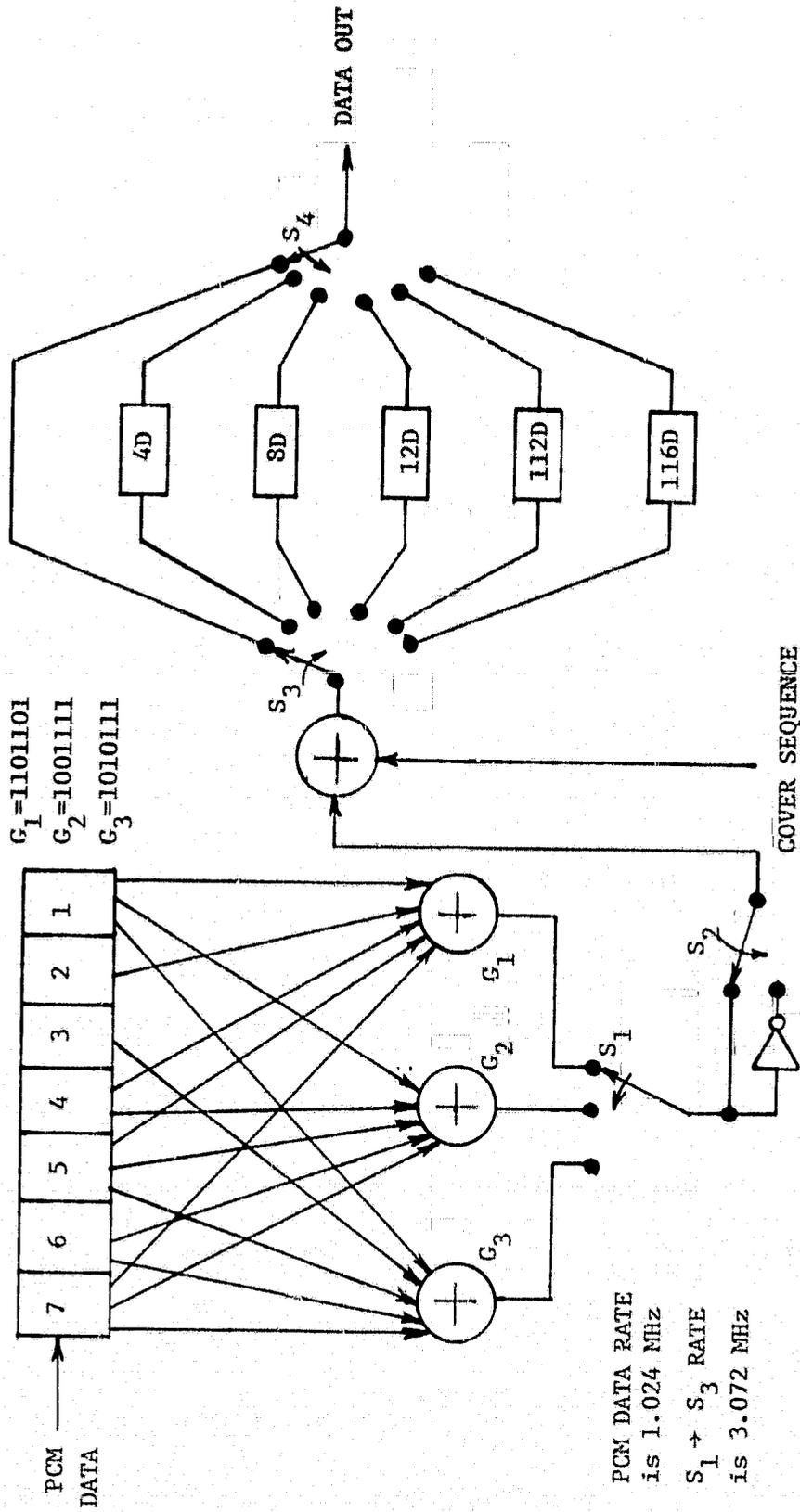


Figure 2.5 Convolutional Encoder with PCI and Cover Sequence

(e) Periodic Convolution Interleaver

The DMS utilizes a (30,116) periodic convolutional interleaver (PCI) with a cover sequence for synchronization in conjunction with the 1/3 convolutional encoder to counteract the burst errors caused by the RFI. The two units together will randomize a channel burst up to 30 symbols by separating any two adjacent input symbols by at least 120 symbols at the output.

The 30 PN sequence is modulo-2 added to the coded symbols prior to interleaving to provide a prior information for deinterleaving synchronization. Also, the deinterleaving sync, and Viterbi decoding branch sync, will occur simultaneously due to the a prior relationship between the G_1 encoder symbol, the cover sequence and the interleaving zero delay element.

The 30 PN cover sequence is a truncated 31 maximal length sequence generated by $1+X^3+X^5$. The truncation is accomplished by the deletion of the shift register word 11110 (MSB) from the normal sequence. The output of the PN generator is inverted prior to being modulo-2 added to the encoded bits.

The PCI is illustrated in Figure 2.6 as commutated delay elements. The input and output commutators are slaved, advance for each encoded bit,

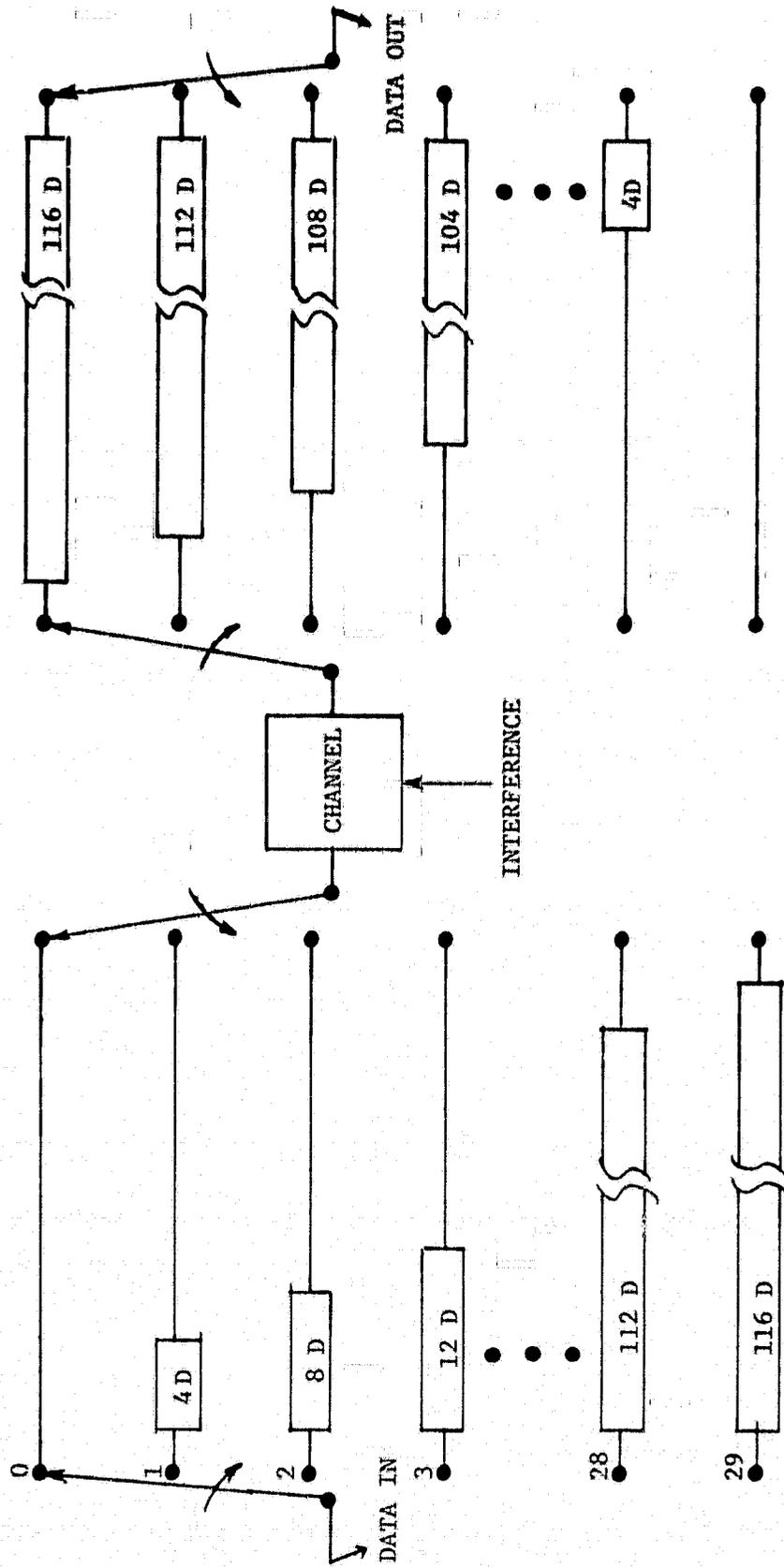


Figure 2.6 Periodic Convolutional Interleaver and Deinterleaver

and recycled every 30 symbols. The input to the zero delay will always be a G_1 encoder symbol modulo-2 added to the initial cover sequence state.

2.A.3.b Instrumentation and Communications System

The interleaved encoded data stream is routed to the I&C where it is used to biphase modulate (BPSK) a 2255.5 MHz 14 watt RF carrier.

The output of the SSA transmitter is multiplexed and switched to provide an RF path for transmission on the HGAs. The HGA system has a beam width of approximately 8.6 degrees providing a half power beam width gain of 22 dB permitting the SSA system to close the link to the TDRSS. The antenna has a two axis rotational control system permitting a close mechanical positioning of the antenna. There are two HGAs, one on either side of the ST that can be positioned so that extended transmission times are provided. A requirement to maintain a minimum 20 minute contact time using one TDRS and one HGA can be achieved. The fine pointing and control subsystem utilizes a continuous instead of a discrete signal to control the positioning of the HGA enabling the system to maintain the center of beam between the ST and TDRS during modulation. The HGA is a 1 meter dish with a 2° minimum full cone angle and has a gain of 24.5 dBi at 1.0° off Boresight.

2.B Tracking and Data Relay Satellite System

The second main group, the return link from the ST to the ground station at White Sands, N.M. via the TDRSS, is specified to have a BER of 1×10^{-5} if certain signal constraints are met. These constraints are listed in Reference 5.

2.B.1 Return Channel Link Model

The TDRSS channel is modeled as memoryless additive white Gaussian channel, even though the channel is subject to both random and burst errors. The burst errors are due to the radio frequency interference (RFI) encountered over certain areas of the world and the inherent characteristic of the Viterbi Algorithm used by the decoder, (commonly called a Viterbi decoder).

Due to the lack of information of the actual effect of the RFI in the return link certain assumptions have been made. The RFI is assumed to degrade the link SNR by 1 dB, at all times. It will cause a 2 dB loss for approximately 2 to 3 minutes per 90 minute orbit while the ST is in a region external to a 1.5° contour of this RFI areas, and a 5 dB loss when the ST is within the 1.5° contour region. These reductions in SNR have been compensated for by a 2.5 dB increase in the EIRP and restraining from transmissions during high RFI periods.

The TDRS will coherent frequency translate the SSA signal up to the K-band in order to utilize the high transmitter power of these bands. Thereby improving the signal to noise ratio of the return link.

2.B.2 Ground Station

The signal will be synchronized, deinterleaved, the PN sequence removed, convolutional decoded using the Viterbi Algorithm and differentially decoded by the ground station at White Sands, N.M.

The bit synchronizer was originally assumed to have a bit slip rate (BSR) of 1×10^{-11} . A bit slip refers to the addition or deleting of a bit time to the incoming symbol sequence. However, the results of recent tests conducted by the manufacturers indicate a much lower BSR. The evaluation was conducted using various data rates from 100 Kbps to 3 Mbps with a 1/2 rate convolutional coding. The channel was characterized by extreme adverse conditions. The ST will not transmit under the simulated conditions. During the several weeks in which the evaluation was conducted, not one occurrence of a carrier or a bit slip was detected.

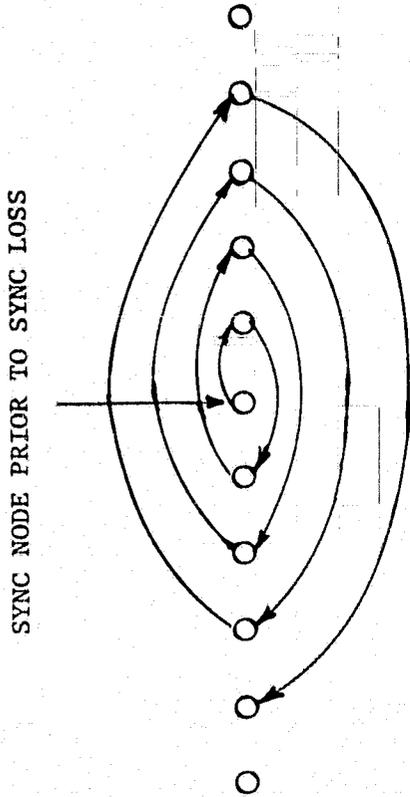
The deinterleaver is said to be synchronized when the deinterleaving commutators are correctly slaved to the interleaving commutators. The propagation delay of channel requires the symbols which are delayed through the $4x$ delay element ($x = 0, 1, 2, \dots, 29$) of the interleaver to be delayed through the $116-4x$ delay element of the deinterleaver. Thirty sync ambiguities exist in the deinterleaver as a result of the thirty positions of the deinterleaver commutator. An initial commutator position or sync state is selected and the results from the Viterbi decoder metric

calculations are used to determine if the selected state is the correct sync state. If the results from the Viterbi decoder indicate an excessive number of errors, it is assumed that an incorrect sync state was selected and a different delay element is selected by the commutator. The decoder again performs the metric calculations and the results tested. Once the correct sync state is selected, the deinterleaver commutator will continue to advance for each input symbol and recycle every 30 symbols.

Since the deinterleaver utilizes feedback from the decoded, it is possible to acquire false sync by locking on one of the sync node adjacent to the correct sync node. The partially deinterleaved sequence has a symbol error rate that is capable of being corrected by the decoder if the input error rate is low (little or no RFI). The 30 PN cover sequence is employed to remedy this situation. The modulo-2 addition of the cover sequence to the encoded symbol prior to interleaving, and again to the deinterleaved symbols prior to decoding, will provide a symbol sequence to the decoder with a very high error rate for any sync node other than the correct sync node. This is due to the autocorrelation properties of the truncated maximal length sequence utilized to generate the cover sequence. Modulo-2 adding the PN cover sequence in this manner assures that the deinterleaver and decoder has essentially a zero probability of locking to any sync node other than the correct node.

The sync strategy for the deinterleaver requires that a search to acquire sync begins with the last sync node then shifts alternately to the next adjacent nodes on the right and left. The sync strategy is shown in Figure 2.7. This strategy is beneficial when a system anomaly occurs, since only a minimal loss of data will occur. The quality indicator from the decoder metric calculations will determine with a very high probability that resynchronization is required. Thus, essentially no false resynchronization will occur and the failure to recognize the need for resynchronization will essentially be zero. This system also has the added advantage that the deinterleaver and decoder will be synchronized simultaneously, since the zero delay element of the interleaver commutators is synchronized to the G_1 symbols of the convolutional encoder. Since the decoder branch sync ambiguity is resolved simultaneously with the resolution of the correct deinterleaver sync node, this minimizes the time required to achieve initial synchronization and resynchronization.

The average number of states searched to acquire initial synchronization for the integrated interleaver/decoder is assumed to be 15. A time of 250 data bits is assumed to be the average sync time of the Viterbi decoder since the decoder does not have to resolve the branch sync ambiguity.



- Total of 30 Sync Nodes for (30,116) PCI
- Sync Search is Always Performed Optimally as Shown From Last Sync Node

Figure 2.7 Synchronization Strategy for the Periodic Convolutional Deinterleaver

The average resynchronization time to recover from a single bit slip is expected to be less than 500 data bits.

The decoder utilizes the Viterbi algorithm and is a maximum likelihood decoder. A maximum likelihood decoder is one which compares the conditional probabilities, $P(Y/X^{(m)})$, where Y is the overall received sequence and $X^{(m)}$ is one of the possible transmitted sequences, and decides in favor of the maximum. One of the disadvantages of this type of decoder is that at low error rate, decoding errors usually occur in bursts.

The output sequence of the Viterbi decoder is converted back to NRZ-L by the differential decoder prior to being released to the NASCOM terminal at White Sands.

2.C. NASA Communications Network

The last main group is the link from the NASCOM terminal at White Sands, N.M., to the NASCOM terminal at GSFC, via DOMSAT system. As previously stated the link has a BER of 1×10^{-7} averaged over a 24 hour period. The data is formulated into the standard 4800-bit NASCOM blocks and a polynomial error detecting code is utilized. This code will only detect errors and has no error correcting capabilities. This link is considered to be transparent and will not be included in the analysis.

Once the data sequence is received at GSFC; it is checked for transmission errors and routed to the STOCC at GSFC. If an error is detected it is tagged and transferred with the other data.

The STOCC has the responsibility of converting the received data stream into a usable form. This entails removing the 255 PN sequence; deinterleaving and decoding the R/S blocks; deleting the dummy data; and compiling the science data into usable information.

2.D. Assumptions

The next section is an analysis of the over all BER for the SSA. The following assumptions were made:

1. The DOMSAT link is transparent
2. The ST SSA link meets all the constraints required by the TDRSS to provide a BER of 1×10^{-5} .
 - a) Rate 1/3 convolutional encoding
 - b) Constraint length of 7
 - c) Soft decision ($Q = 3$ bit quantization)
 - d) Viterbi decoding
 - e) No degradation due to RFI
 - f) Decoder memory is infinite
 - g) 10^{-5} BER for $(E_b/N_o)_1$ of 4.05 dB.
 - h) Interleaving/deinterleaving of the 3 Mbps data stream.
3. Perfect synchronization is maintained.

CHAPTER 3

ANALYSIS OF THE PERFORMANCE OF THE SSA RETURN LINK

This section is an analysis to determine the overall anticipated BER of the scientific data transmitted via the SSA system. The ST utilizes a concatenated coding scheme. The inner coding scheme is the 1/3 rate convolutional code with a Viterbi decoder and PCI with the 30 PN cover sequence. The R/S code with interleaving constitutes the outer coding scheme, thus allowing the SSA return link to be separated into an inner and outer channel (see Figure 3.1). To determine the overall probability of an error, first the probability of an error on the inner channel, $P_1(\epsilon)$, must be calculated, since this is the input error rate to the outer decoder. Once the input error probability is established then the output error probability of the R/S decoder/deinterleaver, $P_2(\epsilon)$, can be determined. Having established both $P_1(\epsilon)$ and $P_2(\epsilon)$, the overall concatenated coding bit error rate, $P_T(\epsilon)$, can be bounded. The material in sections 3.A and 3.A.2 is based on the analysis approach presented by ORI in Reference 2.

3.A Probability of Error for Concatenated Code

The overall bit error probability $P_T(\epsilon)$, may be bounded by bounding the symbol error probability out of the R/S decoder/deinterleaver, $P_{R/S}(\epsilon)$

$$P_T(\epsilon) \leq P_{R/S}(\epsilon) \quad (3.1)$$

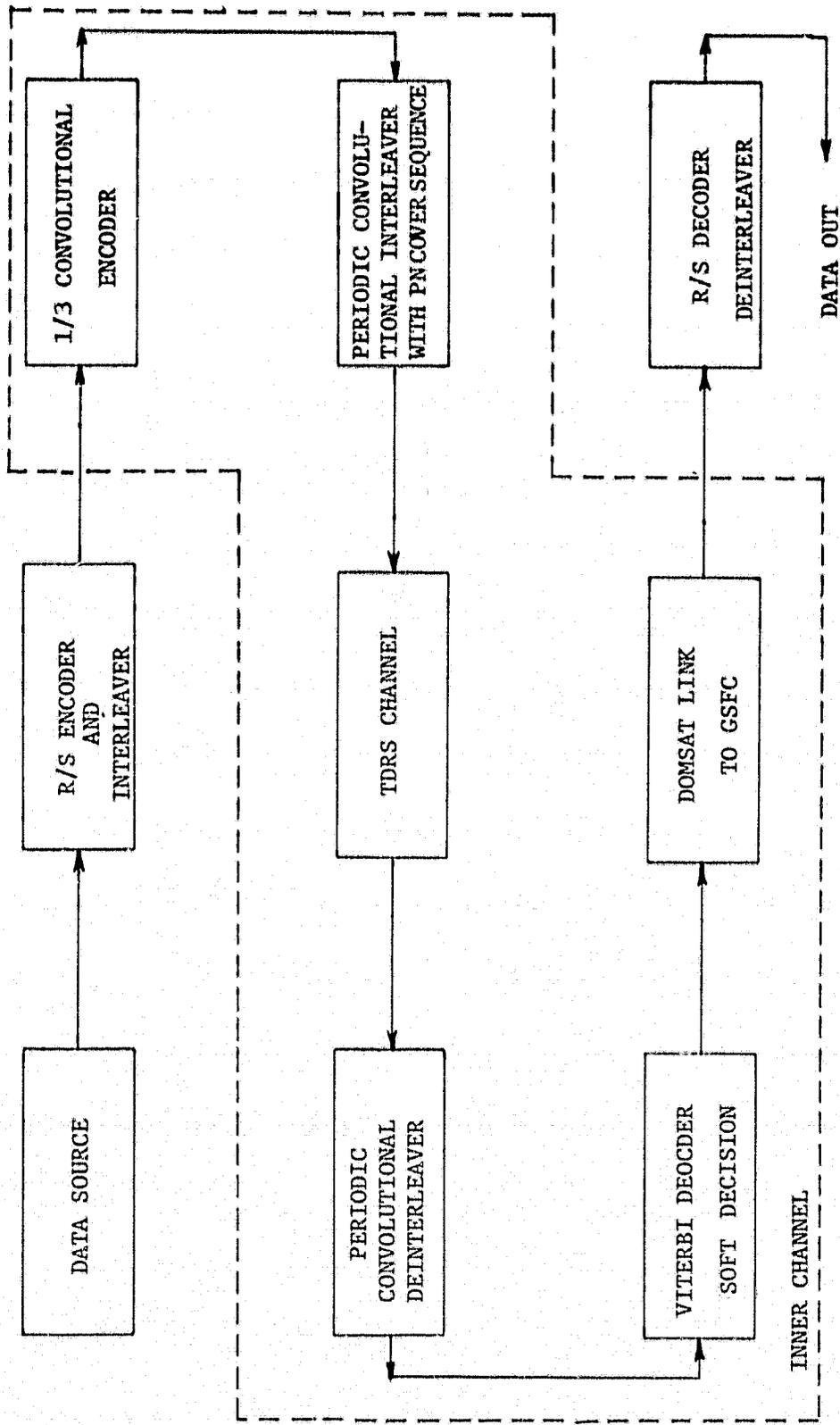


Figure 3.1 General ST/TDRSS Concatenated Coding Concept

The output symbol error probability is obtained by noting that a symbol error occurs only when more symbol errors occur in a R/S block than the code can correct. In general

$$P_{R/S}(\epsilon) < \sum_{K=E+1}^{2^J-1} \frac{K+E}{2^{J-1}} \binom{2^J-1}{K} P_1(\epsilon)^K (1-P_1(\epsilon))^{2^J-1-K} \quad (3.2)$$

where

2^J-1 = number of R/S symbols per block

E = number of correctable symbol errors

J = number of bits per symbol

$P_1(\epsilon)$ = the R/S input symbol error probability

substituting Equation 3.1 into 3.2 and approximating for small $P_1(\epsilon)$ and large E yields the overall bit error probability.

$$P_T(\epsilon) \leq \frac{2E+1}{2^{J-1}} \sum_{K=E+1}^{2^J-1} \binom{2^J-1}{K} P_1(\epsilon)^K (1-P_1(\epsilon))^{2^J-1-K}$$

$$\leq \frac{E}{2^{J-1}} \left\{ 1 - \sum_{K=0}^E \binom{2^J-1}{K} P_1(\epsilon)^K (1-P_1(\epsilon))^{2^J-1-K} \right\} \quad (3.3)$$

The inequality holds due to the assumption of small $P_1(\epsilon)$ and large E . As $P_1(\epsilon)$ increases or E decreases equation 3.3 becomes less accurate and equations 3.2 and 3.1 must be used.

Since the R/S code word error probability is equal to

$$P_2(\epsilon) = \sum_{K=E+1}^{2^J-1} \binom{2^J-1}{K} P_1(\epsilon)^K (1-P_1(\epsilon))^{2^J-1-K} \quad (3.4)$$

which is a summation of the binomial distributions when the number of errors exceeds E. Then Equation 3.3 may be written as

$$P_T(\epsilon) \leq \frac{E}{2^{J-1}} P_2(\epsilon) \quad (3.5)$$

To evaluate $P_T(\epsilon)$, the input R/S symbol error probability $P_1(\epsilon)$, must first be determined. $P_1(\epsilon)$ is the probability of a R/S symbol error occurring on the inner channel.

3.A.1 Transparency of DOMSAT Link

The inner channel consists of the TDRSS link and the DOMSAT link. As previously stated the average bit error rate of the DOMSAT link between White Sands and GSFC is specified to be $P_D(\epsilon) = 1 \times 10^{-7}$. The TDRSS return link is specified to be $P_{WS}(\epsilon) = 1 \times 10^{-5}$, if all the signal constraints are met. It is assumed that the ST meets these requirements. The occurrence of an error on either the DOMSAT or TDRSS link is statistically independent of an error occurring on the other link, but the effects of an error on either link to the data stream is not statistically independent. Therefore the probability of a bit error occurring on the inner channel, $P_b(\epsilon)$, is

$$\begin{aligned}
 P_b(\epsilon) &= P_D(\epsilon) + P_{WS}(\epsilon) \\
 &= 1 \times 10^{-7} + 1 \times 10^{-5} \\
 &= 1.01 \times 10^{-5} \\
 &\approx P_{WS}(\epsilon) \qquad (3.6)
 \end{aligned}$$

Since $P_b(\epsilon) \approx P_{WS}(\epsilon)$, the DOMSAT link is considered to be transparent and has essentially no effect on the overall error probability. This assumption simplifies the analysis by allowing the output error probability of the Viterbi decoder to be considered as the input error probability to the R/S decoder/deinterleaver.

$P_1(\epsilon)$ is a function of the Viterbi decoder output to BER, $P_{VD}(\epsilon)$. The relationship of $P_1(\epsilon)$ to $P_{VD}(\epsilon)$ should be obtained by computer simulation. This was done in Reference 4 and verified in Reference 2. Although the results are not explicitly shown, a comparison of plots and calculations allows the relationship between $P_1(\epsilon)$ and $P_{VD}(\epsilon)$ to be approximated. For $P_{VD}(\epsilon) = 10^{-5}$, the ratio $P_1(\epsilon)/P_{VD}(\epsilon)$ is expected to be slightly less than 2.4.

A non-rigorous analytical expression relating $P_{VD}(\epsilon)$ to $P_1(\epsilon)$ may be obtained in the following manner for a particular case. First the Viterbi decoder output error statistics must be described and quantified. When the Viterbi decoder is operated at low error rates, the resultant output errors not only occur infrequently, but they also occur in bursts.

3.A.2 Probability of A Burst $\geq L$

The sizes of the bursts will be defined as b bits; of these b bits w information bits are in error where $w \leq b$. Data are very difficult to obtain by simulations on burst statistics at low error rates. The data for a 1/3 rate Viterbi decoder operating at $P_{VD}(\epsilon) = 1 \times 10^{-5}$ are presently unavailable, but a 1/2 rate Viterbi decoder operating at $P_{VD}(\epsilon) = 5 \times 10^{-3}$ provides a close approximation to the expected performance of such a decoder. Figure 3.2 shows the probability that a burst is $b=L$ bits in length, given a burst exists. Also shown is the cumulative distribution function as a function of burst length.

$$P(b \leq L \text{ burst exists}) = \sum_{\ell=1}^L P(b=\ell/\text{burst exists}) \quad (3.7)$$

The average values for burst sizes are often easier to obtain than the actual distribution, particularly at low BER. Figure 3.3 taken from Reference 2 is a plot of the average burst size, \bar{b} , and average number of errors per bursty, \bar{w} , as a function of decoder bit error rate $P_{VD}(\epsilon)$. Note that lowering the code rate increases the average burst size by spreading out the distribution function. For $P_{VD}(\epsilon) = 1 \times 10^{-5}$ the average burst size is approximately $\bar{b} = 8$ bits for 1/3 rate Viterbi decoder.

The average probability of a burst is given by

$$P(\text{burst}) = \frac{P_{VD}(\epsilon)}{\bar{w}} \quad (3.8)$$

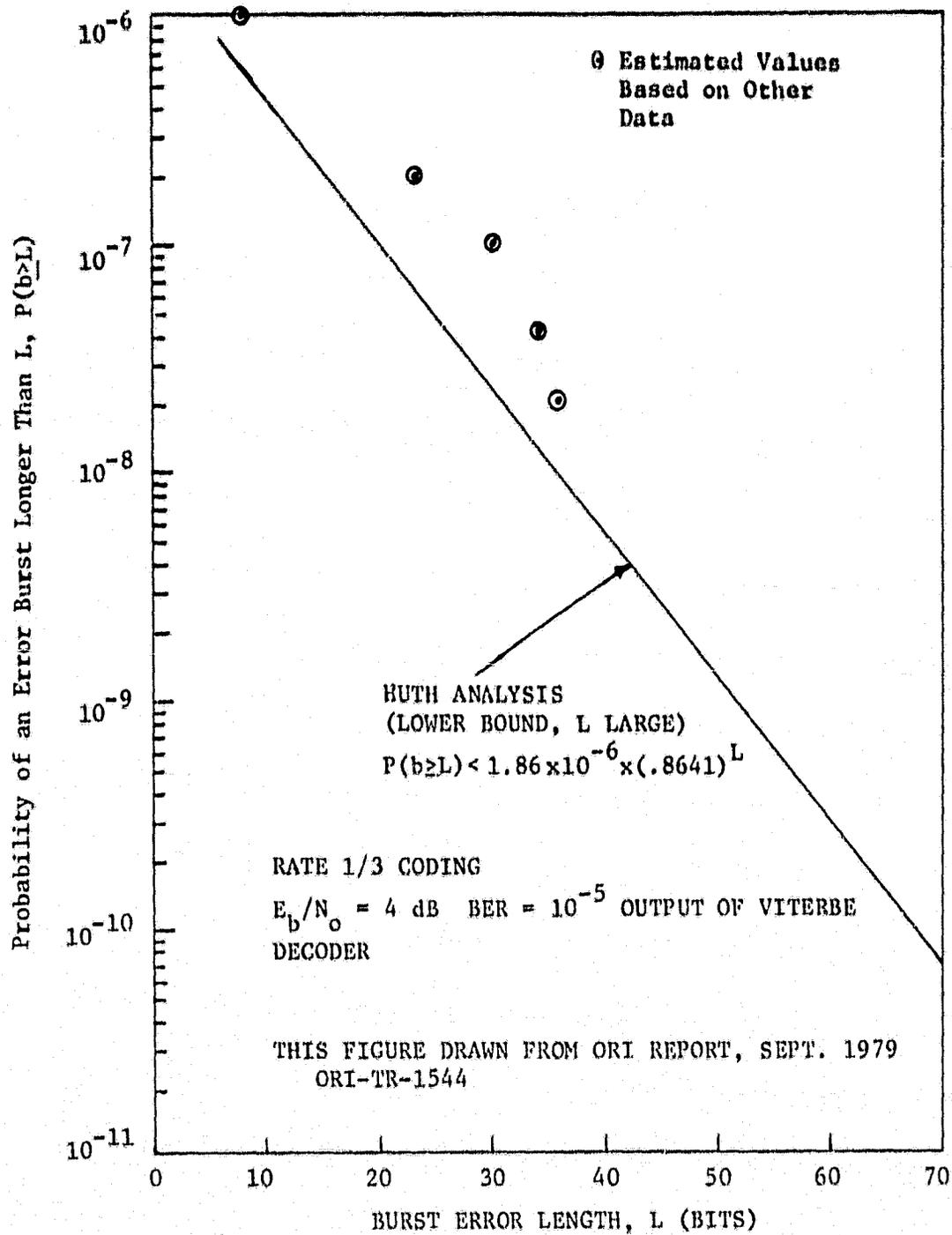


Figure 3.2 Probability of an Error Burst Longer Than L Versus Burst Length for Rate 1/3 Viterbi Decoding with BER= 10^{-5}

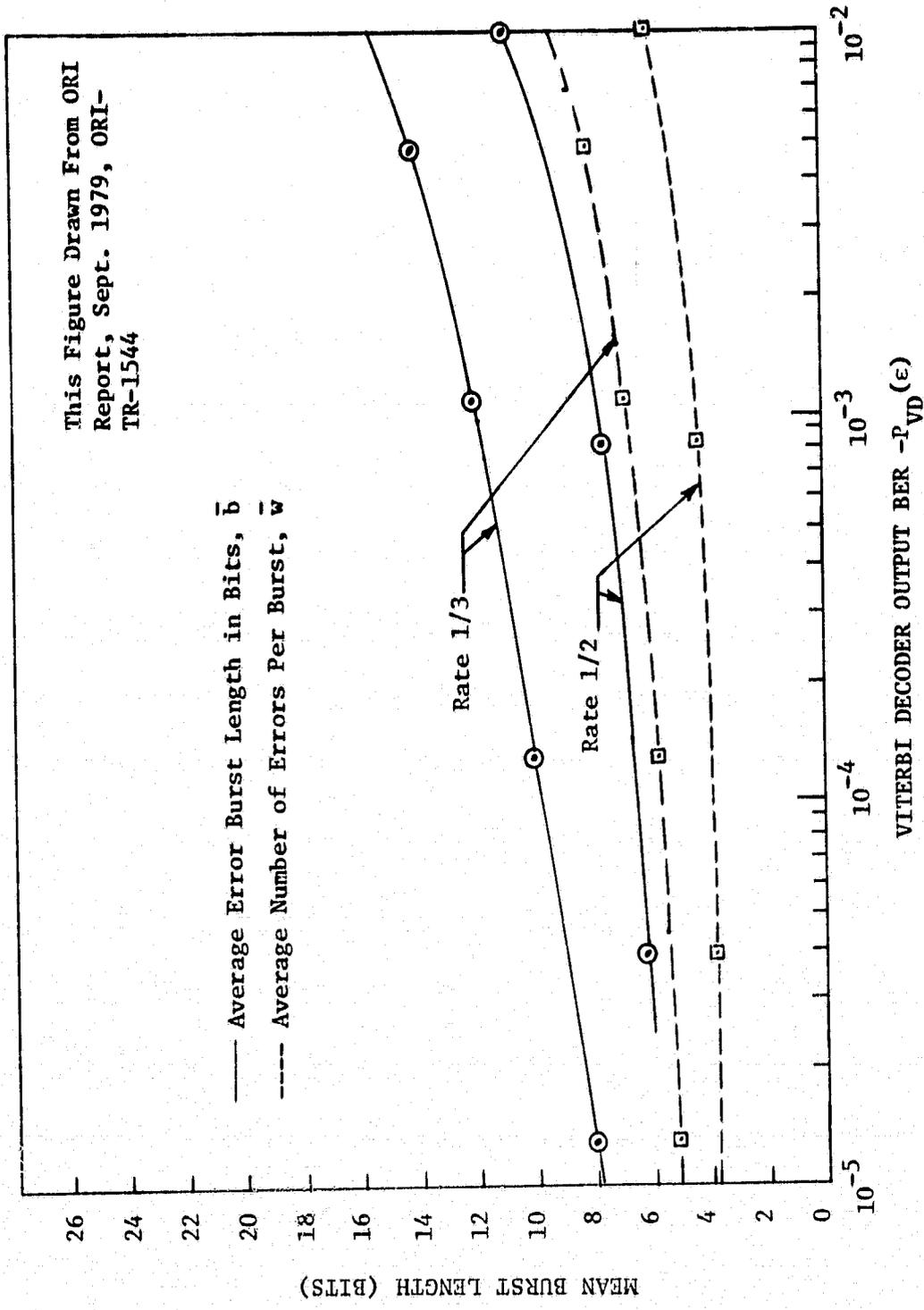


Figure 3.3 Average Burst Length Statistics for Rate 1/2 and 1/3 Viterbi Decoded Errors

where \bar{W} is the average number of information bits in error in the burst. Next the probability density function $P(b=l/\text{burst exist})$ of obtaining a burst of length l , given a burst occurs, must be obtained. The R/S input symbol error probability is then given by

$$\begin{aligned}
 P_1(\epsilon) &= \sum_{l=1}^J \binom{J}{l} P(\text{burst}) \cdot P(b=l/\text{burst exists}) \\
 &= \frac{P_{VD}(\epsilon)}{\bar{W}} \sum_{l=1}^J \binom{J}{l} P(b=l/\text{burst exists}) \quad (3.9)
 \end{aligned}$$

Since the density function $P(b=l/\text{burst exists})$ was assumed to be approximately equivalent for $\frac{1}{2}$ rate with $P_{VD}(\epsilon) = 5 \times 10^{-3}$ and $1/3$ rate with $P_{VD}(\epsilon) = 1 \times 10^{-5}$, the values of $P(b=l/\text{burst exist})$ from Figure 3.2 may be substituted into Equation 3.9.

Then

$$\begin{aligned}
 P_1(\epsilon) &= \frac{P_{VD}(\epsilon)}{5} \sum_{l=1}^8 \binom{8}{l} P(b=l/\text{burst exists}) \\
 &= 2.43 P_{VD}(\epsilon) \quad (3.10)
 \end{aligned}$$

Even with the approximation used for the distribution $P(b=l/\text{bursts exists})$, the results in terms of the ratio $P_1(\epsilon)/P_{VD}(\epsilon)$ are very close to those obtained from Reference 6 ($\frac{1}{2}$ rate convolutional code with $P_{VD} = 5 \times 10^{-3}$ then $P_1(\epsilon)/P_{VD}(\epsilon) = 2.4$). Since the analysis is only a reasonable approximation, the following approximation is used.

$$P_1(\epsilon) = 2.5 P_{VD}(\epsilon) \quad (3.11)$$

Substituting (3.11) into (3.3), the overall concatenated bit error probability is

$$P_T(\epsilon) \leq \frac{E}{2^{J-1}} \left\{ 1 - \sum_{K=0}^E \binom{2^J-1}{K} \left(2.5 P_{VD}(\epsilon) \right)^K \left(1 - 2.5 P_{VD}(\epsilon) \right)^{2^J-1-K} \right\} \quad (3.12)$$

$\leq 1 \times 10^{-12}$ (for $E=8$, $J=8$ and $P_{VD}(\epsilon) = 1 \times 10^{-5}$ to the tenth decimal place).

Comparing this value for $P_T(\epsilon)$ with those in Reference 3 they are in close agreement thereby supporting the analysis and the approximations that were used in Reference 2 and presented in this paper.

Using Equation 3.12 performance calculations were made by ORI showing the trade off between overall bit error rate, $P_T(\epsilon)$, and the inner coding energy per bit to noise density ratio, $(E_b/N_o)_I$. These trade offs are shown in Reference 2 from which Figure 3.4 was taken for $J=8$ and $E=8$. These curves are easily obtained by noting for each value of $P_{VD}(\epsilon)$ in equation 3.11, the corresponding value of $(E_b/N_o)_I$ shown in Figure 3.4 from Reference 2. Since the TDRSS channel will be designed to yield $P_{VD}(\epsilon) = 1 \times 10^{-5}$ with $(E_b/N_o)_I$ 4.05 db, the overall BER shall be less than 1×10^{-7} .

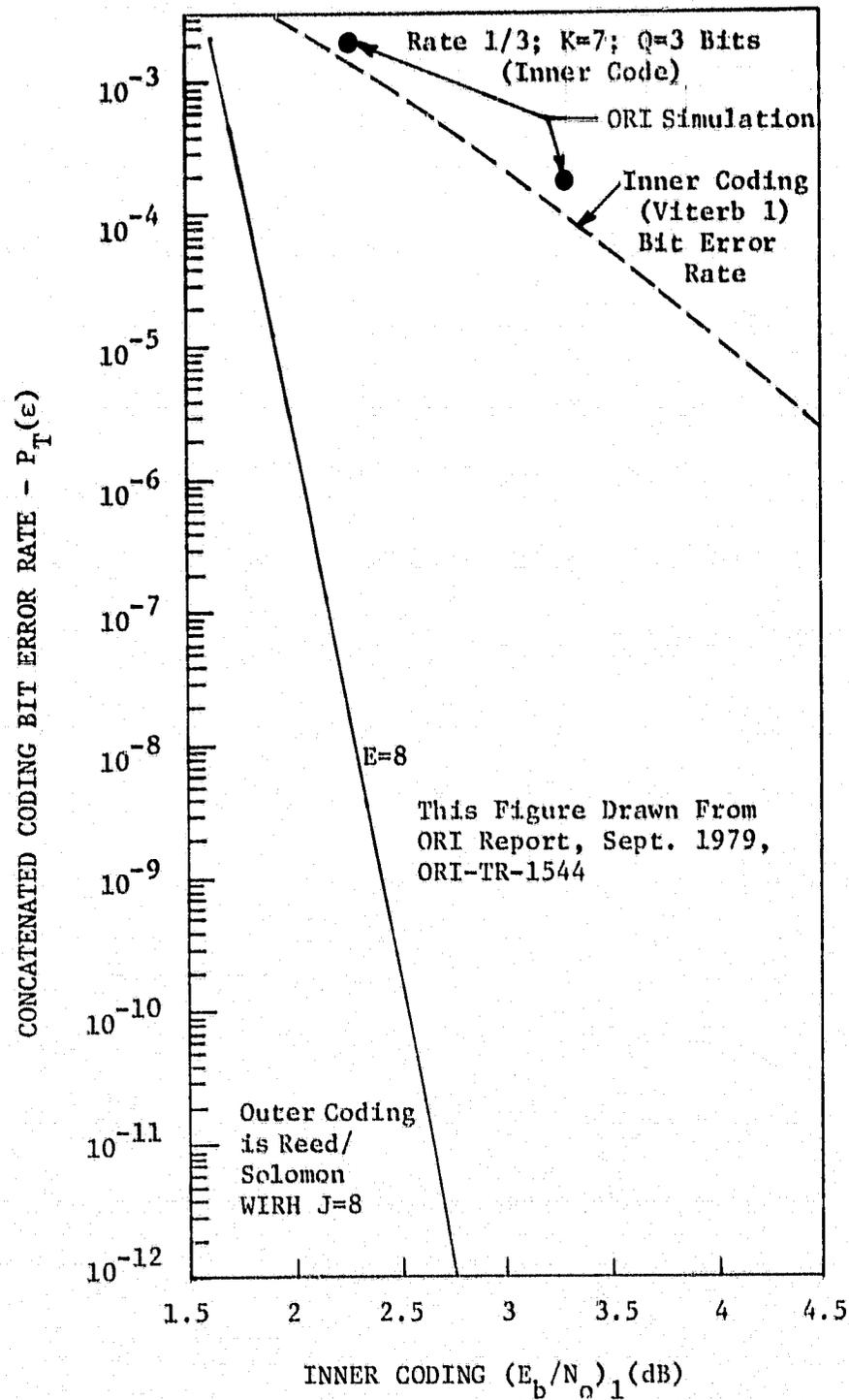


Figure 3.4 Concatenated Coding BER Versus Inner Coding E_b/N_o for a RS Outer Code with J=8

3.B. Probability of Error on the Inner Channel

The remainder of this section will deal with determining the BER of inner channel, the output of the 255 PN encoder to the output of the Viterbi decoder. There are several aspects that must be considered in determining the inner channel BER, and these are:

1. Bit Transition Density
 2. Tape Recorder
 3. Synchronization
 4. Multiple Frame Format
 5. RFI
- a) Bit Transition Density

The ability of the inner channel to meet the TDRSS requirements of at least 1 transition in every 64 symbols and at least 64 transitions in every 512 symbols is examined in this section. The configuration of the system is illustrated in Figure 3.1. The 1/3 rate convolutional encoder with alternate bit inversion of Figure 2.5 will be examined first.

The following discussion concerning the output symbol transition density of the 1/3 convolutional encoder with alternate symbol inversion is based on the material by M.K. Simon and J. F. Smith in Reference 11. Simon and Smith have determined, for a particular class of convolutional codes, that alternate symbol inversion assures a maximum transition-free run of output symbols,

and hence its minimum transition density. This maximum length is independent of the data source model, independent of the code connections, and dependent only on the code constraint length and rate. Simon and Smith separate all v convolutional codes into three classes of codes: v even, v odd for transparent codes, and v odd for nontransparent codes. A transparent code is one which provides the complement of the output sequence for the complement of the input sequence. A simple test to determine if a code is transparent is each row of the generator matrix \underline{C} has an odd number of ones then the code is transparent.

The generator matrix \underline{C} for the 1/3 convolutional code employed by the ST is

$$\underline{C} = \begin{bmatrix} 1 & 1 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 1 \end{bmatrix} \quad (3.13)$$

where the right hand column represents the present input and the left hand column represents the oldest (content of the last shift register K , the code constraint length) input.

Since $v=3$, odd and each row of \underline{C} contains an odd number of ones, the convolutional code is a member of case 2. Simons and Smith state for v odd and transparent codes, the only input bit sequence that will produce an output

alternating sequence longer than N_{\max} symbols where N_{\max} is defined as

$$N_{\max} = K + \left\lceil \frac{K-1}{v-1} \right\rceil - 1 + v \quad (3.14)$$

K = the code constraint length; $\lceil x \rceil$ denotes the smallest integer greater than or equal to x .

is the alternating sequence. Further more, if the encoder is such that the alternating input sequence produces the alternating output sequence, then this output sequence can continue indefinitely, i.e., alternate symbol inversion will not produce a finite transition-free symbol sequence.

Reference 11 provides a test to determine if a case 2 code will produce an alternating output for an alternating input. Split the generator matrix \underline{C} into two matrices $\underline{C}_{\text{odd}}$ and $\underline{C}_{\text{even}}$ where $\underline{C}_{\text{odd}}$ is composed of all the odd columns of \underline{C} and $\underline{C}_{\text{even}}$ all the even columns. If the number of ones in each row of the matrix formed by stacking $\underline{C}_{\text{odd}}$ on top of $\underline{C}_{\text{even}}$ alternates even, odd, even, ... or vice versa, then an alternating input sequence will produce an alternating output sequence. Testing the generator matrix, it is found the number of ones in each row of the test matrix does not alternate even, odd or vice versa. Therefore the

maximum number of transition-free output symbols from the 1/3 convolution encoder with alternate symbol inversion is:

$$\begin{aligned}
 N_{\max} &= K + \left\lceil \frac{K-1}{v-1} \right\rceil - 1 + v \\
 &= 7 + \left\lceil \frac{7-1}{3-1} \right\rceil - 1 + 3 \\
 &= 12 .
 \end{aligned}
 \tag{3.15}$$

The maximum number of transition-free output symbols was also determined to be 12 in References 3 and 10. Magnavox in Reference 3 utilized an extensive computer analysis to arrive at a maximum of 12 and Baument, et.al., Reference 10, used a slightly different mathematical approach to obtain 12 as the maximum bits between transitions and therefore the system is guaranteed to meet the 1 in 64 requirement.

Simon and Smith also prove in Reference 11 the 11-bit input sequence 01110100100 yields the output 01000000000001. Neither this output sequence nor its compliment can be repeated within the next 33 output symbols. The next input will produce at least one additional bit transition therefore the average bit transition for this worse case plus one additional input is 2 transitions per 16 output symbols which yields an average of 1 transition every 8 output symbols. Therefore the output of the 1/3 convolutional encoder

with alternate bit inversion and generator matrix given in Equation 3.13 will meet both the 1 transition per 64 bits and 64 transitions in 512 or an average of 1 transition every 8 bits.

If the 12-bit input sequence is 01110100100 the output will be 01000000000001100 .

If the 12-bit input sequence is 01110100101 the output will be 01000000000001011 .

Since the output of the 1/3 rate convolutional encoder will have a transition at least every 13 bits independent of the data input, it is not necessary to examine the equipment preceeding the encoder. However if the channel interleaver is utilized it is necessary to determine if it is possible to obtain 64 or more symbols out of the interleaver without a transition. The channel interleaver is shown in Figure 2.6. This interleaver will take any two symbols within 30 of each other and separate them by at least 119 bits. Equation 3.16 may be used to express a typical output symbol b_i in terms of the input symbol a_i .

$$b_{j+i} = a_{j+i-4ix30} = a_{j+i-120_i} = a_{j-119_i} \quad j \geq 119_i \quad (3.16a)$$

$$b_{j+i} = 0 \quad j < 119_i \quad (3.16b)$$

where

$$j = 0, 30, 60, 90, 120, \dots$$

$$i = 0, 1, 2, 3, \dots, 29$$

Therefore, a typical output sequence of the interleaver would resemble a sampling of the input sequence with the samples being taken every 119th bit for sequences up to 30 bits in length. In order for the interleaver to have an output of 64 consecutive symbols of the same value, the input data must be such that samples of the input sequence separated by 119 symbols be of the same value. The length of input symbols corresponding to 64 output symbols is approximately 3511. Also noting that the output of the interleaver is combined with a PN cover sequence of length 30, it would appear highly unlikely that a string of 64 ones or zeroes will occur, however due to the systematic construction of the components of the system, it is possible that a sequence of data does exist that will yield a string of 64 output symbol without a transition. Since the actual structure of the data is presently unavailable it is not possible to examine this problem more closely. It would be necessary to examine very closely the structure of the data and how that structure is effected by the various components of the system. (Note Lockheed is presently developing a computer simulation of this system.)

b) Tape Recorders

The ESTRs are subject to phase ambiguity as previously stated in Section 2. If it is assumed that the 3-bit pattern (010) required to re-phase the data appears with sufficient frequency within the data stream either naturally or as part of the fill and/or dummy data, then a BER for the recorders is established at less than 10^{-6} . The degradation to the overall BER due to this problem can thus be neglected similar to the BER of the DOMSAT Link. And since the tape recorder has a zero bit-slip rate according to the manufacturer, the main problem due to the tape recorder will be due to the bit reversal when the recorder is played back in the reverse order. It will be necessary to restore the correct order to the data prior to the R/S decoder/deinterleaver. A procedure to accomplish this was recommended in Reference 3 and it is assumed that this method or one similar will be utilized to resolve the problem.

Due to the above, the ESTRs are assumed to have essentially no effect on the overall error probability.

c) Synchronization

This section discusses the effect on the BER when one of the synchronization components of the

system loses lock. Each element will be examined separately as an entity where possible, and then the interplay among the various components will be discussed. A total data loss due to synchronization loss will be estimated.

The symbol synchronizer is the first processing element operating on the baseband symbols. The unit drives the Viterbi decoder/channel deinterleaver. It takes in noise corrupted demodulated symbols, performs an integration, and outputs Q levels. The Q levels are converted by an A/D and presented to the Viterbi decoder/channel deinterleaver combination. Loss of lock by the symbol synchronizer results in a trend towards an unlocking state for all system elements since all the data following sync loss is in error. Whether or not any given element unlocks depends upon the duration of the symbol synchronizer unlock and the flywheel effect of the elements that follow.

Due to the catastrophic nature of a symbol synchronizer loss of lock, it must be assumed that its probability of occurrence is extremely small under other than abnormal operating conditions. As previously stated in Section 2, the symbol synchronizer has been tested and according to the manufacturer has an extremely low probability of symbol

sync loss occurrence, much less than 10^{-11} as previously considered.

For the low SNR of this system, the acquisition time is expected to be on the order of 1000 symbols, thus the data lost due to symbol synchronizer drop lock and reacquisition would be that which corresponds to the loss of 1000 symbols.

In Section 2 the sync strategy for the decoder and deinterleaver was discussed. Since the deinterleaver utilizes the results from the Viterbi decoder metric calculations to determine its sync node status, the decoder and deinterleaver are considered one unit. The 1 of 3 states of the code itself, and then the deinterleaver state must be resolved prior to decoding. Since the data has been differentially encoded, the alternating symbol ambiguity out of the convolutional encoder does not have to be resolved. Once the deinterleaver acquires sync, the state node sync is also obtained, since the node sync is locked to the deinterleaver as described in Section 2.

Assuming initial sync has been acquired, if drop lock (loss of sync) occurs the deinterleaver will try to reacquire sync beginning with the last sync node then shifting alternately to the next adjacent nodes on the right and left. The sync

strategy is illustrated in Figure 2.7. As a maximum data loss estimate (all 30 nodes searched).

$$\begin{aligned} & (30 \text{ nodes}) \times (200 \text{ to } 500 \text{ information bit durations}) \\ & = 6,000 \text{ to } 15,100 \text{ bits of data lost.} \end{aligned}$$

The 200 to 500 information bit durations are Linkabit's estimate of synchronization time for each of the 30 deinterleaver states.

The R/S decoder/deinterleaver loss of sync will result in the loss of a minimum of one full "frame" of 7904 bits of information. The R/S unit has a high probability, under normal operating conditions, of reacquiring sync on the next frame, thus an estimate of 7904 information bits will be loss due to R/S drop lock. The normal operation of this type will allow 1 to 3 errors in the sync word and allow 1 pattern miss before drop lock occurs.

The loss of sync by any of the system elements will result in the loss of sync by the succeeding elements. If the symbol synchronizer loses lock for any length of time then the total system will require reacquisition of sync. This would involve the loss of 1.4×10^4 to 3.1×10^4 bits of data.

$$\begin{aligned} & (6000 \text{ to } 15000) + (7904 \text{ to } 15808) \\ & = 1.4 \times 10^4 \text{ to } 3.1 \times 10^4 \text{ bits} \end{aligned} \quad (3.17)$$

The factor of 2 accounts for the search and verify operation used in synchronizing the R/S unit.

In the same matter if the Viterbi decoder/channel deinterleaver drops lock, the R/S unit would also lose sync since the 6000 to 15000 bits required to resync the Viterbi decoder/channel deinterleaver would be in error. Losses of sync by the R/S unit would not effect either of the other two elements. Table 3.1 summarizes the results of drop lock for each element.

TABLE 3.1

Data Lost Estimates Due to Sync Loss

System Element	Data Loss Estimation (information bits)
Symbol Synchronizer	Dependent on elements following synchronizer and duration of droplock
Viterbi Decoder/Channel Interleaver	6000 to 15000
R/S Unit	7904 to 15800
TOTAL	1.4×10^4 to 3.1×10^4

d) Multiple Frame Format Operation

The multiple frame lengths of 1000, 2000, and 1024 can be present at the output of the R/S unit or the engineering data frame synchronizer. It is assumed that the frame synchronizers at the ground station will be operationally reconfigured based upon a priori knowledge of the length being received.

e) Radio Frequency Interference

RFI may affect the transmitted signal in two ways. The RFI may cause an inverted bit stream output at the White Sand station as a result of a PSK demodulator carrier slip. The RFI energy may be sufficient to blanket the transmitted signal, make it appear as a sequence of consecutive bits of the same value, thus resulting in a possible loss of lock by the bit synchronizer at White Sands. The following paragraphs examine the probability that either of these conditions will occur.

First, the case of a PSK demodulator carrier slip at White Sands will be discussed. Since the signal is differentially encoded and interleaved, a demodulator carrier slip resulting in an inverted bit stream would be disastrous. A simple illustration is given in Appendix C. However, the PSK demodulator is a Costas loop which typically uses a slow response filter as the loop filter. Figure 3.5 is an illustration of a Costas loop. Once sync is achieved the Costas loop will "ride out" perturbations in the received waveform.

The PSK demodulator has a 100 Hz loop filter. Thus the VCO control voltage variation is bounded by this response rate of 100Hz. If the VCO carrier is allowed to vary a full 360° at 100 Hz rate then in

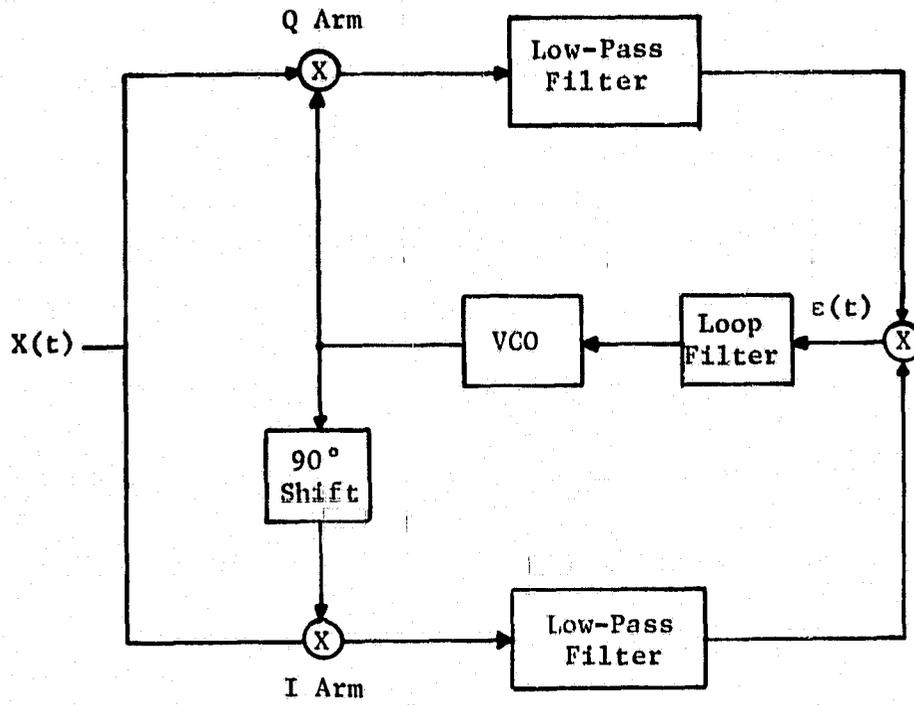


Figure 3.5 Costas Loop

one millisecond only a 36° variation in VCO could occur. A 36° variation would not create a carrier cycle slip if the PSK loop is initially in Lock.

In order to create a 1 millisecond long period of erroneous phase in the signal, the RFI would have to exceed the link margin which is estimated to be 3.7 dBW minimum for the 1 millisecond period. A RFI signal of 3.7 dBW would be considered heavy RFI during which time the ST is not allowed to transmit as stated in Section 2.

For the sake of completeness assume the ST does transmit during this time period and the RFI completely overrides the signal for a 1 millisecond period. The probability of this occurring may be estimated in the following manner.

The data describing the RFI for S Band has been summarized as follows by GSFC:

Pulse Widths: 1 to 5 sec

Repetition Rates: 1 K pulses/sec

Aggregate Pulse

Repetition Rates: 20 K pulses/sec

Activity: High

The ST will be exposed to various levels of RFI during an orbit of approximately 90 minutes of which 20 minutes will be allotted for ST to TDRSS transmissions during a 76 minute look time of availability.

If the RFI is assumed to be:

- . Approximately 1 minute is heavy RFI(>5dB)
- . Approximately 2-3 minutes is medium RFI(>2dB)

Then the random reception of RFI pulses may be modeled by a Poisson Process.

Having made the above assumptions the following discussion derives the probability of PSK carrier cycle slip. It will be shown to be extremely small and in fact is negligible.

A certain event occurs randomly on the average of 2 times per second (averaged over a large interval T) and let K events occur in an interval of time τ . Then the probability of these K events occurring in a τ second interval is

$$P_K(\tau) = \frac{(\alpha\tau)^K e^{-\alpha\tau}}{K!} = \frac{(\lambda\tau)^K e^{-\lambda\tau}}{K!} \quad (3.18)$$

For this case $T=2$ minutes = interval of heavy RFI

$\alpha=20$ K RFI pulses per second received

on the average.

Hence the probability that K pulses occur in an interval $\tau = 5$ μ sec is

$$P_K(5 \mu\text{sec}) = \frac{(.1)^K e^{-.1}}{K!} \quad (3.19)$$

The parameter λ is called the Poisson parameter and is equivalent to the average occurrence of the event in question.

$$\lambda = 20 \times 10^3 = 2 \times 10^4 = \alpha$$

We may tabulate the probability of K pulses being received in a $5 \mu\text{sec}$ interval as

K	$P_K(5 \mu\text{sec}) = \left[(.1)^K e^{-1} \right] / K!$
0	.90483741
1	.090483741
2	.004524187
3	.00015080623
\vdots	\vdots

Assume each pulse has constant width, W .

The cases of interest is the probability of a series of pulse being received over a $1000 \mu\text{sec}$ period such that each pulse is received before the end of the preceeding pulse.

Let X = time between the arrival of the first pulse and the second pulse. Then the probability that $X > 5 \mu\text{sec}$ is

$$\begin{aligned} P(X > 5 \mu\text{sec}) &= e^{-(5 \times 10^{-6})(2)} = e^{-(5 \times 10^{-6})(2 \times 10^4)} \\ &= .90483741 \end{aligned} \quad (3.20)$$

which is the probability of zero pulses being received in 5 μ sec.

The probability that a pulse will be received in 5 μ sec or less is

$$1 - P(X > 5 \mu \text{sec}) \quad (3.21)$$

or

$$P(2^{\text{nd}} \text{ pulse occurs before } 5 \mu \text{sec}) = .095162581$$

For a 1000 μ sec burst of RFI composed of 5 μ sec pulses, each pulse being emitted and received at random with an average emission and reception rate of 20 K pulses per second, at least 200 pulses each within 5 μ sec of the previous pulse must be received. But each pulse is received independently of the others and as a result the probability of receiving 200 with proper timing is bounded by

$$\begin{aligned} P(1 \mu \text{sec of continuous RFI}) &= P(\text{of } 5 \mu \text{sec spacing})^{200} \\ &= (.904162581)^{200} \\ &= (8.381289 \times 10^{-52})^4 \\ &\approx 4.931 \times 10^{-208} \quad (3.22) \end{aligned}$$

Therefore, the chance of an RFI burst long enough to inhibit the TDRSS receiver for even 1 μ sec period is extremely remote, in fact a negligible probability.

The above cases is seen to be the worst case, since the RFI pulses were assumed to have constant

maximum width. In the case of short width pulses, it would require many more received pulses to create a 1 μ sec burst. Hence the probability of receiving a continuous pulse string is even more remote for variable pulse widths. Therefore the cases of PSK carrier slip due to RFI may be neglected.

The second problem caused by RFI is the case of possible channel symbol (bit sync) synchronizer loss. This case corresponds to the situation of 65 μ sec of RFI of the same phase quadrant resulting in a 65 μ sec string of like digits being transmitted from TDRSS to White Sands.

Since the channel is BPSK the probability that a received RFI pulse will cause a one or a zero to be retransmitted is 0.5. Thus the probability that a second received pulse occurs within the 5 μ sec period and that the pulse causes the same value to be transmitted is

$$\left[1 - P(X > 5 \mu\text{sec}) \right]^{1/2} = \frac{.095162581}{2} = .04758129 \quad (3.23)$$

For a 65 μ sec continuous string to occur, a sequence of at least 13 RFI pulses must occur and this probability is

$$\begin{aligned}
 P(13 \text{ pulse pairs at } 5 \mu\text{sec}) &= (.04758129)^{13} \\
 &= 6.407079 \times 10^{-18} \quad (3.24)
 \end{aligned}$$

Actually, since some pulse pairs will occur at intervals closer than 5 μsec , this approach is a weak bound and the actual probability will be less. Since a string of either ones or zeroes would create a potential bit sync loss, therefore

$$\begin{aligned}
 P(\text{of } 65 \mu\text{sec string of either } 1^{\text{S}} \text{ or } 0^{\text{S}}) \\
 = 1.2814158 \times 10^{-17} \quad (3.25)
 \end{aligned}$$

Thus the problem of RFI creating a bit sync loss or a carrier cycle slip is statistically rare and not a factor about which to be concerned when compared to overall system performance. This assumption is supported by test results conducted by the component manufacturer as previously stated.

The preceding discussion varified the validity of assuming the inner channel error rate of 1 error in 10^5 bits assuming the frame synchronizers has a priori knowledge of the format being transmitted, the tape recorder reversal problem is resolved, and the transponders have a BER of 1×10^{-7} . Due to these restrictions, a BER of 1×10^{-4} was substituted into Equation 3.12 with $E=8$ and $J=8$. The overall BER was founded to be

$$P_T(\epsilon) = 1 \times 10^{-9} \quad (3.26)$$

with accuracy to the tenth decimal place.

Therefore it seems reasonable to expect the overall BER for the SSA Link to meet or exceed the desired value of 1 error in 10^7 bits. Table 3.2 depicts the expected operational performance the system will achieve under various operating conditions. The information presented in Table 3.2 is based on material taken from References 2,5,13, and 14. A summary of these material is presented in Section 4. However, it must be emphasized that these values for the expected SSA Link BER do not take into account several important variables such as a reduction in the EIRP and the system susceptibility to synchronization loss. These variables are discussed in Section 4.

3.C 255 PN Sequence

The 255 PN sequence was intentionally omitted from the above analysis. Its removal was recommended in Reference 3. Also, the Lockheed system evaluation indicates the ST will violate the CCIR Flux requirements even with the 255 PN sequence. The only purpose for utilizing the 255 PN sequence was to meet the CCIR requirements. The Lockheed evaluation indicated a small percentage of possible violation if the sequence is removed.

TABLE 3.2

EXCEPTED BIT ERROR RATE FOR THE SSA
LINK DUE TO RFI AND BIT SLIP

OPERATING CONDITION	LINK MARGIN (dB)	EXPECTED SYSTEM BER	RECOMMENDATIONS
CASE I . Low RFI (~.7) . No Bit Slips at White Sands	3.7	$<10^{-12}$	The System BER should meet the desired BER of 1×10^{-7} for this case
CASE II . Medium RFI (2 to 5dB) . No Bit Slips at White Sands	3.7	$<10^{-10}$	The System BER should meet the desired BER of 1×10^{-7} for this case
CASE III . Heavy RFI (>5dB) . No Bit Slips at White Sands	1.2	$<10^{-7}$	Further study is required to determine the ability of the system during heavy RFI
CASE IV . Low RFI (~.7) . 10^{-11} Bit Slip Rate at White Sands	3.7	4.2×10^{-7}	Further analysis is needed to determine the impact of BSR and sync loss on the SYS.
CASE V . Medium RFI (2-5dB) . 10^{-11} Bit Slip Rate at White Sands	3.7	4.2×10^{-7}	Same as above

Assumptions: 1) The BER from ST to White Sands is 1×10^{-5}
 2) The BER from White Sands to STOCC at GSFC is 1×10^{-7}
 3) ST signal meets all other TDRSS requirements of reference 1.

NOTE: 1) The ST will not be allowed to transmit during periods of heavy RFI
 2) The BER for CASE IV and V is based on the lowest estimates for total data loss from Table 3.1

The utilization of the 255 PN sequence creates a potentially disastrous effect on the system BER. Since the sequence generator is reset by the sync pattern for the data segment (1024 bits), a loss of sync would result in the loss of at least one complete data segment. If the sequence generator is out of sync during the R/S check segment, the complete R/S block of 14336 data bits would be lost. This is due to the sequence being added after the data is R/S encoded.

Based on the above discussion an analysis, comparing the CCIR violation which occurs with and without the 255 PN sequence, should be conducted and based on the results, a determination concerning the removal of this sequence could be made.

CHAPTER 4

RECOMMENDATIONS AND RESULTS

The analysis in Section III indicates the S-band Single Access return link should expect a BER of less than 10^{-9} . This estimate is misleading since the system susceptibility to synchronization loss was not accurately represented. This fact is clearly illustrated by cases IV and V in Table 3.2. If a bit slip rate as low as 10^{-11} is assumed, the bit slip rate becomes the main controlling factor for the overall BER. A bit slip rate of 10^{-11} means the total system would lose sync once every 10^{11} channel symbols resulting in the loss of 1.4×10^4 to 3.1×10^4 information bits (see Table 3.1). Since one information bit equals 3 channel symbols, there are 3.3×10^{10} information bits between slips. The BER can be calculated using the following equation

$$\text{BER} = \frac{\text{number of information bits lost due to a slip}}{\text{number of information bits between slips}} \quad (4.1)$$

Substituting into Equation 4.1, the BER for the best case (1.4×10^4 information bits lost) and worst case (3.1×10^4 information bits lost) is found to be

$$\text{(best case) BER} = \frac{1.4 \times 10^4}{3.3 \times 10^{10}} = 4.2 \times 10^{-7}$$

$$\text{(worst case) BER} = \frac{3.1 \times 10^4}{3.3 \times 10^{10}} = 9.3 \times 10^{-7}$$

which is considerable higher BER than due to RFI, but zero

slip rate was assumed in Section 3 analysis (case I and II in Table 3.2).

A similar analysis would illustrate the effect on the system's BER due to the probability of sync loss by the other components. Thus the probability of sync loss for these components must be determined and included in the analysis for the system's BER.

An evaluation of the 1/3 rate Viterbi decoder should also be conducted to determine its actual operating characteristics, since the output burst property of the Viterbi decoder has a direct effect on the R/S decoder BER and the probability of the PN cover sequence losing sync.

The BER for the ESTR was stated to be 10^{-6} or better and its effect on the overall BER was neglected in Section 3. In actuality the ESTR may have substantial affect on the overall system BER due to the phase ambiguity resulting from converting to and from the recording code (Delay Modulation). For this reason the bit structure of the dummy data should be such that the 3 bit sync pattern, 010, appears frequently within the dummy segment.

The EIRP is another of the variables which has a substantial influence on the overall SSA Link BER. Table 4.1 lists the TDRSS EIRP requirements for the SSA Return Link. A reduction in the EIRP will result in an increase in the BER. For example if the antenna pointing system is off 4.6° from the center of beam between the ST and TDRS, the EIRP will be reduced by approximately 2 dB. This will increase the BER by at least two orders of

TABLE 4.1 TDRSS EIRP Requirements for the SSA Return Unit

Assumed Information (Uncoded) Data Rate = 10^6 bps
 Coded (1/2 Rate)Data; RF Channel Rate = 2×10^6 bps
 Coded (1/3 Rate)Data; RF Channel Rate = 3×10^6 bps
 Data Group I, Mode 3, Quadrative Channel Assumed

	NOV. 1976*	JAN. 1978**	DEC. 1979***
Uncoded Required	29.2 dbw	29.2 dbw	29.5 dbw (20.2 dbw)
Rate 1/2 Coded Required EIRP	24.0 dbw	24.0 dbw	24.3 dbw (25.0 dbw)
Rate 1/3 Coded Required EIRP that should meet 10 ⁻⁵ BER	23.5 dbw	23.5 dbw	23.8 dbw (24.5 dbw)
(A .5 db gain is used for Rate 1/3 over Rate 1/2 Coding, NASA TR R-396, Nov. 1972, page 20)			
Achievable Data Rate Without Coding (db relative to 1b/sec)	30.8+EIRP	30.8+EIRP	30.5+EIRP (29.8+EIRP-by mutual agreement only)
Achievable Data Rate with Rate 1/2 Coding (db relative to 1b/sec)	36.0+EIRP	36.0+EIRP	35.7+EIRP (35.0+EIRP-by mutual agreement only)

EXAMPLE: If Rate = 10^6 bps; $10 \log_{10} 10^6 = 60$ db = 30.8+EIRP
 Thus EIRP required = 60 - 30.8 = 29.2 dbw.

NOTE: Coding Rate 1/2 Assumes 5.2 db gain hence requiring less EIRP
 Both Rate 1/2 and Rate 1/3 Coding assumes K = 7.

* Performance Specifications for Services via the TDRSS, S-805-1, Nov. 1976
 ** TDRSS User's Guide, Revision 3, STDN, No. 101.2, Jan. 1978, page 3-15
 *** Performance Specification for Services via the TDRSS, S-805-1, Revision A, Dec. 1979, page 2-16 and 2-16A.

C 2

magnitude (case II of Table 3.2), assuming the Link Margin is held constant. Table 4.2 is a summary of the material used to calculate the values listed for cases I and II in Table 3.2 and the conditions under which these values are valid. For case III, the minimum value for $P_{VD}(\epsilon)$ and still maintain the desired overall BER of 10^{-7} was determined using Figure 4.2. Figure 4.1 was employed to obtain the minimum $(E_b/N_o)_1$ that would provide the required $P_{VD}(\epsilon)$. This value for $(E_b/N_o)_1$ was subtracted from the minimum $(E_b/N_o)_1$ (4.05 dB plus the 3.7 dB minimum expected Link margin per reference 19) to yield the Link Margin listed in Table 3.2.

Even taking into account the duplications and assumptions necessary to perform the analysis of Section 3, the SSA return... Link should still exceed the desired bit error rate of no more than one error in 10^{-7} bits. This is due mainly to the margins built into the system and to the results of test conducted by the various manufacturers as stated in the preceding sections. The system may even be able to operate during periods of heavy RFI.

It is recommended that during periods of heavy RFI, the system be used so as to determine both the actual performance capabilities of the system and to determine the actual RFI structure. Both of these objectives could be achieved through transmission of known bit patterns with specific structure.

TABLE 4.2

SSA PREDICTED PERFORMANCE

MODIFIED SYSTEMS: EIRP = 28.7 dbw - Rate 1/3 Convolutional Encoding
 EIRP Required by TDRSS for 10⁻⁵ BER Using Rate 1/2 Coding = 24.3 dbw (25.0 dbw)
 (References 5, page 2-22, paragraph 2.3.2.2.1, refers to Rate 1/2 Coding Requirement)
 Link Margin = 4.4 dbw (3.7 dbw) and expected BER = 10⁻⁵.

CASE I: Using rate 1/3 convolutional encoding we may expect 0.5 db increase (reference 13) in effective SNR over rate 1/2 convolutional encoding. Even though the WU TDRSS system will not guarantee an increase in performance over 10⁻⁵ BER an estimate is possible 10⁻⁵ BER out of Rate 1/2 VD is equivalent to a 4.7 db SNR into the rate 1/2 decoder (reference 14). A rate 1/3 encoded/decoded system should provide an average BER of 5x10⁻⁷ in theory. A performance curve for the Linkabit LV 7015 LR decoder (rate 1/3) shows an average BER of 10⁻⁶ (reference 2 and figure 4.1) LINK MARGIN = 4.4 dbw (3.7 dbw) and expected BER = 10⁻⁶ at worst. Using concatenated RS/CE/VD we observe from figure 4.2 the expected BER is much less than 10⁻¹² (reference 2, page 1-3).

CASE II: Using rate 1/2 convolutional encoding and R/S concatenation we must consider the burst lengths possible from the VD decoder and the probability of such bursts. Using a set of curves comparing the performance of Viterbi Decoding rate 1/2 (Linkabit data) and rate 1/3 (Batson data) (See figure 3.3 and reference 2) one may degrade the channel by 2 db (assumed to be due to RFI) which (holding the Link Margin Constant) will yield an output BER of approximately 5x10⁻⁴ for rate 1/3 (drawn off figure 4.1). From figure 3.3 we see that the average burst length would be approximately 12 bits long with approximately 6 bits being in error. (These are VD output bits.)

Neglecting any sync loss for the moment the PS outer codes will correct up to 505 bit bursts so a degradation in performance for this situation is not severe.

However if the sync pattern is involved in this error burst or if the VD cover sequence sync is lost then the accumulated errors can be quite significant.

The average BER should still be less than 10⁻¹⁰ (from figure 4.2 with BER from VD = 5x10⁻⁴).

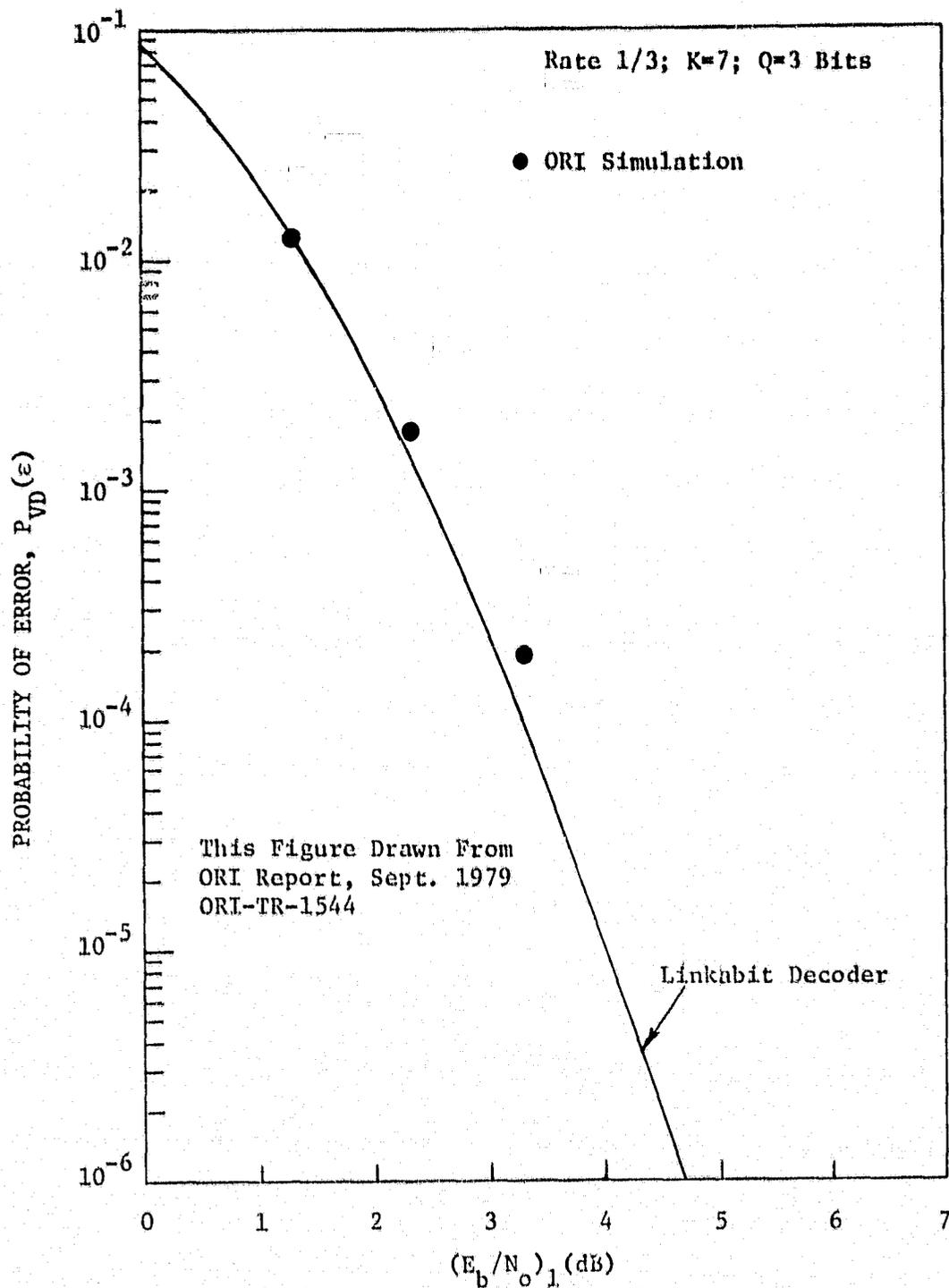


Figure 4.1 Probability of Error Versus Energy Per Bit to Noise Density Ratio for Rate 1/3 Soft Decision Viterbi Decoding with K=7

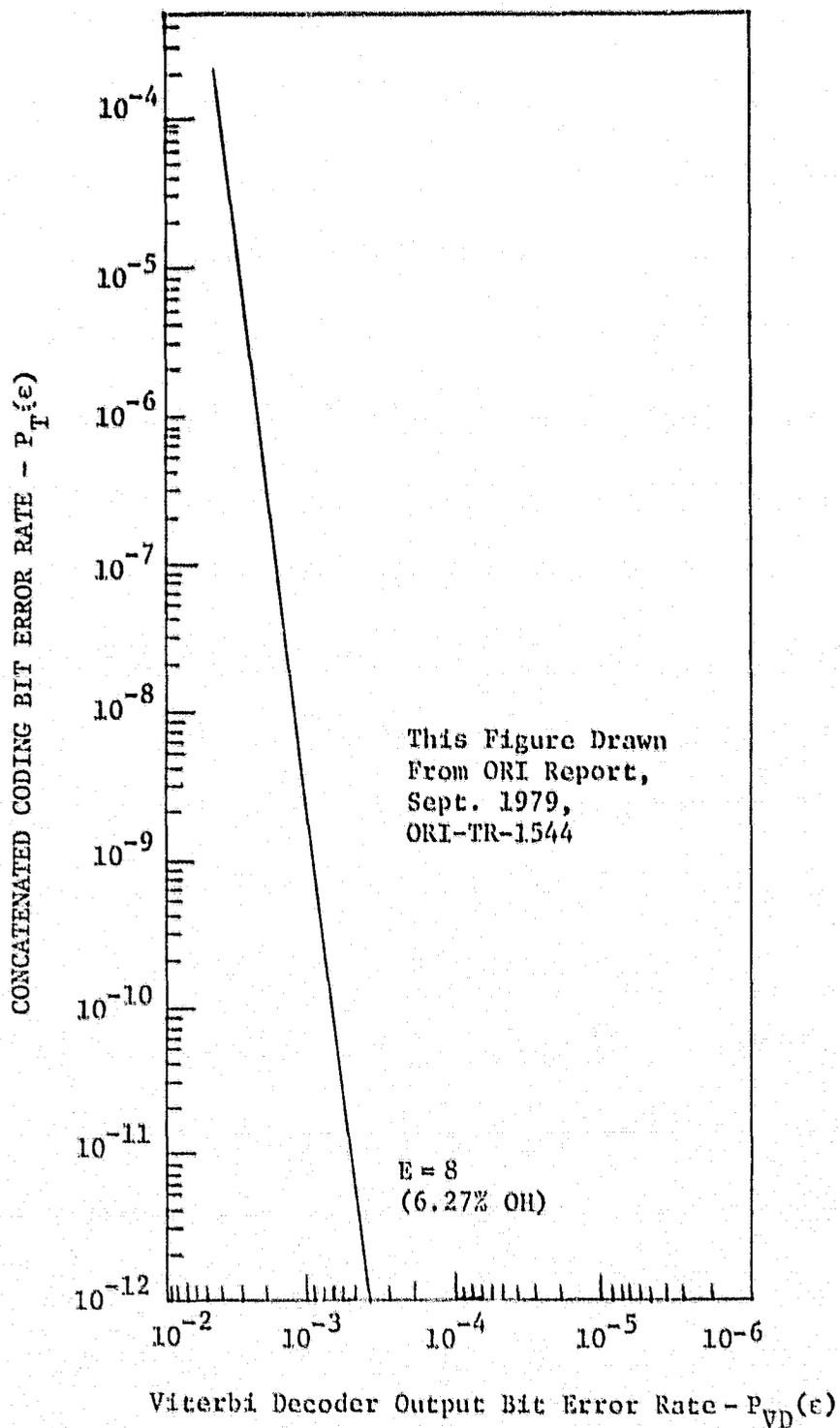


Figure 4.2 Concatenated Coding BER Versus TDRSS Channel Viterbi Decoded BER for $N/S (J=8)$

APPENDICES

APPENDIX 5.A

EXAMPLE OF A REED/SOLOMON ENCODER/INTERLEAVER

One information packet of 14 segments with 1024 bits per segment is to be coded. This will require 224 rows of the 239 rows reserved for information. The remaining 15 rows are considered to be filled with zeroes. The packet is passed by the R/S coder unchanged. After the last bit of the packet is passed by R/S coder, the 16 rows of check bits are sent.

Each of the eight R/S codes consist of 255 symbols of 8 bits, 239 information symbols and 16 check symbols. Let each symbol be an element of the Matrix. Using matrix notation, the R/S codes can be written in terms of data symbols and check symbols by

$$\text{R/S code \#M} = \Lambda_{9-M}$$

Example:

$$\text{R/S code \#1} = [\Lambda_{1,8}, \Lambda_{2,8}, \Lambda_{3,8}, \dots, \Lambda_{239,8}, \Lambda_{240,8}, \Lambda_{241,8}, \dots, \Lambda_{255,8}]^T$$

The R/S codes can also be written in terms of data bits and check bits by

$$\text{R/S code \#M} = \begin{bmatrix} 1 \\ (8M+b)+64a \\ \vdots \\ 0 \end{bmatrix}_{\substack{a=0 \\ b=-7}}^{238}, \begin{bmatrix} P \\ (8M+b)+64a \\ \vdots \\ 0 \end{bmatrix}_{\substack{a=0 \\ b=-7}}^{15}$$

Example:

$$\text{R/S code \#1} = \begin{bmatrix} I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8; I_{65}, I_{66}, \dots, I_{15285}; \\ P_1, P_2, P_3, P_4, P_5, P_6, P_7, P_8; P_{65}, P_{66}, \dots, P_{968} \end{bmatrix}^T$$

Since the information is read into the R/S system by rows and read out by rows, the system appears to have an interleaver of length 8, but the data is passed undisturbed.

An input of the form

$$I_N, \dots, I_3, I_2, I_1$$

$$N \leq 15,295$$

will have an output of the form

$$\dots, S_{2,7}, S_{2,8}, S_{1,1}, S_{1,2}, S_{1,3}, S_{1,4}, S_{1,5}, S_{1,6}, S_{1,7}, S_{1,8}$$

where $S_{n,m}$ is the element in the n^{th} row and m^{th} column of the matrix which is, also, the n^{th} symbol of the R/S code number 9-M or in terms of bits

$$\underbrace{P_{1024}, \dots, P_4, P_3, P_2, P_1}_{\text{Check Bits}} \underbrace{I_N, \dots, I_3, I_2, I_1}_{\text{Same as Input}}$$

Check Bits
(always 1024 bits)

Same as Input

I_1 represents bit one of the information data.

P_1 represents check bit one

Input to R/S encoder

$$I_N \dots I_4 I_3 I_2 I_1 \quad N \leq 15,296$$

Output of R/S encoder

$$P_{1024} \dots P_3 P_2 P_1 I_N \dots I_4 I_3 I_2 I_1$$

Same as Input

APPENDIX 5.B

DELAY MODULATION (MILLER COMPLEMENT)

Delay Modulation (DM) is a procedure for encoding binary data into rectangular waveforms of two levels according to the following rules:

1. A zero is represented by a transition from one level to the other at the midpoint of the bit cell.
2. A one is represented by no transition unless it is followed by another one. The case of consecutive ones is represented by a transition at the end of the leading one bit cell.

These rules are illustrated in Figure B.1.

Delay Modulation has several attractive properties:

1. The majority of the signaling energy lies in frequencies less than one-half the symbol rate.
2. The power spectrum is small in the vicinity of $f = 0$ (that is at D.C.).
3. DM provides at most one transition per bit cell and at the least 2 bit transitions every 3 bit cells; thus, providing a bit stream with a very high bit transition density.

These properties provide DM with the advantage of inherent self-timing information using phase modulation which is not present in NRZ-L, while requiring approximately the same bandwidth as NRZ-L. DM is also suitable for use with tape recorders, especially when higher packing density is required, or with systems which require high bit transition densities.

DM requires a given 3 bit sequence to assure proper bit sync. This sequence is 010. This sequence has a high probability of occurring one or more times in any random data bit stream. The probability that one or more 010-bit sequences will occur increases rapidly as the number of bits in the data sequence increases. The following equation may be used to obtain a close approximation of the probability of 010 occurring n or more times in m bits (the number of bits per sequence).

$$P_m(010 \geq n) = 1 - P_m(010 \leq n) = 1 - [P_m(010=0) + P_m(010=1) + \dots + P_m(010=(n-1))]$$

Where:

$$P_m(010=r) = \binom{k}{r} (q_0^{k-r}) (p_0^r)$$

$$q_0 = \text{the probability of any 3 bits not being 010} = \frac{7}{8}$$

$$p_0 = \text{the probability of any 3 bits being 010} = \frac{1}{8}$$

$$k = m - 2$$

$$\binom{k}{r} = \frac{k!}{(k-r)!r!}$$

For example, let m be 16 (for 16 binary bits) then the probability of a 010-bit sequence occurring one or more times is:

$$\begin{aligned} P_{16}(010 \geq 1) &= 1 - P(010=0) \\ &= 1 - \binom{14}{0} \left(\frac{7}{8}\right)^{14} \left(\frac{1}{8}\right)^0 = 1 - \frac{14!}{14!0!} \left(\frac{7}{8}\right)^{14} = 1 - \left(\frac{7}{8}\right)^{14} = 1 - .154 = .846 \end{aligned}$$

In other words, there is a 84.6% probability of a 010 pattern occurring and hence providing bit sync for a 16 bit sequence. Thus, we should expect a bit sync lock within a very short time upon the start of a DM encoded sequence.

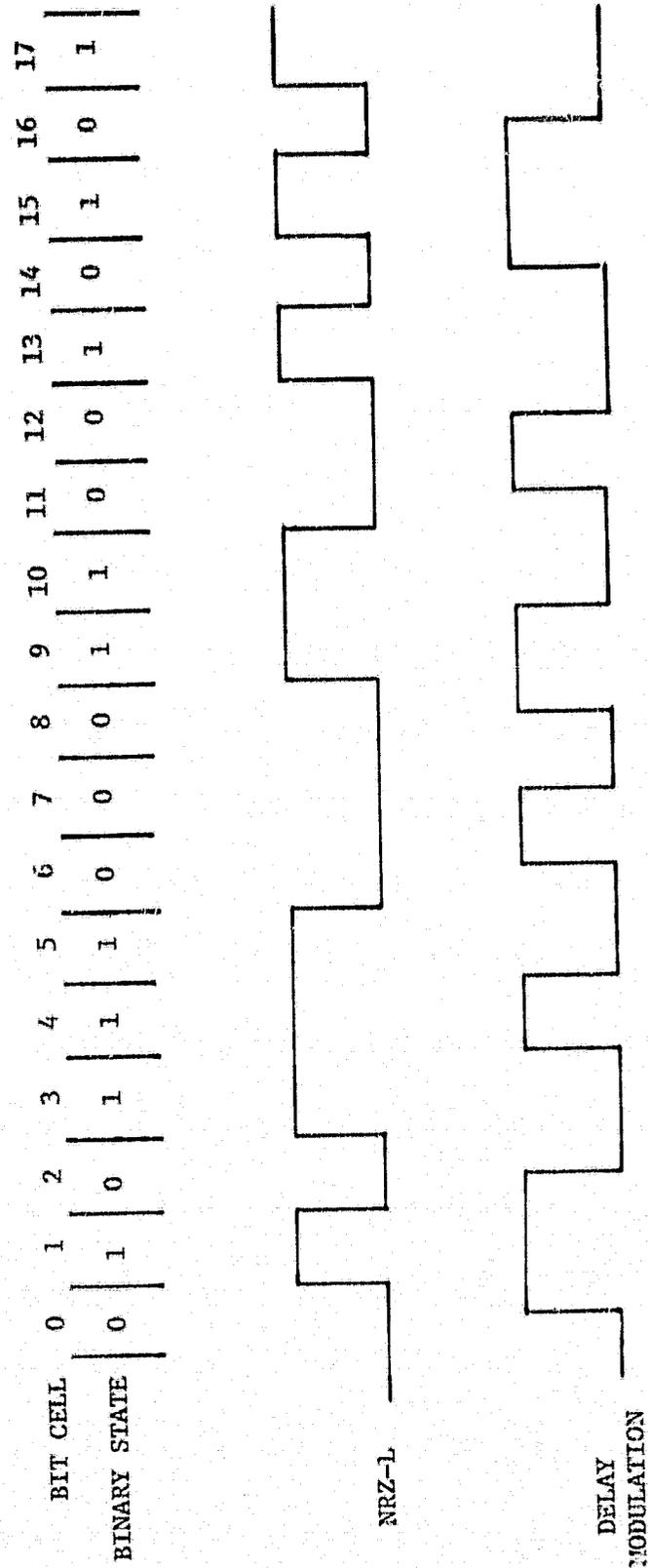


Figure B.1 NRZ-L and Delay Modulation Binary Signal Waveforms

APPENDIX 5.C

EXAMPLE OF A CONCATENATED CODE

Let us start with a code which is being used for error protection over a BSC channel. (Note this type of channel is a Digital error type or hard decision type channel).

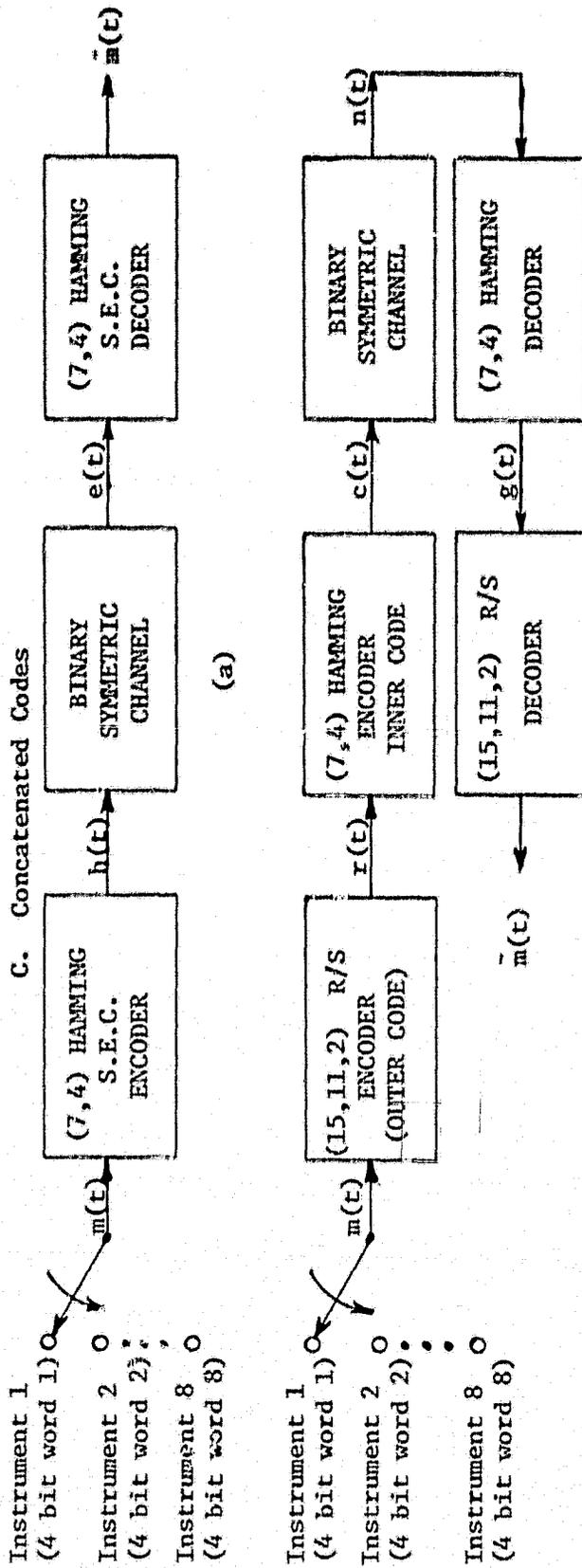
If we use a Hamming (7,4) SEC code (Figure C.1a) and if the probability of a bit being transmitted in error is $p = .025$, then the probability of a transmitted code word not being received (either with 0 errors or with a single correctable error) is

$$P(\text{u not received correctly}) = 1 - [P(0 \text{ errors}) + P(1 \text{ error})]$$
$$= \sum_{k=2}^7 \binom{7}{k} p^k (1-p)^{7-k} = .012071453 = .0121.$$

Now ask yourself how many different messages can we send with a Hamming (7,4) SEC code? The answer is of course 16 (or 15 if all zeroes are not used.)

Suppose we now construct a situation in which we have a source alphabet of 11 symbols. [If these were binary symbols, we could send 2^{11} messages = 2048. If these are 16 level symbols, we can send $16^{11} = 1.7592186 \times 10^{13}$ messages!]. Now, to send our original data, we merely encode 44 bit chunks rather than 4 bit chunks.

We use a R/S code that has as many different symbols as the original code accepted for messages. That is if the original code (outer code) accepted 4 bit message streams then each R/S symbol



Instrument 1
 (4 bit word 1) 0
 Instrument 2 0
 (4 bit word 2) 0
 Instrument 8 0
 (4 bit word 8) 0

Instrument 1
 (4 bit word 1) 0
 Instrument 2 0
 (4 bit word 2) 0
 Instrument 8 0
 (4 bit word 8) 0

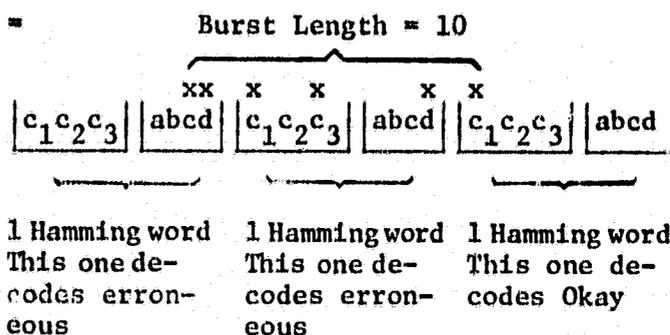
(b)

$$\begin{aligned}
 m(t) &= (WD8) \dots (WD2) (WD1) \\
 n(t) &= (C_1 C_2 C_3 WD8) \dots (C_1 C_2 C_3 WD2) (C_1 C_2 C_3 WD1) \\
 e(t) &= (C_1 C_2 C_3 WD8) \dots (C_1 C_2 C_3 WD2) (C_1 C_2 C_3 WD1) \\
 \bar{m}(t) &= (WD8) \dots (WD2) (WD1) \\
 r(t) &= (P_1 P_2 P_3 P_4 WD21 \dots WD12) (P_1 P_2 P_3 P_4 WD11 \dots WD1) \\
 c(t) &= (C_1 C_2 C_3 P_1) (C_1 C_2 C_3 P_2) \dots (C_1 C_2 C_3 WD2) (C_1 C_2 C_3 WD1) \\
 n(t) &= (C_1 C_2 C_3 P_1) (C_1 C_2 C_3 P_2) \dots (C_1 C_2 C_3 WD2) (C_1 C_2 C_3 WD1) \\
 g(t) &= (P_1 P_2 P_3 P_4 WD22 \dots WD12) (P_1 P_2 P_3 P_4 WD11 \dots WD2 WD1) \\
 m(t) &= (WD21) \dots (WD2) (WD1)
 \end{aligned}$$

must be expressible as 4 bits. Thus, if (7,4) code is outer code $2^4 = 16$ possible messages. Hence, R/S symbol must be 4 bits or 16 levels.

The probability of an error is now twofold in nature. Each channel transmission consists of one R/S symbol (4 bits) followed by 3 check digits for 7 total bits. Thus, it required an 11 digit burst to create a problem for the overall decoded output, since for a burst of 10 digit length only two R/S symbols are corrupted. (Remember the Hamming codewords can correct 1 error each.)

Channel Bit Stream =



.... abcd abcd^x abcd^x abcd to R/S Decoder → output correct.
 can correct 2 of
 15

Thus, a burst capability of 10 bits is now possible compared to the original 1 bit burst.

For random errors, we can correct up to 2 R/S symbols per 15 R/S symbols. Each symbol has probability of error equal to Prob. of word error of (7,4)SEC \approx .0121.

$$\begin{aligned}
 \therefore \text{Prob(of error)} &= 1 - [P_{R/S}^{(0 \text{ errors})} + P_{R/S}^{(1 \text{ errors})} + P_{R/S}^{(2 \text{ errors})}] \\
 &= 1 - [(1 - .0121)^{15} + 15 (.0121)(1 - .0121)^{14} + \binom{15}{2} (.0121)^2 (1 - .0121)^{13}] \\
 &= \underline{.0007} .
 \end{aligned}$$

If we interleave the R/S code (interleave R/S symbols) then the burst correction goes up by factor of n where n = depth of interleaving. R/S codes are particularly well suited to be used for concatenation since the outer coder failure typically results in bursty error failure and the R/S codes are particularly well adapted to burst correction if implemented with binary constructed symbols.

APPENDIX 5.D

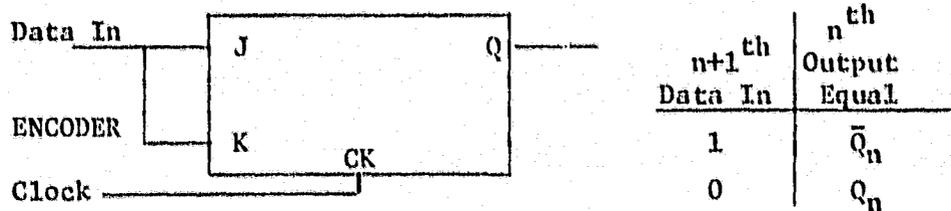
AFFECT OF PSK DEMODULATOR CARRIER SLIP
ON DIFFERENTIAL ENCODED DATA
WITH/WITHOUT INTERLEAVING

Differential Encoding

Rule: Using page 1-9 of Reference 3, 1's cause change in level

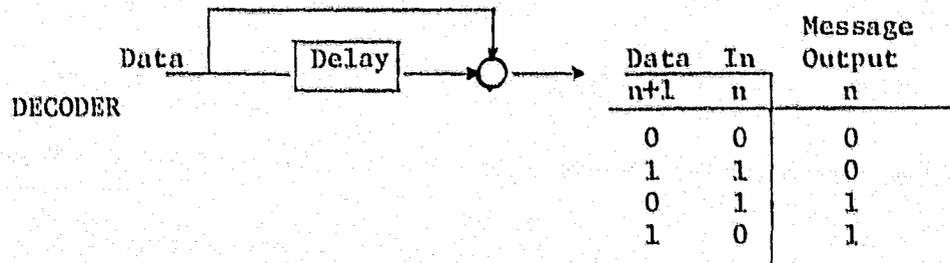
(Note, several possible rules to be used) 0's cause no change in level.

Use this with NRZ-M



Message in ... 1001000111001^{1st} ← assumed reference list in FF
That is $Q=0$ assumed

Output 0111000010111^{1st}

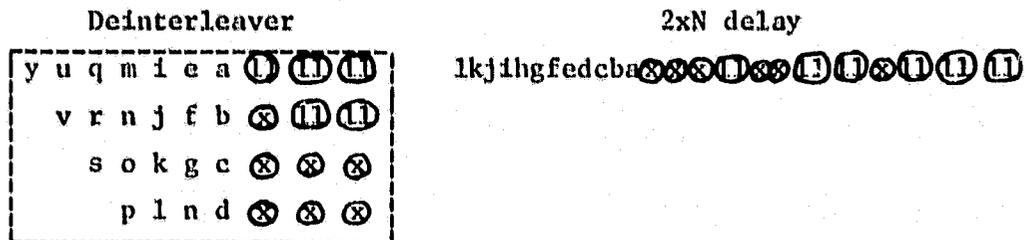


Recreated Message 10010000111001^{1st}

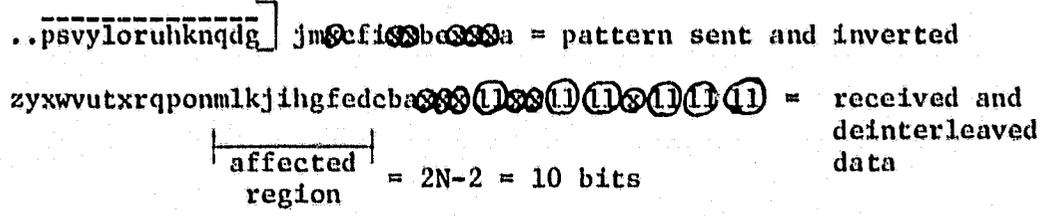
Now let us invert the bit stream so we receive

01110000] 10111^{1st}0
10001111] 10111^{1st}0 or 100011110] 0111^{1st}0

First we see it does work



Now lets send pattern and invert bit stream



Using data stream of previous example	received & deinter decoded data	1100001110011 0100010010101 xx x x x xx
---------------------------------------	---------------------------------	---

INTERLEAVING HELPS BURSTS ON CHANNEL BUT HURTS DIFF. ENCODING/
DECODING IF PSK DEMODULATOR EXHIBITS CYCLE SLIP!

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