NOTICE

THIS DOCUMENT HAS BEEN REPRODUCED FROM MICROFICHE. ALTHOUGH IT IS RECOGNIZED THAT CERTAIN PORTIONS ARE ILLEGIBLE, IT IS BEING RELEASED IN THE INTEREST OF MAKING AVAILABLE AS MUCH INFORMATION AS POSSIBLE.
HIGH SPEED CMOS/SOS STANDARD CELL NOTEBOOK

By RCA
Advanced Technology Laboratories
Government and Commercial Systems
Camden, New Jersey 08102

September 1978

Prepared for

NASA-George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812
This report describes the NASA/MSFC high-speed CMOS/SOS standard cell family. The cells were designed to be compatible with the PR2D (Place, Route in 2-Dimensions) Automatic Layout Program. Included are cell descriptions and the standard cell data sheets for each cell. Each cell sheet includes the logic diagram, the schematic, the truth table, and propagation delays for each logic cell.
## CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>II</td>
<td>HIGH SPEED CMOS/SOS STANDARD CELL FAMILY</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>A. Cell Descriptions</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>B. Procedure for Generating Dynamic Data</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>C. Additional Cell Data</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>APPENDIX</td>
<td>15</td>
</tr>
</tbody>
</table>
LIST OF CMOS/SOS STANDARD CELL DATA SHEETS

1120 Two-Input NOR
1130 Three-Input NOR
1140 Four-Input NOR
1220 Two-Input NAND
1230 Three-Input NAND
1240 Four-Input NAND
1310 Buffer Inverter
1340 Two to One Clocked Trans. Gate
1370 Low Z Transmission Gate
1510 Non-Inverting Buffer
1510 Double Buffer Inverter
1570 On-Chip Tristate
1620 Two-Input AND
1630 Three-Input AND
1640 Four-Input AND
1720 Two-Input OR
1730 Three-Input OR
1740 Four-Input OR
1870 Two, Two AND-Two NOR
1890 Two, Two AND-Three NOR
2000 J/K Flip-Flop with Set/Reset
LIST OF CMOS/SOS STANDARD CELL DATA SHEETS (Concluded)

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020</td>
<td>D Type, M/S S/It Flip-Flop</td>
</tr>
<tr>
<td>2310</td>
<td>Exclusive OR</td>
</tr>
<tr>
<td>2570</td>
<td>Off Chip Tristate Pad</td>
</tr>
<tr>
<td>2810</td>
<td>D Flip-Flop with Inverted Output</td>
</tr>
<tr>
<td>2820</td>
<td>D Type M/S Flip-Flop</td>
</tr>
<tr>
<td>2830</td>
<td>D Flip-Flop with Feedback Loop</td>
</tr>
<tr>
<td>2840</td>
<td>D Flip-Flop with Reset</td>
</tr>
<tr>
<td>7000</td>
<td>PLA Input Decoder</td>
</tr>
<tr>
<td>7010</td>
<td>PLA Output Function String</td>
</tr>
<tr>
<td>9020</td>
<td>Off-Chip Tristate Pad</td>
</tr>
<tr>
<td>9030</td>
<td>Input Inverter Buffer Pad</td>
</tr>
<tr>
<td>9040</td>
<td>Input Inverter Buffer Pad</td>
</tr>
<tr>
<td>9050</td>
<td>Off-Chip Tristate Pad</td>
</tr>
<tr>
<td>9060</td>
<td>Off-Chip Inverting Buffer Pad</td>
</tr>
<tr>
<td>9070</td>
<td>Off-Chip Inverting Buffer Pad</td>
</tr>
<tr>
<td>9130</td>
<td>Buffered Non-Inverting Input Pad</td>
</tr>
<tr>
<td>9140</td>
<td>Buffered Non-Inverting Input Pad</td>
</tr>
</tbody>
</table>
1. INTRODUCTION

This report describes the NASA-MSFC high speed CMOS/SOS standard cell family, which was developed on (1) NASA programs NAS12-2233 and NAS8-29072 under the direction of John Gould, NASA Technical Program Director, MSFC, Huntsville, Alabama, and (2) internal Independent Research and Development programs.

The circuits were designed to be compatible with and maximize the performance of the Automatic Placement and Routing Program PI2D which was also originally developed under NASA program NAS12-2233 directed by John Gould and improved on other Government programs as well as on several Independent Research and Development programs. Together the program and circuits provide the capability of generating high speed, high performance, random logic custom LSI arrays with quick turnaround, high density, and low static and dynamic power.

The basic technology with which circuits are designed is the self-aligned, silicongate CMOS/SOS process.

These cells are used in the generation of design automated custom LSI arrays in virtually the same manner as other RCA-designed standard cell families. Briefly this requires user-generated input data to the computer program which consists of the net or connectivity list of circuit cells as well as the cell or pattern identification numbers which is available from the data sheets. With essentially this information, the computer placement and routing program will provide an automatically generated layout and interconnection in a data format consistent and compatible with an automatic precision mask artwork pattern generator.
This report contains standard cell data sheets for each of the cells. It contains a description of the general information and data that are contained on all data sheets. It also contains additional information and descriptions where appropriate. For example, additional information is provided as to how the dynamic performance curves shown on the data sheets were generated, the validation process, and the means by which their accuracy will be updated. A user's guide is planned, which will complement the data contained here, to provide the design information necessary for complete user utilization.

II. HIGH SPEED CMOS/SOS STANDARD CELL FAMILY

A. CELL DESCRIPTIONS

The table lists the cells that currently make up the CMOS/SOS standard cell family. Data sheets are contained for these cells in the Appendix. Where necessary, the accompanying table contains information additional to that on the data sheets to describe cell operation.

Each data sheet contains the following information:

- Cell family technology.
- Descriptive name of the cell indicating its function.
- Cell identification or pattern number. This number identifies the cell in the input data to the automatic placement and routing program.
- Supply voltage for which the given propagation delay and transition times are applicable.
- Width of the cell in mils.
• Circuit schematic of the logic configuration including the numbering of each input and output connection. These numbers provide the means by which the chip interconnection or net list is generated.

• Capacitance at each input and output connection. This capacitance is computed on the basis of the geometry, topology, and materials associated with the capacitor. The Miller effect is not included in value. It is automatically included when the device is analyzed by computer simulation techniques.

• Logic symbol plus the Boolean equation describing the cell function.

• Truth table.

• Dynamic performance data.

Dynamic performance data at $V_{DD} = 10\ V$ is provided for each logic cell. These data may be presented in several ways. These include propagation delay on a per stage basis, transition time, clock rate, minimum or maximum pulse width, delay measured with respect to the clock, or combinations of these. In all cases the dynamic data are given as a function of load capacitance.

For logic cells like the 1120, 1130, 1140, 1220, 1230, 1240, 1310, 1520 and the 1620, the delay is given in the form of curves showing stage delay and transition times as a function of capacitive loading. The stage delay is the average of the propagation delay as measured at the 50 percent signal swing level for positive and negative going input signals. Similarly, the transition time is measured over the 10 to 90 percent rise and fall times. The input signal to these circuits during the generation of these data is the output of an inverter stage which acts as a buffer against the programmed input pulse. The principal objective of this buffer is to minimize the effect of the transition time of the input on the dynamic data. The dependency, nevertheless, exists and should be considered.
In contrast to this, the dynamic data for those circuits which contain storage devices are given in terms of the minimum pulse width to transfer new data into the master and slave storage elements as well as propagation delay data. In the latter case, the delay is specified from the 50 percent level of the negative transition of the clock to the 50 percent level of the output of the slave.

As new cells are added to the CMOS/SOS family, they will be dynamically characterized in a manner that will optimize the cell's usefulness to the system designer.

B. PROCEDURE FOR GENERATING DYNAMIC DATA

The dynamic data shown on the data sheets are based on computer simulation techniques using a RCA-developed computer circuit analysis and simulation program. Primarily developed for integrated circuit application, the program contains specially developed device models with parameters expressed in process parameters as well as circuit parameters. To characterize a particular process, the parameters of the device models are provided values that correspond directly to the process being used.

A detailed description of how the dynamic data were generated can be found in the final report.1

Briefly, however, each cell was simulated as follows: all transistors were simulated by a device model that included its mask geometries; electrical characteristics like threshold voltages; intrinsic capacitances, process parameters values for mobility, gate oxide, field oxide thickness, and permittivity;

effect of lateral diffusions expressed in terms of modified channel length; and resistance associated with the polysilicon gate and intracell connections. Each cell was analyzed with a load that consists of a series resistor and capacitive load. The series resistor represents the anticipated average resistance that a typical cell will be driving as a result of polysilicon interconnections. In addition, the cell being analyzed is driven by an inverter circuit which is designed to provide a signal that simulates the input signal which it normally encounters in a CMOS/SOS LSI array environment.

A key to the accuracy and reliability of the results produced by the analysis and simulation techniques lies in the accuracy and validity of the values used to define the parameters of the device models. To date RCA has produced more than 50 CMOS/SOS LSI arrays including at least four test chips. Although all of the test chips, including the one described in the reference NASA final report, were designed for different purposes, each one had special circuits designed to characterize the process and generate device model parameter values. Then, as the various functional CMOS/SOS arrays were fabricated and tested, the values of the parameters were improved and updated. In this way, the accuracy and validity of the model are established with a corresponding increase in the accuracy and validity of the performance predicted by the simulation techniques. As additional CMOS/SOS LSI arrays are produced using the CMOS/SOS standard cell family, the model and its parameter values will continue to be improved and updated.

Although the stage propagation delays and transition times given in the data sheets are specifically for a 10-V $V_{DD}$, they can be used to a first-order approximation to provide corresponding cell information at supply voltages other than 10 V. For example, at 5-V $V_{DD}$ and assuming a threshold voltage for P and N at 1.5 V, the delay will be reduced as compared to the 10-V data as follows:
Reduction in stage delay at 5 V = \left[ \frac{(10 - 1.5)^2}{(5 - 1.5)^2} \right] \cdot \left( \frac{5}{10} \right) \cdot (0.8) = 2.4

The 0.8 factor in the equation is an empirical figure that is considered reasonably conservative.

C. ADDITIONAL CELL DATA

1. D-Type, Master/Slave Flip-Flop (Cell No. 2820)

This cell is a true master-slave flip-flop designed for various register applications. With the addition of an external inverter, such as the 1310 or 1520 cell, it may be used for counter and toggle applications. Information is stored by means of tristate type devices, ensuring a data input characteristic that is purely capacitive. Data present at the "D" input are transferred to the "Q" output during the negative-going transition of the clock pulse. Loading the master flip-flop is initiated on the positive-going edge of the clock pulse.

Operating Characteristics

- Clock should remain in the high state for a minimum of 22 ns to insure a proper transfer of the data information into the master flip-flop.
- The clock should remain in the low state for a minimum of 20 ns to insure a proper transfer of the master data to the slave flip-flop.
- The clock transition (10-90 percent) edge time should be kept below 60 ns.
- For output loading on "Q" greater than 0.4 pF, allow a minimum of 26 ns to transfer the data to slave and latch it in.
The cell is implemented with a combination of functional, transmission gate, and tristate logic. The transmission devices are used to connect (and disconnect) the master and slave storage devices from the "D" input and master rank, respectively. Each storage element is implemented with a single inverter and a low conductance feedback tristate device. Information is held by means of the smaller, high impedance tristate inverter. The outputs of these tristate inverters are disconnected while their particular flip-flop is being loaded.

Latch-up occurs during the transition time of the clock signal, during the falling edge for the master flip-flop, and during the rising edge for the slave flip-flop. At this time, the transmission devices are disconnecting. When the clock signal is high, the logical level at the "D" input is propagated through the first transmission device and loaded into the inverter of the master flip-flop. When the clock signal goes from a high to a low (1 to 0) state, two simultaneous events occur. The master's tristate begins to maintain and define the logical level at the input to the master rank, and the input transmission device begins to isolate the master rank from the "D" input. Concurrent with these events, the second transmission device begins to connect the slave to the master. Opposition from the slave's feedback tristate is eliminated by disconnecting the output from this node.

2. Off-Chip Inverting Buffer Pad (Cells No. 9060 and 9070)

These cells are designed for driving large off-chip capacitive loads. To increase the gate density of the arrays using the drivers, the cells have been incorporated into an output pad design. Consequently, they are placed in the pad area. The two cells differ only in their ground and power bus connection.
<table>
<thead>
<tr>
<th>Cell Number</th>
<th>Cell Function</th>
<th>Description/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1120</td>
<td>Two-Input NOR</td>
<td>Logical NOR</td>
</tr>
<tr>
<td>1130</td>
<td>Three-Input NOR</td>
<td>Logical NOR</td>
</tr>
<tr>
<td>1140</td>
<td>Four-Input NOR</td>
<td>Logical NOR</td>
</tr>
<tr>
<td>1220</td>
<td>Two-Input NAND</td>
<td>Logical NAND</td>
</tr>
<tr>
<td>1230</td>
<td>Three-Input NAND</td>
<td>Logical NAND</td>
</tr>
<tr>
<td>1240</td>
<td>Four-Input NAND</td>
<td>Logical NAND</td>
</tr>
<tr>
<td>1310</td>
<td>Buffer Inverter</td>
<td>On-chip operation with loads up to 4 pF</td>
</tr>
<tr>
<td>1340</td>
<td>Inverting 2 x 1</td>
<td>When the control is in the high state (10 V), the output is $\bar{A}$. When the</td>
</tr>
<tr>
<td></td>
<td>Multiplexer</td>
<td>control is low, the output is $B$.</td>
</tr>
<tr>
<td>1370</td>
<td>Low Z Transmission</td>
<td>Electronic equivalent of a single pole, single throw switch. When the</td>
</tr>
<tr>
<td></td>
<td>Gate</td>
<td>control is in the low state, the input and output are effectively disconnected and</td>
</tr>
<tr>
<td></td>
<td></td>
<td>the other node either floats or is defined by other circuit elements. In the high</td>
</tr>
<tr>
<td></td>
<td></td>
<td>state, the transmission gate is in the &quot;ON&quot; state with the output connected to the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>input with a series resistance of approximately 2000 ohms.</td>
</tr>
<tr>
<td>1510</td>
<td>Non-Inverting</td>
<td>Primarily designed for &quot;on-chip&quot; use, this cell can be used to reduce delays when</td>
</tr>
<tr>
<td></td>
<td>Buffer</td>
<td>the load capacitance exceeds 2 pF.</td>
</tr>
<tr>
<td>Cell Number</td>
<td>Cell Function</td>
<td>Description/Comments</td>
</tr>
<tr>
<td>-------------</td>
<td>---------------------</td>
<td>---------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1520</td>
<td>Double Buffer Inverter</td>
<td>For capacitance loads in excess of 4 pF</td>
</tr>
<tr>
<td>1570</td>
<td>On-Chip Tristate</td>
<td>This cell is a tristate device designed for on-chip use. A control is available to determine the operation mode of this cell. With the control high, the cell operates as an inverter buffer capable of driving heavy on-chip loads. With the control low, the cell is in the 'OFF' state, with an extremely high output impedance — on the order of 0.1 pF. This permits the use of bidirectional busses on the chip.</td>
</tr>
<tr>
<td>1620</td>
<td>Two-Input AND</td>
<td>Logical AND through two functional stages</td>
</tr>
<tr>
<td>1630</td>
<td>Three-Input AND</td>
<td>Logical AND through two functional stages</td>
</tr>
<tr>
<td>1640</td>
<td>Four-Input AND</td>
<td>Logical AND through two functional stages</td>
</tr>
<tr>
<td>1720</td>
<td>Two-Input OR</td>
<td>Logical OR through two functional stages</td>
</tr>
<tr>
<td>1730</td>
<td>Three-Input OR</td>
<td>Logical OR through two functional stages</td>
</tr>
<tr>
<td>1740</td>
<td>Four-Input OR</td>
<td>Logical OR through two functional stages</td>
</tr>
<tr>
<td>1870</td>
<td>Two, Two and-Two NOR</td>
<td>This cell performs the function $Z = AB + CD$. Drive capability and performance are similar to the 1120 type cell.</td>
</tr>
<tr>
<td>Cell Number</td>
<td>Cell Function</td>
<td>Description/Comments</td>
</tr>
<tr>
<td>-------------</td>
<td>--------------------------------------</td>
<td>--------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1890</td>
<td>Two, Two, Two And-Three NOR</td>
<td>This cell performs the function $Z = AB + CD + EF$. Drive capability and performance are similar to the 1130 type cell.</td>
</tr>
<tr>
<td>2000</td>
<td>J/K Flip Flop with Set/Reset</td>
<td>This cell is one of the more complex of the standard cells. Both the set and reset are unconditional except that the two positive pulses must not be applied simultaneously. The truth table, shown below, was extracted from the data sheet.</td>
</tr>
</tbody>
</table>
|             |                                      | $\begin{array}{cccccc}
C & J & K & S & R & Q \\
\hline
0 & 0 & 0 & 0 & 0 & Q_{n-1} \\
1 & 0 & 0 & 0 & 1 & \\
0 & 1 & 0 & 0 & 0 & \\
1 & 1 & 0 & 0 & Q_{n-1} & \\
* & * & 0 & 0 & Q_{n-1} & \\
* & * & 1 & 0 & 1 & \\
* & * & 0 & 1 & 0 & \\
* & * & 1 & 1 & \text{Prohibited} & \\
\end{array}$ |
<p>|             |                                      | Note: $Q_{n-1}$ is state of flip-flop before last clock transition.                  |
|             |                                      | * Don't care condition                                                              |
| 2020        | D-Type, M/S, S/R Flip-Flop           | This is another of the more complex of the standard cells. Both the set and reset are unconditional except that the two positive pulses must not be applied simultaneously. The truth table, shown below, was extracted from the data sheet. |</p>
<table>
<thead>
<tr>
<th>Cell Number</th>
<th>Cell Function</th>
<th>Description/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Clock</strong></td>
<td>C&lt;sub&gt;lock&lt;/sub&gt; D R S Q Q</td>
</tr>
</tbody>
</table>
|             |                                       | \[
|             |                                       |   0 0 0 0 1                                                                          |
|             |                                       |   1 0 0 1 0                                                                          |
|             |                                       |   * 1 0 0 1                                                                          |
|             |                                       |   * 0 1 1 0                                                                          |
|             |                                       |   * 1 1 ■ ■                                                                          |

* - Don't Care Case  
■ - Undefined Output Case

2310          | Exclusive OR                          | Exclusive OR through a unique combination of four transistors.                     |
2570          | Off-Chip Tristate Pad                 | A special off-chip tristate device with 5 times the drive power of the 9020/9050 cell. |
2810          | D Flip-Flop with Inverter Output      | This cell is one of three latches in the cell family. This cell provides all the functions of the 2830 cell except that it provides an output in which the polarity of the data is inverted. |
2820          | D Type Master-Slave Flip-Flop         | See Section II C 1.                                                                |
2830          | D Flip-Flop with Open Feed-Back Loop  | This cell performs the function Q = D<sup>C</sup> + Q<sub>n-1</sub> where D is the data input, C is the clock or control element, Q is the output of the latch and Q<sub>n-1</sub> is the state of the latch prior to application of the negative clock. This cell can be used as an input or output register element, for buffering, for temporary storage, and as a control flip-flop. |
<table>
<thead>
<tr>
<th>Cell Number</th>
<th>Cell Function</th>
<th>Description/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>2840</td>
<td>D Flip-Flop with Reset</td>
<td>This cell is the third of the latch type cells in the CMOS/SOS cell family.</td>
</tr>
<tr>
<td>7000</td>
<td>PLA Input Decoder</td>
<td>This cell, together with the 7010, provides a PLA function. This cell provides a full three-input decoded output with an inhibit control that permits expandability. Functionally the cell consists of eight 4-input gates with each providing the full 3 data input decoding.</td>
</tr>
<tr>
<td>7010</td>
<td>PLA Output Function String</td>
<td>This cell provides the programmable part of the PLA through mask programming. It essentially provides the 'OR' function and may be cascaded serially to provide more complex logic functions.</td>
</tr>
<tr>
<td>9020/9050</td>
<td>Off-Chip Tristate Pad</td>
<td>These cells are tristate high current drivers designed to drive high capacitance &quot;off-chip&quot; loads. The state of these cells are determined by a control input. When the control is high the cells are low Z, non-inverting buffers. When control is low, devices become high impedance devices that may be common bussed or phantom ORed. The two cell types are distinguished by their location and orientation in the street area.</td>
</tr>
<tr>
<td>9030/9040</td>
<td>Input Inverter Buffer Pad</td>
<td>An input pad that provides waveform shaping buffering and signal inversion.</td>
</tr>
</tbody>
</table>
TABLE (Concluded)

<table>
<thead>
<tr>
<th>Cell Number</th>
<th>Cell Function</th>
<th>Description/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>9060/ 9070</td>
<td>Off-Chip Inverting Buffer Pad</td>
<td>See Section II C. 2.</td>
</tr>
<tr>
<td>9130/ 9140</td>
<td>Buffered Non-Inverting Input Pad</td>
<td>An Input pad that provides waveform shaping and buffering with no signal inversion.</td>
</tr>
</tbody>
</table>
TWO—INPUT NOR

SOS STANDARD
CELL NO. 1120

4 DEVICES
3 PADS
CELL WIDTH = 3 MILES

V_{DD} = 10 V

SCHEMATIC

LOGIC SYMBOL

TRUTH TABLE

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.030</td>
</tr>
<tr>
<td>3</td>
<td>0.265</td>
</tr>
<tr>
<td>4</td>
<td>0.265</td>
</tr>
</tbody>
</table>

PIN CAPACITANCE (pF)

TOTAL LOAD CAPACITANCE (pF)

STAGE DELAY (ns)

RISE/FALL, 10-90% (ns)
THREE-INPUT NOR

SOS STANDARD
CELL NO. 1130

6 DEVICES
4 PADS
CELL WIDTH = 4 MILS

VDD = 10 V

SCHEMATIC

LOGIC SYMBOL

X = A + B + C

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

PIN | CAPACITANCE (pF)
---|------------------
2  | 0.060
3  | 0.375
4  | 0.375
5  | 0.375

TOTAL LOAD CAPACITANCE

STAGE DELAY (ns)

Rise/Fall, 10/90% (ns)

TOTAL LOAD CAPACITANCE (pF)
FOUR-INPUT NOR

SOS STANDARD
CELL NO. 1140

8 DEVICES
5 PADS  CELL WIDTH = 5 MILS  V_DD = 10 V

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.070</td>
</tr>
<tr>
<td>3</td>
<td>0.450</td>
</tr>
<tr>
<td>4</td>
<td>0.450</td>
</tr>
<tr>
<td>5</td>
<td>0.450</td>
</tr>
<tr>
<td>6</td>
<td>0.450</td>
</tr>
</tbody>
</table>

SCHEMATIC

LOGIC SYMBOL

X = A + B + C + D

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

ALL OTHER INPUT
COMBINATIONS 0

STAGE DELAY (ns)

RISE/FALL - 10-90% (ns)
TWO-INPUT NAND

SOS STANDARD
CELL NO. 1220

4 DEVICES
3 PADS
CELL WIDTH = 3 MILS

V<sub>DD</sub> = 10 V

LOGIC SYMBOL

X = A \cdot B

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

PIN | CAPACITANCE (pF)
---|-------------------|
2  | 0.201             |
3  | 0.201             |
4  | 0.043             |

STAGE DELAY (ns)

0  | 5  | 10 | 15 | 20
---|----|----|----|----
0.5 | 5  | 10 | 15 | 20
1.0 | 5  | 10 | 15 | 20
1.5 | 5  | 10 | 15 | 20
2.0 | 5  | 10 | 15 | 20

RISE/FALL TIME (ns)

0  | 5  | 10 | 15 | 20
---|----|----|----|----
0.5 | 5  | 10 | 15 | 20
1.0 | 5  | 10 | 15 | 20
1.5 | 5  | 10 | 15 | 20
2.0 | 5  | 10 | 15 | 20
THREE-INPUT NAND

SOS STANDARD
CELL NO. 1230

6 DEVICES
4 PADS

CELL WIDTH = 4 MILS

VDD = 10 V

SCHEMATIC

LOGIC SYMBOL

X = A · B · C

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

PIN CAPACITANCE (pF)

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.266</td>
</tr>
<tr>
<td>3</td>
<td>0.266</td>
</tr>
<tr>
<td>4</td>
<td>0.266</td>
</tr>
<tr>
<td>5</td>
<td>0.076</td>
</tr>
</tbody>
</table>

TOTAL LOAD CAPACITANCE (pF)

STAGE DELAY (ns)

RISE/FALL (10-90%) (ns)

TOTAL LOAD CAPACITANCE (pF)

ORIGINAL PAGE IS OF POOR QUALITY
FOUR-INPUT NAND

SOS STANDARD
CELL NO. 1240

0 DEVICES
0 PADS
CELL WIDTH = 5 MILS

VDD = 10 V

LOGIC SYMBOL

X = A · B · C · D

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

ALL OTHER INPUT COMBINATIONS 1

PIN   CAPACITANCE (pF)
---   -----------
2     0.319
3     0.319
4     0.319
5     0.319
6     0.142

STAGE DELAY (ns)

RISE/FALL (10-90%) (ns)

TOTAL LOAD CAPACITANCE (pF)
BUFFER INVERTER

SOS STANDARD
CELL NO. 1310

2 DEVICES
2 PADS
CELL WIDTH = 2 MILS

V<sub>DD</sub> = 10 V

SCHEMATIC

LOGIC SYMBOL

TRUTH TABLE

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.010</td>
</tr>
<tr>
<td>3</td>
<td>0.311</td>
</tr>
</tbody>
</table>

PIN | CAPACITANCE (pF) |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
</tr>
</tbody>
</table>

Graphs showing stage delay and rise/fall time vs. total load capacitance.
INVERTING 2X1 MULTIPLEXER

SOS STANDARD CELL NO. 1340

10 DEVICES
4 PADS

CELL WIDTH = 5.0 MILS

V_DD = 10 V

PIN | CAPACITANCE (pF)
---|------------------
2  | 0.38
3  | 0.01
4  | 0.41
5  | 0.69

LOGIC SYMBOL

CA + CB = Z

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

SCHMATIC

LOGIC SYMBOL

CA + CB = Z

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

STAGE DELAY (ns)

A, B, OR C INPUT

20

15

10

5

0

TOTAL LOAD CAPACITANCE (pF)

RISE/FALL 10-90% (ns)

20

15

10

5

0

TOTAL LOAD CAPACITANCE (pF)
TRUTH TABLE

<table>
<thead>
<tr>
<th>D</th>
<th>C</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>*</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>*</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

* OUTPUT IS UNDEFINED, HI Z STATE

PIN CAPACITANCE (pF)

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.255</td>
</tr>
<tr>
<td>3</td>
<td>0.078</td>
</tr>
<tr>
<td>4</td>
<td>0.335</td>
</tr>
</tbody>
</table>

VDD = 10V

SOS STANDARD
CELL NO. 1370

4 DEVICES
3 PADS
CELL WIDTH = 4 MILS

SCHEMATIC

LOGIC SYMBOL

X = DC

HIGH Z DRIVER

HI Z DRIVER

LOW Z DRIVER

TOTAL LOAD CAPACITANCE (pF)

TOTAL LOAD CAPACITANCE (pF)

C INPUT HI Z DRIVER

C IN LOW Z

D IN

HIGH Z DRIVER

LOW Z DRIVER

STAGE DELAY (ns)

RISE/FALL, 10-90% (ns)
NON-INVERTING BUFFER

SOS STANDARD
CELL NO. 1510

4 DEVICES
2 PADS

CELL WIDTH =

$V_{DD} = 10 \text{ V}$

SCHEMATIC

LOGIC SYMBOL

X = A

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

PIN | CAPACITANCE (pF) |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.310</td>
</tr>
<tr>
<td>3</td>
<td>0.010</td>
</tr>
</tbody>
</table>

Stage Delay (ns)

- Rise/Fall, 10-90% (ns)

- Total Load Capacitance (pF)

- Total Load Capacitance (pF)
DOUBLE BUFFER INVERTER

SOS STANDARD
CELL NO. 1520

2 DEVICES
2 PADS
CELL WIDTH = 3 MILS
VDD = 10 V

SCHEMATIC

LOGIC SYMBOL

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

PIN | CAPACITANCE (pF) | TOTAL LOAD CAPACITANCE (pF) | TOTAL LOAD CAPACITANCE (nF)
---|------------------|-----------------------------|-----------------------------
2  | 0.022            | 0.622                       | 0.010                       | 0.622                       | 0.010                       |
3  | 0.010            | 0.010                       | 0.010                       | 0.010                       | 0.010                       |

STAGE DELAY (ns)

RISE/FALL, 100% (ns)

TOTAL LOAD CAPACITANCE (pF) 0 5 10 15 20
TOTAL LOAD CAPACITANCE (pF) 0 5 10 15 20
TRISTATE

SOS STANDARD
CELL NO. 1670

10 DEVICES
PADS
7 MIL HEIGHT
CELL WIDTH - 8.0 MILS
VDD = 10 V

TOTAL LOAD CAPACITANCE \( tpF \)

DATA TAKEN 16M ZERO IMPEDANCE SOURCE AT
HELD HIGH. 10 W

20 n

LOGIC SYMBOL

\[ Q = D \cdot C \text{ for } C = 1 \]
\[ Q = \text{OPEN CKT. FOR } C = 0 \]

LOGIC EQUATION

TRUTH/TABLE

<table>
<thead>
<tr>
<th>C</th>
<th>D</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>OPEN</td>
</tr>
</tbody>
</table>

* DON'T CARE

NOTE:
ALL DATA TAKEN WITH ZERO IMPEDANCE SOURCE AT
D'.
C HELD HIGH.

CELL I/O CAPACITANCE VALUES

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (( pF ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.294</td>
</tr>
<tr>
<td>3</td>
<td>0.305</td>
</tr>
<tr>
<td>4</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STAGE DELAY (\mu s)</th>
<th>TOTAL LOAD CAPACITANCE (( pF ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>20</td>
<td>18</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RISE/FALL, 100% (\mu s)</th>
<th>TOTAL LOAD CAPACITANCE (( pF ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>20</td>
<td>18</td>
</tr>
</tbody>
</table>
TWO–INPUT AND 6 DEVICES

CELL NO. 1620

3 PADS

CELL WIDTH = 4 MILS

V_{DD} = 10 V

SCHEMATIC

LOGIC SYMBOL

TRUTH TABLE

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.010</td>
</tr>
<tr>
<td>3</td>
<td>0.243</td>
</tr>
<tr>
<td>4</td>
<td>0.243</td>
</tr>
</tbody>
</table>

A  B  X

0  0  0
0  1  0
1  0  0
1  1  1

STAGE DELAY (ns)

RISE/FALL, 10/90% (ns)

TOTAL LOAD CAPACITANCE (pF)
FOUR-INPUT AND

SOS STANDARD

CELL NO. 1640

10 DEVICES
5 PADS

CELL WIDTH = 6 MILS

$V_{DD} = 10 \text{ V}$

PIN CAPACITANCE (pF)

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.010</td>
</tr>
<tr>
<td>3</td>
<td>0.354</td>
</tr>
<tr>
<td>4</td>
<td>0.354</td>
</tr>
<tr>
<td>5</td>
<td>0.354</td>
</tr>
<tr>
<td>6</td>
<td>0.354</td>
</tr>
</tbody>
</table>

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

ALL OTHER COMBINATIONS 0

TOTAL LOAD CAPACITANCE (pF)

STAGE DELAY (ns)

RISE/FALL (10-90%) (ns)
TWO—INPUT OR

SOS STANDARD
CELL NO. 1720

6 DEVICES
3 PADS

CELL WIDTH = 4 MILS

V_{DD} = 10 V

---

SCHEMATIC

LOGIC SYMBOL

X = A + B

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

PIN | CAPACITANCE (pF)
---|----------------|
2   | 0.115          
3   | 0.115          
4   | 0.010          

---

PIN CAPACITANCE (pF)

TOTAL LOAD CAPACITANCE (pF)

STAGE DELAY (ns)

RISE/FALL, 10-90% (ns)

TOTAL LOAD CAPACITANCE (pF)

---
THREE-INPUT OR

SOS STANDARD
CELL NO. 1730

8 DEVICES
4 PADS
CELL WIDTH = 5 MILS

SCHEMATIC

LOGIC SYMBOL

X = A + B + C

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

PIN CAPACITANCE (pF)

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.225</td>
</tr>
<tr>
<td>3</td>
<td>0.225</td>
</tr>
<tr>
<td>4</td>
<td>0.225</td>
</tr>
<tr>
<td>5</td>
<td>0.010</td>
</tr>
</tbody>
</table>

STAGE DELAY (ns)

<table>
<thead>
<tr>
<th>TOTAL LOAD CAPACITANCE (pF)</th>
<th>STAGE DELAY (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>2.0</td>
<td></td>
</tr>
</tbody>
</table>

RISE/FALL, 10-90% (ns)

<table>
<thead>
<tr>
<th>TOTAL LOAD CAPACITANCE (pF)</th>
<th>RISE/FALL, 10-90% (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>2.0</td>
<td></td>
</tr>
</tbody>
</table>
FOUR-INPUT OR

SOS STANDARD
CELL NO. 1740

10 DEVICES
6 PADS
CELL WIDTH = 6 MILS
V_{DD} = 10 V

SCHEMATIC

LOGIC SYMBOL

X = A + B + C + D

TRUTH TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

ALL OTHER INPUT COMBINATIONS

1

PIN |
---|
| CAPACITANCE (pF) |
|---|---|---|---|---|
| 2 | 0.400 |
| 3 | 0.400 |
| 4 | 0.400 |
| 5 | 0.400 |
| 6 | 0.010 |

STAGE DELAY (ns)

TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns)

TOTAL LOAD CAPACITANCE (pF)
2,2 AND–2 NOR

SOS STANDARD
CELL NO. 1870

CELL WIDTH = 5.0 MILE
CELL HEIGHT = 7
VDD = 10

2
3
A
B
C
D
P
P
N
N
N
N
Z

LOGIC SYMBOL

LOGIC EQUATION

Z = AB + CD

TRUTH/TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>*</td>
<td>*</td>
<td>0</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

ALL OTHER INPUT COMBINATIONS 1

DON'T CARE

CELL I/O CAPACITANCE VALUES

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.45</td>
</tr>
<tr>
<td>3</td>
<td>0.45</td>
</tr>
<tr>
<td>4</td>
<td>0.45</td>
</tr>
<tr>
<td>5</td>
<td>0.45</td>
</tr>
<tr>
<td>6</td>
<td>0.03</td>
</tr>
</tbody>
</table>

CELL DELAY (ns)

OUTPUT NODE CAP (pF)

RISE/FALL (15-85%) (ns)

OUTPUT NODE CAP (pF)
2.2.2 AND-3 NOR
12 DEVICES
7 PADS
CELL HEIGHT 7.0 MILS
CELL WIDTH = 7.0 MILS

SOX STANDARD
CELL NO. 1890
VDD = 10

LOGIC SYMBOL

LOGIC EQUATION

Z = AB + CD + EF

TRUTH/TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>0</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>1</td>
<td>1</td>
<td>*</td>
<td>*</td>
<td>0</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>0</td>
</tr>
</tbody>
</table>

ALL OTHER INPUT COMBINATIONS

* DON'T CARE

CELL I/O CAPACITANCE VALUES

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.44</td>
</tr>
<tr>
<td>3</td>
<td>0.44</td>
</tr>
<tr>
<td>4</td>
<td>0.43</td>
</tr>
<tr>
<td>5</td>
<td>0.44</td>
</tr>
<tr>
<td>6</td>
<td>0.44</td>
</tr>
<tr>
<td>7</td>
<td>0.46</td>
</tr>
<tr>
<td>8</td>
<td>0.83</td>
</tr>
</tbody>
</table>

CELL DELAY (ns)

Rise/Fall (10-90%) (ns)

OUTPUT NODE CAP. (pF)
J/K FLIP FLOP WITH SET/RESET

SOS STANDARD
CELL NO. 2000

28 DEVICES
8 PADE

CELL WIDTH = 17 MILS
7 MIL FAMILY @ 10 V

SCHEMATIC

LOGIC SYMBOL

LOGIC EQUATION

\[ Q_n = C \cdot R \cdot Q_{n-1} + C \cdot J_{n-1} \cdot R_{n-1} \cdot R \\
+ S \cdot R \cdot J_{n-1} \cdot K_{n-1} \cdot Q_{n-1} \cdot R \\
\]

Note: \( J_{n-1}, K_{n-1}, \) and \( Q_{n-1} \) ARE THE VALUES OF J, K AND Q BEFORE THE CLOCK CHANGES STATE.

TRUTH/TABLE

<table>
<thead>
<tr>
<th>C</th>
<th>J</th>
<th>K</th>
<th>S</th>
<th>R</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>1</td>
<td>1</td>
<td>PROHIBITED</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES: \( Q_{n-1} \) IS THE STATE OF THE OUTPUT BEFORE THE LAST CLOCK TRANSITION

* DON'T CARE

CELL I/O CAPACITANCE VALUES

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2J</td>
<td>0.12</td>
</tr>
<tr>
<td>3Q</td>
<td>0.90</td>
</tr>
<tr>
<td>4K</td>
<td>0.12</td>
</tr>
<tr>
<td>6C</td>
<td>0.07</td>
</tr>
<tr>
<td>8S</td>
<td>0.16</td>
</tr>
<tr>
<td>7R</td>
<td>0.16</td>
</tr>
</tbody>
</table>

MIN CLK TO LOAD MASTER

MIN CLK TO LOAD SLAVE

MIN SET OR RESET TO LATCH

EXTERNAL LOAD ON Q < 2 pF

10 V OPERATION

STAGE DELAY

54 ns

0 pF

10 pF

20 pF

30 pF

0 ns

60 ns

15 ns

5 or R

1.5 ns

15 ns

20 ns
**D-TYPE, M/S, S/R FLIP FLOP**

**SOS STANDARD**
**CELL NO. 2020**

**SCHHEMATIC**

**LOGIC SYMBOL**

**CELL I/O CAPACITANCE VALUES**

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.20</td>
</tr>
<tr>
<td>3</td>
<td>0.20</td>
</tr>
<tr>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>0.10</td>
</tr>
<tr>
<td>6</td>
<td>0.20</td>
</tr>
<tr>
<td>7</td>
<td>0.20</td>
</tr>
</tbody>
</table>

**TRUTH/TABLE**

<table>
<thead>
<tr>
<th>C L</th>
<th>D</th>
<th>R</th>
<th>S</th>
<th>Q</th>
<th>G</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

* DON'T CARE
* UNDEFINED OUTPUTS

**DYNAMIC DATA @ 10.0 V**

**FLIP-FLOP CHARACTERISTICS**

**OUTPUT INVERTER CHARACTERISTICS**

* ASSUMING 1.0 pF LOAD AT Q

**MIN. CLK. TO LOAD MASTER**

**MIN. "S" OR "R" TO LATCH**

**MIN. CLK. TO LOAD SLAVE**

* WITH 1.0 pF AT Q A

**CELL WIDTH = 4 MILS**

**7 MIL FAMILY @ 10 V**
EXCLUSIVE OR

SOS STANDARD
CELL NO. 2310

V_{DD} = 10 V

8 DEVICES
3 PADS
CELL WIDTH = 6 MILS

SCHEMATIC

LOGIC SYMBOL

TRUTH TABLE

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.366</td>
</tr>
<tr>
<td>3</td>
<td>0.362</td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

PIN | A | B | X
---|---|---|---
2  | 0 | 0 | 0
3  | 0 | 1 | 1
4  | 1 | 0 | 1
1  | 1 | 1 | 0

-stage delay (\mu s)

RISE/FALL: 10-90% (\mu s)

TOTAL LOAD CAPACITANCE (pF)

TOTAL LOAD CAPACITANCE (pF)
SOS STANDARD
CELL NO. 2670

<table>
<thead>
<tr>
<th>PIN</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAPACITANCE (pF)</td>
<td>4.4</td>
<td>2.8</td>
</tr>
</tbody>
</table>

LOGIC SYMBOL

TRUTH TABLE

<table>
<thead>
<tr>
<th>D</th>
<th>0</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>HIGH</td>
<td>IMPED.</td>
</tr>
</tbody>
</table>

TOTAL LOAD CAPACITANCE (pF)

STAGE DELAY (ns)

TRANSITION TIME (ns)
SOS STANDARD
CELL NO. 2810

10 DEVICES
3 PADS
CELL WIDTH = 5 MILS

V_DD = 10 V

SCHEMATIC

LOGIC SYMBOL

TRUTH TABLE

PIN | CAPACITANCE (pF)
---|-----------------|
2  | 0.23
3  | 0.15
4  | 0.05

Q_n-1 IS OUTPUT BEFORE CLOCK GOES HIGH

MIN. CLOCK PULSE WIDTH TO TRANSMIT INPUT, D TO OUTPUT Q.

C -> 20 ns

C-Q DELAY (ns)

TOTAL LOAD CAPACITANCE (pF)
D--TYPE, MASTER/SLAVE FLIP FLOP

SO8 STANDARD
CELL NO. 2820

18 DEVICES
3 PADS

TOTAL LOAD CAPACITANCE

SCHEMATIC

LOGIC SYMBOL

NOTE: \( D_{n-1} \) AND \( Q_{n-1} \) ARE INPUT AND OUTPUT SIGNALS RESPECTIVELY BEFORE CLOCK CHANGES STATE

TRUTH TABLE

<table>
<thead>
<tr>
<th>( D )</th>
<th>( Q_n )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>( Q_{n-1} )</td>
</tr>
<tr>
<td>0</td>
<td>( Q_{n-1} )</td>
</tr>
</tbody>
</table>

\( Q_{n-1} \) IS OUTPUT BEFORE CLOCK GOES HIGH

PIN CAPACITANCE (pF)

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.266</td>
</tr>
<tr>
<td>3</td>
<td>0.229</td>
</tr>
<tr>
<td>4</td>
<td>0.040</td>
</tr>
</tbody>
</table>

10.0 V OPERATION

MIN. CLOCK PULSE WIDTH REQUIRED TO LOAD MASTER

MIN. CLOCK PULSE WIDTHS REQUIRED TO TRANSFER INFORMATION FROM MASTER TO OUTPUT
\( C_L = 0.4 \text{ pF}; T_C = 19 \text{ ns} \)
\( C_L = 3.0 \text{ pF}; T_C = 75 \text{ ns} \)

CONDITIONS:
ALL DELAY INFORMATION BASED ON AN ASSUMED 15 ns 10-90 RISE OR FALL TIME FOR CLOCK SIGNALS

50% CLK 50% OUTPUT Q
D FLIP FLOP WITH OPEN FB LOOP

SOS STANDARD
CELL NO. 2630

12 DEVICES
3 PADS

CELL HEIGHT = 7.0
CELL WIDTH = 6 MILS

V_DD = 10 V

SCHENATIC

LOGIC SYMBOL

LOGIC EQUATION

TRUTH TABLE

<table>
<thead>
<tr>
<th>C</th>
<th>D</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Q_{n-1}</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Q_{n-1}</td>
</tr>
</tbody>
</table>

Q_{n-1} IS OUTPUT BEFORE CLOCK GOES HIGH

CELL I/O CAPACITANCE VALUES

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.069</td>
</tr>
<tr>
<td>3</td>
<td>0.123</td>
</tr>
<tr>
<td>4</td>
<td>-</td>
</tr>
</tbody>
</table>

STAGE DELAY (ns)

TOTAL LOAD CAPACITANCE (pF)

ORIGINAL PAGE IS OF POOR QUALITY
11 DEVICES
4 PADS
CELL WIDTH = 6 Mils

SOS STANDARD
CELL NO. 2940

SCH EMATIC

LOGIC SYMBOL

TRUTH TABLE

C R D G
0 0 1 0
0 0 0 1
1 0 1 \( \bar{G}_{n-1} \)
1 1 0 1
0 1 1 NOT DETERMINED

\( \bar{G}_{n-1} \) IS OUTPUT BEFORE CLOCK GOES HIGH

MIN. CLOCK PULSE WIDTH TO TRANSMIT INPUT 'D' TO OUTPUT 'G'.

DELAY (ns) vs.
TOTAL LOAD CAPACITANCE (pF)
PLA INPUT DECODER

54 DEVICES
5 PADS
8 SIDE CONTACTS

CELL HEIGHT: 14 MILS
CELL WIDTH: 13 MILS

SOS STANDARD
CELL NO. 7000

VDD = 10

SCHEMATIC

LOGIC SYMBOL

LOGIC EQUATION

S = \bar{A}_1 \cdot \bar{A}_2 \cdot \bar{A}_3 \cdot E
T = A_1 \cdot A_2 \cdot A_3 \cdot E
U = A_1 \cdot A_2 \cdot A_3 \cdot E
V = A_1 \cdot A_2 \cdot A_3 \cdot E
W = A_1 \cdot A_2 \cdot A_3 \cdot E
X = A_1 \cdot A_2 \cdot A_3 \cdot E
Y = A_1 \cdot A_2 \cdot A_3 \cdot E
Z = A_1 \cdot A_2 \cdot A_3 \cdot E

NOTE: C NORMALLY HIGH. A 25 ns NEGATIVE PULSE ON C FOLLOWING THE SETTLING OF OTHER INPUTS SPEEDS OUTPUT.

TRUTH/TABLE

<table>
<thead>
<tr>
<th>E</th>
<th>A_1</th>
<th>A_2</th>
<th>A_3</th>
<th>S</th>
<th>T</th>
<th>U</th>
<th>V</th>
<th>W</th>
<th>X</th>
<th>Y</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

NOTES:
1. "* MEANS "DON'T CARE".
2. WHEN C IS LOW, ALL OUTPUTS ARE UNDEFINED. C IS ASSUMED HIGH FOR THE ENTIRE TRUTH TABLE.
3. THE CIRCUITRY IN THIS CELL IS NOT TRUE CMOS. ABOUT 1 mA STANDBY CURRENT IS DRAWN.

CELL I/O CAPACITANCE VALUES

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2,C</td>
<td>0.7</td>
</tr>
<tr>
<td>3,E</td>
<td>0.46</td>
</tr>
<tr>
<td>4,A_1</td>
<td>0.3</td>
</tr>
<tr>
<td>5,A_2</td>
<td>0.3</td>
</tr>
<tr>
<td>6,A_3</td>
<td>0.3</td>
</tr>
<tr>
<td>S, T, U, V, W, X, Y, Z</td>
<td>0.6 EACH</td>
</tr>
</tbody>
</table>

END OF INPUT TRANSIENT

DELAY OF S, T, U, V, W, X, Y, Z (FROM TRAILING EDGE OF C) VERSUS CAPACITIVE LOADS ON S—Z

<table>
<thead>
<tr>
<th>CAP. LOAD (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
</tr>
<tr>
<td>0.9 (7 STRING CELLS)</td>
</tr>
<tr>
<td>2.7 (22 CELLS)</td>
</tr>
</tbody>
</table>

NOTE: C NORMALLY HIGH. A 25 ns NEGATIVE PULSE ON C FOLLOWING THE SETTLING OF OTHER INPUTS SPEEDS OUTPUT.
PLA OUTPUT FUNCTION STRING

SOS STANDARD
CELL NO. 7XX0

V_{DD} = 10

TABLE

<table>
<thead>
<tr>
<th>S</th>
<th>T</th>
<th>U</th>
<th>V</th>
<th>W</th>
<th>X</th>
<th>Y</th>
<th>Z</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X_1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X_2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X_3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X_4</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X_5</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X_6</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>X_7</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X_8</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>FLOATING</td>
</tr>
</tbody>
</table>

NOTES:
1. X_1 \rightarrow X_8 VALUES ARE DETERMINED BY PROGRAMMING AT THE CONTACT MASK LEVEL.
2. COMBINATIONS NOT SHOWN IN TABLE ARE NOT ALLOWED BY THE INPUT DECODER CELL WHICH DRIVES S, T, U, V, W, X, Y, AND Z.
3. EXPANDABILITY ACHIEVED BY PHANTOM OR "ING" OUTPUTS.
INVERTING BUFFER INPUT PAD

SOS STANDARD
CELL NO. 9030 & 9040

DEVICES 2
PADS 2
CELL WIDTH = 8 MILE
7 MIL FAMILY @ 10 V

SCHEMATIC

LOGIC SYMBOL

TRUTH TABLE

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2.5</td>
</tr>
<tr>
<td>Z</td>
<td>0.1</td>
</tr>
</tbody>
</table>

PIN CAPACITANCE (pF)

<table>
<thead>
<tr>
<th>OUTPUT CAP. AT Z (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>20</td>
</tr>
<tr>
<td>30</td>
</tr>
</tbody>
</table>

CELL DELAY (ns)

<table>
<thead>
<tr>
<th>OUTPUT CAP. AT Z (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>20</td>
</tr>
<tr>
<td>30</td>
</tr>
</tbody>
</table>

CELL DELAY (ns)
OFF CHIP INVERTING BUFFER PAD
2 DEVICES

SOS STANDARD
CELL NO. 9060 & 9070
OUTPUT CELL WIDTH = 8 MILS

SCHEMATIC

+V

P-17 mils

N-11.5 mils

LOGIC SYMBOL

2

A

LOGIC EQUATION

X = \bar{A}

TRUTH/TABLE

<table>
<thead>
<tr>
<th>A</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

CELL I/O CAPACITANCE VALUES

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>2.5</td>
</tr>
<tr>
<td>X-COUT</td>
<td>0.03</td>
</tr>
</tbody>
</table>

CELL DELAY (ns)

OUTPUT NODE CAP. (pF)

OUTPUT EDGE 10-90% (ns)

OUTPUT NODE CAP. (pF)
SOS STANDARD
CELL NO. 9130/9140

4 DEVICES
1 PADS
CELL WIDTH = 8 mils

**SCHEMATIC**

```
VDD
/      /
P 1.7   P 16.5
/      /
N 1.0   N 10.5
/      /
VDD
```

**LOGIC SYMBOL**

```
A
```

**TRUTH TABLE**

<table>
<thead>
<tr>
<th>A</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**PIN CAPACITANCE (pF)**

<table>
<thead>
<tr>
<th>PIN</th>
<th>CAPACITANCE (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.06</td>
</tr>
</tbody>
</table>

**Graphs**

![Graph 1: Delay vs. Total Load Cap.](image1)
![Graph 2: Rise/Fall Time vs. Total Load Cap.](image2)