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DESIGN, DEVELOPMENT, FABRICATION AND DELIVERY OF REGISTER AND MULTIPLEXER UNITS

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RCA – ATL

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DESIGN, DEVELOPMENT, FABRICATION AND DELIVERY OF REGISTER AND MULTIPLEXER UNITS

By

A. Feller and T. Lombardi

RCA

SUMMARY

Objective

The primary objective of this program is to produce two complementary MOS monolithic chip types containing a register and multiplexer unit to be used in the central processing unit of a digital computer.

Scope of Work

The scope of this program involves the partition of the logic into a chip size consistent with the characteristics of the packages; photolithic, mask making, process and fabrication capabilities; number of pins; chip area; testing requirements and other factors affecting yield and producibility. Next the logic was implemented by specially configured circuitry designed to layout as well as to optimize the performance by taking full advantage of the unique properties of CMOS logic. Of the several approaches considered for generating the LSI CMOS arrays, the CMOS standard cell array design technique[1] was selected. The remainder of the program involved using these design automation techniques to generate the chip layout, artwork and working master plates, followed by the fabrication and testing of the two chip types. The delivering of 60 functional LSI arrays complete the program.

Conclusions

Several approaches for implementing the register and multiplexer unit into two CMOS monolithic chip types were evaluated. The CMOS standard cell array technique was selected and implemented.

Using this design automation technology, two LSI CMOS arrays were designed, fabricated, packaged and tested for proper static, functional and dynamic operation.

Results have been documented for 60 units, which were delivered to the Contracting Officer, MSFC, Huntsville, Alabama, along with the documented results.

One of the chip types, multiplexer register type 1, is fabricated on a 0.143 x 0.123 inch chip. It uses nine standard cell types for a total of 54 standard cells. This involves more than 350 transistors and has the functional equivalent of 111 gates. The second chip, multiplexer register type 2, is housed on a 0.12 x 0.12 inch die. It uses 13 standard cell types, for a total of 42 standard cells. It contains more than 300 transistors, the functional equivalent of 112 gates.

All of the hermetically sealed units were initially screened for proper functional operation. The static leakage and the dynamic leakage were measured. Dynamic measurements were made and recorded. At 10 V, 14-megabit shifting rates were measured on multiplexer register type 1. At 5 V these units shifted data at a 6.6-MHz rate. The units were designed to operate over the 3-to-15-V operating range and over a temperature range of -55° to 125°C.

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Section I

INTRODUCTION

This report describes the design, fabrication, testing and evaluation of two custom Large Scale Integrated (LSI) Complementary MOS (CMOS) integrated circuit arrays which perform the multiplexer register functions as required by the terms of the contract. In addition, the basic method and approaches used, as well as pertinent support technology, are described.

A. BASIC APPROACH

The final selection in determining the two-chip partitioning of the original logic resulted from an overall evaluation that considered the following parameters:

Chip size

Number of pins or external connections

Reliability

First level package

Yield

Automatic platter characteristics

Photoreduction tolerances

Mask and process constraints

Design automation characteristics.

None of these parameters by itself offered any serious constraints or was a limiting factor. The sum total evaluation of all these parameters in the time frame in which the basic design approach was formulated, combined with the primary constraint that reliable LSI arrays be produced that met the performance requirement, determined the final design criterion.

Various approaches for implementing the custom arrays were examined. These included these three approaches:

Manual layout and design and artwork digitizing

Computer interactive design and layout

Computer placement, routing and automatic artwork generation (LSI CMOS standard cell array approach).

B. SELECTED APPROACH

The LSI CMOS standard cell array approach was selected as the method to mechanize the CMOS LSI arrays.[1,2] This approach uses a series of computer programs to implement automatic placement and routing of a family of predesigned circuit functions called standard cells into the desired logic function. The computer programs then automatically generate a tape containing instructions to drive an automatic plotter, resulting in final precision artwork. The standard cell CMOS LSI array approach is described in more detail later in this report.

The standard cell circuit functions are characterized by circuits that vary in complexity from simple two-transistor inverters to complex 20-transistor subsystems.

C. OTHER COMPUTER AIDS AND SIMULATION TECHNIQUES

Circuit, logic, and system simulation techniques were extensively used not only to minimize design changes and to shorten the design cycle, but more importantly to thoroughly analyze, characterize, optimize, as well as to increase the reliability of the design.

1. Circuit and Device Simulation and Analysis

The circuit cells, as well as larger sections of the array logic, were analyzed and characterized by a special-purpose computer program capable of performing dc and transient analysis of P type, N type or complementary (P and N type) MOS integrated

circuit arrays.[3,4,5] The parameters of the device models used to characterize the MOS circuitry in the computer program are defined in terms of mask and process parameters as well as conventional circuit characteristics. This permits the program to accurately predict performance and operating characteristics of the final circuit array in terms of the fabrication process characteristics as well as the circuit parameters.

2. Logic Simulation (LOGSIM)

The logic configuration for each of the two chip types was verified by the LOGSIM (Logic Gate Simulator)[6] program. This computer program accepts as input the net list of the logic defined in terms of Boolean gates and automatically generates a series of output waveforms in response to a given set of input signals. The program can compare the computed output to a stored sequence and automatically print out the results. Because LOGSIM can accept finite risetimes and accommodate gates with variable delay, the program can be used to check for timing tolerance or race conditions. If the program encounters such a timing problem, it will print a spike, which is to be interpreted as a possible timing problem.

3. AGAT Program (Automatic Generation of Array Tests)

In testing the fabricated chips for correct functional operation, a test sequence was generated that not only verifies that the finished array performs the required logic function, but also checks every gate in the system for the stuck at "1" or stuck at "0" case. The automatic generation of test sequences for combinatorial logic was provided for by the Automatic Generation of Array Tests[7] (AGAT) program. These bit sequences or patterns were programmed into a programmable tester, which not only tested the chips for proper operation but also identified those outputs where the error occurred and the corresponding bit sequences which resulted in an error condition.

D. LSI CMOS MULTIPLEXER REGISTER CHIPS

All of the logic functions required to meet the specifications of this program are incorporated into two chip types - multiplexer register chip, types 1 and 2. In this report, chip type 1 is referred to by its functional name, PRR (product remainder register), or its RCA designation ATL 001A. Similarly, multiplexer register chip type 2 is referred to by its functional name, MQR (multiplier quotient register), or its RCA designation ATL 002A.

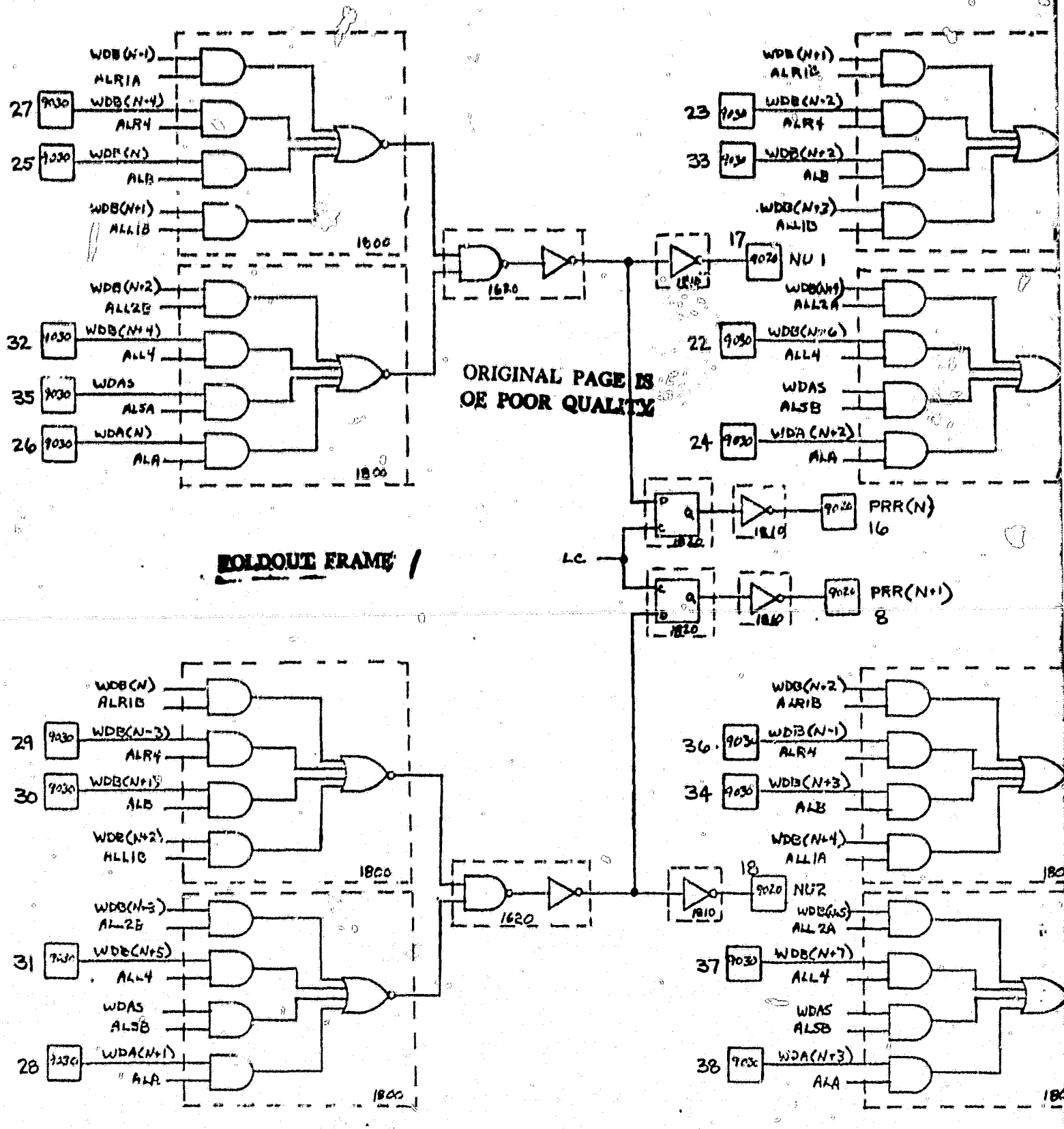
1. Multiplexer Register Chip, Type 1

The 001A register chip is a four-bit multiplexed register which not only provides temporary storage, but has the capability of shifting left or right. Depending on the direction, the shift can be one, two or four places. All the control logic required to make these decisions is contained on the chips. The logic content of the 001A chip is shown in the official logic diagrams, Figs. 1 and 2. For ease in testing the individual chips as well as debugging the systems the logic of the chip has been combined into a single logic diagram as shown in Fig. 10. A microphotograph of the fabricated 001A chip is shown in Fig. 3.

2. Multiplexer Register Chip, Type 2

The 002A or MQR chip contains two four-bit registers, one of which incorporates many of the functions found on the 001A chip. As on the 001A the shifting operation is effected by master-slave registers. In addition to all the necessary control logic to control the mode of the input multiplexers, the 002A chip also contains another four-bit storage register using D-type flip-flops.

The 002A (MQR) chip contains 300 functional transistors (in addition to the input protective devices and other process components) representing the equivalent of 112 gates. The chip measures 0.120 x 0.120 inch. The 001A (PRR chip contains 350



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PIN 21 = GROUND
PACKAGE PIN NUMBERS ARE ADJACENT TO SQUARES.

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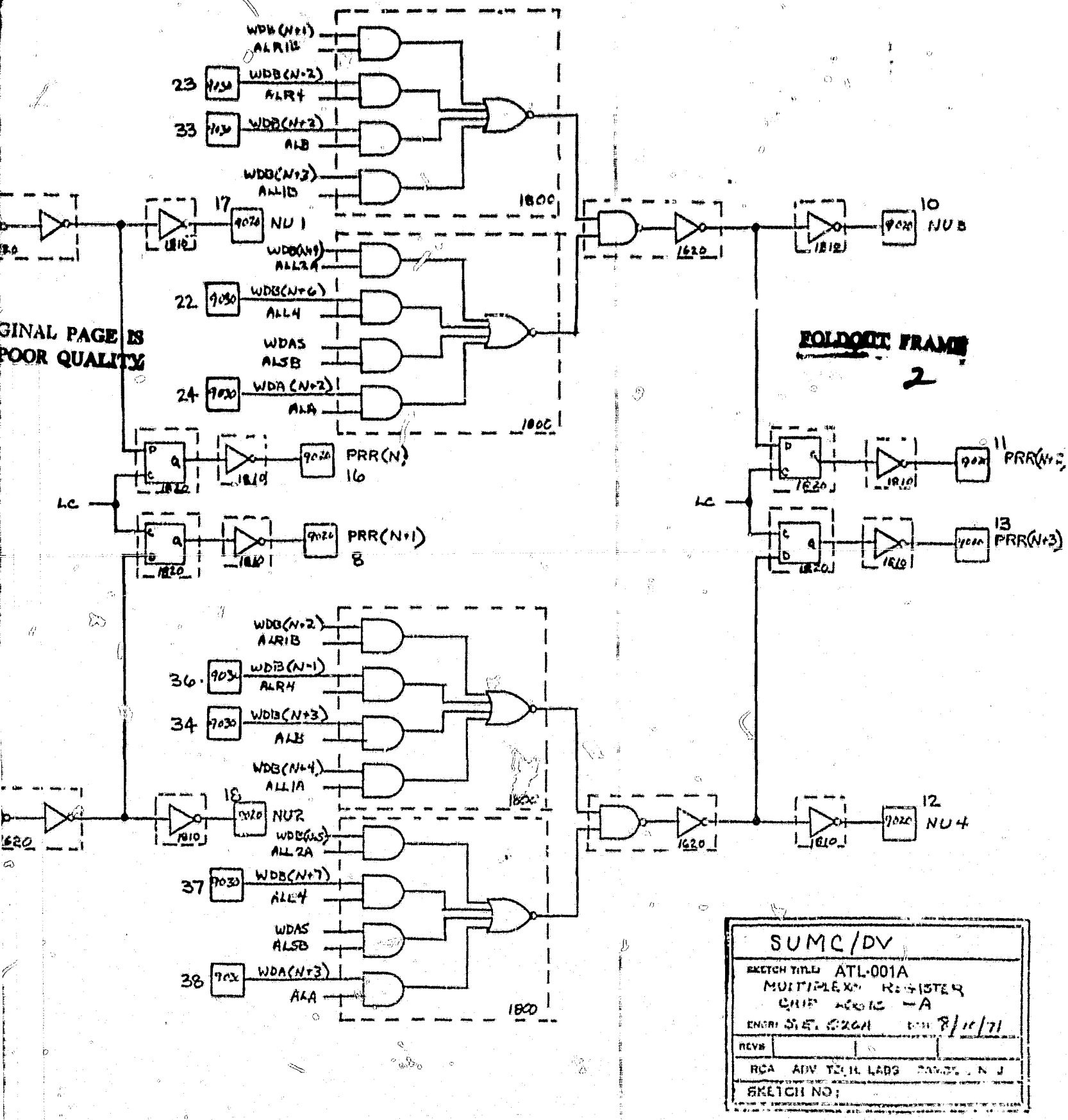

Fig. 1. Logic diagram of 001A, part 1.

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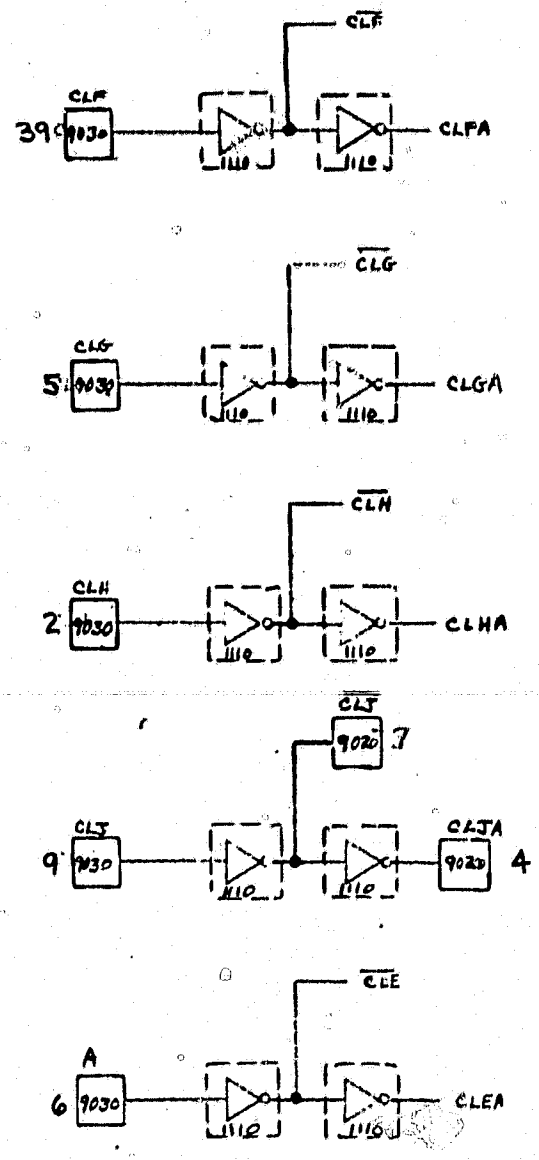

MROM
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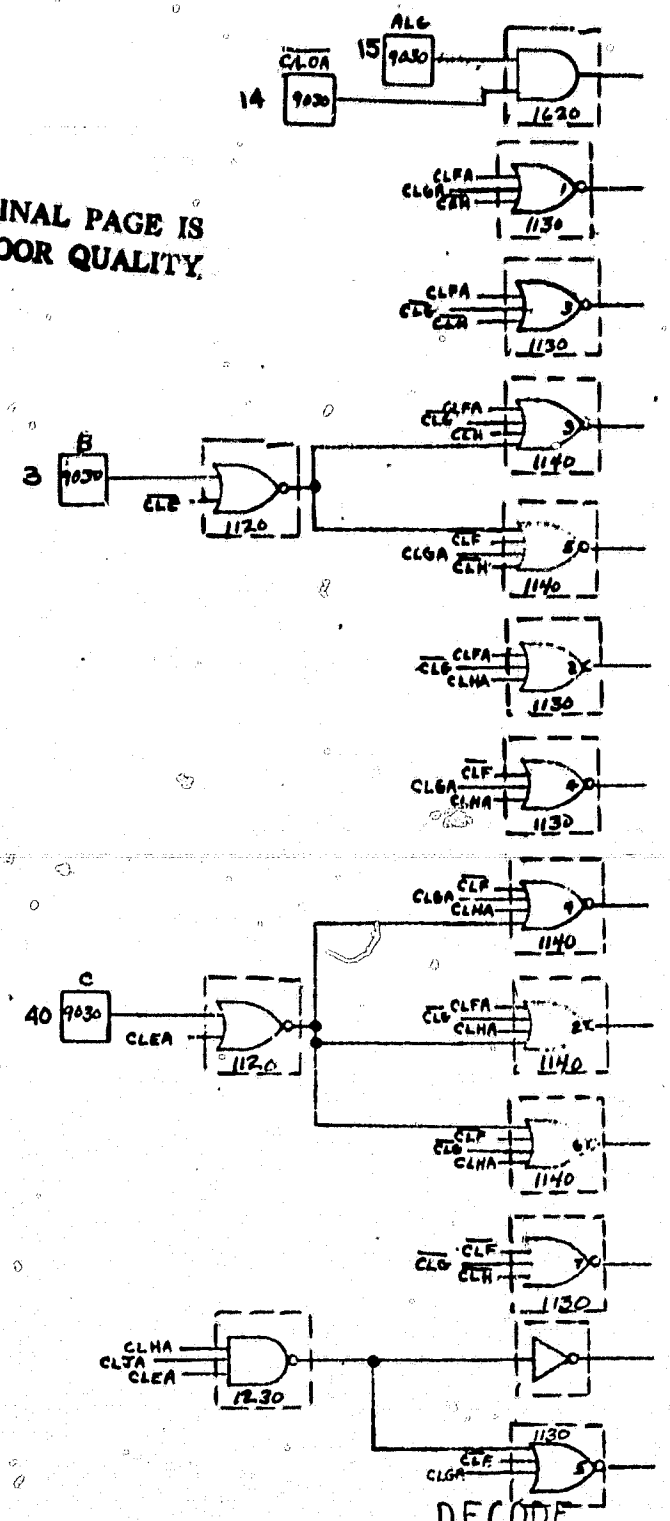

DECODE
LOGIC

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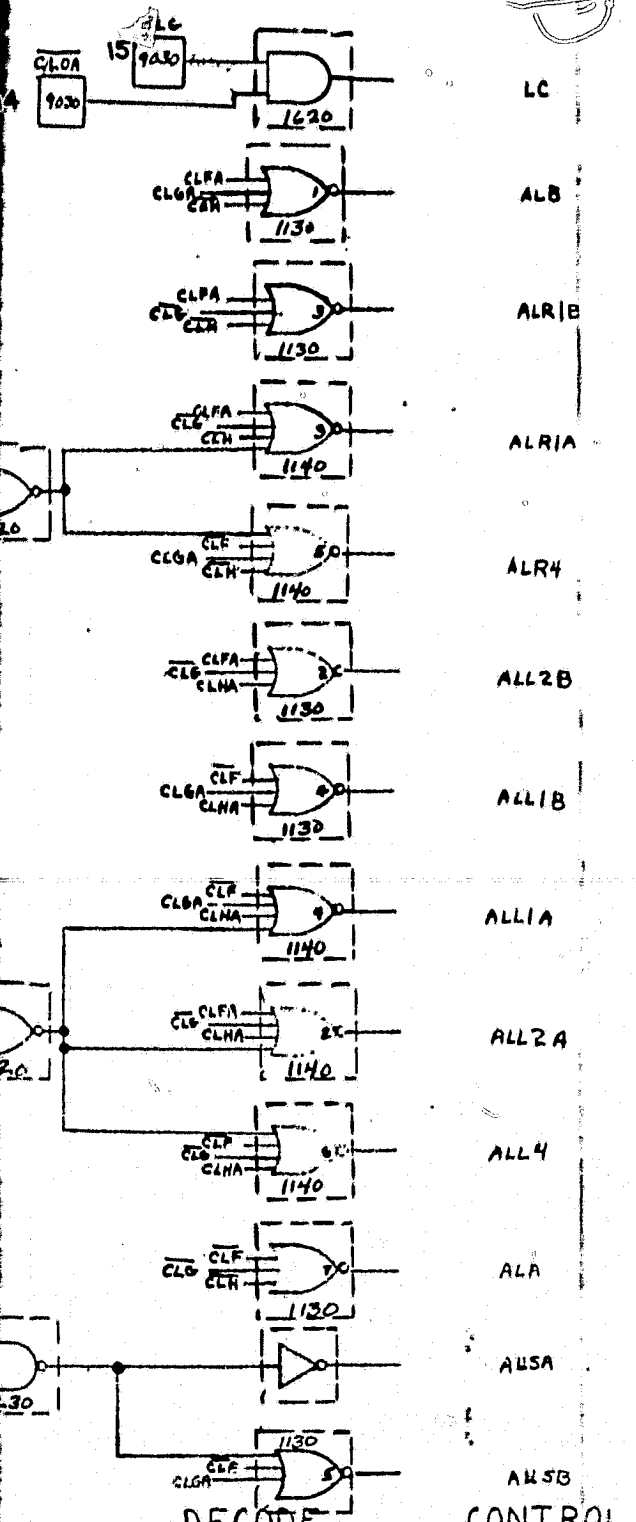
SIGNA

11 PINS

PIN 1 = SUPPLY VOLTAGE
PIN 21 = GROUND
PACKAGE PIN NUMBERS ARE ADJACENT TO SQUARES.



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MULTIPLEXOR REGISTER
D CODE SECTOR -B
S.E. Ozga 1/25/71
8/10/71
SHEET NO.:

Fig. 2. Logic diagram of 001A, part 2.

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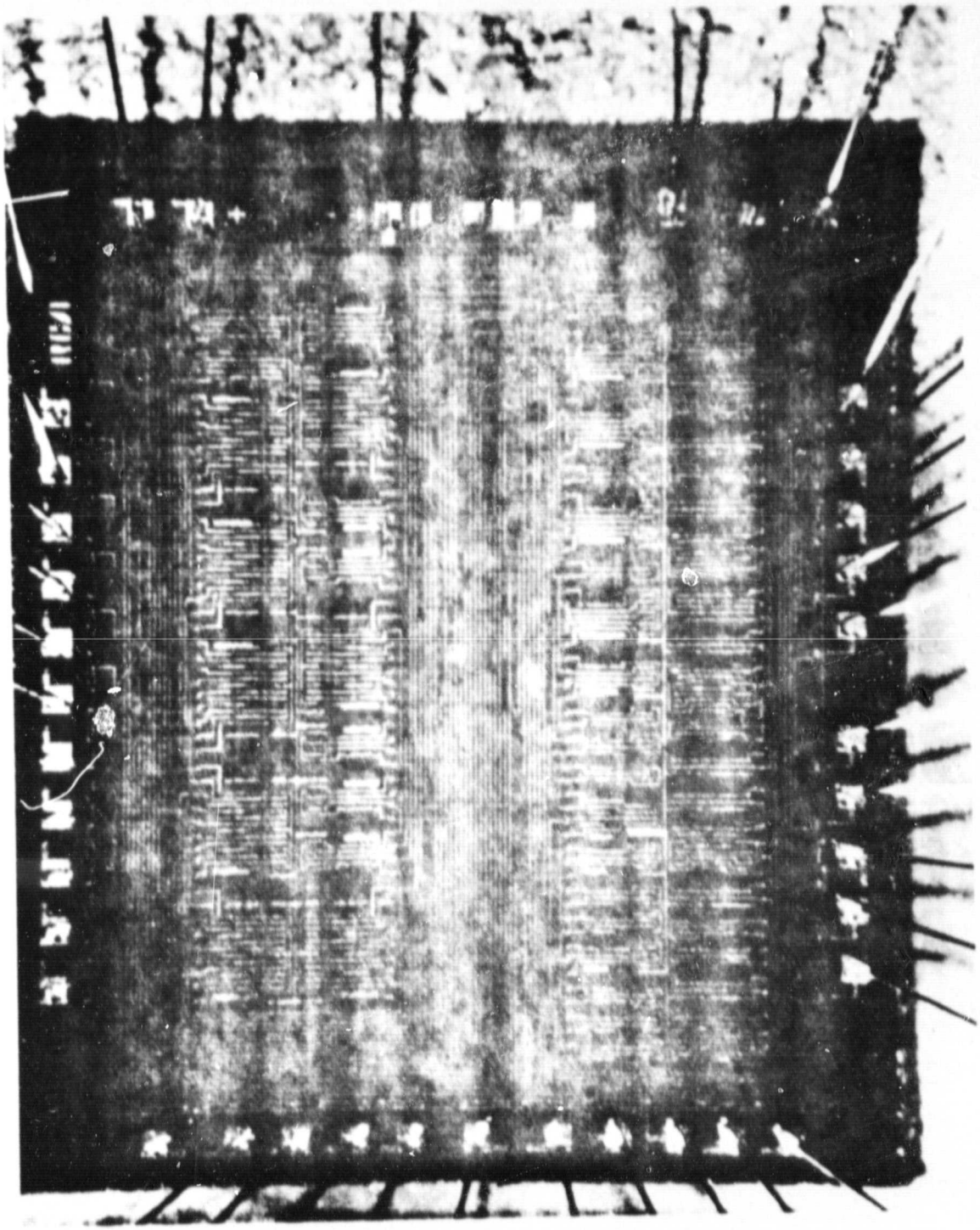

Fig. 3. Microphotograph of 001A.

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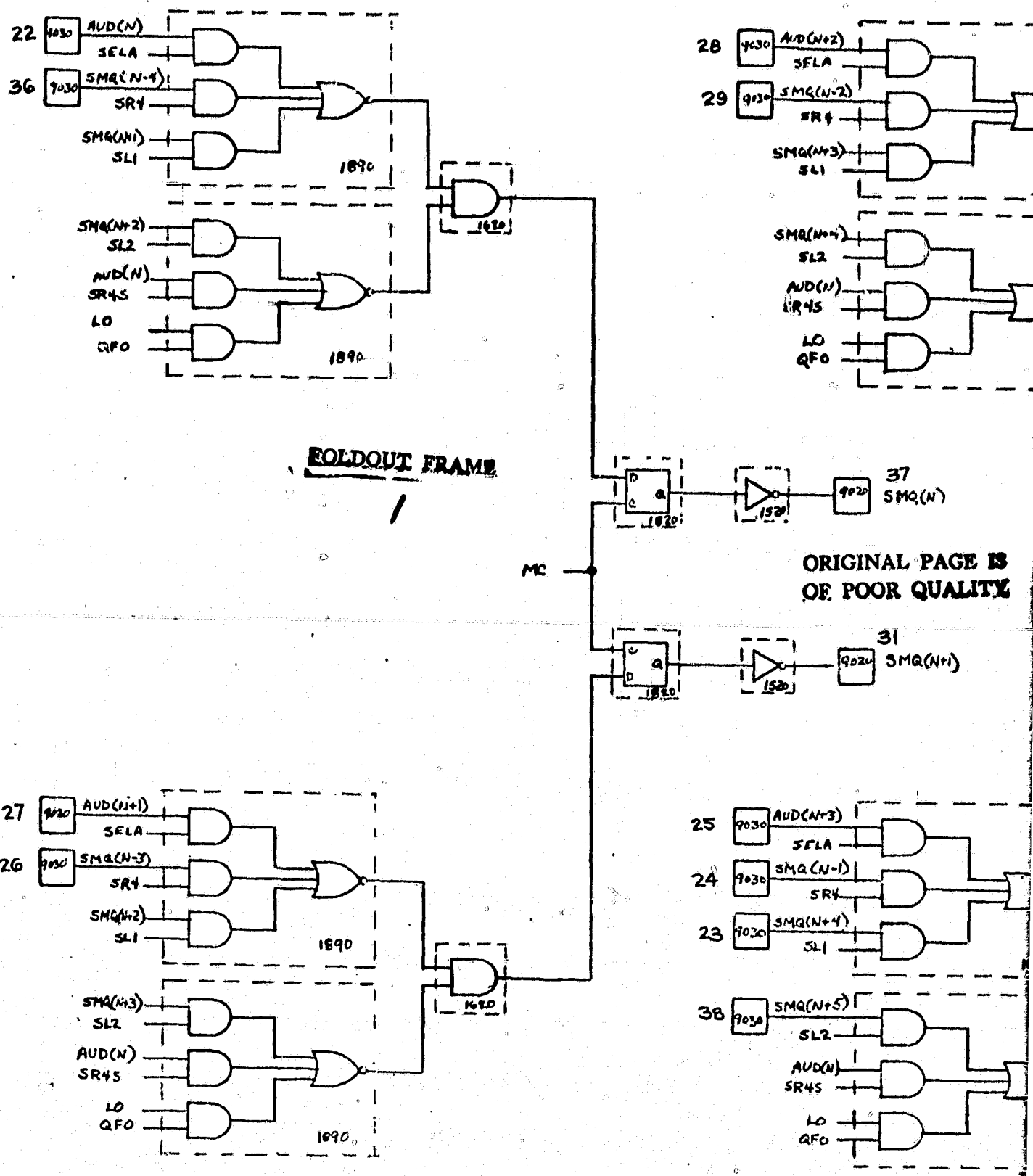
transistors, the equivalent of 111 Boolean gates. The chip measures 0.143 x 0.123 inch and uses 54 standard cells made up of nine different types.

The logic content of the 002A chip is shown in the official logic diagrams, Figs. 4 and 5. As in the case of the 001A, the logic has been incorporated into a single logic diagram, shown in Fig. 14. A microphotograph of the fabricated 002A chip is shown in Fig. 6.

E. PERFORMANCE OF MULTIPLEXER REGISTER CHIP TYPES

In addition to a complete description of the detailed contents of the chips, of the approach selected for the design, and the details involved in mechanizing the design, this report includes a complete summary of the static and dynamic performances measured on 60 chips (forty 001A's and twenty 002A's). These 60 chips constituted some of the deliverable items on the contract and as such were delivered to NASA-MSFC on 22 September 1971.



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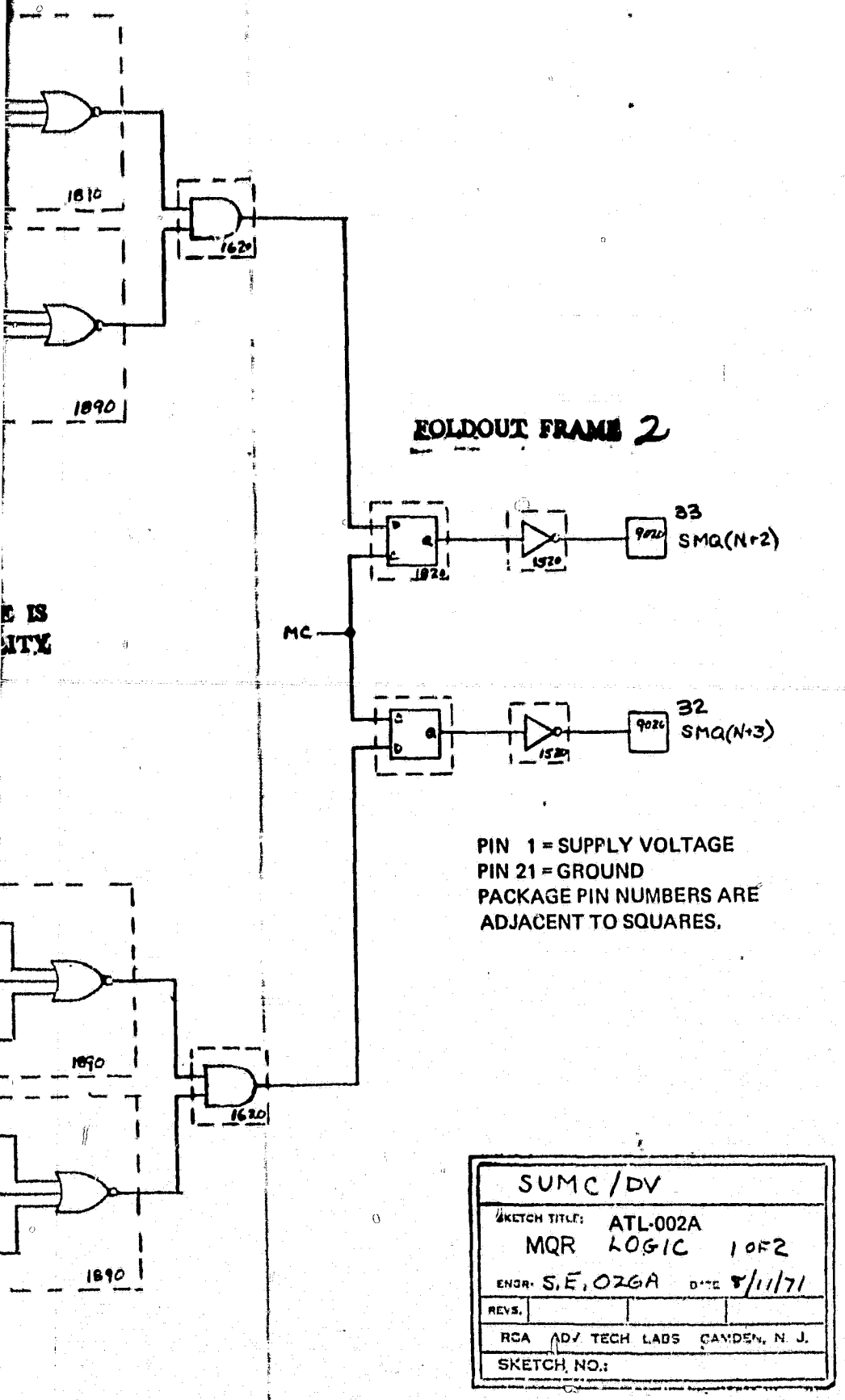

Fig. 4. Logic diagram of 002A, part 1

MQ REGISTER CONTROL DECODE

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23 PINS USED OUT OF 23

PIN 1 = SUPPLY VOLTAGE
PIN 21 = GROUND
PACKAGE PIN NUMBERS ARE ADJACENT TO SQUARES.

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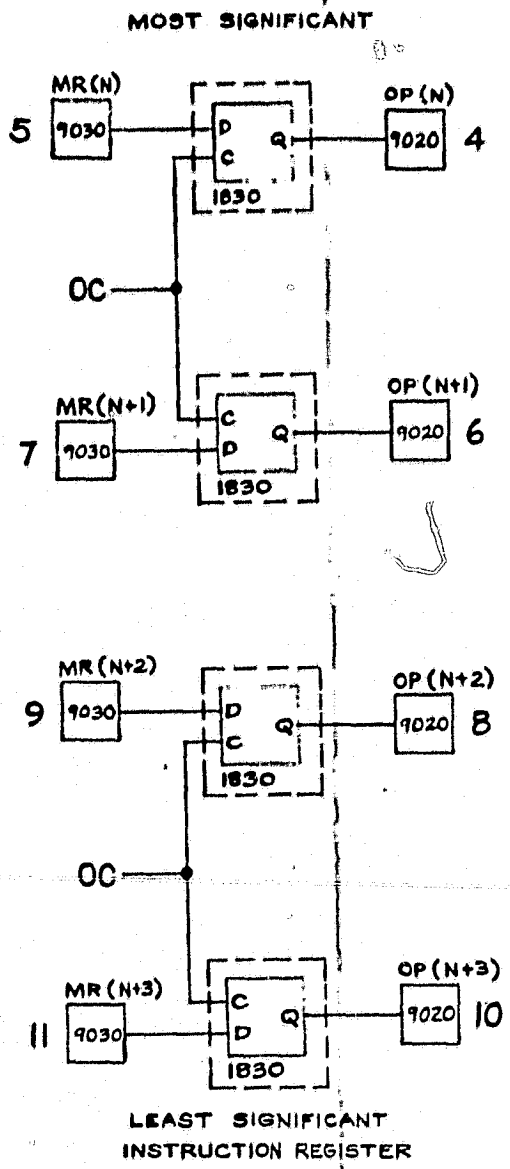

$\overline{CLK}$
CLKA
CLL
CLLA
$\overline{CLM}$
CLMA
$\overline{CLN}$
CLNA

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SKETCH TITLE: ATL 002 A MQR DECODE LOGIC 2 OF 2		
ENGR: A.S.M	DATE: 2/19/71	
REVS. 5/24/71	8/11/71	
RCA ADV. TECH. LABS CAMDEN, N. J.		
SKETCH NO.:		

Fig. 5. Logic diagram of 002A, part 2.

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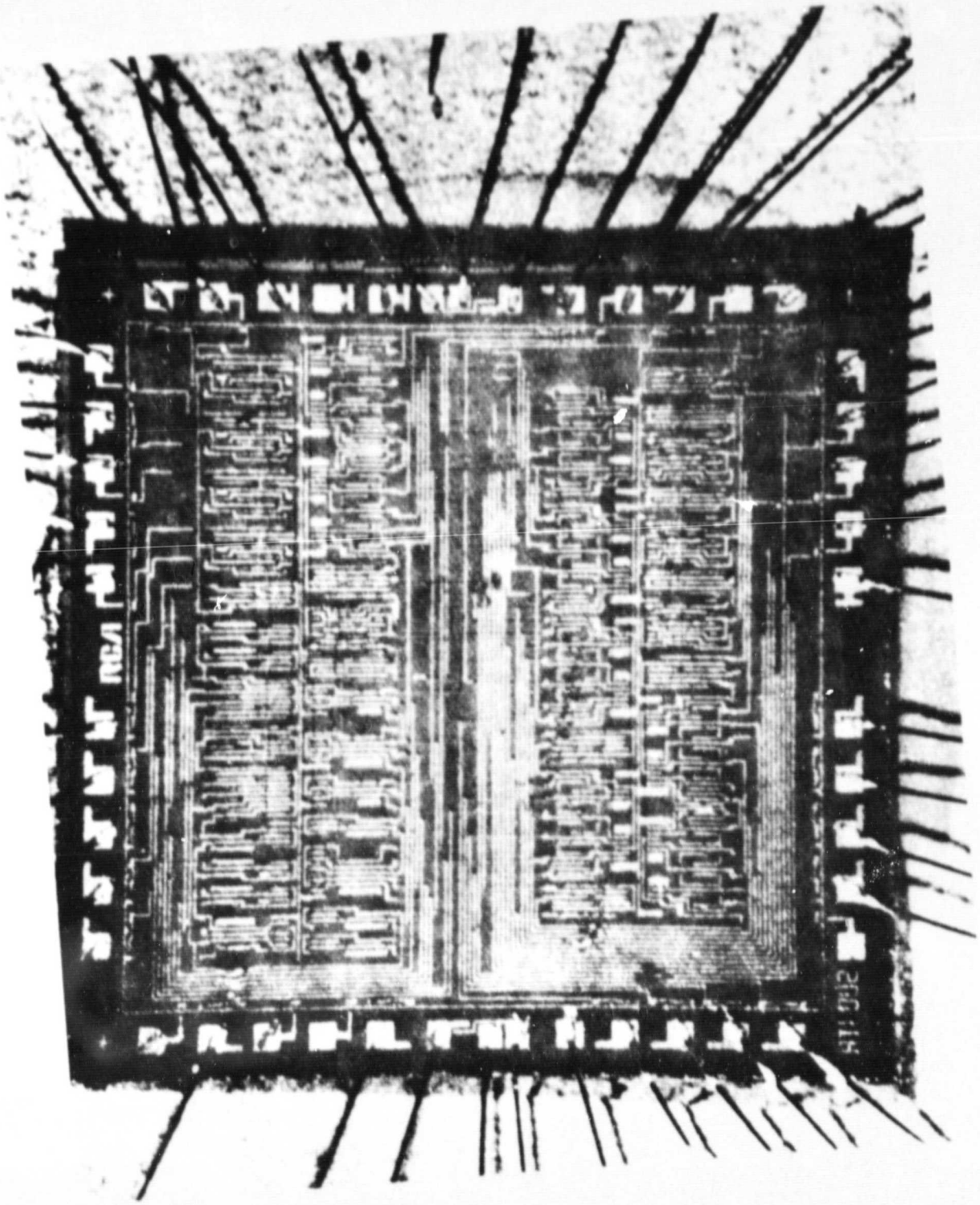

Fig. 6. Microphotograph of 002A.

Section II

SELECTED APPROACH: CMOS LSI STANDARD CELL ARRAYS

This section describes the CMOS LSI standard cell technique used to design and generate the multiplexer register chips. The approach is essentially an automatic technique for generating precision mask artwork for LSI arrays using design automation techniques. The method is based on a family of custom-designed circuits called standard cells which are stored on a library tape and which can, under computer program control, be recalled from memory in order to mechanize a specific function or logical configuration. The method essentially consists of three components:

1) a series of design automation computer programs
2) a family of custom CMOS circuits called standard cells
3) a basic standard cell array topology.

A. DESIGN AUTOMATION COMPUTER PROGRAMS

The CMOS LSI standard cell design automation programs are a family of computer programs that accept as input data the logic diagram defined in terms of the standard cells and generates an output tape containing the instructions for an automatic plotter to generate precision mask artwork for the LSI arrays. These programs contain the following basic subroutines.

1. Placement Program

This program performs an automatic placement based on an algorithm which seeks to minimize total interconnection length and number of crossovers. The program will continue to evolve new placements based on the best of the previous placements for a period specified by a program parameter. The output of the placement program automatically becomes the input data for the routing program.

2. Routing Program

The routing program is designed to interconnect the selected standard cells in accordance with the original net list. The heuristic algorithm seeks to minimize total wire length and crossovers. In addition, the program endeavors to give preference to a metal interconnect as opposed to a P+ tunnel or diffusion interconnection. The type of connection made is determined automatically by the routing program. If the program implements a connection, or a portion of an interconnection, with a P+ diffused tunnel, the program will then automatically place an N+ guard band around the tunnel to minimize the effect of any parasitic device that could be formed with an adjacent tunnel.

A unique feature of this algorithm is that successful interconnection of all the required signals is guaranteed. The program will attempt to minimize chip area with the constraint that the chip has been interconnected faithfully in accordance with the input net list. When the routing program has completed the interconnectivity list, it will automatically generate an output data format that is accepted by the artwork program unless optional manual intervention occurs. In order to facilitate uniform bonding pad placement on the perimeter of the chip, as well as to improve the performance of the array, the optional manual intervention mode will be exercized. To aid in effecting the manual changes desired, a manual modification program is used. With the use of this program all the required manual changes are effected. To ensure that these changes have been implemented correctly, a composite plot is made on a local plotter whose output is of sufficient accuracy to provide the required checking. After the modified wiring has been checked and verified, a data format containing the required placement and routing information is generated that is accepted by the artwork program.

3. Artwork Program

The artwork program takes the modified output of the placement and routing program, combines it with the circuit and cell data relating to those stored cells which are used in the particular logic, and generates a magnetic tape that contains all the

necessary instruction and information that results in the generation of the seven-level mask artwork (usually at 80X) using a Gerber automatic plotter.

B. STANDARD CELL CIRCUIT FAMILY

The standard-cell circuit library is a set of logic circuits that have been defined, configured, designed, topologically laid out, checked, analyzed, simulated, validated and then stored permanently. The cells range in complexity from a two-device inverter to complex super cells having more than 20 devices. The present standard cell family consists of more than 40 cells.

The standard cell designation is used because all cells in the family must be multiples of a standard height. All input and output connections to each cell are made via the input/output cell pads located at the bottom of each cell.

Table 1 contains a list of the cell types and functions that are used in the multiplexer register chip type 1. Nine standard cell types are used to implement the logic of the 001A chip type.

Table 2 contains the standard cell circuit complement for multiplexer register chip type 2, the 002A array. This array type uses 11 standard cell array types, two of which are flip-flops. Cell 1820 is a D-type master-slave flip-flop operating with a positive pulse. Cell 1830 is a D-type storage flip-flop.

C. STANDARD CELL ARRAY TOPOLOGY

An integral part of the standard-cell approach centers on the design and layout of the standard cell array topology. The topological layout was designed to be compatible with the available process and design rules, while allowing the design automation computer program to lay out an optimized topology. The microphotographs in Figs. 3 and 6 are examples of the basic layout. The row of back-to-back cells with a common ground between them is characteristic of the standard cell topology. If more rows are

TABLE 1. 001A STANDARD CELL CIRCUIT COMPLEMENT

CELL NUMBER	CELL NAME/FUNCTION
1110	Inverter
1120	Two-input NOR
1130	Three-input NOR
1140	Four-input NOR
1230	Two-input NAND
1620	Two-input AND
1800	2-2-2-2 AND - 4 NOR
1810	Inverting buffer No. 1
1820	D-type master-slave flip-flop

TABLE 2. 002A STANDARD CELL CIRCUIT COMPLEMENT

CELL NUMBER	CELL NAME/FUNCTION
1120	Two-input NOR
1130	Three-input NOR
1140	Four-input NOR
1310	Inverting buffer No. 2
1520	Double buffer
1620	Two-input AND
1630	Three-input AND
1640	Four-input AND
1820	D-type master-slave flip-flop
1830	D-type storage flip-flop
1890	2, 2, 2, - 3 NOR

required, the program will supply them, following the format illustrated in the two microphotographs. P-type and N-type test transistors, with pads large enough to facilitate probing, are automatically incorporated into every chip. Also characteristic of all the standard cell arrays is a ground bus which runs on the outside perimeter of the chip. The availability of this ground bus provides a ground return for the diodes used in the protective devices on all inputs.

Section III

STATIC AND DYNAMIC PERFORMANCE OF MULTIPLEXER CHIPS

A. MULTIPLEXER REGISTER CHIP TYPE 1

The multiplexer register chip type 1 - PRR (ATL 001A)* is a four-bit multiplexed register utilizing both clocked and direct outputs. Multiplexing of the inputs provides the capability of shifting left or right as well as passing unshifted data. Shift modes available are a one- or four-bit right shift or a one-, two- or four-bit left shift. Control logic on the 001A controls the mode of the input multiplexers.

The 001A is fabricated on a 123 mil by 143 mil die. Implementation of the desired logic functions is achieved by using 54 standard cells (nine standard cell types), which contain 350 transistors and the equivalent of 111 gates.

The following section describes the static and dynamic tests run on the PRR chips. These tests include functional testing, leakage, life tests and propagation delay. All tests were conducted with a 10-V supply voltage and 10-V input pulses. In addition, propagation delay measurements were made with a 5-V supply voltage and 5-V input pulses.

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*The multiplexer register chip type 1 is referenced in this report either by the abbreviation PRR or by the number 001A. The PRR abbreviation refers to the essential function of this chip, the product remainder register. The 001A is an internal number assigned to the chip by the Advanced Technology Laboratories of RCA. The number is a convenient and necessary one if any additional information on this chip type is required.

1. Logical Functionality

A complete set of computer generated test sequences was applied to the inputs of all 001A chips to check the functionality of all of the internal logic.

2. Leakage

a. Static Leakage

Static leakage current was measured in the ground line of all the 001A chips. The measurements were made with all the inputs tied to ground and then with all inputs tied to the supply voltage (+10 V). Median leakage for the 001A chips was 1 μA, and the median static power dissipation was 10 μW per chip. The static leakage test setup is shown in Fig. 7, and the test results for the PRR array are presented in Table 3. The chips listed in this table are a portion of the CMOS standard cell arrays delivered to NASA-MSFC.

b. Dynamic Leakage

Dynamic leakage current was measured in the ground line of four 001A chips for clock frequencies up to 1 MHz. All four of the 001A's master-slave flip-flops were simultaneously clocked during this test. From the dynamic leakage data taken, a graph of the average power dissipation per chip vs. clock frequency was generated (see Fig. 8).

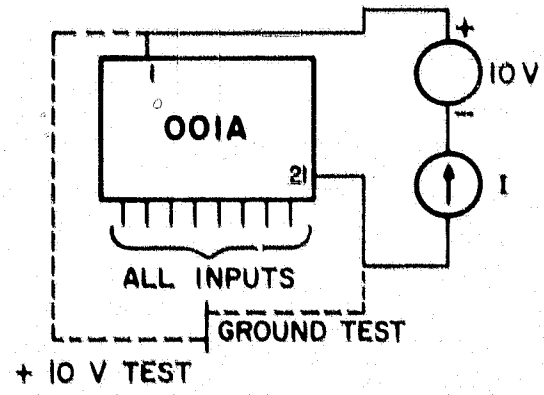


Fig. 7. Static leakage test setup.

TABLE 3. 001A STATIC LEAKAGE CURRENTS

BATCH NUMBER	CHIP NUMBER	LEAKAGE CURRENT (μA)	
		INPUTS AT GROUND	INPUTS AT 10V
7123F	9	4000	5700
7123F	12	2100	1650
7123F	17		< 1
7128C	1	420	0.8
7128C	2	2.3	110
7128C	3	0.4	1.0
7128C	4	0.7	0.6
7128C	6	3.0	46
7128C	7	0.4	0.4
7128C	8	1600	83
7128D	2	0.3	0.3
7128D	4	0.4	0.4
7128D	5	0.3	1.7
7135E	3	6000	< 1
7135E	4	< 1	< 1
7135E	5	180	< 1
7135E	8	< 1	6.5
7135E	10	< 1	< 1
7135F	1	0.4	0.4
7135F	2	0.4	0.4
7135F	5	< 1	< 1
7135F	7	< 1	< 1
7135F	8	< 1	< 1
7135F	10	< 1	< 1
7135F	12	< 1	< 1

TABLE 3. 001A STATIC LEAKAGE CURRENTS
(Continued)

BATCH NUMBER	CHIP NUMBER	LEAKAGE CURRENT (μA)	
		INPUTS AT GROUND	INPUTS AT 10V
7135F	14	< 1	< 1
7135F	15	< 1	< 1
7135F	16	< 1	< 1
7135F	19	< 1	< 1
7135F	20	< 1	< 1
7135F	22	< 1	< 1
7135F	23	< 1	< 1
7135F	26	< 1	< 1
7135F	28	< 1	< 1
7135F	29	< 1	< 1
7135F	30	85	< 1
7135F	31	< 1	80
7135F	32	< 1	< 1
7135F	33	< 1	< 1
7135F	35	< 1	< 1

On a CMOS chip, the average dynamic power dissipation is directly related to the energy required to charge and discharge the circuit capacitance to its extreme voltage. Most simply, each capacitance is charged and discharged to the supply voltage. In the general case, however, dynamic power dissipation is proportional to the effective system capacitance, the pulse repetition frequency and the square of the effective voltage swing. On a single-chip basis, power dissipation is given by:

$$P_{chip} = P_{quiescent} + C_{eff} f_{clock} V^2_{eff} \qquad (1)$$

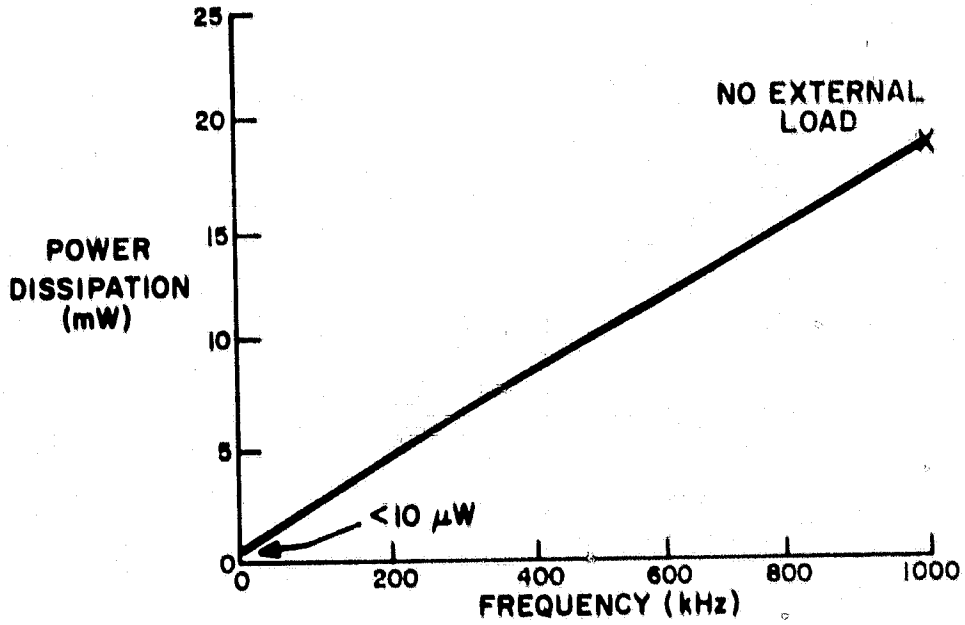


Fig. 8. PRR (001A) average power dissipation vs. clock frequency.

From Fig. 8 it can be seen that the CV^2f losses associated with chip operation at even moderately slow clock frequencies are still several orders of magnitude greater than the quiescent chip power dissipation.

3. Life Tests

a. Elevated Temperature Leakage

A static leakage life test at elevated temperatures is presently being conducted on two PRR chips. The test was started on 8 July 1971 and includes data for temperatures from 25°C to 100°C. Present plans call for the test to continue to 125°C before a temperature cycling routine is initiated. Provisions to check the dynamic performance of the 001A's under test have been included in the test sequence. To date, no dynamic failures have occurred. Condensed data on the static leakage life test is presented in Table 4.

TABLE 4. 001A STATIC LEAKAGE LIFE TEST AT ELEVATED TEMPERATURES

DATE	TEMPERATURE (°C)	LEAKAGE TEST CHIP 1 (μA)	LEAKAGE TEST CHIP 2 (μA)
7/8/71	25	25	0.014
7/9/71	60	33	0.055
7/13/71	60	41	0.16
7/19/71	60	41	0.15
7/30/71	60	41.5	0.16
8/6/71	60	42	0.19
8/12/71	60	42	0.20
8/18/71	60	42	0.18
8/30/71	60	42	0.20
9/10/71	85	43.5	0.40
9/13/71	85	43.5	0.21
9/21/71	85	43.5	0.22
9/28/71	85	44.5	0.21
10/5/71	85	44	0.21
10/12/71	85	43.5	0.21
10/18/71	85	43.5	0.19
10/25/71	100	46	0.23

b. Dynamic Performance at Ambient Temperature

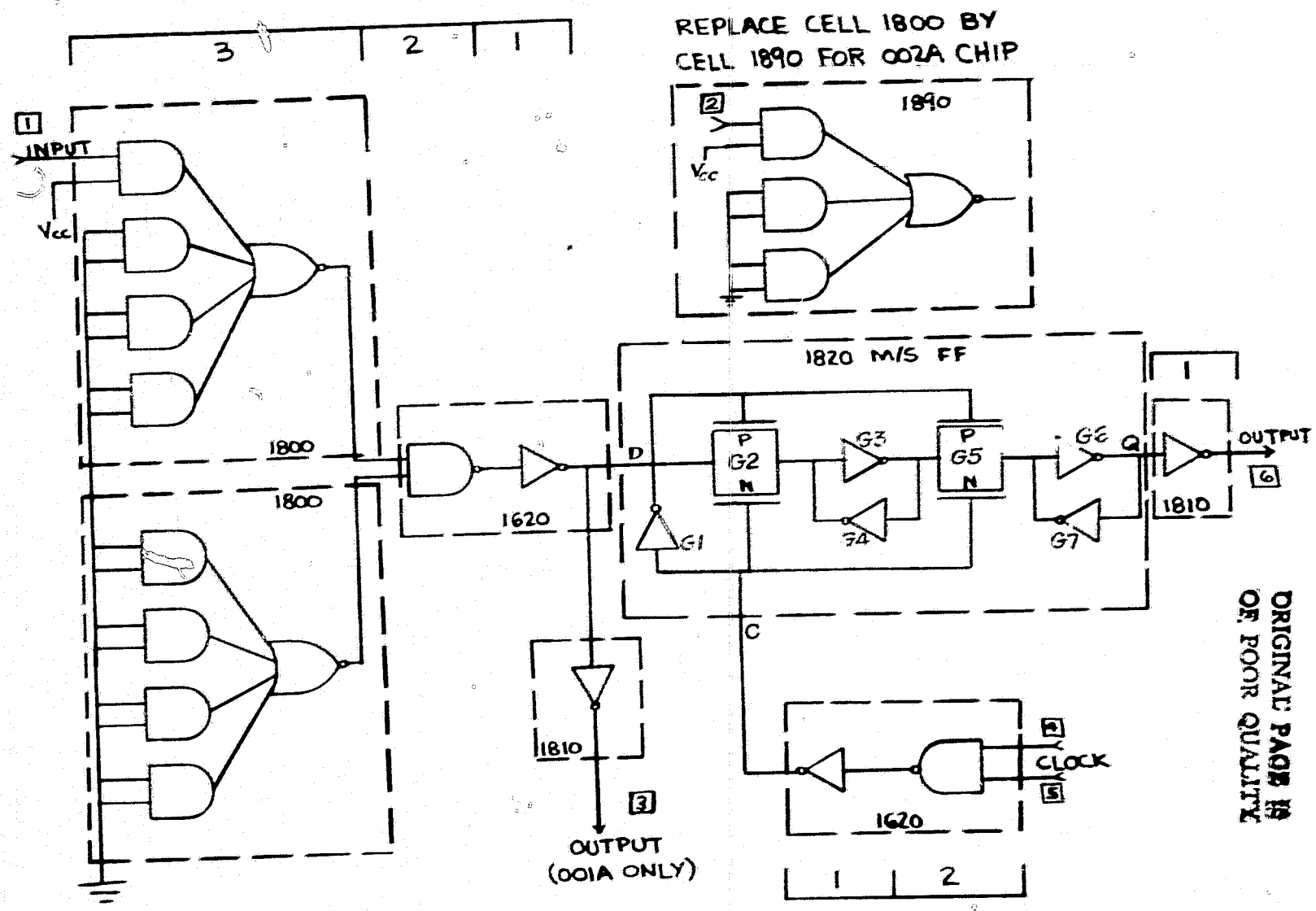
Two CMOS LSI standard cell chips, the ATL-NASA test chip and the ATL-000, have been under continuous dynamic stress at 25°C since 28 May 1971. No degradation in dynamic performance has occurred.

4. Propagation Delay

a. Propagation Delay of Master-Slave Cell 1820

The No. 1820 master-slave flip-flop cell is used on both the 001A and 002A chips. This flip-flop, shown in detail in Fig. 9, is a single-input D-type master-slave register in which not only can the data, D, be jam-transferred into the master register (the combination of G3 and G4), but the input can be multiplexed from a common bus because of G2, which is used to isolate the D input line from the master register. The jam-transfer capability with a single input arises out of the special high impedance (low capacitance) characteristics of the CMOS technology combined with the special design of the G2 and G4 gates. The G4 gate is designed with very low conductance devices that keep the output impedance of G4 high enough so that it can be driven directly from the data, D, through G2, but low enough that it can hold the stored data in the master register, which consists of G3 and G4. Gate G5 is a bidirectional switch that is used to isolate the slave register, G6 and G7, when new data is being stored in the master. Figure 10 shows the complete logic contained on the PRR (ATL 001A) chip. A data input pulse to the 001A (or 002A) passes through three stage delays before reaching the master-slave flip-flop. The clock pulse passes through two stage delays, and the output from the master-slave flip-flop passes through one stage delay before reaching the output of the chip. The internal stage delays on the chip guarantee that the propagation delay associated with the master-slave flip-flop will be no worse than the delay measurements made at the inputs and outputs of the chip. This condition is illustrated in Fig. 11.

The solid lines represent waveforms at the inputs and output of the chip, while the dashed lines represent waveforms at the inputs and output of the master-slave flip-flop. As can be seen, chip time delay measurements are always greater than or equal to the master-slave time delays. Three timing measurements were made on the 001A master-slave flip-flops. The first measurement is designated the "ripple through" time, which is the minimum time necessary to place a bit of information at the flip-flop



BOXED NUMBERS, □, ARE REFERENCE NODES AND NOT PIN NUMBERS

Fig. 9. 001A master-slave flip-flop circuit.

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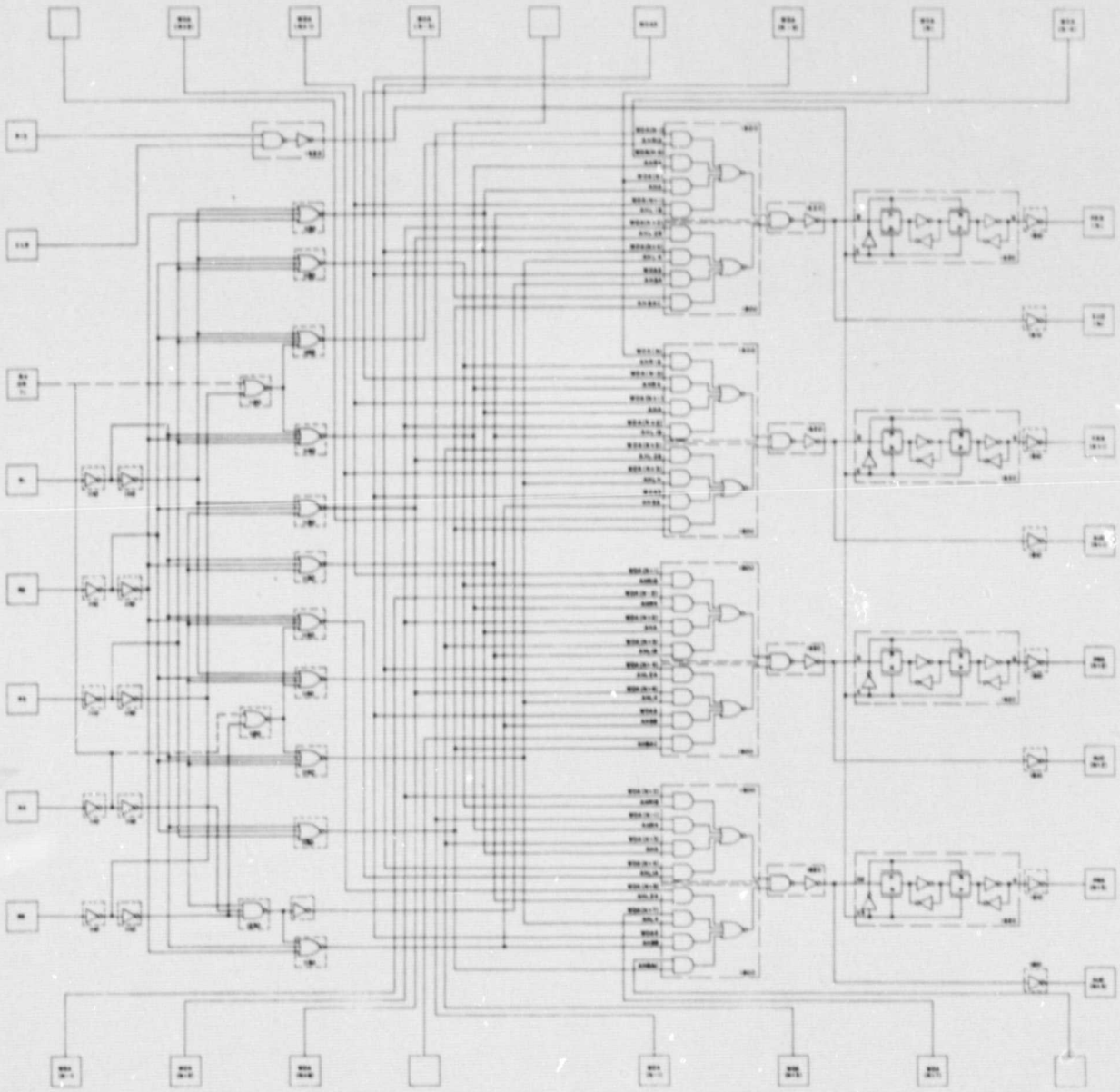

PIN 1 = SUPPLY VOLTAGE
PIN 21 = GROUND

Fig. 10. 001A multiplexer register chip, type 1 (PRR).

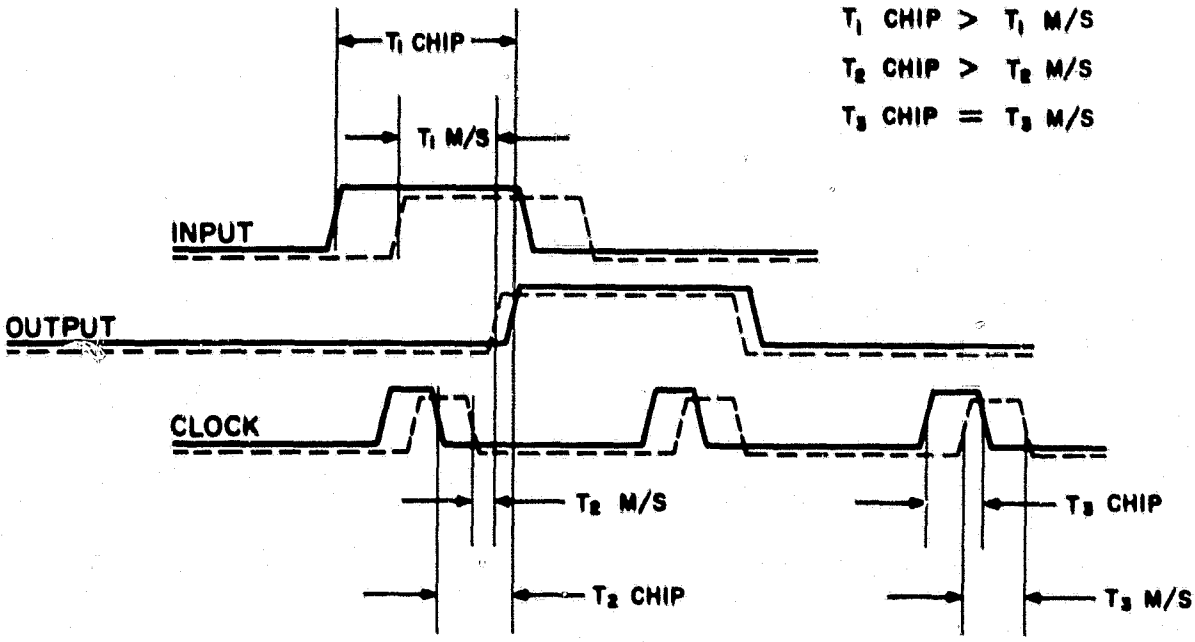

Fig. 11. Master-slave flip-flop delay vs. chip delay.

input, clock the information into the master and then into the slave. The ripple through timing waveforms are shown in Fig. 12. As shown in Table 5, for 10-V

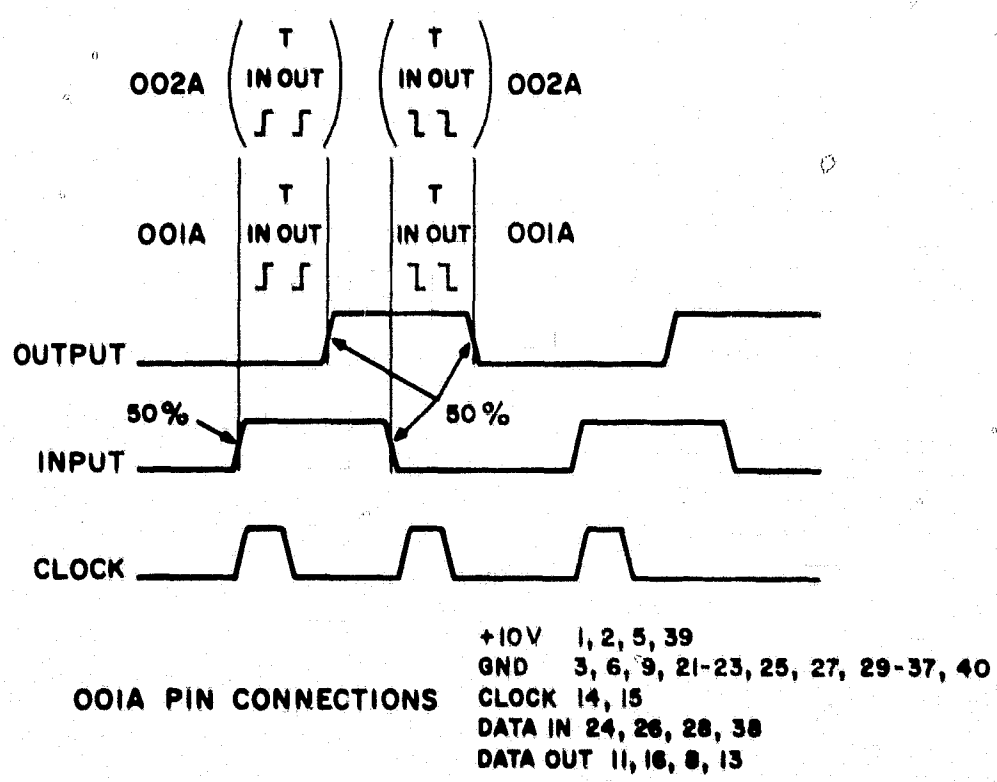

Fig. 12. Ripple through timing waveforms.

TABLE 5. RIPPLE THROUGH TIME

10-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY IN ⎍ OUT ⎍ (ns)	TIME DELAY IN ⎏ OUT ⎏ (ns)	INPUT PIN	OUTPUT PIN
7128C	7	11.0	143	116	24	11
7128C	7	10.8	134	110	26	16
7128C	8	11.0	164	133	24	11
7128C	8	11.2	160	129	26	16
7128C	7	29	162	129	24	11
7128C	8	29	184	140	24	11
7128C	7	111	243	167	24	11
7128C	8	111	276	181	24	11

5-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY IN ⎍ OUT ⎍ (ns)	TIME DELAY IN ⎏ OUT ⎏ (ns)	INPUT PIN	OUTPUT PIN
7128C	7	11	500	350	24	11
7128C	7	29	560	380	24	11
7128C	7	111	790	450	24	11

operation and an average total output node capacitance of 11.0 pF, the average time delay between a rising input edge and a rising output edge was 150 ns. Average time delay between a falling input edge and a falling output edge measured 122 ns.

The intrinsic capacitance associated with an output node, the packaging capacitance, the wiring capacitance and the scope probe capacitance combine to generate an output capacitive load of from 9.5 to 13.0 pF. One set of propagation delay data

on all PRR and MQR chips was taken at this output loading condition. Additional propagation delay measurements were made with as much as 100 pF of extra capacitance loading the outputs.

The second delay measurement made on the master-slave flip-flops was the "clock-out" time, which is the time delay between the activation of the slave (falling edge of the clock pulse) and the appearance of the slave information at the output of the chip (see Fig. 13). Representative clock-out data is presented in Table 6. For 10-V

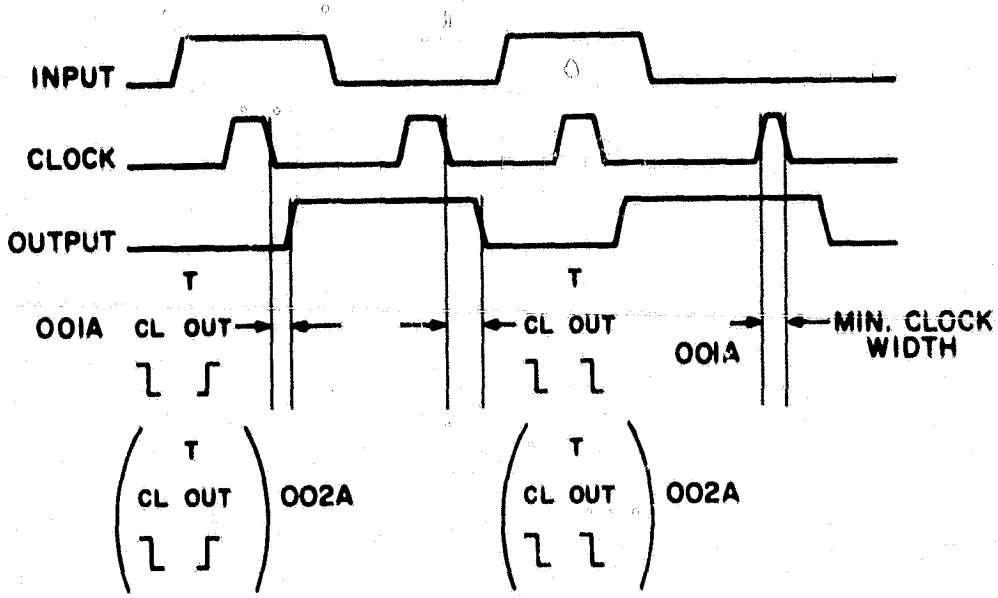

Fig. 13. Clock-out and minimum clock width.

operation and an average total node capacitance of 10.2 pF, the average time delay between a falling clock edge and a rising output edge measured 70 ns. The average time delay between the falling clock edge and the falling output edge was found to be 51 ns.

The third test made on the PRR (001A) master-slave was the determination of the minimum clock pulse width necessary to transfer information into the master. The test was conducted by placing a bit of information at the input of the master-slave flip-flop and increasing the clock pulse width until the bit of information was passed

TABLE 6. 001A CLOCK-OUT TIME

10-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY CL OUT (ns)	TIME DELAY CL OUT (ns)
7135F	10	10.8	68	51
7128C	7	9.9	65	49
7128C	8	9.9	71	51
7135F	10	28.8	90	72
7128C	7	27.9	85	65
7123F	17	28.3	97	64
7135F	2	110.8	200	115
7135F	7	111.1	225	137
7135F	10	110.8	196	141

Input Pulse: pin 28
Output Pulse: pin 8
Clock Pulse: pins 14, 15

5-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY CL OUT (ns)	TIME DELAY CL OUT (ns)
7128C	7	11	245	107
7128C	7	19	306	132
7128C	7	111	528	208

through the master-slave flip-flop. For 10-V operation, the minimum clock pulse width averaged 22 ns, independent of output pin loading. For 5-V operation the minimum clock pulse width averaged 80 ns for the three chips tested at 5 V.

b. Multiplexed Direct Output Propagation Delay

Input data to the four master-slave flip-flops on the PRR chip is inverted and brought out on output pins 10, 12, 17 and 18. Propagation delay was measured

from the multiplexed inputs of the PRR chip to these direct outputs. The data path that was measured was from input node [1] to output node [3] (see Fig. 9). Typical propagation delays for this path are shown in Table 7. For 10-V operation and an average total output node capacitance of 11.3 pF, the propagation delay from a rising edge input to a rising edge output averaged 65.6 ns and the delay from a falling edge input to a falling edge output averaged 79.6 ns.

TABLE 7. 001A DIRECT OUTPUT PROPAGATION DELAY

10-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY IN ⎍ OUT ⎍ (ns)	TIME DELAY IN ⎌ OUT ⎌ (ns)	INPUT PIN	OUTPUT PIN
7128C	7	11.5	66	78	28	18
7128C	7	10.7	64	78	38	12
7128C	8	11.5	71	87	28	18
7128C	8	10.8	66	87	38	12
7128C	7	33.5	94	95	28	18
7128C	7	32.7	94	95	38	12
7128C	8	33.5	99	104	28	18
7128C	8	32.8	101	108	38	12

5-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY IN ⎍ OUT ⎍ (ns)	TIME DELAY IN ⎌ OUT ⎌ (ns)	INPUT PIN	OUTPUT PIN
7128C	7	10.5	133	178	24	10
7128C	7	28.5	182	196	24	10
7128C	7	110.5	410	270	24	10

c. Stage Delay

Average stage delay for a data path is defined as the propagation delay associated with that data path divided by the number of stages in the path. The average stage delay was calculated for three paths in the PRR chip. They are the "ripple through" path, the "clock-out" path and the "multiplexer direct output" path. These three paths (see Fig. 9) represent signals passing from nodes 1 to 6, 4-5 to 6, 1 to 3, respectively. The average stage delay for each of these paths is presented in Table 8.

TABLE 8. AVERAGE STAGE DELAY (10-V OPERATION)

BETWEEN NODES			AVERAGE PROPAGATION DELAY (ns)	AVERAGE NUMBER OF STAGES	AVERAGE STAGE DELAY (ns)
1	6	⌠ ⌠	150*	8	18.8
1	6	⌡ ⌡	122*	8	15.3
4-5	6	⌡ ⌠	70	5	14
4-5	6	⌡ ⌡	51	5	10.2
1	3	⌠ ⌠	65.6	4	16.4
1	3	⌡ ⌡	79.6	4	19.9

*Includes time to clock data from input to master and from master to slave output.

B. MULTIPLEXER REGISTER CHIP, TYPE 2

The logic for the multiplexer register chip, type 2, MQR (ATL 002A)*, is contained in Fig. 14. One of the two four-bit registers included on the MQR chip incorporates many of the logic functions found on the PRR chip. One register has multiplexed inputs which allow the passage of unshifted data, a right shift of four bits or a left shift of one or two bits. Master-slave flip-flops are utilized as the storage elements. Control logic on the MQR array controls the mode of the input multiplexers.

*The multiplexer register chip type 2, is referenced in this report either by the abbreviation MQR or the RCA-ATL number 002A.

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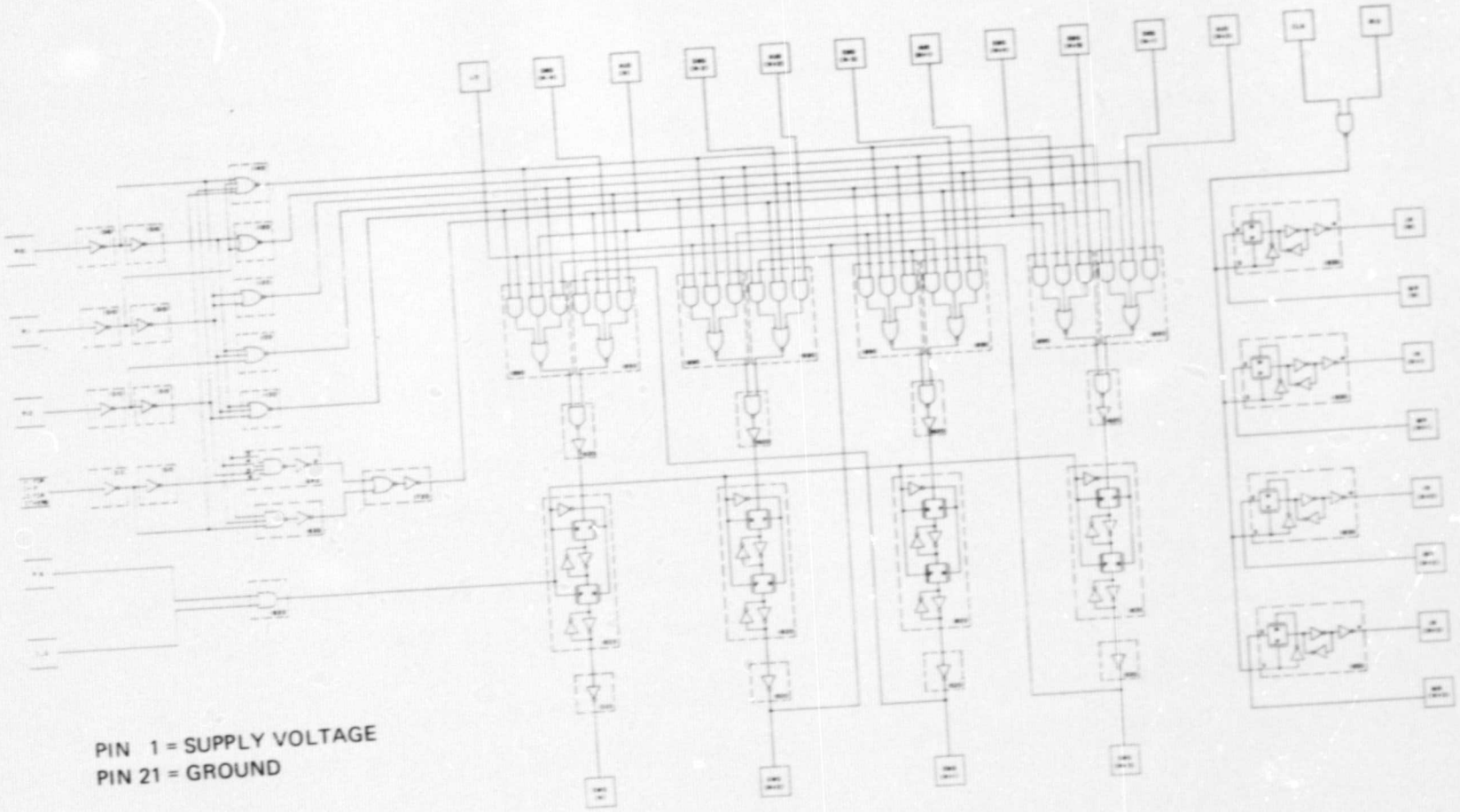

Fig. 14. Multiplexer register chip, type 2, MQR (ATL 002A).

Also included on the MQR chip are four register bits using D-type flip-flops. No shift capability is provided in this register. Implementation of the desired logic functions is achieved by using 42 standard cells (13 standard cell types), which represent 300 transistors or 112 gates. The chip measures 0.120 x 0.120 inch.

Many of the tests conducted on the PRR chips are similar to tests performed on the MQR chips. For this reason, frequent reference will be made to PRR test explanations.

The tests conducted on the MQR chips fall under the general headings of functional testing, leakage and propagation delay. All tests were conducted with a 10-V supply voltage and 10-V input pulses. In addition, all propagation delay measurements were conducted with a 5-V supply voltage and 5-V input pulses.

1. Functional Testing

A complete set of computer generated logical conditions was applied to the inputs of all of the MQR chips to check the correctness of the internal logic.

2. Leakage

a. Static Leakage

Static leakage current was measured in the ground line of all of the chips with all inputs tied to ground. Figure 7 shows the MQR static leakage test setup.

Median leakage for the chips was 1 μA; therefore, the median static power was 10 μW per chip. Table 9 shows the results for the static leakage tests.

b. Dynamic Leakage

Dynamic leakage current was measured in the ground line of four MQR chips for clock frequencies up to 1 MHz. The four master-slave flip-flops and the four D-type flip-flops were simultaneously clocked during the dynamic leakage test.

TABLE 9. STATIC LEAKAGE - MQR CHIP

BATCH NO.	CHIP NO.	STATIC LEAKAGE (μA)	BATCH NO.	CHIP NO.	STATIC LEAKAGE (μA)
7135G	1	< 1	7135H	11	< 1
7135G	2	< 1	7135H	12	< 1
7135G	4	< 1	7135H	13	< 1
7135G	5	550	7135H	14	360
7135H	1	< 1	7135H	15	< 1
7135H	2	< 1	7135H	16	18
7135H	5	< 1	7135H	17	< 1
7135H	6	< 1	7135H	18	< 1
7135H	8	40	7135H	21	1.2
7135H	10	< 1	7135H	23	< 1

Clock pulses were entered on pins 12, 13, 34 and 35. Data was entered to the eight flip-flops at half the clock frequency on pins 5, 7, 9, 11 and 22. Pins 16, 21 and 36 were grounded and supply voltage was applied to pins 1, 5, 7, 9, 11-15, 17, 23, 24, 26, 29 and 39. The pin connections to ground and supply voltage were also used for all other dynamic tests.

Figure 15 shows the average power dissipation per chip vs. clock frequency. Similarly, as with the PRR chip, dynamic power consumption of the 002A chip is several orders of magnitude greater than static power consumption for even moderately slow clock frequencies (0.34-0.5 MHz).

3. Propagation Delay

a. Propagation Delay of Master-Slave Flip-Flop

Three propagation delay measurements were made on the data paths, which include the No. 1820 master-slave flip-flops. The propagation delay

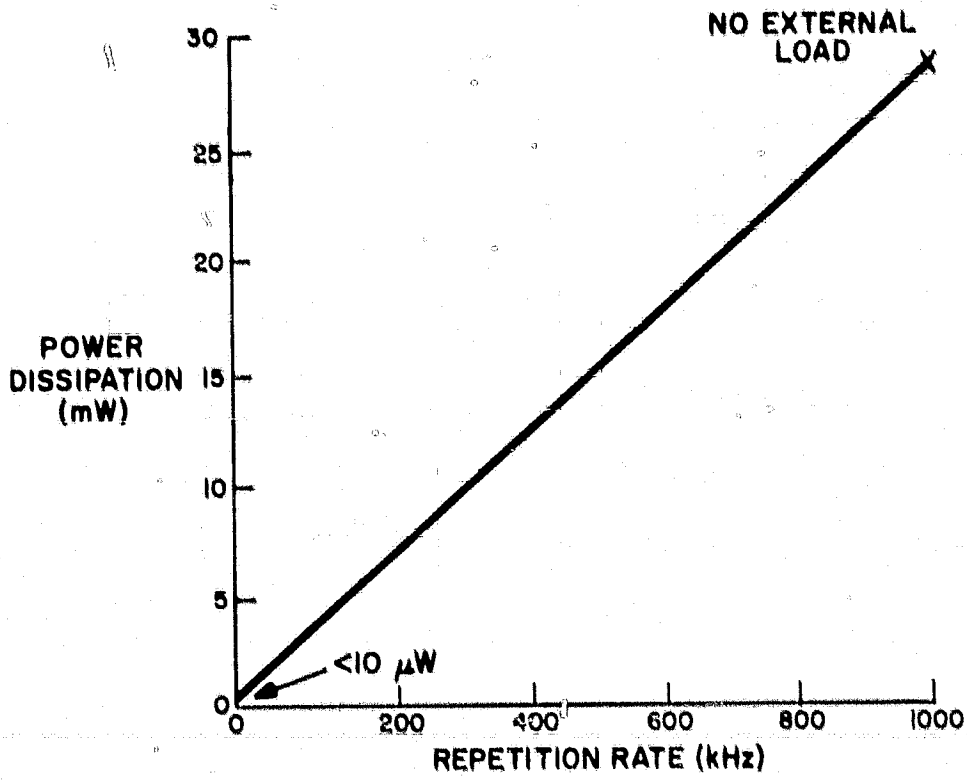

Fig. 15. Average power dissipation vs. clock frequency, MQR chip (002A).

measurements made on the 002A master-slave register were the "ripple through" time, the "clock-out" time and the "minimum clock pulse width." The descriptions for these tests are the same as those for the PRR (001A) chip.

The data test paths involving the master-slave flip-flops for the 001A and 002A are identical in function. The MQR master-slave data path is implemented differently than the 001A in two respects: 1) the 001A input multiplexers are 2, 2, 2, 2 AND - 4 NOR gates, while the 002A input multiplexers are 2, 2, 2 AND - 3 NOR gates; and 2) the output driver on the 002A chip is larger than that on the PRR chip.

Representative ripple through propagation delay data is shown in Table 10. For 10-V operation the average propagation delay for a rising edge input pulse is 126 ns and for a falling edge is 109 ns, for an average total output node capacitance of 14.4 pF.

TABLE 10. 002A (MQR) RIPPLE THROUGH TIME

10-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY IN ⎍ OUT ⎍ (ns)	TIME DELAY IN ⎏ OUT ⎏ (ns)	INPUT PIN	OUTPUT PIN
7135G	1	14.8	120	105	22	32
7135H	1	14.3	131	109	22	32
7135H	2	14.1	125	111	22	32
7135H	5	14.3	128	110	22	32
7135G	1	32.8	134	120	22	32
7135H	1	32.3	142	120	22	32
7135G	1	114.8	177	156	22	32
7135H	1	114.3	191	156	22	32

5-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY IN ⎍ OUT ⎍ (ns)	TIME DELAY IN ⎏ OUT ⎏ (ns)	INPUT PIN	OUTPUT PIN
7135G	1	14.8	244	212	22	32
7135G	1	32.8	256	228	22	32
7135G	1	114.8	324	280	22	32

Representative clock-out data for the 002A is presented in Table 11. With an average total output node capacitance of 14.4 pF, the average time delay between a falling clock edge and a rising output edge was 56 ns. The average time delay between a falling clock edge and a falling output edge measured 47 ns. The clock-out timing waveforms are shown in Fig. 13.

TABLE 11. 002A (MQR) CLOCK-OUT TIME

10-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY CL ⎿ OUT ⎾ (ns)	TIME DELAY CL ⎿ OUT ⎿ (ns)
7135G	1	14.8	54	46
7135H	1	14.3	55	45
7135H	2	14.1	58	51
7135H	5	14.3	55	46
7135G	1	32.8	66	59
7135H	1	32.3	66	59
7135G	1	114.8	110	98
7135H	1	114.3	116	94

Input Pulse - pin 22
Output Pulse - pin 32
Clock - pins 34, 35

5-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	TIME DELAY CL ⎿ OUT ⎾ (ns)	TIME DELAY CL ⎿ OUT ⎿ (ns)
7135G	1	14.8	113	101
7135G	1	32.8	130	119
7135G	1	114.8	212	172

The average minimum clock pulse width necessary to transfer information into the master of the MQR master-slave flip-flops was 22 ns at 10-V operation. The minimum clock pulse width is independent of the output node capacitance.

b. Propagation Delay of D-Type Flip-Flop

The 002A array has four D-type flip-flops per chip, each of which has a single input, single output and a common clock. The D-type flip-flop cell configuration

and pin numbers are shown in Fig. 16. Two delay measurements were made on the D flip-flop. They are designated as the "direct feedthrough" time and the "D clocked output" time. In the direct feedthrough test, the clock inputs (pins 12 and 13) to the D flip-flops were held high so that input information could pass directly through the flip-flop. Propagation delay was measured between the input and output of the flip-flop. For the D clocked output test, a data level was placed at the input of a D flip-flop and then the clock input was enabled (rising edge pulse). The propagation delay was measured between the enabling clock edge and the flip-flop output. The timing waveforms for the direct feedthrough and the D clocked output tests are shown in Fig. 17.

Representative data for the direct feedthrough and D clocked output tests is presented in Table 12. For 10-V operation and an average total node capacitance of 10.6 pF the average direct feedthrough propagation delay associated with a rising edge input is 36 ns. For the falling edge input the average propagation delay is 33 ns. For the D clocked output test, the average delay from a positive clock edge to a positive output edge is 50 ns. From a positive clock edge to a falling output edge the average delay is 53 ns.

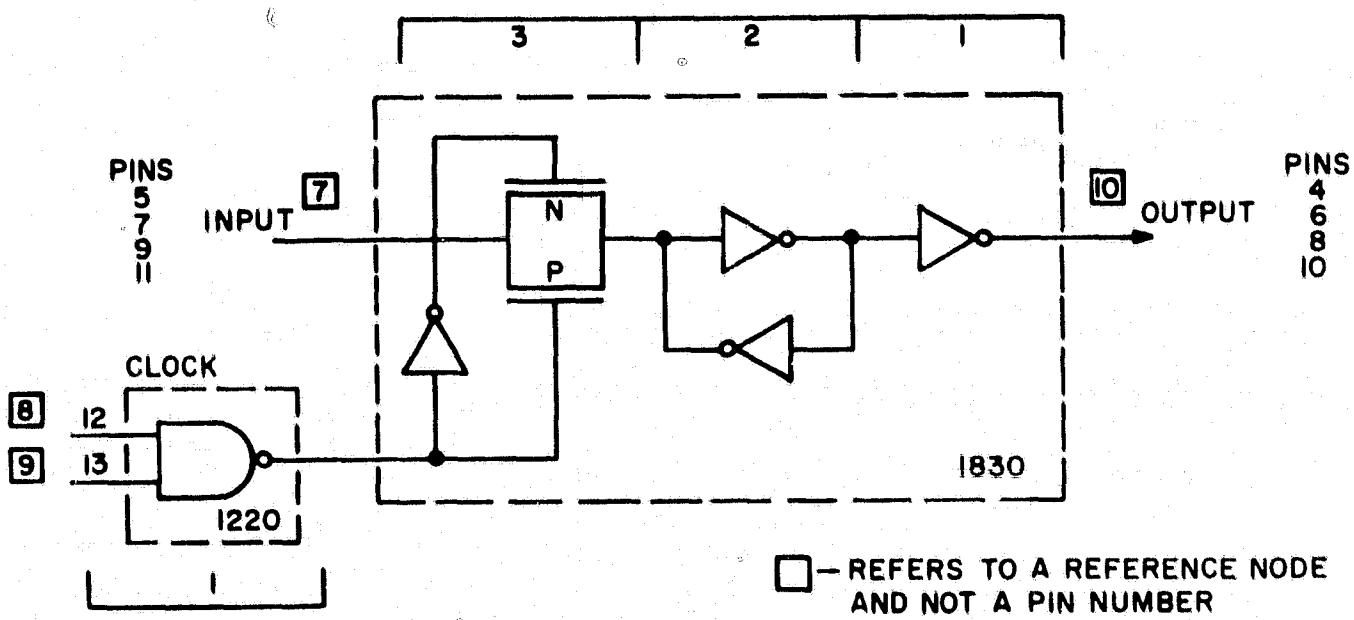

Fig. 16. D-type flip-flop on 002A chip.

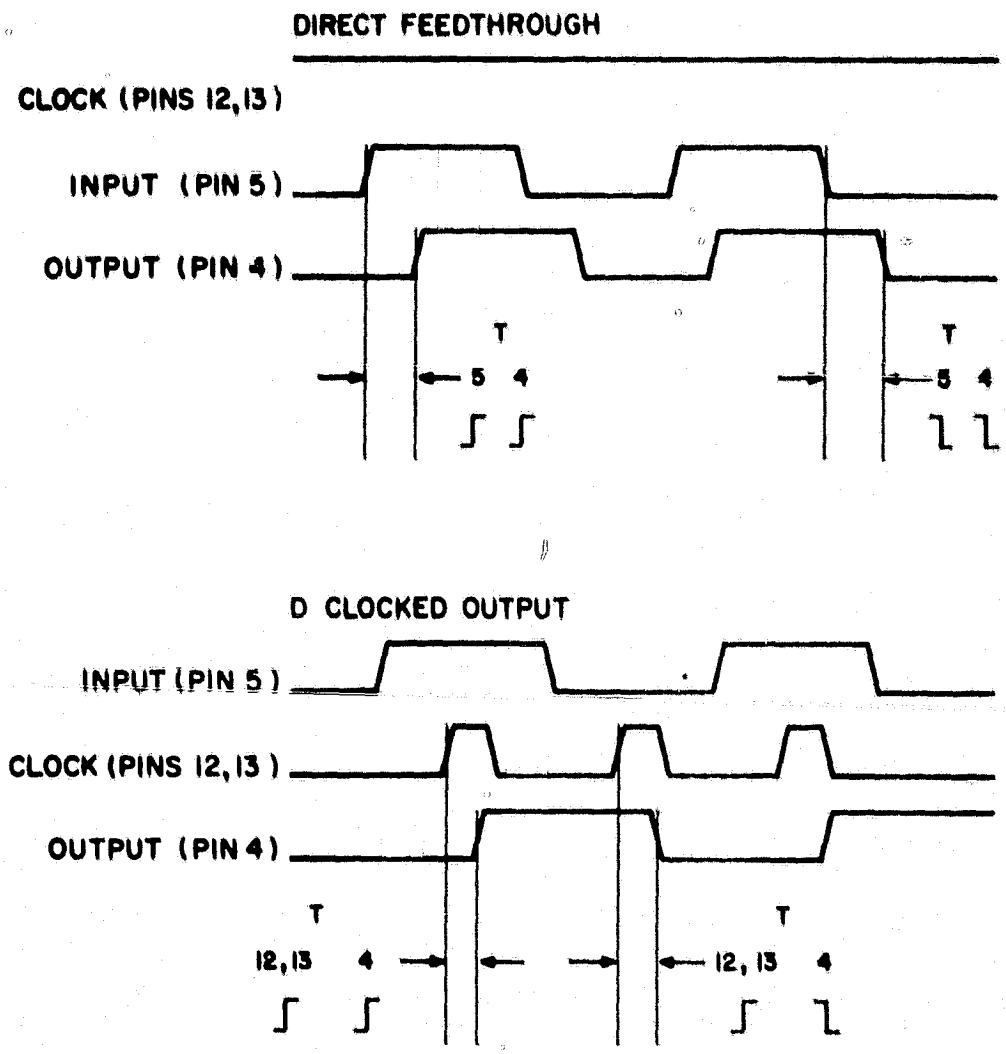

Fig. 17. D-type flip-flop waveforms.

c. Average Stage Delay

The average stage delay is calculated in Table 13 for each of the four delay measurements made on the master-slave and D-type flip-flops. The number of stages involved in each measurement can be determined by referring to Fig. 9 for the master-slave flip-flop tests and to Fig. 14 for the D-type flip-flop tests.

TABLE 12. DIRECT FEEDTHROUGH, D CLOCKED OUTPUT

10-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	DIRECT FEED-THROUGH		D CLOCKED OUTPUT	
			TIME DELAY 5 4 (ns)	TIME DELAY 5 4 (ns)	TIME DELAY 12, 13 4 (ns)	TIME DELAY 12, 13 4 (ns)
7135H	1	10.6	39	36	52	54
7135G	1	10.7	36	33	48	52
7135H	1	28.6	58	47	70	60
7135G	1	28.7	51	45	63	64
7135H	1	110.6	130	91	143	110
7135G	1	110.7	118	93	125	110

5-V OPERATION

BATCH NUMBER	CHIP NUMBER	OUTPUT NODE CAPACITANCE (pF)	DIRECT FEED-THROUGH		D CLOCKED OUTPUT	
			TIME DELAY 5 4 (ns)	TIME DELAY 5 4 (ns)	TIME DELAY 12, 13 4 (ns)	TIME DELAY 12, 13 4 (ns)
7135H	1	10.6	63	76	102	114
7135H	1	28.6	99	101	140	136
7135H	1	110.6	238	177	292	222

C. SUMMARY

A summary of the average values of all data taken on the PRR and MQR chips is presented in Table 14. All average values shown are for 10-V operation and no external output capacitance.

TABLE 13. 002A AVERAGE STAGE DELAY

10-V OPERATION

	BETWEEN NODES			AVERAGE PROPAGATION DELAY (ns)*	AVERAGE NUMBER OF STAGES	AVERAGE STAGE DELAY (ns)
RIPPLE THROUGH	2	6	⎍ ⎍	126*	8	15.8
	2	6	⎏ ⎏	109*	8	13.6
CLOCK-OUT	4-5	6	⎏ ⎍	56	5	11.2
	4-5	6	⎏ ⎏	47	5	9.4
DIRECT FEEDTHROUGH	7	10	⎍ ⎍	36	3	12
	7	10	⎏ ⎏	33	3	11
D CLOCKED OUT	8-9	10	⎍ ⎍	50	4	12.5
	8-9	10	⎍ ⎏	53	4	13.3

*Includes time to clock data from input to master and from master to slave output.

TABLE 14. SUMMARY OF TEST RESULTS – 001A AND 002A (10-V OPERATION)

Table 14

FUNCTIONAL PROPAGATION DELAY

TEST	STATIC LEAKAGE		DYNAMIC LEAKAGE	LIFE TESTS	PROPAGATION DELAY RIPPLE THROUGH (ns)		PROPAGATION DELAY CLOCK-OUT (ns)		PROPAGATION DELAY MIN. CLOCK WIDTH (ns)	PROPAGATION DELAY MASTER-SLAVE BYPASS (ns)	
	ALL INPUTS TIED TO GROUND	ALL INPUTS TIED TO +10 V	CLOCK FREQUENCY EQUALS 1 MHz	STATIC LEAKAGE, DYNAMIC PERFORMANCE, ELEVATED TEMP.	∫ ∫	⎍ ⎍	⎍ ∫	⎍ ⎍		∫ ∫	⎍ ⎍
001A	< 1 μA	< 1 μA	1.8 mA	In Progress	150	122	70	51	22	65.6	79.6
002A	< 1 μA	–	2.8 mA	None	126	109	56	47	22	–	–

AVERAGE STAGE DELAY

TEST	PROPAGATION DELAY DIRECT FEEDTHROUGH (ns)		PROPAGATION DELAY D CLOCKED OUTPUT (ns)		AVERAGE STAGE DELAY RIPPLE THROUGH (ns)		AVERAGE STAGE DELAY CLOCK-OUT (ns)		AVERAGE STAGE DELAY MULTIPLEXED DIRECT OUTPUT (ns)		AVERAGE STAGE DELAY DIRECT FEEDTHROUGH (ns)		AVERAGE STAGE DELAY D CLOCKED OUTPUT (ns)	
	∫ ∫	⎍ ⎍	∫ ∫	∫ ⎍	∫ ∫	⎍ ⎍	⎍ ∫	⎍ ⎍	∫ ∫	⎍ ⎍	∫ ∫	⎍ ⎍	∫ ∫	∫ ⎍
001A	–	–	–	–	18.8	15.3	14	10.2	16.4	19.9	–	–	–	–
002A	36	33	50	53	15.8	13.6	11.2	9.4	–	–	12	11	12.5	13.3

Section IV

CONCLUSIONS

The required logic for the register and multiplexer units was incorporated into the design of two chip types—multiplexer register chip, types 1 and 2. These LSI arrays, which used the CMOS circuit technology, were designed and fabricated by using the standard cell design automation technology. This technology uses a series of design automation computer programs, combined with a family of previously designed and stored circuits called standard cells, to generate precision mask artwork for the LSI CMOS arrays.

Multiplexer register chip type 1 is fabricated on a 0.143 x 0.123 inch chip. The logic is implemented by using nine standard cell types for a total of 54 standard cells. This involves more than 350 transistors and has the functional equivalent of 111 gates. Multiplexer register chip type 2 is fabricated on a 0.12 x 0.12 inch die. It uses 13 standard cell types for a total of 42 standard cells. The chip contains more than 300 transistors, the functional equivalent of 112 gates.

The circuits are housed in hermetically sealed 40-pin dual-inline ceramic packages and subjected to the standard IC qualification testing procedures. To pass the initial screening, all circuits were tested for correct functional operation. Subsequent screening included static and dynamic leakage testing, followed by extensive dynamic performance testing.

Sixty units (forty ATL 001A's and twenty ATL 002A's) were delivered as required by the contract. Over 40 of these units yielded static currents of less than 1 μA for a total static dissipation of less than 10 μW at 10 V.

Several of the units were subjected to static and dynamic life testing at elevated temperatures. In addition to the extensive testing at 10 V, the results of which are documented in this report, many of the units were tested dynamically at 5 V. This included propagation delay measurements through logic circuits to the maximum shifting rate of the D-type master-slave register. At 10 V some registers shifted data at a 14-MHz rate, and at 5 V the units operated at a 6.6-MHz rate.

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