A system for displaying at a remote station data generated at a central station and for powering the remote station from the central station. A power signal is generated at the central station and time multiplexed with the data and then transmitted to the remote station. An energy storage device at the remote station is responsive to the transmitted power signal to provide energizing power for the circuits at the remote station during the time interval data is being transmitted to the remote station. Typically, the data is time of day information and the remote station effects remote display of the time.

Energizing power for the circuits at the remote station is provided by the power signal itself during the time this signal is transmitted. Preferably the energy storage device is a capacitor which is charged by the power signal during the time the power is transmitted and is slightly discharged during the time the data is transmitted to energize the circuits at the remote station. The transmitted time of day data is pulse width modulated and decoder circuitry at the remote station is responsive to the transmitted data to effect decoding thereof.

13 Claims, 6 Drawing Figures
FIG. 1

CONTROL LOGIC CIRCUITRY

SERIAL DISPLAY DATA LOGIC CIRCUITRY (FIG. 3)

DISPLAY DRIVER CIRCUITRY (FIG. 4)

TIME CODE RECEIVER AND DISPLAY (FIG. 4)

TIME COUNTING CIRCUITRY

FIG. 2

TRUE LOGIC LEVEL

TZ

TZ + 53µS

TZ + 53µS

TZ + 69µS

TZ + 69µS

+V LEVEL

+V

FIG. 5

CLOCK SAMPLE POINT

"0"

2.0µS

OV

"1"

5.0µS

8.0µS

10.0µS
SYSTEM FOR DISPLAYING AT A REMOTE
STATION DATA GENERATED AT A CENTRAL
STATION AND FOR POWERING THE REMOTE
STATION FROM THE CENTRAL STATION

ORIGIN OF INVENTION

The invention described herein was made by an em-
ployee of the United States Government and may be
manufactured and used by and for the Government for
governmental purposes without the payment of any
royalties thereon or therefor.

BACKGROUND OF THE INVENTION

This invention relates to data display systems and, in
particular, to systems for remotely displaying data such as
the time of day.

Previous systems for remotely displaying time of day
information basically involve either the parallel or serial
transmission of the time data. Typically, in parallel
transmission systems, 30 line drivers are required at the
sending end with a 30 wire cable connecting the remote
read-out to the master generator. Further, the remote
display unit requires 30 line receivers with nine, 4-to-10
(for Nixie) or 4-to-7 segment (for LED) decoders de-
pending on the type of display. Also a large power
supply is required if gas discharge type read-outs are employed.

In serial transmission systems, a serial code is em-
ployed with a frame sync pattern to transmit BCD data
in segmented time divisions, requiring sub-frame identifi-
cation and a modulated carrier. At the remote display,
a sophisticated automatic gain control is required to
normalize the signal so it can be reliably demodulated.

Further, a frame sync detector is required along with
frame sync counters, data storage, 4-to-10 or 4-to-7
decoders, along with display drivers, current limiting
resistors for each segment and a large power supply
with several voltages to operate the logic circuitry.

Again, a high power supply voltage (approximately
250 volts D.C.) is needed if a gas display read-out is em-
ployed.

It is known in the prior art to transmit data from a
first location to a second location over a single line and
to send a power signal back to the first location from the
second location over the same line. Thus, a data collec-
tion system is known wherein a series of remote trans-
mitters are connected to sensors for forwarding data to
a central receiver. Power for the transmitters is sent
over the line to recharge batteries respectively associ-
ated with the transmitters. It is also known to provide a
digital compass which is supported by a gimbal assem-
bly which, in turn, is electrically connected to a con-
ductor. Energizing power is supplied to the compass
through the gimbal and data for read-out in the same
manner. Other telemetry systems and similar systems
are also known having a signal line carrying power in
one direction and data in the other. However, in none of
the foregoing systems are the power and data both
transmitted in the same direction to a remote device
such as a remote time display.

SUMMARY OF THE INVENTION

This invention relates to a system for displaying at at
least one remote station data generated at a central
station and for powering the remote station from the
central station over the same line employed for data
transmission. The foregoing is effected by circuitry
which results in a straightforward, low cost, small size,
reliable, data display device having low energy require-
ments and no power supply.

Other objects and advantages of this invention will be
apparent from a reading of the following specification
and claims taken with the drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of an illustrative, overall
system in accordance with the invention.

FIG. 2 is a waveform showing an illustrative data
signal employed in the system of FIG. 1.

FIG. 3 is a combined block and schematic diagram of
illustrative serial display data logic circuitry for use in
the system of FIG. 1.

FIGS. 4a and 4b are a combined block and schematic
diagram of illustrative display driver circuitry and time
code receiver and display circuitry for use in the system
of FIG. 1.

FIG. 5 shows waveforms illustrating the decoding
operation effected at the time code receiver of FIG. 1.

DETAILED DESCRIPTION OF THE
PREFERRED EMBODIMENTS OF THE
INVENTION

Reference should be made to the drawing where like
reference numerals refer to like parts.

In FIG. 1, there is shown an illustrative embodiment
of an overall system in accordance with the invention
where the generator 10 within the dotted block pro-
duces the data and power which are transmitted over
line 12 to time code receiver and display 14. The gener-
ator 10 included conventional time counting circuitry
16 which may have 63 output lines indicated at 18
where the signals on the output lines correspond to the
time of day (days (3 digits), hours (2 digits), minutes (2
digits), and seconds (2 digits)). Since, in this illustrative
embodiment, the data is intended for LED display,
which may have 63 output lines indicated at 18
where the signals on the output lines correspond to the
time of day (days (3 digits), hours (2 digits), minutes (2
digits), and seconds (2 digits)). Since, in this illustrative
embodiment, the data is intended for LED display,
where the generator 10 within the dotted block pro-
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line 12 to time code receiver and display 14. The gener-
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16 which may have 63 output lines indicated at 18
where the signals on the output lines correspond to the
time of day (days (3 digits), hours (2 digits), minutes (2
digits), and seconds (2 digits)). Since, in this illustrative
embodiment, the data is intended for LED display,
seconds. At TZ +1 microsecond the data is transmitted at a 100-kHz bit rate with a logic level at 0 V dc for 2 microseconds representing a logic "0" and a logic level at 0 V dc for 8 microseconds representing a logic "1".

Reference is now made to FIG. 3 which shows illustrative data logic circuitry 20 for generating the signal of FIG. 2 from the 63 parallel segments from time counting circuitry 16. The 63 segments are loaded into a plurality of shift registers 32 through 46 by an LDSR (LOAD SHIFT REGISTER) signal, which is generated by control logic circuitry 23 at TZ +51 microseconds and passed through a gate 31. The hundreds digit of the "day" data is applied in parallel to shift register 32 and is represented by the letters HDA through HDG. The progression from the hundreds digit of the "day" data to the units digit of the "second" data is from register 32 through register 46 where the units "second" digit is represented by the letters USA through USG. At the same time, a zero bit is loaded into the last stage (from TZ +689 to the next TZ). It should be appreciated that the transmission of the data signal can commence at some other time than TZ +51. Typically, the beginning of the data signal should be delayed after TZ to provide sufficient time for the +V signal to decrease to the true logic level of +4.0 volts shown in FIG. 2.

When D.C. power is on line 12, it is applied through a diode 78 in receiver 14 to supply D.C. power to a monostable multivibrator 80 and a plurality of serial-in, parallel-out shift registers 82 through 98. Further, the D.C. power charges a capacitor 100 to typically a +5 V dc level. When a data signal is on the line, diode 78 is preferably reverse-biased since the true logic level is +4 volts and since the size of capacitor 100 is preferably such that the voltage thereon decreases to no more than 4.5 volts during the time interval from TZ to TZ +689 microseconds. Accordingly, during this time the charge on capacitor 100 supplies D.C. power to multivibrator 80 and shift registers 82 through 98; however, it is preferably bled off from line 12 by diode 78.

At TZ +51 microseconds, the logic level drops from the true level (+4 V dc) to a zero level (0 V dc). This negative transition is applied to terminals 102 and 104 of multivibrator 80. After a delay of 5 microseconds as determined by resistor 106 and capacitor 108, a positive transition is applied to input terminal 110 to supply a clock signal to terminal 112 of shift registers 82 through 98, this being illustrated in FIG. 5.

The data signal is also applied to the base of a transistor 114 where it is inverted and applied to terminals 116 and 118 of shift register 82. If the input at these latter terminals is high at the 5 microseconds clock transition, the register is set; if it is low, the register is reset. This process continues for 64 clock cycles of which 63 are retained for use by a 9 digit LED display (7 segments for each digit) represented by blocks 120 through 130.

Resistor 136 provides load resistance for transistor 114; resistor 138 provides the pull-up resistance for the unused gates within multivibrator 80 and resistor 140 does the same for shift registers 82 through 98. Resistor 142 is the termination resistance for line 12 while resistors 132, 134 and 137 provide current limiting. For illustrative values of the resistors and other components of the system of this invention, the table below may be consulted, it being understood there is no intent that the invention be limited to any or all of these component values.
<table>
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<tr>
<th>REFERENCE NUMERAL</th>
<th>DESCRIPTION</th>
<th>MANUFACTURER</th>
<th>MANUFACTURER PART NO.</th>
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<tr>
<td>31,54</td>
<td>Gate</td>
<td>Texas Instruments</td>
<td>7408</td>
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<tr>
<td>32-58</td>
<td>Shift Registers</td>
<td>Texas Instruments</td>
<td>74LS165</td>
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<td>50</td>
<td>Gate</td>
<td>Texas Instruments</td>
<td>74LS02</td>
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<tr>
<td>52,56</td>
<td>Flip-flops</td>
<td>Texas Instruments</td>
<td>74LS74</td>
</tr>
<tr>
<td>60</td>
<td>Gate</td>
<td>Texas Instruments</td>
<td>74LS32</td>
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<tr>
<td>66</td>
<td>Drivers</td>
<td>Texas Instruments</td>
<td>74128</td>
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<tr>
<td>70</td>
<td>Transistor, silicon, high power, NPN</td>
<td>Motorola</td>
<td>MJE2100</td>
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<td>2N3904</td>
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<td>76</td>
<td>Diode, silicon, reference, 6.8 V dc (nominal)</td>
<td>Motorola</td>
<td>1N754A</td>
</tr>
<tr>
<td>78</td>
<td>Diode, silicon, hot-carrier, 400 mV (forward biased)</td>
<td>Motorola</td>
<td>1N5820</td>
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<td>80</td>
<td>Integrated Circuit, monostable multivibrator, multiple-input</td>
<td>Texas Instruments</td>
<td>74121</td>
</tr>
<tr>
<td>82-98</td>
<td>Integrated Circuit 8-bit gated serial parallel-in, right/ left shift register</td>
<td>Texas Instruments</td>
<td>74164</td>
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<tr>
<td>100</td>
<td>Capacitor, electrolytic, 330 μF, 10 V</td>
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<td>106</td>
<td>Resistor, fixed, composition, 7.5 KΩ ±10%, 1W</td>
<td></td>
<td></td>
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<tr>
<td>108</td>
<td>Capacitor, ceramic 0.001 μF, 50 V</td>
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<td>120-130</td>
<td>LED 7-segment</td>
<td>Monsanto</td>
<td>MAN6740</td>
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<tr>
<td>136,137</td>
<td>Resistor, fixed, composition, 5.6 KΩ ±10%, 1W</td>
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<tr>
<td>138,140</td>
<td>Resistor, fixed, composition, 1 KΩ ±10%, 1W</td>
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</tr>
</tbody>
</table>

Thus, in summary, there has been generally disclosed a system for displaying at at least one remote station data generated at a central station and for powering the remote station from the central station. The system generally may include means (power supply 28) at the central station for generating a power signal; means (circuits 20 and 24 of FIG. 1) for time multiplexing the data and power signal over a plurality of successive cycles so that the data occurs during a first interval (TZ + 689 microseconds, for example) of each cycle and the power signal occurs during a second interval of each cycle (TZ + 689 microseconds to the next TZ); transmission means (line 12, for example) for transmitting the time multiplexed signal to the remote station; storage means (capacitor 100) at the remote station responsive to the transmitted, time multiplexed signal for storing the power signal and display means (LED'S 120 through 130) at the remote station for displaying the data, the display means being powered by storage 65 means 100 during the first interval of each cycle. Further, a rechargeable battery could be employed as the power storage means in place of capacitor 100. However, a capacitor is preferred as being more compact and less costly.

What is claimed is:

1. A system for displaying at at least one remote station data generated at a central station and for powering the remote station from the central station, said system comprising:

   means at the central station for generating a power signal;

   means at the central station for generating a data signal;

   means at the central station for time multiplexing the data signal and power signal over a plurality of successive cycles so that said data signal occurs during a first interval of each cycle and said power signal occurs during a second interval of each cycle;

   transmission means for transmitting the time multiplexed signals to the remote station;

   storage means at the remote station responsive to the transmitted, time multiplexed signals for storing said power signal; and
display means at the remote station for displaying said data signal, said display means being powered by said storage means during said first interval of each cycle.

2. A system as in claim 1 where said data signal is a time of day signal.

3. A system as in claim 1 where said display means is powered by said power signal during said second interval of each cycle.

4. A system as in claim 1 where said storage means comprises a capacitor which is charged by said power signal during said second interval of each cycle.

5. A system as in claim 4 including rectifying means, said capacitor being charged through said rectifying means.

6. A system as in claim 5 where said rectifying means prevents said power signal from being returned to said transmission means during said first interval of each cycle.

7. A system as in claim 1 where said data signal comprises a sequence of pulse width modulated signals and where said remote station includes a demodulator responsive to said modulated signals and powered by said storage means during said first interval of each cycle.

8. A system as in claim 1 or 7 where said central station includes means for generating a plurality of signals respectively corresponding to elements of symbols to be displayed by said display means and means for pulse width modulating each of said plurality of signals for transmission as said data signal during said first interval of each cycle.

9. A system as in claim 8 where said power signal generating means includes means for generating a D.C. signal during said second interval of each cycle.

10. A system as in claim 9 where said power signal generating means further includes means for interrupting said D.C. signal during the first interval of each cycle.

11. A system as in claim 8 where said pulse width modulated signals are either a first or second width and where said remote station includes demodulating means including (a) means responsive to said pulse width modulated signals for generating clock signals a predetermined time after the beginning of each pulse width modulated signal, said predetermined time being greater than the time corresponding to said first pulse width and less than the time corresponding to said second pulse width and (b) means responsive to said pulse width modulated signals and said clock signals to determine the width of each of the pulse width modulated signals.

12. A system as in claim 1 where said power signal generating means includes means for generating a D.C. signal during said second interval of each cycle.

13. A system as in claim 12 where said power signal generating means further includes means for interrupting said D.C. signal during the first interval of each cycle.

* * * * *