SOLID STATE SYSTEMS CONCEPTS

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1.0 INTRODUCTION

This paper describes two prototype solid-state phased array systems concepts for potential use in the Solar Power Satellite (SPS). In both concepts, the beam is centered on the rectenna by means of phase conjugation of a pilot signal emanating from the ground. Also discussed is on-going solid-state amplifier development.

The basic systems concepts are now described in more detail.

2.0 OVERVIEW OF SOLID-STATE ARRAY CONCEPTS

Two different solid-state array concepts are being developed at this time: The End-Mounted Space System (Figure 1) and the Sandwich (Figure 2). Both concepts use the same element and spacing, but in the end-mounted system 36-watt amplifiers are mounted on the ground-plane, whereas in the sandwich the amplifiers are elevated to the dipoles, and their waste heat is dissipated by beryllium oxide discs. The feed lines are underneath the ground-plane, and a coaxial transmission line is carried all the way to the amplifier input. (See section on RF Signal Distribution). Figure 4 in Section 4 shows the sandwich dipole layout in close-up view.

3.0 SOLID-STATE PHASE CONTROL

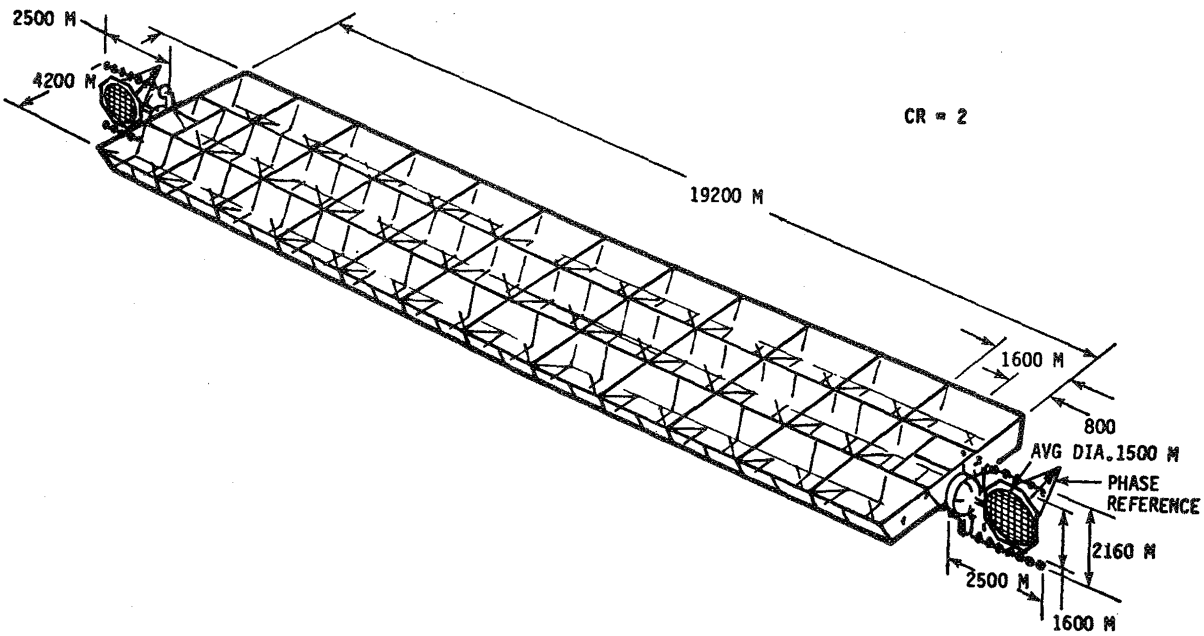
3.1 REFERENCE PHASE DISTRIBUTION

Phase conjugation at the 10 meter by 10 meter subarray is used to steer the beam. The reference phase signal is distributed over the spacetenna aperture via a radio link. Figure 3 illustrates this method giving a perspective view of the top of the aperture. Two important features are: (a) the phase reference signal originates from a single transmit location at the rear of the aperture; and (b) phase reference and pilot antennas are orthogonally polarized with respect to the power dipoles to avoid feedback loops. Instead of an endfire (e.g., "Cigar") array, broadside arrays can be used for reference and pilot pick-up. Both configurations shall be considered in more detail in future studies.

The phase reference signal is distributed as follows:

From the shaped-beam illuminator antenna an RF signal is distributed over a cone with maximally 90 degrees beamwidth. All reference pick-up antennas see approximately the same signal strength. The local oscillator and driver amplifer is redundant. Large variations in aperture flatness can be compensated modulo 2 π since bandwidth is of no concern for the reference phase signal. The phase at each subarray pick-up point is normalized with respect to a perfectly flat

FIGURE 1. END-MOUNTED SOLID STATE CONCEPT (REF. 1)

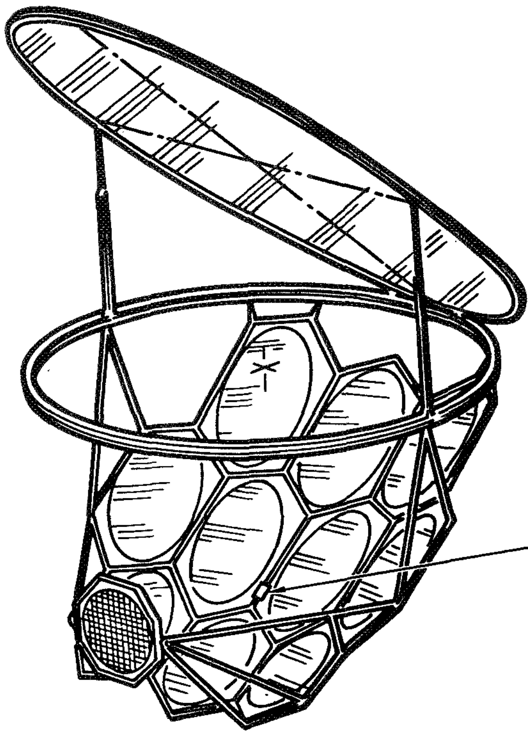


END-MOUNTED SOLID-STATE CONCEPT CHARACTERISTICS

- o GaAs SOLAR ARRAY
- o GEOMETRIC CR = 2.0
- o DUAL END-MOUNTED MICROWAVE ANTENNAS
- o AMPLIFIER BASE TEMPERATURE = 125^{o}C
- o AMPLIFIER EFFICIENCY = 0.8
- o ANTENNA POWER TAPER - 10dB
- o ANTENNA DIAMETER = 1.35 km
- o POWER AT UTILITY INTERFACE = 2.61 GW PER ANTENNA (5.22 GW TOTAL)
- o RECTENNA BORESIGHT DIAMETER = 7.51 km PER RECTENNA

Ref. 1) After: G. M. Hanley, SPS Concept Definition Study (Exhibit D), First Performance Review - 10 October 1979.

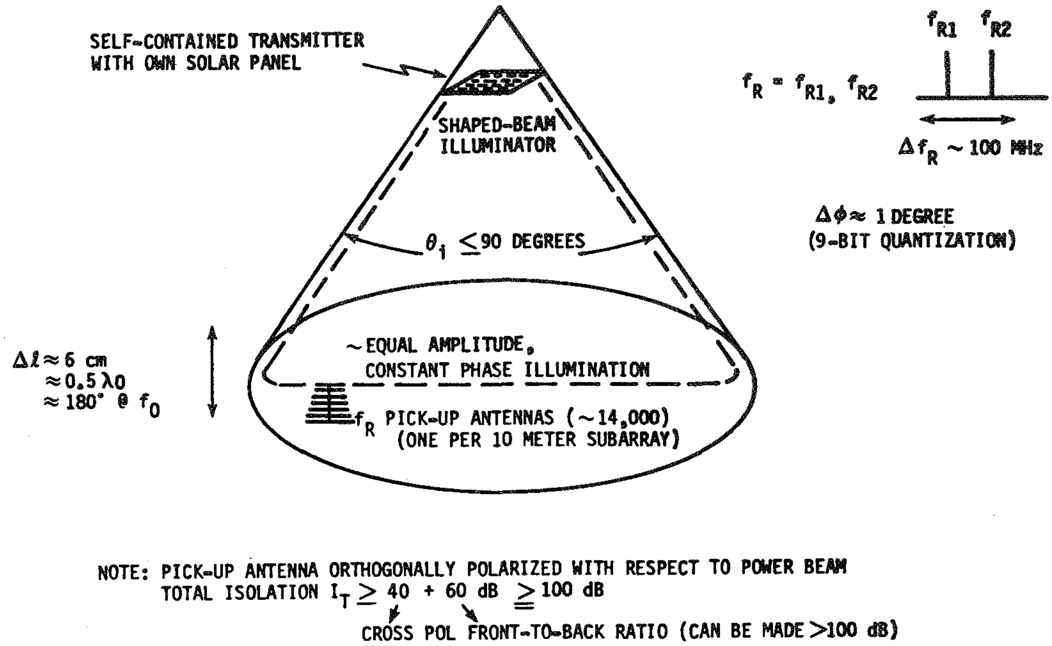
FIGURE 2. SOLID STATE SANDWICH CONCEPT RECOMMENDED FOR POINT DESIGN (REF. 1)

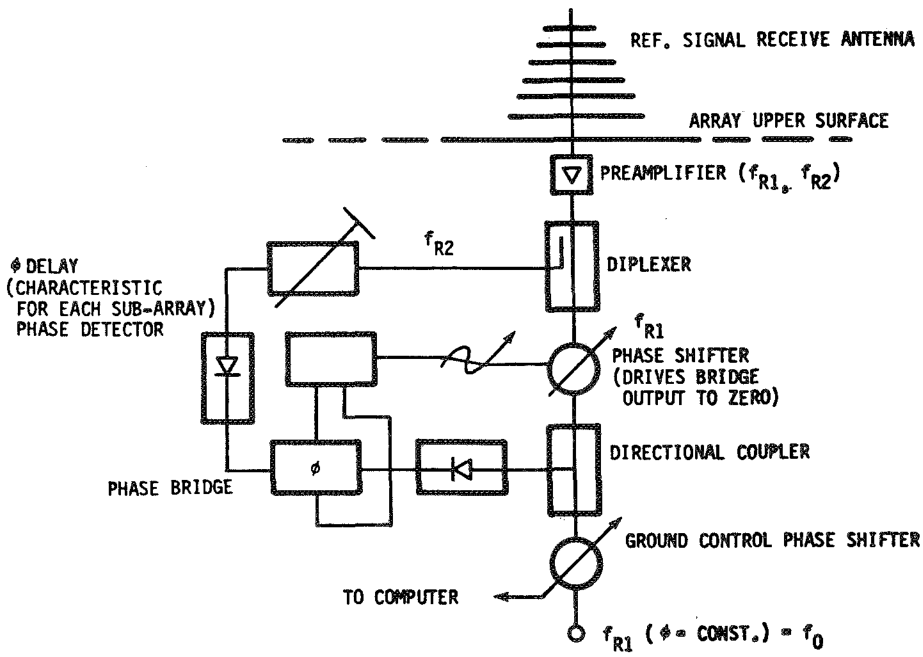


RECOMMENDED SOLID-STATE SANDWICH CONCEPT CHARACTERISTICS

CHARACTERISTIC	PRIMARY	SECONDARY
SOLAR ARRAY TYPE	GaAs	MULTI-BANDGAP
EFFECTIVE CR	6	5 TO 6
SOLAR ARRAY TEMP. (^{o}C)	200	200
AMPLIFIER BASE TEMP. (^{o}C)	125	125
AMPLIFIER EFFICIENCY	0.8	0.8
ANTENNA TAPER RATIO (dB)	0	0
ANTENNA DIAMETER (Km)	1.77	1.64 TO 1.58
POWER AT UTILITY INTERFACE (GW)	1.26	1.47 TO 1.54
RECTENNA BORESIGHT DIA. (Km)	5.10	5.39 TO 5.68

FIGURE 3. PHASE REFERENCE SIGNAL DISTRIBUTION SYSTEM AND REFERENCE SIGNAL CONTROL LOOP





uniform aperture by means of a servo loop shown in the bottom part of Figure 3. For each subarray center location, a phase delay differential ("reference standard") is computed which occurs for the two generating frequencies f_{R1} and f_{R2} if the receiving antenna is located on a perfect plane. These delays can be calculated, and tuned in the lab to fractions of a degree. The output of the phase bridge then drives a phase shifter until the path delay differential equals that of the reference standard.

Since this circuit is used at every subarray, the subarray center points are electrically normalized to show $\phi = \phi_0$ constant across the entire array. This provides the conjugation circuit with the required reference phase.

3.2 RETRODIRECTIVE BEAM CONTROL

A retrodirective control circuit which compensates for pilot-generated beam shifts (without ionospheric effects) is the Chernoff circuit, with additional isolation added by (a) separating the pilot and power frequency paths, (b) using orthogonally polarized radiating elements; and (c) providing the remaining isolation in separate bandpass filters. The total required filter isolation is 70 dB, according to preliminary pilot system calculations.

This pilot system is predicated on $\sim$ 100 dBw pilot power. The proposed implementation of this pilot system consists of a circular array of low to medium-gain elements placed at the periphery of the rectenna, on top of utility poles if necessary to avoid interference from the power collection and transmission system.

The system provides vastly improved reliability over a single-dish, concentrated amplifier pilot system, and also provides such a wide power tube when the near-field beam enters the ionosphere that certain ionospheric effects will be mitigated. If ionospheric tests show that delay compensation through the ionosphere is required, a three-tone pilot system will be used as described in the Phase Control Session.

3.3 RF SIGNAL DISTRIBUTION SYSTEM

The current baseline distribution system for the conjugated RF signal is the same for both solid-state concepts.

Seven levels of corporate divisions provide equiphase feeding to the 16,384 elements in each 10m x 10m subarray.

The salient features of this distribution network are: weight of 0.67 million killograms for the total array using UT-47M; 250°C temperature capability; approximately 10dB ohmic loss (in addition to 42dB splitting loss). All layers of coax are pressed together behind the ground-plane, and very little thermal resistance is presented to the heat being radiated rearward from the ground-plane in the end-mounted concept, and toward the ground-plane (from the solar cells) in the sandwich concept. The composite heat transfer will be established by the spacing between the ground plane and the solar cells in the case of the sandwich.

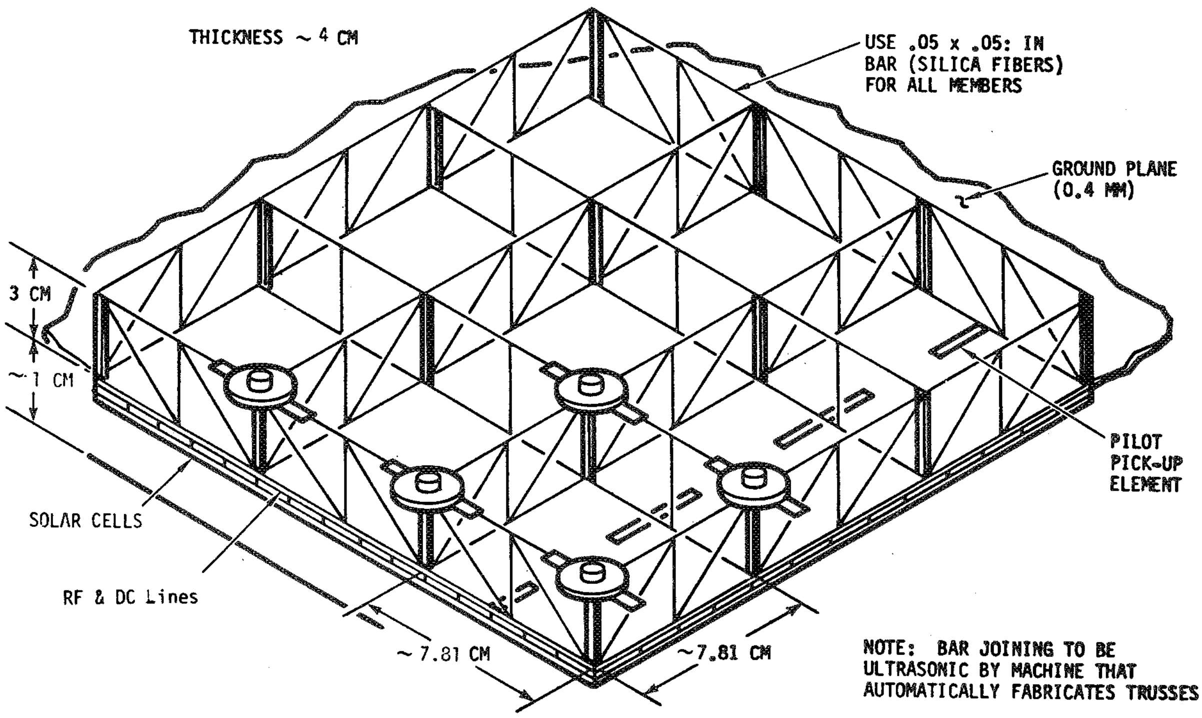
4.0 SOLID-STATE RADIATORS

A number of elements have been considered for the reference phase pick-up and pilot-tone pick-up elements: Helices; disc-on-rod antennas; yagis; dipole arrays; slot arrays; patch-type microstrip arrays; and arrays of various other strip-type radiators.

For the power radiators, all of the above array elements (except for high-gain end-fire arrays) have been considered but thin dipoles were selected because a) they lead to a minimum power requirement for the amplifier module; b) provide the necessary heat removal characteristics, and c) yield maximum reliability.

Figure 4 shows the dipole layout selected for the sandwich concept. The pilot pick-up slots are interspersed, but the power dipoles can be removed from this section if additional isolation is required, and/or space is required for the conjugation circuit.

FIGURE 4. SANDWICH ANTENNA WITH DIPOLES OVER GROUND PLANE



5.0 SOLID-STATE POWER AMPLIFIERS

The assessment of solid-state devices for r-f conversion in the SPS microwave power transmission system has included to date both an analytical effort and an amplifier development program.

5.1 Analytical Studies

The analytical study was carried out for Rockwell International at the University of Waterloo, Canada. The first phase of the study consisted of a computer simulation of bipolar transistors, in Class C and Class E type circuits. Both silicon and GaAs bipolar transistors were modelled. In the second part of the study, GaAs MESFETs were modelled in Class B and Class C circuits. Work is currently in progress to obtain Class E results.

The study was undertaken as an evaluation of transistors for the microwave space power system. The goal was the determination of transistor fabrication parameters suitable for power conversion efficiencies of at least 80% with power gains of at least 10 dB.

5.2 Bipolar Transistor Simulation

The simulation is carried out by using two basic programs. The first program generates a circuit model of the transistor, from inputs consisting of the impurity profile and lifetimes, plus geometry data. The second program is a circuit analysis program where the device model is incorporated into the desired external circuit. The results of the bipolar transistor analysis indicated that GaAs devices perform better at high temperatures with respect to efficiency than Si devices of similar geometrical parameters as shown in Figures 5 and 6. A comparison of Class C with Class E operation for the silicon transistor at 27^{o}C, shows that at high power levels (20 watts) the saturated Class-C mode gives the best results (Figure 7), while at lower power levels (10 watts) Class C gives better results at gains below 13 dB and Class E performs better at higher gains, (Figure 8).

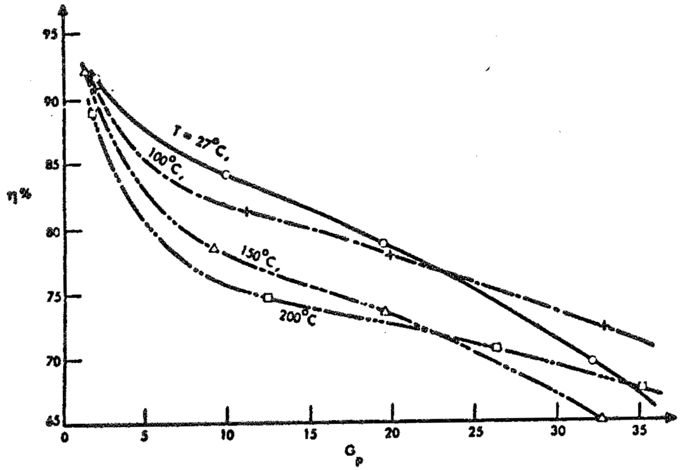


FIGURE 5. Results of High Temperature Study for the Silicon Transistor at 2.45 GHz

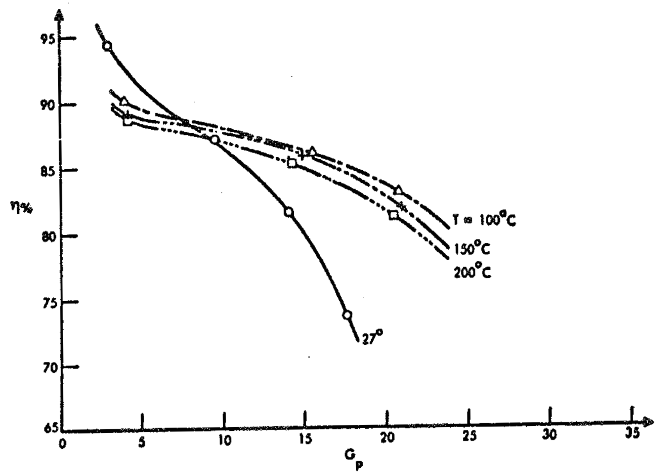


FIGURE 6. Results of High Temperature Study for the GaAs Transistor at 2.45 GHz

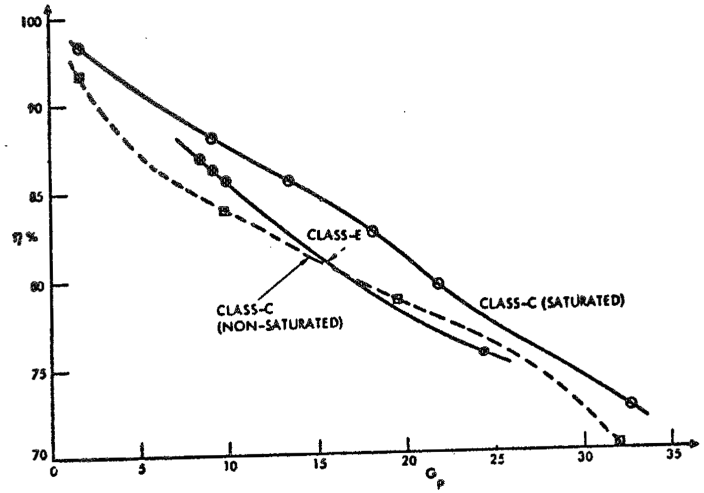


FIGURE 7. Efficiency vs Power Gain at 2.45 GHz and High Power Level for Silicon

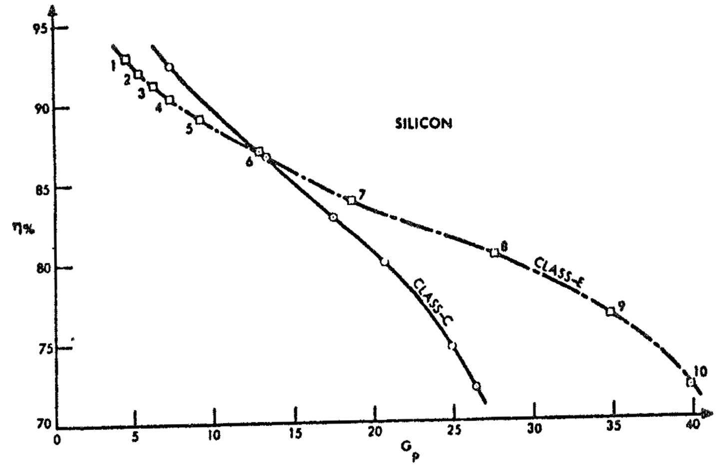


FIGURE 8. Efficiency vs Power Gain at 2.45 GHz and Low Power Level for Silicon

5.3 GaAs MESFETs Simulation

This study, currently in progress, follows the procedure used for the bipolar transistor simulation. A circuit model is generated by an appropriate program and is fed into the circuit analysis program. The devices modelled, so far, were basic one-cell structures, with low overall power output capability. The power output, power gain and efficiency obtained for the five structures modelled so far are shown in Figure 9. This figure shows plots of power added efficiency versus P_{out}/P_{max} for each device, where the three values shown correspond to conduction angles of 80^{o}, 120^{o} and 180^{o}. The dashed lines indicate a mode of operation which cannot be attained physically, because the gate source voltage exceeds the breakdown voltage for that transistor.

6.0 POWER AMPLIFIER DEVELOPMENT

The goal of the power amplifier development program is to demonstrate that efficient operation at a 5 to 10 watt power level can be achieved with off the shelf GaAs power FETs and to show that the performance can be improved with optimized devices of similar type. The high efficiency power amplifiers are being developed for Rockwell International by RCA and will be discussed in a subsequent presentation.

GaAs devices were selected because of data showing that GaAs performs better than silicon at the temperatures likely to be encountered in the SPS environment. Several transistor structures should be investigated to establish possible trade-offs with respect to power level, comparative efficiencies and reliability. Schottky barrier FETs are the first choice for testing at the experimental level in view of the high degree of activity in their development due to their use as power devices at microwave frequencies.

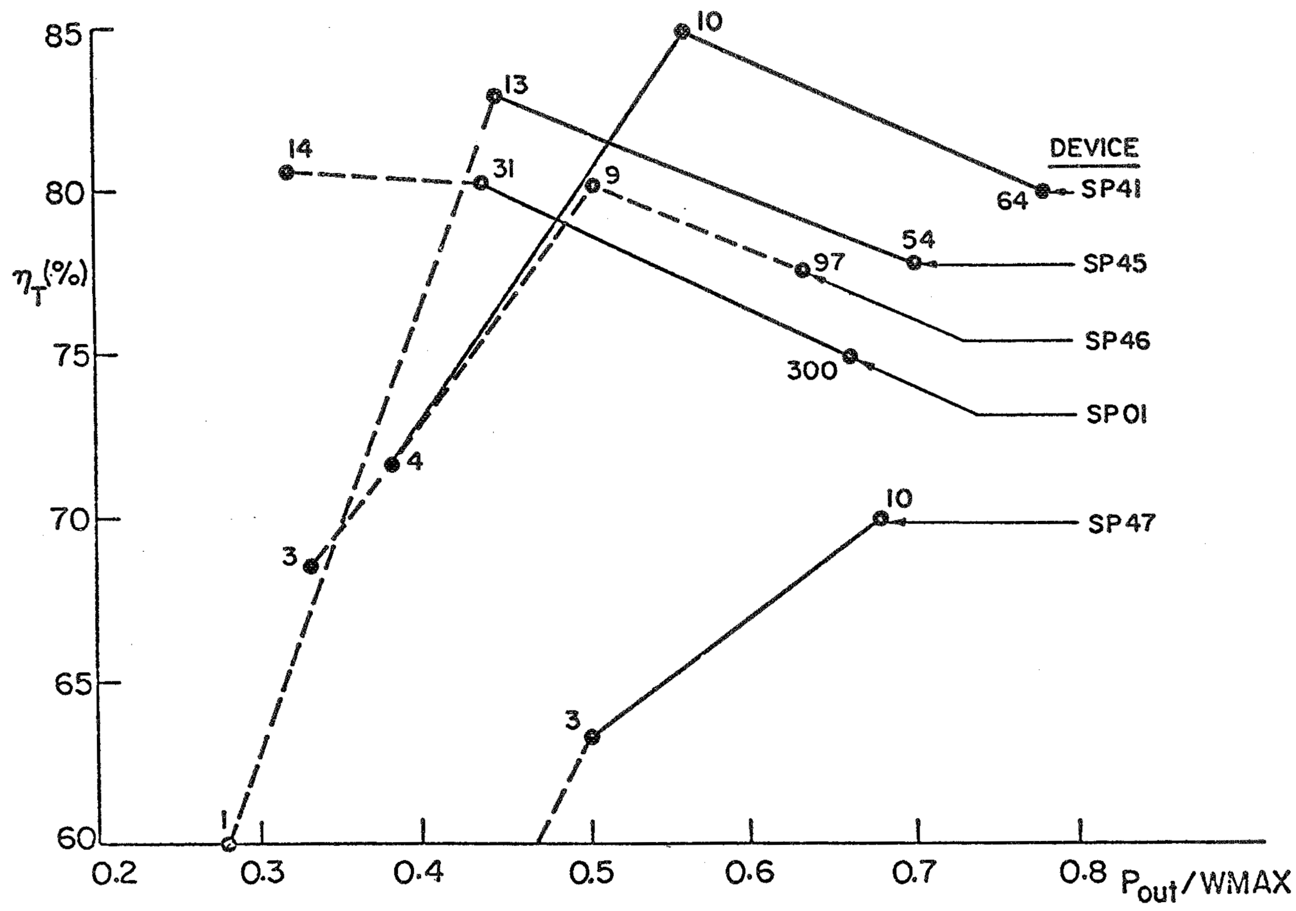


FIGURE 9. Total Efficiency vs (Output power/Wmax) for Sinusoidal Drive at 2.45 GHz for Five Different FETs. NOTE: The numbers indicate power gains.