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High-Efficiency Thin-Film GaAs Solar Cells

Phase II Final Report

Y. C. M. Yeh

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March 15, 1981

Prepared for
Solar Energy Research Institute
and
U.S. Department of Energy
Through an agreement with
National Aeronautics and Space Administration
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FOREWORD

This Final Report describes work performed for the Solar Energy Research Institute/Department of Energy under Contract No. XJ-9-8171-1 through an agreement with the National Aeronautics and Space Administration by the Advanced Photovoltaic Development Group, Solar Energy Conve sion Systems Section, JPL/California Institute of Technology, Pasadena, California 91109, during the period from July 1, 1979 to January 30, 1981.

ABSTRACT

This research demonstrates the feasibility of producing high-efficiency (15% or greater) thin-film gallium arsenide (GaAs) solar cells with costs suitable for terrestrial power generation by growing thin epi-GaAs films on suitably prepared low-cost substrates to replace the expensive single-crystal GaAs wafers used conventionally. These substrates are made of either recrystallized-Ge films previously deposited on metal substrates or epi-Ge films grown by chemical vapor deposition (CVD) on low-cost, low-grade single-crystal Si substrates.

For the first time, thin GaAs epi-layers with good crystallographic quality have been grown using a (100) Si-substrate on which a thin Ge epi-interlayer has first been grown by CVD from germane. Both anti-reflection coated metal oxide-semiconductor (AMOS) and n^+/p homojunction structures were studied. AMOS cells were fabricated on undoped-GaAs epi-layers deposited on bulk poly-Ge substrates using organo-metallic CVD film-growth, with the best achieved AM1 conversion efficiency being 9.1%. Both p-type and n^+-type GaAs growth have been optimized using 50 ppm dimethyl zinc and 1% hydrogen sulfide, respectively. A new direct GaAs deposition method in fabricating ultra-thin top layer, epitaxial n^+/p shallow homojunction solar cells on (100) GaAs substrates (without anodic thinning) was developed to produce large area (1 cm^2) cells, with 19.4% AM1 conversion efficiency achieved. Additional, an AM1 conversion efficiency of 18.4% (17.5% with 5% grid coverage) was achieved for a single-crystal GaAs n^+/p cell grown by OM-CVD on a Ge wafer.

CONTENTS

I. INTRODUCTION.....1-1

II. POLYCRYSTALLINE GaAs SOLAR CELLS.....2-1

A. AMOS CELLS ON BULK POLYCRYSTALLINE Ge SUBSTRATES.....2-1

B. HOMOJUNCTION POLYCRYSTALLINE CELLS.....2-12

III. SINGLE-CRYSTAL OM-CVD GROWN GaAs JUNCTION SOLAR CELLS.....3-1

A. GaAs GROWTH.....3-1
1. p-type GaAs Growth.....3-1
2. Highly-Doped n-type GaAs Growth.....3-6

B. OHMIC-CONTACT EVALUATION.....3-10
1. Vacuum-Deposited Ohmic Contact.....3-10
2. Electro-plated Ohmic Contact.....3-14

C. SINGLE-CRYSTAL n^+/p SHALLOW HOMOJUNCTION CELLS ON GaAs.....3-17

D. SINGLE-CRYSTAL n^+/p SHALLOW HOMOJUNCTION CELLS ON Ge.....3-37

IV. LOW-COST SUBSTRATE.....4-1

A. RECRYSTALLIZED Ge ON TUNGSTEN (W).....4-1
1. Ge Growth on W Substrates.....4-1
2. Electron-Beam Recrystallization of Ge/W.....4-2

B. Ge EPI-INTERLAYER ON SINGLE-CRYSTAL Si.....4-7
1. Ge Epi-interlayer Growth on Si substrates.....4-8
2. Pulsed Laser Annealing of Ge/Si.....4-16
3. GaAs/Ge Epi-interlayer/Si.....4-26

REFERENCES.....R-1

FIGURES

2-1. Light I-V characteristics of 700°C growth GaAs thin-film AMOS solar cells on bulk poly-Ge substrates.....2-4

2-2. Dark forward I-V characteristics of the best (700°C growth) AMOS GaAs/poly-Ge solar cell.....2-6

2-3. Light I-V characteristics of the best (625°C growth) AMOS GaAs/poly-Ge solar cell.....2-7

2-4. Dark forward I-V characteristics of the cell shown in Fig. 2-3.....2-8

2-5. Capacitance-voltage relationship of the cell shown in Fig. 2-3.....2-9

2-6. SEM photomicrograph of the AR-coated sample shown in Fig. 2-3.....2-10

3-1. Temperature dependence of hole concentration for OM-CVD p-GaAs.....3-3

3-2. Temperature dependence of resistivity for OM-CVD p-GaAs.....3-4

3-3. Temperature dependence of Hall mobility for OM-CVD p-GaAs.....3-5

3-4. Dependence of Hall mobility on hole concentration at room temperature for OM-CVD p-GaAs.....3-7

3-5. Dependence of resistivity on hole concentration at room temperature for OM-CVD p-GaAs.....3-8

3-6. Dependence of room-temperature hole concentration on dimethylzinc (DMZ) mole fraction for p-GaAs films grown by OM-CVD at 700°C and 725°C.....3-9

3-7. Dependence of room-temperature electron concentration on H_2S mole fraction for n^+-GaAs films grown by OM-CVD.....3-11

3-8. Dependence of Hall mobility on electron concentration at room temperature for OM-CVD n^+-GaAs.....3-12

3-9. Mesa-etch photomask for Hall and C-V measurements as well as contact-resistance evaluation.....3-15

3-10. Contact resistance test pattern.....3-16

3-11. A photomicrograph of the contact resistance pattern made on an n^+/p structure.....3-18

FIGURES (Continued)

3-12. The front contact grid design for 1 cm x 1 cm n^+/p solar cell....3-20

3-13. Dark forward I-V characteristics of a small-area n^+/p diode....3-22

3-14. Simulated light I-V characteristics of the same n^+/p GaAs junction used in the previous figure....3-24

3-15. SIMS depth profile of an $n^+/p/p^+$ structure on (100) GaAs substrate (purchased from Morgan Semiconductors)....3-27

3-16. SIMS depth profile of an $n^+/p/p^+$ structure on (100) GaAs substrate (purchased from Crystal Specialites)....3-28

3-17. Light I-V characteristics of a 1 cm x 1 cm area n^+/p GaAs/GaAs solar cell....3-31

3-18. Dark I-V characteristics of the same solar cell used in obtaining the curve of Fig. 3-17....3-32

3-19. Light I-V characteristics of a small (2.36 mm^2 active area) n^+/p GaAs/GaAs solar cell made by the sequential anodization-etching technique....3-34

3-20. Dark I-V characteristics of the solar cell used for obtaining the curve in Fig. 3-19....3-35

3-21. Light I-V characteristics of a large area (1.0 cm^2) n^+/p GaAs/GaAs solar cell made by the direct deposition method without anodic thinning (see text)....3-38

3-22. Photomicrograph of the GaAs/Ge surface with CP4 etch prior to GaAs growth....3-40

3-23. Photomicrograph of the GaAs/Ge surface with HCl in-situ etch prior to GaAs growth....3-41

3-24. Photomicrograph of the GaAs/Ge surface with $HF:HNO_3:H_2O_2:CH_3COOH$ = 9:4:4:20 etch prior to GaAs growth....3-42

3-25. Light I-V characteristics of an n^+/p GaAs/Ge solar cell....3-44

3-26. Dark I-V characteristics of the solar cell used for obtaining the curve in Fig. 3-25....3-45

FIGURES (Continued)

4-1. Photomicrographs of typical Ge films CVD-grown at 800°C.....4-3

4-2. Chemical vapor deposition system for growth of Si or Ge interlayer.....4-4

4-3. Dependence of sample-holder temperature on heater current.....4-6

4-4. SEM photomicrograph at 2000X of a Ge film grown by CVD on (111) Si at 657°C with H_2 carrier gas.....4-10

4-5. SEM photomicrograph at 6000X of the same Ge films as used for Figure 4-4.....4-11

4-6. Laue back-reflection photograph of the same film as used for Fig. 4-4.....4-12

4-7. Typical X-ray diffraction chart obtained on a Ge/Si sample grown at 700°C in H_2 carrier.....4-14

4-8. X-ray diffraction chart with high angular-resolution and low sensitivity obtained on the same sample used in Fig. 4-7.....4-15

4-9. SEM photomicrograph (2700X) of a typical Ge film grown at 700°C on (100) Si substrate.....4-17

4-10. SEM photomicrograph (7000X) of a Ge/Si sample annealed at an average energy-density of about 0.34 J cm^{-2} (Ge film grown at 700°C).....4-24

4-11. SEM photomicrograph (7000X) of a Ge/Si sample annealed at an average energy-density of about 0.49 J cm^{-2} (Ge film grown at 700°C).....4-25

4-12. SEM photomicrograph (2700X) of a Ge/Si sample annealed at an average energy-density of about 0.64 J cm^{-2} (Ge film grown at 700°C).....4-27

4-13. X-ray diffraction chart of the annealed Ge/Si substrate.....4-28

4-14. X-ray diffraction chart of an epi-GaAs/epi-GE/Si sample.....4-30

4-15. SEM photomicrograph (10,000X) of the cleaved cross-section of the GaAs/Ge/Si structure.....4-31

4-16. SEM photomicrograph (2700X) of the GaAs/Ge/Si sample.....4-32

SECTION I

INTRODUCTION

The use of GaAs as the semiconductor material in photovoltaic devices is widely recognized as one of the expected means for obtaining high efficiencies with thin-film solar cells. This is partially due to its high light absorption and good match to the solar spectrum. Also, high efficiencies are to be expected because the barriers used in GaAs, such as shallow n^+/p homojunctions and Ga(Al)As heteroface p/n junctions are reasonably stable at normal operating temperatures and do not have the problems of many heterojunctions. Such problems, except for the InP/CdS configuration, arise from lattice parameter and electron affinity mismatch between the two components of the heterojunction. These, in turn, can cause high interface recombination state densities and unwanted barriers in the conduction bands, respectively, leading to reduced open-circuit voltages (V_{OC}) and fill factors (FF).

The overall objective of this research is to demonstrate the feasibility of producing high-efficiency (15% or greater) thin-film GaAs solar cells at a cost reasonable for terrestrial solar electric power generation (under $0.70 per peak Watt in 1980 dollars). To fulfill this objective, a research and development effort on GaAS solar cells was initially directed towards the goals of demonstrating that 1) high-efficiency shallow-homojunction solar cells can be fabricated by organo-metallic chemical vapor deposition (OM-CVD); 2) high-efficiency AMOS or shallow-homojunction solar cells can be fabricated on polycrystalline Ge substrates; 3) fabricating and evaluating recrystallized Ge films on tungsten metal should be conducted as a preliminary investigation

directed toward development of a low-cost substrate for thin-film GaAs solar cells. Progress towards goal 1 during this reporting period is discussed in Section III, and, progress towards goal 2 and 3 are discussed in Sections II and IV.A., respectively. Due to the difficulty encountered in achieving good efficiency for GaAs solar cells made on polycrystalline Ge substrates, a new approach utilizing single-crystal Si as the low-cost substrate to circumvent the problems associated with a polycrystalline substrate was pursued. Hence, a new goal was adopted, goal 4, to demonstrate that hetero-epitaxial Ge interlayers on single-crystal Si substrates can be fabricated which are suitable for use as low-cost substrates for thin-film epitaxial GaAs solar cells. Progress towards goal 4 is discussed in Section IV.B.

SECTION II

POLYCRYSTALLINE GaAs SOLAR CELLS

The technical approach of this program is based on the use of a recrystallized Ge film previously deposited on a surface passivating layer covering a low-cost metal sheet, all serving to replace an expensive bulk GaAs wafer as the substrate for subsequent epitaxial growth of a thin-film GaAs layer. To prepare a low-cost solar cell using this thin film technology, either an AMOS or a homojunction structure could be made. Recently, however, a more promising approach capable of high efficiency is being developed, involving the growth of an epitaxial single-crystal GaAs thin-film solar cell on a Ge epi-interlayer on a single-crystal Si substrate. This approach and the status of the work involved will be discussed below in Section IV.

A. AMOS CELLS ON BULK POLYCRYSTALLINE Ge SUBSTRATES

Although a p/n junction as a poly-GaAs thin film solar cell may offer better long-term stability and higher potential efficiency than a corresponding Schottky barrier cell, the fabrication of such a successful junction has not yet been demonstrated. Hence the AMOS structure, which has reasonable stability at room temperature when formed on a single-crystal substrate, was studied experimentally as a potentially viable alternative for low-cost polycrystalline thin-film GaAs solar cells.

To circumvent problems with diffusion of metal atoms into the Ge film during its recrystallization, such as reported previously, AMOS cells were first fabricated on GaAs deposited on bulk poly-Ge substrates. This permitted an

investigation of the possible role of doping effects on the GaAs by Ge arising from grain boundaries in the substrate, as well as the role of the OM-CVD poly-GaAs grain boundaries on Schottky barrier-type solar cells.

AMOS solar cells were fabricated on undoped poly-GaAs layers using OM-CVD film-growth temperature from 610° to 700°C, As/Ga mole ratios from 4 to 11, and a constant H_2 flow rate of 3 liters/min. In order to study the uniformity of solar cell performance within the 1.2 cm x 1.2 cm wafer area, a number of 1-mm and 5-mm diameter circular cell arrays were made on each wafer. A definite improvement in solar cell performance with decreasing As/Ga mole ratios was observed. The best performance was found for GaAs films grown using an As/Ga mole ratio of 4 at growth temperatures of 610°-625°C. As the As/Ga mole ratio was increased, a progressively higher leakage current was evidenced by lower open-circuit voltage (V_{OC}) and fill factor (FF) values. This leakage was caused by an excessively high doping concentration (indicated by C-V measurements) and/or higher defect densities near the grain boundary regions, causing reduced barrier heights and increased thermionic field emission effects upon the diode current.

With an As/Ga ratio of 4, the effective doping concentration (measured by the C-V method) increased from 7×10^{15} to 1×10^{17} cm^{-3} as the growth temperature increased from 610° to 700°C. At a growth temperature of 700°C and an As/Ga ratio of 4, the doping concentration for GaAs films grown on single-crystal GaAs substrates in our reactor was always under 1×10^{15} cm^{-3}. Therefore, the 1×10^{17} cm^{-3} doping concentration observed for GaAs grown on the poly-Ge substrates must have been due to auto-doping from the Ge substrate. The auto-doping is probably also responsible for the high leakage currents observed for AMOS solar cells made on GaAs thin-films grown at temperatures higher than 625°C on poly-Ge substrates. The probable cause for this auto-doping was

preferential diffusion of Ge along grain boundaries and/or the introduction of inadvertent gaseous products into the OM-CVD gas mixture by its interaction with the bulk poly-Ge substrate. Subsequently, an experiment was conducted to test this hypothesis. In different trials using a 700°C growth temperature and an As/Ga ratio of 4, single-crystal GaAs test samples were placed surrounding either a bulk poly-Ge wafer or a single-crystal GaAs wafer. Analysis of C-V measurements on the various test samples showed that the effective doping concentration of the epi-GaAs films on either GaAs or bulk poly-Ge wafers was about 1×10^{17} cm^{-3} when they were placed near each other during the same growth experiment. On the other hand, the doping concentration was less than 1×10^{15} cm^{-3} for those GaAs test samples surrounding the single-crystal GaAs wafer during the GaAs growth. This experimental observation unambiguously indicates that there are significant amounts of auto-doping originating from the CVD gas mixture on account of its interaction with the bulk poly-Ge substrate. Hence, the lower the growth temperature, the less was the effect of auto-doping. Unfortunately, for OM-CVD growth at atmospheric pressure, the lower bound of the growth temperature for epitaxy on poly-GaAs was found to be approximately 600°C. For growth temperatures below 600°C, non-epitaxial growth with a matte surface occurred, leading to very low short-circuit current density and poor energy conversion efficiency for the AMOS cells. Curves 1 and 2 of Fig. 2-1 represent the light I-V data of the best solar cell and of a typical cell, respectively, using 700°C GaAs growth temperature. The observed low open-circuit voltage (about 0.25 V) and nearly linear light I-V characteristics (Curve 2 of Fig. 2-1) indicate that a high-leakage shunt is responsible for the poor photovoltaic response of the typical 700°C-grown GaAs solar cell. Even for the best cell, the open-circuit voltage is low (about 0.51 V),

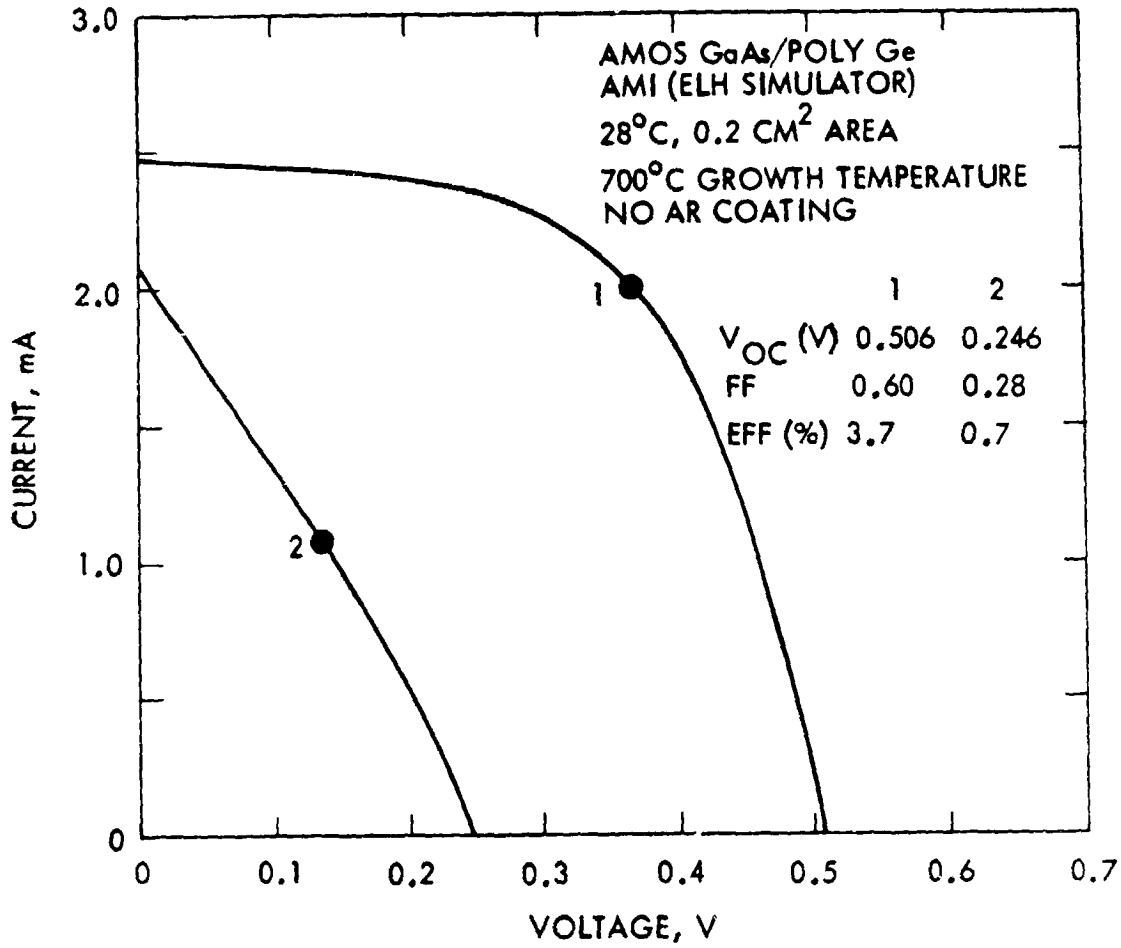


FIG. 2-1. Light I-V characteristics of 700°C growth GaAs thin-film AMOS solar cells on bulk poly-Ge substrates.

as shown in Curve 1 of Fig. 2-1. Figure 2-2 shows the dark forward I-V characteristic of the solar cell as shown in Curve 1 of Fig. 2-1. The low open-circuit voltage for this sample apparently arises from excessive diode current due to recombination at the interface or at grain boundaries within the depletion region leading to high reverse saturation current densities in the sample.

At lower growth temperatures (610°-625°C), a considerable reduction in the leakage current was indicated by the observation of higher open-circuit voltages nearly reaching 0.7 V. The highest conversion efficiency observed was about 7% for a 0.2 cm^2 AMOS cell made without AR coating on a poly-Ge substrate at 625°C GaAs growth temperature. The light I-V characteristic for this cell is shown as Curve 2 in Fig. 2-3. A solar AM1 conversion efficiency of 11% is expected for this cell after AR coating. However, after the AR coating was applied, an AM1 conversion efficiency of only 9.1% was calculated from the light I-V characteristic, shown as Curve 1 in Fig. 2-3. The reason for the lower observed conversion efficiency is the lower observed FF value of the AR-coated solar cell (0.52 instead of 0.64). This was due to problems associated with contacting the back side of the substrate.

The dark forward I-V curve, the C-V characteristics and a SEM photomicrograph for the sample are shown in Figs. 2-4, 2-5 and 2-6, respectively. The near-exponential dependence of diode current on voltage in the current range from 10^{-7} to 10^{-4} A for the 625°C growth GaAs cell indicates that the high leakage encountered in 700°C growth is no longer the major problem. However, the high value for the diode factor, n and the concomitant high saturation current compared to AMOS cells fabricated on single-crystal wafers show that the grain boundaries do locally affect the Schottky barrier interface states, even for AMOS-treated GaAs surfaces. This effect was not observed for AMOS

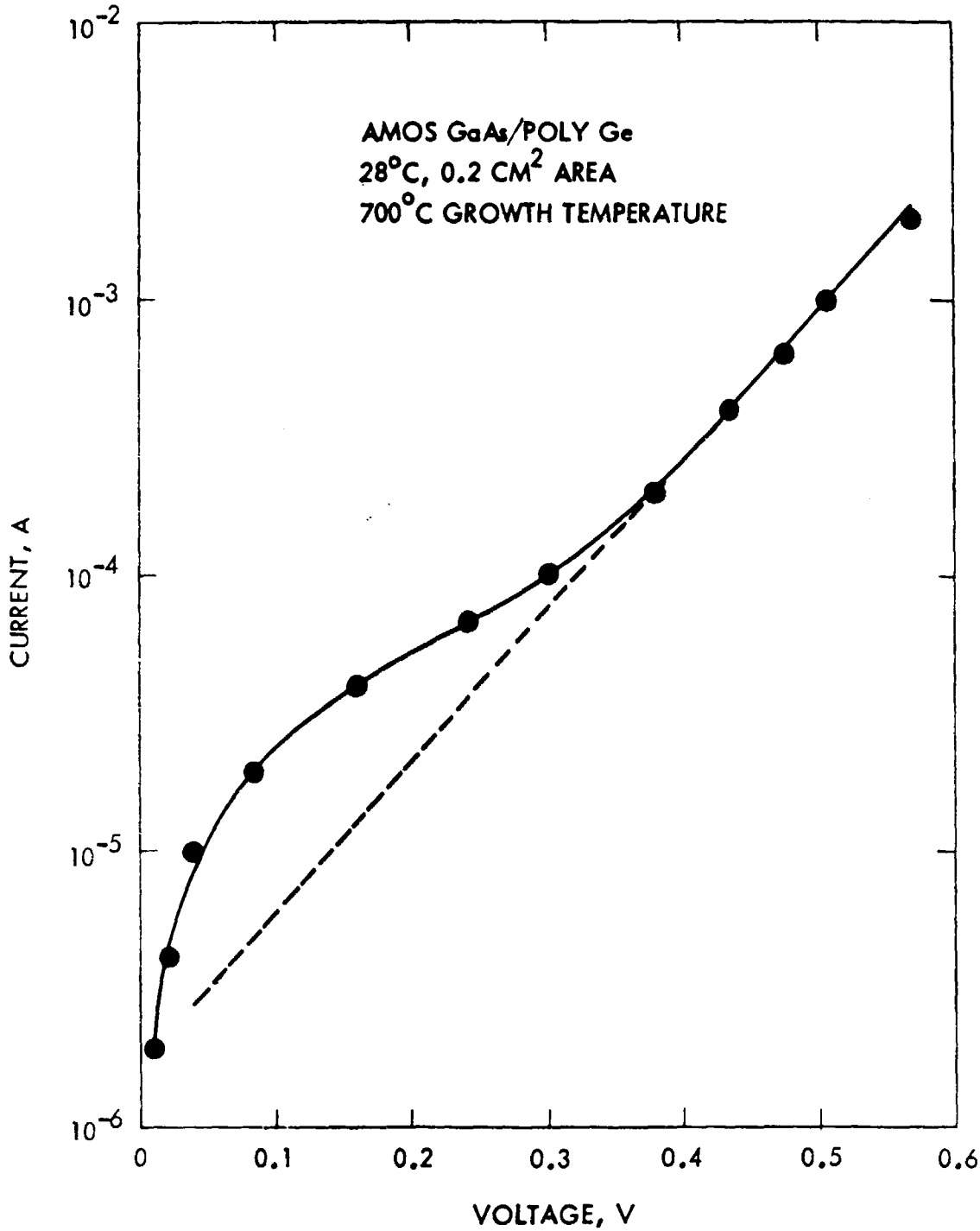


FIG. 2-2. Dark forward I-V characteristics of the best (700°C growth) AMOS GaAs/poly-Ge solar cell.

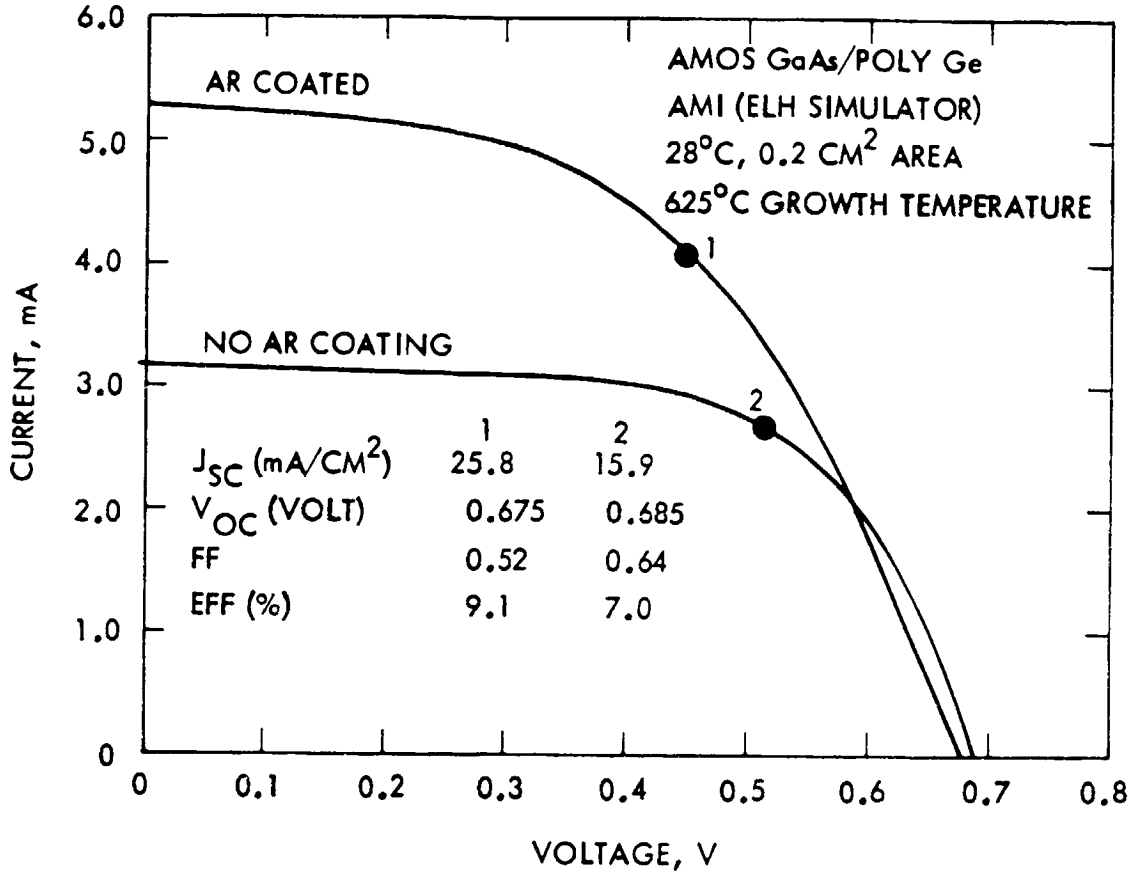


FIG. 2-3. Light I-V characteristics of the best (625°C growth) AMOS GaAs/poly-Ge solar cell.

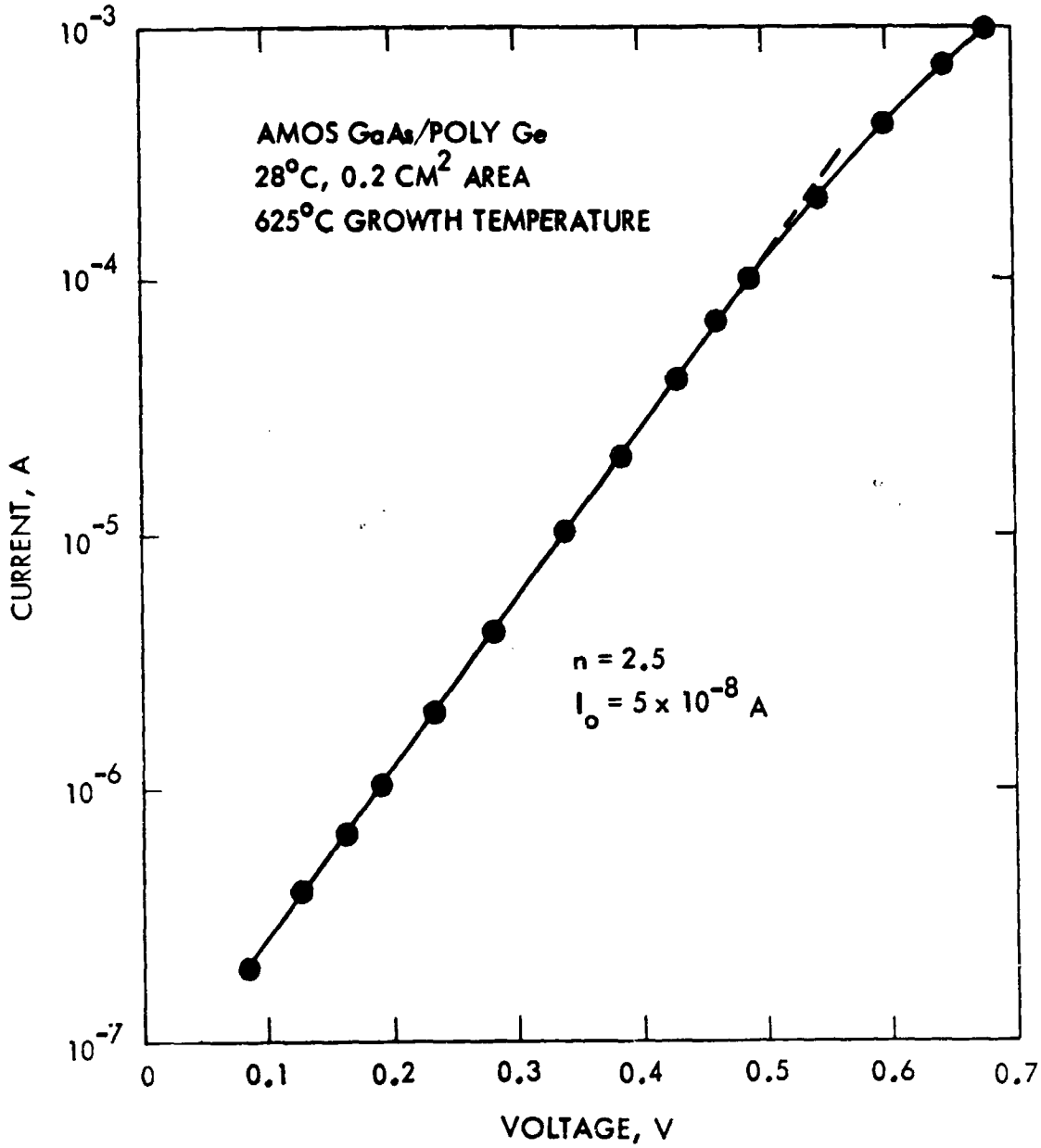


FIG. 2-4. Dark forward I-V characteristics of the cell shown in Fig. 2-3.

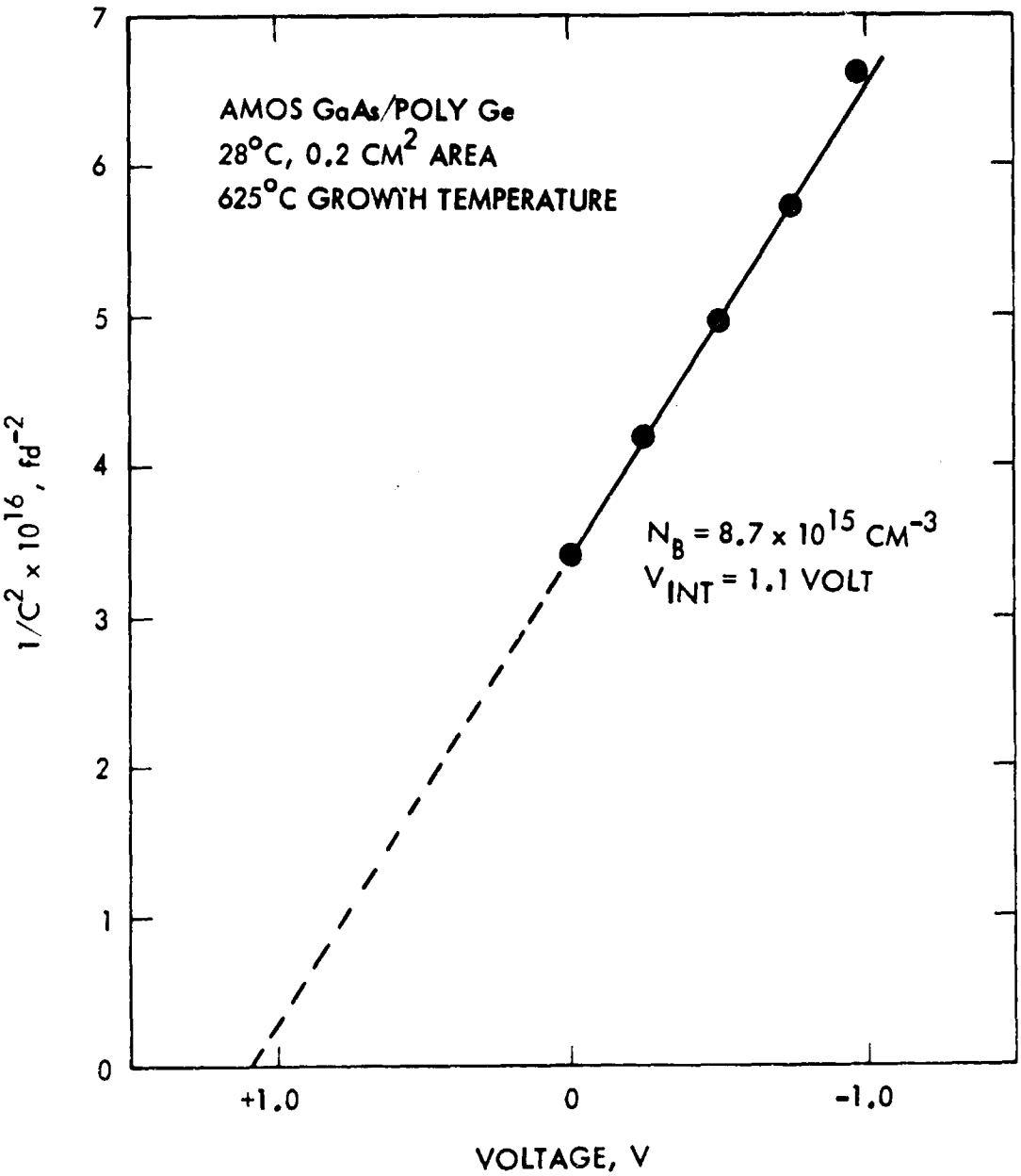
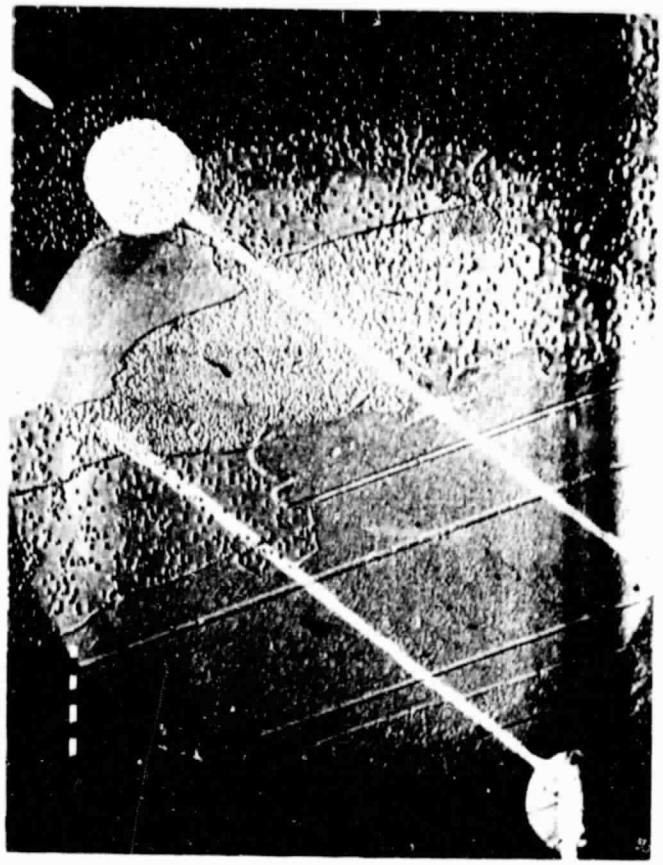


FIG. 2-5. Capacitance-voltage relationship of the cell shown in Fig. 2-3.



0.5 mm

FIG. 2-6. SEM photomicrograph of the AR-coated sample shown in Fig. 2-3.

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cells on sliced poly-GaAs wafers obtained from ingots grown from the melt, for which efficiencies of about 14-16% were obtained (Ref. 2-1). Evidently, the properties of grain boundaries in GaAs deposited from the vapor behave differently with respect to their effect on metal-semiconductor contacts. Thus, even with large grain sizes such as found on these sliced poly-Ge wafers or as obtained by deposition on recrystallized Ge films, the relatively small areas associated with the regions at the grain boundaries do seriously degrade the overall cell performance. This is because of the exponential dependence of diode current on barrier height and because of the likelihood that a considerable number of interface states in the grain boundary regions contribute to large recombination currents. The poor values of FF and V_{oc} observed by other researchers on GaAs films deposited by various techniques and on various substrates are probably also related to these phenomena.

The doping concentration of the low growth-temperature cell was calculated from the slope of the C-V characteristic curve (shown in Fig. 2-5) to be 8.7×10^{15} cm^{-3}. This is a desirable doping concentration for GaAs AMOS solar cells. A SEM photomicrograph of the AR-coated sample, using a Robinson collector attachment for backscattered primary electrons, is shown in Fig. 2-6. The bright lines with small circles attached are 2000 Å silver electrodes for electrical contacts. The large, faint circle indicates the area of the solar cell coated with 590 Å-thick Sb_2O_3 AR coating. The slightly smaller circle (5-mm dia.) inside the large circle indicates the 60 Å-thick silver area of the AMOS GaAs/poly-Ge solar cell. The crystalline structure of the poly-Ge substrate is composed of elongated crystal grains with crystallite size of 0.2-1 mm in the narrow direction (see Fig. 2-6). The speckled pattern is due to etch pits formed during GaAs etching prior to AMOS processing.

AMOS solar cells were also fabricated on GaAs grown on laser-recrystallized Ge which had been e-beam deposited on tungsten sheet or tungsten-coated steel substrates. The best efficiency found for the small-area AMOS thin-film solar cell was 4.8% (8% with AR coating), as previously reported (Ref.2-2). Once again, the main reason for the low efficiency was the low cell output voltage.

B. HOMOJUNCTION POLYCRYSTALLINE CELLS

Since low conversion efficiencies arising from low V_{OC} values were consistently observed for AMOS cells made on GaAs/poly-Ge substrates, an investigation of homojunction GaAs structures on low-cost poly-Ge substrates was deemed necessary. However, before fabricating such structures on poly-crystalline Ge substrates, a study of OM-CVD grown shallow homojunction structures on single-crystal GaAs and single-crystal Ge substrates was made. The procedures and results are described in the next section.

SECTION III

SINGLE-CRYSTAL OM-CVD GROWN GaAs JUNCTION SOLAR CELLS

The technical approach of this program is based on the use of epitaxial GaAs thin-films on suitably prepared low-cost single-crystal substrates to replace the expensive bulk GaAs wafer. In due course, producing high-efficiency GaAs thin-film solar cells requires epitaxial growth of GaAs n/p junctions with appropriate additional solar-cell-making procedures.

Although successful growth of thin-film n^+/p homojunction GaAs structures by CVD using halide transport of Ga (Ref. 3-1) has been demonstrated, growth of high-efficiency GaAs cells with similar structure by OM-CVD techniques has not been established. The use of OM-CVD is preferred over hydride- or halide-CVD, because: (1) there is no excessive etching of the low-cost Si substrates or the interlayer by HCl, (2) the growth temperature can be lower with correspondingly lowered auto-doping by diffusion and less detrimental effects because of thermal-expansion mismatch between the GaAs film and substrate, and (3) the use of a single-temperature zone and a cold-wall reactor should ultimately allow for future scale-up and the achievement of low-cost fabrication.

A. GaAs GROWTH

1. p-type GaAs Growth

Previously, an OM-CVD facility for undoped or lightly doped n-type GaAs (doping concentration less than 10^{17} cm^{-3}) epitaxial thin-film growth on poly-Ge substrates was established. For fabricating the epitaxial GaAs homojunction solar cell structure, the OM-CVD reactor was modified to accommodate additional dopant lines for both n^+- and p-type dopants. Optimization of p-type GaAs growth using 50 ppm dimethyl zinc (DMZ) as doping gas was completed.

Hole concentrations ranging from 2×10^{17} to 3×10^{18} cm^{-3} were consistently achieved using growth temperatures of 700-725°C, DMZ mole fractions (MF) from 8×10^{-7} to 6×10^{-6}, a growth rate of 0.17 micrometer/min, arsine (AsH_3) MF of 1.6×10^{-3}, trimethyl gallium (TMG) MF of 4×10^{-4}, and H_2 flow rate of 3000 cc/min. Although a room-temperature hole concentration as low as 6×10^{16} cm^{-3} can be achieved with a low MF of DMZ, the reproducibility was poor. The inability to achieve well-controlled low-doping at a low MF of DMZ is possibly due to the loss of DMZ by adsorption on the walls of the tubing or reactor, and/or loss by hydrolysis with the residual moisture in the system.

The characterization of the p-type GaAs film growth was achieved by employing van der Pauw measurements on p-type films grown on (100)-oriented Cr-doped semi-insulating GaAs substrates. The dependences of hole concentration (p), resistivity (ρ), and Hall mobility (μ_H) as a function of measurement temperature for several representative samples are displayed in Figs. 3-1, 3-2 and 3-3, respectively. Clearly, even for samples doped as low as the high 10^{17} cm^{-3} range, the hole-concentration data show impurity conduction effects as indicated by the absence of appreciable carrier freeze-out. Figure 3-2 shows that the dependence of resistivity on temperature gradually decreases as the doping concentration of DMZ increases. For the highest-doped sample (MF of DMZ = 6×10^{-6}, room-temperature hole concentration $p_0 = 3.5 \times 10^{18}$ cm^{-3}), the temperature dependence of ρ is reduced significantly. Using optical techniques, Queisser and Panish (Ref. 3-2) reported the merging of the acceptor level with the valence bands at a hole concentration of about 2×10^{18} cm^{-3}, near the doping level in our highest-doped sample. The critical acceptor concentration, N_{cr}, at which the impurity conduction becomes "free" (zero activation energy), is given by (Ref. 3-3) $N_{cr} = (0.25/A_{Zn})^3$, where A_{Zn} given by $q^2/(\varepsilon \times \Delta E)$

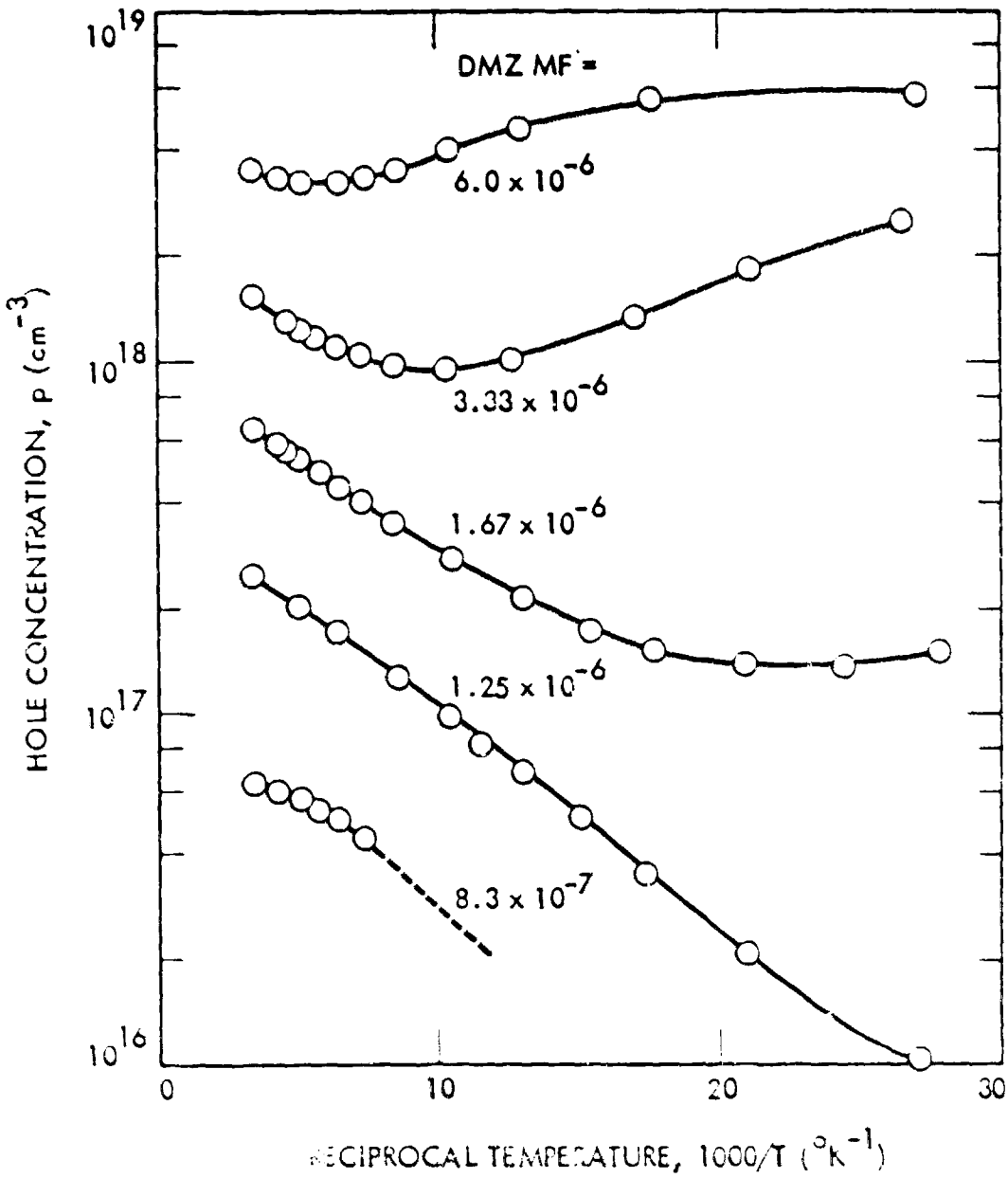

FIG. 3-1. Temperature dependence of hole concentration for UM-CVD p-GaAs.

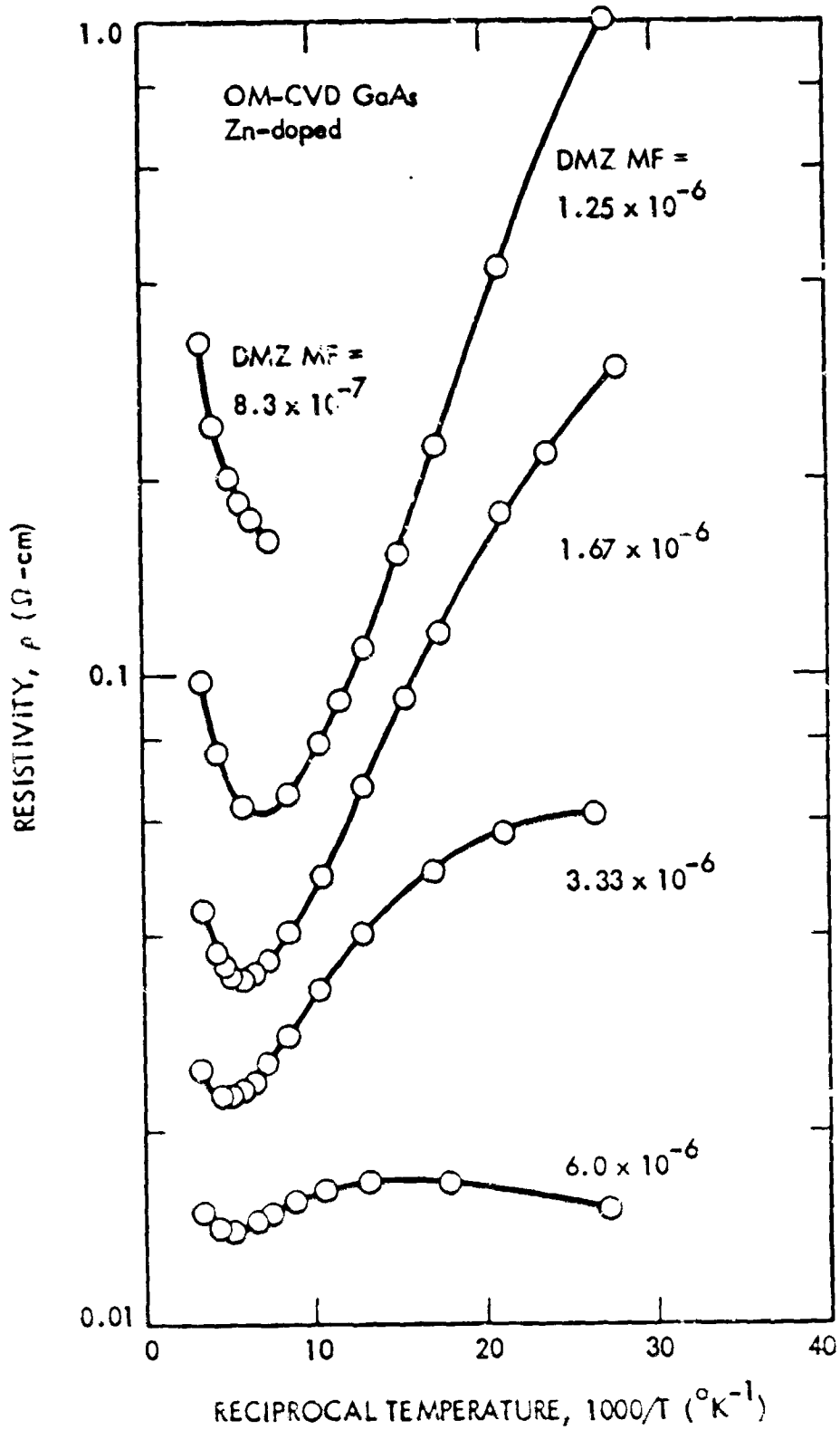

FIG. 3-2. Temperature dependence of resistivity for OM-CVD p-GaAs.

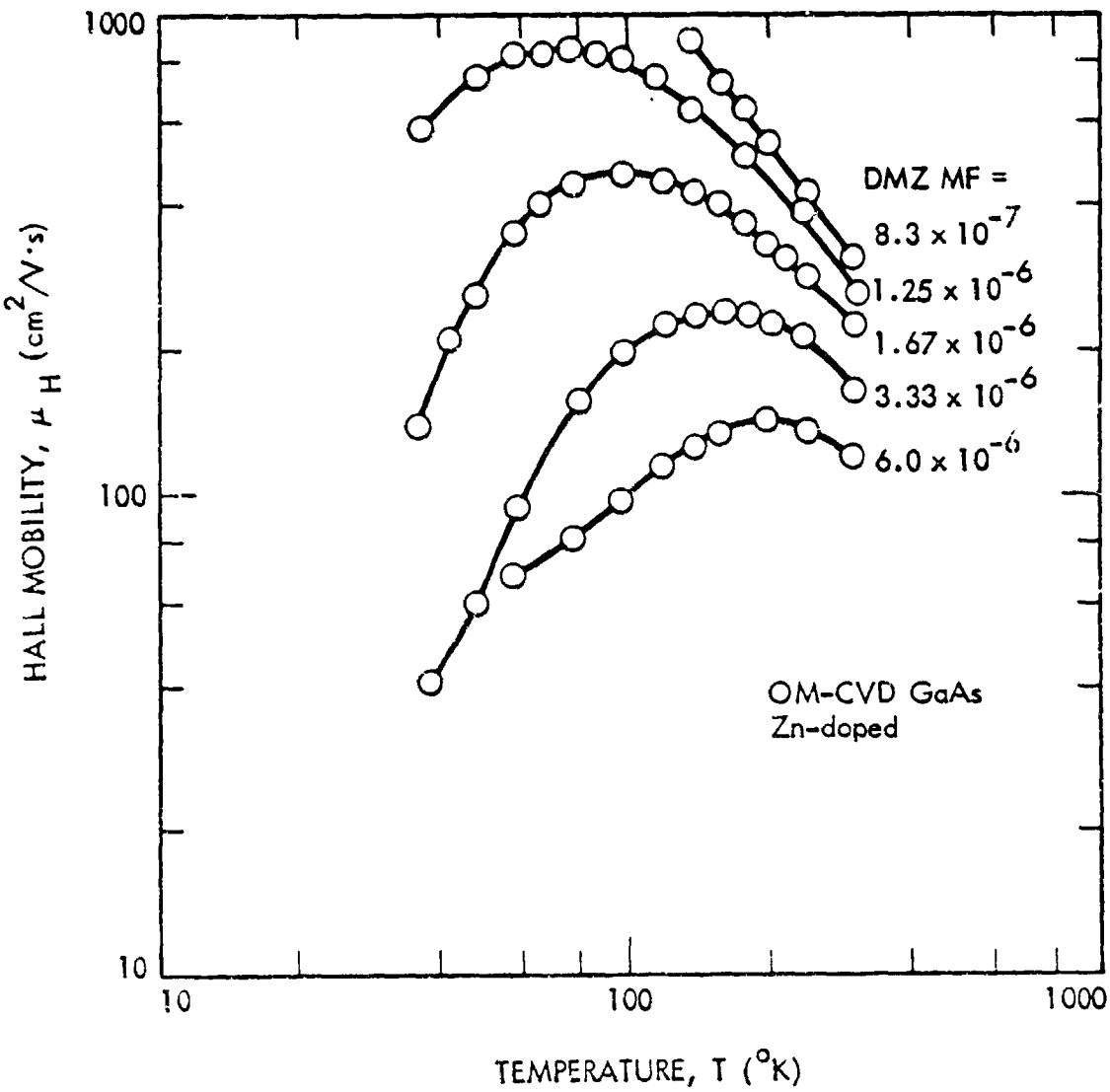

FIG. 3-3. Temperature dependence of Hall mobility for OM-CVD p-GaAs.

is the radius of the hole orbit around the Zn acceptor. With the static dielectric constant of 12.8 and the binding energy E of 30.7 meV for the hole on Z_n in GaAs (Ref. 3-4), the value for N_{cr} of 2.53×10^{18} cm^{-3} is obtained.

The room-temperature Hall mobility as a function of hole concentration is shown in Fig. 3-4. For comparison, data reported in the literature are also included here. The solid line is calculated (Ref. 3-5) from the Brooks-Herring formula with an assumed value of 400 $cm^2V^{-1}s^{-1}$ for the lattice-limited mobility. The experimental result of Sze and Irvin (Ref. 3-6) is also included -- indicated by a broken line. For a given hole concentration, the mobility we obtained is comparable to or higher than that reported by others, indicating good sample quality for the OM-CVD GaAs films grown during this contract period.

The room-temperature bulk resistivity as a function of hole concentration for the present Zn-doped OM-CVD GaAs is shown in Fig. 3-5, along with data obtained by Sze and Irvin (Ref. 3-6). For completeness, the functional dependences of room-temperature hole concentration (p) on the MF of DMZ at 700°C and 725°C growth temperatures are shown in Fig. 3-6. It should be pointed out that no doping-saturation effect was observed up to the highest doping concentration (3×10^{18} cm^{-3}) in our experiments. This was expected because the solubility limit of Zn in GaAs is higher than 10^{20} cm^{-3}. The inability to achieve a consistent doping concentration at a low MF of DMZ is clearly shown, as discussed previously.

2. Highly Doped n-type GaAs Growth

The investigation of a low-doped, n-type OM-CVD GaAs, using 10 ppm H_2S doping gas, was reported at the 7th International Conference on Chemical Vapor Deposition held during the Electrochemical Society Meeting in October 1979. Hence, no further discussion will be given here.

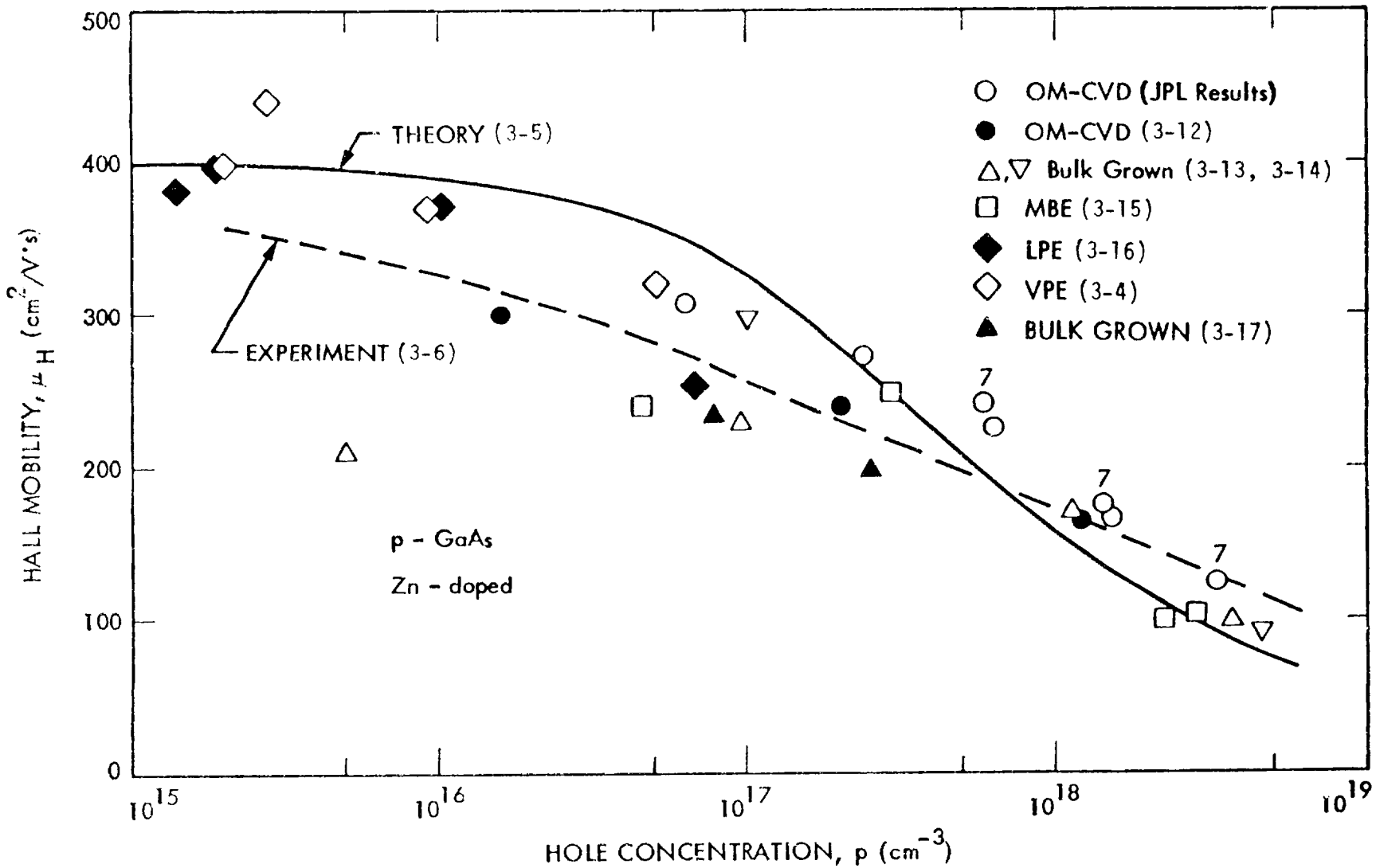

FIG. 3-4. Dependence of Hall mobility on hole concentration at room temperature for OM-CVD p-GaAs.

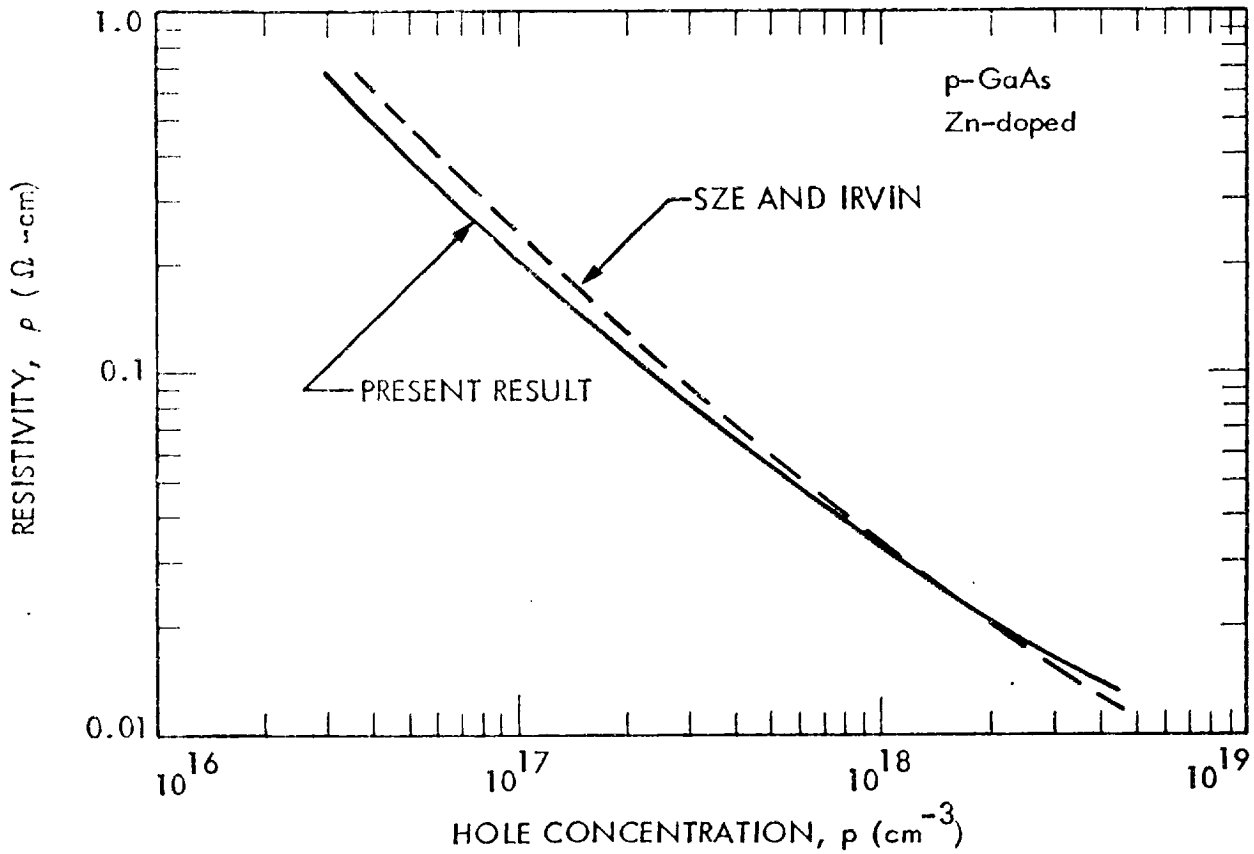

FIG. 3-5. Dependence of resistivity on hole concentration at room temperature for OM-CVD p-GaAs.

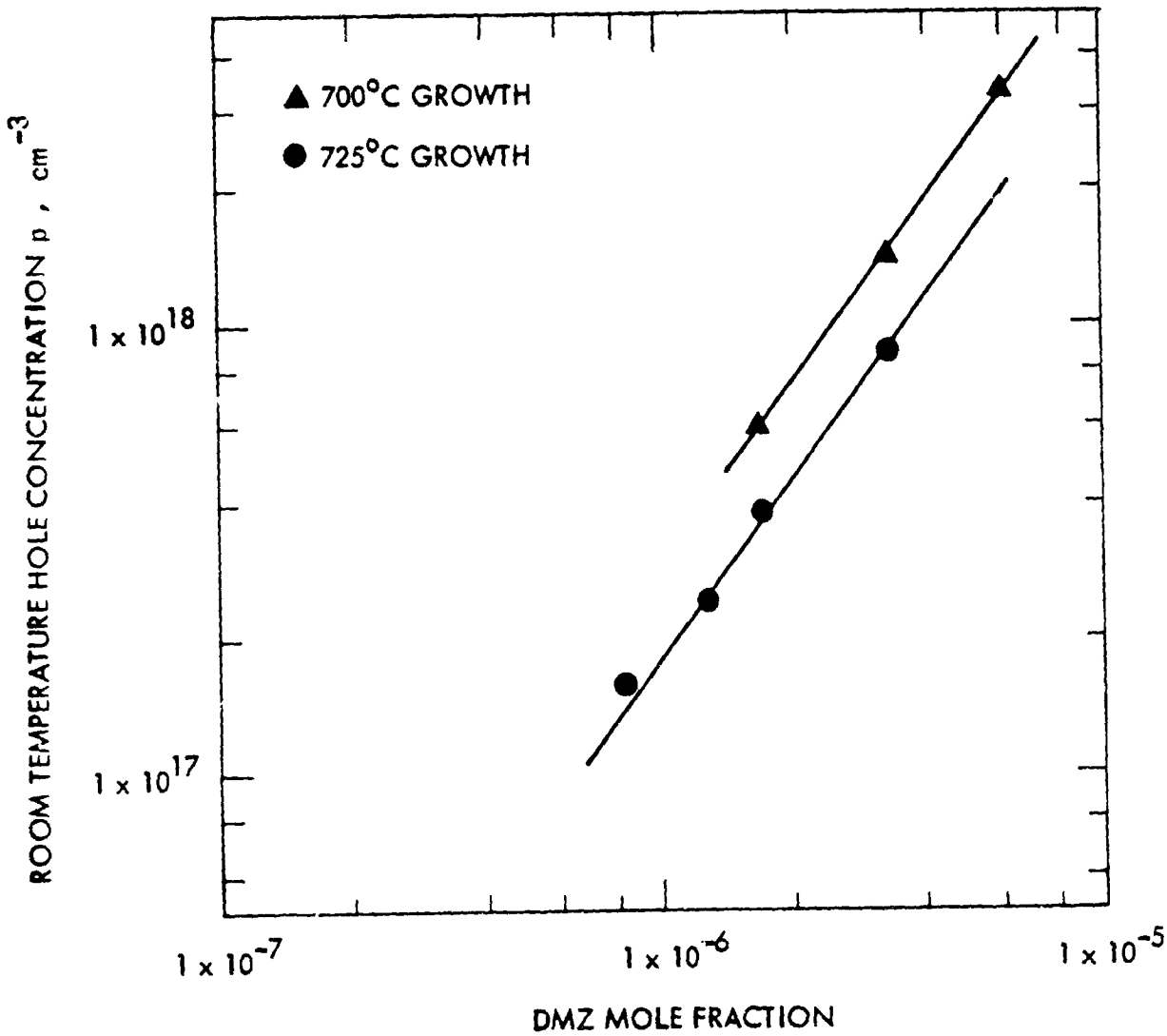

FIG. 3-6. Dependence of room-temperature hole concentration on dimethylzinc (DMZ) mole fraction for p-GaAs films grown by OM-CVD at 700°C and 725°C.

The investigation of depositing highly doped n-type GaAs using 1% H_2S in nitrogen was completed early in the program. Reproducible room-temperature electron concentrations, ranging from 9×10^{17} to 4×10^{18} cm^{-3}, were achieved at a growth temperature of 725°C, using a MF of H_2S between 1.7×10^{-5} and 4×10^{-4}, MF of AsH_3 of 1.6×10^{-3}, MF of TMG of 4×10^{-4}, H_2 flow rate of 3000 cc/min and a growth rate of 0.17 micrometer/min on Cr-doped, (100)-oriented GaAs wafer substrates.

Figure 3-7 shows the relationship between the room-temperature electron concentration and the mole fraction of H_2S doping gas. The saturation of room-temperature electron concentration at high mole fraction of H_2S due to the solid solubility limit of S in GaAs is clearly indicated. The room-temperature Hall mobility yielded values between 1248 and 3133 $cm^2V^{-1}s^{-1}$ for samples with room-temperature electron concentration (n) values between 4×10^{18} and 9×10^{17} cm^{-3}, respectively, as shown in Fig. 3-8. The Hall mobility value at $n = 9 \times 10^{17}$ cm^{-3} is very close to that measured by Sze and Irvin (Ref. 3-6) on GaAs at 300°K, as shown by the solid curve in Fig. 3-8 (dopant species unreported). However, at higher doping levels, an increased level of acceptor concentration due to residual impurities in the gas stream occurs concomitantly with the saturation of S in GaAs as the H_2S flow rate is increased. Hence, the observed Hall mobility values at increased doping levels were lower than those measured by Sze and Irvin (Ref. 3-6) because of the higher compensation ratio.

B. OHMIC-CONTACT EVALUATION

1. Vacuum-Deposited Ohmic Contact

A number of n^+/p homojunction, single-crystal GaAs solar cells were made by growing sequential-pair layers of p-type and n^+-type GaAs with varying thicknesses and doping concentrations on (100) p^+-type GaAs wafer substrates.

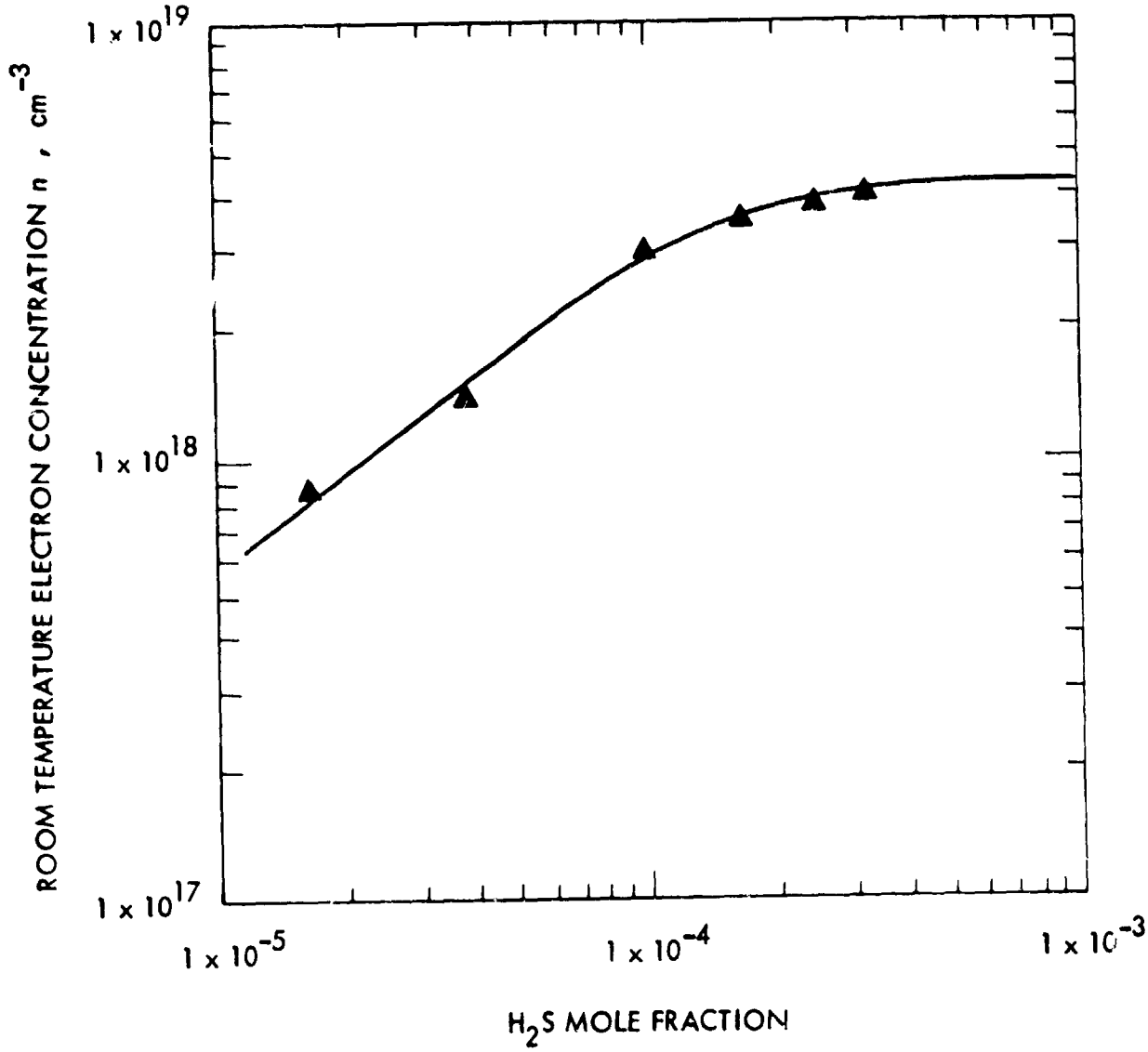

FIG. 3-7. Dependence of room-temperature electron concentration on H_2S mole fraction for n^+-GaAs films grown by OM-CVD.

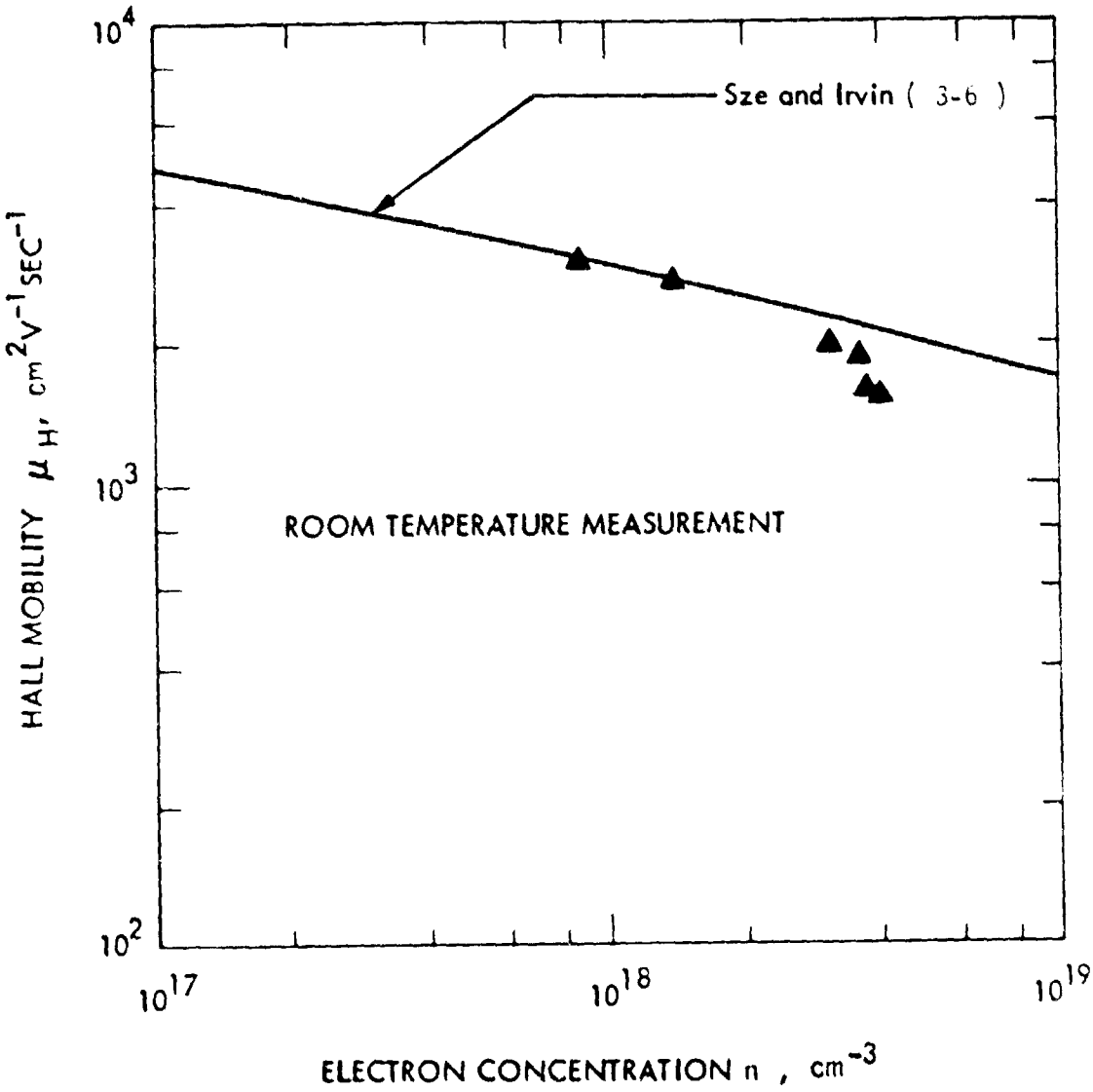

FIG. 3-8. Dependence of Hall mobility on electron concentration at room temperature for OM-CVD n^+-GaAs.

Initially, ohmic contacts on both the back surface of the p^+ substrate and the front surface of the n^+ grown layer were made by vacuum-deposition of either Au or Au:Ge eutectic compound (12% Ge by weight), due to lack of plating solutions at that time. Poor energy-conversion efficiency with AM1 simulation was generally obtained (ELH lamp calibrated by a standard Si solar cell). The main problem stemmed from the low value of the fill factor due to high contact resistance -- evidenced by non-ohmic behavior between isolated pads on n^+/p test samples. In an n^+/p homojunction solar cell structure, the n^+ layer needs to be thin (<1000Å). In order to avoid in-diffusion of the metallization, sintering is undesirable for forming the ohmic contact. However, ohmic contact processes for GaAs given in the literature almost invariably rely on sintering at temperatures higher than 300°C for times longer than 2 minutes. Therefore, vacuum-deposition of different materials on Te-doped (2×10^{17} cm^{-3}) substrates, S-doped (4×10^{18} cm^{-3}) films, and Zn-doped (2×10^{18} cm^{-3}) substrates were studied. The materials were deposited in an array pattern of 2-mm diameter dots with 3-mm center-to-center distance. Resistance values were calculated from I-V curves measured between two separate pads and corresponding to the zero-voltage value.

The best results on 2×10^{17} cm^{-3} Te-doped GaAs were achieved by depositing Au:Ge (12% Ge), with resistance between contact pads in the range of 3-12 ohm, without sintering. However, some contacts were not ohmic, showing excessive resistance values exceeding 10 k ohms. An HCl etch of the GaAs wafer before deposition and sintering did not eliminate the problem. The use of vacuum deposition of other metals, including Au, Ag:In:Ge (90:5:5 by weight) and Zn, also did not lead to good ohmic contacts without prolonged sintering (contact resistance of 5-10 ohms can be achieved for Au and Ag:In:Ge after sintering at 400-450°C for 1-3 mins). Similar results to those of 2×10^{17} cm^{-3} Te-doped GaAs were observed for 4×10^{18} S-doped GaAs.

With 2×10^{18} cm^{-3} Zn-doped GaAs (ground-surface finish), the best results were obtained on samples having metallized contacts of pure gold. A contact resistance of ≤ 1 ohm was achieved using gold contacts without sintering. Silver was the next best metal, with a contact resistance of about 5 ohms before sintering. However, the contact resistance increased after sintering at 300°C. Other metals used, including Ag:Zn (10% Zn by weight) and In, produced contact resistances of about 30 and 500 ohms before sintering, and about 70 ohms and 35 ohms after sintering, respectively.

2. Electro-plated Ohmic Contact

Because of the difficulties with evaporated and sintered contacts, a basic gold cyanide plating solution with pH ≥ 12 was used to form the ohmic contact on n^+ and p^+ GaAs substrates. Ohmic contacts were obtained on Te or S-doped n^+ GaAs substrates.

Subsequently, an Aurall 292 gold-plating solution was tried with separate contact pads on each wafer (either an n^+ or p^+ GaAs substrate with doping concentration in the range of $2\text{-}4 \times 10^{18}$ cm^{-3}) using a suitable masking process. Ohmic contacts with a contact resistance ≤ 1 ohm was observed for all such samples studied. To characterize the ohmic contact more precisely, photo-masks were designed for defining the patterns for etching cells and test structures. The masks were made for us by the Marshall Space Flight Center, where there is computerized capability for generating such masks. Figure 3-9 shows one of the photomasks for defining the mesa-etch pattern. These masks can be used not only for contact-resistance evaluation, but also for Hall measurement as well as C-V characterization.

To characterize the contact and to evaluate the contact resistance on GaAs, the transmission-line model (TLM) (Ref. 3-7) is most suitable. Figure 3-10

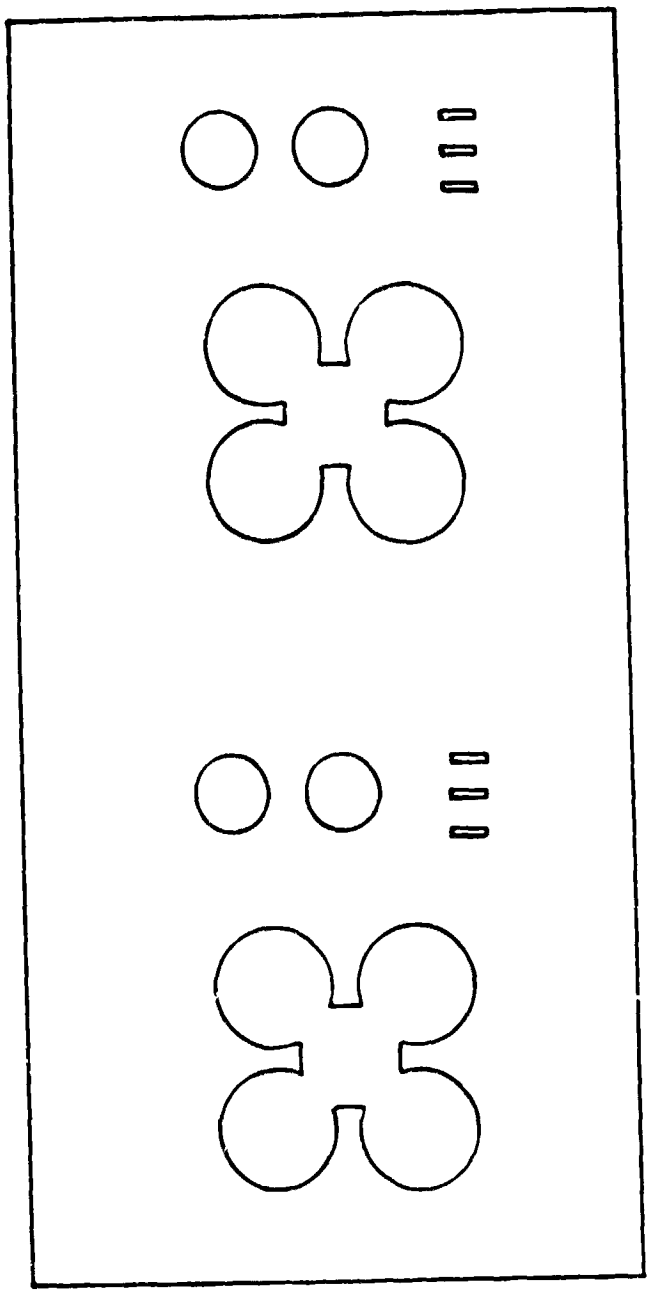

FIG. 3-9. Mesa-etch photomask for Hall and C-V measurements as well as contact-resistance evaluation.

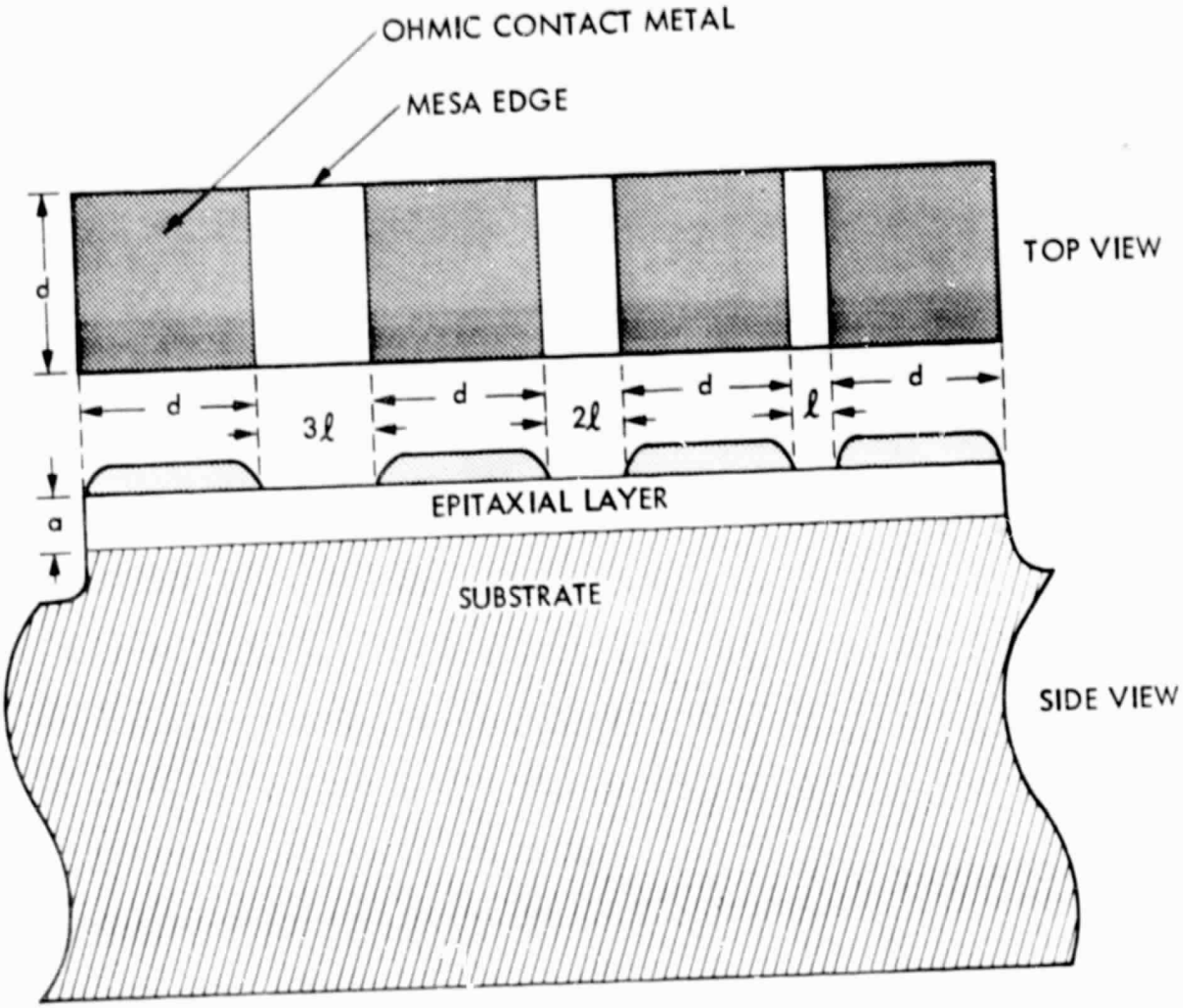

FIG. 3-10. Contact resistance test pattern.

shows such a contact-resistance test-pattern employing the TLM method. For a given material with known bulk resistivity ρ_B, epitaxial layer thickness a, and expected contact resistivity ρ_C, the dimensions of ℓ and d in Fig. 3-10 can be calculated from:

$$\ell = 1/(10\alpha) \quad \text{and} \quad d = 2/(\alpha),$$

where

$$\alpha = [\rho_B/(a\rho_C)]^{1/2}.$$

A photolithographic method was used to define the TLM test patterns for the evaluation of the ohmic-contact produced by the Lea Ronal Aurall 292 gold-plating process on the n^+/p GaAs substrate.

Figure 3-11 shows a photomicrograph of the contact resistance pattern of a sample made on an n^+/p GaAs structure. The gold pads were deposited at 55°C with about 2 mA/cm^2 current density using fresh gold-plating solution passed through a 0.4 micrometer filter. The filtration is important for maintaining good edge-definition during the plating process. After evaluation of numerous test patterns made on n^+/p GaAs substrates having doping concentration n^+ of about 4×10^{18} cm^{-3}, the upper bound of the ohmic contact-resistivity was found to be less than 10^{-2} ohm-cm^2. This contact-resistivity value is sufficiently low for solar cells intended for use without solar concentration.

C. SINGLE-CRYSTAL n^+/p SHALLOW HOMOJUNCTION CELLS ON GaAs

Since low conversion efficiency arising from low V_{OC} values was observed for AMOS cells made on GaAs/poly-Ge substrates, the emphasis of our program was shifted towards the n^+/p shallow-homojunction as the initial alternate approach. A good photolithographic system is essential in obtaining consistent results on large area n^+/p solar cells. During this reporting period, an existing dark room was converted into a "yellow room" for the photolithographic process.

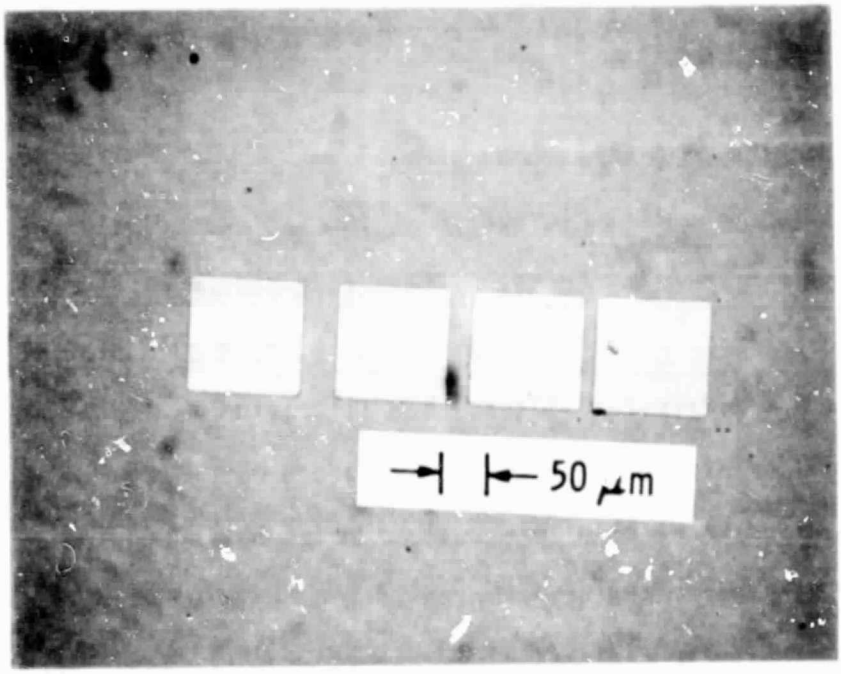

Fig. 3-11. A photomicrograph of the contact resistance pattern made on an n^+/p structure.

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Specially designed photomasks for a front-contact grid structure were made and used to produce a 1 cm x 1 cm mesa-etch. Figure 3-12 shows the front-contact structure.

In the front-contact grid design, ten lines 0.95 cm long and 12.5 micrometers wide, spaced 1 mm apart, were used to minimize the series resistance due to the high sheet-resistance of the very thin top n^+-layer. A wedge-shaped bus-line situated in the center of the 1 cm x 1 cm structure and perpendicular to the conducting fingers was used to collect current from each finger. The wedge-shaped bus-line design is employed to reduce the shadowing loss. The thick end of the wedge was terminated by a rectangular pad 2 mm x 1 mm as a probe or soldering contact. Two additional lines 0.95 cm long and 50 micrometers wide were placed perpendicularly to the fine-line conducting fingers as built-in redundancy elements for collecting the photogenerated current in case of broken finger-lines. The shadowing loss of this front-grid structure was only about 4.6%.

Initially, due to lack of a mask aligner at that time, a number of 1 cm x 1 cm-area n^+/p GaAs solar cells were made using a photolithographic method with the alignment of photomasks done by hand. Unfortunately, the results were inconsistent and not reproducible. Poor fill factors and poor conversion efficiencies were observed for these 1 cm^2-area devices.

In order to discover the cause for the poor photovoltaic response of the 1 cm x 1 cm-area n^+/p solar cells, arrays of small-area n^+/p solar cells (0.005 cm^2) were made on particular substrates. Initially, inconsistent photovoltaic responses were also observed between these small array cells on the same wafer. By correlating a test-cell response with its appearance under the optical microscope, it was determined that the bad solar cells had poor mesa-etch photomask registration, resulting in overlap of the mesa-etched edge with the gold contacting-pad. The observed poor photovoltaic response was

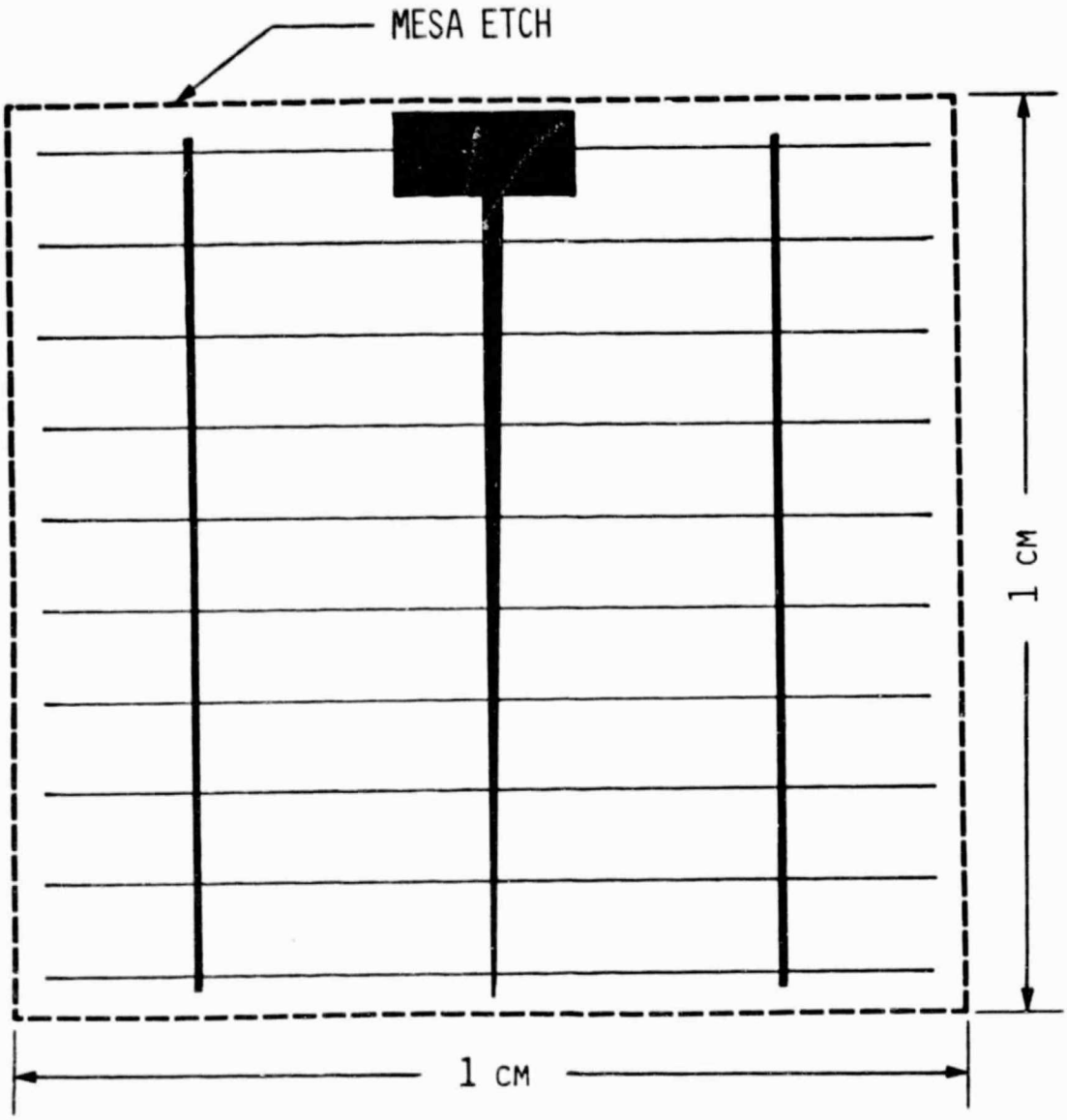

FIG. 3-12. The front contact grid design for 1 cm x 1 cm n^+/p solar cell.

therefore probably due to the replating of gold across the mesa-etched edge during mesa-etching of the n^+/p GaAs wafer in the presence of the exposed gold contacting-pad nearby. Such replating of gold created additional shunting across the n^+/p junction and caused the observed low photovoltaic response of the solar cell. This finding might also partially explain why poor photovoltai response was observed for the 1 cm x 1 cm n^+/p solar cell. Some portion of the gold contact fingers overlapped the mesa-etched edge, thereby causing increased leakage current.

Subsequently, improved techniques for hand alignment of the metallizing and mesa-etching of small-area mesa solar cell structures led to some encouraging diode dark I-V characteristics. The dark forward I-V characteristics curve typical of such diodes with 5×10^{-3} cm^{-2} area is shown in Fig. 3-13. The apparent diode ideality factor n in this case was about 1.4 when a single-exponential curve-fitting procedure was performed on the high-current portion of the dark I-V curve. The corresponding reverse saturation current density was about 2×10^{-14} A/cm^2. A double-exponential curve fitting was also performed. The procedure is based on the expression:

$$J_D = J_{01} (\exp (qV_D/n_1kT) - 1) + J_{02} (\exp (qV_D/n_2kT) - 1) + V_D/R_{SH} , \quad (1)$$

where J_D is the measured dark forward current density, J_{01} is the reverse saturation current density associated with the diffusion current of an ideal junction, q is the electronic charge, k is the Boltzmann constant, J_{02} is the equivalent reverse saturation current density due to additional current transport mechanisms (e.g., recombination in the depletion region due to undesirable trapping centers, surface recombination at the junction edges, etc.),

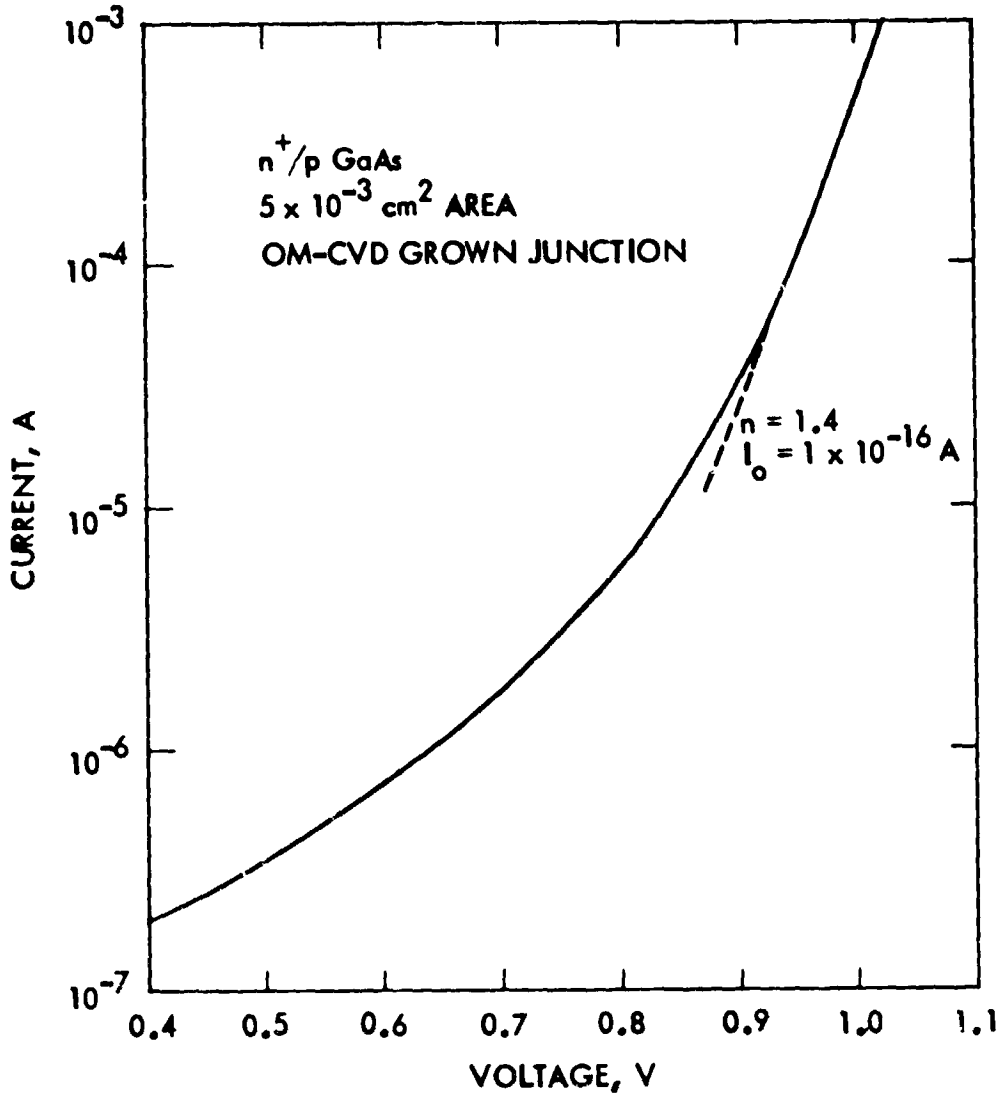

FIG. 3-13. Dark forward I-V characteristics of a small-area n^+/p diode.

and R_{SH} is the shunt resistance across the diode. The voltage across the junction of the diode, V_D, is related to the applied voltage V by $V_D = V - J_D R_S$, where R_S is the series resistance per unit area. The results of such curve fitting are as follows: $J_{01} = 1 \times 10^{-18}$ A/cm^2, $n_1 = 1$, $J_{02} = 1.4 \times 10^{-8}$ A/cm^2, $n_2 = 2.8$, $R_{SH} = 6.9$ k ohm cm^2 and $R_S = 7.5 \times 10^{-2}$ ohm cm^2, with an rms error of about 1.5% through the current range from 10^{-6} to 10^{-3} A. Comparing the magnitude of the diode current density associated with the different parameters, it was found that at a current density higher than 13 mA/cm^2, the diffusion current term of the ideal junction characteristic begins to dominate the diode current term. However, even at 30 mA/cm^2 which is essentially the maximum theoretical current density (Ref. 3-8) for a GaAs solar cell under AM1 illumination (Refs. 3-9 and 3-10), about one third of the diode current is contributed by the term associated with the non-ideal diode factor of $n_2 = 2.8$.

From the diode dark I-V characteristics, a simulated light I-V relationship can be derived according to the following expression:

$$J = J_L - J_D \,, \qquad (2)$$

where J_D is given by eq. (1), J is the measured output current density, and J_L is the light-generated current density. Based on the diode dark I-V characteristics shown in Fig. 3-13 and assuming a short-circuit current density of 24.5 mA/cm^2 under AM1 conditions (normalized to 100 mW/cm^2 input power density), a simulated light I-V curve was derived and is shown in Fig. 3-14. From this curve, the projected V_{oc}, FF and conversion efficiency are 0.956V, 0.8, and 18.8%, respectively. Subsequently, a small mesa-etched diode of 2 mm-diameter with a 1-mm electrode was fabricated on a second wafer during the same OM-CVD growth experiment. The photovoltaic data obtained supports the projected V_{oc} and FF values. This indicates that fairly accurate estimates

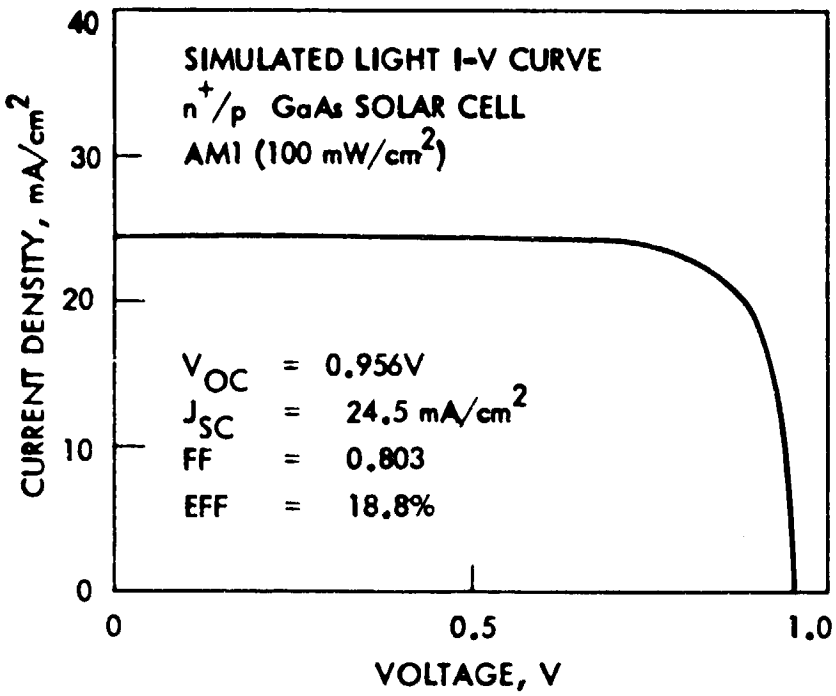

FIG. 3-14. Simulated light I-V characteristics of the same n^+/p GaAs junction used in the previous figure.

of the photovoltaic results may be obtained by studying the dark forward I-V characteristics. Further study of the simulated light I-V characteristics indicated that the improvement in V_{oc} is very minor (about 0.01V) even if one can eliminate the current term due to the non-ideal junction (n_2 = 2.8) behavior. This is because of the logarithmic dependence of V_{oc} on diode current density. On the other hand, the improvement in FF is significant (from 0.80 to 0.87). Due to the improvement in both V_{oc} and FF, the expected performance of such a solar cell would have a conversion efficiency of 20.6% as compared to the original 18.8%. For comparison purposes, the reverse saturation current density of an ideal, abrupt n^+/p GaAs junction is 1.2×10^{-19} A/cm^2 (assuming $n^+ = 4 \times 10^{18}$ cm^{-3}, $p = 2 \times 10^{17}$ cm^{-3}, electron mobility in the p-region equal to 3000 cm^{2}V^{-1}s^{-1}, electron diffusion length in the p-region equal to 5 micrometers and the intrinsic carrier concentration equal to 10^6 cm^{-3}), which is about one-eighth of the measured J_{01} value (9.7×10^{-19} A/cm^{-3}) obtained from curve fitting of the dark I-V characteristics. Hence, some improvement in the grown n^+/p junction should be achievable.

One possible cause of the deviation of reverse saturation current density from that for the ideal abrupt junction was postulated to be a lack of abruptness in the grown n^+/p homojunction. A non-abrupt junction structure could be caused by the in-diffusion of the n^+ dopants into the p-layer during the OM-CVD growth of the n^+ top layer, or by non-ideal phasing of the dopant-gas flows. The non-abruptness would then reduce the built-in potential across the n^+/p junction, leading to higher-than-expected reverse saturation current density. To determine the abruptness of the n^+/p junction, samples of OM-CVD grown n^+/p substrates were sent to Charles Evans & Associates, San Mateo, California, for analysis using Secondary Ion Mass Spectrometry (SIMS). The samples were analyzed under high resolution to distinguish between ^{32}S and $^{32}(O_2)$.

During the analysis of the S profile, cesium ions were used to probe the surface with total sputtering time ranging from 1200 to 2200 seconds. After obtaining the depth profiles for the n^+/p samples, the samples were shipped back to JPL and the depth of each crater formed during the ion sputtering was determined by a Model 10 Alpha-step Microtopographer made by Tencor Instruments, Inc., Mountain View, California. The depth profiles of both [S] and [O_2] obtained by SIMS for two samples are shown in Figures 3-15 and 3-16.

The n^+/p GaAs sample of Figure 3-15 was grown on a (100) p^+-GaAs substrate purchased from Morgan Semiconductor, Garland, Texas. The initial p^+- and p-layers (each about 1.8 micrometers thick) were grown at 725°C with a Zn-doping concentration of 3×10^{18} and 2×10^{17} cm^{-3}, respectively. The subsequent n^+-layer was grown at the same temperature with a S-doping concentration of 4×10^{18} cm^{-3} and a thickness of about 0.2 micrometer.

The n^+/p GaAs sample of Figure 3-16 was grown on a (100) p^+-GaAs substrate purchased from Crystal Specialties, Monrovia, California. This substrate has higher residual S concentration than the substrate of Fig. 3-15, as evidenced by the step shown in the [S] depth profile. For this sample, an initial p^+-layer was grown at 700°C with a Zn-doping concentration of 3×10^{18} cm^{-3} and a thickness of about 2 micrometers, followed by a p-layer grown at 725°C with a Zn-doping concentration of 2×10^{17} cm^{-3} and a thickness of about 2 micrometers. The final n^+-layer was grown at 725°C with a S-doping concentration of 4×10^{18} cm^{-3} and a thickness of about 0.2 micrometer. The figures clearly indicate some diffusion of the n^+-dopant (S) into the underlying p-layer. The tail portion of the observed S concentration, can be approximated by the expression

$$[S] \propto \exp(-x/L) \quad ,$$

where x is the depth parameter and L is a constant. The value of L was found to be about 0.1 micrometer for most of our samples. This diffusion of S would

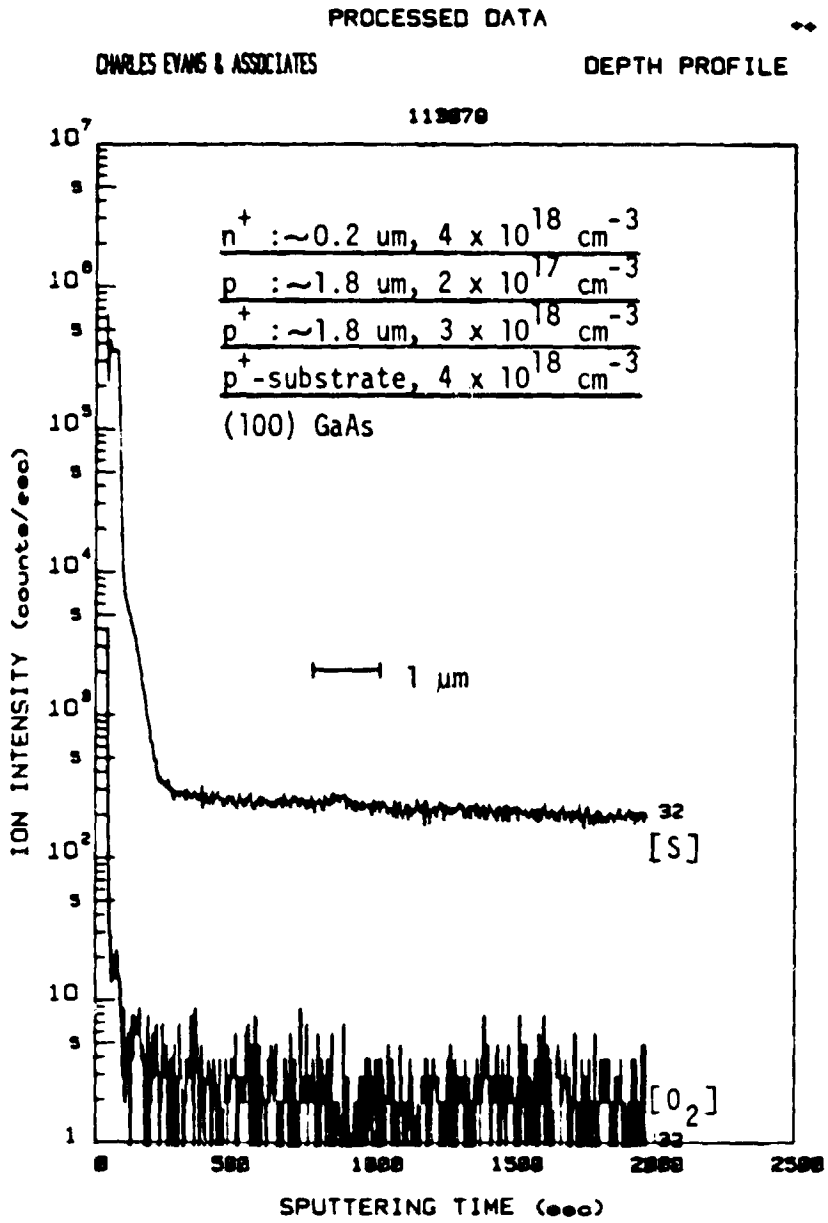

FIG. 3-15. SIMS depth profile of an $n^+/p/p^+$ structure on (100) GaAs substrate (purchased from Morgan Semiconductors).

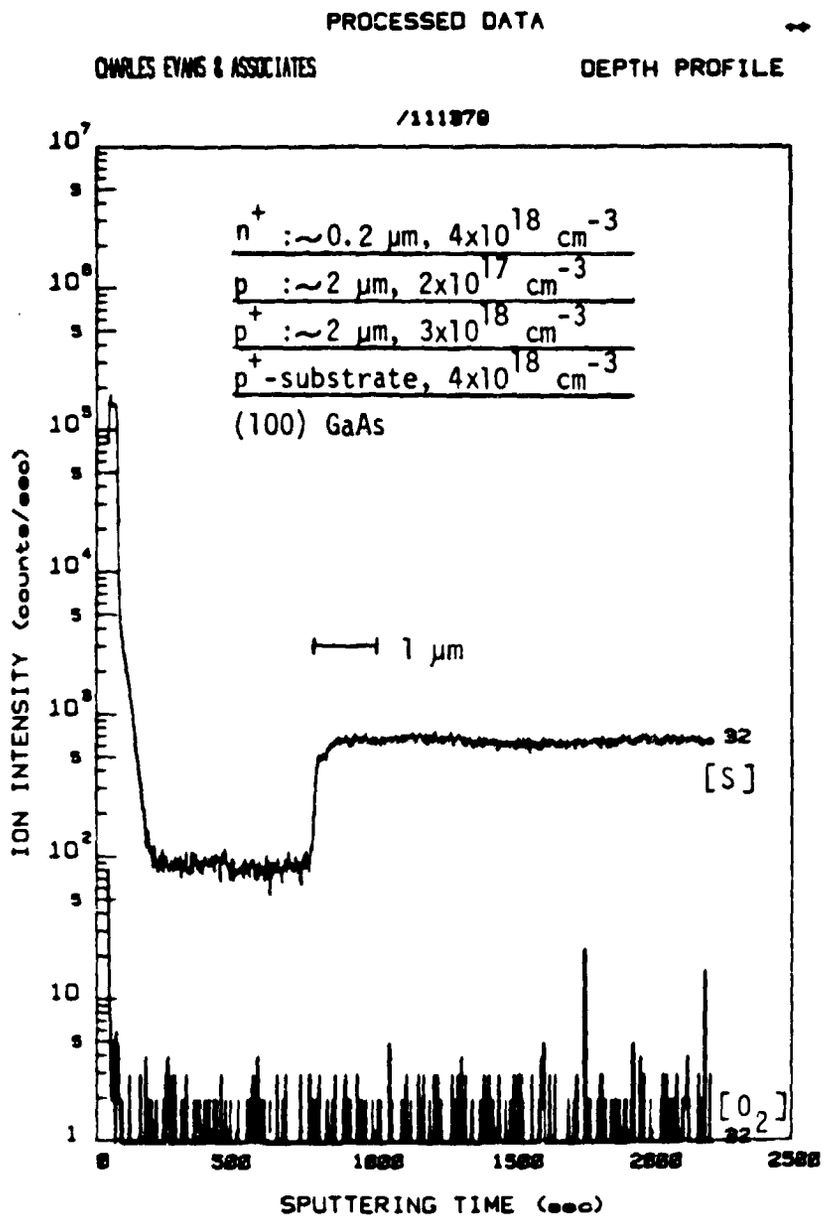

FIG. 3-16. SIMS depth profile of an $n^+/p/p^+$ structure on (100) GaAs substrate (purchased from Crystal Specialties).

decrease the abruptness of the n^+/p junction, leading to a configuration closer to a graded-junction structure. Hence, a lower built-in potential and open-circuit voltage than that of the ideal abrupt n^+/p junction would be measured, agreeing with the observation of the less-than-ideal behavior of the n^+/p diode, as discussed above. The initially high SIMS oxygen signal, dropping rapidly as the bulk is approached in both Figures 3-15 and 3-16, may be due to surface oxidation. The $^{32}[O_2]$ level in the bulk region was really below the detection limit of the SIMS instrument, with the fluctuations being due to instrumental noise.

As discussed earlier, poor photovoltaic response was observed for initially made 1 cm x 1 cm n^+/p solar cells, due to poor mesa-etch edge definition before proper photomask alignment equipment was obtained. Subsequently, a Kasper Model 2001C mask aligner was ordered and received. It was then modified to the approximating-printing mode and installed in the yellow room. Good line definition and registration were then obtained for front-contact-grid and mesa-etch patterns. Subsequently, the mask aligner was used to make contacts for 1 cm x 1 cm n^+/p GaAs shallow-homojunction solar cells grown by OM-CVD on single-crystal (100) GaAs substrates.

Additional GaAs cells were made by sequential growths of a 2 micrometers thick p^+-layer ($p^+ = 3 \times 10^{18}$ cm^{-3}, Zn-doped), a 2 micrometers thick p-layer ($p = 2 \times 10^{17}$ cm^{-3}, Zn-doped) and a 0.2 micrometer thick n^+ layer ($n^+ = 4 \times 10^{18}$ cm^{-3}, S-doped) on Zn-doped p^+ GaAs ($p^+ = 4 \times 10^{18}$ cm^{-3}) substrates with orientation approximately 2° off (100) toward the (110) plane. The OM-CVD GaAs growth temperature was 725°C, and an As/Ga mole ratio of 6, arsine MF of 1.6×10^{-3}, TMG MF of 9×10^{-4}, and H_2 flow rate of 3000 cc/min were used. In fabricating the

n^+/p solar cells, the back contact was first deposited by the electroplating method. Subsequently, an AR coating of approximately 1000 Å was produced by an anodic method similar to the one described by Hasegawa and Hartnagel (Ref. 3-11). Anodization of the GaAs was performed at room-temperature using a 4N purity aluminum plate as the cathode. During the anodization process, about 550 Å of GaAs at the surface was oxidized. Both the thickness of the AR coating as well as the thickness of the oxidized GaAs layer were measured by the Model 10 Alpha-step Microtopographer.

Typical energy conversion efficiencies of about 15% were obtained for these solar cells under simulated AM1 conditions (ELH lamp), with the best efficiency being 15.3%. The light I-V characteristics curve for the best solar cell is shown in Fig. 3-17. The values of V_{oc}, J_{sc} and FF for this solar cell were about 0.97 volt, 20 mA/cm^2 and 0.79, respectively. The dark I-V characteristics curve for the same solar cell is shown in Fig. 3-18. A double-exponential curve fitting using the expression of Eq. (1) above was performed. The parameter values obtained were: $J_{01} = 1.4 \times 10^{-19}$ A/cm^2, $J_{02} = 5.6 \times 10^{-12}$ A/cm^2, $n_1 = 1$ and $n_2 = 1.8$. For convenient comparison purposes, the curve-fitting results for the best small-area n^+/p GaAs solar cell discussed earlier were: $J_{01} = 1.0 \times 10^{-18}$ A/cm^2, $J_{02} = 1.4 \times 10^{-18}$ A/cm^2, $n_1 = 1$ and $n_2 = 2.8$. The remarkable reduction in J_{01}, J_{02} and n_2 values for the n^+/p GaAs solar cell with much larger area (1 cm^2) was due to improvements in the photolithographic process, which also caused the improvement in FF and V_{oc} values shown in Fig. 3-17. It is significant to note that the low J_{sc} value was expected, since the thickness of the top n^+-layer (about 1500 Å) was not optimized at that time. Hence it was expected that reducing the n^+-layer thickness to an optimum value should result in n^+/p GaAs cells with efficiencies above 18%.

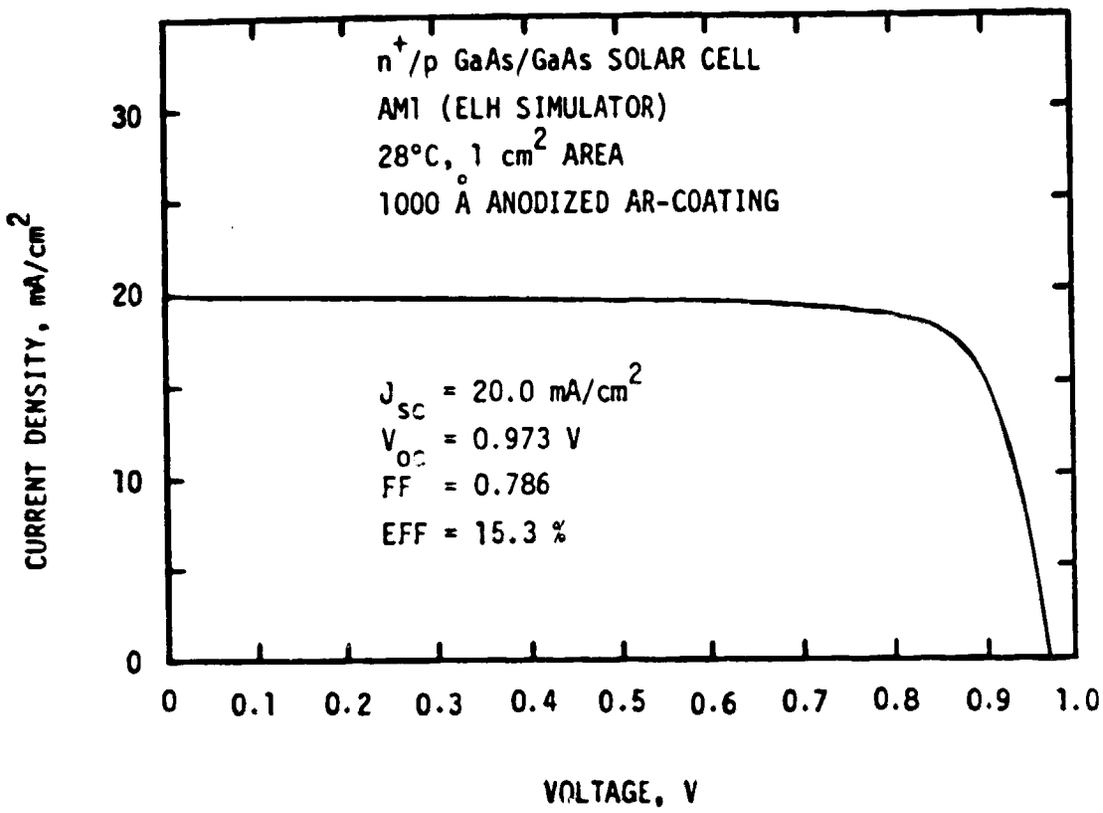

FIG. 3-17. Light I-V characteristics of a 1 cm x 1 cm area n^+/p GaAs/GaAs solar cell.

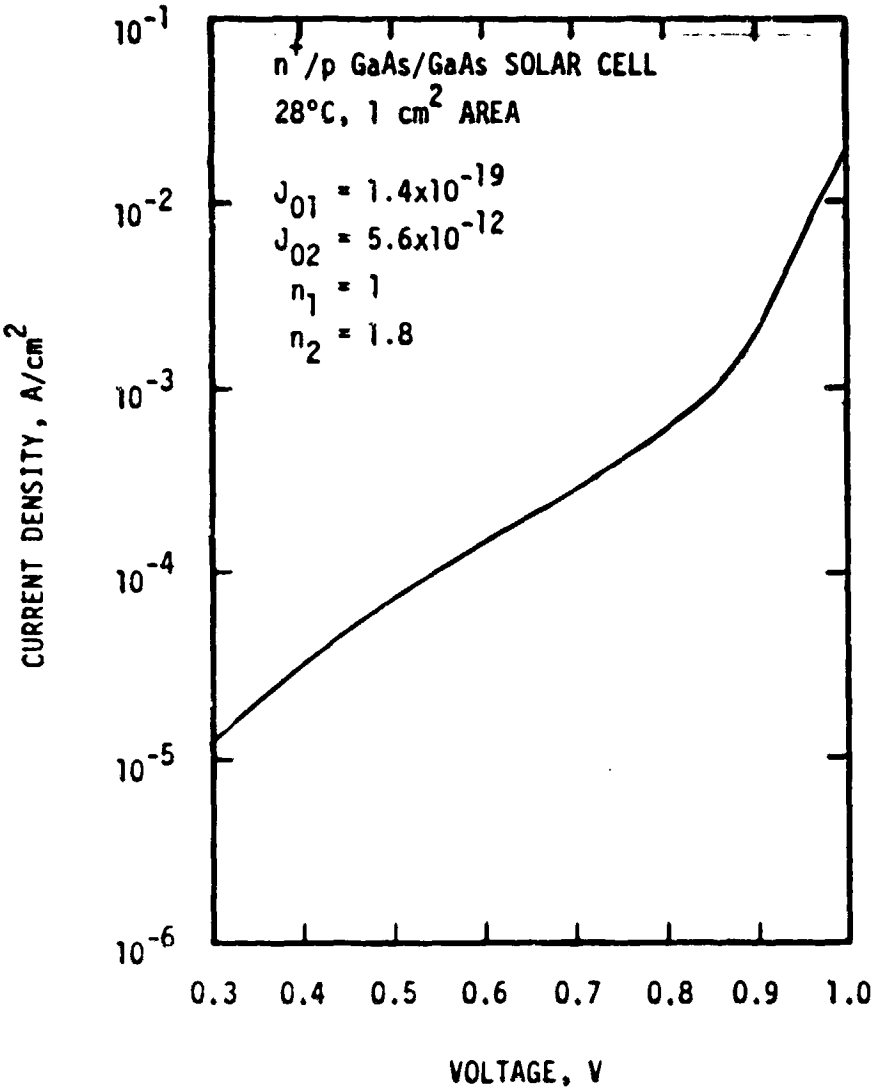

FIG. 3-18. Dark I-V characteristics of the same solar cell used in obtaining the curve of Fig. 3-17.

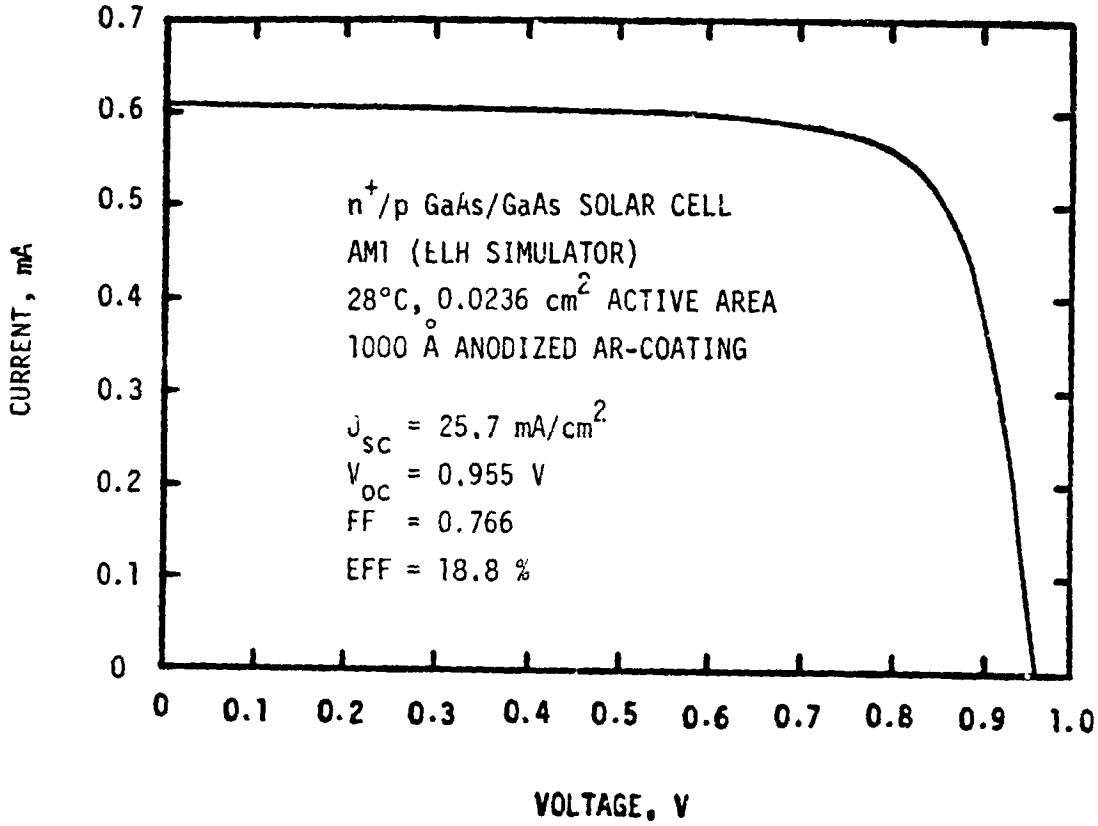

FIG. 3-19. Light I-V characteristics of a small (2.36 mm^2 active area) n^+/p GaAs/GaAs solar cell made by the sequential anodization-etching technique.

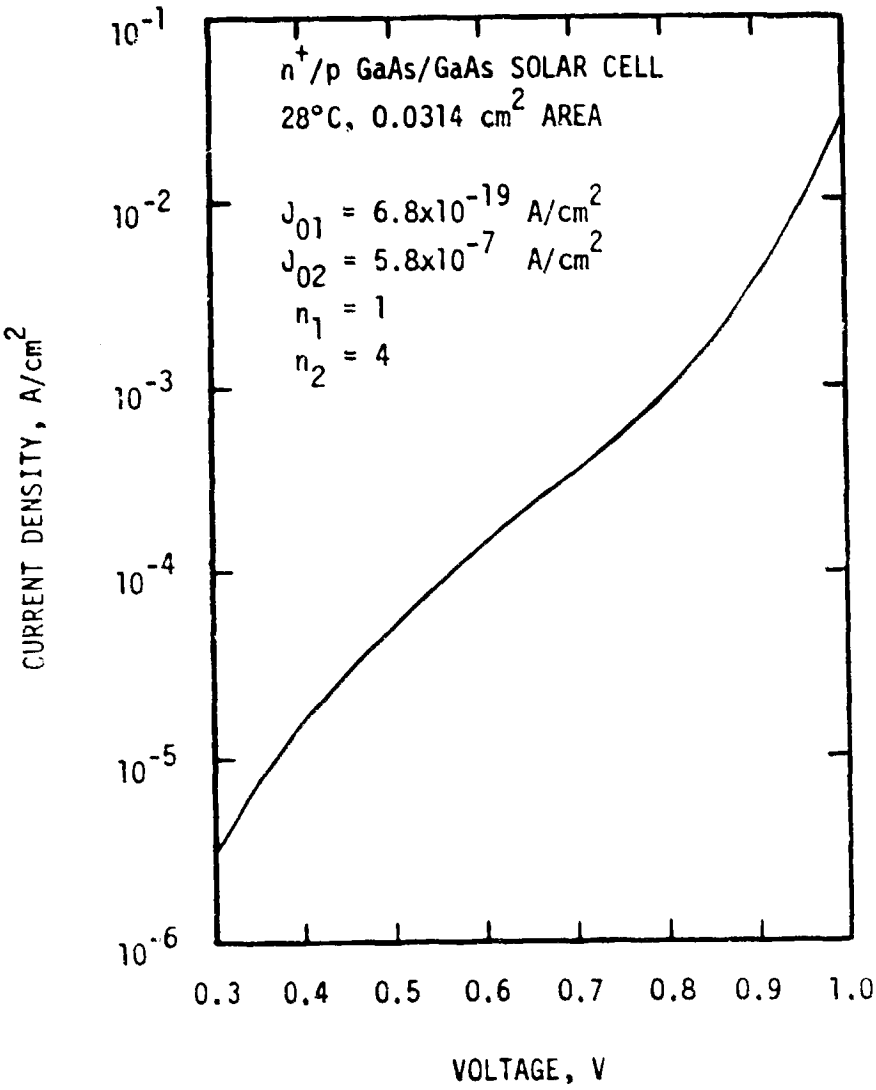

FIG. 3-20. Dark I-V characteristics of the solar cell used for obtaining the curve in Fig. 3-19.

n^+-layer shown in Fig. 3-18, it is clearly evident that its J_{02} value is 10^5 times larger (5.8×10^{-7} A/cm^2 vs. 5.6×10^{-12} A/cm^2) and its n_2 value is more than twice as large (4 vs. 1.8), indicating deleterious high current leakage.

It was postulated that the thinning of the top n^+-layer by the sequential anodization-etching technique apparently was not uniform, and probably introduced localized pin holes or ultra-thin regions with thickness less than the dimension of the normal depletion-width. As a result, there existed undesirable shunting effects between the grid metallization and the p-type base layer. Indeed, this was verified from the observation that photovoltaic responses of array cells made on a 1.2 x 1.2 cm GaAs wafers were not consistent when the sequential anodization-etching technique was used. Hence, it would be very difficult to make a large area (1 cm^2 or larger) n^+/p shallow-homojunction device and obtain a conversion efficiency similar to the best small area (2.36mm^2 active area) cells using this technique.

One solution to this problem that has been proposed elsewhere is to grow the n^+-layer to a thickness of about one micrometer, then deposit the grid metallization, and by many successive oxidations and etching steps (stripping), to reduce the average thickness of the n^+-layer between the grid metallizations to about 500 Å. This procedure imposes stringent requirements on the thickness control of the stripping, is costly and time-consuming, and thus economically unfavorable for large-scale production.

Subsequently, a new approach for fabricating high-efficiency shallow homojunction n^+/p GaAs solar cells was successfully developed in our work, resulting in GaAs solar cells showing an AM1 conversion efficiency of 20.3% (19.3% when a 5% grid coverage is assumed) and having an active area of 2.36 mm^2. The corresponding values of V_{oc}, J_{sc} and FF for a typical solar cell were 0.97 V, 25 mA/cm^2

and 0.82, respectively. In addition, by employing this new innovative technique, large area (1 x 1 cm) homojunction n^+/p GaAs/GaAs solar cells having AM1 conversion efficiencies of greater than 19% (ELH Lamp) were also successfully fabricated. These cells were made by the direct growth of an ultra-thin (about 500 Å) n^+-GaAs top layer using OM-CVD, instead of thinning it down by sequential anodization-etching steps from the originally grown thickness. Vacuum-deposited Sb_2O_3 was used for the anti-reflection coating instead of the anodization method previously used. The cells typically had values of V_{oc}, J_{sc} and FF of 0.98V, 25 mA/cm^2 and 0.76, respectively. The light I-V curve of one such cell is shown in Fig. 3-21. The greater cell efficiencies obtained by using the new technique arise from the consistently good V_{oc} and FF values because the detrimental problems of anodization are avoided altogether. One of these solar cells was delivered to SERI for evaluation in November 1980.

D. SINGLE-CRYSTAL n^+/p SHALLOW HOMOJUNCTION CELLS ON Ge

Before undertaking the development of the GaAs/Ge/low-cost-substrate solar cell structure, it was deemed necessary to study the hetero-epitaxial growth of GaAs on a single-crystal Ge wafer. Hence, fabrication of n^+/p structures on single-crystal Ge substrates was undertaken using the same growth parameters and, for the initial work, the sequential anodization-etching technique previously described for the single-crystal GaAs substrates. Very poor surface morphology and leaky diode characteristics were observed on the first few n^+/p GaAs/Ge structures made. The leaky diode performance was partially caused by the poor substrate-surface morphology, resulting in a shunted junction after electroplating the conducting grid contact on the top surface. In addition, some portions of the top n^+-layer might have been completely removed during

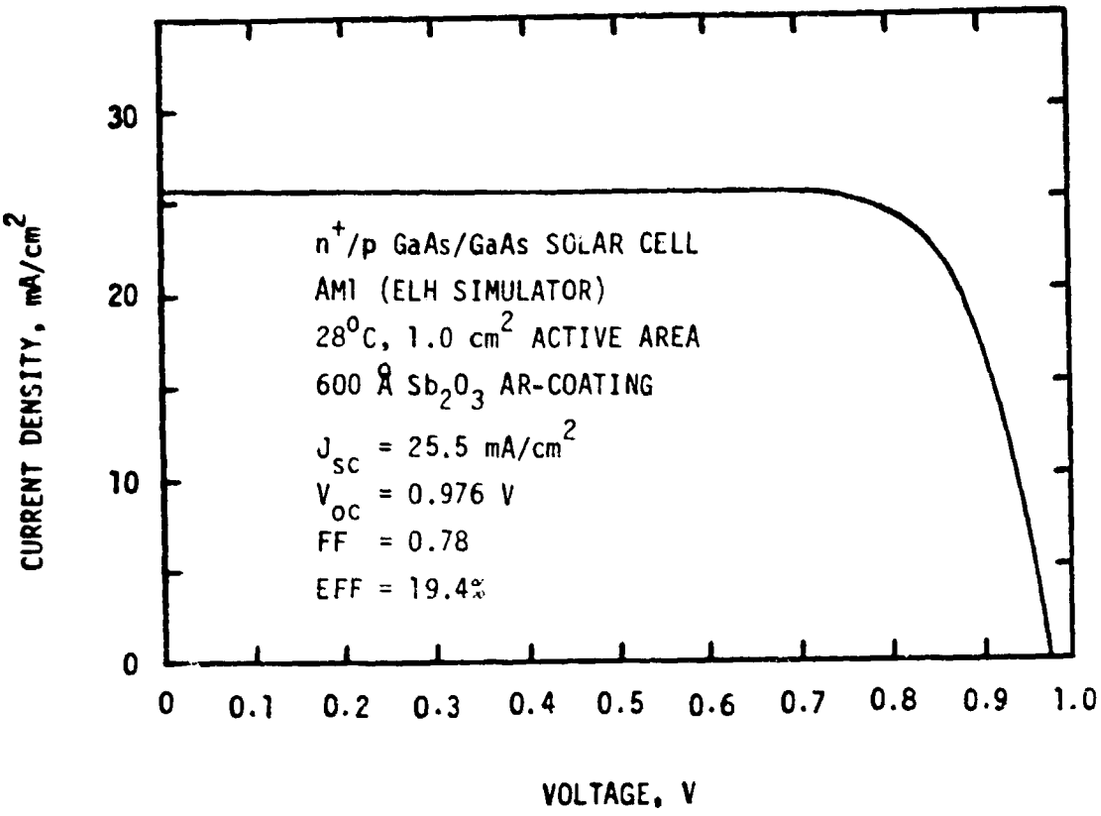

FIG. 3-21. Light I-V characteristics of a large area (1.0 cm^2) n^+/p GaAs/GaAs solar cell made by the direct deposition method without anodic thinning (see text).

thinning arising from the anodization process and from producing the 1000 Å-thick anodic AR coating. Another possible cause of the shunted junction might have been auto-doping from the Ge substrate.

To resolve these problems associated with the n^+/p GaAs/Ge structure, a study was undertaken of the properties of GaAs grown on (100) Ge using different substrate surface treatment and growth conditions. Among the different chemical etchants used were CP4, CP4A, $HF:H_2O_2:H_2O:CH_3COOH$, and $HF:HNO_3:H_2O_2:CH_3COOH$ (9:4:4:20). The last etch was found to result in the best GaAs surface morphology after OM-CVD growth. Figure 3-22 is a photomicrograph of a GaAs/Ge surface for which a CP4 etch of the Ge substrate was used prior to the OM-CVD growth. Figure 3-23 is a photomicrograph of a GaAs/Ge surface for which an HCl in-situ vapor etch of the Ge substrate was used. Poor surface morphology is evident in each case. On the other hand, Fig. 3-24 is a photomicrograph of the GaAs surface using the $HF:HNO_3:H_2O_2:CH_3COOH$ (9:4:4:20) etch prior to GaAs growth, showing a fairly smooth surface morphology.

The surface morphology of GaAs grown on Ge was also found to be strongly influenced by the growth temperature. Smooth GaAs epi-layers on Ge substrates were obtained at growth temperatures of 700°C or higher. However, auto-doping by Ge from the substrate at 700°C was excessive (N_d of about 10^{18} cm^{-3} for otherwise undoped GaAs, as determined by Hall measurement). At 625°C growth temperature, Ge auto-doping was not observed, but poor surface morphology was invariably obtained, indicating that this temperature was too low for heteroepitaxial growth of GaAs on (100) Ge. In order to improve the surface morphology and yet avoid high auto-doping, a method using sequential GaAs growths at two temperatures, a higher one for initial nucleation and a lower one for continued growth was found to be beneficial and is currently under investigation.

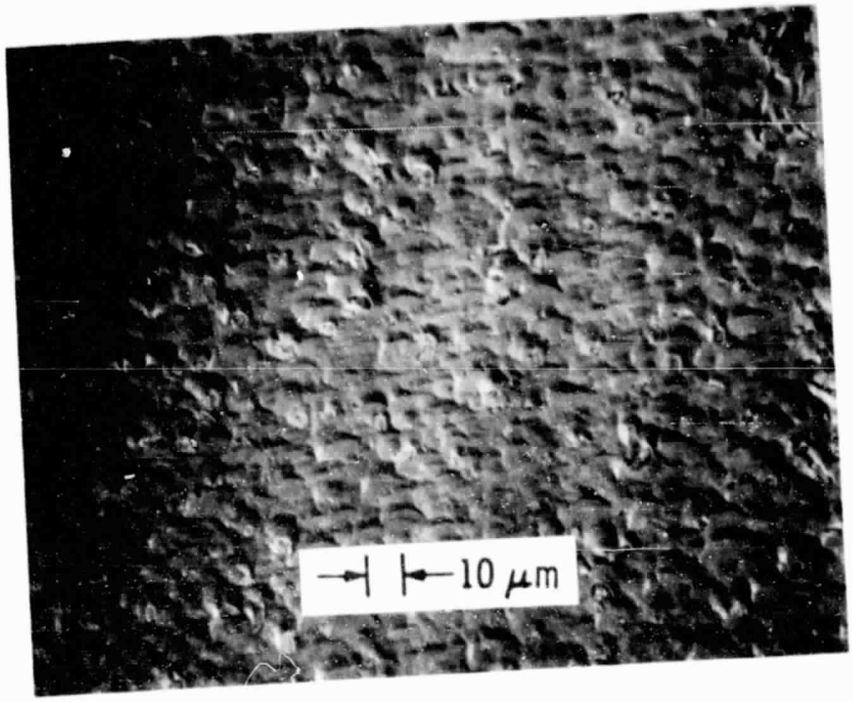

FIG. 3-22. Photomicrograph of the GaAs/Ge surface with CP4 etch prior to GaAs growth.

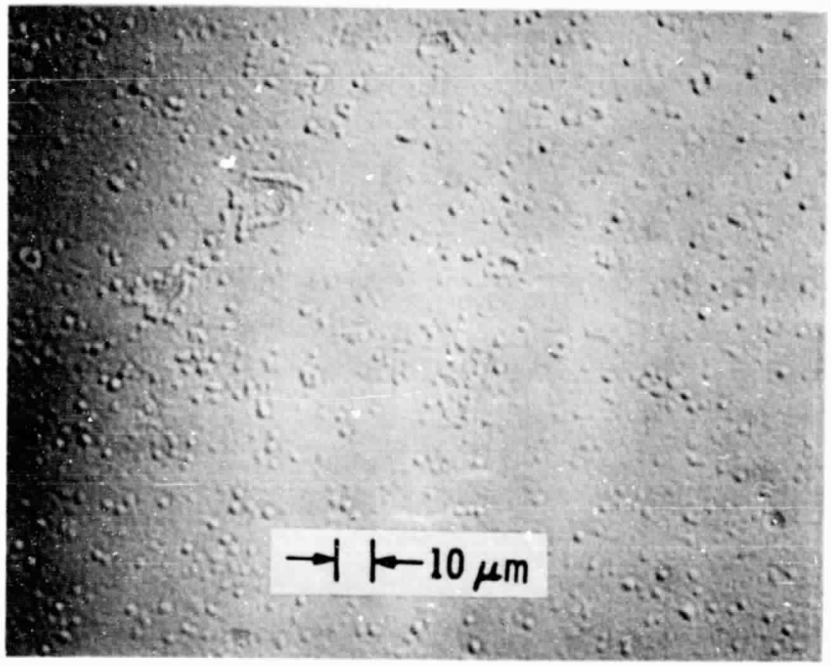

FIG. 3-23. Photomicrograph of the GaAs/Ge surface with HCl in-situ etch prior to GaAs growth.

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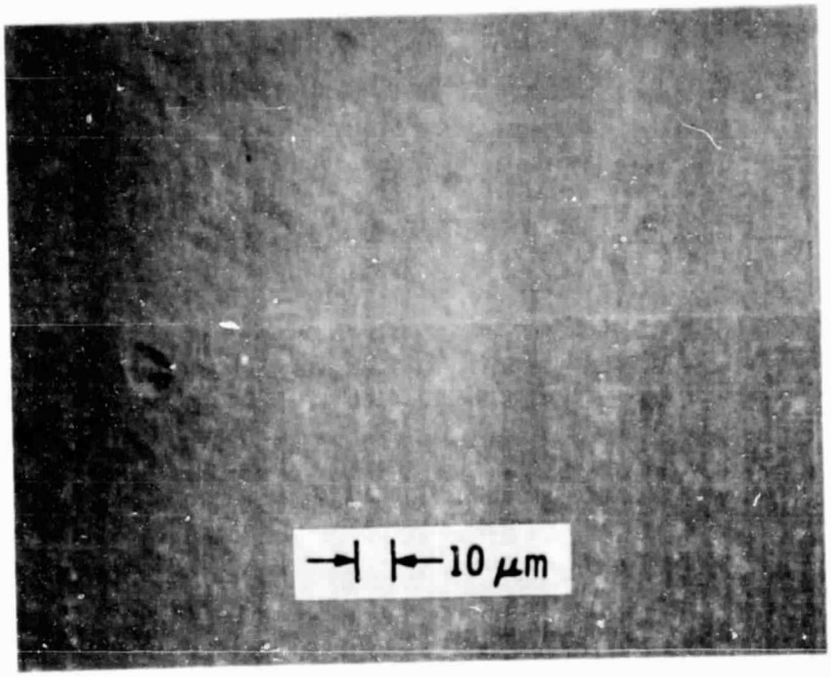


FIG. 3-24. Photomicrograph of the GaAs/Ge surface with $HF:HNO_3:H_2O_2:CH_3COOH$ = 9:4:4:20 etch prior to GaAs growth.

By using this improved method, an AM1 (ELH lamp) efficiency of 18.4% (17.5% when a 5% grid coverage is assumed) has been measured for an n^+/p GaAs/Ge solar cell of 2.36 mm^2 area, with the top n^+-layer thinned to about 1000 Å. The values of V_{oc}, J_{sc} and FF for this solar cell are 0.998V, 23.5 mA/cm^2 and 0.785, respectively. The light I-V curve of this solar cell is shown in Fig. 3-25. The excellent V_{oc} value for this cell indicates that the shunting due to auto-doping from the Ge was no longer a problem. The dark I-V characteristics of this cell are shown in Fig. 3-26. A double-exponential curve fitting using the expression of Eq. (1) was performed on the dark I-V characteristics. The values of the parameters obtained were: $J_{01} = 4.1 \times 10^{-19}$ A/cm^2, $J_{02} = 1.3 \times 10^{-8}$ A/cm^2, $n_1 = 1$, $n_2 = 2.85$. Further experiments need to be done using the new technique described above in subsection III-C, for the direct growth of the 500 Å-thick n^+ top layer of the GaAs cell, in order to avoid all anodization processes and thereby to achieve minimal values for the J_{02} and n_2 parameters.

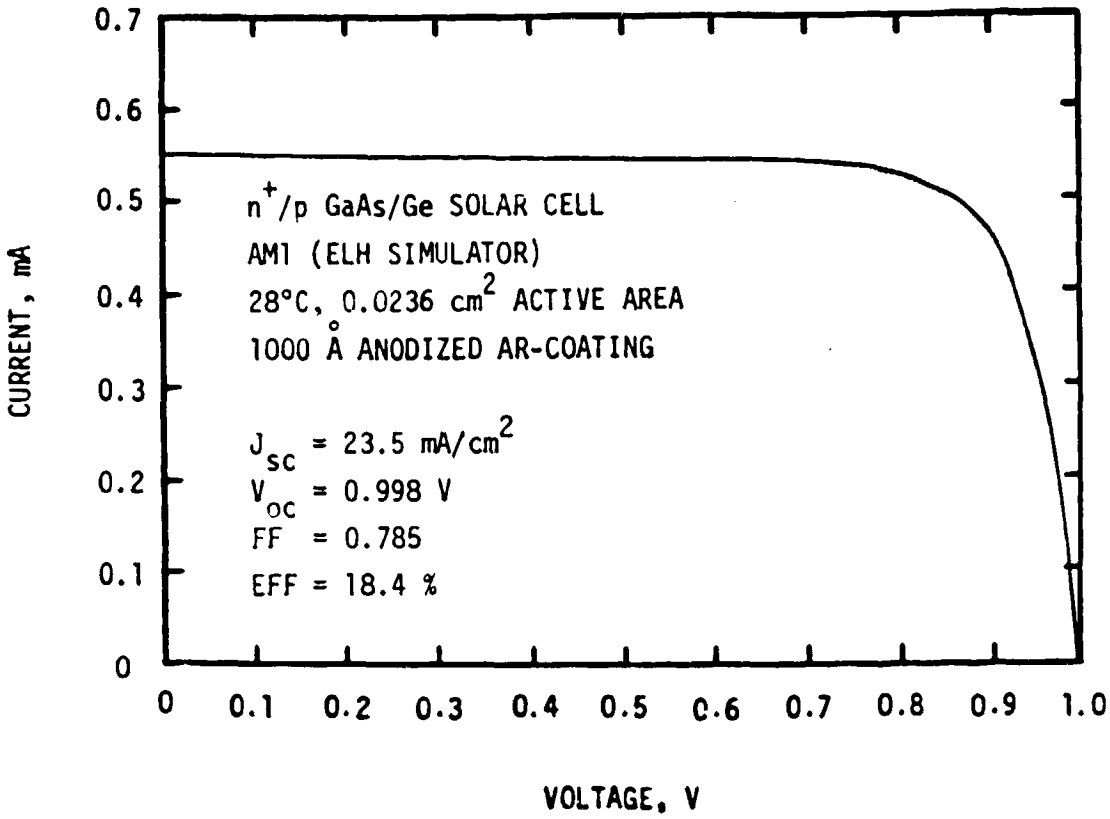


FIG. 3-25. Light I-V characteristics of an n^+/p GaAs/Ge solar cell.

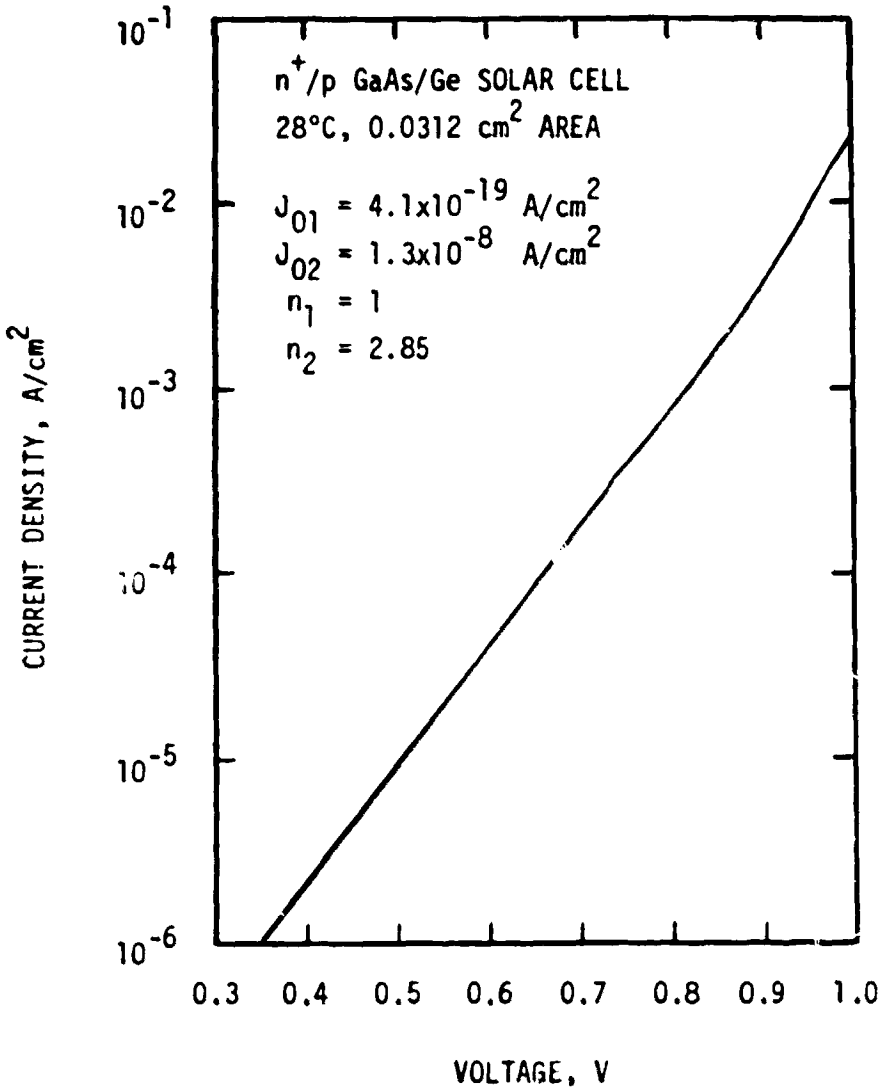


FIG. 3-26. Dark I-V characteristics of the solar cell used for obtaining the curve in Fig. 3-25.

SECTION IV

LOW-COST SUBSTRATE

The key to successful development of low-cost thin-film GaAs solar cells is the successful preparation of a low-cost substrate covered by a Ge interlayer having large crystallite size, suitable for hetero-epitaxial growth of a good quality GaAs epi-layer cell. The two structures used in this program for providing the low-cost substrate are: 1) recrystallized Ge on a passivated, low-cost conducting substrate, and, 2) hetero-epitaxial surface-processed Ge on a low-cost single-crystal Si substrate.

A. RECRYSTALLIZED Ge on TUNGSTEN (W)

1. Ge Growth on W Substrates

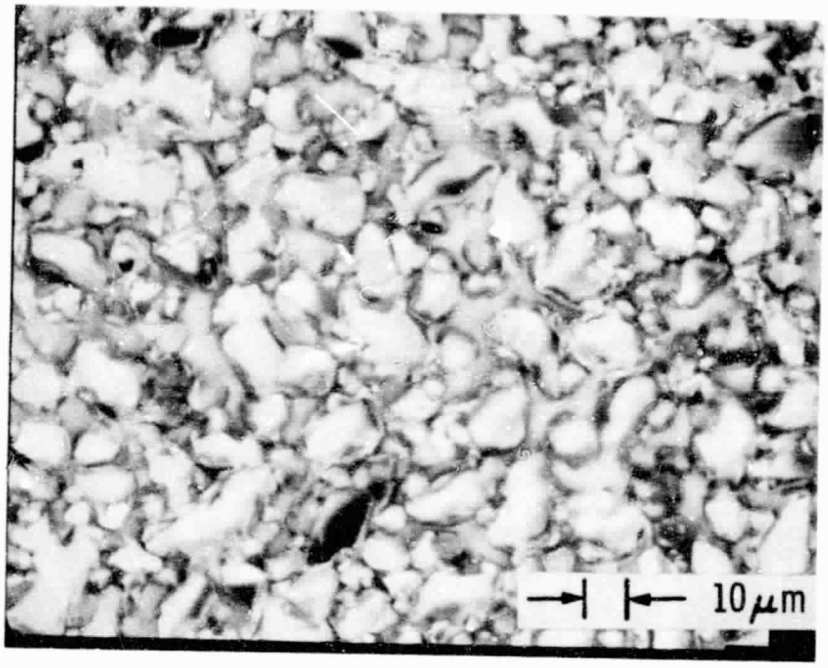
Prior to the use of low-cost steel substrate covered by a W passivation layer, a W substrate itself was used for Ge deposition to gain experience with the recrystallization of the Ge layer and the influence of the W on the physical properties of the Ge during and after recrystallization. The detailed discussion of laser recrystallization of Ge films deposited on W by the e-gun method was reported in the previous Final Report (Ref. 4-1). As described in that Final Report, e-beam deposition of Ge introduced Cu and Fe from the e-gun hearth into the deposited Ge films. In subsequent work, molybdenum (Mo) and W liners were also tried but without success due to excessive alloying with Ge which resulted in a very short useful lifetime of the liners.

Hence, during the early part of the current contract period, an investigation was conducted of Ge layer deposition on W substrates, employing arsine (AsH_3)

(as the n-type dopant), germane (GeH_4) and hydrogen (H_2) gas mixtures in the existing OM-CVD GaAs growth system. A growth rate of 0.09 to 0.16 micrometer/min for heavily-doped Ge was achieved with deposition temperatures of 700° to 800°C, a H_2 flow-rate of 3 liters/min, an AsH_3 mole fraction of 6×10^{-5}, and a GeH_4 mole fraction between 0.015-0.033. Photomicrographs of typical CVD Ge films grown at 800°C are shown in Fig. 4-1. The surface has a rough matte finish, with an average granule size of 10 micrometers. The addition of a thin silicon interlayer was found to be beneficial for promoting the bonding between the Ge layer and W substrate. Hence, pyrolysis of silane (SiH_4) was also performed using a growth rate of 0.1 to 0.5 micrometer/min at a deposition temperature of 1000°C. Contamination of the OM-CVD system after using SiH_4 and GeH_4 was indicated by the much higher residual doping concentration measured on subsequently undoped GaAs growths. Hence, a CVD system dedicated to the growth of Ge and Si from GeH_4 and SiH_4 sources was designed and constructed to avoid such cross-contamination. Figure 4-2 shows the front view of the completed Ge and Si CVD system. Successful growths of Ge films on W substrates were made using similar deposition parameters described above and with similar good results.

2. Electron-Beam Recrystallization of Ge/W

In the past, the recrystallization of Ge layers was done by rastering a focused Nd:YAG laser beam with a mirror scanner, resulting in a crystallite size of the order of millimeters. However, the poor energy utilization factor, high reflected power during the liquid phase of the Ge, and difficulties with



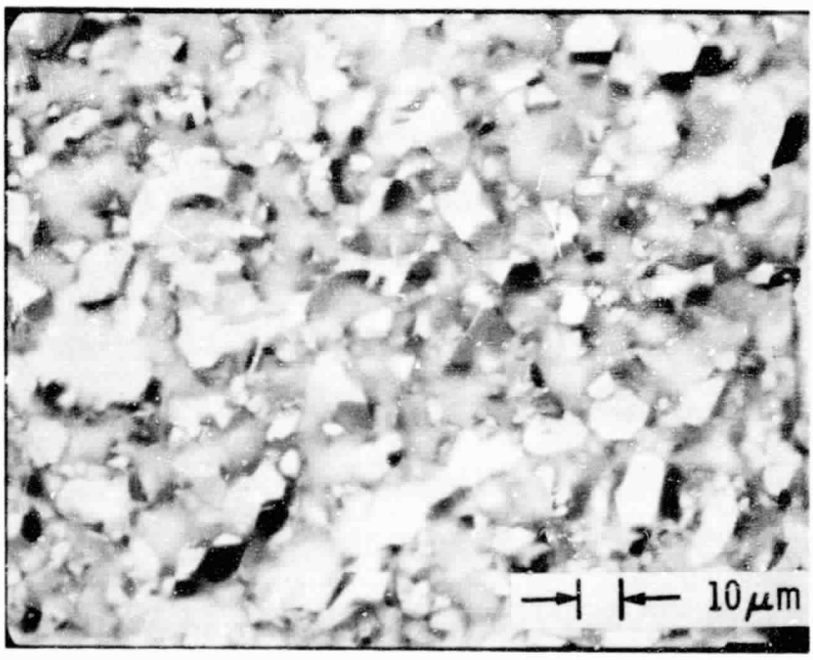


FIG. 4-1. Photomicrographs of typical Ge films CVD-grown at 800°C.

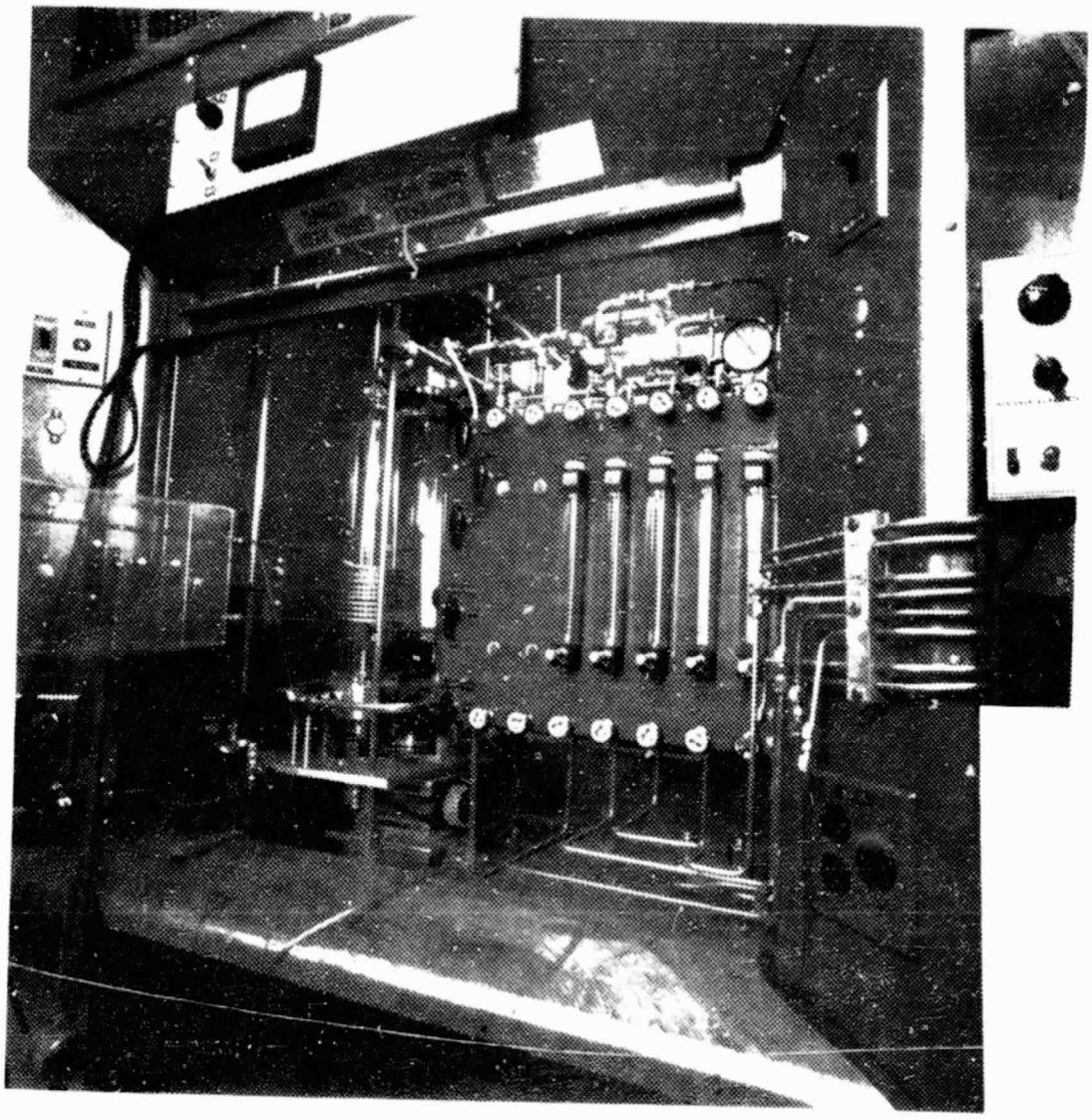


FIG. 4-2. Chemical vapor deposition system for growth of Si or Ge interlayer.

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fine focusing and beam steering imposed some limitations on the quality of the recrystallized Ge. A possibility for overcoming these limitations was to perform the recrystallization using an electron-beam system.

To study the feasibility of such an approach, a service purchase order was established with the Electron Beam Welding Co., Inc., Los Angeles. Subsequently, a sample holder with radiant background heating for use in the vacuum chamber of an e-beam welding machine (Model EB-312) was constructed. The temperature-calibration curve for background heating describing the temperature of the sample holder in vacuum as a function of heater current is shown in Fig. 4-3. Construction of the linear-sweep electronic apparatus and vacuum hardware to interface with the existing sine-wave-drive e-beam machine were also completed. Subsequently, experiments were performed in the vacuum chamber of the e-beam welding machine. Molten Ge films were obtained using the scanned electron-beam, forming a stationary, line-focused heated zone on a vacuum-deposited Ge film on a tungsten sheet, while moving the sample holder by a motorized translation stage inside the vacuum chamber. When a 30 keV scanned-electron beam was used, the minimum beam current required to melt the Ge film was about 0.1 mA, using a sample background temperature of 900°C. Due to the interaction between the scanned electron beam and the magnetic field created by the A.C. background-heater current (about 15 A, r.m.s.), an uneven molten surface was obtained. Eliminating this problem simply involves using D. C. heating or a non-inductive heater winding configuration for the background heater.

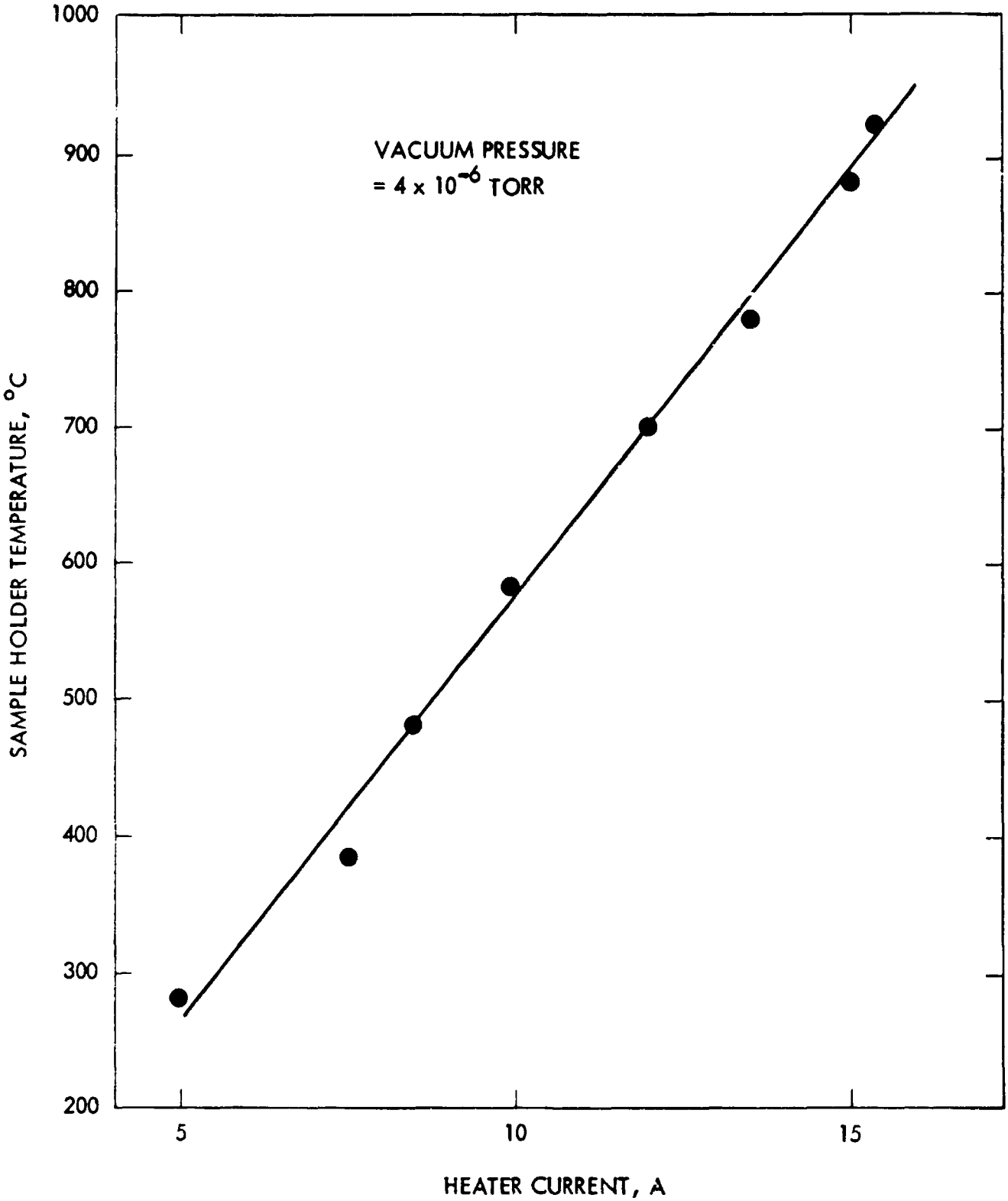

FIG. 4-3. Dependence of sample-holder temperature on heater current.

B. Ge EPI-INTERLAYER ON SINGLE-CRYSTAL Si

During this reporting period, the work in the photovoltaic community has not been successful for developing 15% efficient polycrystalline thin-film GaAs solar cells. Efficiencies this high would probably be needed, for economic viability, given the costs of the materials and processes that are likely to be required. Furthermore, suitable substrates other than those studied, having the required physical properties and low cost also have not identified. The deleterious effects of grain boundaries on solar cell electrical properties are considerable, whether the potential barrier is a grown p/n junction or an oxide-enhanced Schottky barrier (AMOS). Excess leakage currents of at least two types are the primary loss mechanisms, leading to low values of V_{OC} and FF. In addition, the relative roughness of poly-GaAs films, whether grown on recrystallized Ge interlayers or directly on foreign substrates, can lead to serious practical problems in cell and module fabrication. This is particularly true for "sensitive" structures such as the AMOS or shallow n^+/p homojunction. The electrochemical or liquid-junction structure utilizing poly-GaAs has, perhaps, the greatest chance of overcoming these problems. However, stable, high-efficiency, low-cost GaAs cells using polycrystalline materials have yet to be demonstrated.

Hence, a new approach which can circumvent most of the problems by utilizing single-crystal structures is needed if GaAs is to play a significant role in terrestrial photovoltaics. Because the cost of single-crystal Si substrates will be dramatically lowered through the efforts of the JPL Low-Cost Solar Array (LSA) Project and its contractors, an approach which would involve single-crystal GaAs films deposited on Si substrates was initiated at JPL. This new approach uses Ge as an interlayer between GaAs and Si, to reduce the effects of both lattice and thermal-expansion mismatches between them. In this

approach, Si is not being used as an active semiconductor. Hence, the use of lower-grade Si wafers with higher-impurity contents should be feasible provided that good crystallinity is preserved. Employing this approach, the cost of the finished single-crystal GaAs solar cell could be significantly reduced. Our progress with this approach will be discussed in the following three subsections.

1. Ge Epi-interlayer Growth on Si Substrates

Deposition of the Ge epi-interlayer on Si wafer substrates was made by pyrolysis of germane rather than halide compounds of Ge. The reasons for this are similar to those used to justify using metal-organic systems in place of halide or hydride systems: 1) lower growth temperatures, 2) absence of HCl vapor etch back - particularly of the substrate, 3) single-temperature zone, and 4) cold-wall reactor providing for reduced maintenance and higher material utilization. Initially, helium (He) instead of more conventional H_2 was used as the carrier gas on the expectation of being able to successfully grow good quality, tightly adherent epitaxial layers of Ge on Si wafers, at even lower temperatures, and thus minimize the effect of thermal coefficient mismatch upon final cooling to room temperature. Previous investigations with SiH_4 alone (Ref. 4-2) or GeH_4 alone (Ref. 4-3) had shown that He as a carrier gas does allow lower growth temperatures for a fixed growth rate or higher rates for a fixed temperature. For example, a crystalline homo-epitaxial growth of Si from SiH_4 was obtained at 800°C with He as compared to 910°C with H_2 (Ref.4-2). By comparison, typical growth temperatures with H_2 as carrier gas at atmospheric pressure are about 1200°C with $SiCl_4$, about 1150°C with $SiHCl_3$, and about 1000°C with SiH_2Cl_2. One study has demonstrated

the growth of single-crystal Si from SiH_4 using N_2 as the carrier gas with a growth temperature as low as 780°C (Ref. 4-4). Other experiments with N_2, He or Ar as carrier gas are reviewed by Bryant (Ref. 4-5), where single-crystal Si growths were obtained at temperatures as low as 700°C and growth rates about 0.1 micrometers/min.

The CVD-Ge growth on Si was made in the same system as the CVD deposition of Ge on W described in Section IV.A.1. An additional HCl gas line was added for in-situ etching of the Si substrate prior to growth, and two lines for p- and n-type dopants were provided for subsequent use. Although the Si substrate and Ge interlayer are photovoltaically inactive, the doping polarity of each must be the same as that of the GaAs base layer to avoid a reverse-biased junction between them.

During the initial growth procedure, the graphite susceptor was out-gassed in He at 1000°C for several hours. Unfortunately, poor surface morphology for Ge epitaxial films on Si with (111) orientation was obtained at a growth temperature of about 650°C with a He gas flow rate of 4500 cc/min and an admixture of GeH_4/He gas (5:95) at a flow rate of 7.7 cc/min. No dopants were added at that stage. The surface morphology of the Ge layer was examined by optical and scanning electron microscopy. Figures 4-4 and 4-5 show SEM photographs at 2000X and 6000X, respectively. The surface appears to be quite rough, although it is shiny (though not mirror-like) to the naked eye. The degree of crystallinity of the Ge layer was investigated by Laue back-reflection and transmission as well as by X-ray diffraction. Figure 4-6 shows a back-reflection photograph which indicates a high degree of (111) orientation. Several accelerating voltages from 15 to 45 keV were used to verify that the pattern obtained was due to the Ge layer and not the Si substrate. However, although X-ray diffraction

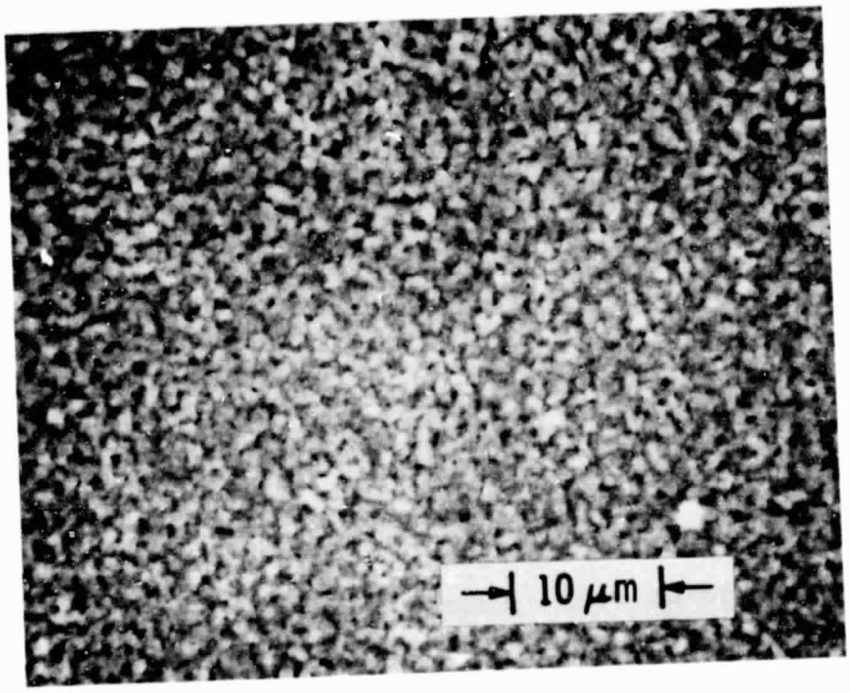

FIG. 4-4. SEM photomicrograph at 2000X of a Ge film grown by CVD on (111) Si at 657°C with H_2 carrier gas.

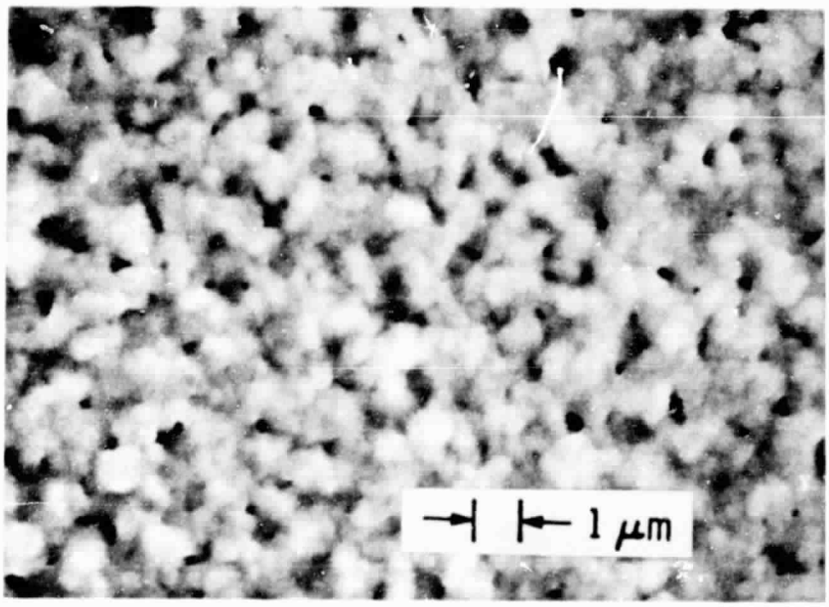

FIG. 4-5. SEM photomicrograph at 6000X of the same Ge films as used for Figure 4-4.

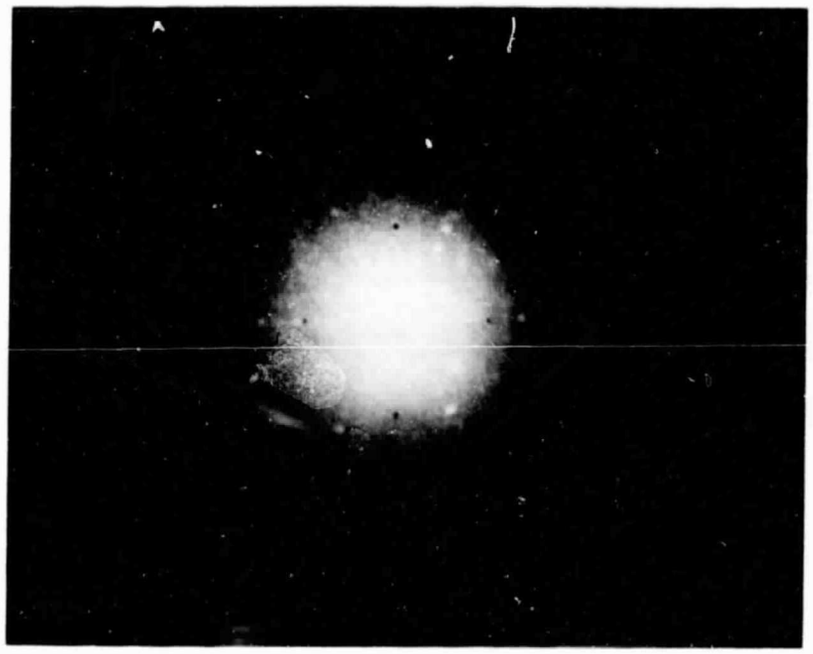

Fig. 4-6. Laue back-reflection photograph of the same film as used for Fig. 4-4.

data showed a preponderance of the (111) orientation, very weak reflections from two or three other orientations were also present.

Work was continued for several months, but without success, to determine the growth conditions needed to promote better nucleation, better single-crystal characteristics and smoother surface for the heteroepitaxy of Ge on Si using He as carrier gas.

Subsequently, H_2 was used as the carrier and dilutant gas for the GeH_4 to see if the Ge-interlayer grown on Si could be grown with better crystallographic characteristics and surface morphology. Indeed, successful growth of a Ge interlayer was achieved with a high-quality surface and with single crystallinity. During this study, various growth temperatures ranging from 700°C-800°C, GeH_4 mole fractions ranging from 8×10^{-4} to 4×10^{-3} and a hydrogen flow rate of 5000 cc/min were employed. The best surface morphology of the as-grown Ge films was achieved at growth temperatures between 700°-750°C for all the GeH_4 mole fractions used in our experiment. X-ray diffraction measurements were employed to examine the crystallinity characteristics of Ge epi-layers grown on the Si substrates. Figure 4-7 shows a typical x-ray diffraction chart obtained on a Ge/Si sample grown at 700°C. The vertical axis indicates the relative intensity of the diffracted x-ray signal and the horizontal axis indicates the 2θ angle value in degrees (θ is the angle between the plane of the sample surface and the incident x-ray radiation). The peaks #1 and #3 are due to Si(400) planes associated with Cu-K_α and Cu-K_β x-ray radiation used in this experiment, respectively. In addition, the peaks #2 and #4 are due to Ge(400) planes associated with Cu-K_α and Cu-K_β radiation, respectively. The absence of any other peaks through the range of 20°-76° indicates that the (100) Ge-film has been epitaxially grown on the (100) Si substrates. In Fig. 4-8, higher angular resolution and lower ensitivity are used to reveal the details

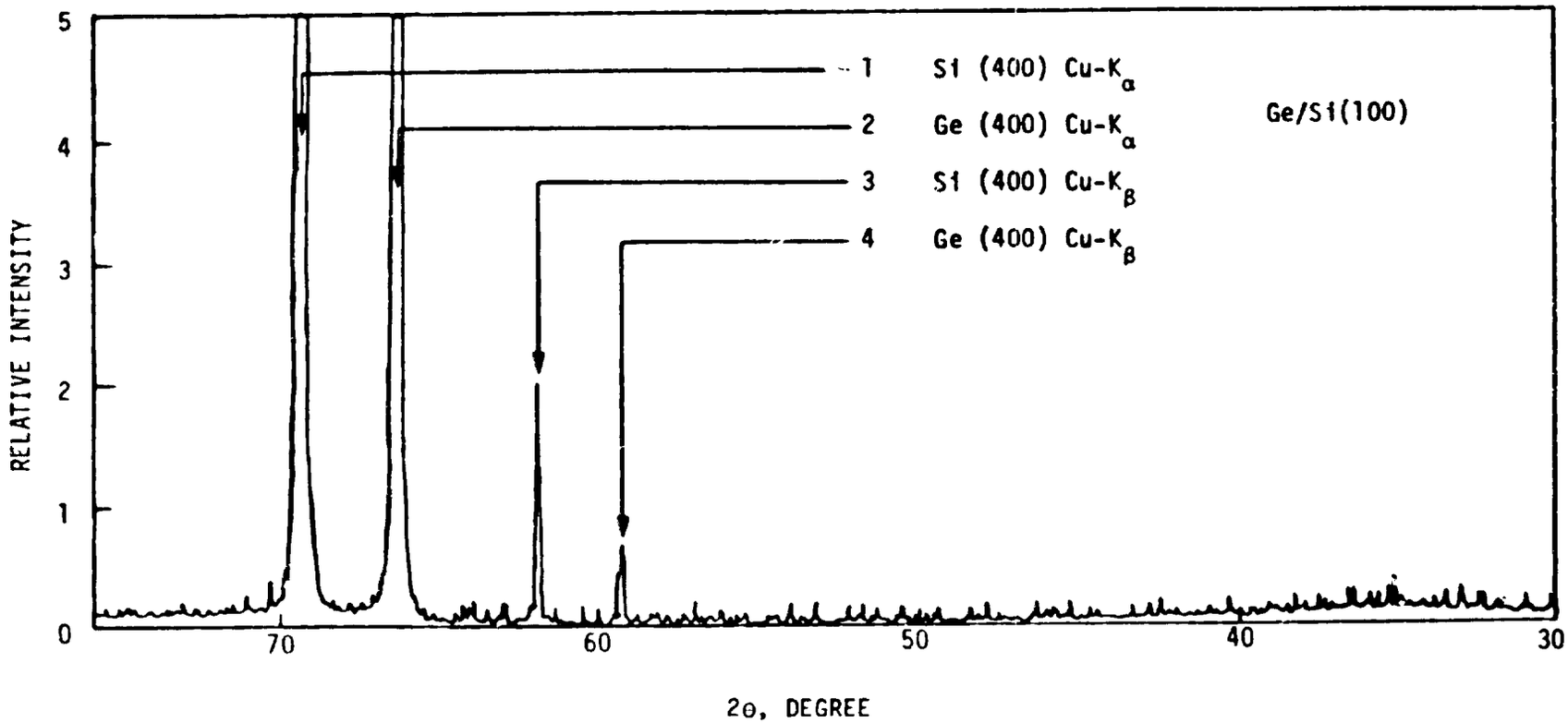

Fig. 4-7. Typical X-ray diffraction chart obtained on a Ge/Si sample grown at 700°C in H_2 carrier gas.

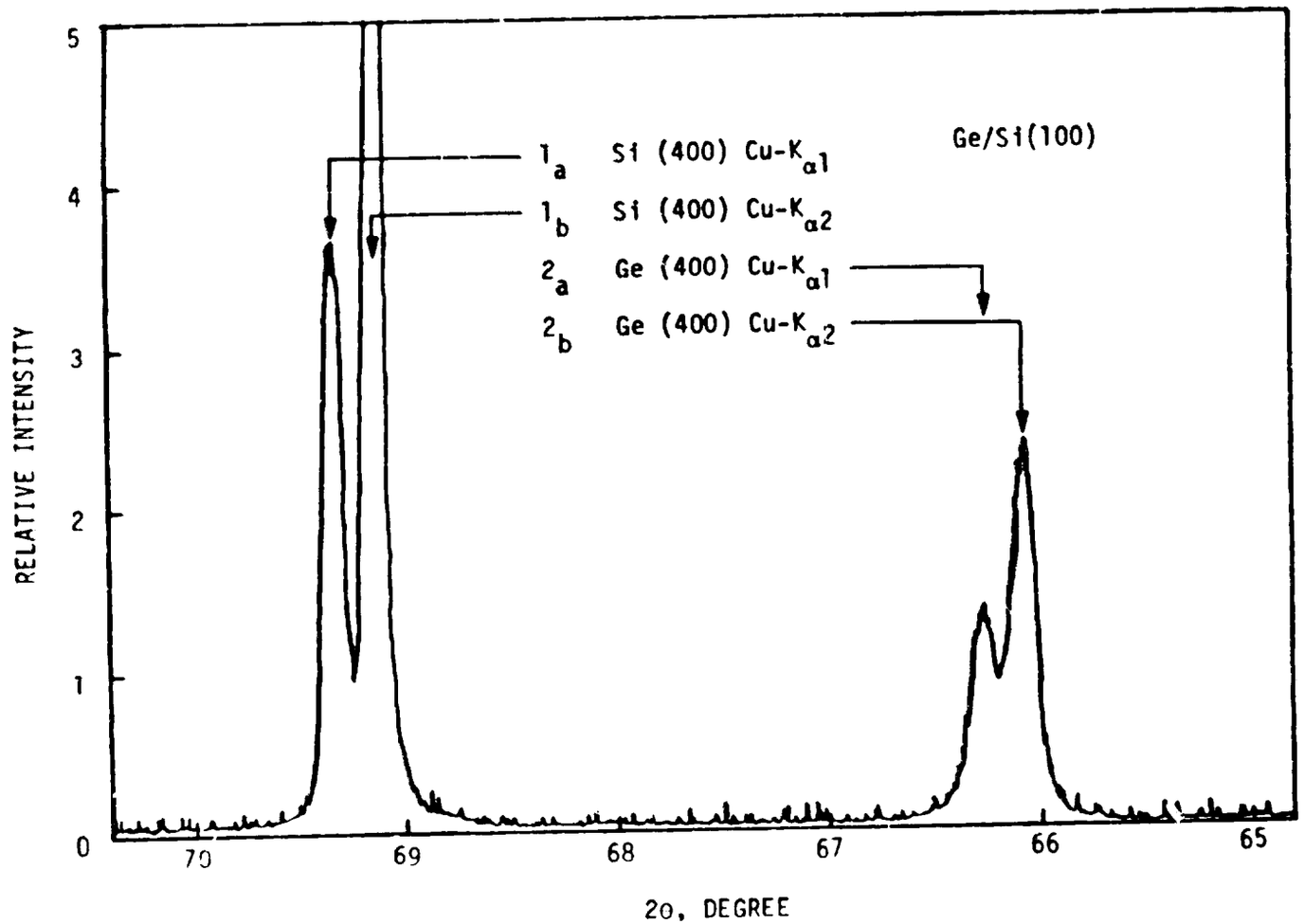

Fig. 4-8. X-ray diffraction chart with high angular-resolution and low sensitivity obtained on the same sample used in Fig. 4-7.

of the peaks #1 and #2 which are off-scale in Fig. 4-7. The Ge(400) signal has been split into two peaks, 2a and 2b, and are associated with the Cu-$K_{\alpha 1}$ and Cu-$K_{\alpha 2}$ radiations, respectively.

For examining the surface morphology of the as-grown Ge epi-layers on Si, the scanning electron microscope (SEM) was employed. A SEM photomicrograph (2700x) of a typical Ge film grown at 700°C is shown in Fig. 4-9. This figure shows that although the surface looks rather shiny to the naked eye, the surface contains many microscopic pits and requires processing. The surface morphology of these Ge deposits can be improved by laser-annealing or a mechanical-chemical polishing technique as discussed in the next two subsections (IV.B.2 and IV.B.3).

2. Pulsed Laser Annealing of Ge/Si

Since there exist significant differences in lattice constants and thermal-expansion coefficients between Ge and Si, a very large density of dislocations may be expected. Consequently, an annealing step for the inter-layer may be desirable before the GaAs growth is initiated so that the majority of the defects which intersect the growth surface do not, in turn, induce similar defects in the GaAs during the initial stages of growth In addition when rough surface morphology of the as-grown Ge film is obtained, the use of pulsed-laser annealing may promote smoother surface finish by rapid surface melting and regrowth. A review of the considerable literature published these past several years on laser and electron beam processing (mostly on Si material) indicates that pulsed energy-beam recrystallization is potentially a viable process step for obtaining nearly defect-free surfaces on the outermost Ge layer.

It is now known that there are basically two different recrystallization modes, depending on the dynamics of the energy beam (Refs. 4-6 and 4-7). Most

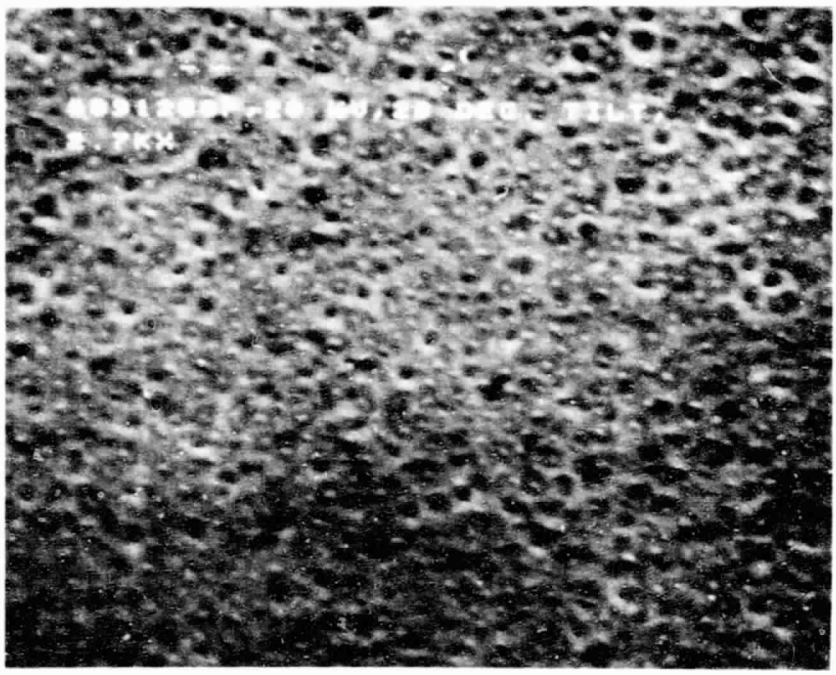

Fig. 4-9. SEM photomicrograph (2700X) of a typical Ge film grown at 700°C on (100) Si substrate.

data relate to the case of amorphous, ion-implanted layers on high-quality crystalline substrates, but the results are probably general in nature. In the case of scanned CW laser beams (usually the Argon-ion laser at 5145 Å and elevated substrate temperatures), the regrowth mechanism is solid-state recrystallization - similar to that obtained by furnace annealing. Typical dwell times for the energy beam are of the order of milliseconds, and perfection of the recrystallized layer is dependent on heating to a depth sufficient to allow regrowth from the interface region.

The mechanism for pulsed laser beams (usually Q-switched or mode-locked Nd:YAG or ruby lasers) or pulsed electron beams where the dwell time is of the order of tens to hundreds of nanoseconds, is clearly the formation of a thin molten layer followed by rapid recrystallization. The references are far too numerous to cite here, but several Proceedings of Symposia are very useful (Ref. 4-8). The recovery of crystalline perfection in this mode is related to the extremely high recrystallization velocities (as high as 1 m/sec), which are higher than the climb velocity for dislocations. Complete removal of misfit dislocations and other defects have been demonstrated for the case of imperfect crystalline Si, i.e., no amorphous regions, which is relevant to the deposited Ge interlayer in this program (Refs. 4-9 and 4-10). The latter work also demonstrated the permanence of the defect removal after subsequent thermal anneals up to 1100°C, where the misfit dislocations were induced by high concentrations of a dopant, such as phosphorus, with smaller ionic radius than Si. Among the different schemes used, pulsed-laser annealing on Si and GaAs has been found to give better results in many cases than the use of CW lasers. The pulsed-laser method has been reported not only to crystallize an amorphous layer, but also to remove displacement damage (Refs. 4-11, 4-12) and crystal

imperfections due to loops and precipitates (Refs. 4-13, 4-14). Hence, the pulsed Nd:YAG laser was selected for use in the annealing/recrystallization experiment.

During the period of this program, modification of our existing CW Nd:YAG laser to a pulsed operation was completed. The modified pulsed-laser system consists of a Quantronix Model 114-2 Nd:YAG laser (the basic laser unit), a Model 305A spatial-mode selector (to allow for single TEM_{00} mode operation), a Model 317 polarizer/shutter assembly (to linearly polarize the laser beam for improved output stability by eliminating mode competition between randomly polarized modes), a Model 301 acousto-optical Q-switch system (for pulsed-mode operation with the pulse-repetition rate adjustable from 0-100 kHz), a General Scanning Corp. Model G-100PD mirror scanner with Model CCX-102-1 scanner control unit, a motorized vacuum-tight sample chamber, and the usual optics and pulse-power measuring instrumentation.

The basic operating mode of the laser annealing system involves several steps. The output beam of the pulsed Nd:YAG laser passes through an optical system which focuses the laser beam onto a small area on the sample surface to yield the necessary energy density. The focused beam will be deflected by the mirror scanner to form an annealed-line region on the substrate. Simultaneously, the motorized sample chamber continuously translates the substrate in the direction perpendicular to the annealed line. This results in appropriate overlapping between annealed-line regions, until the entire sample surface has been exposed. The advantages of using the combination of mirror scanner and motorized translation stage are : 1) elimination of the pin-cushion distortion of a dual mirror-scanner system, 2) allowance for faster scanning speeds as contrasted to the dual-motorized translation-stage system because

of lower inertial mass, and 3) the probability of longer operating lifetime relative to that of the dual-motorized system.

The use of a repetitively Q-switched Nd:YAG laser in the annealing system is preferred, due to its stability compared to pulsed-YAG or ruby lasers (Ref.4-15). Repeatability is probably the most important laser parameter, because in laser annealing, a carefully controlled temperature distribution must be achieved. Energy densities below a threshold value will not have the desired effect, whereas too high an energy density will cause surface damage. Thus, there is a "window" region of energy densities for optimum laser annealing. The pulse-to-pulse repeatability for the acousto-optical Q-switched Nd:YAG laser is about 5%, with a maximum pulse energy of about 1 mJ and a full-width-at-half-maximum (FWHM) of about 110 ns.

To restrict melting to a shallow depth, it is necessary that the pulse width be small compared to the thermal diffusion time, t_d (Ref. 4-15). Therefore, this requires that

$$t_d = \rho c Z^2/k, \qquad (2)$$

where ρ, c and k are the density, specific heat and thermal conductivity, respectively. For solid Ge, $\rho = 5.2$ gm/cm^{-3}, c = 0.096 cal gm^{-1}K^{-1}, and k = 0.174 Watt cm^{-1}K^{-1} at 937°C, the melting temperature of Ge. Hence, the heating depth (Z) is calculated to be about 2 micrometers with a thermal diffusion time (t_d) of 110 ns for Ge at 937°C.

The appropriate energy density required for pulsed-laser annealing of Ge can presently only be estimated because of insufficient information in the open literature regarding the application of this procedure to Ge. In general, the energy density required for such annealing of semiconductor substrates is

related to the melting point of the substrate material, since melting of the surface layer must precede the fast recrystallization. From numerous studies reported in the literature, the energy density needed for laser annealing was found to be 0.2 to 0.3 J cm^{-2} for GaAs (melting-point of 1238°C) and 1 to 2 J cm^{-2} for Si (melting-point of 1410°C). Hence, it was estimated that the energy density needed to laser-anneal Ge (melting-point of 940°C) is less than 1 J cm^{-2}. This estimate matches very well with our experimental observation, which will be discussed later.

After the optimum energy density I_0 for laser annealing is experimentally determined, the spot size D_0 (diameter of the 1/e power point) can be determined by the following expression:

$$D_0 = (4E/\pi I_0)^{1/2}, \tag{3}$$

where E is the total energy per laser pulse. In this case, E = 1 mJ, and for an upper limit of I_0 = 1 J cm^{-2}, D_0 is calculated to be 347 micrometers. For a 2 cm x 2 cm-annealing area, with the Nd:YAG laser operating at 800 pps (the stability of pulse will deteriorate and the energy per pulse will decrease when operating at higher frequencies), and with 50% overlapping for both coordinates during pulse annealing, the scanning frequency for the mirror scanner and the scanning speed for the motorized translating stage are calculated to be 7.1 Hz and 1.27 mm s^{-1}, respectively. Hence, it should take only 15.8 seconds to anneal a 2 cm x 2 cm-Ge sample.

At the time our modified pulsed Nd:YAG laser system was completed, an opportunity occurred for us to be able to use a large pulsed Nd:YAG laser

system available at the Lockheed Corp., Sunnyvale, California. The output energy-per-pulse of this laser system is large enough to anneal the entire 2 cm x 2 cm wafer area with an energy-density up to several J cm^{-2}, using a beam homogenizer. The possible lateral stress induced due to localized heating by the small scanned laser-beam can thus be avoided. Hence, we decided that the experimental work in annealing/recrystallization of the Ge interlayers should first be performed using the laser system at the Lockheed Corp. This laser system consisted of a laser oscillator followed by three stages of laser-amplifiers operating at a wavelength of 1.06 micrometers with a pulse width of less than 150 ns. The output laser beam was passed through a 30mm-diameter quartz optical beam homogenizer to improve the uniformity of the laser radiation power-density upon the samples being annealed.

Systematic experiments were first performed on (100) Ge substrates with both polished as well as rough surface finishes to estimate the approximate energy-density needed in the actual annealing of Ge/Si samples. During this experiment, energy densities ranging between 0.09 J cm^{-2} to 1.14 J cm^{-2} in more than twenty values were used. It was found that damage was readily visible at high energy densities, with the creation of excessive surface pits. The damage-threshold energy-densities for visible damage are about 0.39 J cm^{-2} and 0.19 J cm^{-2} for polished and rough surface Ge, respectively. The lower value for the rough surface Ge is expected, because the laser energy is more readily absorbed by the rough surface due to the light-trapping effect.

Based on the results obtained above, the damage-threshold energy-density of the Ge/Si sample studied was estimated to be greater than that for the polished Ge wafer (0.39 J cm^{-2}) because Si has a larger thermal-conductivity than Ge.

Subsequently, systematic annealing experiments were performed on epi-Ge/Si samples with energy-densities ranging from 0.35 to 0.79 J cm^{-2}. Much improved surface morphology was obtained for the annealed Ge-films on Si substrates as compared to the as-grown Ge-films. The surface morphology of the annealed Ge epi-layers on Si substrates was examined using the SEM. A photomicrograph (7000X) of a Ge epi-layer annealed at a moderate average energy density of about 0.34 J cm^{-2} is shown in Fig. 4-10. This figure shows that the annealed Ge epi-layer possesses a smoother surface morphology but has similar surface micro-pit density as compared with the unannealed Ge-film shown in Fig. 4-9. Further increase in the laser energy density to about 0.49 J cm^{-2} leads to much greater improvement in the surface morphology of the Ge/Si substrate. A SEM photomicrograph (7000X) of such a sample is shown in Fig. 4-11. This figure shows that the further increase in laser energy density has eliminated many surface micro-pits (area density reduced about 3X) and also has reduced their diameter from about 8000 Å to less than 4000 Å as contrasted to the appearance of the as-grown and lightly annealed samples shown in Figs. 4-9 and 4-10, respectively. The size of the surface micro-pits would now be small enough for subsequent GaAs OM-CVD growth to form a continuous epi-layer on the Ge. Under these conditions, further processing for improving the surface morphology of the Ge epi-interlayer (the mechanical-chemical polishing as discussed in the next section) could be eliminated. The surface micro-pit densities for the samples

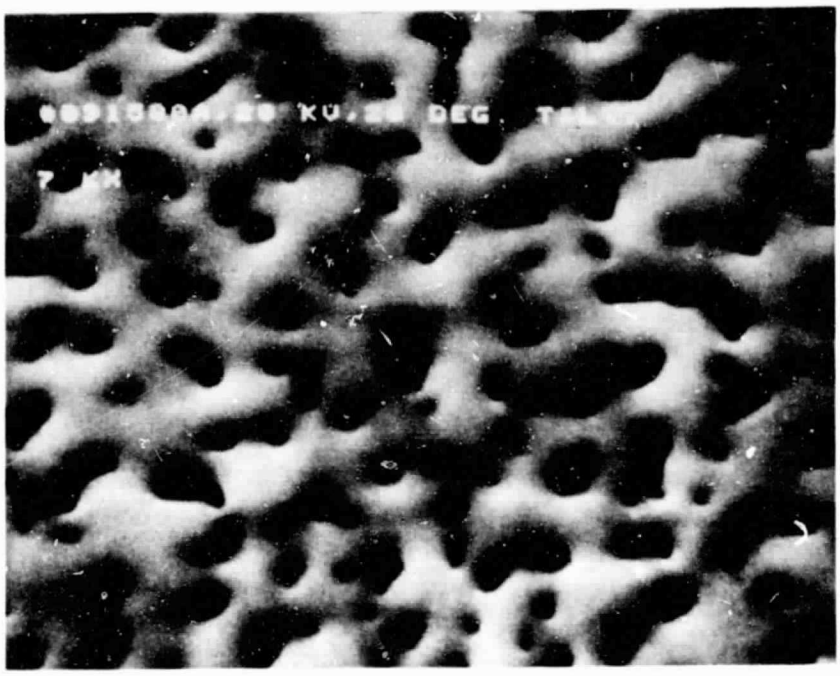

Fig. 4-10. SEM photomicrograph (7000X) of a Ge/Si sample annealed at an average energy-density of about 0.34 J cm^{-2} (Ge film grown at 700°C).

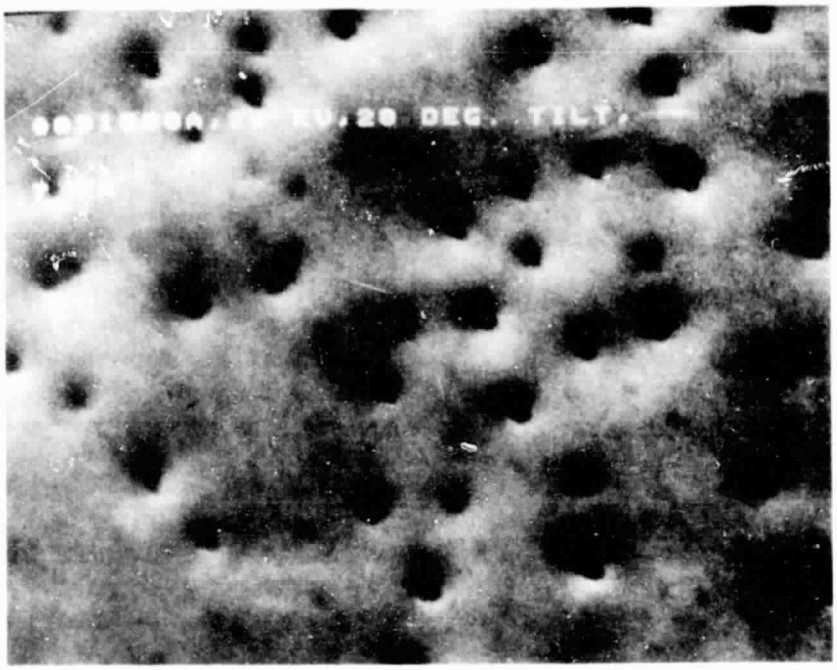

Fig. 4-11. SEM photomicrograph (7000X) of a Ge/Si sample annealed at an average energy-density of about 0.49 J cm^{-2} (Ge film grown at 700°C).

shown in Figs. 4-9, 4-10 and 4-11 were found to be about 6×10^7, 6×10^7 and 2×10^7 cm^{-2}, respectively. A surface micro-pit density of an order of magnitude less, about 6×10^6 cm^{-2}, was achieved on one Ge/Si sample with a laser-beam energy density of about 0.64 J cm^{-2}. The SEM photomicrograph (2700X) of this sample is shown in Fig 4-12.

To examine the crystallinity of the annealed samples, x-ray diffraction measurements were performed on the samples. It was found that after laser annealing, the double peak of Ge(400) due to Cu-$K_{\alpha 1}$ and Cu-$K_{\alpha 2}$ had been broadened into one single peak (#2) in the x-ray diffraction chart (Fig. 4-13) of the annealed Ge/Si substrate. This broadening suggests that there might be significant alloying between Ge and Si at the interface during the molten phase of the Ge epi-layer in the laser-annealing process.

Since the thermal mismatch between Ge and Si is significant, there is serious concern as to whether such an epi-layer/substrate bond would survive exposure to rapid and large temperature excursions. Therefore, several Ge/Si samples were directly immersed in liquid nitrogen and withdrawn to room temperature several times. It is significant to note that after the samples (each with about 1 micrometer Ge-interlayer) were subjected to such cycles, no evidence of film peeling and/or surface cracking was observed, indicating that the films were tightly adherent.

3. GaAs/Ge Epi-interlayer/Si

To prove the suitability of the Ge/Si substrate for the subsequent epitaxial deposition of GaAs, OM-CVD growth of GaAs on surface-processed Ge/Si substrates was attempted. A relatively thick (about 5 micrometers) undoped epi-layer of Ge was CVD-grown on (100) Si, then carefully mechanical-chemically polished to a smooth finish. A thin epitaxial layer of GaAs, bright and shiny,

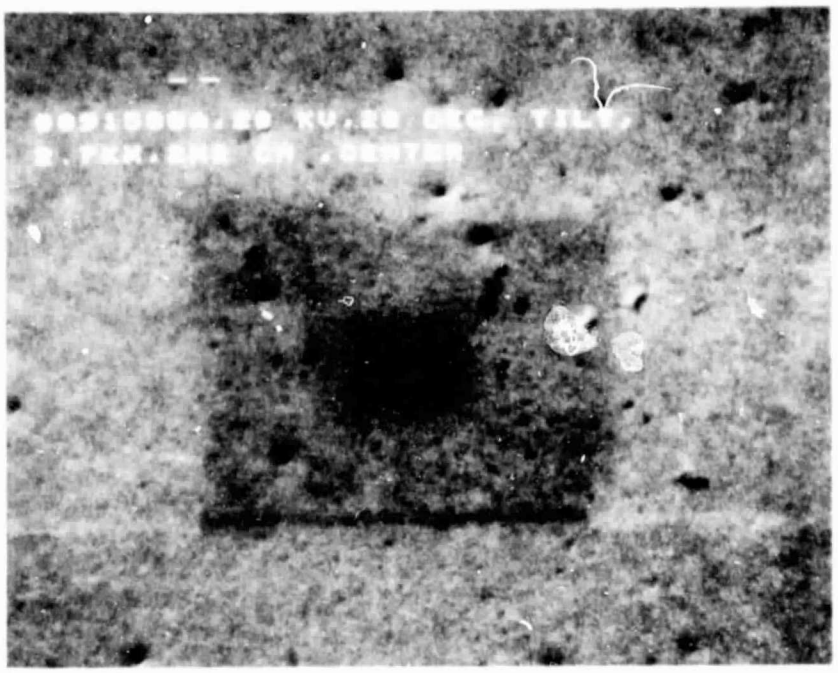

Fig. 4-12. SEM photomicrograph (2700X) of a Ge/Si sample annealed at an average energy-density of about 0.64 J cm^{-2} (Ge film grown at 700°C).

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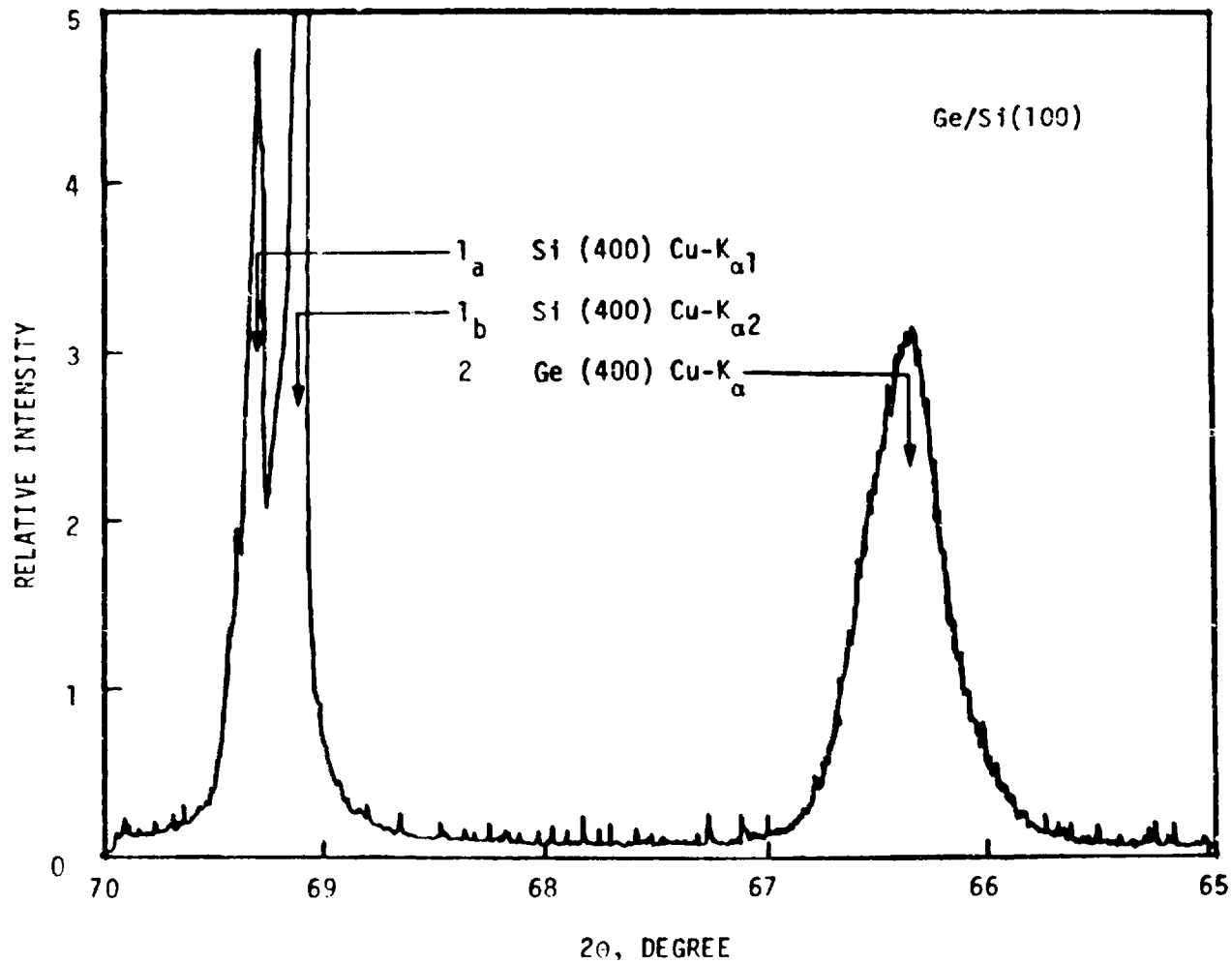

Fig. 4-13. X-ray diffraction chart of the annealed Ge/Si substrate.

was successfully grown on the polished Ge layer, exhibiting a very uniform appearance. X-ray diffraction measurements indicated that both the Ge-interlayer and the GaAs layer were completely single crystal, having the same (100) orientation as the Si substrate. This is the first report of the fabrication of such a structure having a quality suitable for making solar cells. An x-ray diffraction chart of such a sample is shown in Fig. 4-14. Note that because of the top GaAs layer, the Si x-ray signals are much weaker than the GaAs or Ge signals (GaAs and Ge signals are nearly identical and not resolvable by the x-ray instrument used in this experiment) as compared to that in the x-ray diffraction chart of Ge/Si shown in Fig. 4-7 or 4-13. The thickness of the GaAs and Ge epi-layers were determined by SEM measurements of the cleaved cross section of the GaAs/Ge/Si structure. A SEM photomicrograph of such a sample is shown in Fig 4-15, from which the layer thicknesses for GaAs and Ge are found to be about 4 and 1 micrometers, respectively.

The surface morphology of the GaAs/Ge/Si sample was also studied by the SEM. Figure 4-16 shows a SEM photomicrograph (2700X) of the GaAs/Ge/Si sample. Other than relatively few surface micro-pits (density about 6×10^5 cm^{-2}) a very smooth surface is evident as compared to any samples discussed in the previous two sections.

This encouraging result demonstrates that the GaAs/Ge/Si structure physically can be successfully fabricated. Further research activity will first be conducted with a p-doped Ge epi-interlayer (instead of the undoped one) to facilitate the evaluation of the electronic properties of this structure. Subsequent experiments will be directed toward optimizing the structure for the fabrication of solar cells.

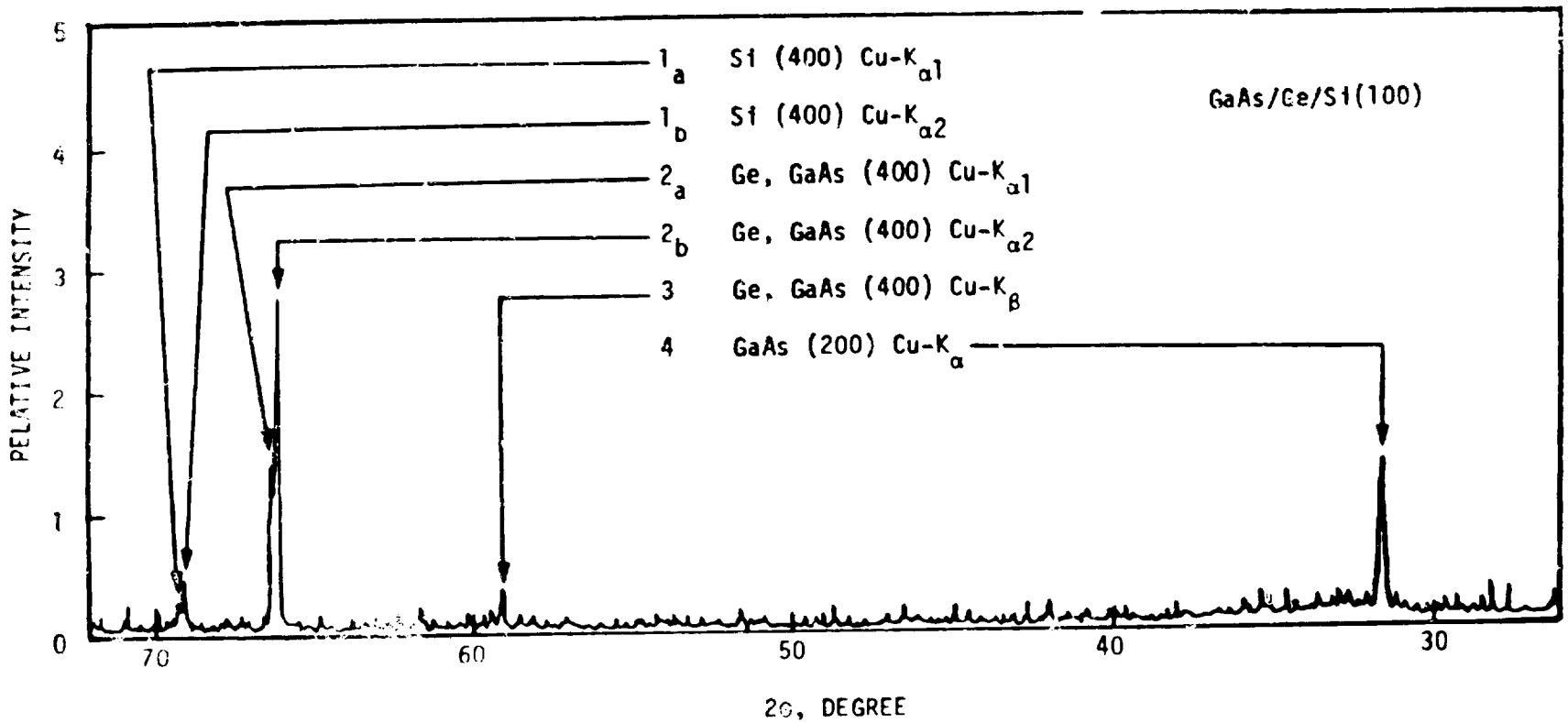

Fig. 4-14. X-ray diffraction chart of an epi-GaAs/epi-Ge/Si sample.

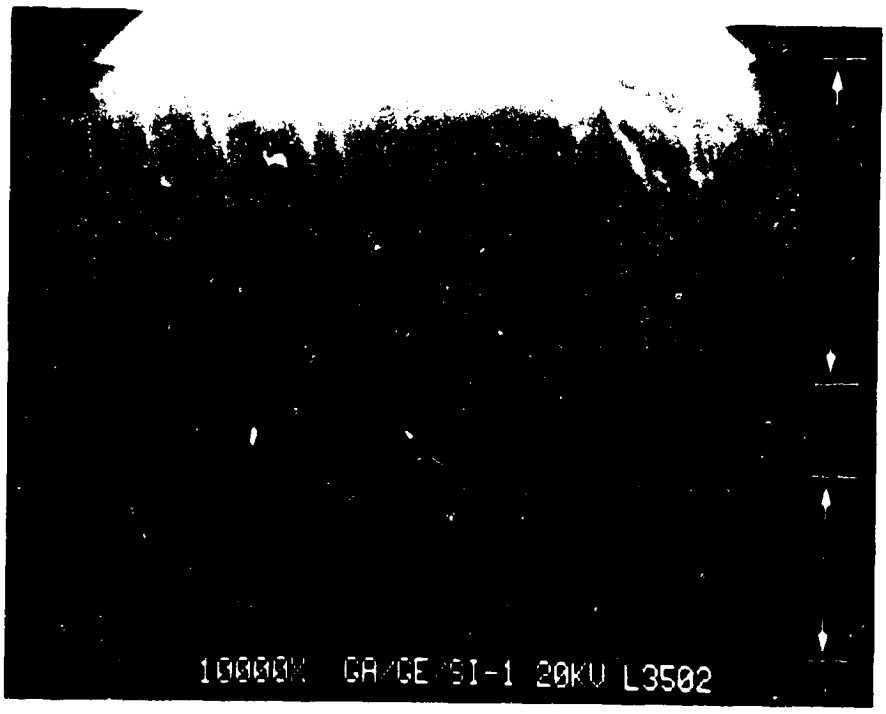

Fig. 4-15. SEM photomicrograph (10,000X) of the cleaved cross-section of the GaAs/Ge/Si structure.

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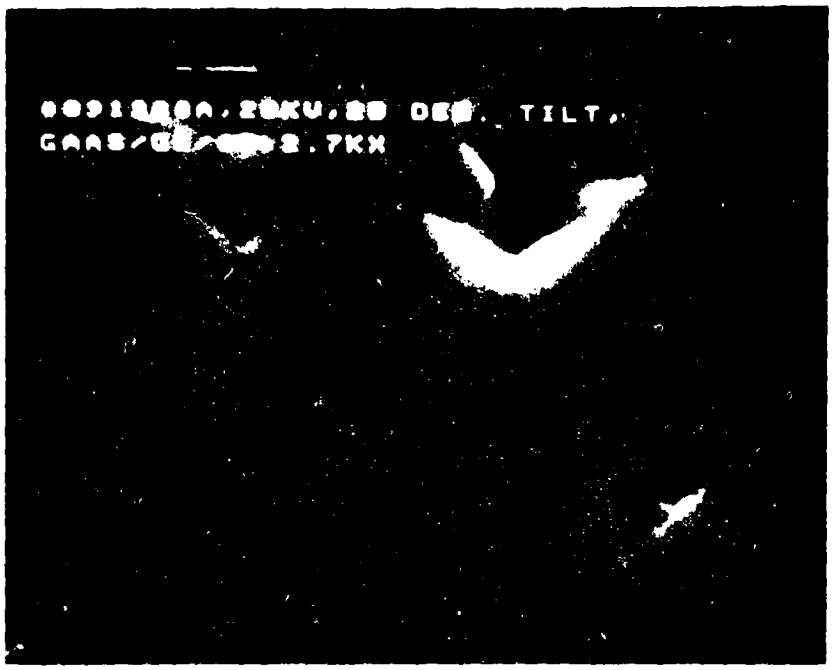

Fig. 4-16. SEM photomicrograph (2700X) of the GaAs/Ge/Si sample.

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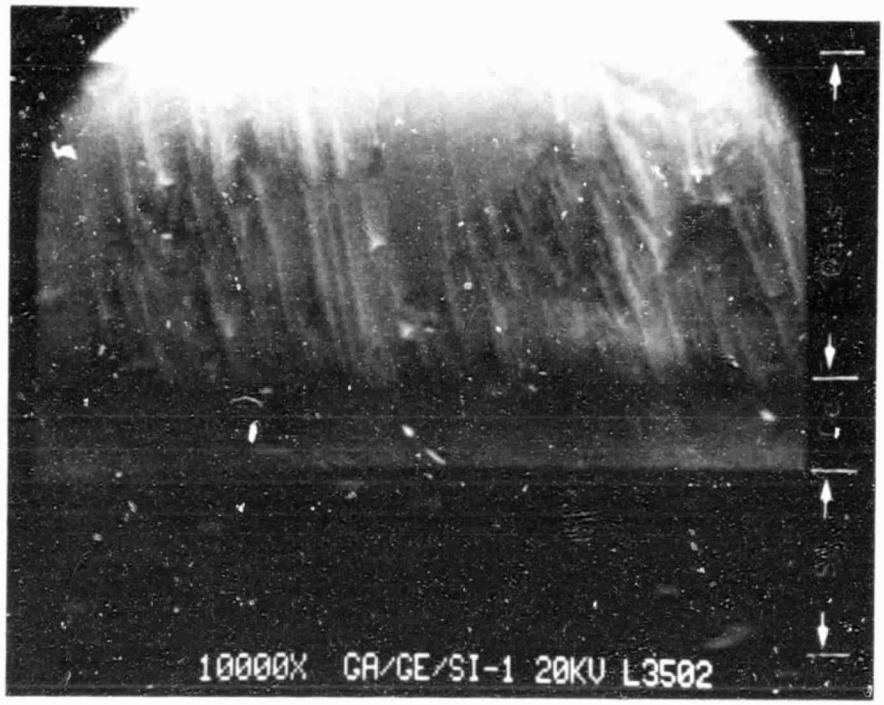

Fig. 4-15. SEM photomicrograph (10,000X) of the cleaved cross-section of the GaAs/Ge/Si structure.

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Fig. 4-16. SEM photomicrograph (2700X) of the GaAs/Ge/Si sample.

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