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MODELING AND ANALYSIS OF POWER PROCESSING SYSTEMS (MAPPS)

FINAL REPORT

VOLUME I - TECHNICAL REPORT

By

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Prepared for:

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16. Abstract

Computer aided design and analysis techniques are applied to Power Processing Equipment. This project is a further continuation of the modeling and analysis of power processing systems reported in CR-134686, CR-135173, and CR-135174.

This report, Volume I, covers work performed on the following Power Processing Modeling and Analysis topics:

(a) Discrete Time Domain analysis of switching regulators for performance analysis.

(b) Design Optimization of Power Converters using Augmented Lagrangian Penalty Function Technique.

(c) Investigation of Current-Injected Multiloop Controlled Switching Regulators.

(d) Application of Optimization for Navy VSTOL Energy Power System

The discussion includes the generation of the mathematical models and the development and application of computer aided design techniques to solve the different mathematical models.

Recommendations are made for future work that would enhance the application of the computer aided design techniques for Power Processing Systems.

Volume II contains the supporting appendices.

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FOREWORD

The Modeling and Analysis tasks were performed by the following personnel:

Task I - Discrete Time Domain Analysis of Switching Regulator

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Task II - Design Optimization of Power Converters

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Virginia Polytechnic Institute & State University

Task III - Investigation of Current Injected Multiloop Controlled Switching Regulators

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Virginia Polytechnic Institute & State University

Task IV - MAPPS Demonstration Problem for VSTOL Emergency Power Systems

Dr. Yuan Yu
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1.0 INTRODUCTION

"Modeling and Analysis of Power Processing Systems," (Contract NAS3-21051), provides basic analytical tools, in the form of mathematical models, and the computer-aided techniques required to solve those models, to guide engineers in the various aspects of power processing equipment and system design. Early work in this area included a feasibility study done by TRW Systems[1] and General Electric[2], and the initial modeling and analysis performed by TRW Systems[3] and California Institute of Technology[4]. The present effort, performed by TRW Systems and Virginia Polytechnic Institute and State University, is an extension of that early work.

The four tasks completed on this contract include the following:

- Performance Analysis of Buck, Boost, and Buck-Boost DC-DC Converters using dual-loop feedback control system[5],[6].
- Design Optimization for Boost and Buck-Boost DC-DC Converters. (Design Optimization for Buck DC-DC Converters is contained in Reference [3].)
- Investigation of Current-Injected, Multiloop-Controlled Switching Regulators.
- Application of Design Optimization to U.S. Army VSTOL Emergency Power System.

A technical summary is presented in the following chapters on each of these tasks.

2.0 DC-DC CONVERTERS.

2.1 Introduction.

The following sections are both tutorial, and application oriented. Because of the variety of operating converter power and control schemes, the tutorial is necessary to understand the various analytical procedures and their use. Once understood, the material may be applied to a designers specific needs through the various analysis and simulation subprograms which are provided. Starting with a description of the basic characteristics of DC-DC converters, a general evaluation of discreet time domain analysis, and the performance analysis of the buck, boost, & buck-boost converters is given.

Due to the finite flux capacity of the inductive elements, a DC-DC converter must be oscillatory in nature. The oscillation is achieved by cyclically operating the power switch of the converter in conduction and non-conduction state. Consequently, the converter control system must be able to accept an analog signal obtained from the sensing circuit and the reference, and to convert it into discrete time intervals in controlling the conduction and non-conduction of the power switch.

The electrical performance of a DC-DC converter depends primarily on the quality of its control system. The performance characteristics of interest to a converter designer include stability as well as the converter-output response to step and sinusoidal disturbances, both from the line and the load.

2.1 Introduction. (Cont.)

Functionally, a DC-DC regulated converter can be divided into two parts: A power circuit, and a control circuit. By definition, the power circuit handles the energy transfer from the source to the load. Three most commonly used power circuits are the buck, the boost, and the buck-boost.

The control circuit manages the rate of the source-load energy transfer as a function of the load demands. During nominal steady-state and transient operations, the control objectives are associated with (A) the tracking of a certain controlled quantity in accordance with a given reference, and (B) the compliance to converter specifications such as the system response to step or sinusoidal line and load disturbances, and to external command signals. During transicnt operations, the control objective is to limit electrical-stress for all the elements associated with the converter, providing effective protection against catastrophic/degradation types of failures. A control circuit thus serves the multiple functions of regulation, command, and protection.

A generalized standardized control module (SCM) has been developed to implement the above control functions (Reference 5,6,7). For the purpose of this report, the SCM Control circuit has been selected to accommodate the power circuits mentioned above.

A SCM-controlled DC-DC converter is shown in Fig. 2.1. The power circuit, occupying the upper half of the block diagram, processes the transfer of energy from a raw input V_i to a regulated output V_o. Three basic power stages are shown here: Buck, boost, and buck-boost. The control circuit regulates the rate of energy transfer. It receives an analog signal (V_o) from the power-stage output, and delivers a discrete-time interval signal(d) to achieve the required on-off control of the switch in the power stage. The discrete-time voltage or current pulses generated in the power stage are averaged by an LC filter having a much longer time constant than the discrete-time pulse intervals. The averaged output therefore contains negligible switching-frequency components., and can be regarded as an analog signal containing only lower-frequency information.

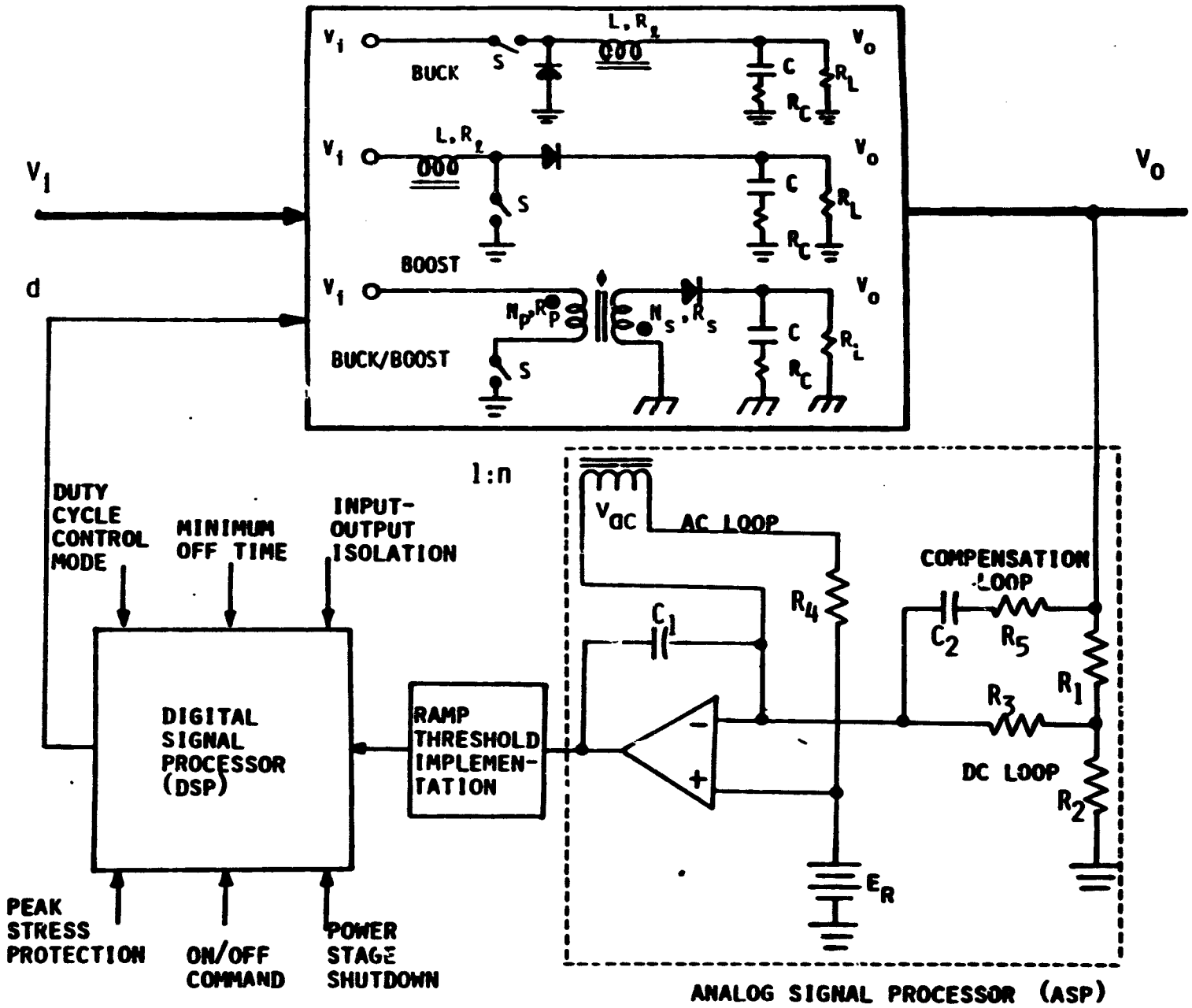

FIG. 2.1 SCM CONTROLLED SWITCHING REGULATORS

2.1 Introduction (Cont.)

The SCM, occupying the lower half of the block diagram, performs the control function within the converter. It contains an Analog Signal Processor (ASP) and a Digital Signal Processor (DSP). Implementations of both ASP and DSP are standardized: They combine to provide the required analog signal to discrete-time interval conversion. The key feature of the SCM is the utilization of an inherent AC switching-frequency signal within the power stage. This utilization is in addition to the conventional DC sensing of output V_0. The sensed AC signal and the DC error are processed by the ASP. As a result, an adaptive stability is obtained which is independent of the filter parameter changes. The SCM control function is completed by the DSP, which processes the control-signal output from the ASP in conjunction with a prescribed control law, and operates the "ON-OFF" of the power switch via a duty-cycle signal, d.

As stated previously, the control-circuit functions also include command and protection. The command function generally requires the converter to respond to an external signal capable of overriding control signal(d) in determining the on-off of the power switch. The protection function includes power-component peak-stress limiting and the converter shutdown in the event of a sensed abnormality such as overvoltage, undervoltage, or overcurrent beyond a predetermined, tolerable level and duration. These functions are performed within SCM by the DSP[5,6,7].

The three basic functional blocks of an SCM-controlled converter are shown in the block diagram of Figure 2.2.

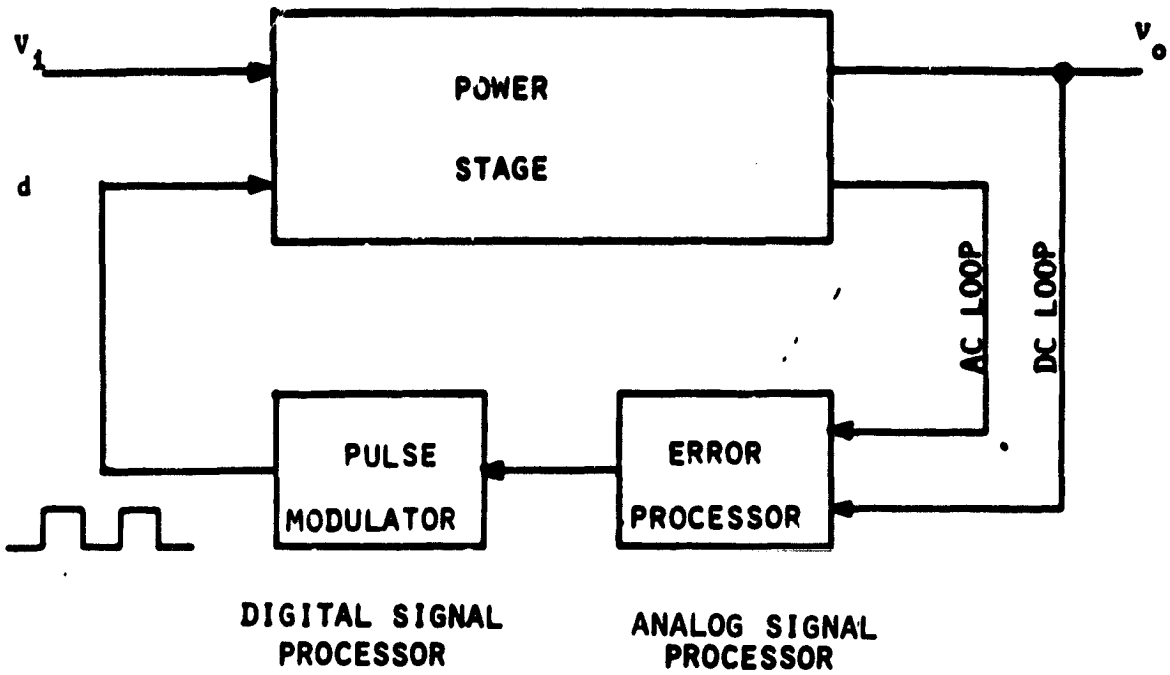

FIG. 2.2. SWITCHING REGULATOR BLOCK DIAGRAM

2.2 Performance Analysis and Simulation Techniques.

2.2.1 Nonlinear Operation of Switching Regulator.

A dc-dc switching-regulated converter is inherently a nonlinear device. The first major nonlinearity exists in the power stage, and is due to the operation of the power switch. Different circuit topologies correspond to the respective on and off time intervals in the switching cycle. The second major nonlinearity exists in the Digital Signal Processor (DSP). Harmonic frequencies, which are multiples of the input disturbance frequency, are contained in the DSP output. Because of such system nonlinearities, difficulties are encountered in reaching performance assessments of various system performances such as stability, attenuation of sinusoidal/step line disturbances, and response to sinusoidal/step load disturbances.

The Power Stage nonlinearity will be elaborated here, and various analytical approaches capable of treating this type of nonlinearity will be discussed. In light of the stated objective of this program, which is the performance analysis and simulation of dc-dc switching regulators, a specific approach will then be selected as the basic analytical tool for the entire program.

2.2.2 Power Stage Nonlinearity.

Each of the power stages shown in Figure 2.1 can be divided as a function of the output filter inductor MMF status. In Figure 2.3(A), often referred to as "continuous-conduction" or Mode 1 operation, the MMF ascends during on time T_{on} when the power switch in ON and the diode is OFF, and descends during T_{F1} when power switch is OFF and the diode is ON. Notice that the MMF never vanishes in the output inductor. In Figure 2.3(B), often referred to as "discontinuous-conduction" or Mode 2 operation, the MMF ascends from zero MMF at the beginning of T_{on}, and descends back to zero during T_{F1}. An additional off time T_{F2} exists when both the power switch and the diode are OFF, during which the inductor MMF remains zero, and load current is supplied entirely by the output-filter capacitor.

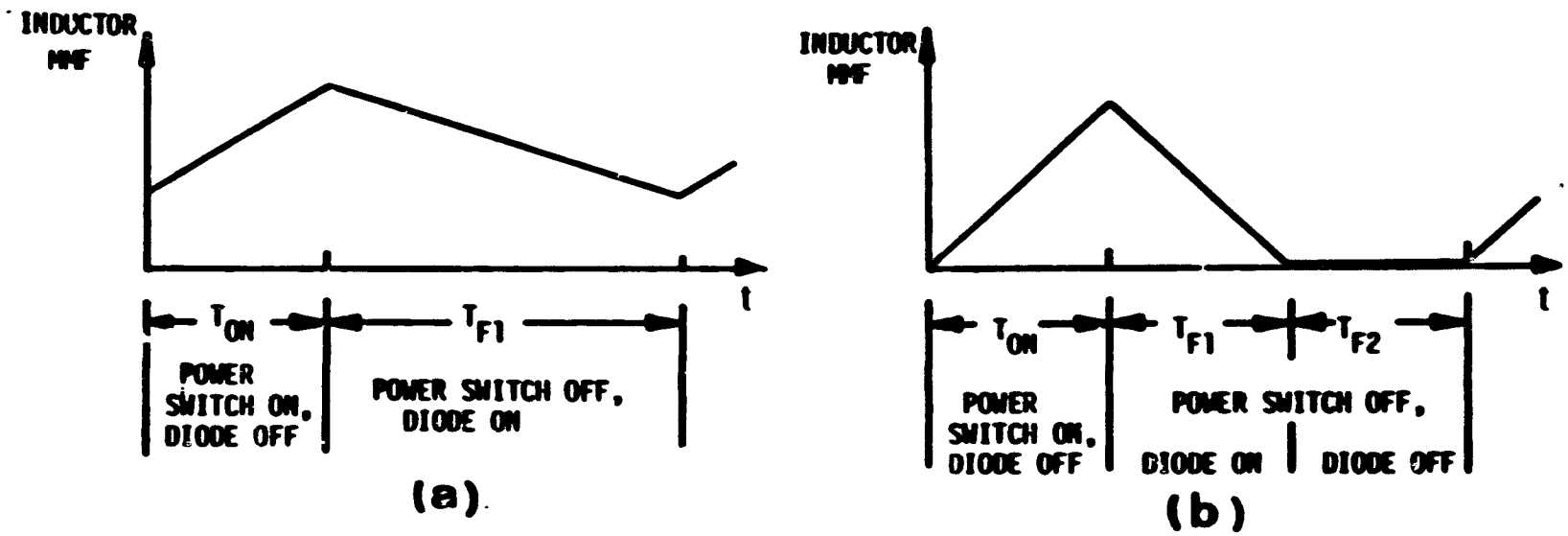

FIG. 2.3 INDUCTOR CURRENT WAVEFORMS (A) CONTINUOUS MMF OPERATION
(B) DISCONTINUOUS CURRENT OPERATION

2.2.2 Power Stage Nonlinearity - (Con't)

Topologies of the buck, boost, and buck-boost power stages correspond to T_{on}, T_{F1}, and T_{F2}, are illustrated in Figures 2.4 to 2.6, respectively. Even though a given power stage is linear for each time interval, the combination of all different linear circuits for the purpose of analyzing a complete cycle of switching-regulator operation becomes a piecewise-linear nonlinear analysis problem.

The difficulty is integrating these different topologies and collectively evaluating their responses to various line/load disturbances having a much longer time period than individual T_{on}, T_{F1}, T_{F2}.

The basic modeling approaches for conducting performance analysis and simulation include the following:

- Discrete Time-Domain Analysis
- Average Time-Domain Analysis
- Exact Frequency-Domain Analysis

.... Small Signal Analysis

- Discrete Time-Domain Simulation .... Large Signal Analysis

Techniques for all four approaches have been established in the previous MAPPS program phases[1,3,4]. Their respective utility for a given application depends on the analysis objective, the desired accuracy, the control-circuit type, the nature of the disturbance, and perhaps most important, the user's analytical backgoround. A summary description of all four approaches is presented in Table 2-I.

The exact frequency domain analysis will not be pursued in the proposed program due to its difficulty in incorporating the input filter which often causes major complications in the design for the required performances in regulator stability as well as in audiosusceptibility and output impedance.

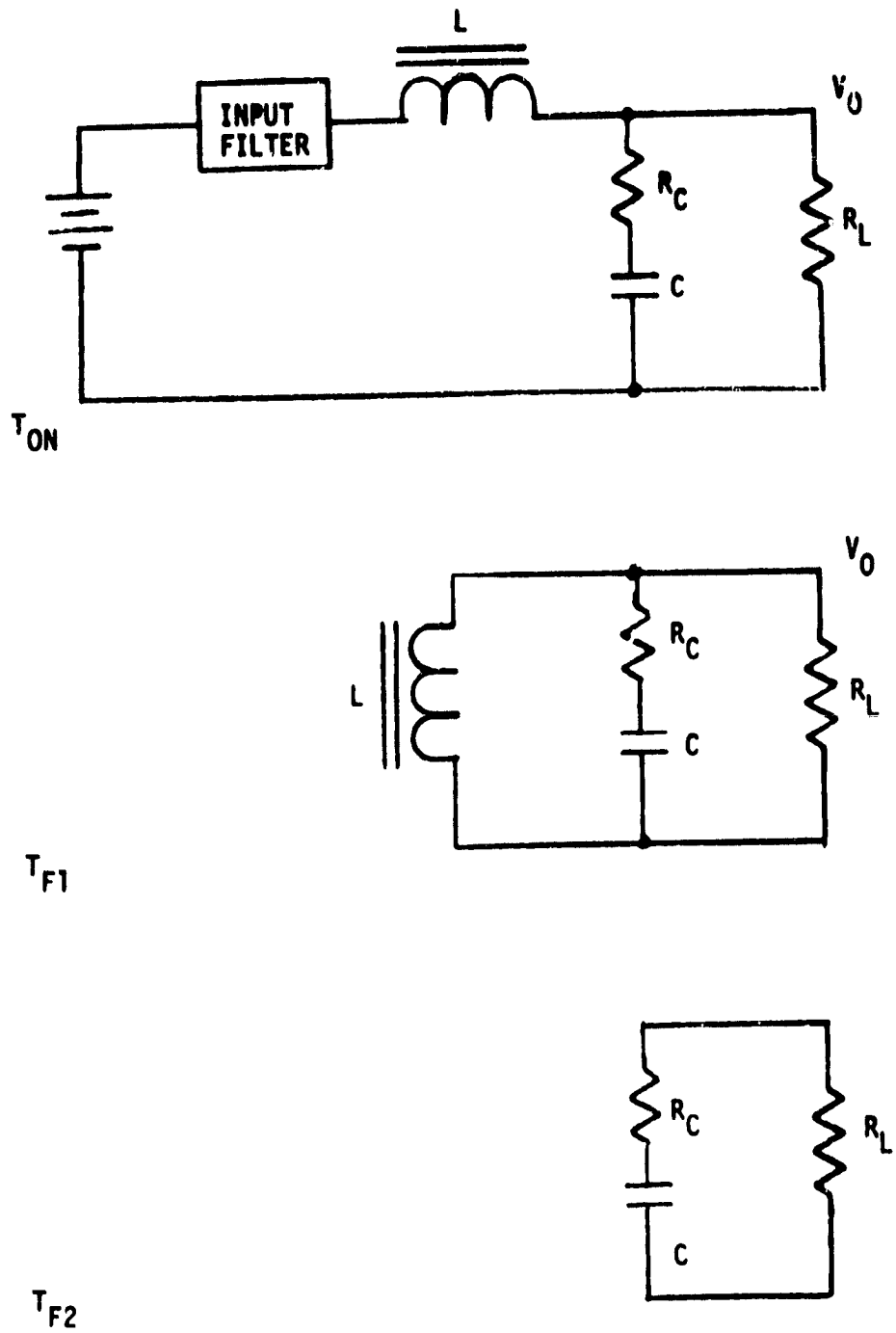

FIGURE 2.4 BUCK POWER STAGE TOPOLOGIES

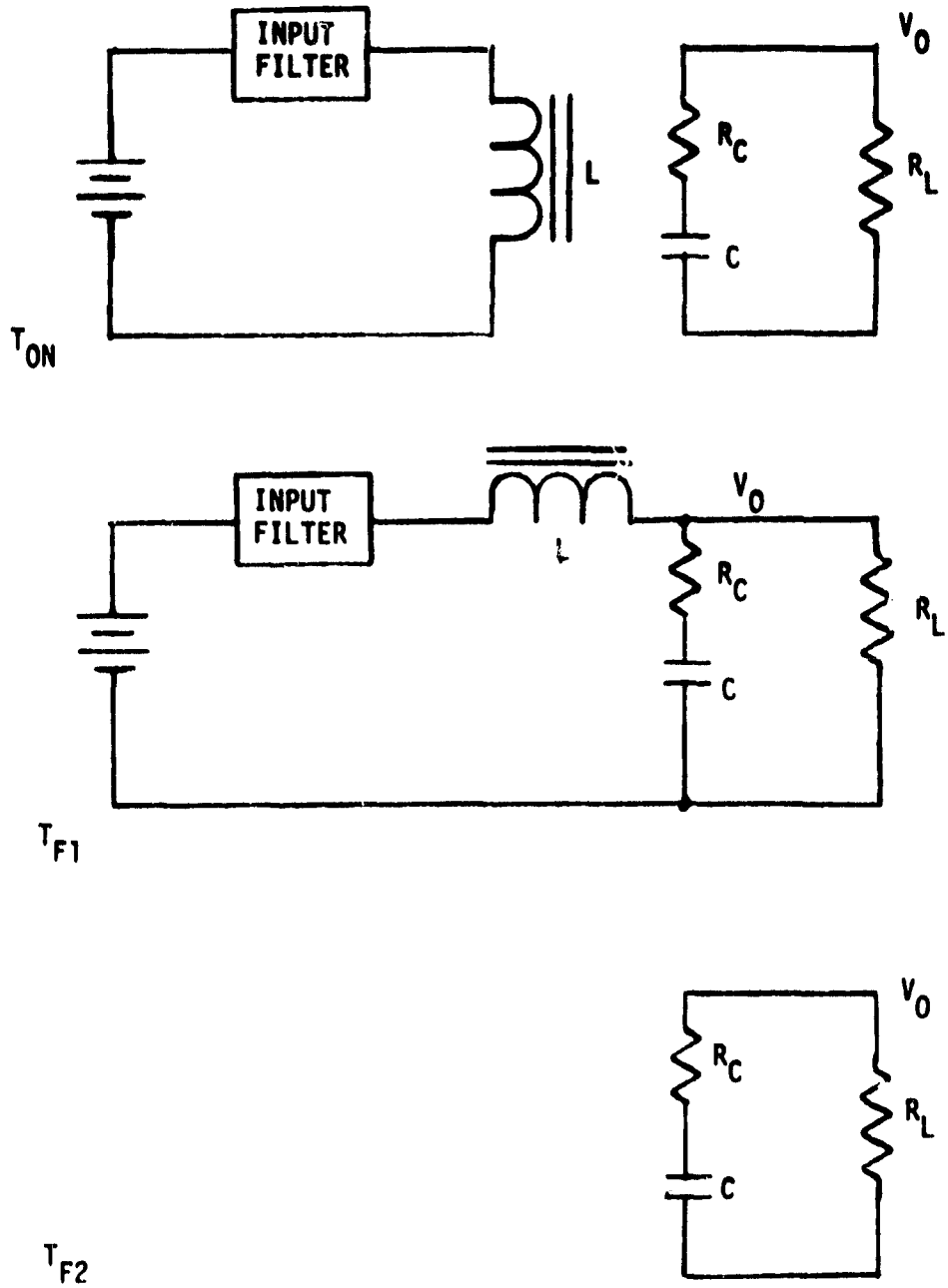

FIGURE 2.5 BOOST POWER STAGE TOPOLOGIES

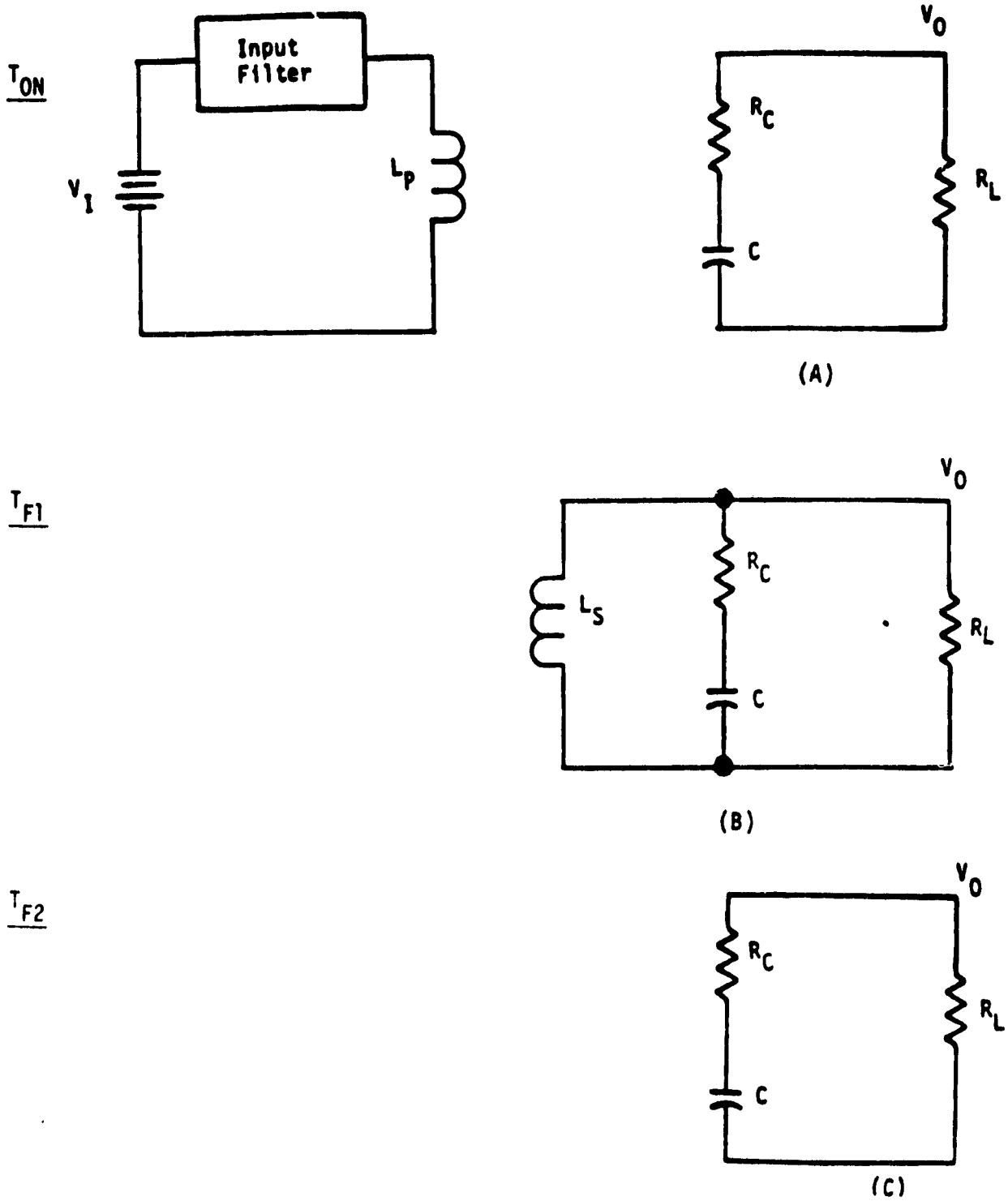

FIGURE 2.6 BUCK-BOOST POWER STAGE TOPOLOGIES

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TABLE 2-I Major Performance Analysis Approaches

MODELING APPROACH / DESCRIPTION	AVERAGE TIME DOMAIN	EXACT FREQUENCY DOMAIN	DISCRETE TIME DOMAIN ANALYSIS	DISCRETE TIME DOMAIN SIMULATION
BASIC MODELING	Take advantage of the much lower output-filter resonant frequency in relation to the equipment switching frequency, the nonlinear switching power stage is approximated by a continuous small-signal average model.	Represent the power stage with a linearized discrete impulse response function. The discrete time model is then transferred into the frequency domain.	Exact formulation of state equations, and use iteration method (Newton's) to solve for the exact equilibrium state. Linearized about the equilibrium state to become linear and time-invariant. Z-transformation to frequency domain when needed.	Base on recurrent discrete time-domain analytical expressions, and propagate recurrent equations through Fortran computation.
BACKGROUND NEEDED	Linear control theory and/or linear state space model.	State space techniques.	State space techniques and Fortran programming.	State space techniques and Fortran programming.
MERITS	• Gain more insight on equipment parameter design. • Analytical skill resides in many design engineers. • Readily applicable to high-order circuits and equipment.	• More accurate power stage model at higher signal frequencies, up to one-half of the switching frequency.	• Most accurate stability analysis through eigenvalues. • No need to separate a converter into functional blocks. Most straightforward analysis. • Directly lead to cost-effective performance simulation. • Most suitable for a standardized design.	• Handle large-signal disturbance analysis such as sudden output short and regulator starting. • much faster than general purpose simulation programs such as ECAP, SCEPTRE, etc.
MAJOR LIMITATIONS	Diminishing accuracy below 10-15% of switching frequency. Not suitable for high bandwidth regulators.	Difficult to incorporate input filter and pulse modulation.	Basically a numerical approach. No closed-form insight can be gained.	None other than loss of insight generally associated with simulation efforts when not supported by analyses.

2.2.2 Power Stage Nonlinearity - (Con't)

The performance requirements associated with the analysis and simulation effort are:

- Regulator control-loop stability (local)
- Audio susceptibility (attenuation of source small signal disturbance)
- Transient response (response to source/load large-signal step change)

For the first two performance categories, the nature of the disturbances is such that the regulator can be regarded as a time-invariant system without a significant loss in analytical accuracy, and linearized about its equilibrium state to obtain a linear analytical model for small-signal performance evaluations. For the last category, the generally varying duty cycle subsequent to a step line/load change represents a time-varying nonlinear system. Since any practical system is likely to be higher than second-order, performance evaluation is through tactics closely identified with simulation techniques.

2.2.3 The Discrete-Time Domain Analysis.

Realizing that a switching regulator is inherently a highly nonlinear circuit containing analog-to-discrete-time conversion, it is only natural that it can be more accurately analyzed through discrete time-domain modeling and analysis. Therefore, discrete time-domain analysis has been selected as the approach to be utilized for the performance, analysis and simulation program.

In this approach, state-space techniques are employed to characterize regulators exactly through the formulation of nonlinear discrete time-domain equations in vector form. Newton's iteration is then used to solve for the equilibrium state of the regulator. The system is then linearized about its equilibrium state to arrive at a linear discrete time model. The closed-loop regulator is thus modeled as a single entity rather than the three separated functional blocks shown in Figure 2.1. The stability is studied by examining the eigenvalues of the linear system. The analysis can be extended, through Z-transform, to determine frequency-related performance characteristics such as audiosusceptibility. The modeling and analysis approach makes extensive use of the digital computer, making automation in regulator analysis possible.

2.2.4 Discrete Time-Domain Analysis Objective.

Discrete time-domain analysis is the most accurate and straight forward of the different mathematical modeling techniques available. The user need only be proficient in the use of state-space analysis. Discrete time-domain analysis is applicable to all types of power and control circuit configurations, operating in either continuous or discontinuous mode. Thus, it clearly stands as the best approach available.

The performance analysis and simulation objective is twofold: (1) the creation of generally applicable, practical, analysis subprograms and (2) a tutorial role of providing power processing designers with an effective analytical tool.

2.2.4 Discrete Time-Domain Analysis Objective - (con't)

While time-domain analysis readily fulfills the second objective, the subprograms can only be applied by the prospective user if the user's regulator power and control circuitry is identical to the circuit configuration upon which the subprograms are based. Consequently, in pursuing time-domain analysis, the objective is to achieve the following:

(1) To present clearly the tutorial information needed, by a user conducting time-domain analysis, for adopting the analysis to his specific application.

(2) To create subprograms for regulators with standardized multiple-loop feedback control.

2.2.5 General Description of Performance Analysis and Simulation Techniques.

Time-domain analysis may be applied to energy-storage converters to yield transient and steady-state solutions, stability, and audiosusceptibility. This approach has been applied here to buck, boost, and buck/boost converters with constant frequency and constant OFF time control. By way of introduction, a general step-by-step procedure for performing time-domain analysis of energy storage converters will now be presented.

Step 1: Select the n x 1 system state variable vector $\underline{x} = [x_1, \ldots, x_n]^T$. Normally, the state variables are the voltage across the capacitors and currents through the inductors. However, for the convenience of each individual problem, state variables can be chosen differently.

Step 2: Write the system equations according to the modes of operation of the converter which are defined as follows:

Mode 1 Operation: The current through the inductor is always greater than zero. The period of each switching cycle can be clearly divided into two time intervals. T_{ON} and T_{F1}. During T_{ON}, the power transistor is "ON" and the diode is "OFF", and during T_{F1}, the power transistor is "OFF" and the diode is "ON".

<u>Mode 2 Operation</u>: The current through the inductor reduces to zero and resides at zero for a time interval T_{F2}. During this time interval, both the transistor and the diode are "OFF". The time intervals T_{ON} and T_{F1} defined in the Model operation also exist in the Mode 2 operation.

The system representation for the Mode 1 operation is

$$\dot{\underline{x}} = F1\ \underline{x} + G1\ \underline{u} \qquad \text{during } T_{ON} \qquad (2\text{-}1)$$

$$\dot{\underline{x}} = F2\ \underline{x} + G2\ \underline{u} \qquad \text{during } T_{F1} \qquad (2\text{-}2)$$

where

$$\dot{x} \triangleq \begin{bmatrix} \frac{dx_1}{dt} \\ \frac{dx_2}{dt} \\ \cdot \\ \cdot \\ \cdot \\ \frac{dx_n}{dt} \end{bmatrix}$$

and

$$u \triangleq \begin{bmatrix} u_1 \\ u_2 \\ \cdot \\ \cdot \\ \cdot \\ u_m \end{bmatrix}$$

The column vector $\underline{u}$ is a (mxl) input vector, containing the input voltage E_I, the reference E_R, the saturation voltage drop across the power transistor, and the forward voltage drop across the diode. The nxn matrices F1 and F2 and the nxm matrices G1 and G2 are constant matrices containing various circuit parameters.

In the Mode 2 operation, equation (2-3), must be added to the system representation:

$$\dot{\underline{x}} = F3\,\underline{x} + G3\,\underline{u} \;.\;.\;.\;.\;.\; \text{during } T_{F2} \qquad (2\text{-}3)$$

The dimensions of F3 and G3 are not necessarily the same as those of F1 and G1, respectively.

The converters, which are basically nonlinear switching circuits, are accurately described by the piecewise-linear representations (2-1) to (2-3).

<u>Step 3</u> The general solution of the linear differential equation

$$\dot{\underline{x}} = F_i\,\underline{x} + G_i\,\underline{u} \qquad i = 1, 2, 3 \qquad (2\text{-}4)$$

is

$$\underline{x}(t_k+T) = \phi_i(T)\underline{x}(t_k) + D_i(T)\,\underline{u} \qquad (2\text{-}5)$$

where $\phi_i(T) = e^{F_iT} \qquad i = 1, 2, 3$

$$D_i(T) = e^{F_iT}\left[\int_0^T e^{-F_iS}ds\right] G_i \qquad i = 1, 2, 3$$

The terms $\phi_i(T)$ and $D_i(T)$ can be computed either analytically or numerically. If they are computed numerically, the following Taylor series expansion may be used:

$$e^{F_iT} = 1 + F_iT + \frac{(F_iT)^2}{2!} + \frac{(F_iT)^3}{3!} + \;.\;.\;.\;.\; \quad i = 1, 2, 3$$

<u>Step 4</u> Write the discrete-time-domain equation for the converter. The discrete-time-domain equation can be expressed as

$$\underline{x}(t_{k+1}) \overset{\Delta}{=} \phi\,\underline{x}(t_k) + V\,\underline{u} \qquad (2\text{-}6)$$

where t_k and t_{k+1} correspond to instants of time at the beginning of the k<u>th</u> cycle and the k+1 <u>th</u> cycle, respectively.

Mode 1 Operation

It may be shown, for Mode 1 operation, that the terms ϕ and V of equation (2-6) are given by -

$$\phi \triangleq \phi_2(T_{F1}^k)\ \phi_1(T_{ON}^k) \tag{2-7}$$

$$V \triangleq \phi_2(T_{F1}^k)\ D1(T_{ON}^k) + D2(T_{F1}^k) \tag{2-8}$$

where T_{ON}^k and T_{F1}^k represent the T_{ON} and T_{F1} intervals during the kth cycle. The time intervals T_{ON}^k and T_{F1}^k can be determined through the following two conditions:

Condition 1 A threshold condition, which is determined by the particular type of digital control signal processor employed in the converter, and may be expressed as -

$$\xi_1(\underline{x}(t_k),\ T_{ON}^k,\ T_{F1}^k) = 0 \tag{2-9}$$

Condition 2 A condition which specifies whether the converter is operating at a constant frequency, or a constant ON time, or a constant OFF time, or a constant voltage-second, and is expressed as -

$$\xi_2(T_{ON}^k,\ T_{F1}^k) = 0 \tag{2-10}$$

Mode 2 Operation

For mode 2 operation, the terms ϕ and V of eq. (2-6) are given by -

$$\phi \triangleq \phi_3(T_{F1}^k)\ \phi_2(T_{F1}^k)\ \phi_1(T_{ON}^k) \tag{2-11}$$

$$V \triangleq \phi_3(T_{F2}^k)\ \phi_2(T_{F1}^k)\ D_1(T_{ON}^k)$$

$$+ \phi_3(T_{F2}^k)\ D_2(T_{F1}^k) + D_3(T_{F2}^k) \tag{2-12}$$

In order to determine the time intervals T_{ON}^k, T_{F1}^k and T_{F2}^k, a third condition, in addition to (2-9) and (2-10), should be included to detect the time instant when the inductor current reduced to zero. This condition may be written -

$$\xi_3(\underline{x}(t_k), T_{ON}^k, T_{F1}^k, T_{F2}^k) = 0 \qquad (2\text{-}13)$$

Of course, in the Mode 2 operation, the time interval T_{F2}^k should also be a parameter in (2-9) and (2-10). Thus, for Mode 2 operation,

$$\xi_1(\underline{x}(t_k), T_{ON}^k, T_{F1}^k, T_{F2}^k) = 0 \quad \text{and} \quad \xi_2(T_{ON}^k, T_{F1}^k, T_{F2}^k) = 0$$

Equations (2-6 to 2-13) are the complete representation of the converters.

<u>Step 5</u> Solve for the approximate steady state $\tilde{\underline{x}}$.*

The approximate solution is employed later as an initial guess toward solving the exact steady state through Newton's iteration method. In the steady state, equation (2-6) may be written as

$$\tilde{\underline{x}}^* = \Phi\, \tilde{\underline{x}}^* + V\, \underline{u} \qquad (2\text{-}14)$$

The Φ matrix and V matrices can be computed for the given T_{ON}, T_{F1}, and T_{F2}. For given input-output requirements of the converter, the approximate time intervals, T_{ON}, T_{F1} and T_{F2} can be determined. Reference 1 gives a detailed list of duty cycle formulae for different power stages and different control schemes.

If the matrix $(I-\phi)$ is non-singular, equation (2-14) may be solved for $\tilde{x}^*$

$$\underline{\tilde{x}}^* = (I - \phi)^{-1} V \underline{u} \qquad (2\text{-}15)$$

However, in many cases, the matrix $(I-\phi)$ is singular. In order to solve for $\tilde{x}^*$, equation (2-6) together with (2-9) is required.

<u>Step 6</u> Solve for the exact steady state $\underline{x}^*$.

Newton's iteration method is employed to find the steady-state solution with the initial guess $\underline{\tilde{x}}^*$. Equations (2-6) through (2-13) are used in the iteration process until a specified state-matching condition is satisfied. The state-matching condition can be defined as

$$\sqrt{\sum_{i=1}^{n} [x_i(t_{k+1}) - x_i(t_k)]^2} < \varepsilon \qquad (2\text{-}16)$$

for an arbitrarily small positive number, or it can be defined simply as

$$|x_i(t_{k+1}) - x_i(t_k)| < \varepsilon \qquad (2\text{-}17)$$

<u>Step 7</u> Linearize the discrete-time-domain equation, Eq. (2-6), about the equilibrium state $\underline{x}^*$ for studying stability, audiosusceptibility, and transient response to a small step change of the input or the load.

Equation (2-6) may be written in the form

$$\underline{x}(t_{k+1}) = f\,(\underline{x}(t_k),\ u_1,\ T_{ON},\ T_{F1},\ T_{F2}) \qquad (2\text{-}18)$$

where u_1 is the input voltage.

Form the term $\delta \underline{x}(t_{k+1})$ by taking partial derivatives of Eq. (2-18) with respect to $\underline{x}$ and u_1 and writing

$$\delta \underline{x}(t_{k+1}) = \frac{\partial f}{\partial \underline{x}} \delta \underline{x}(t_k) + \frac{\partial f}{\partial u_1} \delta u_1$$

$$\stackrel{\Delta}{=} \psi \, \delta \underline{x}(t_k) + \Gamma \, \delta u_1 \qquad (2\text{-}19)$$

where ψ is a (nxn) matrix and Γ is a (nx1) column matrix.

The differentiation of (2-18) can be performed analytically, if the problem is simple, or numerically by difference quotients.

Step 8 Analyze the stability of the converter.

The linearized system (2-19), is stable if and only if all the eigenvalues λ_i of the matrix ψ are absolutely less than unity, i.e.,

$$|\lambda_i| < 1 \qquad i = 1, \ldots, n$$

The eigenvalues are evaluated by the computer. Changes of eigenvalues as a function of system parameters can be plotted in the complex plane, the λ-plane. The location of the eigenvalues in the λ-plane indicates not only the stability but also the transient behavior of the system, i.e., damping and rapidity of response.

Step 9 Analyze the Audio-Susceptibility of the converter.

Audiosusceptibility may be defined as the frequency response of the output voltage V_o to a small amplitude sinusoidal perturbation of the input voltage u_1. The Z-transformation may be used with Equation (2-19) to derive the audiosusceptibility as a frequency domain transfer function.

The output voltage v_o may be expressed as

$$v_o(t_k) = C\,\underline{x}\,(t_k) \tag{2-20}$$

where C is a constant (1xn) row matrix.

The Z transformation of (2-19) is

$$\delta\,x\,(Z) = (IZ - \psi)^{-1}\,\Gamma\delta u_1(Z) \tag{2-21}$$

The frequency-domain transfer function can be derived after replacing Z with e^{jwT_p} in (2-21), and combining (2-20) and (2-21).

$$G(jw) \triangleq \frac{\delta v_o(jw)/E_R}{\delta u_1(jw)/E_I} = \frac{E_I}{E_R}\,C\,(I\,e^{jwT_p} - \psi)^{-1}\Gamma \tag{2-22}$$

where E_I and E_R are the dc average of the input voltage and the output voltage, respectively.

<u>Step 10</u> Study the transient response of the Converter.

The linearized system remains valid for a small step change of input voltage or load, since the system still continues to operate about its equilibrium state. The behavior of the transient with respect to damping, oscillatory nature, decay time, and overshoot of the equilibrium position is governed by the location of the eigenvalues on the λ-plane.

2.2.6 Performance Analysis and Simulation Objectives

Since the principles and procedures for performing the time-domain analysis are the same regardless of the circuit configuration used, both objectives stated in the previous section can be achieved by conducting the time-domain analysis on regulators using SCM multiple-loop control. Certain Performance Analysis Subprograms (PAS's) using this control were generated in the initial MAPPS phase II effort under NAS3-19690[4]. A summary on what has been done is presented in Table 2-II.

In Table 2-II, the three basic power stages, buck, boost, and buck-boost, are separated into Mode I and Mode II operations with constant on time, constant volt-second, constant off time, and constant frequency control. To cover all possible categories, there are a total of twenty-four different power/control configurations. For the particular multiple-loop control configurations marked by "x", time-domain analysis has been applied and completed through previous contracts. Those marked by "NA" are configurations incompatible with the control implementation, and therefore are not recommended for hardware design or time-domain analysis.

Multiple-loop control senses the rectangular voltage across the inductor, and integrates it to form a triangular ramp output. The triangular ramp possesses a negative slope during on time T_N and a positive slope during off time T_F. Since the regulator control determines the point at which the ramp intersects the fixed threshold level, the following conclusions become apparent:

(a) <u>In constant on time or constant volt-second control, regulation is achieved by controlling off time T_F</u>. The threshold level therefore prescribes the peak of the triangular ramp as the intersection of the ascending ramp with the threshold level marks the end of off-time interval T_F.

TABLE 2-II Status of Multiple-Loop Control Time Domain Analysis

Power Stage	Inductor MMF	Duty Cycle Control Schedule			
		Constant On-Time	Constant Volt-Second	Constant Off-Time	Constant Frequency
Buck	Continuous	X	X	X	X
	Discontinuous	NA	NA	X	X
Boost	Continuous	0	0	0	X
	Discontinuous	NA	NA	X	X
Buck Boost	Continuous	0	0	X	X
	Discontinuous	NA	NA	X	X

X : Completed

NA: Configuration Not Recommended

0 : Not yet performed

2.2.6 Performance Analysis and Simulation Objectives (Cont.)

(b) In constant off time or constant frequency control, regulation is achieved by controlling the on time T_{ON}. The threshold level therefore prescribes the valley of the triangular ramp, as the intersection of the descending ramp with the threshold level marks the end of the on-time interval T_{on}.

This rule governing the ramp-threshold interface is further illustrated in Figure 2.7 for continuous inductor-MMF operations. Here, the inductor voltage and the integrator output voltage are shown for constant-on-time control. Notice the difference in the relative position of the threshold level with respect to the triangular ramp.

When the inductor MMF becomes discontinuous, in Figure 2.7(B), the inductor voltage vanishes for a certain interval. During this interval, the integrator output exhibits a flat top. In the constant-on-time control, this flat top coincides with the threshold level. Any slight noise in either the flat top or the threshold level is likely to trigger the on-off control, making the constant-on-time control highly susceptible to noise when engaging in discontinous-MMF operation. Conversely, in the constant-off-time control, the flat top caused by the zero inductor voltage level is above the threshold level, thereby eliminating this noise susceptibility problem. Since the MMF is discontinuous when the regulator output load is light, the constant-on-time and the constant-volt-second control, shown in Figure 2-II, are considered to have limited utility, and therefore are not to be included in the analytical effort.

Hence, this effort concentrates on the time-domain analysis of multiple-loop control based on constant off time and constant frequency. The analysis includes all three power stages, with both continuous and discontinuous MMF operations.

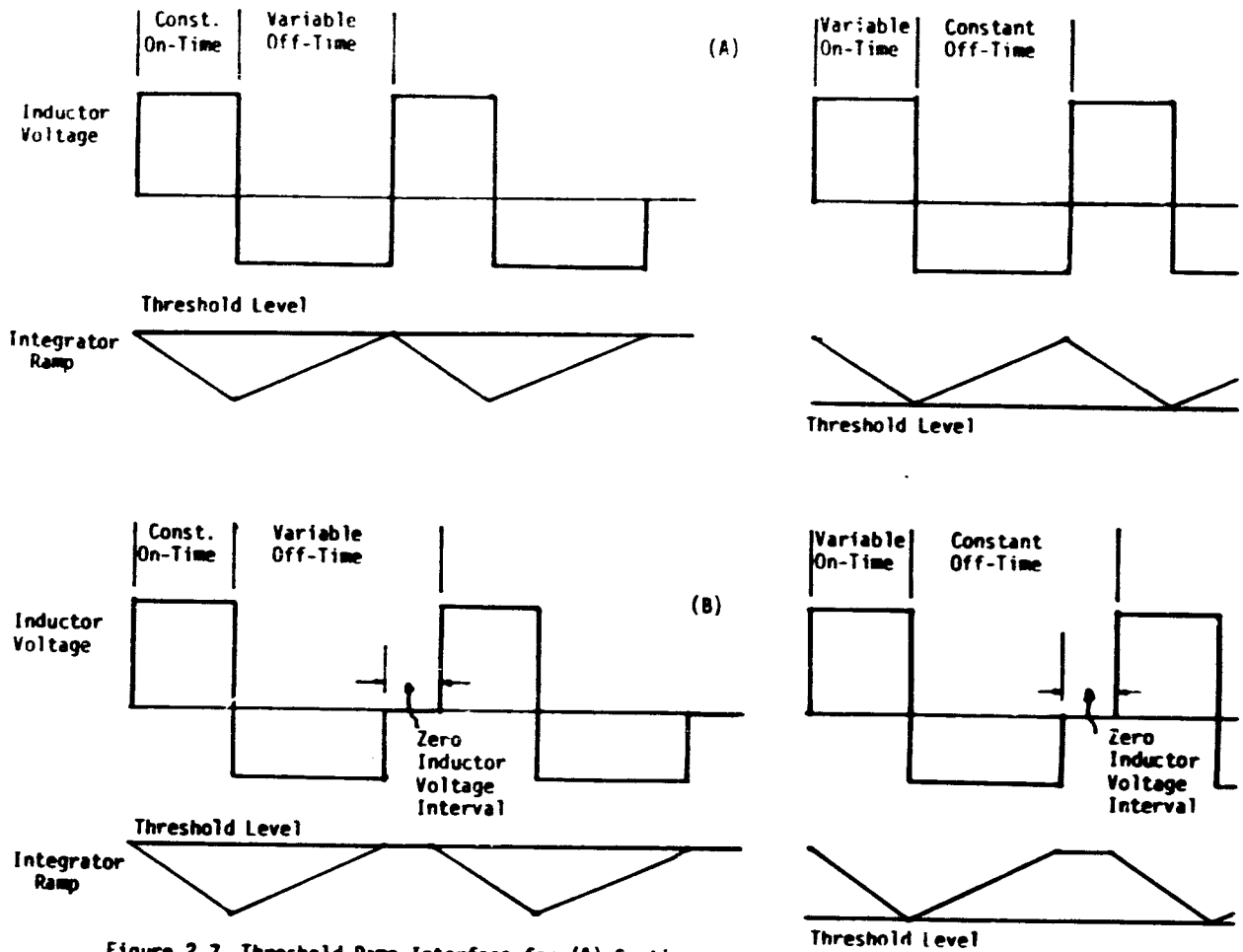


Figure 2.7 Threshold-Ramp Interface for (A) Continuous-MMF and (B) Discontinuous MMF

2.2.6 Performance Analysis and Simulation Objectives (Cont.)

Perform Discrete Time-Domain Analysis

In performing the discrete time-domain analysis, three subprograms, one for each of the three basic power stages, are created. Each subprogram includes both continuous and discontinuous-MMF operations as well as the constant off time and constant frequency control schemes. Each subprogram (buck, boost, and buck-boost) has the capability of:

(1) Either constant-off-time or constant-frequency control in one composite subprogram, or

(2) Either continuous- or discontinuous-MMF operation in the same subprogram.

In discontinuous-MMF operation, the existence of a third time interval during which the inductor MMF vanishes complicates the composite subprogram to a certain extent. Two separate computer subroutines are needed to compute the exact equilibrium state of the system for both continuous and discontinuous modes. The information is then fed into a common linearization subroutine to numerically derive the linearized system for small-signal analysis.

An information flow chart is presented in Figure 2.8 to show how the converter, with both continuous and discontinuous current operations together with two types of duty-cycle controllers, can be implemented in a single computer program. The flow chart presented here is self-explanatory, therefore no description will be given.

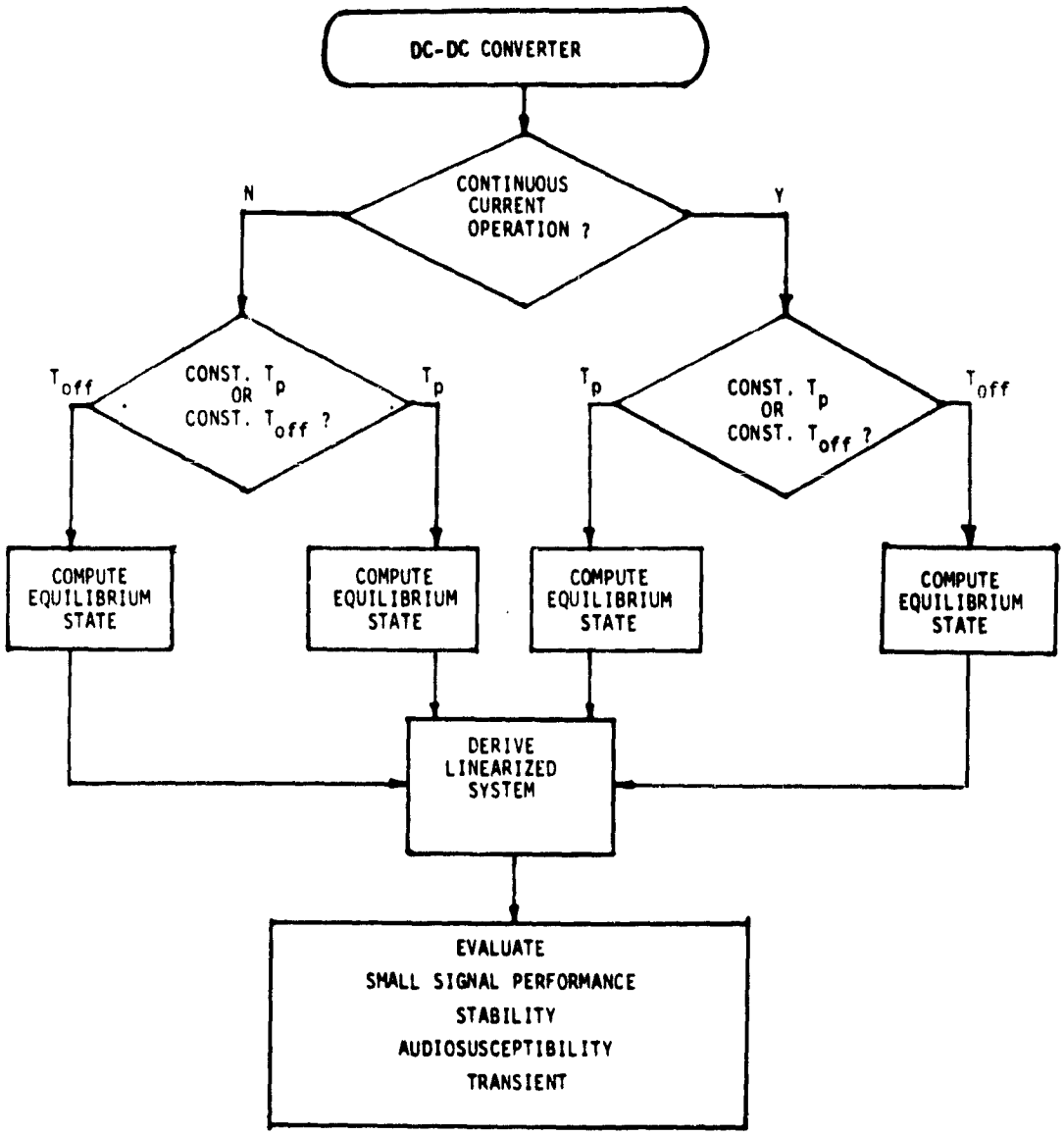


Figure 2.8 Information Flow Chart on a Composite Subprogram

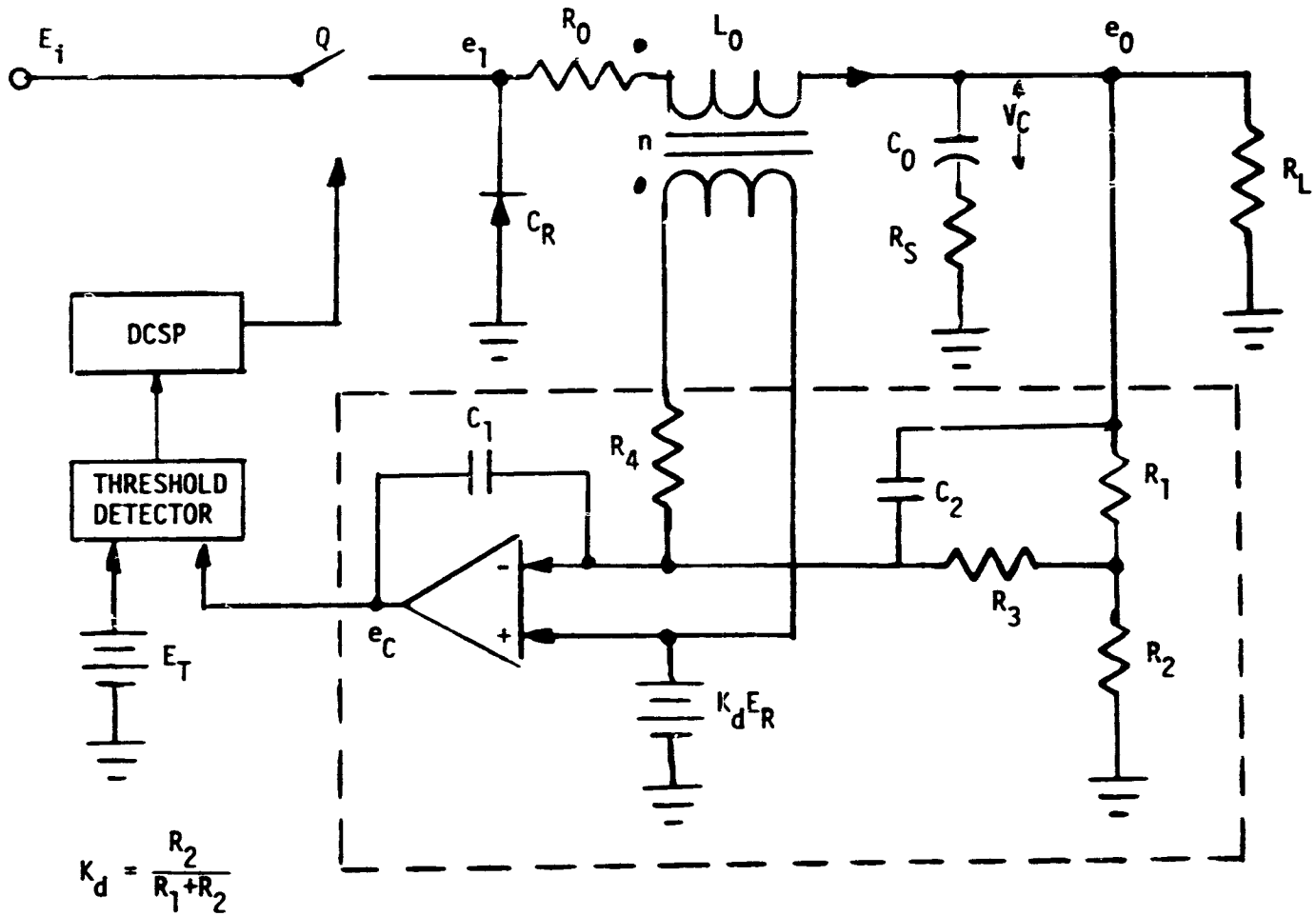
2.3 Formulation of State Equotions

Mathematical models have been generated for the Buck, Boost, and Buck-Boost DC-DC convertions using the constant frequency and constant off-time pulse-width-modulation techniques, and are discussed in detail in the following sections.

2.3.1 Buck DC-DC Converter

2.3.1.1 Constant Frequency Buck Regulator

The buck dc to dc power converter topology is shown in Figure 2.9. The analysis approach is based on the ensuing mathematical model and the capability to consider both continuous and discontinuous inductor current operation.



$$K_d = \frac{R_2}{R_1+R_2}$$

n = Turns Ratio

FIGURE 2.9 BUCK REGULATOR

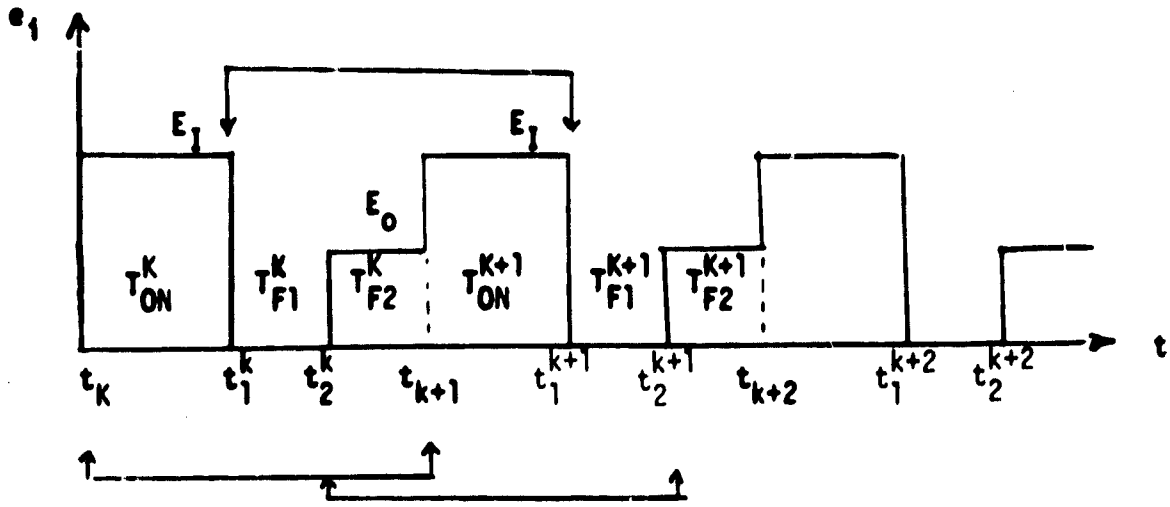


Fig.2-10 Waveform of e_1 for Discontinuous Inductor-Current Operation.

EQUIVALENT DISCRETE TIME SYSTEM

The waveform of e_1 vs. time shown in Fig. 2.10 is used to establish some notation regarding the time instant t_k when each cycle starts and each switching action occurs:

In steady state operation,

At t_k, t_{k+1}, t_{k+2} . . . . . the clock pulse turns the power switch "ON"

At t^k_1, t^{k+1}_1, t^{k+2}_1 . . . . . the threshold condition turns the power switch "OFF"

At t^k_2, t^{k+1}_2, t^{k+2}_2 . . . . . the zero inductor current condition turns off the power diode.

The time intervals $t^k_1 - t_k$, $t^k_2 - t^k_1$, and $t_{k+1} - t^k_2$ are defined as T^K_{ON}, T^k_{F1} and T^k_{F2}, respectively. These time intervals may vary from cycle to cycle. However, the time interval between t_k and t_{k+1} is a constant equal to the period of oscillation T_p, i.e.,

$$t_{k+1} - t_k = T_p \quad \text{for all } k \tag{2-23}$$

The system equations for Figure 2.9 are:

$$\dot{\underline{X}} = F1\underline{X} + G1\underline{U} \qquad t_k \le t < t_1^k \tag{2-24}$$

$$\dot{\underline{X}} = F2\underline{X} + G2\underline{U} \qquad t_1^k \le t < t_2^k \tag{2-25}$$

$$\dot{\underline{X}} = F3\underline{X} + G3\underline{U} \qquad t_2^k \le t < t_{k+1} \tag{2-26}$$

where F1, F2, F3, G1, G2, and G3 are (3x3) constant matrices determined by the system parameters.

$$F1 = F2 = \left[\begin{array}{cc|c} -\dfrac{1}{C_o(R_5+R_L)} - \dfrac{R_5R_L}{L_o(R_5+R_L)} & \dfrac{R_L}{C_o(R_5+R_L)} - \dfrac{R_oR_5R_L}{L_o(R_5+R_L)} & 0 \\ -\dfrac{1}{L_o} & -\dfrac{R_o}{L_o} & 0 \\ \dfrac{n}{R_4C_1} - \dfrac{k_d}{R_3C_1} + \dfrac{C_2}{C_1C_o(R_5+R_L)} + \dfrac{C_2R_5R_L}{C_1L_o(R_5+R_L)} & \dfrac{C_2R_oR_5R_L}{C_1L_o(R_5+R_L)} - \dfrac{mR_o}{R_4C_1} + \dfrac{R_LC_2}{C_1C_o(R_5+R_L)} & 0 \end{array}\right]$$

$$F3 = \left[\begin{array}{c|c|c} -\dfrac{1}{C_o(R_5+R_L)} & \dfrac{R_L}{C_o(R_5+R_L)} - \dfrac{R_oR_5R_L}{L_o(R_5+R_L)} & 0 \\ 0 & -\dfrac{R_o}{L_o} & 0 \\ -\dfrac{k_d}{R_3C_1} + \dfrac{C_2}{C_1C_o(R_5+R_L)} & \dfrac{C_2R_oR_5R_L}{C_1L_o(R_5+R_L)} - \dfrac{R_LC_2}{C_1C_o(R_5+R_L)} & 0 \end{array}\right]$$

$$G1 = \left[\begin{array}{c|c} \dfrac{R_5R_L}{L_o(R_5+R_L)} & 0 \\ \dfrac{1}{L_o} & 0 \\ -\dfrac{n}{R_4C_1} - \dfrac{C_2R_5R_L}{C_1L_o(R_5+R_L)} & \dfrac{k_d}{R_3C_1} \end{array}\right]$$

and,

$$G_2 = G_3 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & \frac{k_d}{R_3 C_1} \end{bmatrix}$$

The vectors $\underline{X}$ and $\underline{U}$ are state variable and forcing function vectors, respectively.

$$\underline{X} \triangleq \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} = \begin{bmatrix} e_o \\ i \\ e_c \end{bmatrix}$$

$$\underline{U} \triangleq \begin{bmatrix} U_1 \\ U_2 \end{bmatrix} \quad \begin{bmatrix} E_I \\ E_R \end{bmatrix}$$

The constraints of the system are governed by the threshold condition at $t = t_1^k, t_2^k \ldots$.

$$X_3 (t_k^1) = E_T, \tag{2-27}$$

the zero inductor current condition at $t = t_2^k, t_2^{k+1} \ldots$.

$$X_2 (t_k^2) = 0, \tag{2-28}$$

and the constant frequency condition . . . .

$$T_{ON}^k + T_{F1}^k + T_{F2}^k = T_p \quad \text{for all } k. \tag{2-29}$$

Each of the linear equations (2-24) to (2-26) admits a closed form solution of the form

$$\underline{X}(t_k^1) = \underline{X}(t_k+T_{ON}^k) = \phi 1(T_{ON}^k)\ \underline{X}\ (t_k) + D1(T_{ON}^k)\ \underline{U} \tag{2-30}$$

$$\underline{X}(t_k^2) = X(t_k^1+T_{F1}^k) = \phi 2(T_{F1}^k)\ \underline{X}\ (t_k^1) + D2(T_{F1}^k)\ \underline{U} \tag{2-31}$$

$$\underline{X}(t_{k+1}) = \underline{X}(t_k^2+T_{F2}^k) = \phi 3(T_{F2}^k)\ \underline{X}\ (t_k^2) + D3(T_{F2}^k)\ \underline{U} \tag{2-32}$$

$$\text{where } \phi i(T) = e^{FiT} \qquad i = 1,\ 2,\ 3 \tag{2-33}$$

$$Di(T) = e^{Fit}\left[\int_0^T e^{-FiS}dS\right] Gi \qquad i = 1,\ 2,\ 3 \tag{2-34}$$

The structures of the matrices ϕi and Di for $i = 1, 2, 3$ have the following forms:

$$\phi i = \begin{bmatrix} \phi i_{11} & \phi i_{12} & 0 \\ \phi i_{21} & \phi i_{22} & 0 \\ \phi i_{31} & \phi i_{32} & 1 \end{bmatrix}$$

$$Di = \begin{bmatrix} di_{11} & 0 \\ di_{21} & 0 \\ di_{31} & di_{32} \end{bmatrix}$$

$$Di = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & di_{32} \end{bmatrix} \qquad \text{for } i = 1,\ 2,\ 3$$

Using equation (2-30) in equation (2-31), and the result in equation (2-32) the equivalent discrete time system for the constant frequency buck converter is given by:

$$\underline{X}(t_{k+1}) = \phi 3(T^k_{F2})\ \phi 2(T^k_{F1})\ \phi 1(T^k_{ON})\ \underline{X}\ (t_k) + \phi 3(T^k_{F2})\ \phi 2(T^k_{F1})\ D1(T^k_{ON})\ \underline{U}$$

$$+ \phi 3(T^k_{F2})\ D2(T^k_{F1})\ \underline{U} + D3(T^k_{F2})\ \underline{U} \qquad (2\text{-}35)$$

Also required in this description are the threshold conditions derived from (2-27)

$$\phi 1_{31}(T^k_{ON})\ X_1(t_k) + \phi 1_{32}(T^k_{ON})\ X_2(t_k) + \phi 1_{33}(T^k_{ON})\ X_3(t_k) + d1_{31}(T^k_{ON})\ U_1$$

$$+ d1_{32}(T^k_{ON})\ U_2 = E_T, \qquad (2\text{-}36)$$

the zero inductor current condition, derived from (2-28)

$$\phi 2_{21}(T^k_{F1})\ X_1(t_{k,1}) + \phi 2_{22}(T^k_{F1})\ X_2(t_{k,1}) = 0, \qquad (2\text{-}37)$$

and the constant frequency condition

$$T^k_{F2} = T_P - T^k_{ON} - T^k_{F1}\,. \qquad (2\text{-}38)$$

Equilibrium Solutions

In steady-state, the following conditions prevail:

$$\underline{X}(t_{k+1}) = \underline{X}(t_k) = \underline{X}^* = \text{constant} \quad \text{for all } k \tag{2-39}$$

$$T_{ON}^{k+1} = T_{ON}^{k} = T_{ON}^{*} = \text{constant} \tag{2-40}$$

$$T_{F1}^{k+1} = T_{F1}^{k} = T_{F1}^{*} = \text{constant} \tag{2-41}$$

$$T_{F2}^{k+1} = T_{F2}^{k} = T_{F2}^{*} = \text{constant} = T_p - T_{ON}^{*} - T_{F1}^{*} \tag{2-42}$$

The Approximate Steady State

The approximate T_{ON}^{*}, T_{F1}^{*} and T_{F2}^{*} can be computed using the following formulae:

$$T_{ON}^{*} = \sqrt{\frac{2L_o T_p P_o}{E_I(E_I - E_R)}} \tag{2-43}$$

$$T_{F1}^{*} = \sqrt{\frac{2L_o T_p P_o \ (E_I - E_R)}{E_I \ E_R^2}} \tag{2-44}$$

$$T_{F2}^{*} = T_p - T_{ON}^{*} - T_{F1}^{*} \tag{2-42}$$

where L_o = the energy storage inductance

P_o = output power

E_I = input voltage

E_R = output voltage

Substituting (2-39 to 2-42) into (2-35), one obtains

$$\underline{X}^* = \phi 3(T^*_{F2})\ \phi 2(T^*_{F1})\ \phi 1(T^*_{ON})\ \underline{X}^* + \Big\{ \phi 3(T^*_{F2})\ \phi 2(T^*_{F1})\ D1(T^*_{ON}) + \phi 3(T^*_{F2})\ D2(T^*_{F1}) + D3(T^*_{F2}) \Big\}\ \underline{U}$$

$$\triangleq \phi\ (T^*_{ON},\ T^*_{F1},\ T^*_{F2})\ \underline{X}^* + \underline{V}\ (T^*_{ON},\ T^*_{F1},\ T^*_{F2})\ \underline{U} \qquad (2\text{-}45)$$

where $(T^*_{ON},\ T^*_{F1},\ T^*_{F2}) = \phi 3(T^*_{F2})\ \phi 2(T^*_{F1})\ \phi 1(T^*_{ON})$ and $\underline{V}\ (T^*_{ON},\ T^*_{F1},\ T^*_{F2})$

$= \phi 3(T^*_{F2})\ \phi 2(T^*_{F1})\ D1(T^*_{ON}) + \phi 3(T^*_{F2})\ D2(T^*_{F1}) + D3(T^*_{F2})$.

The magnitudes of T^*_{ON}, T^*_{F1}, and T^*_{F2} are obtained from equations (2-42) to (2-44)

Equation (2-45) may now be solved for the state vector $\underline{X}^*$. Using this solution we may now solve for the states X^*_1, X^*_2, and X^*_3. Solution begins by arbitrarily setting $X^*_2 = 0$. Then:

$$\begin{aligned} X^*_1 = {} & [\phi 3_{11}(\phi 2_{11}\ \phi 1_{11} + \phi 2_{12}\phi 1_{21}) + \phi 3_{12}(\phi 2_{21}\phi 1_{11} + \phi 2_{22}\phi 1_{21})]\ X^*_1 \\ & + (\phi 3_{11}\phi 2_{11}d1_{11} + \phi 3_{11}\phi 2_{12}d1_{21} + \phi 3_{12}\phi 2_{21}d1_{11} + \phi 3_{12}\phi 2_{22}d1_{21})\ E_I \\ & + (\phi 3_{11}d2_{11} + \phi 3_{12}d2_{21})\ E_I \\ & + d3_{11}E_I \end{aligned} \qquad (2\text{-}46)$$

Equation (2-46) may be solved for X^*_1

$$\begin{aligned} X^*_1 = {} & \frac{1}{1 - [\phi 3_{11}(\phi 2_{11}\phi 1_{11} + \phi 2_{12}\phi 1_{21}) + \phi 3_{12}(\phi 2_{21}\phi 1_{11} + \phi 2_{22}\phi 1_{21})]} \\ & \{\phi 3_{11}[\phi 2_{11}d1_{11} + \phi 2_{12}d1_{21} + d2_{11}] + \phi 3_{12}[\phi 2_{21}d1_{11} + \phi 2_{22}d1_{21} \\ & + d2_{21}] + d3_{11}\ \}\ E_I \end{aligned} \qquad (2\text{-}47)$$

Using this result, the state X_3^* may now be derived from equation (2-36):

$$X_3^* = E_T - \phi 1_{31} X^*_1 - \phi 1_{32} X_2^* - d1_{31} E_I - d1_{32} E_R \tag{2-48}$$

In this approximation, the threshold condition where the inductor current X_2^* equals zero may not be satisfied. This approximation is merely employed as a starting point in order to search for the exact steady state.

The Exact Steady State

Define the system state with the power switch off as

$$\underline{Y}(t_k) \triangleq \underline{X}\,(t_k + T_{ON}^k) \tag{2-49}$$

$$\underline{Z}(t_k) \triangleq \underline{X}\,(t_k + T_{ON}^k + T_{F1}^k) \tag{2-50}$$

where, using Fig. 2-32, it is clear that

$$Y_3(t_k) = E_T \qquad \text{for all } k \tag{2-51}$$

$$Z_2(t_k) = 0 \tag{2-52}$$

In steady-state operation

$$\underline{Y}^* = \phi 1(T_{ON}^*)\underline{X}^* + D1(T_{ON}^*)\underline{U} = f1(T_{ON}^*, \underline{X}^*) \tag{2-53}$$

$$\underline{Z}^* = \phi 2(T_{F1}^*)\underline{Y}^* + D2(T_{F1}^*)\underline{U} = f2(T_{F1}^*, \underline{Y}^*) \tag{2-54}$$

and

$$\underline{X}^* = \phi 3(T_{F2}^*)Z^* + D3(T_{F2}^*)\,\underline{U} \tag{2-55}$$

It is important to note that T_{ON}^* and T_{F1}^* are functions of $\underline{X}^*$ and $\underline{U}$ via the threshold conditions (2-51) and (2-52).

If T_{ON}^* and T_{F1}^* are the exact steady state values, then the steady-state $\underline{X}^*$ calculated from (2.46 to 2-48) has to satisfy the following two matching conditions:

(1) the zero-inductor-current condition

$$B_{match}(\underline{X}^*, T^*_{ON}, T^*_{F1}) = \phi 2_{21}(T^*_{F1})\, Y_1 + \phi 2_{22}(T^*_{F1})\, Y_2 = 0 \qquad (2\text{-}56)$$

(2) the state matching condition

$$S_{match}(\underline{X}^*, T^*_{ON}, T^*_{F1}) = \phi 3_{d1}(T^*_{F2}) Z_1 + \phi 3_{32}(T^*_{F2})\, Z_2 + E_T$$

$$+ d3_{32}(T^*_{F2})\, U_2 - X^*_3 = 0 \qquad (2\text{-}57)$$

Newton's method may now be used to find the T^*_{ON} and T^*_{F1} which satisfy the matching conditions.

The step-by-step procedure is described as follows:

Step 1 Use the approximate $\tilde{T}^*_{ON}$, $\tilde{T}^*_{F1}$ given in (2-43 & 2-44) to derive the approximate state $\tilde{\underline{X}}^*$ from (2-46) to (2-48).

Step 2 Find a new T^*_{F1} by Newton's method such that for the given $\tilde{X}^*$ and $\tilde{T}^*_{ON}$ together with the new T^*_{F1}, the zero-current condition B_{match} $(\tilde{T}_{ON}, \tilde{\underline{X}}^*, \tilde{T}^*_{F1}) = 0$ will be satisfied.

$$T^*_{F1} = \tilde{T}^*_{F1} - \frac{B_{match}(\tilde{T}^*_{ON}), \tilde{\underline{X}}, \tilde{T}^*_{F1})}{[\partial B_{match}/\partial T_{F1}]_{\tilde{T}^*_{F1}}}$$

Step 3 Check if $S_{match} = 0$ is satisfied.

Step 4 If $S_{match} = 0$ is not satisfied, modify T^*_{ON} according to the equation

$$T^*_{ON} = \bar{T}^*_{ON} - \frac{S_{match}(\bar{T}^*_{ON}, T^*_{F1})}{[\partial S_{match}/\partial T_{ON}]_{\bar{T}^*_{ON}}}$$

Step 5 Use the new T^*_{ON} and T^*_{F1}, calculated in Step 2 and Step 4, to derive a new approximate state $\underline{X}^*$. Then to go to Step 2 and repeat the process until the state matching condition, $S_{match} = 0$, is satisfied.

A flow diagram for determining the steady state is presented in Fig. 2.11(A) and (B). A subroutine B_{match} is developed to search for a proper T_{F1} to satisfy the zero-inductor condition shown in (2-56) This subroutine is contained in another subroutine S_{match} which ultimately computes the state matching condition given in (2-57)

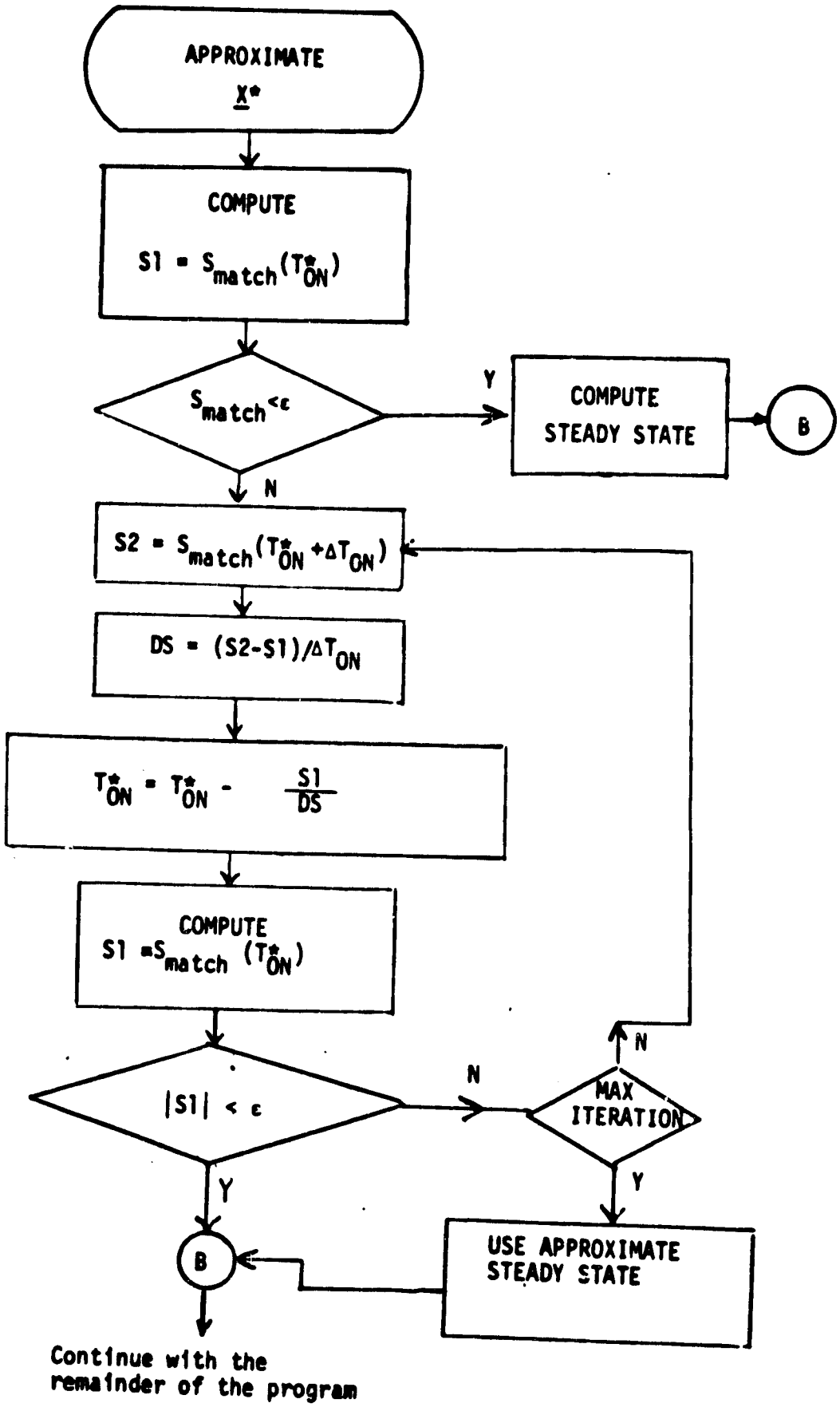


FIGURE 2.11A **FLOW DIAGRAM FOR DETERMINING THE STEADY STATE**

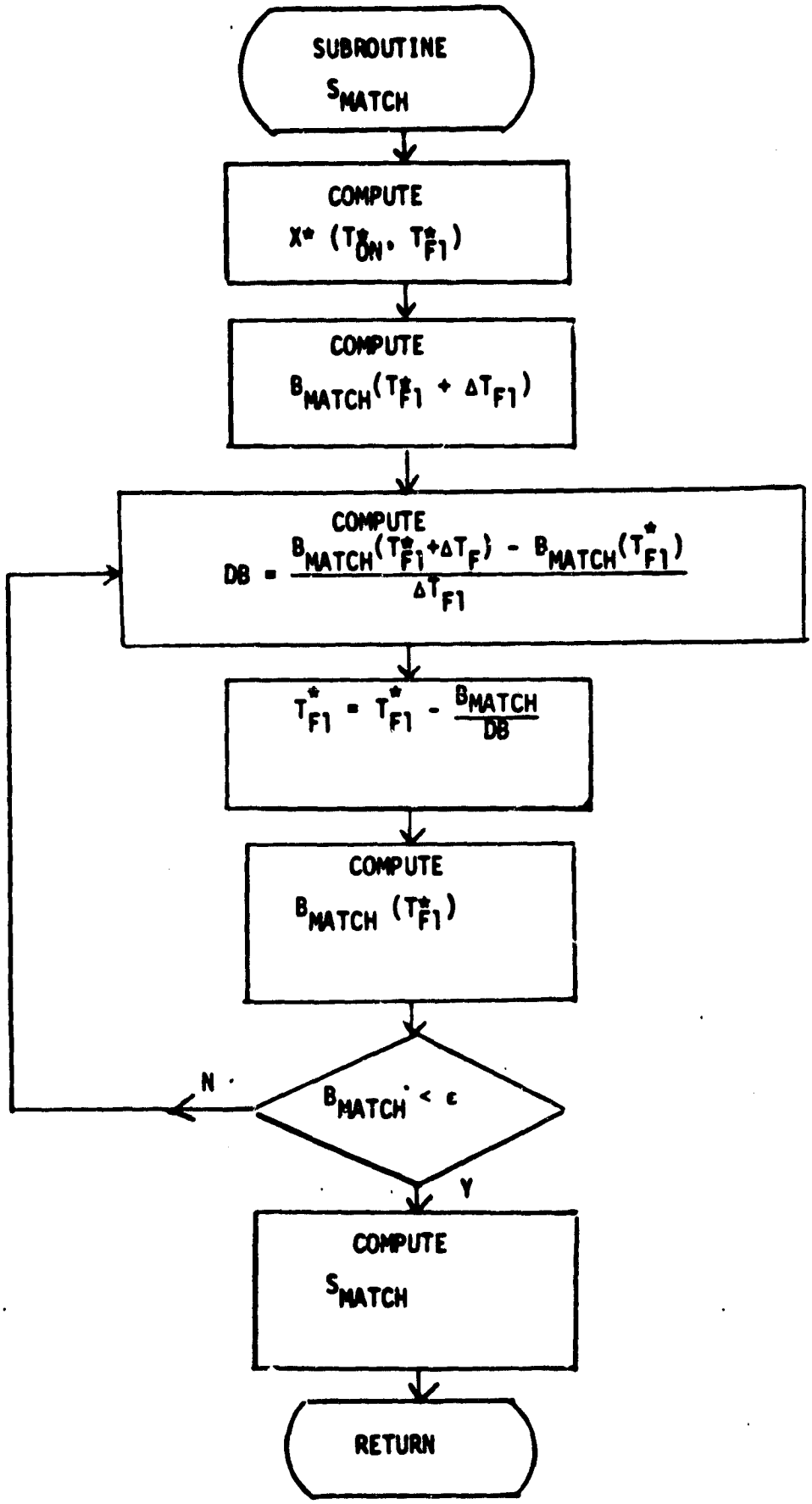


FIGURE 2.11B **FLOW DIAGRAM FOR DETERMINING THE STEADY STATE**

Analysis of Linearized Discrete Time System

The analysis of stability, audio susceptibility, and transient response due to step change in the input voltage and the load, is presented. The analysis is based on a discrete system linearized about its equilibrium state.

Derivation of the Linearized System

The linearized system can be derived by perturbing the system at the kth cycle. After the perturbation the nonlinear discrete time system equation (2-35) can be rewritten as:

$$\underline{x}_{k+1} = \underline{f}\,(\underline{x}_k, \underline{U})$$

$$\begin{aligned} \text{where } \underline{f}\,(\underline{X}_k, \underline{U}) = {} & \phi 3\,(T_{F2}^k)\,\phi 2\,(T_{F1}^k)\,\phi 1\,(T_{ON}^k)\,\underline{x} \\ & + \phi 3\,(T_{F2}^k)\,\phi 2(T_{F1}^k)\,D1\,(T_{ON}^k)\,\underline{U} \\ & + \phi 3\,(T_{F2}^k)\,D2\,(T_{F1}^k)\,\underline{U} \\ & + D3\,(T_{F2}^k)\,\underline{U} \end{aligned} \qquad (2\text{-}55)$$

This system can be linearized about its equilibrium state $\underline{x}^*$.

If the following two terms are defined:

$$\delta\underline{x}\,(t_k) = \underline{x}\,(t_k) - \underline{x}^*$$

and

$$\delta U_1\,(t_k) = U_1\,(t_k) - U_1^*$$

it follows that:

$$\delta\underline{x}\,(t_{k+1}) = \psi\,\delta\underline{x}\,(t_k) + \Gamma\delta U_1\,(t_k) \qquad (2\text{-}56)$$

where $\psi = \frac{\partial}{\partial x} \underline{f}\,(\underline{x}_k, \underline{U}_1)\,\Big|_{\underline{x}^*,\, \underline{U}^*}$ (2-57)

and $\Gamma = \frac{\partial}{\partial U_1} \underline{f}\,(\underline{x}_k, \underline{U})\,\Big|_{\underline{x}^*,\, \underline{U}^*}$ (2-58)

The matrix ψ is 3x3 and the matrix Γ is 3x1.

The partial derivatives may be approximated by difference quotients, and evaluated numerically.

For sufficiently small Δx_i, $(i = 1, \ldots, 3)$,

$$\psi = \frac{\partial \underline{f}}{\partial \underline{x}}\Big|_{\underline{x}^*,\, \underline{U}^*} \approx \begin{bmatrix} \frac{f_1(x_1^*+\Delta X_1) - f_1(x_1^*)}{\Delta x_1} & \cdots & \frac{f_1(x_3^*+\Delta x_3) - f_1(x_3^*)}{\Delta x_3} \\ \vdots & & \vdots \\ \frac{f_3(x_1^*+\Delta x_1) - f_3(x_1^*)}{\Delta x_1} & \cdots & \frac{f_3(x_3^*+\Delta x_3) - f_3(x_3^*)}{\Delta x_3} \end{bmatrix} \tag{2-59}$$

Since $\underline{x}$ does not appear explicitly in $\underline{f}$, the change of T_{on}, T_{F1}, and T_{F2} due to a change of Δx_i, $i = 1 \ldots, 3$, must be determined first in evaluating (2-59). The new T_{on} and T_{F1} are computed according to the threshold conditions (2-36) and (2-37).

Similarly,

$$\Gamma = \frac{\partial f}{\partial u_1}\Big|_{\underline{x}^*,\, \underline{U}^*} \approx \begin{bmatrix} \frac{f_1(U_1+\Delta U_1) - f_1(U_1)}{\Delta U_1} \\ \vdots \\ \frac{f_3(U_1+\Delta U_1) - f_3(U_1)}{\Delta U_1} \end{bmatrix}_{\underline{x}^*,\, \underline{U}^*} \tag{2-60}$$

It is important to select the appropriate increments Δx_j and ΔU_l. Some experimentation with the increment size is advisable, since the accuracy of the partial derivatives depends on it. If the linearized system shows high sensitivity, that is, changes its behavior rather rapidly as it moves away from equilibrium, then the results obtained for the linearized system are valid only for very small perturbations about the equilibrium state.

The Stability of the Linearized System

The linearized system

$$\delta \underline{x}(t_{k+1}) = \psi\, \delta \underline{x}\,(t_k) + \Gamma \delta U_l(t_k),$$

is stable if and only if all the eigenvalues of ψ are absolutely less than unity, i.e.,

$$|\lambda_i| < 1 \qquad i = 1, 2, 3, 4 \tag{2-61}$$

The eigenvalues are evaluated by the computer. Changes of eigenvalues as a function of system parameters can be plotted in the complex plane. The location of the eigenvalues in the complex plane indicates not only the stability but also the transient behavior of the system, i.e., damping and rapidity of response.

2.3.1.2 Buck Converter with Constant Off-Time Duty Cycle Control

The basic structure, and analysis approach, for the buck PAS program with constant off-time duty cycle control are the same as for the constant frequency buck PAS program. The differences between the two converter schemes exist in the procedures for the computations of the converter switching times.

Constant off-time, T_F, as defined in the context of previous converter analyses, is the total time that the switching transistor remains off during a switching cycle. Therefore,

$$T_F \equiv T_{F1} + T_{F2} \equiv \text{constant} \tag{2-62}$$

Arbitrarily, T_F has been assigned the value of the sum of T_{F1} and T_{F2}, determined for the constant frequency buck converter operating in MODE 1.

The expression of conservation of power for the buck converter is given as:

$$T_{ØN}^2 = \frac{2\, L_o\, T_P\, P_o}{E_I\,(E_I - E_R)} \tag{2-63}$$

Substituting $T_P = T_{ON} + T_F$ in the above equation results in the following quadratic equation for $T_{ØN}$:

$$E_I(E_I - E_R)\, T_{ØN}^2 - 2\, L_o\, P_o\, T_{ØN} - 2\, L_o\, P_o\, T_F = 0 \tag{2-64}$$

Solving this quadratic equation for $T_{ØN}$ gives the following expression:

$$T_{ØN} = \frac{L_o\, P_o + \sqrt{(L_o\, P_o)^2 + E_I(E_I - E_R)(2\, L_o\, P_o\, T_F)}}{E_I(E_I - E_R)} \tag{2-65}$$

Where the "+" sign has been chosen before the square root term since

$$L_o\, P_o < \sqrt{(L_o\, P_o)^2 + E_I(E_I - E_R)(2\, L_o\, P_o\, T_F)} \tag{2-66}$$

As in the constant frequency buck control, the clock pulse initiates the $T_{ØN}$ period. Following the computation of $T_{ØN}$, the other switching times can be readily computed:

$$T_{F1} = \frac{(E_I - E_R)}{E_R} * T_{ØN} \tag{2-67}$$

$$T_{F2} = T_F - T_{F1} \tag{2-68}$$

$$T_P = T_{ØN} + T_F \tag{2-69}$$

The sequence of testing for the duty cycle scheme and inductor MMF mode of operation is illustrated in the computational flow chart presented in Figure 2.12. As in the constant frequency buck PAS program, the error criterion for MODE 2 operation is that T_{F2} is greater than EPS = 1.E-6.

The buck PAS program (Appendix A, Volume II) is written such that one computer program package may be used to analyze both duty cycle control schemes operating in either continuous or discontinuous inductor MMF mode.

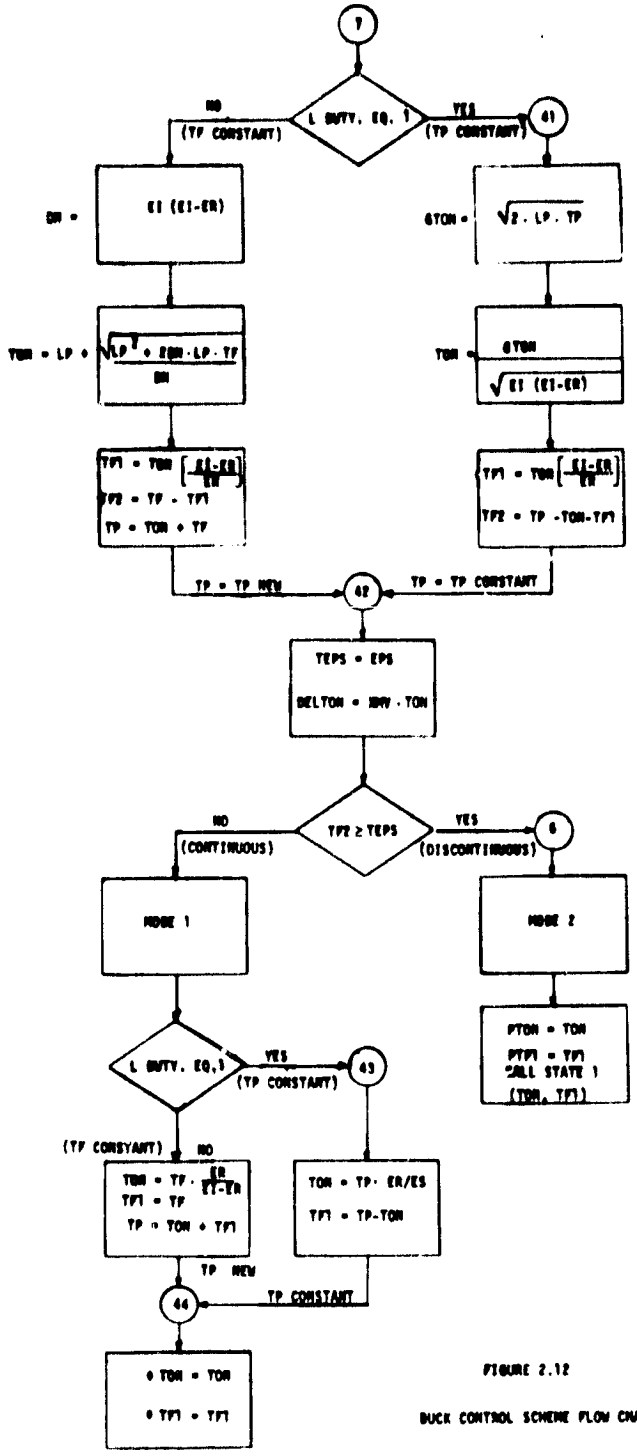


FIGURE 2.12

BUCK CONTROL SCHEME FLOW CHART

2.3.2 Boost DC-DC Converter

2.3.2.1 Boost Converter with Constant Frequency Duty Cycle Control

Given the boost circuit of Figure 2.13, and the state and input vectors defined above, the state equations can be readily determined. To facilitate the development of the state equations, two dummy variables, the voltage e_1 and the current i_D, as defined in Figure 2.13, are introduced. The resulting generalized state equations for all modes of operation within each switching cycle can be expressed in terms of the state and dummy variable and inputs.

$$\dot{v}_c = -\frac{1}{C_o(R_L + R_s)} \cdot v_c + \frac{R_L}{C_o\,(R_L + R_s)} \cdot i_D \tag{2-70}$$

$$\frac{di}{dt} = -\frac{R_o}{L_o} \cdot i - \frac{1}{L_o} \cdot e_1 + \frac{1}{L_o} \cdot E_I \tag{2-71}$$

$$\dot{e}_R = -\frac{1}{C_2R_5} \cdot e_R + \frac{1}{C_2R_C} \cdot \frac{R_L}{(R_L + R_S)} \cdot v_c + \frac{1}{C_2R_5} \cdot \left(\frac{R_SR_L}{R_L + R_S}\right) \cdot i_D \tag{2-72}$$

$$\begin{aligned}\dot{e}_c = {} & \left[-\frac{1}{C_1R_5} - \frac{1}{C_1R_2}\left(\frac{R_2}{R_L + R_S}\right)\right] \cdot \left(\frac{R_L}{R_L + R_S}\right) \cdot v_c + \left(\frac{nR_o}{C_1R_4}\right) \cdot i + \left(\frac{1}{C_1R_5}\right) \cdot e_R \\ & + \left[-\frac{1}{C_1R_5} - \frac{1}{C_1R_3}\left(\frac{R_2}{R_1 + R_2}\right)\right] \cdot \left(\frac{R_L\ R_S}{R_L + R_S}\right) \cdot i_D + \left(\frac{n}{C_1R_4}\right) \cdot e_1 \\ & + -\frac{n}{C_1R_4} E_I \cdot + \frac{1}{C_1R_3} \cdot E_R\end{aligned} \tag{2-73}$$

Similarly, the output voltage, e_o, can be written:

$$e_o = \left(\frac{R_L\ R_S}{R_L + R_S}\right) \cdot i_D + \left(\frac{R_L}{R_L + R_S}\right) \cdot v_c \tag{2-74}$$

The general form of the state equations is:

$$\underline{\dot{x}} = \underline{F_i}\, x + \underline{G_i}\, \underline{u}$$

where i = 1, 2 and 3 refer to the times T_{on}, T_{F_1}, and T_{F_2}, respectively.

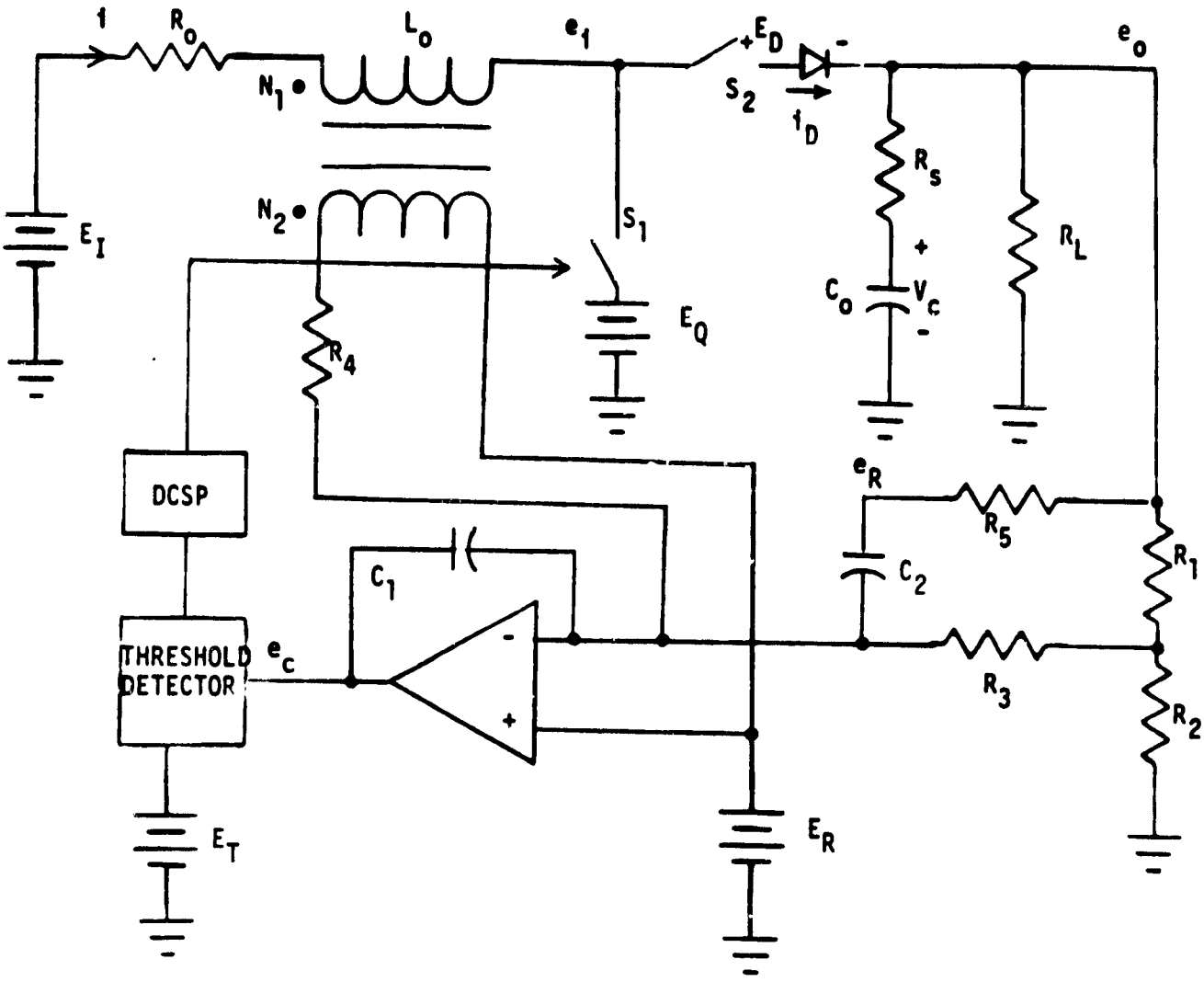


FIGURE 2.13 BOOST CONVERTER

During T_{on}, the power switch S_1 is on and the power diode S_2 is off. Therefore, the dummy variables are set to the following values:

$$e_1 = E_Q$$
$$i_D = o$$

Consequently, Fl and Gl can be expressed as follows:

$$Fl = \begin{bmatrix} fl_{11} & o & o & o \\ o & fl_{22} & o & o \\ fl_{31} & o & fl_{33} & o \\ fl_{41} & fl_{42} & fl_{43} & o \end{bmatrix} \tag{2-75}$$

$$Gl = \begin{bmatrix} o & o & o & o \\ gl_{21} & o & gl_{23} & o \\ o & o & o & o \\ gl_{41} & gl_{42} & gl_{43} & o \end{bmatrix} \tag{2-76}$$

where

$$fl_{11} = \frac{1}{-C_o(R_S + R_L)} \quad fl_{22} = -\frac{R_o}{L_o} \quad fl_{31} = \frac{1}{C_2 R_5}\left(\frac{R_L}{R_L + R_S}\right)$$

$$fl_{33} = -\frac{1}{C_2 R_R} \quad fl_{41} = -\left[\frac{1}{C_1 R_5} + \frac{1}{C_1 R_3}\left(\frac{R_2}{R_1 + R_2}\right)\right]\left(\frac{R_L}{R_L + R_5}\right)$$

$$fl_{42} = \frac{nR_o}{C_1 R_4} \quad fl_{43} = \frac{1}{C_1 R_5} \quad gl_{21} = -gl_{23} = \frac{1}{L_o}$$

$$gl_{41} = -\frac{n}{C_1 R_4} \quad gl_{42} = \frac{1}{C_1 R_3} \quad gl_{43} = \frac{n}{C_1 R_4}$$

The output voltage becomes:

$$e_o = \frac{R_L}{R_L + R_S} \cdot v_c \tag{2-77}$$

During T_{F1}, the power switch S_1 is off and the power diode S_2 is on. Therefore, e_1 and i_D are:

$$e_1 = \frac{R_L}{R_S + R_L} \cdot v_c + \frac{R_S R_L}{R_S + R_L} \cdot i + E_D \tag{2-78}$$

$$i_D = i \tag{2-79}$$

The resulting F2 and G2 are:

$$F2 = \begin{bmatrix} f2_{11} & f2_{12} & o & o \\ f2_{21} & f2_{22} & o & o \\ f2_{31} & f2_{32} & f2_{33} & o \\ f2_{41} & f2_{42} & f2_{43} & o \end{bmatrix} \tag{2-80}$$

$$G2 = \begin{bmatrix} o & o & o & o \\ g2_{21} & o & o & g2_{24} \\ o & o & o & o \\ g2_{41} & g2_{42} & o & g2_{44} \end{bmatrix} \tag{2-81}$$

where

$$f2_{11} = -\frac{1}{C_o(R_L + R_S)}; \quad f2_{12} = \frac{1}{C_o}\frac{R_L}{(R_L + R_S)}; \quad f2_{21} = \frac{R_L}{L_o(R_S + R_L)}$$

$$f2_{22} = -\left(R_o + \frac{R_S R_L}{R_L + R_S}\right)\frac{1}{L_o}; \quad f2_{31} = \frac{1}{C_2 R_5}\left(\frac{R_L}{R_L + R_S}\right)$$

$$f2_{32} = \frac{1}{C_2 R_5}\left(\frac{R_S R_L}{R_L + R_S}\right); \quad f2_{33} = -\frac{1}{C_2 R_5}$$

$$f2_{41} = -\left[\frac{1}{C_1 R_3}\left(\frac{R_2}{R_1 + R_2}\right) + \frac{1}{C_1 R_5} - \frac{n}{C_1 R_4}\right]\left(\frac{R_L}{R_L + R_S}\right)$$

$$f2_{42} = \frac{nR_o}{C_1R_4} - \left[\frac{1}{C_1R_3}\left(\frac{R_2}{R_1+R_2}\right) + \frac{1}{C_1R_5} - \frac{n}{C_1R_4}\right]\left(\frac{R_SR_L}{R_L+R_S}\right)$$

$$f2_{43} = \frac{1}{C_1R_5}\ ; \quad g2_{21} = -g2_{24} = \frac{1}{L_o}\ ; \quad g2_{41} = \frac{n}{C_1R_4}$$

$$g2_{42} = \frac{1}{C_1R_3}\ ; \quad g2_{44} = \frac{n}{C_1R_4}$$

The output voltage e_o is now

$$e_o = \left(\frac{R_L}{R_S+R_L}\right) \cdot v_c + \left(\frac{R_SR_L}{R_S+R_S}\right) \cdot i \tag{2-82}$$

During T_{F_2}, the inductor current has gone to zero and both the power switch S_1 and the power diode S_2 are off. The dummy variables take on the following values.

$$e_i = E_I$$
$$i_D = i = 0$$

The F3 and G3 matrices discribing this mode of circuit operation are:

$$F3 = \begin{bmatrix} f3_{11} & o & o & o \\ o & o & o & o \\ f3_{31} & o & f3_{33} & o \\ f3_{41} & o & f3_{43} & o \end{bmatrix} \tag{2-83}$$

$$G3 = \begin{bmatrix} o & o & o & o \\ o & o & o & o \\ o & o & o & o \\ o & g3_{42} & o & o \end{bmatrix} \tag{2-84}$$

where

$$f3_{11} = -\frac{1}{C_o(R_L + R_S)}; \qquad f3_{31} = \left(\frac{1}{C_2R_5}\right) \cdot \left(\frac{R_L}{R_L + R_S}\right)$$

$$f3_{33} = -\frac{1}{C_2R_5}; \qquad f3_{41} = -\left[\left(\frac{1}{C_1R_3}\right) \cdot \left(\frac{R_2}{R_1 + R_2}\right) - \frac{1}{C_1R_5}\right]\left(\frac{R_L}{R_L + R_S}\right)$$

$$f3_{43} = \frac{1}{C_1R_5}; \qquad g3_{42} = \frac{1}{C_1R_3}$$

The output voltage, e_o, is the same as during T_{on}:

$$e_o = \frac{R_L}{R_L + R_S} \cdot v_c \tag{2-85}$$

By transforming the state equations into the state transistion format (Ref.) the preceeding equation sets may be represented in standard form:

$$\underline{X}_{k+1} = \underline{\Phi 1 X_k} + \underline{D1}\ \underline{u}$$

During each time duration within a switching cycle, the following state transition and control distribution matrices are generated

For T_{on},

$$\Phi 1 = \begin{bmatrix} \phi 1_{11} & o & o & o \\ o & \phi 1_{22} & o & o \\ \phi 1_{31} & o & \phi 1_{33} & o \\ \phi 1_{41} & \phi 1_{42} & \phi 1_{43} & 1 \end{bmatrix} \qquad D1 = \begin{bmatrix} o & o & o & o \\ d1_{21} & o & d1_{23} & o \\ o & o & o & o \\ d1_{41} & d1_{42} & d1_{43} & o \end{bmatrix}$$

For T_{F_1},

$$\Phi 2 = \begin{bmatrix} \phi 2_{11} & \phi 2_{12} & o & o \\ \phi 2_{21} & \phi 2_{22} & o & o \\ \phi 2_{31} & \phi 2_{32} & \phi 2_{33} & o \\ \phi 2_{41} & \phi 2_{42} & \phi 2_{43} & 1 \end{bmatrix} \qquad D2 = \begin{bmatrix} d2_{11} & o & o & d2_{14} \\ d2_{21} & o & o & d2_{24} \\ d2_{31} & o & o & d2_{34} \\ d2_{41} & d2_{42} & o & d2_{44} \end{bmatrix}$$

For T_{F_2},

$$\Phi 3 = \begin{bmatrix} \phi 3_{11} & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ \phi 3_{31} & 0 & \phi 3_{33} & 0 \\ \phi 3_{41} & 0 & \phi 3_{43} & 0 \end{bmatrix} \qquad D\,3 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & d3_{42} & 0 & 0 \end{bmatrix}$$

where

$$\Phi i = e^{FiT}$$

$$Di = e^{FiT}\left[\int_0^T e^{-Fis}\, ds\right] Gi \qquad i = 1, 2, 3$$

By combining the above state transition matrices, the nonlinear discrete state transition equation for a complete switching cycle is obtained.

$$\underline{X}\,(t_{k+1}) = \Phi \underline{X}\,(t_k) + V\,\underline{u}$$

where t_k and t_{k+1} correspond to the time instances at the beginning of the kth cycle and the (k+1)th cycle, respectively. The Φ and V matrics have the following structures:

$$\Phi = \begin{bmatrix} \phi_{11} & \phi_{12} & 0 & 0 \\ \phi_{21} & \phi_{22} & 0 & 0 \\ \phi_{31} & \phi_{32} & \phi_{33} & 0 \\ \phi_{41} & \phi_{42} & \phi_{43} & 1 \end{bmatrix} \qquad V = \begin{bmatrix} V_{11} & 0 & V_{13} & V_{14} \\ V_{21} & 0 & V_{23} & V_{24} \\ V_{31} & 0 & V_{33} & V_{34} \\ V_{41} & V_{42} & V_{43} & V_{44} \end{bmatrix}$$

From the structure of Φ, it is apparent that the next values of X_1, X_2 and X_3 are independent of past values of X_4, a property which is useful in determining the steady state solution.

Analysis

In order to approximate the steady-state solution necessary for the linearized system analysis, the approximate switching times T_{ON}, TF1, and TF2 must be computed. The following formulae may be used:

$$T_{ON} = \sqrt{\frac{2L_0T_pP_o\ (E_0 + E_D - E_I)}{\eta\ E_I\ (E_I-E_Q)(E_0+E_D-E_Q)}} \tag{2-86}$$

$$T_{F1} = \sqrt{\frac{2L_0T_pP_o\ (E_I - E_Q)}{\eta\ E_I\ (E_0+E_D-E_I)(E_0+E_D-E_Q)}} \tag{2-87}$$

$$T_{F2} = T_P - T_{ON} - T_{F1} \tag{2-88}$$

where

L_0 = the energy storage inductance
P_0 = output power
η = efficiency
E_I = input voltage
E_0 = output voltage
E_Q = saturation voltage drop of the power transistor
E_D = forward voltage drop of the diode

The expressions for T_{ON} and TF1 are generated based on the flux and energy conservation principles given below (refer to Figure 2.13):

Flux Conservation

$$TON(EI - EQ) = TF1(EO + ED - EI) \tag{2-89}$$

Energy Conservation

$$\frac{\eta EI(EI - EQ)\ TON^2}{2LT_p} + \frac{\eta EI(EO + ED - EI)\ TF1^2}{2LT_p} = P_o \tag{2-90}$$

For the computation of the approximate steady-state solution, $\underline{X}^*$, the following state transition equation is solved:

$$\underline{X}^* = \Phi\ \underline{X}^* + \underline{V}\ \underline{U}$$

Therefore:

$$X^* = [I - \phi]^{-1} \underline{V}\,\underline{U}$$

By imposing the property of the state transition matrix, ϕ, noted above, the state variables X_1, X_2 and X_3 can be computed independently of X_4. Therefore, the solution of the steady-station expression may be partitioned such that only a 3x3 matrix need be inverted to solve for the X_1, X_2, and X_3 states. The existing voltage restriction on X_4 (t_k) [capacitor C_1 voltage in Figure 2.13] is used to solve for X_4. The following expressions are the closed form solutions for the approximate steady-state vector:

$$X1 = [(1-\phi_{22})\,\underline{VU}_1 + \phi_{12}\,VU_2]/DEN \qquad (2\text{-}91)$$

$$X2 = \begin{cases} [\phi_{21}\,\underline{VU}_1 + (1-\phi_{11})\,VU_2]/DEN & MODE = 1 \\ 0 & MODE = 2 \end{cases} \qquad (2\text{-}92)$$

$$X3 = [(\phi_{21}\,\phi_{32} + \phi_{31}\,(1-\phi_{22}))\,\underline{VU}_1 + (\phi_{32}\,(1-\phi_{11}) + \phi_{12}\,\phi_{31})\,\underline{VU}_2)]/DET + \underline{VU}_3/(1-\phi_{33}) \qquad (2\text{-}93)$$

$$X4 = ET - \phi 1_{41}\,X1 - \phi 1_{42}\,X2 - \phi 1_{43}\,X3 - d1_{41}\,U1 - d1_{42}\,U2 - d1_{43}\,U3 - d1_{44}\,U4 \qquad (2\text{-}94)$$

The voltage restriction on $X4(t_k)$ [e_{c1} (Figure 2.13)]

where

$$\underline{VU} = \underline{V}\,\underline{U}$$

$$DEN = (1-\phi_{11})(1-\phi_{22}) - \phi_{12}\,\phi_{21}$$

$$DET = (1-\phi_{33})\,DEN$$

$$MODE = \begin{cases} 1 & \text{continuous inductor current operation} \\ 2 & \text{discontinuous inductor current operation} \end{cases}$$

The performance of PAS2 (Appendix B), Volume II, with these computation procedures was checked out.

Continuous Inductor Current Mode of Operation

In order to make it complete in its capability of analyzing converters, PAS2 was modified to incorporate the continuous inductor current mode of operation. The appropriate subroutines requiring modifications were:

1) PAS2
2) STATE2
3) PSIM2
4) FFUNC2
5) GAMM2

Linearized System Analysis

The eigenvalues of the Jacovian matrix characterize the linearized system stability and indicate the system transient behavior, i.e., damping and response time.

The system eigenvalues, as functions of the circuit parameters, are computed numerically. In order to characterize the stability boundaries (if relevant) of the linearized system, these eigenvalues are parametically plotted on the Z-plane and analyzed with respect to stability and response criterion.

Eigenvalues near the positive real axis of the Z-plane indicate that the system has a long time constant; eigenvalues equal to zero in discontinuous current mode indicate that the inductor current state variable sampled at any cycle is insensitive to the state variable in the previous cycle. The indictor current translates to zero following any small signal perturbation.

2.3.2.2 Boost Converter with Constant Off-Time Duty Cycle Control

The primary structure, and analysis approach, of the boost PAS program for constant off-time duty cycle control are the same as for the constant frequency boost PAS program except for differences in the evaluation of the converter switching times.

Off-time, T_F, as defined in the context of previous converter analyses, is the total time that the switching transformer remains off during a switching cycle. Therefore:

$$T_F = T_{F1} + T_{F2} \tag{2-95}$$

In constant off-time control, T_F is held constant while T_{F1} and T_{F2} are allowed to vary. Arbitrarily, T_F has been assigned the value determined for the constant frequency boost converter operating in MODE 2.

The conservation of power for the boost converter may be represented by the equation:

$$T_{ØN}^2 = \frac{2\, L_o\, P_o\, T_p\, (E_O + E_D - E_I)}{\eta\, E_I\, (E_I - E_Q)(E_O + E_D - E_Q)} \tag{2-96}$$

Substituting the expression $T_p = T_{ON} + T_F$ in the above equation results in the following quadratic equation for $T_{ØN}$:

$$\eta\, E_I\, (E_I - E_Q)(E_O + E_D - E_Q)\, T_{ØN}^2 - 2\, L_o\, P_o\, (E_O + E_D - E_I)\, T_{ØN} - 2\, L_o\, P_o\, (E_O + E_D - E_I)\, T_F = 0 \tag{2-97}$$

Therefore, solving this quadratic equation for $T_{ØN}$ gives the following solution:

$$T_{ØN} = \frac{QB + \sqrt{QB^2 + 4\, QA\, QC}}{2QA} \tag{2-98}$$

where

$$QA = n\, E_I\, (E_I - E_Q)(E_O + E_D - E_Q)$$

$$QB = -2\, L_o\, P_o\, (E_O + E_D - E_I)$$

$$QC = QB \cdot T_F$$

and where the positive sign has been chosen before the square root since

$$QB < \sqrt{(QB^2) + 4 \cdot QA \cdot QC}$$

As in constant frequency boost control, the clock pulse initiates the $T_{\emptyset N}$ period. Following the computation of $T_{\emptyset N}$, the other switching times can be readily computed:

$$T_{F1} = T_{\emptyset N} \cdot \frac{(E_I - E_Q)}{E_O + E_D - E_I} \tag{2-99}$$

$$T_{F2} = T_P - T_{\emptyset N} - T_{F1} \tag{2-100}$$

$$T_P = T_{\emptyset N} + T_F \tag{2-101}$$

The testing sequence for the constant off-time duty cycle scheme and the different inductor MMF modes of operation are illustrated in the computational flow chart presented in Figure 2-14. As in the revised constant frequency boost converter PAS program, the error criterion for MODE 2 operation is that T_{F2} must be greater than 1% of the switching period.

The boost PAS2 program (Appendix B, Volume II) is written such that one computer program package may be used to analyze both duty cycle control schemes operating in either continuous or discontinuous inductor MMF mode.

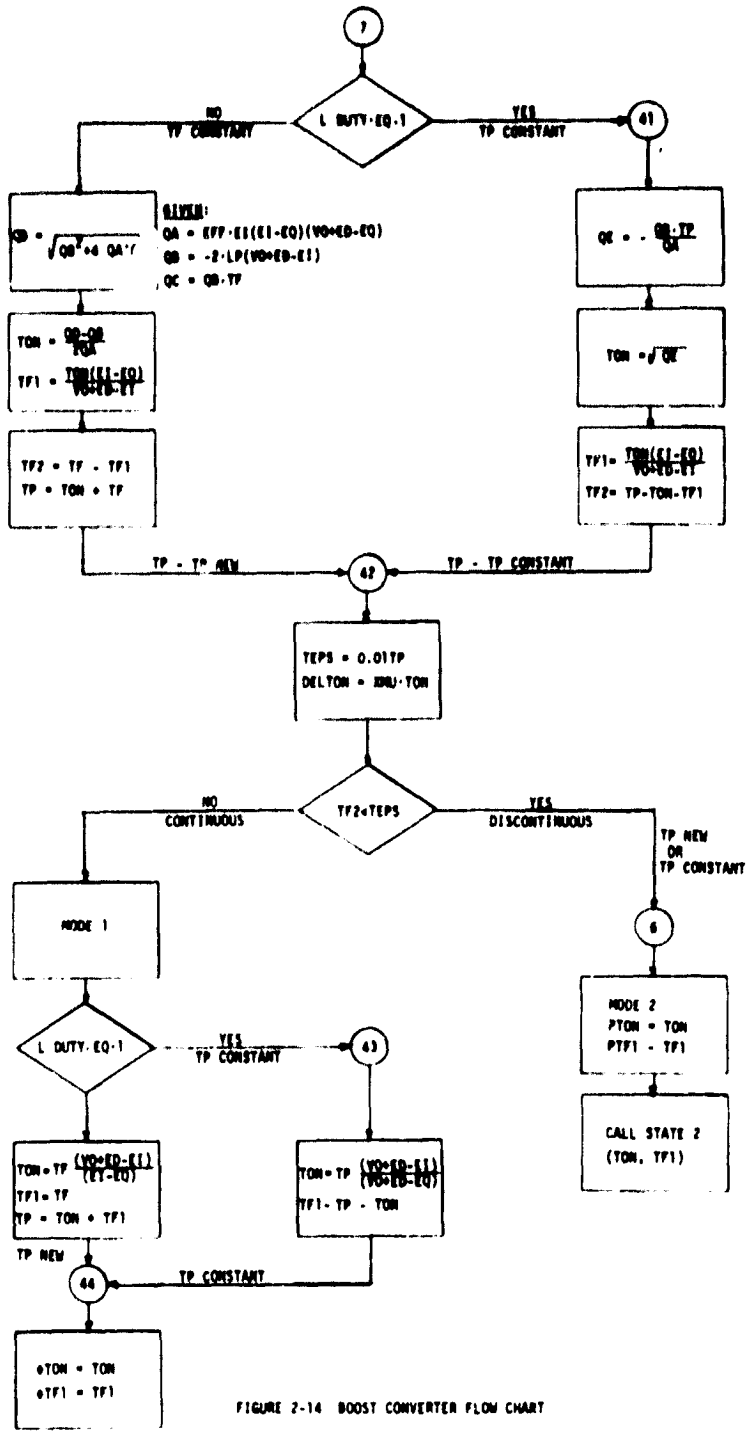


FIGURE 2-14 BOOST CONVERTER FLOW CHART

2.3.3 Buck Boost DC-DC Converter

2.3.3.1 Buck Boost Converter with Constant Frequency Duty Cycle Control

Figure 2-15 prese. . he circuit configuration of the buck-boost converter with a constant frequency duty cycle scheme.
As opposed to the inductor current state variable representation utilized in the previous BUCK and BOOST power converter analysis programs, the inductor flux, which is continuous, replaces the discontinuous inductor current as a system state variable. Therefore, the state and input vectors, $\underline{X}$ and $\underline{U}$ are defined as:

$$\underline{X} \triangleq \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \end{bmatrix} = \begin{bmatrix} V_C \\ \text{Flux} \\ e_R \\ e_C \end{bmatrix} \tag{2-102}$$

$$\underline{U} = \begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ U_4 \end{bmatrix} = \begin{bmatrix} E_I \\ E_R \\ E_Q \\ E_D \end{bmatrix} \tag{2-103}$$

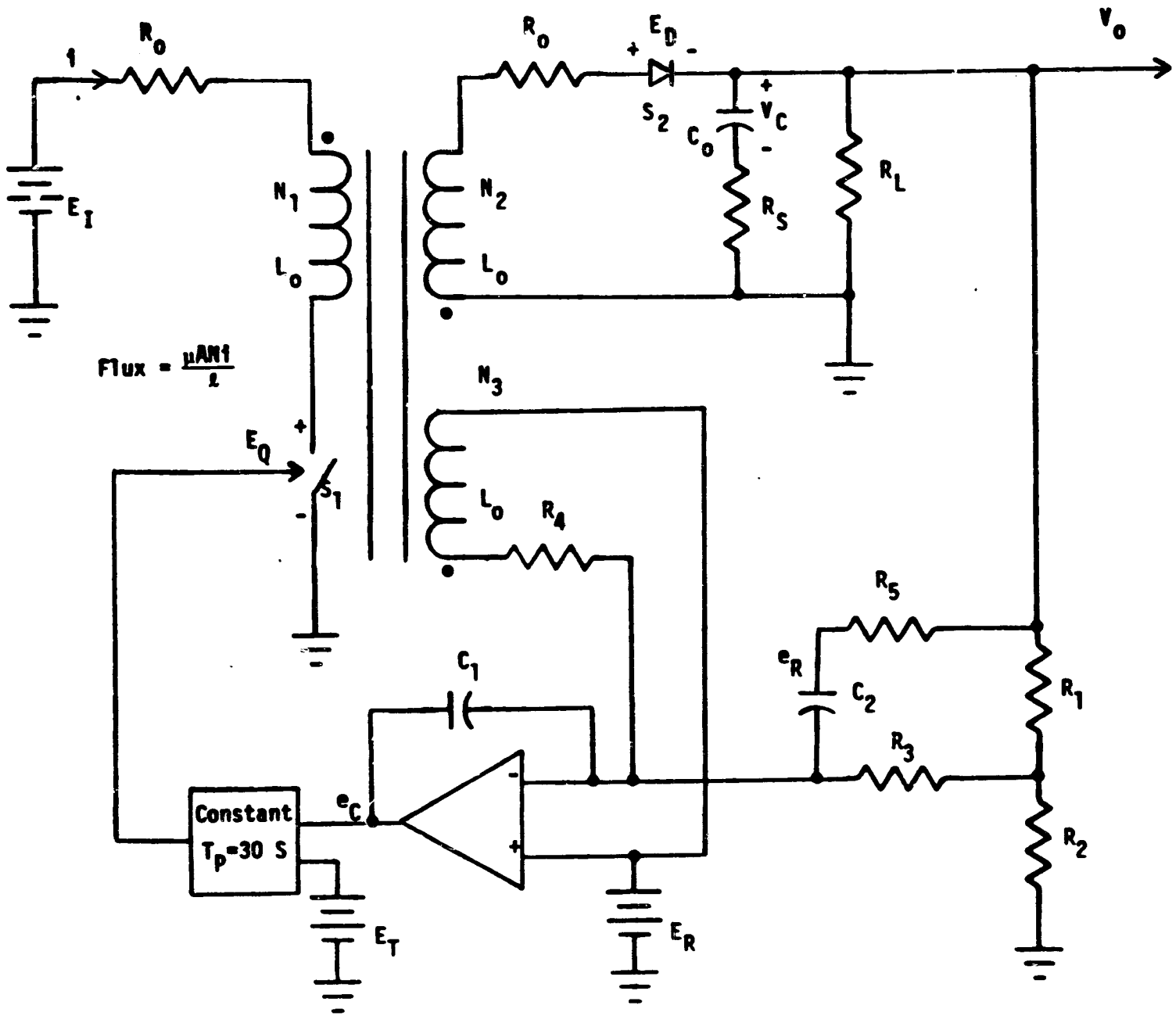


FIGURE 2-15 BUCK BOOST CONVERTER

The constraints on this system are:

1) $X_4(t_k^1) = e_C(t_k^1) = E_T$ (2-104)

2) $X_2(t_k^2) = \text{Flux}(t_k^2) = 0$ (2-105)

3) $T_{ON}^k + T_{F1}^k + T_{F2}^k = T_P$ (2-106)

In order to utilize the inductor flux as a state variable, the magnetization characteristics of the inductor have been quantified. The flux is expressed by the following equation:

$$\text{Flux} = \frac{\mu A N i}{\ell}$$

where $\mu \equiv$ permeability or the ratio of the flux density to the magnetizing force

$A \equiv$ cross-sectional area

$\ell \equiv$ length

$N \equiv$ number of turns

$i \equiv$ current

For convenience in deriving the state equations, a constant k is defined:

$$k \equiv \frac{\mu A}{\ell}$$

Therefore, the expression for Flux may be written:

$$\text{Flux} = kNi = \frac{Li}{N}$$

The following expression for k can then be utilized for the resulting equation set:

$$k = \frac{L}{N^2}$$

where k is in units of webers per amp-turns.

In the derivation of the state equations, it is convenient to define the current i in the following manner:

$$i = K_p \text{ Flux}, \qquad \text{where } K_p = \frac{k^{-1}}{N}$$

During the T_{ON} period, when the switching transistor is on and the diode is off, the following set of equations describes the power converter operation:

$$\dot{v}_c = -\frac{1}{C_0(R_S+R_L)} v_c \tag{2-107}$$

$$\dot{\text{Flux}} = -\frac{R_0}{L_0}\text{Flux} + \frac{E_I}{N_1} - \frac{E_Q}{N_1} \tag{2-108}$$

$$\dot{e}_R = \frac{1}{C_2R_5} \cdot \frac{R_L}{R_L+R_S} \cdot v_c - \frac{1}{C_2R_5} \cdot e_R \tag{2-109}$$

$$\begin{aligned}\dot{e}_c = &-\left[\frac{1}{C_1R_5} + \frac{R_2}{C_1(R_1R_2+R_3(R_1+R_2))}\right]\frac{R_L}{R_L+R_S} v_c + \frac{N_3R_0}{C_1R_4L_0}\text{Flux} \\ &+ \frac{1}{C_1R_5} e_R - \frac{1}{C_1R_4}\frac{N_3}{N_1} \cdot E_I + \frac{1}{C_1\left(R_3+\frac{R_1R_2}{R_1+R_2}\right)} \cdot E_R \\ &+ \frac{1}{C_1R_4}\frac{N_3}{N_1} E_Q\end{aligned} \tag{2-110}$$

$$v_o = \frac{R_L}{R_L+R_S} v_c \tag{2-111}$$

During the T_{F1} period when the switching transistor is off and the power diode is on, the following equation set describes the system:

$$\dot{v}_c = -\frac{1}{C_0(R_L+R_S)} v_c + \frac{R_L}{C_0(R_L+R_S)} K_p \text{ Flux} \tag{2-112}$$

$$\dot{\text{Flux}} = -\left(\frac{R_L}{R_L+R_S}\right)\frac{1}{N_2} v_c - \left(\frac{R_S R_L}{R_L+R_S} + R_0\right)\frac{1}{L_0}\text{Flux} - \frac{1}{N_2} E_D \tag{2-113}$$

$$\dot{e}_R = \frac{1}{C_2 R_5}\left(\frac{R_L}{R_L+R_S}\right) v_c + \frac{1}{C_2 R_5}\left(\frac{R_S R_L}{R_L+R_S}\right) K_p \cdot \text{Flux} - \frac{1}{C_2 R_5} e_R \tag{2-114}$$

$$\begin{aligned}\dot{e}_c = &-\left(\frac{1}{C_1 R_5} + \frac{R_2}{C_1(R_1R_2+R_3(R_1+R_2))} - \frac{1}{C_1 R_4}\frac{N_3}{N_2}\right)\left(\frac{R_L}{R_S+R_L}\right)\cdot v_c \\ &-\left[\left(\frac{1}{C_1 R_5} + \frac{R_2}{C_1(R_1R_2+R_3(R_1+R_2))} - \frac{1}{C_1 R_4}\frac{N_3}{N_2}\right)\left(\frac{R_S R_L}{R_L+R_S}\right) - \frac{1}{C_1 R_4}\frac{N_3}{N_2} R_0\right] K_p \cdot \text{Flux} \\ &+ \frac{1}{C_1 R_5} e_R + \frac{1}{C_1\left(R_3 + \frac{R_1 R_2}{R_1+R_2}\right)} E_R + \frac{1}{C_1 R_4}\frac{N_3}{N_2} E_D\end{aligned} \tag{2-115}$$

$$v_o = \frac{R_L}{R_L+R_S}\cdot v_c + \frac{R_S R_L}{R_L+R_S} K_p \cdot \text{Flux} \tag{2-116}$$

where

$$K_p = \frac{k^{-1}}{N_2}$$

During the T_{F2} period when both the switching transistor and the power diode are off, the following state equations describe the converter system operation.

$$\dot{v}_c = -\frac{1}{C_0(R_L+R_S)} v_c \tag{2-117}$$

$$\text{Flux} = 0 \tag{2-118}$$

$$\dot{e}_R = \frac{1}{C_2R_5}\left(\frac{R_L}{R_L+R_S}\right) v_c - \frac{1}{C_2R_5} e_R \tag{2-119}$$

$$\dot{e}_c = -\left[\frac{1}{C_1R_5} + \frac{R_2}{C_1(R_1R_2+R_3(R_1+R_2))}\right]\left(\frac{R_L}{R_L+R_S}\right) v_c + \frac{1}{C_1R_5} e_R$$

$$+ \frac{1}{C_1\left(R_3+\frac{R_1R_2}{R_1+R_2}\right)} E_R \tag{2-120}$$

$$v_o = \frac{R_L}{R_L+R_S} v_c \tag{2-121}$$

In matrix representation, the above state equations for each time period may be expressed in the general form:

$$\underline{\dot{x}} = \underline{Fi}\ \underline{X} + \underline{Gi}\ \underline{U} \qquad i = 1,2,3$$

where for T_{ON}

$$F1 = \begin{bmatrix} f1_{11} & 0 & 0 & 0 \\ 0 & f1_{22} & 0 & 0 \\ f1_{31} & 0 & f1_{33} & 0 \\ f1_{41} & f1_{42} & f1_{43} & 0 \end{bmatrix}, \qquad G1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ g1_{21} & 0 & g1_{23} & 0 \\ 0 & 0 & 0 & 0 \\ g1_{41} & g1_{42} & g1_{43} & 0 \end{bmatrix}$$

and for T_{F1}

$$F2 = \begin{bmatrix} f2_{11} & f2_{12} & 0 & 0 \\ f2_{21} & f2_{22} & 0 & 0 \\ f2_{31} & f2_{32} & f2_{33} & 0 \\ f2_{41} & f2_{42} & f2_{43} & 0 \end{bmatrix}, \qquad G2 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & g2_{24} \\ 0 & 0 & 0 & 0 \\ 0 & g2_{42} & 0 & g2_{44} \end{bmatrix}$$

and for T_{F2}

$$F3 = \begin{bmatrix} f3_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ f3_{31} & 0 & f3_{33} & 0 \\ f3_{41} & 0 & f3_{43} & 0 \end{bmatrix}, \qquad G3 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & g3_{42} & 0 & 0 \end{bmatrix}$$

The state transition equations are of the form:

$$X_{k+1} = \phi i \, X_k + Di \, u \qquad i = 1,2,3$$

where

$$\phi 1 = \begin{bmatrix} \phi 1_{11} & 0 & 0 & 0 \\ 0 & \phi 1_{22} & 0 & 0 \\ \phi 1_{31} & 0 & \phi 1_{33} & 0 \\ \phi 1_{41} & \phi 1_{42} & \phi 1_{43} & 1 \end{bmatrix} \quad D1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ d1_{21} & 0 & d1_{23} & 0 \\ 0 & 0 & 0 & 0 \\ d1_{41} & d1_{42} & d1_{43} & 0 \end{bmatrix}$$

and

$$\phi 2 = \begin{bmatrix} \phi 2_{11} & \phi 2_{12} & 0 & 0 \\ \phi 2_{21} & \phi 2_{22} & 0 & 0 \\ \phi 2_{31} & \phi 2_{32} & \phi 2_{33} & 0 \\ \phi 2_{41} & \phi 2_{42} & \phi 2_{43} & 1 \end{bmatrix} \quad D2 = \begin{bmatrix} 0 & 0 & 0 & d2_{14} \\ 0 & 0 & 0 & d2_{24} \\ 0 & 0 & 0 & d2_{34} \\ 0 & d2_{42} & 0 & d2_{44} \end{bmatrix}$$

and $$\phi 3 = \begin{bmatrix} \phi 3_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \phi 3_{31} & 0 & \phi 3_{33} & 0 \\ \phi 3_{41} & 0 & \phi 3_{43} & 1 \end{bmatrix} \quad D3 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & d3_{42} & 0 & 0 \end{bmatrix}$$

<u>Switching Times Analysis</u>

The approximate steady-state switching times may be derived for the constant frequency control case. The boundary condition inherent with this system is that the time T_p is a constant, that is:

$$T_P = T_{ON} + T_{F1} + T_{F2} = \text{constant} \tag{2-122}$$

Due to the conservation of flux in the inductor, the following restriction applies:

$$V_0 + E_D = \frac{N_2}{N_1} (E_I - E_Q) \frac{T_{ON}}{T_{F1}} \tag{2-123}$$

Finally, an expression involving the conservation of power is needed to complete the necessary information for calculating the approximate times:

$$\frac{T_{ON}^2 E_I (E_I - E_Q)}{2LT_p} = \frac{P_o}{\eta} \tag{2-124}$$

Using these expressions, it is possible to derive the following relationships:

$$T_{ON} = \sqrt{\frac{2LT_p P_o}{\eta E_I (E_I - E_Q)}} \tag{2-125}$$

$$T_{F1} = \frac{N_2}{N_1} \left(\frac{E_I - E_Q}{V_0 + E_D}\right) T_{ON} \tag{2-126}$$

$$T_{F2} = T_P - T_{ON} - T_{F1} \tag{2-127}$$

As in the previous material, Mode 1 is the condition that $T_{F2} = 0$ (inductor current is continuous), and Mode 2, the condition that $T_{F2} \neq 0$ (inductor current is discontinuous). Assume that the circuit now operates with a load resistance such that $T_{F2} = 0$. Allow the load to vary uniformly in a direction where inductor current at the end of T_{F1} approaches zero. That value of load resistance at which the inductor current at the end of T_{F1} first becomes zero is a critical resistance. (Equivalently, the value of resistance that first gives a non-zero T_{F2} is a critical resistance). This critical resistance may be found in the following way:

From the power conservation expression, we have:

$$T_{ON}^2 = \frac{2LP_o}{\eta E_I (E_I - E_Q)} (T_{ON} + T_{F1} + T_{F2}) \tag{2-128}$$

From this expression, and using the expression for T_{F1}, we have:

$$T_{F2} = \left[\frac{\eta E_I (E_I - E_Q) R_L T_{ON} - 2LV_0^2 \left(1 + \frac{N_2}{N_1} \left(\frac{E_I - E_Q}{V_0 + E_D}\right)\right)}{2LV_0^2} \right] \cdot T_{ON} \tag{2-129}$$

The critical load resistance may now be found:

$$R_C = \text{critical } R_L = \frac{2LV_0^2 \left(1 + \frac{N_2}{N_1} \left(\frac{E_I - E_Q}{V_0 + E_D}\right)\right)}{\eta E_I (E_I - E_Q) T_{ON}} \tag{2-130}$$

For MODE 2, the switching times are given above. For MODE 1, however, the following times are more easily calculated using the equations:

$$T_{ON} = \frac{T_P}{1 + \frac{N_2}{N_1} \left(\frac{E_I - E_Q}{V_0 + E_D} \right)} \tag{2-131}$$

$$T_{F1} = T_P - T_{ON} \tag{2-132}$$

$$T_{F2} = 0 \text{ (by definition)} \tag{2-133}$$

For the actual PAS program, the criterion for MODE 2 operation is given by the inequality constraint:

$$T_{F2} > 0.01\, T_P$$

that is, T_{F2} must be greater than 1% of the switching period.

Steady-State Solution

Propagating the state variables through a complete switching cycle results in the following expression:

$$\underline{x}(t_{k+1}) = \underline{\phi 3}\ \underline{\phi 2}\ \underline{\phi 1}\ \underline{x}(t_k) + [\underline{\phi 3}\ \underline{\phi 2}\ \underline{D1} + \underline{\phi 3}\ \underline{D2} + \underline{D3}]\ \underline{u} \qquad (2\text{-}134)$$

$$\equiv \underline{\phi}\ \underline{x}(t_k) + \underline{V}\ \underline{u}$$

Since $\underline{x}(t_{k+1}) = \underline{x}(t_k) = \underline{x}^*$, the approximate steady-state $\underline{x}^*$ may be calculated using the following procedure:

$$\underline{x}^* = [I - \underline{\phi}]^{-1}\ \underline{V}\ \underline{u}$$

where $\underline{x}^* = [x_1^*\ x_2^*\ x_3^*]^T$ and

$$x_4^* = E_T - \phi 1_{41}\ x_1^* - \phi 1_{42}\ x_2^* - \phi 1_{43}\ x_3^* - d1_{41}\ u_1 - d1_{42}\ u_2 - d1_{43}\ u_3$$

The exact steady-state solution for the state variables can be computed using a Newton-Raphson iteration algorithm to find the proper T_{ON} and T_{F1}, and hence, $\underline{x}^*$, which satisfy the state matching conditions defined below. The matching condition on the integrator output voltage, S^k_{match}, and on the inductor flux, B^k_{match}, defined below:

$$S^k_{match} = x_4^{k+1} - x_4^k = \phi 3^k_{41}\ z_1^k + \phi 3^k_{43}\ z_3^k + z_4^k + d3^k_{42}\ u_2 - x_4^k$$

$$B^k_{match} = z_2^k = \phi 2^k_{21}\ y_1^k + \phi 2^k_{22}\ y_2^k + D2^k_{24}\ u_4$$

Iterating on T_{ON} and T_{F1} in order to drive these matching conditions to zero results in the proper exact steady-state solution for $\underline{x}$.

Therefore, by defining the following variables

$$\underline{y}(t_k) \equiv \underline{x}(t_k + T^k_{ON}) = \underline{\phi 1}_k\ \underline{x}(t_k) + \underline{D1}_k\ \underline{u}$$

$$\underline{z}(t_k) \equiv \underline{y}(t_k + T^k_{F1}) = \underline{\phi 2}_k\ \underline{y}(t_k) + \underline{D2}_k\ \underline{u}$$

$$\underline{x}(t_{k+1}) \equiv \underline{z}(t_k + T^k_{F2}) = \underline{\phi 3}_k\ \underline{z}(t_k) + \underline{D3}_k\ \underline{u}$$

the state variable boundary conditions may be expressed as:

$$y_4(t_k) = \phi 1_{41}\, x_1(t_k) + \phi 1_{42}\, x_2(t_k) + \phi 1_{43}\, x_3(t_k) + x_4(t_k) + d1_{41}\, u_1 + d1_{42}\, u_2 + d1_{43}\, u_3 = E_T \tag{2-135}$$

$$z_2(t_k) = \phi 2_{21}\, y_1(t_k) + \phi 2_{22}\, y_2(t_k) + d2_{24}\, u_4 = 0 \tag{2-136}$$

$$T_{F2}^{k} = T_P - T_{ON}^{k} - T_{F1}^{k} \tag{2-137}$$

2.3.3.2 Buck-Boost Converter with Constant Off-Time Duty Cycle Control

The basic structure and analysis approach of the buck-boost PAS program for constant off-time duty cycle control is the same as for the constant frequency buck-boost PAS program. The differences between the two converter schemes exist in the procedures for the computations of the converter switching times.

Constant off-time, T_F as defined previously, is the total time that the switching transistor remains off during a switching cycle. Therefore

$$T_F \equiv T_{F1} + T_{F2} \equiv \text{constant} \tag{2-138}$$

Arbitrarily, T_F has been assigned the value of the sum of T_{F1} and T_{F2} determined for the constant frequency buck-boost converter operating in MODE 1.

Conservation of power for the buck-boost converter is expressed in the equation:

$$T_{\emptyset N}^2 = \frac{2\, L_o\, T_p\, P_o}{\eta\, E_I (E_I - E_Q)} \tag{2-139}$$

Substituting for T_p in the above equation results in the following quadratic equation for $T_{\emptyset N}$:

$$\eta\, E_I (E_I - E_Q)\, T_{\emptyset N}^2 - 2\, L_o\, P_o\, T_{\emptyset N} - 2\, L_o\, P_o\, T_F = 0 \tag{2-140}$$

Solving this quadatric equation for $T_{\emptyset N}$ gives:

$$T_{\emptyset N} = \frac{L_o\, P_o + \sqrt{(L_o\, P_o)^2 + \eta\, E_I (E_I - E_Q)(2\, L_o\, P_o\, T_F)}}{\eta\, E_I (E_I - E_Q)} \tag{2-141}$$

Where the "+" sign has been chosen before the square root because

$$L_o\, P_o < \sqrt{(L_o\, P_o)^2 + \eta\, E_I (E_I - E_Q)(2\, L_o\, P_o\, T_F)} \tag{2-142}$$

As in the constant frequency buck-boost control, the clock pulse initiates the $T_{\emptyset N}$ period. Following the computation of $T_{\emptyset N}$, the other switching times can be readily computed:

$$T_{F1} = \frac{(E_I - E_Q)}{} * T_{\emptyset N} \tag{2-143}$$

$$T_{F2} = T_F - T_{F1} \tag{2-144}$$

$$T_P = T_{\emptyset N} + T_F \tag{2-145}$$

The sequence of testing for the duty cycle scheme and inductor MMF mode of operation are illustrated in the computational flow chart presented in Figure 2-16. As in the constant frequency buck-boost PAS program, the threshold criterion for MODE 2 operation is that T_{F2} is greater than 1% of the switching period.

The buck-boost PAS program (Appendix C, Volume II) is written such that one computer program package may be used to anlayze both duty cycle control schemes operating in either continuous or discontinuous inductor MMF mode.

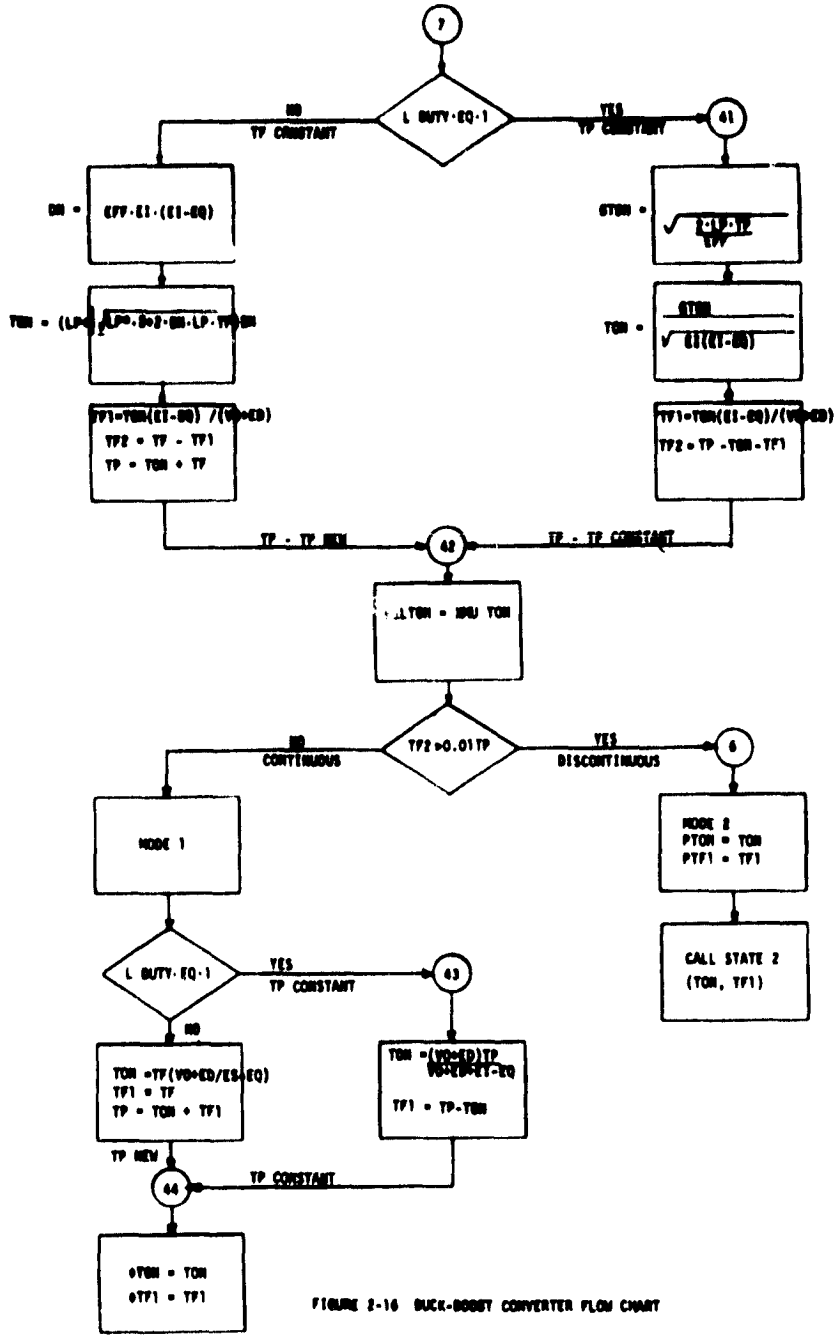


FIGURE 2-16 BUCK-BOOST CONVERTER FLOW CHART

2.4 Computer Programs.

Computer programs have been generated using the three mathematical models described. Figure 2-17 shows the general information flow chart for a composite subprogram including both continuous and discontinuous inductor current operation, and constant frequency or constant off-time control.

The performance analysis computer flow diagrams are included as part of Appendix A through C, Volume II, for the buck, boost, and buck-boost regulators, respectively. Although the programs are similar, that for the buck-boost is most complex. In review of the presently available data, it seems reasonable that the buck-boost computer program can be modified so that it is capable of performing the buck, boost and buck-boost DC-DC converter performance analysis.

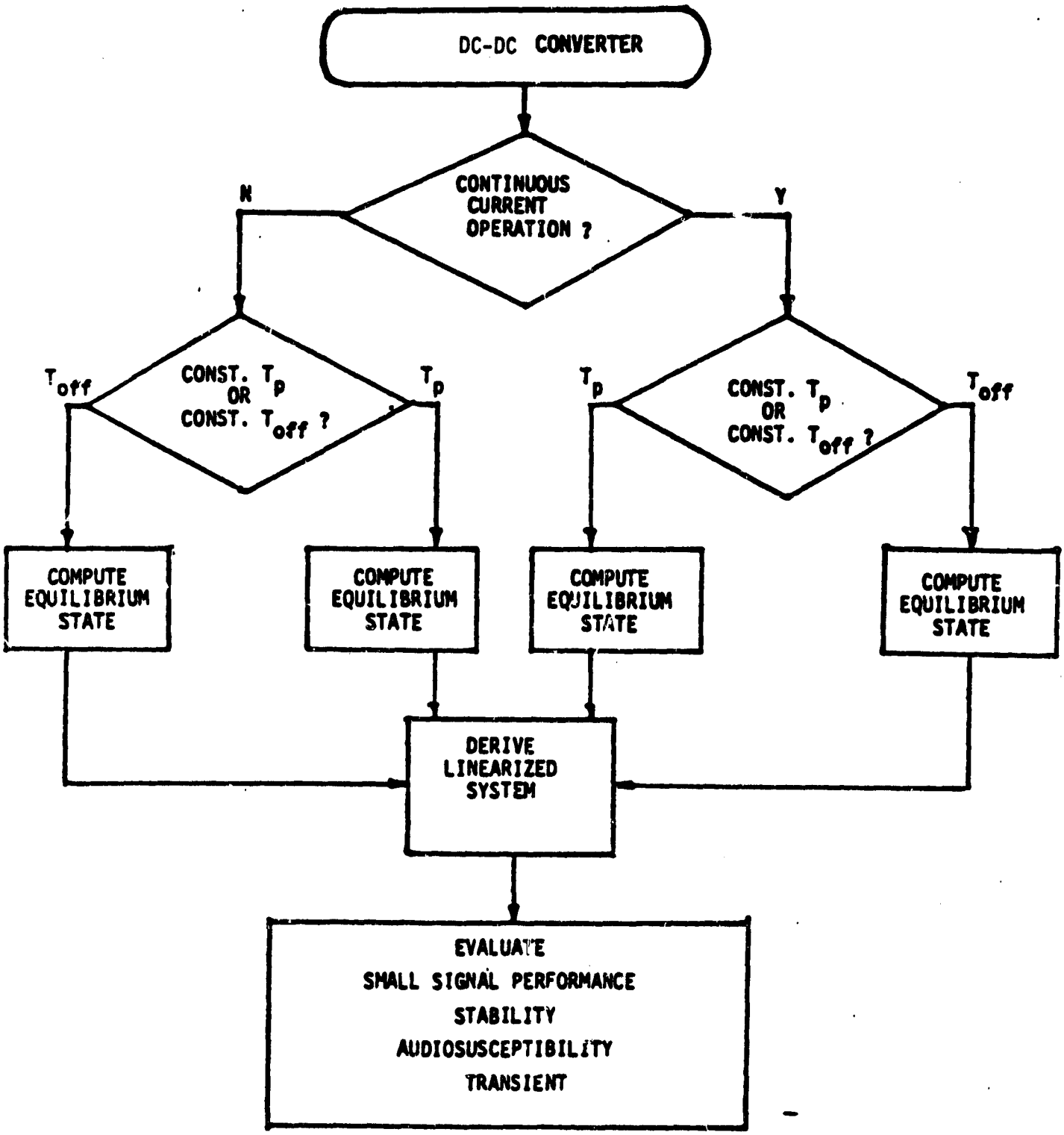


Figure 2-17 Information Flow Chart on a Composite Subprogram

2.5 Computer Performance Analysis Results.

The performance analysis computer programs provide the following results:

- Linearized stability analysis.
- Root locus analysis - up to 10 optional system parameters.
- Audio-susceptibility analysis.
- Transient response analysis - linearized system.
- Discontinuous or continuous inductor MMF mode of operation.
- Load change analysis - linearized system.
- Analysis of a non-linear transition response to a step input voltage.
- Constant frequency or constant off-time duty cycle control.

The computer programs contained in Appendix A through C (Volume II) have been verified experimentally for the buck, boost and buck-boost regulators, respectively.

A brief example of the computer results for a buck-boost converter is presented to illustrate the type of data available.

Figures 2-18 to 2-21 show the root locus results of a buck-boost DC-DC converter where circuit parameters are varied in order to establish the relative stability of the converter.

- Figure 2-18 C2 varied
- Figure 2-19 R5 varied
- Figure 2-20 R4 varied
- Figure 2-21 C0 varied

Figure 2-22 and 2-23 show the small signal open-loop gain and phase relationship. Figure 2-24 shows the output transient response when the input voltage is changed from 24 VDC to 40 VDC.

Figure 2-25 shows the output transient response when the output load resistance is changed from 49 ohms to 600 ohms.

FIGURE 2-18 **EIGENVALUES AS A FUNCTION OF THE COMPENSATION CAPACITOR C_2**

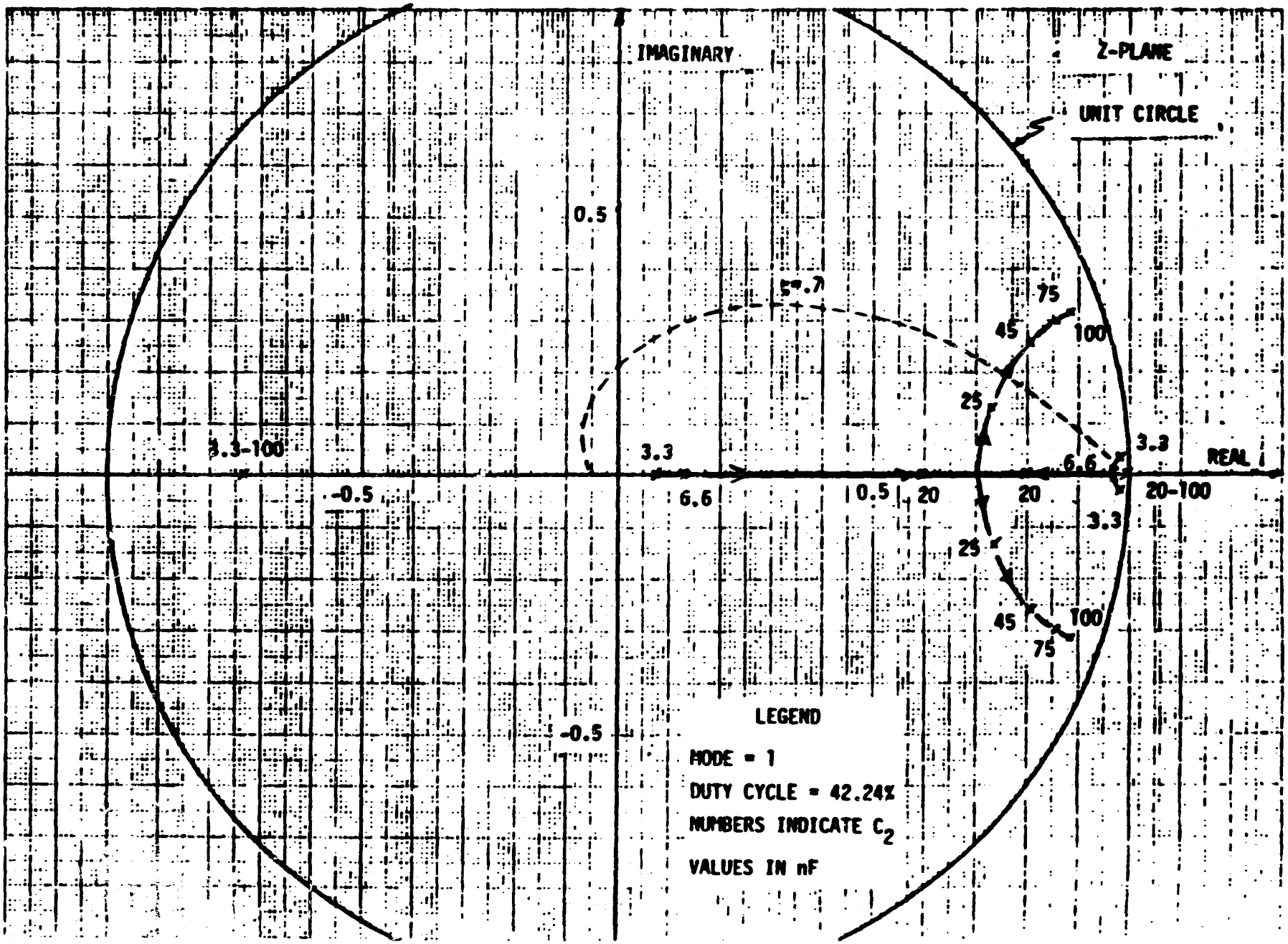


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FIGURE 2-19 EIGENVALUES AS A FUNCTION OF THE COMPENSATION LOOP RESISTOR R_5

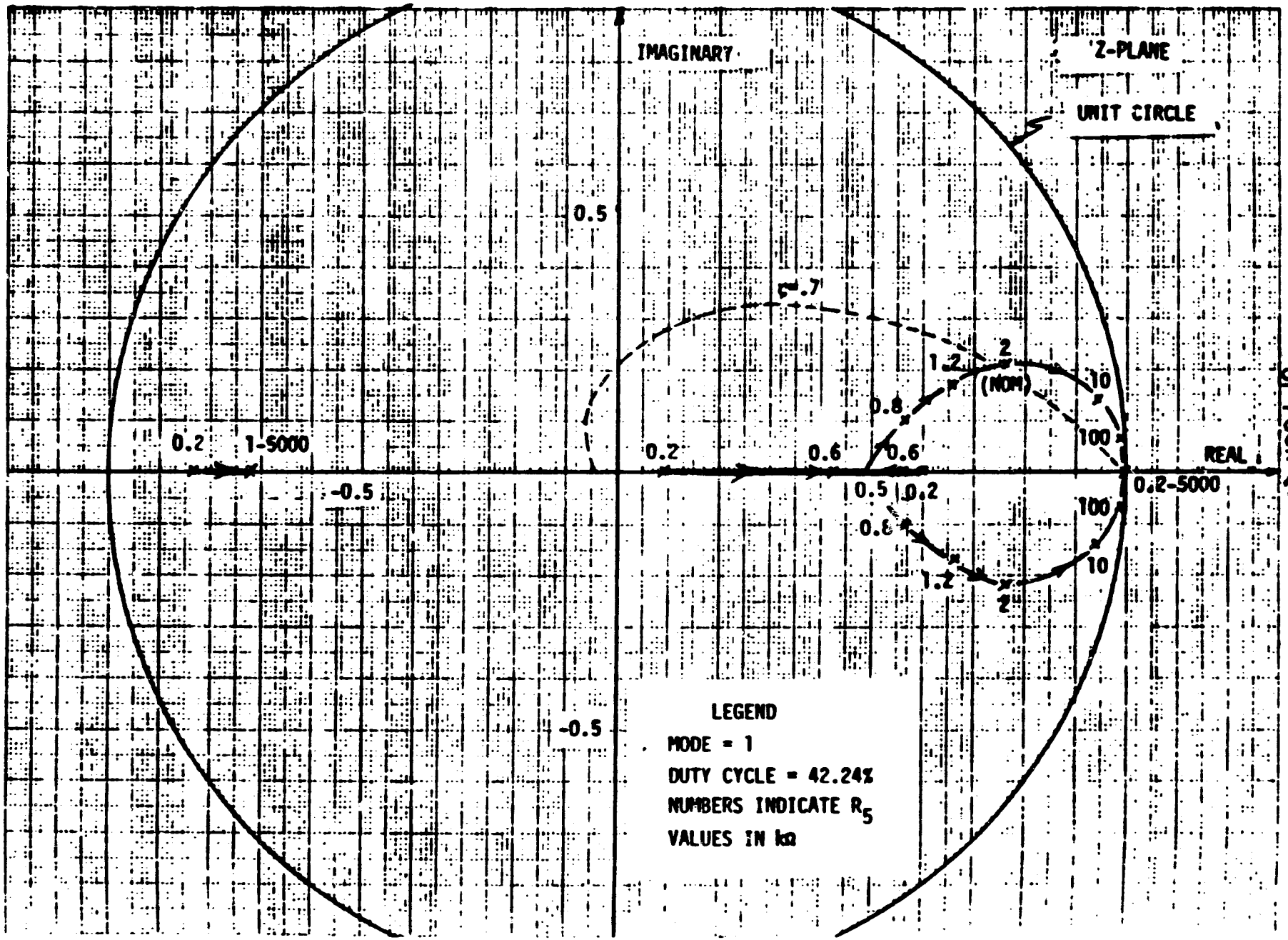

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FIGURE 2-20 EIGENVALUES AS A FUNCTION OF THE AC-LOOP RESISTOR R_4

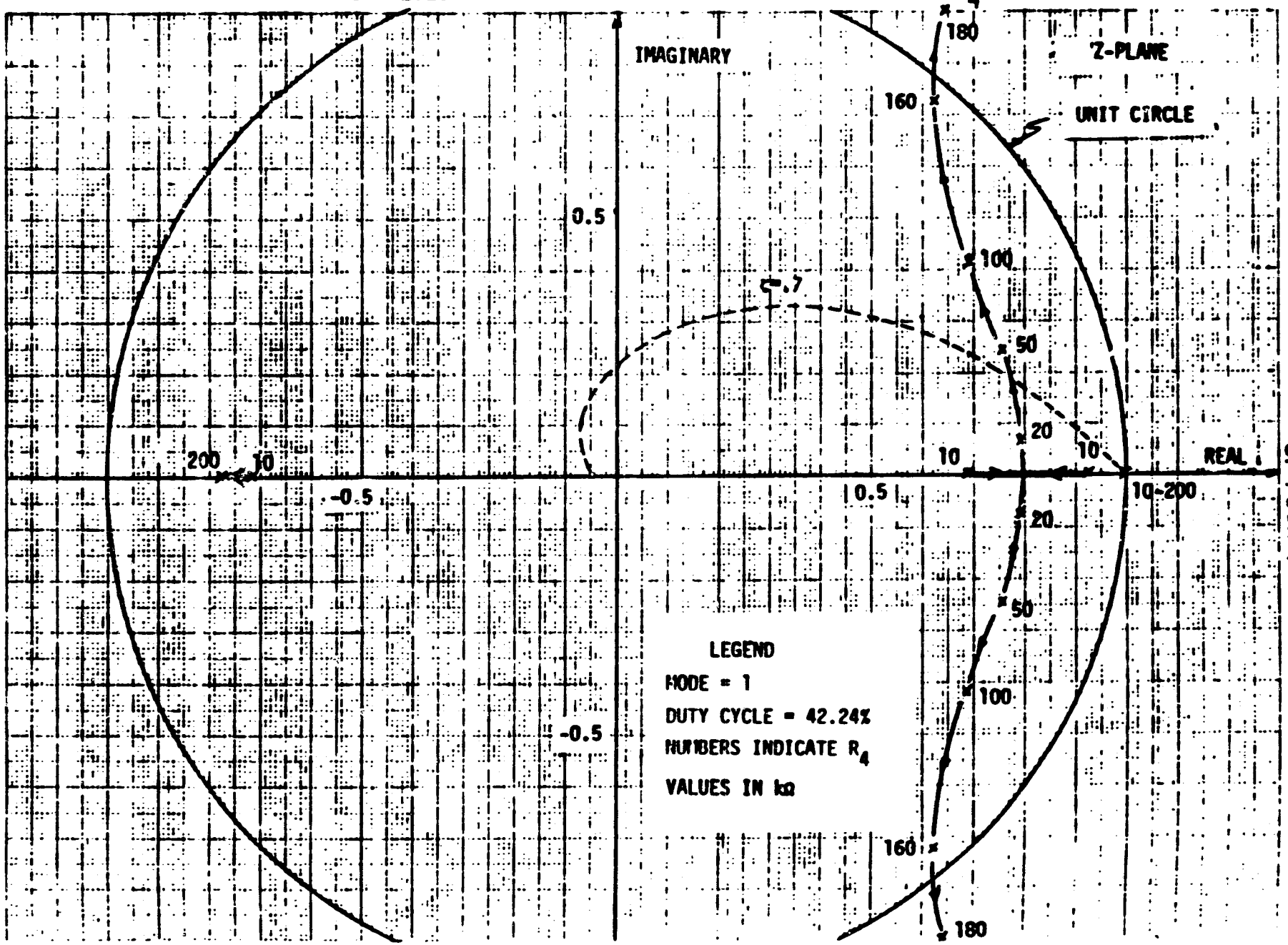

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FIGURE 2-21 EIGENVALUES AS A FUNCTION OF THE OUTPUT FILTER CAPACITOR C_0

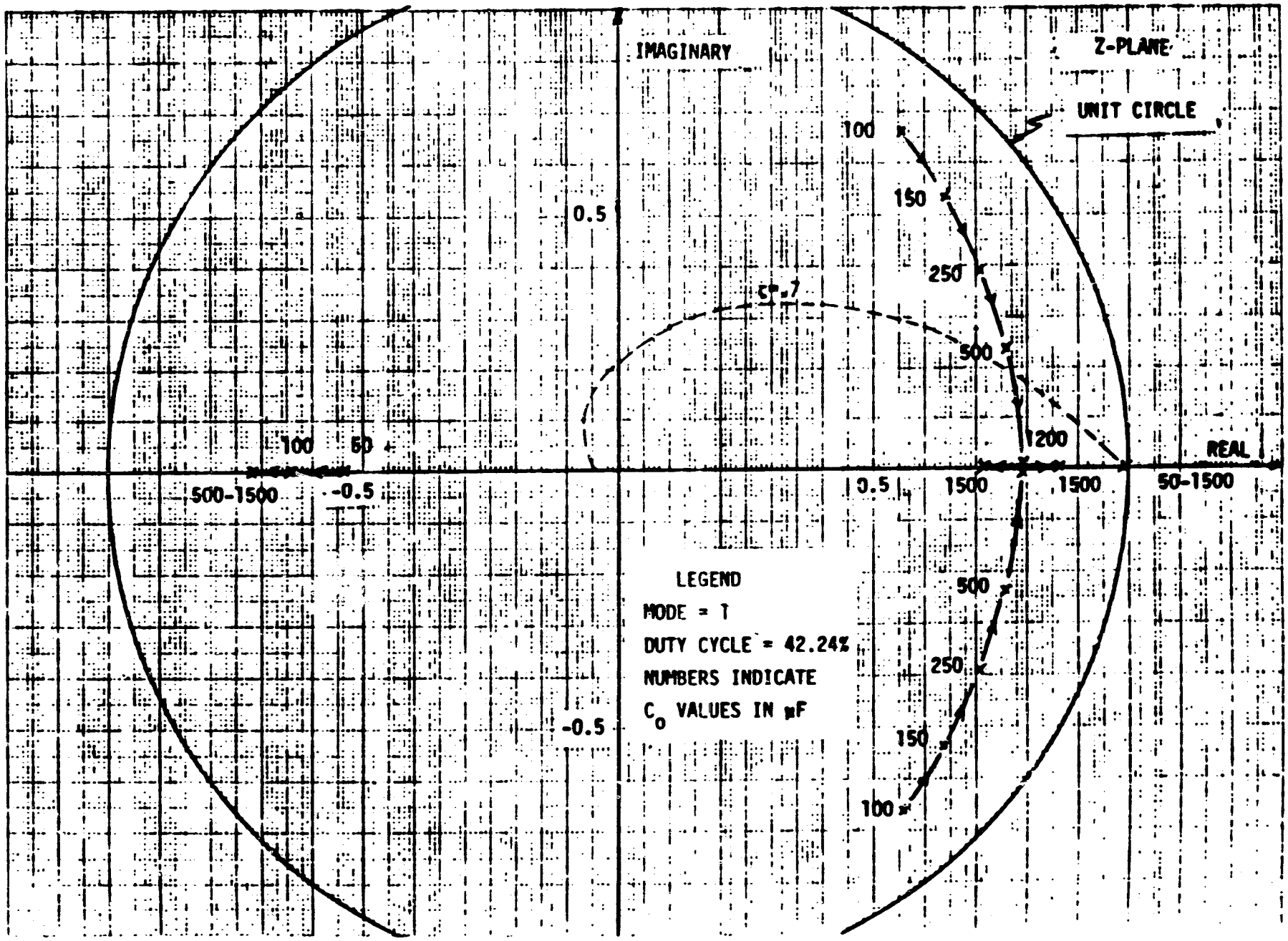

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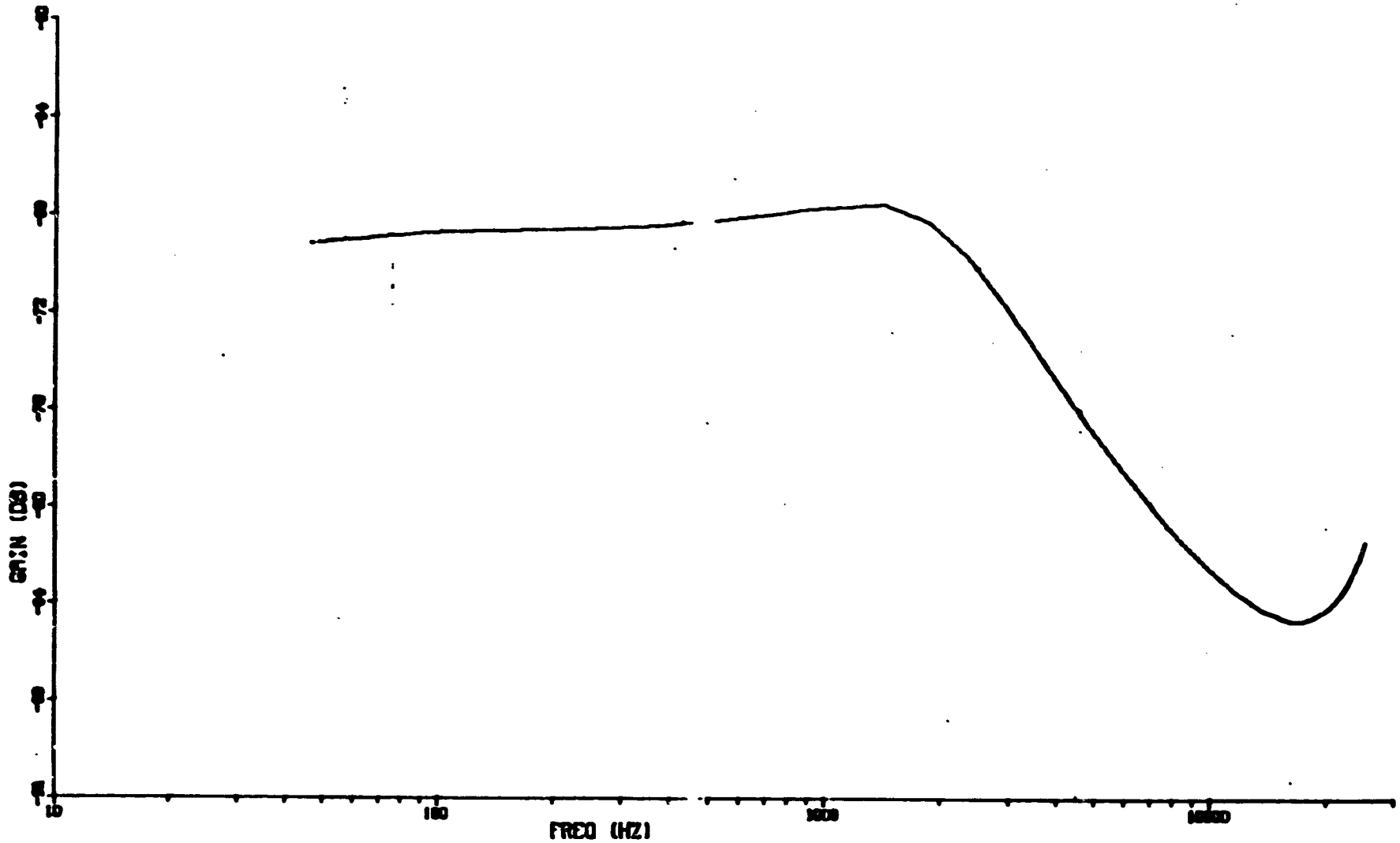
Figure 2-22 Constant T_p Frequency Response (Gain)



E1-40 RL-40 MODE-1

Figure 2-23 Constant T_p Frequency Response (Phase)

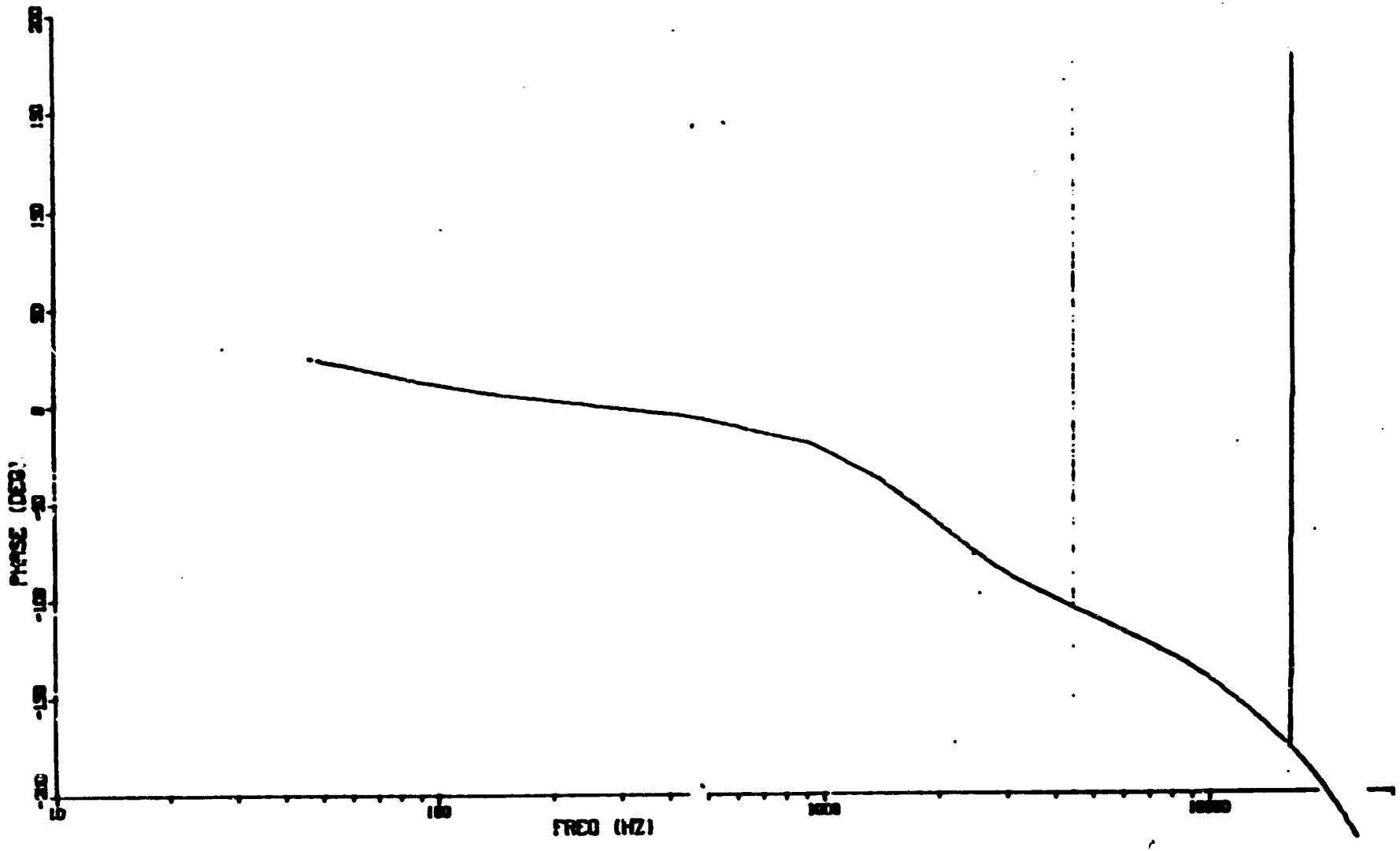
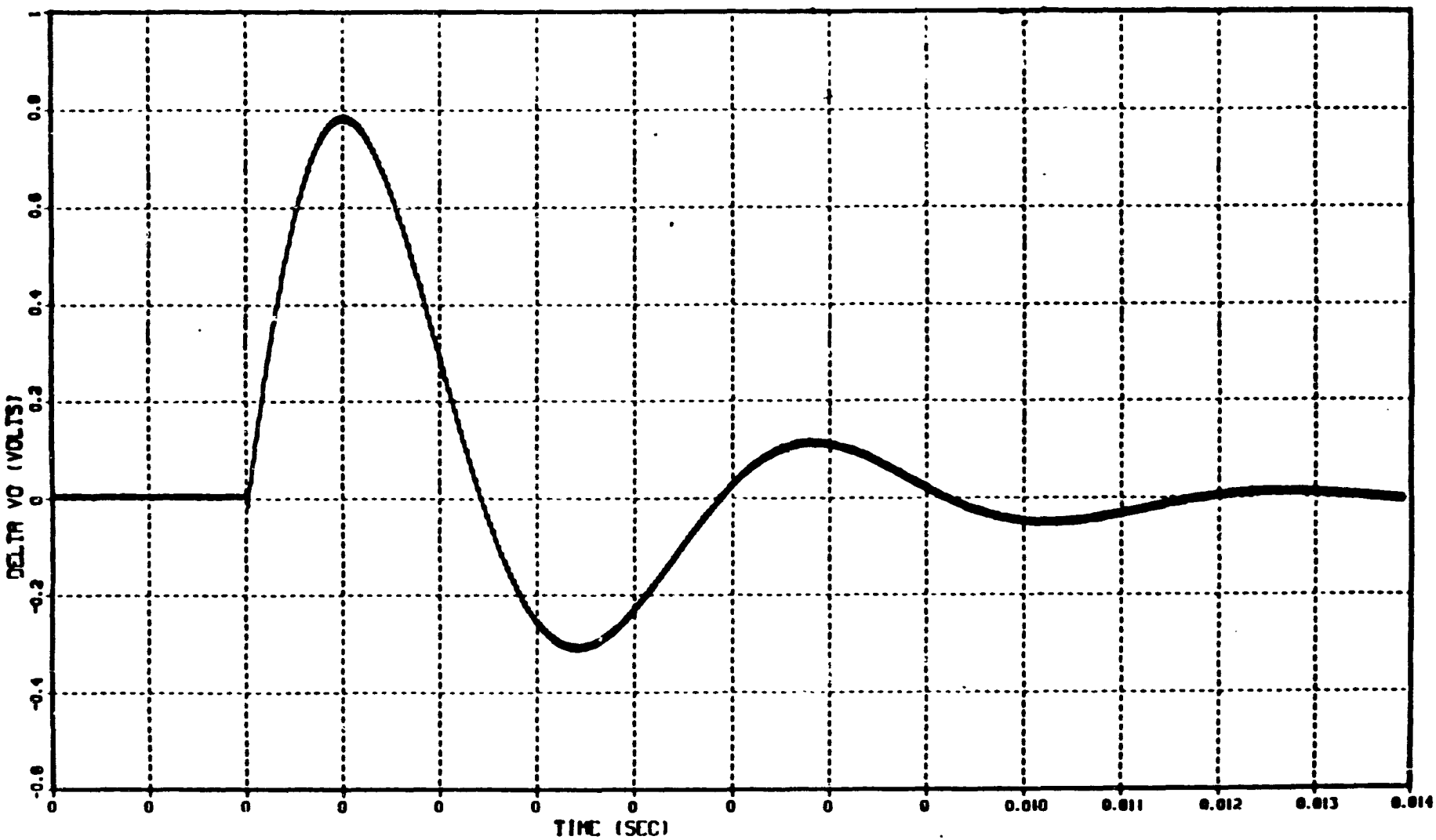
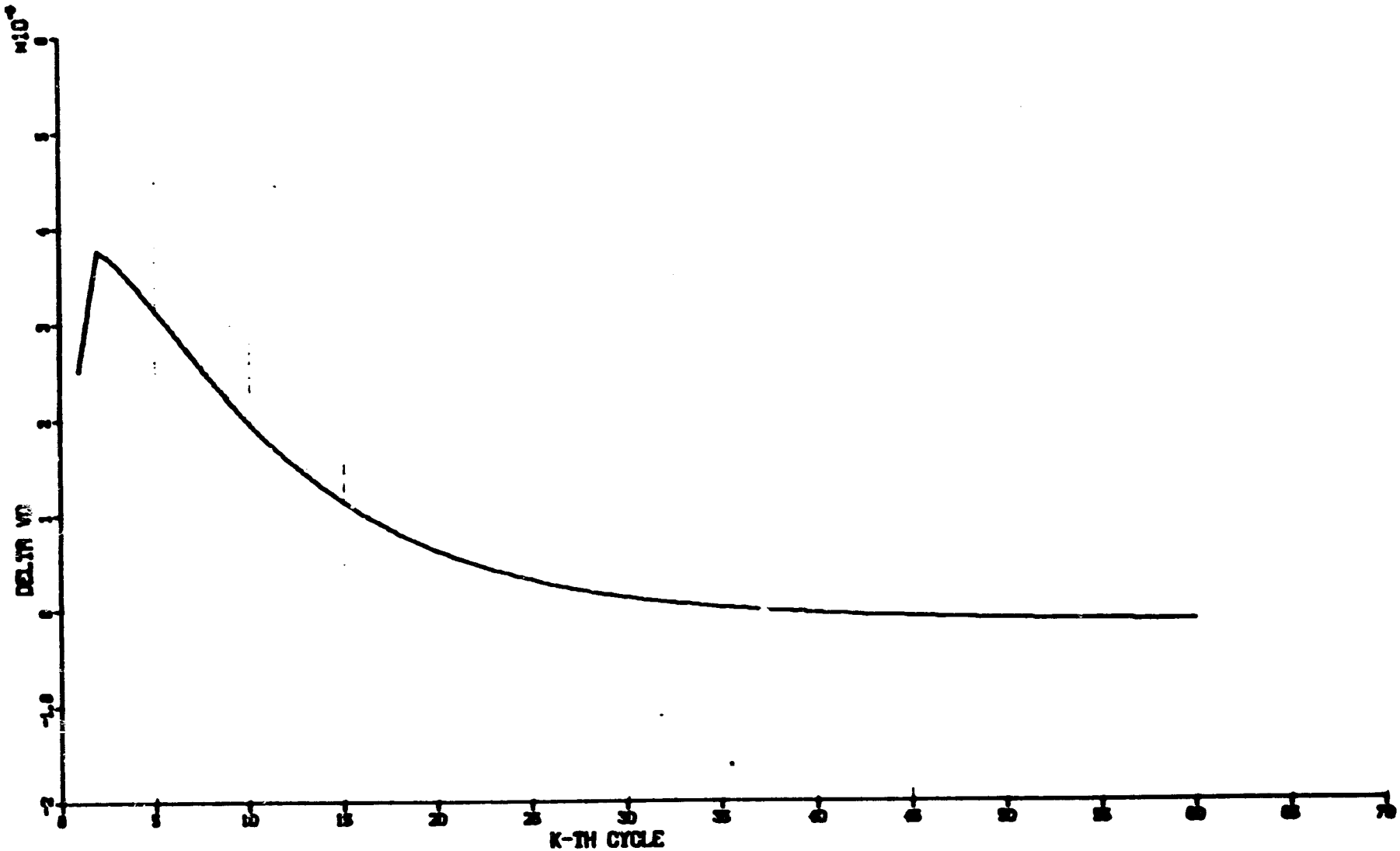


Figure 2-24 Constant T_p Transition Response



EI-24-40 RL-60 M-1-2

Figure 2-25 Step Load Change Transient Response



LCR EI-40 RL-40 RLSWIT-600

3.0 DESIGN OPTIMIZATION OF POWER CONVERTER

3.1 Introduction.

In converter design practice, it is often attempted to find the smallest possible magnetic core to accommodate the necessary windings in order to satisfy a given set of design requirements [8]. It is hoped, in return, that the weight and size of the overall converter would be reduced. One effective way to reduce the weight and size of the magnetic components (a way which many designers are pursuing nowadays) is to increase the switching frequency of the converter. To a certain extent, this approach is viable. Equations which govern the selections of design variables (such as magnetic components and capacitors), however, are nonlinear and interdependent due to the complex nature of various functions of power converter design. Employing the conventional design approach, only a piecemeal, suboptimum converter design at best can be achieved. For example, when the size of the energy storage inductor is reduced, the ac switching current component is invariably increased. Consequently, a penalty is imposed on the weight and size of the input filter design in order to attenuate the ac switching current component which reflects back into the source. Similarly, as the ac switching current component is increased, larger output filter capacitors should be used to limit the output ripple voltage component. To give further illustration of the complex interrelations: When the switching frequency is increased beyond a certain range, the gain of weight- and size-saving of magnetic components is diminished because the magnetic core losses and the semiconductor switching losses are increased as a function of switching frequency. Thus, higher losses and heavier overall system design can result due to the increase of weight and size of package and heatsink. The goal of a minimum weight converter

design is seldom achieved, despite the extensive and time-consuming trial and error design process.

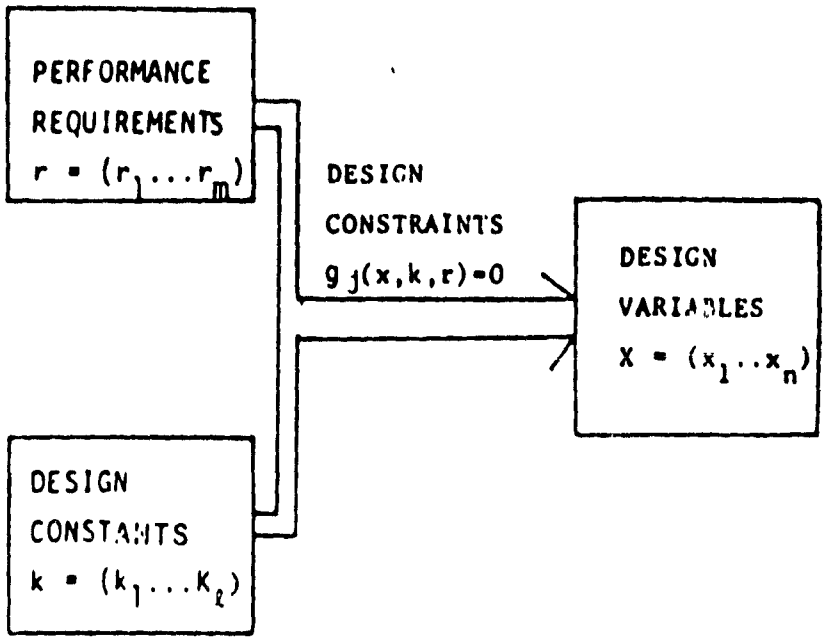
In power-converter design, the key to implementing a successful design optimization rests largely on the availability of suitable mathematical and computer programming technique Handicapped by a lack of suitable design and optimization tools, the tendency has been for a designer to rely on time-consuming intuitive and empirical methods resulting in a sub-optimum design. Such inadequacies invariably lead to penalties involving equipment weight, operating efficiency or other performances.

The philosophy of design optimization [8] of a power converter is briefly described in the following:

3.1.1 Design Optimization

A non-optimum design (illustrated in Fig. 3.1.1) generally involves four design ingredients First, a set of performance requirements such as output ripple factor and frequency-dependent source conducted EMI level, $r = (r_1, r_2, \ldots, r_m)$, is given to guide the design. Second, a set of design constants, such as transistor switching times and maximum magnetic operating flux density, $k = (k_1, k_2, \ldots, k_\ell)$, is employed. These constants are known to a designer either through manufacturers' data sheet, or designer's common sense and experience. Third, the objective of the design is to pinpoint numerically all the unknown design variables such as the detailed magnetic core size, mean magnetic path length and other component sizes, $x = (x_1, x_2, \ldots, x_n)$. These three design ingredients are then integrated together with the fourth ingredient, the nonlinear design constraints such as output ripple voltage constraint, EMI constraint, window area constraints and flux density constraints, $g_j(x,k,r) = 0$.

DESIGN APPROACH WITHOUT OPTIMIZATION



$n > j \Rightarrow$ INFINITE SET OF SOLUTIONS TO SATISFY

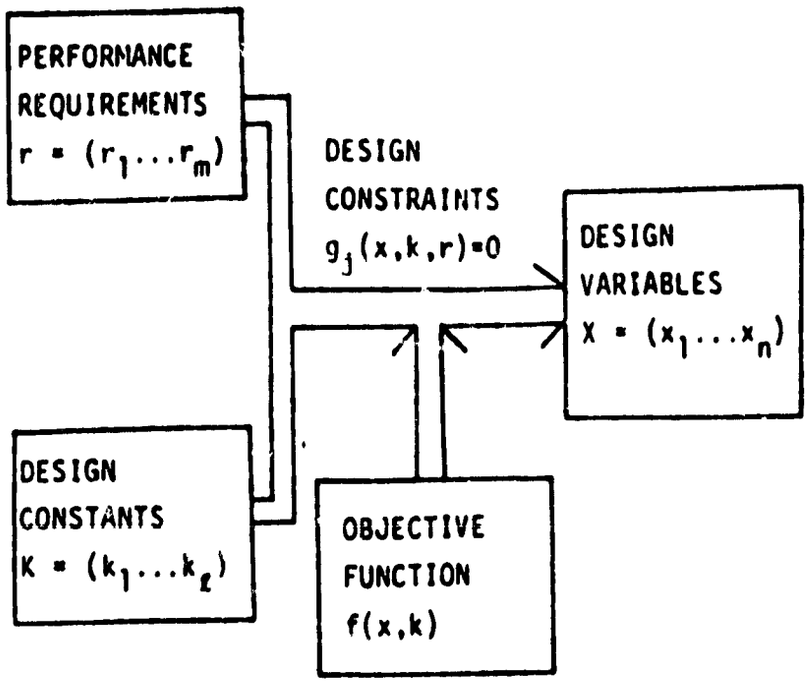
ALL CONSTRAINTS $g_j(x,k,r) = 0$

AND PERFORMANCE REQUIREMENTS

Fig. 3.1.1 Conventional design approach

Due to the design complexities of the switching power converter, the number of unknown design variables generally exceeds that of the constraints. Therefore there exists a virtually infinite set of solutions which satisfy both the constraints and performance requirements. Different designers may come out with completely different designs based on individual design experience and approaches. For example: Having selected a power circuit configuration, the designer picks a power-converter switching frequency through intuition or experience; then, using the performance requirements, he proceeds to obtain input filter design, output filter design, and energy storage inductor design. The same procedure may be repeated several times for different switching frequencies before a comparatively lower weight power-circuit design is achieved. Such a design is characterized by the designer's subjective judgement. Despite the time consuming iterations, optimization of the overall power converter is seldom achieved.

The optimum design approach takes advantage of powerful, computer-aided, nonlinear programming that integrates all the design ingredients in the objective function - that is, the function to be optimized - defined by the designer. The objective function can be the converter weight, efficiency, or any other realizable physical quantity. The philosophy of design optimization (shown in Fig. 3.1.2) is obtained through the injection of an objective function f(x,k) into the [illegible]onal design approach. The essence of the design optimization is then to realize a set of design variables using nonlinear programmin[illegible]ique. This set will satisfy all constraints $g_j = 0$ and requirements [illegible], and concurrently optimize a certain converter characteristics, f(x,k), defined by the designer. By introducing the objective function into the design process, the infinite set of design solutions presented in Fig. 3.1. [illegible]s reduced to a single solution set that is an optimum of the objective function.



BY INTRODUCING THE OBJECTIVE FUNCTION INTO THE DESIGN PROCESS, SINGLE SET OPTIMUM SOLUTION $(x_1, x_2, \ldots, x_n)$ CAN BE PINPOINTED TO SATISFY ALL CONSTRAINTS $g_j = 0$ AND CONCURRENTLY OPTIMIZE THE OBJECTIVE FUNCTION $f(x,k)$

Fig. 3.1.2 Optimum design approach

C-2

3.1.2 Power Converter Optimization

The purpose of this report is to demonstrate the usefulness of an Augmented Lagrangian Multiplier (ALAG) based nonlinear programming technique. This is used for a minimum weight design of the boost and buck-boost power converters. Previous experiences of the authors with the use of ALAG based programming techniques for power converter design optimizations [15] have encouraged such an approach. According to expectations, reliable results have also been obtained for boost and buck-boost converters.

At the beginning, mathematical models are presented for the boost and buck-boost converters. Various design requirements and physical operating characteristics of these converters are summarized in the form of equality and inequality constraints. The minimum weight design requirement is formulated as the objective function.

A. Problem Formulation

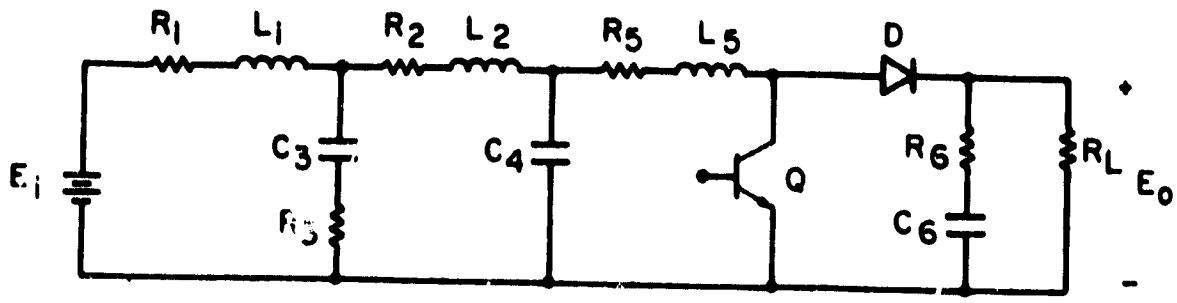
The circuit schematic, the objective function, and set of constraints are briefly discussed here for the boost and the buck-boost converters shown in Fig. 3.1.3.

A.1. Objective Function: The objective function is formulated as a sum of various component weights which include:

(i) Core weight.

(ii) Winding weight.

(iii) Capacitor weight.



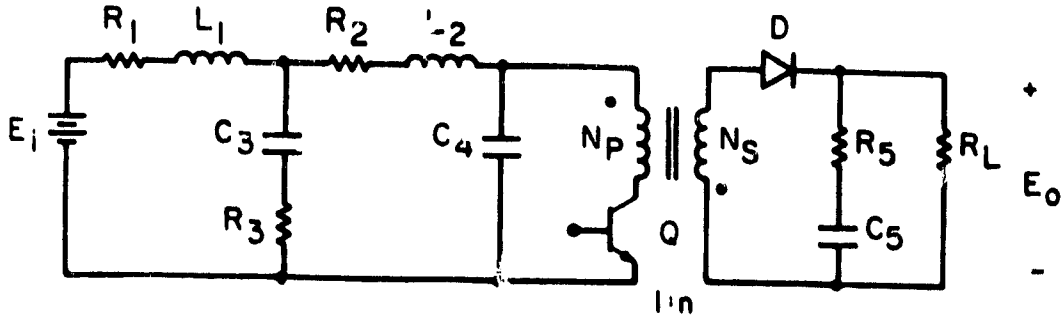


Fig. 3.1.3 Schematic of the (a) Boost Converter, (b) Buck/Boost Converter

(iv) Source weight.

(v) Package and heat sink weights.

A.2 Constraint are: A number of equality and inequality constraints form the constraint set:

(i) The loss constraint which is composed of input filter copper loss, conduction and switching losses of transistor and diode, two-winding-inductor copper and core loss, and output filter capacitor ESR loss.

(ii) Operating flux density constraint.

(iii) Window area constraint.

(iv) Parasitic resistance constraint.

(v) Input filter peaking constraint.

(vi) Frequency dependent source EMI constraint.

B. Solution Methodology

The stringent requirements for modeling the power converter design give rise to a set of very complicated nonlinear equations and an objective function. Obviously, such a model does not lend itself to a closed form solution; but one may use numerical techniques to arrive at an optimum solution. There are several nonlinear programming algorithms which provide convergence from a reasonable set of initial guesses. The selection of such an algorithm depends on the characteristics of the problem at hand, and the availability or non-availability of a feasible starting solution.

In the course of this research project two nonlinear programming algorithms were found to be appropriate for use in the minimum weight design optimization study. Both of these algorithms are based on transforming a constrained optimization problem into a sequence of unconstrained problems. The successive solutions of unconstrained

problems converge to a solution of the constrained problem. The Sequential Unconstrained Minimization Technique T) [10,11] and the Augmented Lagrangian Multiplier Technique (ALAG) [12, 13, 14] are two popular parametric transformation techniques that have been examined during this study. The ALAG algorithm has been found to be the faster and easier technique for the problem at hand [15]. The design optimization results that are presented in this report are obtained using the ALAG algorithm.

The following optimization approach is proposed for finding the converter minimum weight design:

(i) Fix the switching frequency.

(ii) Find all the circuit parameters which give the minimum system weight for the given frequency.

(iii) Change the system frequency over a certain desirable range and repeat the process.

C. Advantages of Computer Aided Design (CAD)

Using the Computer-Aided-Design (CAD) approach, designers no longer have to relay on subjective and brute-force trial and error methods. Computer-aided design not only provides the optimum solution but also offers the following advantages:

(1) The CAD approach is cost effective, since the switching frequency, circuit components and optimum magnetic designs, (down to the details of core size, mean magnetic path length, etc.) can be obtained in one computer run. This capability has a unique distinction over the conventional piecemeal suboptimum design. The CAD

approach integrates the interdependent nature of the various functions of the power converter.

(2) By treating the switching frequency as a parametric constant in the simulation process, the overwhelming computation time and convergence difficulties which otherwise result can be reduced to a minimum.

(3) Assessment of tradeoffs between converter weight and loss as function of switching frequency is immediately possible through the proposed approach.

3.2 BOOST CONVERTER OPTIMIZATION - OBJECTIVE FUNCTION AND CONSTRAINTS

In this chapter, the formulation of objective functions and design constraints for the boost power converter are presented:

(1) To use this practical example in order to illustrate the power converter design optimization using the nonlinear programming techniques; and (2) To demonstrate the minimum weight design of the switching power converter and its weight/loss tradeoffs. The circuit schematic with a two-stagic input filter is shown in Fig. 3.2.1. The energy storage inductor L_5 stores the energy when the transistor Q is on, then releases the energy to the load and recharges the output filter capacitor when transistor is off. The key operating waveforms of this circuit are shown in Fig. 3.2.2. In this figure:

I_i = input average DC current,

I_0 = output average load current,

2d = peak to peak ripple current in L_5.

The waveforms are employed to facilitate drivations of the objective function and the constraints.

3.2.1 Unknown Design Variables.

There are 22 design variables for this boost power converter including RLC component values, and details of magnetic design such as core cross-sectional area, mean magnetic path length, number of turns and winding area. The transitor switching frequency and converter overall operating efficiency are two other important variables.

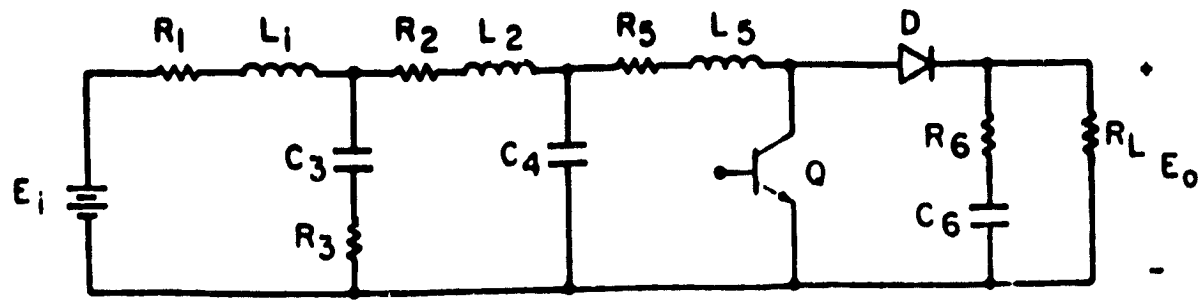


Fig. 3.2.1 Boost converter power circuit

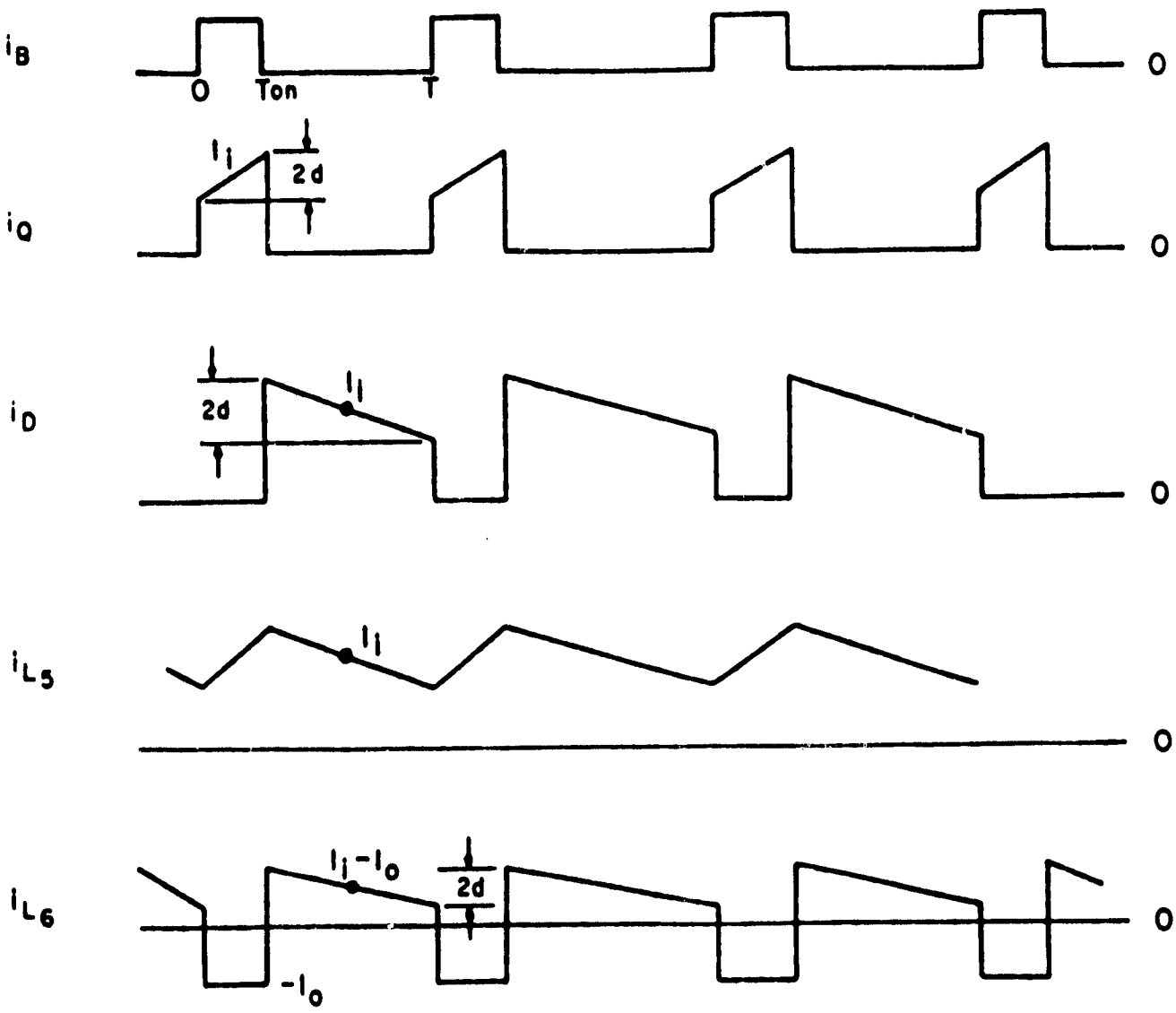


Fig. 3.2.2 Important waveforms for the Boost converter

R_1, R_2, R_5 : DC winding resistances of inductors L_1, L_2, L_5 respectively.

R_3 : Input filter damping resistor.

L_1, L_2 : Input filter inductors.

L_5 : Energy storage inductor.

C_3, C_4, C_6 : Filter capacitors.

A_1, A_2, A_5 : Core cross-section area of inductors L_1, L_2 and L_5, respectively.

Z_1, Z_2, Z_5 : Mean magnetic path length of inductors L_1, L_2 and L_5, respectively.

N_1, N_2, N_5 : Number of turns on inductors L_1, L_2 and L_5, respectively.

A_{C1}, A_{C2}, A_{C5}: Winding areas per turn for L_1, L_2 and L_5, respectively.

F : Transistor switching frequency.

eff : Overall operating efficiency.

3.2.2 Design constants.

Design constants are obtained either through manufacturer's specifications or designers' own experiences. Numerical values in MKS units are given in the parenthesis.

F_C : Winding pitch factor = $\frac{\text{mean length per turn}}{\text{core circumference}}$: (1.9).

F_W : Core window fill factor: (0.4).

ρ : conductor resistivity: (0.172×10^{-7}).

D_I : Core density: (7800).

D_C : Conductor density: (8900).

B_S : Maximum operating flux density: (0.4).

D_K : Weight per farad: (D_{K3}, D_{K4}, D_{K6}/210, 1100, 72).

V_{ST} : Transistor saturation voltage drop: (0.25V).

V_{BE} : Transistor emitter-to-base voltage drop: (0.8V).

T_{SR} : Transistor turn-on rise time: (0.15μs).

T_{SF} : Transistor turn-off fall time: (0.2 μs).

V_D : Diode conduction voltage drop: (0.9V).

T_{ND} : Diode turn-on rise time: (0.03 μs).

T_{FD} : Diode turn-off fall time: (0.05 μs).

T_{RE} : Diode turn-off recovery time: (0.03 μs).

K_H : Heat sink weight density: (15.4 w/kg).

K_S : Source weight density: (30.8 w/kg).

3.2.3 Power Converter Performance Requirements.

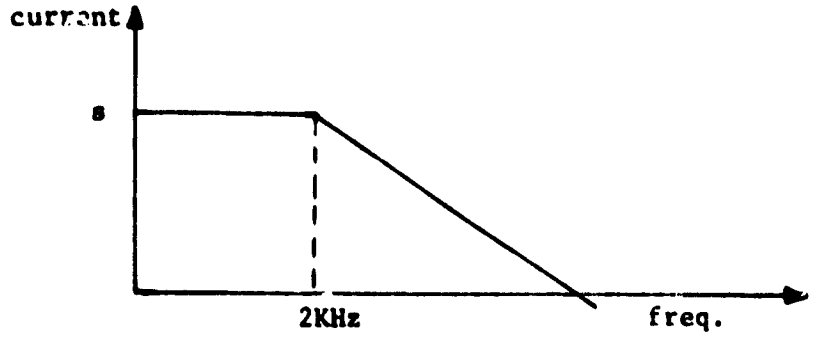
The performance requirements specified below will be employed in the next section to formulate design constraints.

E_i : Input voltage: (28V).

E_O : Output voltage: (37.5V).

P_O : Output power: (70W).

S : Frequency dependent source conducted interference: (0.1A). This specification limits the maximum percentage of the switching current being reflected back to the source ensuring that the source is not significantly disturbed by the switching action downstream. Referenced here is mil - sta 461, whose characteristic curve is shown as follows:



V_R : output ripple factor: (1%).

The output ripple factor is defined as output ripple factor: (?%) Δ.

$$\frac{\text{peak-to-peak output ripple voltage}}{\text{nominal dc output voltage}}.$$

PEI : Input-filter resonant peaking limit: (2).

The input filter peaking at its resonant frequency should be limited in order not to degrade the stability and the audiosusceptibility of the converter.

3.2.4 Objective Function.

The objective function is defined as the total weight of the converter, which is the sum of various component weights including:

(a) Core Weight: $WI = D_I(A_1Z_1 + A_2Z_2 + A_5Z_5)$

(where AZ = core volume)

(b) Winding Weight: $WTW = 4F_CD_C(A_{C1}N_1\sqrt{A_1} + A_{C2}N_2\sqrt{A_2} + A_{C5}N_5\sqrt{A_5})$

(where $4F_C\sqrt{A_1}$ = mean length per turn of the winding)

(c) Capacitor Weight: $WC = D_{K3}C_3 + D_{K4}C_4 + D_{K6}C_6$

(d) Source Weight: $WS = \frac{P_O}{effK_s}$

(where $\frac{P_O}{eff}$ = input power)

(e) Heat Sink Weight: $WH = \frac{P_O(1 - eff)}{eff\ K_H}$

(where $\frac{P_O}{eff} - P_O$ = total loss)

<u>Objective Function</u>: $F = WI + WTW + WC + WS + WH$ (3.2.1)

3.2.5 Design Constraints.

In this study, the design effort is carried out using appropriate models which portray the physical characteristics of the boost power

converter. Some of the more significant characteristics are: power loss, core window area, core flux density, and magnetic winding resistance. Inclusion of these characteristics results in a very complicated set of nonlinear constraints. Mathematical restrictionsfor these contraints can be found in Appendix D.

(a) <u>Loss Constraint</u>: $C(1) = 0$

$$C(1) = P_O\left(\frac{1}{eff} - 1\right) - PIF - PQ - PD - POF - PCAP \qquad (3.2.2)$$

where PIF = input filter copper loss

$$= \left(\frac{P_O}{eff\ E_i}\right)^2 (R_1 + R_2),$$

PQ = Transistor saturation loss + Base drive loss

+ transistor turn on switching loss

+ transistor turn off switching loss

$$= \frac{P_O V_{ST}(E_O - E_i)}{eff\ E_i E_O} + 0.1\ \frac{P_O V_{BE}(E_O - E_i)}{eff\ E_i E_O}$$

$$+ \frac{T_{SR}F}{6}\ (E_O + V_D + 2V_{ST})\left(\frac{P_O}{eff\ E_i} - \frac{E_i(E_O - E_i)}{2L_5 E_O F}\right)$$

$$+ \frac{T_{SF}F}{6}\ (E_O + V_D + 2V_{ST})\left(\frac{P_O}{eff\ E_i} + \frac{E_i(E_O - E_i)}{2L_5 E_O F}\right), \qquad (3.2.3)$$

P_D = Diode conduction loss

+ Turn on loss

+ Turn off and recovery loss

$$= \frac{P_O V_D}{\text{eff } E_O} + \frac{E_O T_{ND} F}{12}\left[\frac{P_O}{\text{eff } E_I} + \frac{E_i(E_O - E_i)}{2L_5 E_O F}\right]$$

$$+ \frac{E_O(T_{FD} + 3T_{RE})F}{12}\left[\frac{P_O}{\text{eff } E_i} - \frac{E_i(E_O - E_i)}{2L_5 E_O F}\right] , \qquad (3.2.4)$$

POF = Output filter copper and core loss =

$$\left[\left(\frac{P_O}{\text{eff } E_i}\right)^2 + \frac{1}{12}\frac{E_i^2(E_O - E_i)^2}{L_5^2 E_O^2 F^2}\right] R_5$$

$$+ \frac{80\ E_i(E_O - E_i)Z_5 \times 0.0022\sqrt{F}}{E_O N_5} , \qquad (3.2.5)$$

PCAP = Output filter capacitor ESR loss =

$$\left(1 - \frac{E_i}{E_O}\right)\left(\frac{P_O}{E_O}\right)^2 R_6 + \frac{E_i}{E_O}\left[\frac{E_i^2\ (E_O - E_i)^2}{12\ L_5^2 E_O^2 F^2}\right.$$

$$\left. + \left(\frac{P_O}{\text{eff } E_i} - \frac{P_O}{E_O}\right)^2\right] R_6 . \qquad (3.2.6)$$

(b) <u>Operating flux density constraint: C(5) = C(6) = C(9) = 0</u>

This constraint ensures that the magnetic core will not exceed its intended maximum operating flux density. Notice that L_5 handles both DC and ripple components.

$$C(5) = N_1 A_1 - \frac{L_i P_O}{\text{eff} E_i B_{s1}} \qquad (3.2.7)$$

$$C(6) = N_2A_2 - \frac{L_2P_0}{effE_1B_{s2}} \tag{3.2.8}$$

$$C(9) = N_5A_5 - \frac{L_5}{B_{s5}}\left[\frac{P_0}{effE_1} + \frac{E_1(E_0 - E_1)}{2L_5E_0F}\right] \tag{3.2.9}$$

(c) <u>Window area constraint: $C(7) = C(8) = C(10) = 0$</u>

All the inductor windings must be accommodated within the physical confinement of the available core window area. All cores employ a toroidal configuration with square cross section area.

$$C(7) = \left(\frac{N_1A_{C1}}{\pi F_W}\right)^{0.5} - \frac{Z_1}{2\pi} + \frac{A_1}{2}^{0.5} = 0 \tag{3.2.10}$$

$$C(8) = \left(\frac{N_2A_{C2}}{\pi F_W}\right)^{0.5} - \frac{Z_2}{2\pi} + \frac{A_2}{2}^{0.5} = 0 \tag{3.2.11}$$

$$C(10) = \left(\frac{N_5A_{C5}}{\pi F_W}\right)^{0.5} - \frac{Z_5}{2\pi} + \frac{A_5}{2}^{0.5} = 0 \tag{3.2.12}$$

(d) <u>Parasitic resistance for L_1, L_2, L_5: $C(2) = C(3) = C(12) = 0$</u>

$$C(2) = R_1A_{C1} - 4\rho F_C\sqrt{A_1}\,N_1 \tag{3.2.13}$$

$$C(3) = R_2A_{C2} - 4\rho F_C\sqrt{A_2}\,N_2 \tag{3.2.14}$$

$$C(12) = R_5A_{C5} - 4\rho F_C\sqrt{A_5}\,N_5 \tag{3.2.15}$$

(e) <u>Input filter peaking constraint: C(4) = 0</u>

This constraint is important in determining the audio-susceptibility performance and the control loop stability.[16]

$$C(4) = (PEI)^2 - \frac{1 + \left(\frac{R_3^2 C_3}{L_1}\right)}{\left(\frac{C_4}{C_3}\right)^2 + \left(R_3^2 \frac{C_3}{L_1}\right)\left[1 - \frac{C_4}{C_3} - \frac{L_2 C_4}{L_1 C_3}\right]^2} \qquad (3.2.16)$$

(f) <u>Output ripple constraint: C(11) = 0</u>

Output ripple factor (in percentage) is expressed as

$$V_R = \left[\frac{P_0}{effE_1E_0} + \frac{E_1(E_0 - E_1)}{2L_5E_0^2F}\right] R_6 + \frac{P_0(E_0 - E_1)}{2E_0^3C_6F} \qquad (3.2.17)$$

$$C(11) = V_R - \left[\frac{P_0}{eff\ E_1\ E_0} + \frac{E_1(E_0 - E_1)}{2L_5E_0^2F}\right] R_6 \qquad (3.2.18)$$

$$- \frac{P_0(E_0 - E_1)}{2E_0^3C_6F}.$$

(g) <u>Frequency dependent source EMI constraint: C(13) ≥ 0</u>

This constraint limits the maximum percentage of the switching current being reflected back to the source.

The input filter must be designed to satisfy the following requirement:

Required attenuation at switching frequency

$$= \frac{\text{EMI requirement}}{\text{Fundamental component of the switching current}}$$

$$C(13) = \frac{S}{|A|\sqrt{1 + (\frac{F}{2000})^2}} - \left\{\left(\frac{L_2C_4}{L_1C_3}\right)(2\pi F\sqrt{L_1C_3})^3 \frac{1}{D} - \frac{C_4}{C_3}(2\pi F\sqrt{L_1C_3})^2\right\}^{-1} \tag{3.2.19}$$

where

$$A = \frac{-E_0}{\pi^2 L_5 F}\left(\sin \frac{\pi(E_0 - E_1)}{E_1}\right)^2$$

$$D = R_3 \left(\frac{C_3}{L_1}\right)^{0.5}$$

(h) <u>Additional inequality constraints: C(14), C(15), C(16), C(17) $\geq$ 0</u>

These constraints are needed to confine some of the variables in reasonable ranges in order to facilitate program convergence.

$$C(14) = 0.97 - \text{eff} \geq 0 \tag{3.2.20}$$

$$C(15) = R_T - R_1 - R_2 \geq 0 \tag{3.2.21}$$

$$C(16) = C_4 - 1.0 \times 10^{-6} \geq 0 \tag{3.2.22}$$

$$C(17) = C_3 - 1.0 \times 10^{-6} \geq 0 \tag{3.2.23}$$

3.3 INTRODUCTION TO NONLINEAR PROGRAMMING AND AUGMENTED LAGRANGIAN (ALAG) PENALTY FUNCTION METHOD

Most optimization problems arising from practical power converter applications are sufficiently complicated to defy closed-form solutions. To numerically realize an optimum design, one has to resort to nonlinear programming algorithms which can provide fast convergence to an optimum solution from a reasonable guess of the starting point. The nonlinear programming problem (NLP) of extremizing (maximizing or minimizing) a function of n variables, while requiring other functions of the same variables to satisfy either equality or inequality constraint relationships, is called constrained NLP. The problem is to maximizing or minimizing a function of n variables without regard to side conditions or constraints is called an unconstrained NLP. While there exist numerous methods of nonlinear programming, the effectiveness of each method depends greatly on the particular multidimensional problem to which the method is applied. The availabilty of numerous efficient numerical methods for solving the unconstrained optimization problem has motivated the design of algorithms that transform a constrained problem into a sequence of unconstrained problems such that the successive solutions of the unconstrained problems converge to a solution of the constrained problem. These transformation methods implicitly incorporate all the constraints into the objective function that is to be optimized. The algorithms based on the transformation approach are conceptually simpler and easier to implement than the algorithms that handle the constraints directly because of the relative ease of extremizing an unconstrained problem compared to a constrained one.

3.3.1 Nonlinear Programming Penalty Function Method.

The Penalty Function Technique employs the aforementioned transformation method [11]. Let us define problem P1 as the original constrained NLP problem and P2 as the transformed unconstrained NLP problem.

P1: Minimize objective function $f(x)$ subject to: (3.3.1)

1.) Inequaltiy constraints $g_i(x) \geq 0$, $i = 1,2,\ldots, P$.

2.) Equality constraints $h_j(x) = 0$, $j = 1,2,\ldots, q$.

P2: Minimize $A(x, w^m, g, h)$, $m = 1, 2, \ldots$ (3.3.2)

Where x = vector of n unknown variables.

$A(x,w^m)$ = new objective function formed by augmenting the original objective function $f(x)$ with weighted terms (penalty terms) that depend on the constraints g and h.

w^m = controlling weighting factor, on penalty term, a vector of Lagrange Multipliers.

m = number of iterations.

The essence of transforming the constrained NPL into an unconstrained NLP is that by gradually removing the effect of the constraints in the new objective function (by controlling the weighting factor w^m) it is possible to generate a sequence of unconstrained problems that have solutions converging to the solution of the original constrained problem.

That is: $$\lim_{m \to \infty} A(x, w^m g, h) - f(x^*) = 0, \qquad (3.3.3)$$

After initerations, the variable x approaches the optimum x^*. In effect, the influence of the constraints on the augmented objective function is relaxed and, in the limit, removed, and the augmented objective function $A(x, w^m, g, h)$ converges to the same optimum value $f(x^*)$ of the original objective function.

3.3.2 Sequentially Unconstrained Minimization Technique (SUMT).

SUMT was developed, validated, extended and refined by Fiacco and McCormick [10,11]. This method replaces the constrained problem P1 defined below by a sequence of unconstrained minimization problems as defined in P2.

P1: Minimize $f(x, y)$ subject to: (3.3.4)

1.) $g_i(x, y, z) \geq 0, \; i = 1, 2, \ldots, P$

2.) $h_j(x, y, z) = 0, \; j = 1, 2, \ldots, q$

P2: Minimize $P(x, r_k) = f - r_k \sum_{i=1}^{P} \ln g_i + \frac{1}{r_k} \sum_{j=1}^{q} h_j^2$ (3.3.5)

where $P(x, r_k)$ is the penalized objective function, r_k is a monotonically decreasing sequence tending to zero, and x is an n-dimensional vector representing the design variables to be optimally selected. In the power converter design optimization, the components of x are values of R, L, C, and the design details for magnetics such as core cross-section area, mean magnetic path length, wire size, number of turns on magnetic winding, etc. y represents the vector of constants related to component characteristics such as winding and core densities, transistor and diode switching times, the intended maximum operating flux density of given magnetics, etc. z represents the vector of performance requirements to be met by optimum design such as the maximum output ripple, EMI requirement, output power, input filter peaking limit, etc. $f(x,y)$ represents the objective function (such as the total converter weight) to be minimized.

The basic idea of SUMT is to solve a sequence of unconstrained problems like P2 whose solution approaches the solution of P1. Considerable computational difficulties have been experienced with the SUMT algorithm. The most serious handicaps are summarized below. The contours of $P(x,r_k)$

correspond to increasingly steep sided valleys as the controlling parameter decreases, and the Hessian of the function becomes progressively more ill-conditioned as $r_k \to 0$ and the optimum solution x^* is approached. As a result, the search directions may become misleading. The rate of convergence depends on the initial value of r_0 and the method of reducing r_k. Finally, most of the information about the topology of $f(x,y)$ and $P(x,r_k)$ is discarded from one stage to the next even if some type of extrapolation is incorporated in the algorithm. The attempts to overcome these computational difficulties have resulted in several modifications of SUMT. The ALAG penalty function technique resulted from such efforts to improve the computational method. It has gained recognition as one of the most effective methods for solving constrained optimization problems. The algorithm based on this method converges at a superlinear rate; the computational effort per iteration falls off rapidly; the initial starting point need not be feasible; and the transformation function is defined for all values of the parameters.

3.3.3 ALAG Penalty Function Technique.

The Augmented Lagrangian Penalty Function for P1 is obtained by combining the Powell-Hestenes [12,13] penalty function and the Rockefellar penalty function [14] as in P3 in the equation below.

P3: Minimize $\psi(x,\lambda,\sigma)$

$$\text{where } \psi(x,\lambda,\sigma) = f(x,y) - \sum_{j=1}^{q} [\lambda_j h_j - \frac{1}{2}\sigma_j h_j^2] + \frac{1}{2}\sum_{i=1}^{P}\left[\sigma_i\left(g_i - \frac{\lambda_i}{\sigma_i}\right)_-^2 - \frac{\lambda_i^2}{\sigma_i}\right] \tag{3.3.6}$$

$$\text{where } \left(g_i - \frac{\lambda_i}{\sigma_i}\right)_- = \min[(g_i - \frac{\lambda_i}{\sigma_i}), 0], \quad \sigma_i = \lambda_i\theta_i, \quad \forall i$$

$$\lambda_i \varepsilon E^{P+q}, \ \theta_i \varepsilon E^{P+q}, \ \sigma_i \varepsilon E_+^{P+q} \quad \forall i$$

The θ_i's and σ_i's are controlling parameters, whereas the SUMT algorithm has only one controlling parameter r_k. The parameter σ_i is changed only when the rate of convergence is not satisfactory and θ_i is changed in every iteration to enforce constraint satisfaction. The important feature of this approach is that $1/\sigma_i$, which corresponds to the controlling parameter r_k in SUMT, is not required to tend to zero for convergence of the algorithm. In the penalty function ψ defined above, the term λ_i/σ_i represents a penalizing threshold for the ith inequality constraint. Increasing σ_i to enforce faster convergence reduces the penalty threshold level and leads to closer constraint satisfaction. When the inequality constraint $g_i > 0$, then λ_i (or θ_i) is relaxed to zero; otherwise, it is changed to make the corresponding constraint active at the current solution x.

3.3.4 Comparison Between SUMT and ALAG

The SUMT package was utilized in the initial phase of this design optimization. Considerable effort was spent in computer coding and implementation of the SUMT package. Although optimum solutions were reached, the results were less satisfactory and were sensitive to initial guesses. Therefore another software package, ALAG, requiring only slight modification of the original SUMT Code, was adopted to explore an alternative means of design optimization. The trials on the ALAG algorithm were quite successful. The two algorithms are compared briefly below [15].

(1) Since SUMT requires first and second order derivatives for the constraints and the objective function, many hours of data praparation are needed. The ALAG algorithm needs only the first derivatives.

(2) The initial starting point in SUMT should be strictly feasible with respect to the inequality constraints in order to get proper convergence. The ALAG algorithm does not require the starting point to be feasible.

(3) SUMT requires about ten times more computer storage and CPU time than the ALAG algorithm.

(4) ALAG converges much more readily than SUMT.

(5) Computational comparisons between SUMT and ALAG were obtained using Buck converter as an example [15]. The comparisons are shown in Table 3.3-I.

Table 3.3-I COMPARISONS BETWEEN SUMT AND ALAG USING BUCK CONVERTER DESIGN OPTIMIZATION PROGRAM

	SUMT	ALAG
COMPILING TIME (SECOND)	4.61 (USER PROGRAM ONLY)	6.54 ENTIRE PROGRAM
EXECUTION TIME	197	6.34
TOTAL TIME	201 + ?	13
INPUT CARDS	2719	1299
KILOBYTE SECONDS	165216	10652
TOTAL RUN CHARGES	$16.65	$4.29

Since the ALAG was found generally superior to SUMT in several aspects, it was adopted to implement the computer-aided design optimization for the remainder of the study.

3.4 IMPLEMENTATION OF COMPUTER CODE AND USER'S GUIDE

The nonlinear programming package ALAG is designed with the user convenience in mind. There is one main program and nine subroutines in the whole package. A list of computer programs is given in the Appendix F. The nine subroutines are:

ALAGA
ALAGZ
QNTA
MUDA
MUDB
MUDE
BQMA
BQMB
ALAGB → User's supplied subroutine

All subroutines except ALAGB are supplied in the ALAG package. The user also needs to supply the main program including the objective function, constraints and their derivatives. The flow-chart of general optimization sequence using a multiplier algorithm is shown in Figure 3.4.1.

3.4.1 User Supplied Main Program and Parameters

The main program basically supplies the controlling parameters, the input data (such as design constants, performance requirement, initial starting point), variable and constraint scaling factors, and the output information with print-out format. Detailed descriptions of the main program and the subroutine ALAGB are given in this chapter and Appendix E. Both of these programs may serve as a limited user's application guideline.

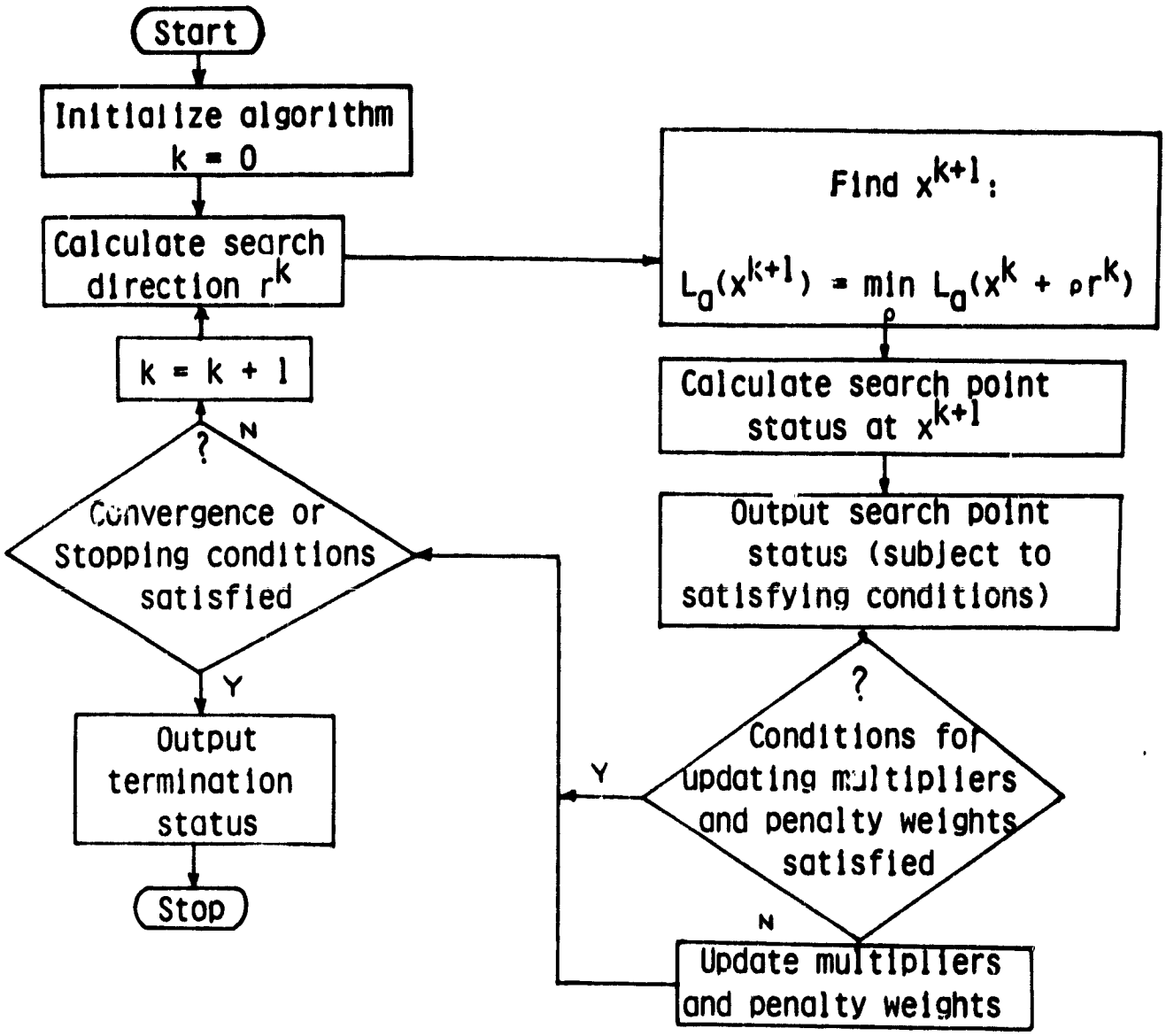


Figure 3.4.1 General Minimization Sequence Using a Multiplier Algorithm

The user supplied controlling parameters are explained in the following:

<u>Controlling Parameters</u>

N	:	An integer set to the number of variables, $N \geq 2$.
M	:	An interger set to the total number of constraints, $M \geq 1$.
K	:	An integer set to the total number of equality constraints.
EPS	:	A real array of N elements used in variable convergence criterion. EPS(I) should be set such that EPS(I)/X(I) = AFMIN, where X(I) is a real array of N elements in which the initial estimate of the solution is set.
AKMIN	:	A real number in which the relative error tolerance required in the constraint residuals must be set.
MAXFN	:	An integer in which the maximum number of calls of ALAGB (users' supplied subroutine) on any unconstrained minimization must be set.
IPR1	:	An integer controlling the frequency of printing for ALAGA subroutine, IPR1 is usually set to 1 for printing, if IPR1 = 0, then no printing.
IPR2	:	IPR2 = MAXFN + IPR1, an integer controlling the frequency of printing from QNTA, the minimization routine.
IW	:	An integer giving the amount of storage available in COMMON statement.
MODE	:	An integer controlling the mode of operation of ALAGA. A normal setting is that MODE = 1.
DFN	:	DFN is set to zero.

The important controlling parameters the user needs to change for different programs are N, M, K, EPS, AKMIN, MAXFN.

3.4.2 User Supplied Subroutine ALAGB.

ALAGB is the only user supplied subroutine. This subroutine gives the information about constraint equations and their first order derivatives. The following steps are used to prepare the computer code for this subroutine:

Step 1

Define array variables x(1) to x(N), were N is to the number of the design unknowns.

Step 2

Manipulate the constraint equations such that they are simplified as much as possible.

Step 3

Examine the constraints obtained in Step 2, and assign a name to common constant terms in order to further simplify the constraint equations. Step 2 and 3 will save computer data preparation time.

Step 4

Now transform all the constraint equations in terms of the array variables X(1) to X(N) and the constant name created in Step 3. The computer program layout is such that the inequality constraints come after the equality constraints. The constraints are designated from C(1) to C(M), where M is the total number of equality and inequality constraints.

Step 5

Take first derivatives of the objective function and the constraints with respect to their corresponding variables. For example, assume constraint C(i) contains one variable X(j), then the derivative will be designated as GC(j,i). For the objective function, the derivative will be designated as G(j), where j is one of the variables contained in the objective function.

Step 6

The computer code for the subroutine ALAGB will have the following layout:

```
COMMON STATEMENT
EQUATE Xi = X(i) (This enables the users to use Xi instead
                  of X(i))
OBJECTIVE FUNCTION F
CONSTRAINT EQUATION C(i)
DERIVATIVES OF OBJECTIVE FUNCTION G(j)
DERIVATIVES OF ALL THE CONSTRAINTS GC(j,i)
RETURN
END
```

The user is referred to Appendix B for more programming details.

Example

Consider the EMI constraint:

$$C(13) = \frac{S}{\sqrt{1+\left(\frac{F}{2000}\right)^2}} \quad \frac{1}{A} - \left[\left(\frac{L_2C_4}{L_1C_3}\right)(2\pi F\sqrt{L_1C_3})^3 \frac{1}{D} - \frac{C_4}{C_3}(2\pi F\sqrt{L_1C_3})^2\right]^{-1}$$

$$\text{where } A = \frac{E_0}{\pi^2 L_5 F} \quad \text{Sin} \frac{\pi(E_0-E_1)}{E_1}$$

$$D = R_3\left(\frac{C_3}{L_1}\right)^{0.5}$$

Step 1: Assign variable name:

$X_7 = L_1$
$X_9 = C_3$
$X_{10} = C_4$
$X_{15} = R_3$
$\frac{X_7}{PEI} = L_2$
$X_{20} = L_5$

Step 2: Manipulate the equation:

$$C(13) = \frac{S}{\sqrt{1+\left(\frac{F}{2000}\right)^2}} \; \frac{1}{\frac{E_0}{\pi^2 L_5 F} \operatorname{Sin} \frac{\pi(E_0-E_1)}{E_1}} - \frac{1}{4\pi^2 F^2 C_4 L_1 \left[\frac{2\pi F L_1}{PEIR_3} - 1\right]}$$

Step 3: Assign constant name:

$$\text{let } XM26 = \frac{S}{\sqrt{1+\left(\frac{F}{2000}\right)^2}} \; \frac{1}{\frac{E_0}{\pi^2 F} \operatorname{Sin} \frac{\pi(E_0-E_1)}{E_1}}$$

$$XM27 = 4\pi^2 F^2$$

$$XM28 = \frac{2\pi F}{PEI}$$

Step 4: Constraint equation:

Now C(13) becomes

$$-1 + (XM26)(XM27)X_7X_{10}X_{20}\left(XM28\frac{X_7}{X_{15}} - 1\right) \geq 0.$$

Step 5: Take first derivatives

$$GC(7,13) = 2.0(XM26)(XM27)(XM28)\frac{X_7X_{10}X_{20}}{X_{15}}$$

$$-(XM26)(XM27)X_{10}X_{20}$$

$$GC(10,13) = (XM26)(XM27)\;X_7X_{20}\left(XM28\frac{X_7}{X_{15}} - 1\right)$$

$$GC(15,13) = -(XM26)(XM27)(XM28)\frac{X_7^2X_{10}X_{20}}{X_{15}^2}$$

$$GC(20,13) = (XM26)(XM27)X_7X_{10}\left(XM28\frac{X_7}{X_{15}} - 1\right)$$

STEP 6: = Set up computer code for subroutine ALAGB.

3.4.3 Initial Starting Point and Scaling Technique

3.4.3.1 Selection of initial starting point

For a complicated nonlinear optimization problem with 20 or more variables, proper selection of the initial starting point plays an important role in the speed of convergence and accuracy of the solution. As a general guideline, the initial starting point should be selected such that the value of each equality constraint is as small as possible. This point must also satisfy the inequality constraints in order to stay in the feasible region. A properly selected initial starting point will speed up the rate of convergence. The time and effort spent to choose a good initial point prior to running the program is well worth the result. For a practical problem, choice of a good initial starting point can usually be based on the designer's past experience, or on some simplified design guidelines and equations.

3.4.3.2 Variable scaling technique and convergence

In a switching power converter design, the values of the design variables are scattered over a wide range. The capacitance may be in the order of 10^{-4}, for example, and the switching frequency in the order of 10^{5}. This wide scattering of values is one of the primary causes of convergence difficulty. Therefore, a variable scaling technique is provided in the computer program to scale all the variables between values of 1 and 10. For example: if $x_1 = 0.5\text{x}10^{-6}$ and $x_2 = 0.8\text{x}10^{3}$, then one can use VSCAL (1) = 10^{-7}, VSCAL (2) - 10^{2}, so that:

$$\frac{x_1}{\text{VSCAL (1)}} = 5.0 \quad \frac{X_2}{\text{VSCAL (2)}} = 8.0,$$

where VSCAL (1), VSCAL (2) are scale factors for the respective variables.

For reasonably acceptable accuracy, the tolerance for variable convergence (EPS) is set around EPS = 10^{-6} to 10^{-7}. For the program to exist from the iterative computation through the variable convergence criterion, it must satisfy the following requirement:

$$\max \left| x_i^{(k)} - x_i^{(k-1)} \right| \leq \text{EPS}$$

This requirement states that the largest difference between two values of any variable from consecutive iterations must be less than the tolerance required. It should also be mentioned that the program can exist via a constraint convergence criterion.

3.4.3.3 Constraint scaling technique and convergence

It is very unlikely that the initial starting point can satisfy all the constraints to the extent that each equality constraint residual is smaller than the constraint tolerance and each inequality constraint is also satisfied. If the starting poing did satisify all the constraints, then, of course, the problem would already be solved. In reality, the constraint values based as the initial guess can vary over a wide range. Since conditions where certain constraint values may be so large that the effects of other constraints are obscured should be avoided, it is desirable to scale each constraint by such a factor that the effect of violating any given constraint is of the same order of magnitude as the effect of violating any other constraint. Unfortunately there are no universal guidelines for selecting the constraint scaling paramerters. It has been observed that faster convergence can be achieved by the proper selection of these parameters; however, improper use of constraint scaling can cause divergence problems. Experience shows

that by scaling the constraint values in a range between 10^2 and 10^{-2}, and setting the constraint tolerance around 10^{-3}, the program can achieve a faster rate of convergence.

For an acceptable accuracy, the constraint tolerance AKMIN is set around 10^{-3} to 10^{-4} using the scaling technique. Whenever the maximum scaled constraint violation $AKK^{(k)}$ is less than AKMIN, program convergence is reached. This stopping criteria can be put in a more concise way in the following.

$C_i^{(k)}$: Constraint value for ith constraint in iteration k

SC_i : Scale factor for the ith constraint

$WW_i^{(k)}$: Scaled constraint violation for ith constraint in iteration k

That is $$WW_i^{(k)} = \frac{|C_i^{(k)}|}{SC_i}$$

$AKK^{(k)}$: Largest scaled constraint violation in iteration k, that is,

$$AKK^{(k)} = \max_i \{WW_i^{(k)}\}$$

Whenever $AKK^{(k)} \leq AKMIN$, the convergence is reached and computation is terminated.

The program sometimes can also be run without using the constraint scaling technique. Experience shows, however, that by using the constraint scaling technique the program can be brought under better control.

3.4.4 Stopping Criteria for Computation

For normal exit, there are constraint convergence criterion and variable convergence criterion as mentioned in the previous subsections. In most cases, constraint convergence is deemed more desirable. The accuracy of the result however depends on how to choose the constraint tolerance and variable tolerance. In some circumstances, the solution via variable

convergence criterion is sufficiently accurate to be acceptable. Infinite looping and abnormal exit are also possible as shown in the flowchart in Fig. 3.4.2.

Discussion of flowchart

EXIT 1

This exit means the objective function has been evaluated a number of times equal to the user's supplied paramteter MAXFN. The solutions from this exit are in most cases not accurate. The user may increase MAXFN to get proper convergence and more accurate solutions.

EXIT 2

This exit means the largest scaled constraint violation is less than the constraint tolerance. The solution from this exit is deemed most desirable.

EXIT 3

The exit means the largest difference of variables between consecutive iteration is less than the variable tolerance. Depending on the exit condition, the solution from this exit is often acceptable.

LOOP 4

In this red tape loop, the program is never converged. The user must set execution time limit or printing page limit in case endless loop occurs.

3.4.5 Checklist for Computer Printout

The following checklist is provided for the user to assure the final solution is accurate and acceptable.

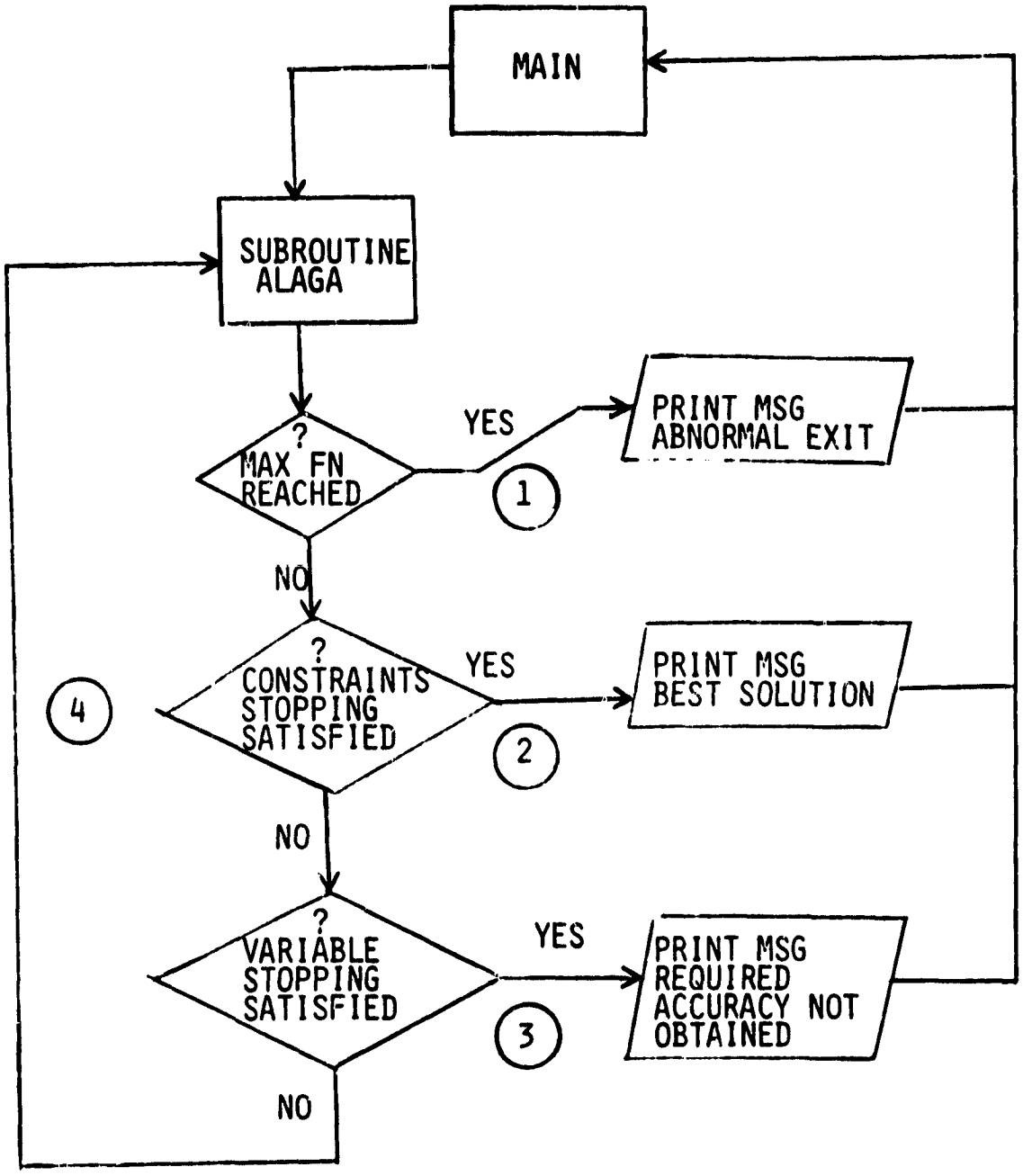
(1) Check if the solution C is in the feasible region, that is, if the inequality constraint residuals are all greater than zero.

(2) Check the accuracy of the solution obtained. That is: check if largest scaled constraint violation is less than AKMIN.

(3) Check if MAXFN IS REACHED, if the exit is normal or abnormal.

(4) Check if the solution X is reasonable using common sense and previous experience.

If the solution obtained is not accurate enough then one can follow the flowchart as shown in Fig. 3.4.3, by changing the starting point (using the final result of the previous run) or readjusting the scaling factors and rerun the program.



where

MAIN = main program

ALAGA = subroutine that manages the stopping algorithm

Figure 3.4.2 Flowchart of Computation Stopping Algorithm

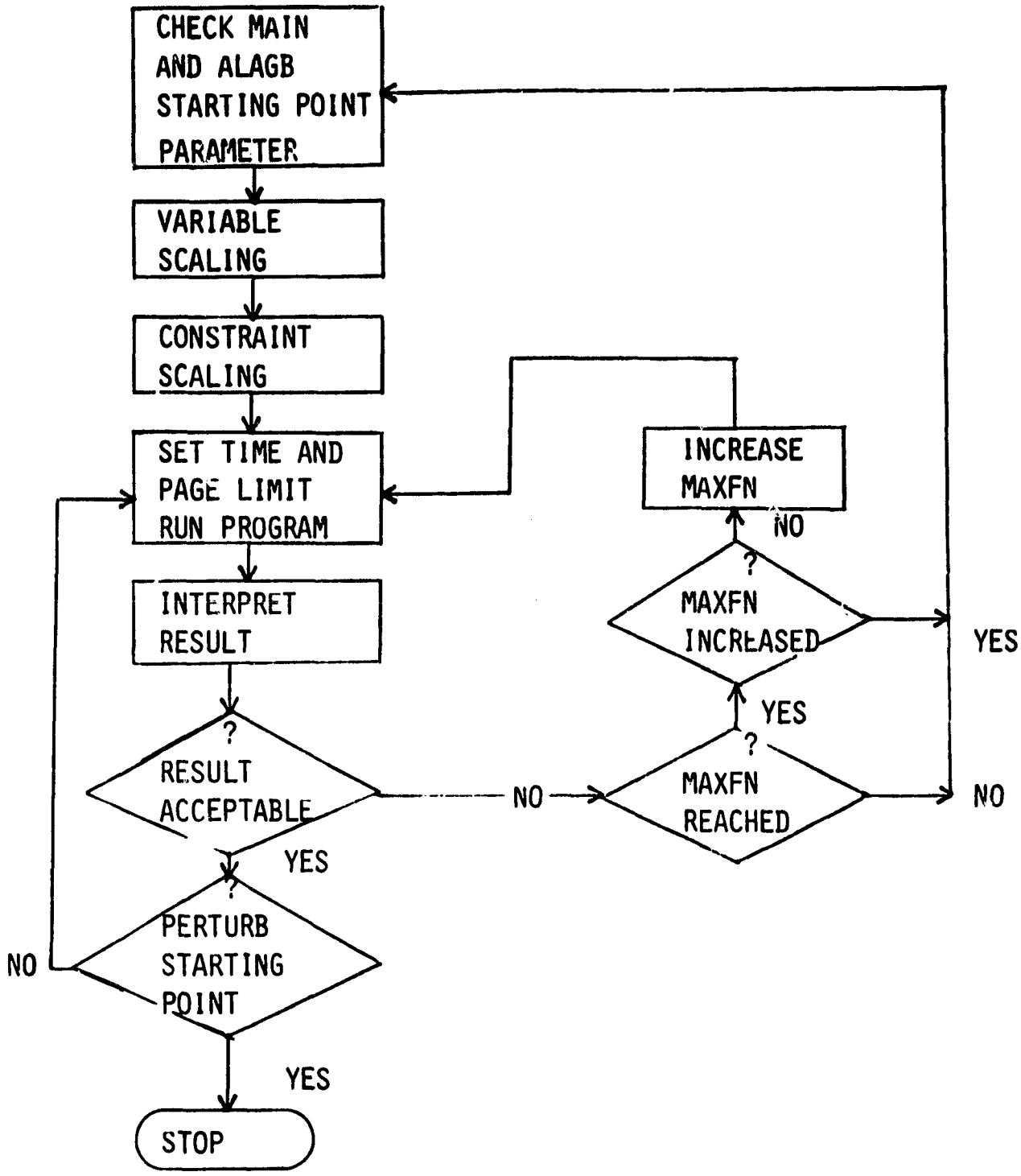


Figure 3.4.3 Flowchart of Effective Programming Approach

3.5 OPTIMIZATION RESULTS OF BOOST CONVERTER

The transistor switching frequency is a critical parameter in the minimum weight design of switching power converter. In the course of optimization the frequency is held constant for a computer run and a sufficient number of runs are collected carrying the frequency over a certain range of interest. Several distinct advantages can be obtained in this approach:

(1) By treating the frequency as a constant in each computer run, the nonlinear optimization problem is simpler and reaches convergence easily.

(2) Important design insights can be obtained when the weight and loss are plotted against frequency. Instead of identifying a single optimum switching frequency and a minimum weight design as in our earlier optimization attempt [8], the curve presented here provides a range of frequencies in which the system weight is minimized in all practical sense. The curve will also provide information regarding sensitivity of the converter weight as a function of the switching frequency.

(3) The trade-offs between weight and loss as a function of switching frequency can be evaluated readily. This information can be used as a design guideline for the weight/efficiency optimization.

By treating the switching frequency as a constant in the optimization process, a set of design data as a function of switching frequency is obtained by varying the frequency between 20KHz to 120KHz in a 10KHz step. The design parameters specified in Section 3.2 are employed to make these computer runs. Detailed design results including the detailed loss and weight breakdowns of various components are collected and tabulated in Table 3.5-I. The minimum weight converter design data including the details of magnetic design for each chosen frequency are shown in each column. This helps in the

F	20K	30K	40K	50K	60K	70K	80K	90K	100K	110K	120K
A1	0.469×10^{-5}	0.438×10^{-5}	0.436×10^{-5}	0.358×10^{-5}	0.459×10^{-5}	0.279×10^{-5}	0.229×10^{-5}	0.236×10^{-5}	0.208×10^{-5}	0.175×10^{-5}	0.174×10^{-5}
N1	94.297	79.345	79.098	69.350	27.441	26.907	27.109	19.767	22.550	22.798	22.771
AC1	0.384×10^{-6}	0.322×10^{-6}	0.319×10^{-6}	0.243×10^{-6}	0.119×10^{-6}	0.856×10^{-7}	0.783×10^{-7}	0.604×10^{-7}	0.634×10^{-7}	0.556×10^{-7}	0.555×10^{-7}
Z1	0.405×10^{-1}	0.349×10^{-1}	0.347×10^{-1}	0.289×10^{-1}	0.169×10^{-1}	0.137×10^{-1}	0.129×10^{-1}	0.111×10^{-1}	0.112×10^{-1}	0.105×10^{-1}	0.104×10^{-1}
R1	0.697×10^{-1}	0.676×10^{-1}	0.678×10^{-1}	0.708×10^{-1}	0.645×10^{-1}	$0.6[illegible]\times10^{-1}$	0.688×10^{-1}	0.659×10^{-1}	0.673×10^{-1}	$0.71[illegible]\times10^{-1}$	0.710×10^{-1}
L1	0.665×10^{-4}	0.527×10^{-4}	0.523×10^{-4}	0.376×10^{-4}	0.189×10^{-4}	0.113×10^{-4}	0.931×10^{-5}	0.673×10^{-5}	0.672×10^{-5}	0.564×10^{-5}	0.562×10^{-5}
A2	0.306×10^{-5}	0.250×10^{-5}	0.247×10^{-5}	0.186×10^{-5}	0.906×10^{-5}	0.247×10^{-5}	0.203×10^{-5}	0.135×10^{-5}	0.127×10^{-5}	0.103×10^{-5}	0.102×10^{-5}
N2	48.282	46.461	46.648	44.602	8.288	10.119	10.214	11.584	12.280	12.934	12.945
AC2	0.369×10^{-6}	0.351×10^{-6}	0.349×10^{-6}	0.278×10^{-6}	0.135×10^{-6}	0.102×10^{-6}	0.952×10^{-7}	0.726×10^{-7}	0.709×10^{-7}	0.642×10^{-7}	0.642×10^{-7}
Z2	0.291×10^{-1}	0.276×10^{-1}	0.275×10^{-1}	0.240×10^{-1}	0.130×10^{-1}	0.106×10^{-1}	0.100×10^{-1}	0.878×10^{-2}	0.878×10^{-2}	0.829×10^{-2}	0.829×10^{-2}
R2	0.300×10^{-1}	0.274×10^{-1}	0.274×10^{-1}	0.286×10^{-1}	0.181×10^{-1}	0.204×10^{-1}	0.200×10^{-1}	0.243×10^{-1}	0.256×10^{-1}	0.267×10^{-1}	0.267×10^{-1}
L2	0.222×10^{-4}	0.176×10^{-4}	0.174×10^{-4}	0.125×10^{-4}	0.631×10^{-5}	0.375×10^{-5}	0.310×10^{-5}	0.224×10^{-5}	0.224×10^{-5}	0.188×10^{-5}	0.187×10^{-5}
A5	0.178×10^{-4}	0.127×10^{-4}	0.108×10^{-4}	0.902×10^{-5}	0.886×10^{-5}	0.643×10^{-5}	0.592×10^{-5}	0.433×10^{-5}	0.440×10^{-5}	0.331×10^{-5}	0.318×10^{-5}
N5	34.332	37.577	34.494	35.774	35.111	45.280	45.681	74.055	70.519	76.611	76.534
AC5	0.398×10^{-6}	0.329×10^{-6}	0.295×10^{-6}	0.259×10^{-6}	0.101×10^{-6}	0.912×10^{-7}	0.816×10^{-7}	0.396×10^{-7}	0.347×10^{-7}	0.291×10^{-7}	0.285×10^{-7}
Z5	0.340×10^{-1}	0.309×10^{-1}	0.282×10^{-1}	0.265×10^{-1}	0.199×10^{-1}	0.194×10^{-1}	0.185×10^{-1}	0.161×10^{-1}	0.154×10^{-1}	0.141×10^{-1}	0.139×10^{-1}
R5	0.477×10^{-1}	0.531×10^{-1}	0.504×10^{-1}	0.541×10^{-1}	0.1353	0.1648	0.1786	0.510	0.589	0.626	0.626
L5	0.255×10^{-4}	0.273×10^{-4}	0.229×10^{-4}	0.220×10^{-4}	0.245×10^{-4}	0.246×10^{-4}	0.239×10^{-4}	0.320×10^{-4}	0.317×10^{-4}	0.244×10^{-4}	0.239×10^{-4}
C3	0.133×10^{-4}	0.322×10^{-5}	0.318×10^{-5}	0.201×10^{-5}	0.200×10^{-5}	0.200×10^{-5}	0.200×10^{-5}	0.200×10^{-5}	0.199×10^{-5}	0.205×10^{-5}	0.200×10^{-5}
R3	0.163×10^{-1}	0.162×10^{-1}	0.162×10^{-1}	0.162×10^{-1}	0.524×10^{-2}	0.524×10^{-2}	0.524×10^{-2}	0.524×10^{-2}	0.523×10^{-2}	0.523×10^{-2}	0.522×10^{-2}
C4	0.655×10^{-5}	0.161×10^{-5}	0.159×10^{-5}	0.101×10^{-5}	0.100×10^{-5}	0.100×10^{-5}	0.100×10^{-5}	0.100×10^{-5}	0.996×10^{-6}	0.103×10^{-5}	0.100×10^{-5}
C6	0.109×10^{-3}	0.760×10^{-4}	0.678×10^{-4}	0.595×10^{-4}	0.511×10^{-4}	0.468×10^{-4}	0.442×10^{-4}	0.390×10^{-4}	0.376×10^{-4}	0.389×10^{-4}	0.378×10^{-4}
E	0.9397	0.9465	0.9467	0.9462	0.9389	0.9355	0.9316	0.8991	0.8929	0.8821	0.8816
PQ	0.3883	0.4427	0.5106	0.5729	0.6319	0.6945	0.7581	0.3362	0.9056	0.9916	1.0570
PD	1.7682	1.7725	1.7776	1.7904	1.8243	1.8457	1.8622	1.9635	1.9918	2.020	2.0354
PCAP	1.30×10^{-1}	0.175×10^{-1}	0.198×10^{-1}	0.226×10^{-1}	0.277×10^{-1}	0.310×10^{-1}	0.333×10^{-1}	0.479×10^{-1}	0.518×10^{-1}	0.538×10^{-1}	0.556×10^{-1}
PMAG	2.3232	1.7262	1.6362	1.5969	2.0648	2.2546	2.3244	5.009	5.4482	6.2944	6.2469
PT	4.4928	3.9589	3.9442	3.9829	4.5489	4.8259	4.9780	7.8568	8.3975	9.3600	9.3050
WS	2.4186	2.4013	2.4007	2.4020	2.4204	2.4294	2.4343	2.5278	2.5454	2.5766	2.5778
WH	0.2917	0.2571	0.2561	0.2586	0.2954	0.3133	0.3232	0.5101	0.5453	0.6078	0.6101
WI	0.691×10^{-2}	0.479×10^{-2}	0.409×10^{-2}	0.302×10^{-2}	0.249×10^{-2}	0.148×10^{-2}	0.124×10^{-2}	0.843×10^{-3}	0.799×10^{-3}	0.573×10^{-3}	0.554×10^{-3}
WW	0.113×10^{-1}	0.834×10^{-2}	0.757×10^{-2}	0.518×10^{-2}	0.136×10^{-2}	0.108×10^{-2}	0.925×10^{-3}	0.603×10^{-3}	0.554×10^{-3}	0.445×10^{-3}	0.434×10^{-3}
WC	0.179×10^{-1}	0.798×10^{-2}	0.730×10^{-2}	0.581×10^{-2}	0.519×10^{-2}	0.489×10^{-2}	0.470×10^{-2}	0.432×10^{-2}	0.422×10^{-2}	0.436×10^{-2}	0.424×10^{-2}
WMAG	0.182×10^{-1}	0.111×10^{-1}	0.117×10^{-1}	$0.8[illegible]1\times10^{-2}$	0.385×10^{-2}	0.236×10^{-2}	0.217×10^{-2}	0.145×10^{-2}	0.135×10^{-2}	0.102×10^{-2}	0.989×10^{-3}
WT	2.7465	2.6794	2.6759	2.6747	2.7249	2.7502	2.7644	3.0437	3.0962	3.1898	3.1930

Table 3.5-I Boost Converter Optimization Results

assessment of the optimum component design as a function of switching frequency. The designations utilized in the loss and weight breakdowns are shown below.

PQ	=	Total power dissipation in the transistor
PD	=	Power dissipation in the diode
PCAP	=	Power dissipation in the output filter capacitor
PMAG	=	Total magnetic loss (core loss + winding loss)
PT	=	Total loss
WS	=	Source weight
WH	=	Packaging Weight
WI	=	Magnetic core weight
WC	=	Capacitor weight
WW	=	Winding (copper conductor) weight
WMAG	=	WW + WI
WT	=	Total weight

In order to gain more design insights, the total-weight/total-loss and the component weights/loss breakdowns are plotted against the switching frequency in Fig. 3.5.1 and Fig. 3.5.2, respectively. Summarized in the following are several important observations from the table and curves.

(1) The curve of total weight versus frequency exhibits U-shape characteristics. The converter weight is heavier at both low frequency end and high frequency end.

(2) The total weight of the converter reaches its minimum value in the frequency range from 30KHz to 50KHz.

(3) The U-shape curve is also observed by plotting the total loss characteristics against frequency. The rapid decrease of the total loss at lower switching frequencies is caused by the reduction of winding losses of the magnetics, meanwhile the increasing total loss at higher frequencies is caused by the higher switching

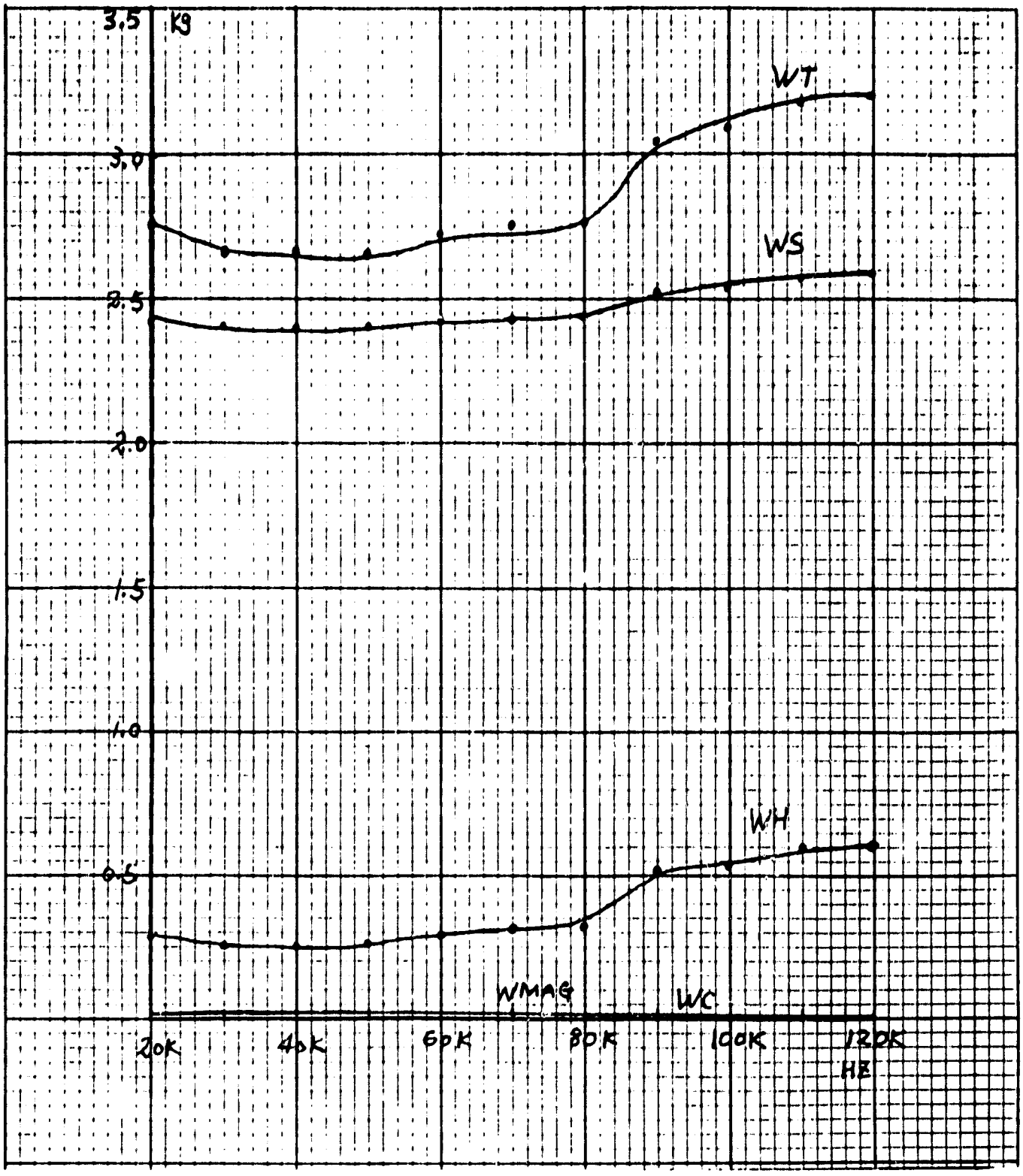


Figure 3.5.1 Weight Breakdowns for Boost Converter

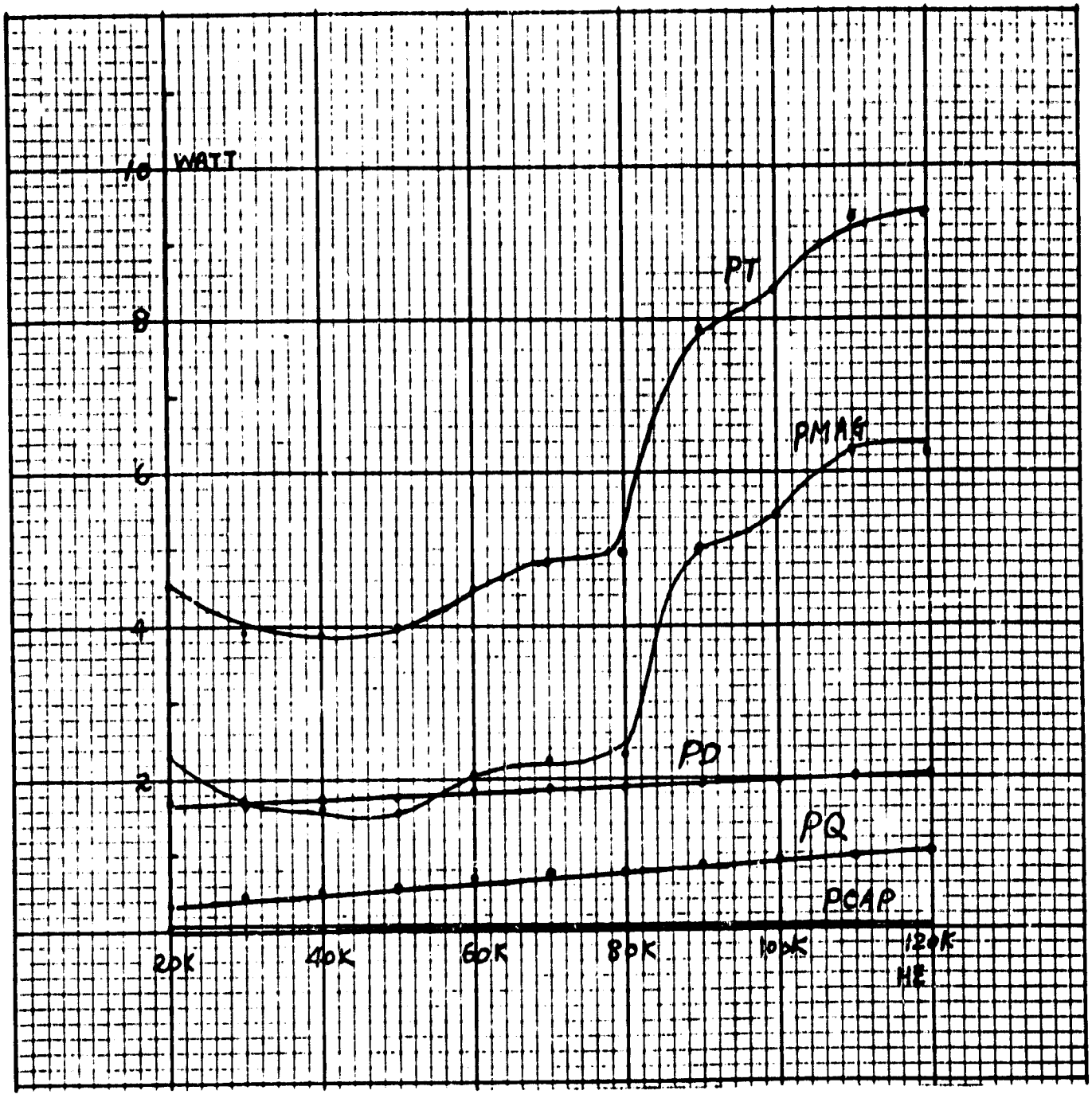


Figure 3.5.2 Loss Breakdowns for Boost Converter

losses and much rapidly increasing magnetic losses. As a result of the increase of total loss at high frequencies, the source weight and packaging weight also increase rapidly. The weight reduction due to the decreasing magnetic component weight as frequency increases is less pronounced than the increase of packaging and source weight. Therefore a U-shape curve of total weight vs. frequency is formed. The U-shaped curve implies that there exists an optimal switching frequency.

3.6 DESIGN OPTIMIZATION OF BUCK-BOOST CONVERTER

The Buck-Boost switching power converter is chosen as a second example. The same procedure used for the design of Boost converter is now applied to Buck-Boost. The circuit schematic and problem formulation are stated in the following. The input-output relationship and derivations of the constraints are given in Appendix F. The results of design optimization are demonstrated in Section 3.7.

3.6.1 Circuit Schematic, Design Variables, and Waveforms

The circuit parameters and design unknowns are shown in Fig. 3.6.1. There are 24 unknown variables including the details of magnetic design. This circuit contains a two-stage input-filter, a two-winding energy storage inductor, a power transistor, a diode and an output filter. When the transistor is turned on, the energy from the source is stored in the two-winding energy storage inductor; the output filter capacitor C_5 supplies power to the load. When the transistor is switched off, the energy previously stored in the inductor is dumped out to the load where it also replenishes the output-filter-capacitor energy.

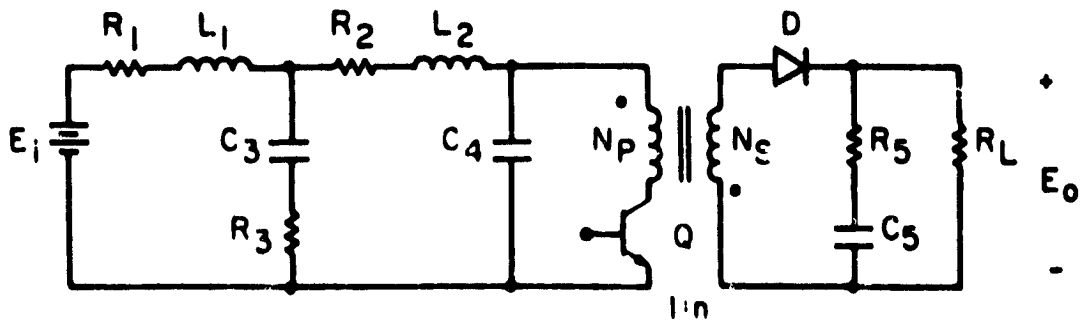
The operating waveforms are shown in Fig. 3.6.2. These waveforms are used in derivations of design constraints such as the output ripple factor, and EMI constraint, etc. The notations marked on the waveform are defined as follows:

$2d$ = peak-peak ripple current through transistor Q

$I_i \frac{Ton}{T}$ = average input current from source E_i

I_0 = output DC current

n = primary-to-secondary turns ratio of energy storage inductor, (= 1 in the design example presented in Section 3.7).



Design Unknowns: 24 variables

R_1, R_2, R_p	:	DC winding resistance of inductor and transformer
R_3	:	Input filter resistor
L_1, L_2	:	Input filter inductor
L_p	:	Primary inductance of two winding inductor
C_3, C_4, C_5	:	Filter capacitor
A_1, A_2, A_p	:	Cross section area of inductor or transformer
Z_1, Z_2, Z_p	:	Mean magnetic path length
N_1, N_2, N_p	:	Number of turns of the winding
A_{C1}, A_{C2}, A_{Cp}	:	Winding area per turn
F	:	Switching frequency
eff	:	Overall efficiency

FIGURE 3.6.1 Circuit Schematic and Design Variables of Buck-Boost Converter

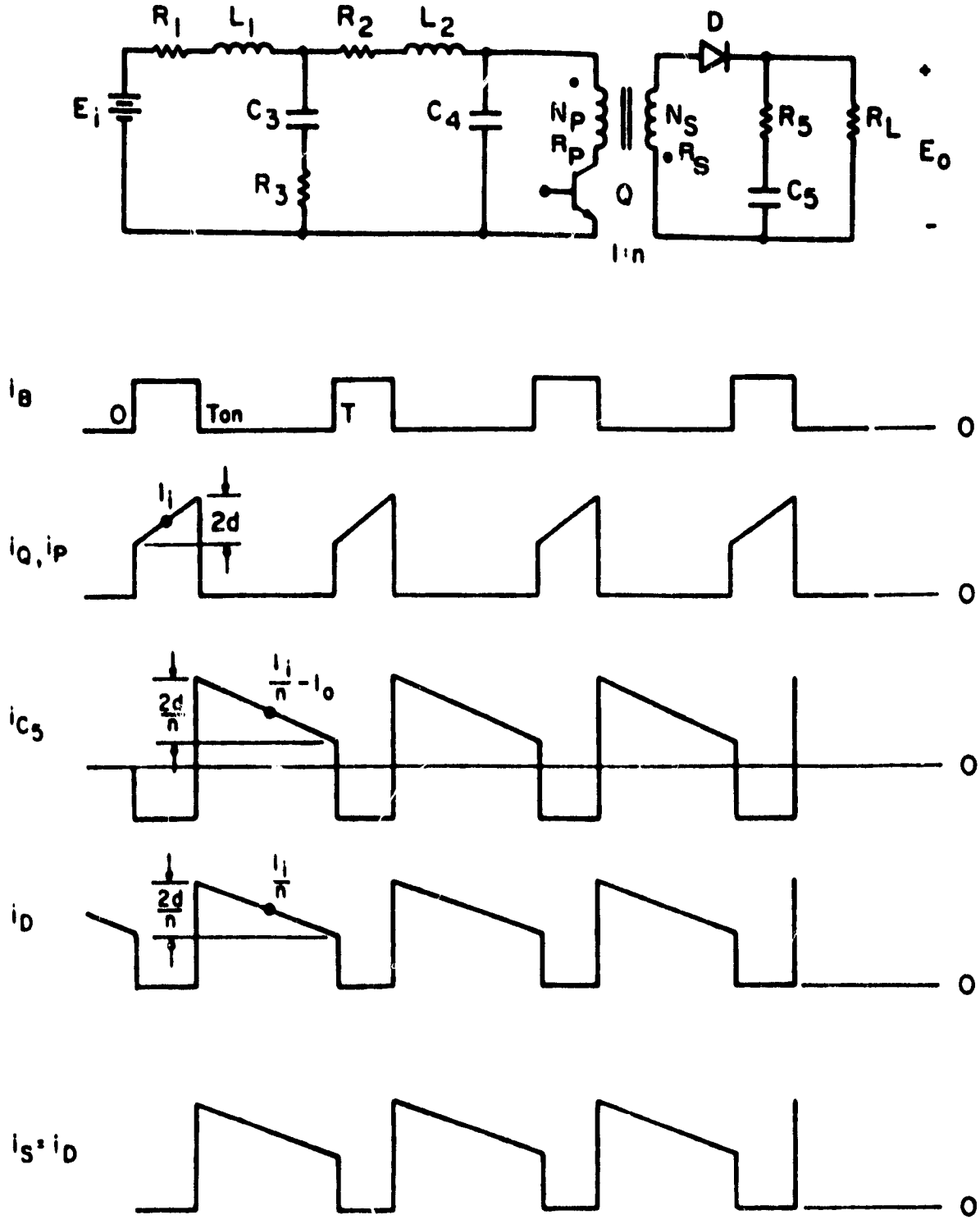


FIGURE 3.6.2 Operating Waveforms of Buck-Boost Converter

3.6.2 Objective Function and Constraints

The notations used previously for the Boost converter are adopted here for Buck-Boost.

3.6.2.1 Objective function: total weight

Core Weight $WI = D_I(A_1Z_1 + A_2Z_2 + A_pZ_p)$

where AZ = Core volume

Winding weight $WTW = 4F_CD_C\ (A_{C1}N_1\sqrt{A_1} + A_{C2}N_2\sqrt{A_2}$

$+ 2A_{Cp}N_p\sqrt{A_p})$

where $4F_C\sqrt{A_1}$ = mean length per turn of the winding

Capacitor weight $= D_{K3}C_3 + D_{K4}C_4 + D_{K5}C_5$

Source weight $= WS = \dfrac{P_0}{\text{eff } K_s}$, where $\dfrac{P_0}{\text{eff}}$ = input power

Heat sink weight $WH = \dfrac{P_0\ (1\text{-eff})}{\text{eff } K_H}$,

where $\dfrac{P_0}{\text{eff}} - P_0$ = total power loss

Objective function $= WI + WTW + WC + WS + WH$ (3.6.1)

3.6.2.2 Constraints

Loss constraint $C(1) = 0$

$$C(1) = P_0\left(\frac{1}{eff} - 1\right) - PIF - PQ - PD - POF \qquad (3.6.2)$$

where

PIF = Input filter copper loss

$$= \left(\frac{P_0}{eff\ E_I}\right)^2 (R_1 + R_2)$$

PQ = Transistor saturation loss + Base drive loss

+ transistor turn on loss + transistor turn off loss

$$= \frac{P_0 V_{ST}}{eff\ E_I} + \frac{0.1\ P_0 V_{BE}}{eff\ E_I}$$

$$+ \frac{T_{SR} F}{6}\left(\frac{E_0 + V_D}{n} + E_I + 2V_{ST}\right)\left(\frac{P_0}{eff\ E_I}\frac{E_0 + nE_I}{E_0} - \frac{E_I E_0}{2L_p(E_0 + nE_I)F}\right)$$

$$+ \frac{T_{SF} F}{6}\left(\frac{E_0 + V_D}{n} + E_I + 2V_{ST}\right)\left(\frac{P_0}{eff\ E_I}\frac{E_0 + nE_I}{E_0} + \frac{E_I E_0}{2L_p(E_0 + nE_I)F}\right) \qquad (3.6.3)$$

PD = Diode conduction loss + Turn on loss

+ Turn off loss

$$= \frac{P_0 V_D}{eff\ E_0} + \frac{(nE_I + E_0)}{12}\left[\frac{P_0(E_0 + nE_I)}{eff\ nE_I E_0} + \frac{E_1 E_0}{2nLp(E_0 + nE_I)F}\right]$$

$$+ \frac{(nE_I + E_0)(T_{SD} + 3T_{RE})F}{12}\left[\frac{P_0(E_0 + nE_I)}{eff\ nE_I E_0}\right.$$

$$\left. - \frac{E_I E_0}{2nLp(E_0 + nE_I)F}\right] \tag{3.6.4}$$

POF = Two-winding inductor T copper and core losses

$$= \frac{E_0}{(E_0 + nE_I)}\left[\left(\frac{P_0(E_0 + nE_I)}{eff\ E_I E_0}\right)^2 + \frac{E_I{}^2 E_0{}^2}{12L_p^2(E_0 + nE_I)^2 F^2}\right]R_p$$

$$+ \frac{nE_I}{E_0 + nE_I}\left[\frac{E_I{}^2 E_0{}^2}{12n^2 L_p{}^2 (E_0 + nE_I)^2 F^2}\right.$$

$$\left. + \frac{(E_0 + nE_I)^2 P_0{}^2}{eff^2 n^2 E_I{}^2 E_0{}^2}\right]n^2 R_p$$

$$+ \frac{E_I E_0}{(E_0 + nE_I)N_p}(80\ Z_p\sqrt{F})(0.0022) \tag{3.6.5}$$

PCAP = Output filter capacitor ESR loss

$$= \frac{E_0}{E_0 + nE_I}\left(\frac{P_0}{E_0}\right)^2 R_5 + \frac{nE_I}{E_0 + nE_1}\left[\frac{E_I{}^2 E_0{}^2}{12n^2 L_p{}^2 (E_0 + nE_I)^2 F^2}\right.$$

$$\left. + \left(\frac{(E_0 + nE_I)P_0}{nE_I E_0 e_{ff}} - \frac{P_0}{E_0}\right)^2\right]R_5 \tag{3.6.6}$$

Parasitic resistance for L_1, L_2, T, C(2) = C(3) = C(12) = 0

$$C(2) = R_1 A_{C1} - 4pF_C N_1 \sqrt{A_1} \tag{3.6.7}$$

$$C(3) = R_2 A_{C2} - 4pF_C N_2 \sqrt{A_2} \tag{3.6.8}$$

$$C(12) = R_p A_{Cp} - 4pF_C N_p \sqrt{A_p} \tag{3.6.9}$$

Input filter peaking constraint C(4) = 0

$$C(4) = (PEI)^2 - \frac{1 + \frac{R_3^{\,2} C_3}{L_1}}{\left(\frac{C_4}{C_3}\right)^2 + \left(\frac{R_3^{\,2} C_3}{L_1}\right)\left[1 - \frac{C_4}{C_3} - \frac{L_2}{L_1}\frac{C_4}{C_3}\right]^2} \tag{3.6.10}$$

Operating flux density constraint C(5) = C(6) = C(9) = 0

$$C(5) = N_1 A_1 - \frac{L_1 P_0}{\text{eff } E_I B_{S1}} \tag{3.6.11}$$

$$C(6) = N_2 A_2 - \frac{L_2 P_0}{\text{eff } E_I B_{S2}} \tag{3.6.12}$$

$$c(9) = N_p A_p - \frac{L_1}{B_{Sp}}\left[\frac{P_0(E_0 + nE_I)}{\text{eff } E_I E_0} + \frac{E_I E_0}{2Lp(E_0 + nE_I)F}\right] \tag{3.6.13}$$

Window area constraint C(7) = C(8) = C(10) = 0

$$C(7) = \left(\frac{N_1 A_{C1}}{F_W}\right)^{0.5} - \frac{Z_1}{2\pi} + \frac{\sqrt{A_1}}{2} \tag{3.6.14}$$

$$C(8) = \left(\frac{N_2 A_{C2}}{F_W}\right)^{0.5} - \frac{Z_2}{2\pi} + \frac{\sqrt{A_2}}{2} \tag{3.6.15}$$

$$C(10) = \left(\frac{2N_p A_{Cp}}{F_W}\right)^{0.5} - \frac{Z_p}{2\pi} + \frac{\sqrt{A_p}}{2} \tag{3.6.16}$$

Output ripple factor constraint C(11) = 0

$$C(11) = V_R - \left[\frac{P_0(E_0 + nE_I)}{\text{eff } E_I E_0^2 n} + \frac{E_I}{2Lp(E_0 + nE_I)nF}\right] R_5 - \frac{P_0}{2E_0(E_0 + nE_I)C_5 F} \tag{3.6.17}$$

Frequency dependent source EMI constraint C(13) ≥ 0

$$C(13) = \frac{S}{\sqrt{1 + \left(\frac{F}{2000}\right)^2}} \frac{1}{\sqrt{A^2 + B^2}} - \left[\left(\frac{L_2 C_4}{L_1 C_3}\right)(2\pi F\sqrt{L_1 C_3})^3 \left(\frac{1}{D}\right) - \frac{C_4}{C_3}\left(2\pi F\sqrt{L_1 C_3}\right)^2\right]^{-1} \tag{3.6.18}$$

where $A = \frac{2P_0(E_0 + nE_I)}{\pi \text{eff } E_I E_0} \sin \frac{\pi E_0}{E_0 + nE_I}$

$$B = \frac{E_I E_0}{\pi L p (E_0 + nE_1) F} \left[\cos \frac{\pi E_0}{E_0 + nE_1} - \frac{\sin \frac{\pi E_0}{E_0 + nE_I}}{\frac{\pi E_0}{E_0 + nE_1}} \right]$$

$$D = R_3 \left(\frac{C_3}{L_1} \right)^{0.5}$$

<u>Other inequality constraint C(14), C(15), C(16), C(17) ≥ 0</u>

$$C(14) = 0.97 - \text{eff} \geq 0 \tag{3.6.19}$$

$$C(15) = R_T - R_1 - R_2 \geq 0 \tag{3.6.20}$$

$$C(16) = C_3 - 1.0 \times 10^{-6} \geq 0 \tag{3.6.21}$$

$$C(17) = C_4 - 1.0 \times 10^{-6} \geq 0 \tag{3.6.22}$$

3.7: OPTIMIZATION RESULTS OF BUCK-BOOST CONVERTER

By treating the switching frequency as a constant in each optimization run, a set of converter parameter data is obtained. This set of parameter data represents the optimum converter design for the specified switching frequency. A sufficient number of runs are executed by varing the frequency between 20 KHz to 120 KHz in a 10 kHz step. Detailed optimization results, following the afore-described design process are collected and tabulated in Table 3.7-I. To facilitate comparison of optimal converter designs between the boost converter and the buck/boost converter, the same input-output requirements, design constants, and converter performance specifications are used. (Reference to Section 3.2 for detailed information.) The turn-ratio $n = N_P/N_S = 1$. The designations employed in Table 3.7.1 are the same as those in Table 3.5-I. To provide more design insights, the weight and loss breakdowns are plotted against the switching frequency in Fig. 3.7.1 and Fig. 3.7.2, respectively.

The difference between converter optimization results for the boost converter and buck/boost converters are summarized as follows:

(1) The Buck-Boost converter is heavier than the Boost converter. In order to have the mininum weight design the Buck-Boost converter has to operate at a higher frequency than Boost power converter.

(2) Switching losses of semiconductor devices are higher for the Buck-Boost converter. This is logical since the switching current amplitude is considerable higher than that of the boost converter for the same input and output voltage and the same power level.

(3) The magnetic component for the buck/boost converter are generally larger in size and heavier in weight.

(4) The magnetic losses (PMAG = core loss + winding loss) for the buck/boost converter are dominated by the winding loss in low frequencies. The PMAG loss characteristic falls rapidly as the switching frequency increases. The high magnetic losses in low frequencies cause severe weight penalty. It is clearly demonstrated in Fig. 3.7.1 and 3.7.2 that in order to minimize the converter weight/loss, it is desirable to operate the converter frequency about 80KHz ~ 100KHz. For the minimum weight/loss boost converter design, however, the optimal frequency rest about 40KHz ~ 60KHz.

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I	20K	30K	40K	50K	60K	70K	80K	90K	100K		120K
A1	0.324×10^{-4}	0.288×10^{-4}	0.254×10^{-4}	0.226×10^{-4}	0.202×10^{-4}	0.174×10^{-4}	0.938×10^{-5}	8.942×10^{-5}	0.954×10^{-5}	0.91	0.911×10^{-5}
N1	50.611	44.098	41.895	40.892	40.050	43.077	61.340	57.774	53.123	51.	48.837
AC1	0.543×10^{-6}	0.444×10^{-6}	0.398×10^{-6}	0.366×10^{-6}	0.335×10^{-6}	0.323×10^{-6}	0.321×10^{-6}	0.309×10^{-6}	0.284×10^{-6}	0.272	0.251×10^{-6}
Z1	0.473×10^{-1}	0.417×10^{-1}	0.387×10^{-1}	0.366×10^{-1}	0.346×10^{-1}	0.340×10^{-1}	0.345×10^{-1}	0.333×10^{-1}	0.315×10^{-1}	0.306	0.291×10^{-1}
R1	0.699×10^{-1}	0.698×10^{-1}	0.695×10^{-1}	0.694×10^{-1}	0.702×10^{-1}	0.729×10^{-1}	0.766×10^{-1}	0.752×10^{-1}	0.756×10^{-1}	0.754	0.768×10^{-1}
L1	0.217×10^{-3}	0.167×10^{-3}	0.141×10^{-3}	0.123×10^{-3}	0.108×10^{-3}	0.103×10^{-3}	0.805×10^{-4}	0.763×10^{-4}	0.712×10^{-4}	0.671	0.619×10^{-4}
A2	0.203×10^{-4}	0.166×10^{-4}	0.145×10^{-4}	0.128×10^{-4}	0.125×10^{-4}	0.167×10^{-4}	0.121×10^{-4}	0.113×10^{-4}	0.103×10^{-4}	0.966×10^{-5}	0.0964×10^{-5}
N2	27.167	25.535	24.420	24.121	21.563	14.872	15.952	16.099	16.440	16.539	15.377
AC2	0.534×10^{-6}	0.452×10^{-6}	0.400×10^{-6}	0.370×10^{-6}	0.336×10^{-6}	0.295×10^{-6}	0.310×10^{-6}	0.297×10^{-6}	0.284×10^{-6}	0.274×10^{-6}	0.271×10^{-6}
Z2	0.355×10^{-1}	0.318×10^{-1}	0.295×10^{-1}	0.279×10^{-1}	0.262×10^{-1}	0.246×10^{-1}	0.234×10^{-1}	0.228×10^{-1}	0.222×10^{-1}	0.217×10^{-1}	0.212×10^{-1}
R2	0.300×10^{-1}	0.302×10^{-1}	0.304×10^{-1}	0.305×10^{-1}	0.297×10^{-1}	0.271×10^{-1}	0.234×10^{-1}	0.238×10^{-1}	0.243×10^{-1}	0.245×10^{-1}	0.231×10^{-1}
L2	0.725×10^{-4}	0.558×10^{-4}	0.469×10^{-4}	0.409×10^{-4}	0.358×10^{-4}	0.342×10^{-4}	0.268×10^{-4}	0.254×10^{-4}	0.237×10^{-4}	0.224×10^{-4}	0.206×10^{4}
AP	0.327×10^{-4}	0.248×10^{-4}	0.207×10^{-4}	0.180×10^{-4}	0.165×10^{-4}	0.140×10^{-4}	0.160×10^{-4}	0.149×10^{-4}	0.146×10^{-4}	0.131×10^{-4}	0.886×10^{-5}
NP	68.957	63.842	59.057	55.911	54.317	50.082	27.325	27.883	29.712	30.358	44.22
ACP	0.172×10^{-6}	0.142×10^{-6}	0.125×10^{-6}	0.115×10^{-6}	0.111×10^{-6}	0.135×10^{-6}	0.179×10^{-6}	0.175×10^{-6}	0.188×10^{-6}	0.181×10^{-6}	0.175×10^{-6}
ZP	0.452×10^{-1}	0.395×10^{-1}	0.358×10^{-1}	0.335×10^{-1}	0.332×10^{-1}	0.324×10^{-1}	0.301×10^{-1}	0.297×10^{-1}	0.307×10^{-1}	0.299×10^{-1}	0.314×10^{-1}
RP	0.301	0.294	0.281	0.269	0.261	0.182	0.796×10^{-1}	0.807×10^{-1}	0.791×10^{-1}	0.796×10^{-1}	0.384×10^{-1}
LP	0.940×10^{-4}	0.692×10^{-4}	0.545×10^{-4}	0.461×10^{-4}	0.428×10^{-4}	0.326×10^{-4}	0.148×10^{-4}	0.156×10^{-4}	0.188×10^{-4}	0.172×10^{-4}	0.179×10^{-4}
C3	0.103×10^{-3}	0.779×10^{-4}	0.621×10^{-4}	0.519×10^{-4}	0.453×10^{-4}	0.389×10^{-4}	0.438×10^{-4}	0.353×10^{-4}	0.128×10^{-4}	0.115×10^{-4}	0.774×10^{-5}
R3	1.128	1.106	1.136	1.166	1.173	1.228	1.129	1.330	1.408	0.974	0.931
C4	0.162×10^{-4}	0.112×10^{-4}	0.898×10^{-5}	0.760×10^{-5}	0.672×10^{-5}	0.563×10^{-5}	0.836×10^{-5}	0.788×10^{-5}	0.720×10^{-5}	0.605×10^{-5}	0.399×10^{-5}
C5	0.148×10^{-3}	0.121×10^{-3}	0.107×10^{-3}	0.985×10^{-4}	0.907×10^{-4}	0.892×10^{-4}	0.112×10^{-3}	0.101×10^{-3}	0.881×10^{-4}	0.868×10^{-4}	0.819×10^{-4}
E	0.8208	0.8238	0.8271	016295	0.8319	0.0567	0.8751	0.8761	0.8783	0.8751	0.8691
PQ	1.4679	1.7866	1.9036	2.1187	2.3252	2.4924	2.8014	2.9771	3.1171	3.3447	3.5515
PD	2.0944	2.1174	2.1389	2.1650	2.1994	2.1445	1.9662	2.0273	2.1182	2.1492	2.2235
PCAP	0.1958	0.2275	0.2489	0.2637	0.2736	0.2761	0.3397	0.3188	0.2964	0.3016	0.3018
PMAG	11.5281	10.9421	10.3432	9.8383	9.3489	6.7959	4.8831	4.5803	4.1676	4.1959	4.4609
PT	15.2862	14.9736	14.6346	14.3857	14.1471	11.7030	9.9904	9.9035	9.6993	9.9915	10.5377
WS	2.7689	2.7589	2.7479	2.7398	2.7320	2.6529	2.5971	2.5943	2.5876	2.5971	2.6149
WH	0.9925	0.9723	0.9503	0.9341	0.9186	0.7603	0.6487	0.6431	0.6298	0.6488	0.6843
WI	0.02992	0.02114	0.01678	0.01394	0.01214	0.01138	0.847×10^{-2}	0.793×10^{-2}	0.762×10^{-2}	0.691×10^{-2}	0.583×10^{-2}
WW	0.02419	0.01639	0.01275	0.01068	0.911×10^{-2}	0.857×10^{-2}	0.790×10^{-2}	0.735×10^{-2}	0.705×10^{-2}	0.652×10^{-2}	0.650×10^{-2}
WC	0.0501	0.03744	0.03065	0.02634	0.02342	0.02078	0.02646	0.02336	0.01694	0.0153	0.0119
WMAG	0.0534	0.03753	0.02952	0.2462	0.02126	0.01995	0.01638	0.01528	0.01467	0.01344	0.01234
WT	3.8650	3.8062	3.7583	3.7249	3.6954	3.4539	3.2886	3.2759	3.2491	3.2747	3.3234

TABLE 3.7-I Buck-Boost Converter Optimization Results

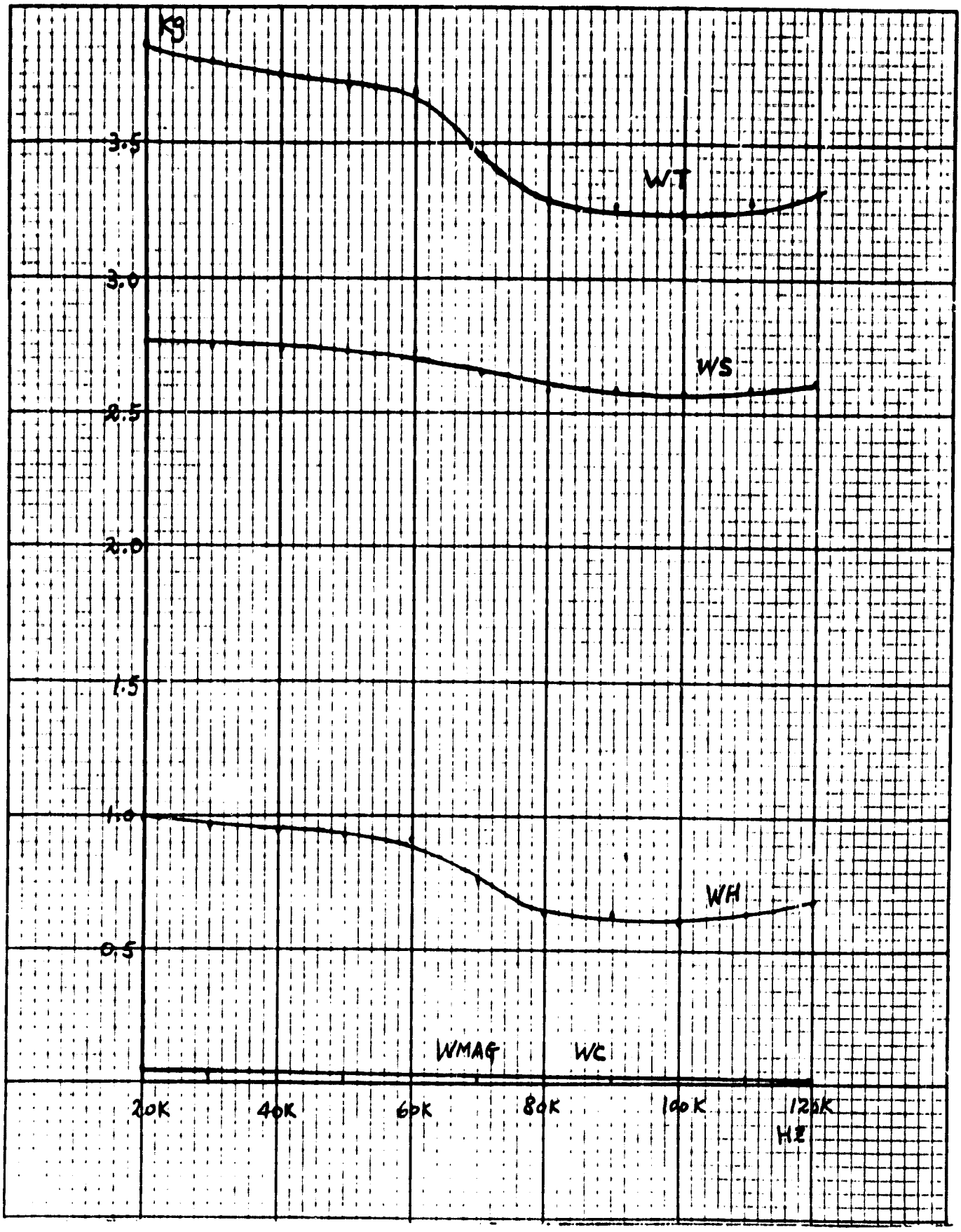

FIGURE 3.7.1 Weight Breakdowns for Buck-Boost Converter

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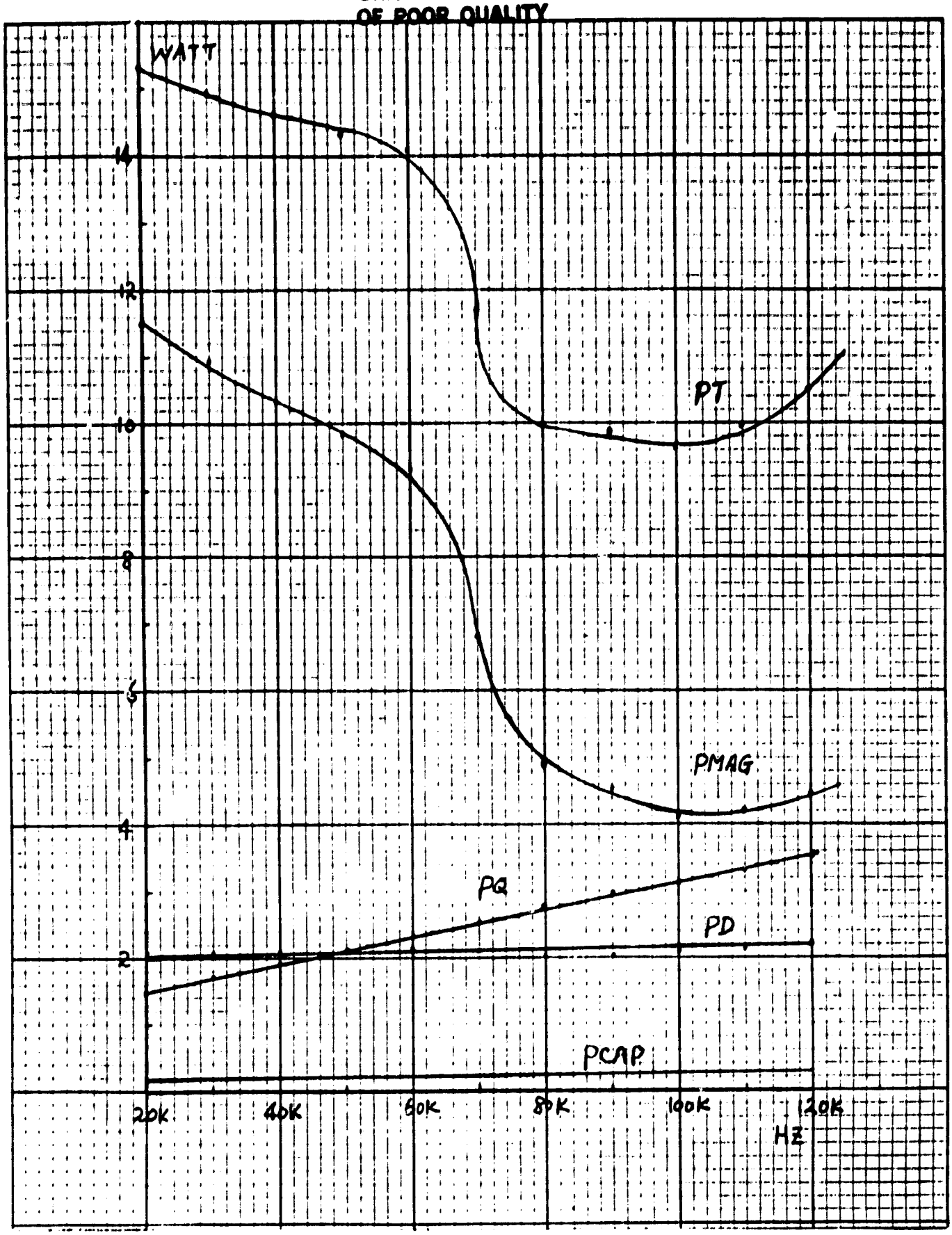


FIGURE 3.7.2 Loss Breakdowns for Buck-Boost Converter

3.8 CONCLUSIONS AND SUGGESTED FUTURE WORKS

3.8.1 Conclusions

Nonlinear programming techniques have been successfully employed to implement the minimum-weight design of switching power converters. Two different computational algorithms - ALAG and SUMT-based on the penalty function method were compared and their figure of mertis were assessed. For power converter optimization, the ALAG package was deemed more effective than its counterpart the SUMT package, when the computation time, ease of coding, and rate of convergence are concerned.

Adopting the ALAG rountine, a cost-effective computer-aided design approach is presented which provides a minimum-weight converter design down to the details of component level and concurrently meets all power-circuit performance requirements. This computer-aided design approach provides important design insights which helps to assess the following important design concerns:

(1) The trade-offs between weight and loss as the switching frequency is increased.

(2) The optimum converter design down to the details of component levels.

(3) The optimum component designs as a function of the switching frequency and their relationships to the overall system optimization.

(4) The significance of the U-shape curves representing total-weight/total-loss versus frequency as observed in the collected sub-optimization runs. This allows the designer to easily identify the optimum switching frequency or a range of frequencies over which the total weight/loss is minimum in the partical sense.

(5) Impact of various critical component characteristics, such as magnetic losses, switching losses of semiconductor devices, to the overall system.

(6) The optimal converter topology for a given application.

Employing the nonlinear-program based optimization technique, the power converter designer can conceive the overall optimum system design taking into consideration the power-circuit related performance requirements with the design objective of either minimizing weight, loss, or any other physical realizable quantity. It thus sets the stage for a more scientific design approach instead of subjective brute-force, trial-and-error, piecemeal design.

3.8.2 Suggested Future Works

The investigations of complex converter optimization problems using nonlinear programming techniques have shown marked success. Demonstration of the buck converter optimization in the previous modeling and analysis phases sponsored by NASA, the half-bridge converter optimization sponsored by NAVY, together with the boost and buck/boost converter optimization presented in this report have collectively provided clear evidence that a large scale converter optimization is feasible using NLP techniques; yet, the development of such a tool has not reached the stage of maturity where it can be widely used. Presently, it takes a person with considerable insight to the nonlinear programming algorithms, and with sufficient converter design experience, to make the program converge. It is our belief, however, that the afore-described NLP techniques could be made easier and more systematic than they are now. The following tasks are suggested as means for improving the NLP techniques to make them a more universal converter design tool with wide user applicability.

(1) Systematic way of improving initial starting point.

(2) Means of optimizing variable scalings and constraint scalings.

(3) Means of optimizing convergence stopping criteria.

(4) Improved method of formulating nonlinear constraints to enhance convergence.

(5) Establish conditions for convergence.

(6) Program transportability.

4.0 INVESTIGATION OF CURRENT-INJECTED MULTILOOP CONTROLLED SWITCHING REGULATORS.

4.1 INTRODUCTION

In recent years, vast amounts of interest and research in universities and industries have been directed toward development of a multi-loop, multi-state control scheme which could be applied to switching regulators. This collaborated effort has resulted in astonishing improvements of stability and dynamic performance of switching regulators.

A host of control schemes has emerged many of which employ the principle of current-injected control [17,18,19,20,21]. These control schemes share, the common property of transforming a switching converter from a voltage source into a current source. This control concept has exhibited many desirable properties such as inherent over-load protection, stable and equal load sharing when several power converter modules are in parallel, and f[illegible] system response.

Illustrated in Fig. 4.1.1 is a buck/boost converter employing current-injected control. The control is implemented by sensing the output voltage v_o of the converter and the instantaneous current ip through the power switch. The duty cycle signal is terminated when switching current ascends and intersects the threshold voltage v_x (dc error signal) determined by subtracting v_o from the reference voltage E_R. Since the switch current waveform sensed by the current transformer contains both the dc bias current component, and the small amplitude ac modulation signal (to be used for additional error compensation), the control thus provides inherent transistor peak-current protection (from the dc-current component) and improved dynamic performances (from the ac modulation signal).

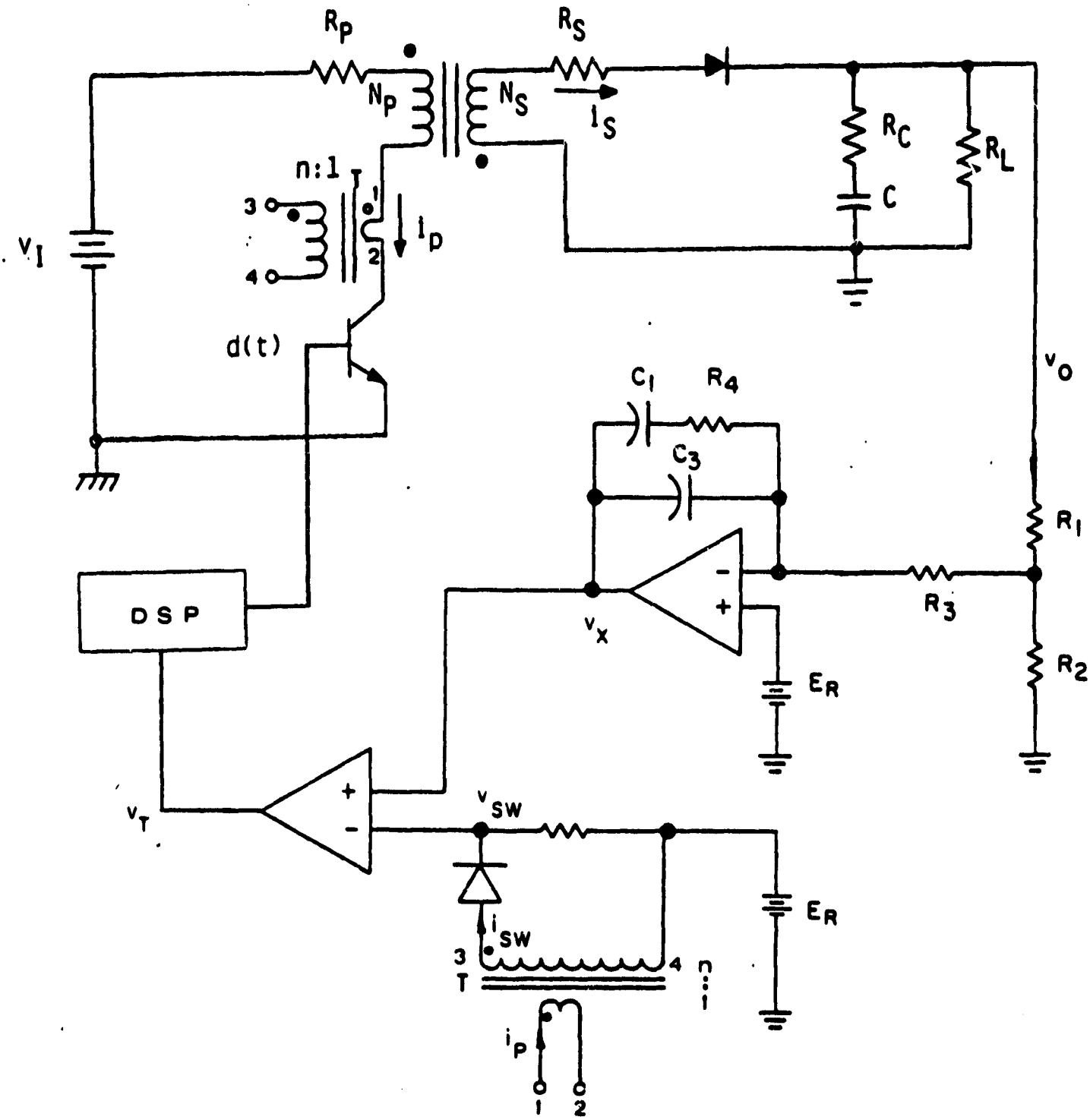


Fig. 4.1.1 CIRCUIT SCHEMATIC OF CURRENT-INJECT CONTROLLED BUCK/BOOST REGULATOR

Presented in this report is the modeling and analysis of the current-injected control system. The modeling approach employed in the present paper, a departure from previous efforts [17,20], provides additional insight to the current-injected control characteristics which failed to be manifested in the previous modeling and analysis efforts. To facilitate comparison between the method presented in this report and the approach employed in the earlier attempts, a brief review of the earlier work is provided. The concept of major loop and minor loop was employed in the previous works [17,20]. By considering the dc-feedback and compensation network being the major loop, and the ac-(switch current) feedback as being the minor loop, the minor loop was lumped into the power stage in the process of modeling. The multi-loop converter was thus reduced to a single loop system as shown in Fig. 4.1.2. The ac feedback loop which contains the switching current information is embedded in the "new" power stage. The transfer function of the new power stage $\hat{v}_o/\hat{v}_x$ has a surprisingly simple form (only a single pole and a single zero). The authors feel that while this modeling approach offers a way to examine certain small signal characteristics of the system, little information is provided regarding the relative stability of the system (the concept of the gain margin and the phase margin). Even though the dc loop can be opened, the ac loop is inherently closed in the "new" power stage model. A true open loop characteristic, where both the dc and the ac loop are opened, is thus not accessible in this modeling approach.

The modeling and analysis approach of the multi-loop current injected control presented in this report eliminates the aforementioned modeling dilemma. Following an approach similar to that described in the

author's previous work [22,23,24,25], the small signal model of the converter in Fig. 4.1.1 is derived as shown in Fig. 4.1.3. The small signal model has the following features:

(1) The power stage has three inputs and two outputs.

The three inputs are:

line disturbance $\hat{v}_i$

load disturbance $\hat{v}_o$

duty cycle disturbance $\hat{d}$

The two outputs are:

the output voltage $\hat{v}_o$

the switch current $\hat{i}_p$

(2) The error processor senses the two modulation signals $\hat{i}_o$ and $\hat{v}_o$. The transfer function F_{AC} represents the gain of the ac loop and F_{DC} represents the combined gain of the dc loop and the compensation network.

(3) The duty cycle modulator is represented by a describing function F_M.

Employing the above described small signal model one can readily examine the following performance characteristics:

(1) The control-to-output characteristics $\hat{v}_o/\hat{v}_x = F_M F_{D1}(\Delta + F_M F_{AC} F_{D2})$ where $\Delta = S^2 + 2\zeta W_o S + W_o^2$. (This is the characteristic examined in the previous papers [17,20] which exhibits a single-pole and and single-zero).

(2) The open dc loop characteristic

$G_{DL} = F_M F_{DC} F_{D1}/(\Delta + F_M F_{AC} F_{D2})$.

(3) The open loop characteristics (open both dc loop and ac loop)

$G_T = \frac{1}{\Delta} F_M (F_{DC} F_{D1} + F_{AC} F_{D2})$.

The open loop characteristic G_T is used to examine the relative

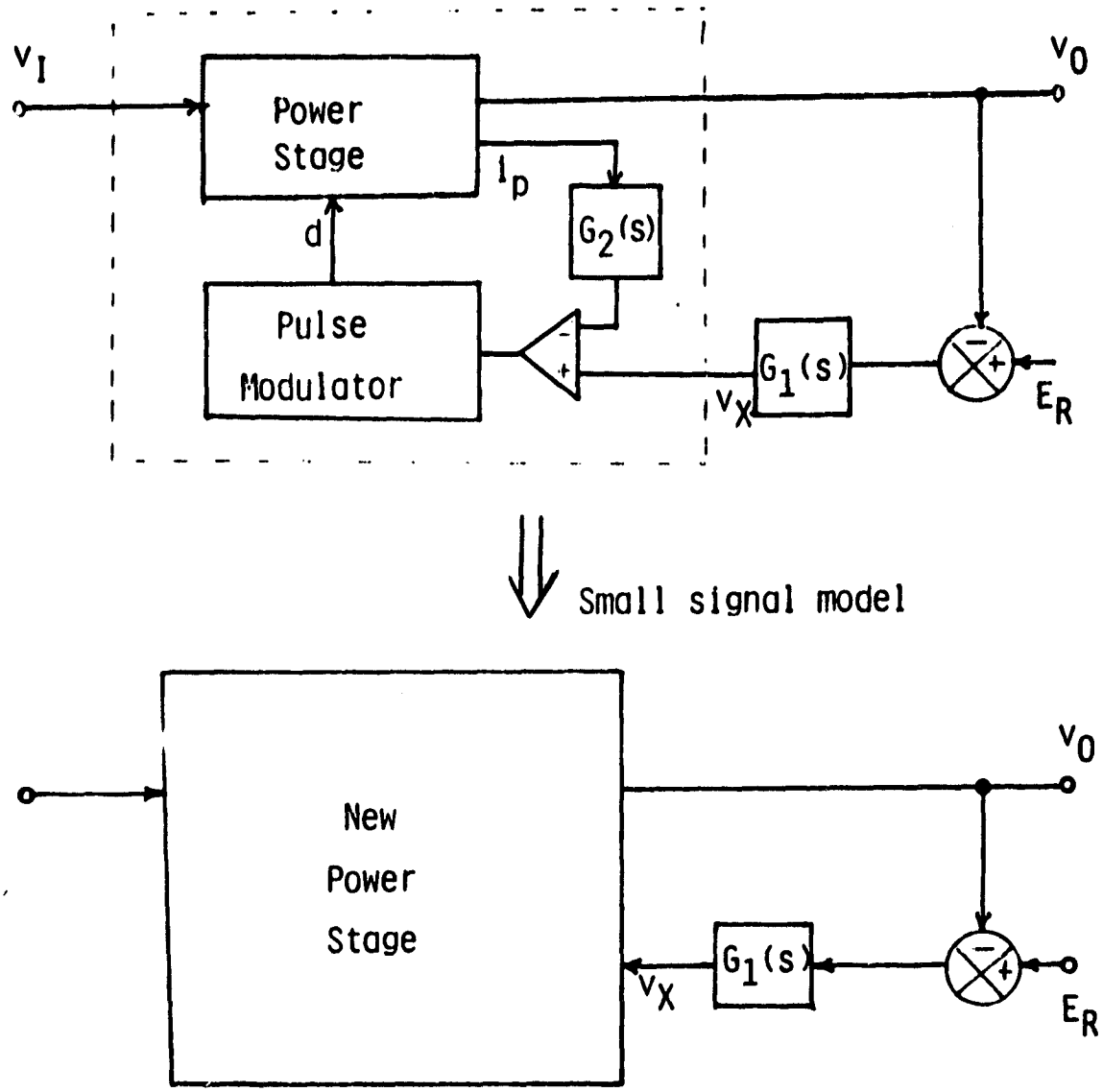


FIG. 4.1.2 Discussion of CALTECH Modeling Approach of Current-Injected Control

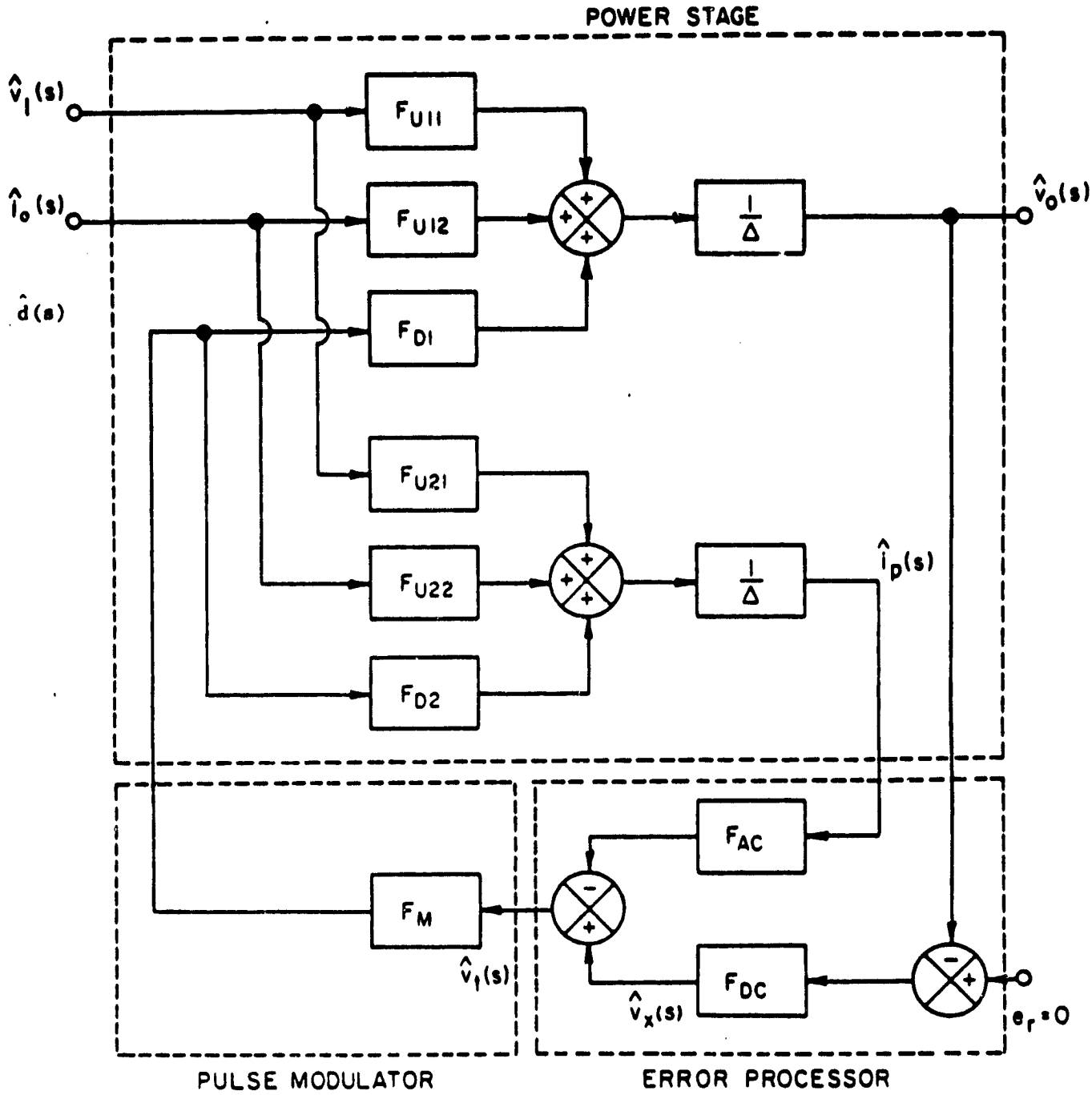


FIG. 4.1.3 Small Signal Model for the Current-Injected Control Buck/Boost Regulator

stability of the system.

(4) The audiosusceptibility characteristic $G_A = \hat{v}_o/\hat{v}_i$

$$G_A = \frac{1}{1 + G_T} \left\{ \frac{1}{\Delta^2} F_{U11}(\Delta + F_M F_{AC} F_{D2}) - F_{D1} F_M F_{AC} F_{U21} \right\}.$$

(5) The output impedance characteristic $Z_o = \hat{v}_o/\hat{i}_o$

$$Z_o = \frac{1}{1 + G_T} \left\{ \frac{1}{\Delta^2} F_{U12}(\Delta + F_M F_{AC} F_{D2}) - F_{U22} F_{AC} F_M F_{D1} \right\}.$$

Modeling of the power-stage, error processor, and pulse modulation is presented in chapters 4.2, 4.3, and 4.4, respectively. Various open and closed-loop performance characteristics are evaluated in chapters 4.5 and 4.6. Effects of dc-loop and ac-loop gain, and of compensation networks, are also discussed. Finally, guidelines for selecting control circuit parameters are provided.

4.2.0 CURRENT-INJECTED BUCK/BOOST POWER STAGE MODEL

4.2.1 Power Circuit Description

The function of the dc-dc converter is to process and transfer electric power from an unregulated input v_I to a regulated output v_0. The output voltage of the two-winding buck-boost converter shown in Fig. 4.2.1.1 can be either greater than or less than the input voltage, depending on the duty cycle of the switch and the turn ratio of the storage inductor. The magnetically-coupled windings, provided by the energy-storage inductor, allow input/output isolation and multiple outputs. Proper choice of the inductor's turn ratio also can alleviate the difficulty of implementing the extreme duty-cycle condition due to wide ranges of input and output voltages.

The energy exchange transpires in the power stage (Fig. 4.2.1.1(a)) in the following fashion. The state of the duty-cycle drive d(t), shown in Fig. 4.2.1.1.(b), determines the instantaneous position of the switch. The high-level of d(t) indicates the conduction, or on-state, and the low-level determines the off-time, or off-state, of the power switch. During T_{on}, a voltage approximately equal to $v_I(t)$ (neglecting the losses due to the parasitic resistance in the primary winding) is established across N_p which causes a current $i_p(t)$ to increase as illustrated in Figure 4.2.1.1.(c). Occurring simultaneously, a voltage $v_S(t)$ is induced across N_s by transformer action, but no conduction is allowed because of the reverse biased diode. As the off-time, T_{off} is initiated, the energy associated with N_p is transferred to N_s by an ampere-turn redistribution. As a result, the current $i_p(t)$ is reduced

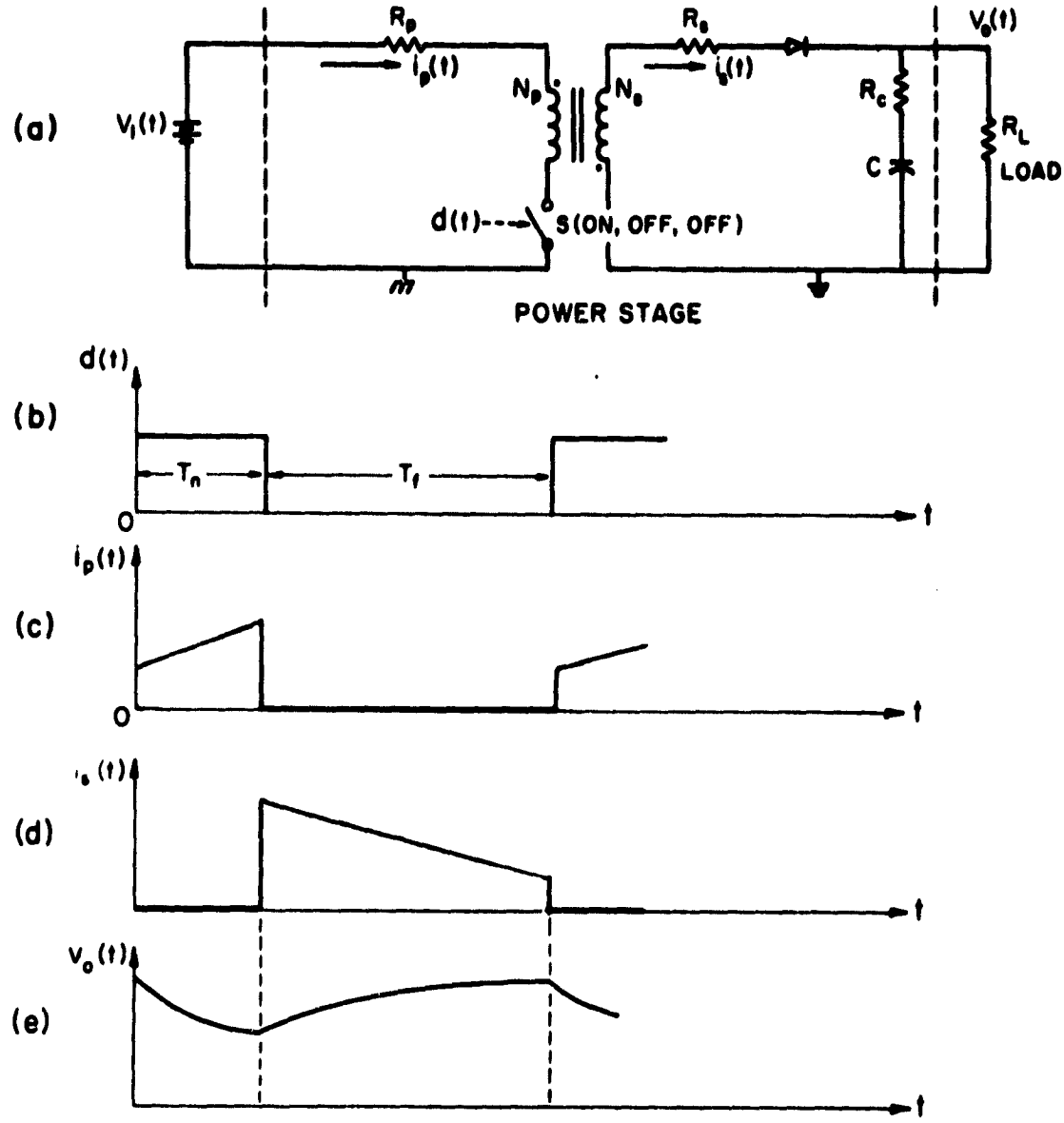


FIG. 4.2.1.1 Dc-dc two-winding buck-boost converter
(a) equivalent circuit, (b)-(e) waveforms

to zero and $i_S(t)$ is forced to a magnitude needed to maintain a continuous MMF flow through the inductor. The output voltage in Figure 4.2.1.1.(e) is kept nearly constant due to the large capacitive filter at the output which absorbs the pulsating current $i_S(t)$ and delivers a dc current with minimal ripple to the load.

4.2.2 Analytical Implementation

The switched dc-to-dc converter, assumed to be nondissipative, is nonlinear in nature. The basic dc-to-dc voltage conversion is achieved by repetitive switching between a number of linear networks switches and diodes. The number of linear networks in one switching cycle is determined by the mode of operation of the inductor's magnetomotive force, MMF. If the MMF is continuous as shown in Fig. 4.2.2.1.(a), the power stage model has two linear networks corresponding to a mode 1 type operation. For a discontinuous inductor MMF operation as shown in Figure 4.2.2.1.(b) the power stage model is composed of three linear networks corresponding to a mode 2 type operation.

Each linear circuit model is described by a set of linear state-space equations. For the current-injected buck-boost power stage the state variables (independent variables) are customarily the magnetic flux, ϕ, and the capacitor voltage, v_C. The total number of storage elements determines the order of the system.

4.2.2.1 State Space Averaging Technique

To derive a linear model for the power stage, the averaging technique is used.[27] Employing the mode 1 operation as an example, the

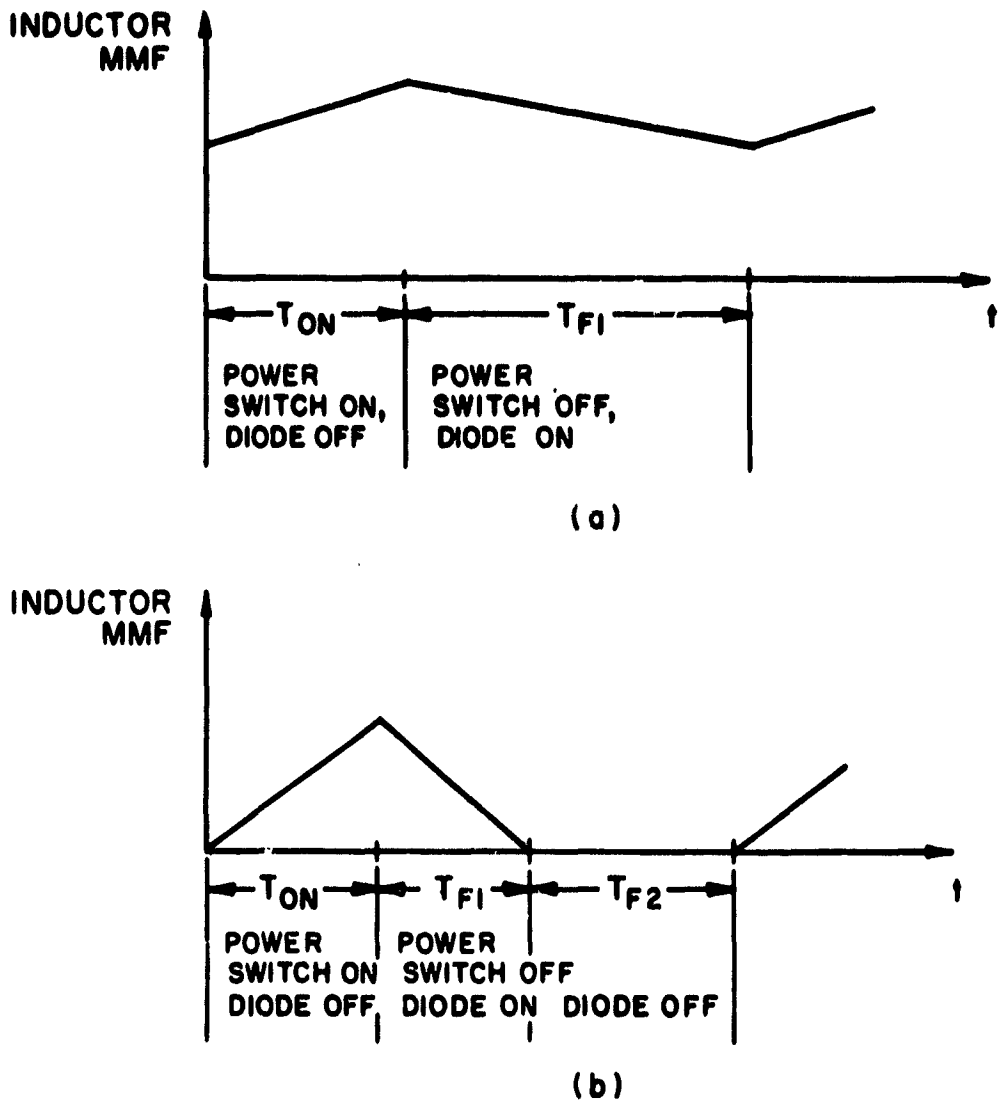


Fig. 4.2.2.1 Inductor magneto-motive force.

power stage is modelled by two intervals of operation, T_{on} and T_{F1}, respectively.

(i) interval T_{on}

$$\dot{\underline{x}} = A_1\underline{x} + B_1\underline{u}$$
$$\underline{y} = c_1\underline{x} + E_1\underline{u}$$

(ii) interval T_{F1}

$$\dot{\underline{x}} = A_2\underline{x} + B_2\underline{u} \qquad (4.2.2.1)$$
$$\underline{y} = C_2\underline{x} + E_2\underline{u}$$

The principal of the average method is to replace the state-space description of the two linear circuits by a single state-space description which represents the approximate behavior of the system through one cycle of operation. Taking the average of both intervals and summing the results yields the following linear time-varying continuous system:

$$\dot{\underline{x}} = d(A_1\underline{x} + B_1\underline{u}) + d'(A_2\underline{x} + B_2\underline{u}) \qquad (4.2.2.2)$$
$$\underline{y} = d(C_1\underline{x} + E_1\underline{u}) + d'(C_2\underline{x} + E_2\underline{u})$$
$$d = \frac{T_{on}}{T_p} \qquad d' = \frac{T_{F1}}{T_p}$$

where T_p is the period of the switching cycle.

The basic requirement for the average method is that the effective filter corner frequency of the switching converter be much lower than the switching frequency [27].

The linear time-varying equations (4.2.2.2) can be rewritten in the following form:

$$\dot{\underline{x}} = A\underline{x} + B\underline{u} \qquad (4.2.2.3)$$
$$\underline{y} = C\underline{x} + E\underline{u}$$

where $A = dA_1 + d'A_2$ (4.2.2.4)

$$B = dB_1 + d'B_2$$
$$C = dC_1 + d'C_2$$
$$E = dE_1 + d'E_2$$

4.2.2.2. Perturbation

To study the small-signal behavior, the linear time-varying equations (4.2.2.3) are perturbed. The introduction of input variations and duty-cycle variations in turn perturb the output and state vectors. The perturbed input vectors are:

$$u = \underline{U} + \hat{\underline{u}} \qquad \text{and} \qquad d = D + \hat{d} \qquad (4.2.2.5)$$

where U and D are the steady-state values and $\hat{u}$ and $\hat{d}$ are small perturbations. These perturbations in turn lead to following:

$$\underline{x} = \underline{X} + \hat{\underline{x}} \qquad \text{and} \qquad \underline{y} = \underline{Y} + \hat{\underline{y}}$$

where $\underline{X} + \underline{Y}$ are the steady-state values and $\hat{x}$ and $\hat{y}$ are small perturbations. With the corresponding perturbations substituted into equation (4.2.2.3) the basic model becomes:

$$\dot{\hat{\underline{x}}} = \underbrace{A\underline{X} + B\underline{U}}_{\text{(dc term)}} + \underbrace{A\hat{\underline{x}} + B\hat{\underline{u}}}_{\text{(line variation)}} + \underbrace{[(A_1 - A_2)\underline{X} + (B_1 - B_2)\underline{U}]\hat{d}}_{\text{(duty ratio variation)}} \qquad (4.2.2.7)$$

$$+ \underbrace{[(A_1 - A_2)\hat{\underline{x}} + (B_1 - B_2)\hat{\underline{u}}]\hat{d}}_{\text{(nonlinear second order)}}$$

$$\underline{Y} + \hat{\underline{y}} = \underbrace{C\underline{X} + E\underline{U}}_{\text{(dc term)}} + \underbrace{C\hat{\underline{x}} + E\hat{\underline{u}}}_{\text{(line variation)}} + \underbrace{[(C_1 - C_2)\underline{X} + (E_1 - E_2)\underline{U}]\hat{d}}_{\text{(dute ratio variation)}} \qquad (4.2.2.8)$$

$$+ \underbrace{[(C_1 - C_2)\hat{\underline{x}} + (E_1 - E_2)\hat{\underline{u}}]\hat{d}}_{\text{(nonlinear second order)}}$$

The perturbed state-space description is nonlinear owing to the presence of the product of time-dependent quantities $\hat{\underline{x}}$ and $\hat{u}$ with $\hat{d}$.

4.2.2.3. Linearization

Since the ac variations are very small in magnitude compared to their steady-state value, the following small-signal approximations can be made:

$$\frac{\hat{u}_1}{U_1}, \frac{\hat{u}_2}{U_2} << 1; \frac{\hat{d}}{D} << 1; \frac{\hat{x}_1}{X_1}, \frac{\hat{x}_2}{X_2} << 1; \frac{\hat{y}_1}{Y_1}, \frac{\hat{y}_2}{Y_2} << 1 \qquad (4.2.2.9)$$

where $\underline{\hat{u}} = (\hat{u}_1, \hat{U}_2)$, $\underline{V} = (U_1, U_2)$, $\underline{\hat{x}} = (\hat{x}_1, \hat{x}_2)$, e

Using the approximations (4.2.2.9), the nonlinear second order terms in equations (4.2.2.7) and (4.2.2.8) can be neglected, resulting in a linear system. Separating the steady-state (dc) and dynamic (ac) parts of the linearized system, the final state-space model is acquired.

Steady-state (dc) model:

$$\underline{X} = - A^{-1}B\underline{U} \qquad (4.2.2.10)$$

$$\underline{Y} = C\underline{X} + E\underline{U} \qquad (4.2.2.11)$$

$$= (E - CA^{-1}B)\underline{U}$$

Linear Dynamic (ac) model:

$$\dot{\underline{\hat{x}}} = A\underline{\hat{x}} + B\underline{\hat{u}} + [(A_1 - A_2)\underline{X} + (B_1 - B_2)\underline{U}]\hat{d} \qquad (4.2.2.12)$$

$$\underline{\hat{y}} = C\underline{\hat{x}} + E\underline{\hat{u}} + [(C_1 - C_2)\underline{X} + (E_1 - E_2)\underline{U}]\hat{d} \qquad (4.2.2.13)$$

4.2.2.4. Transfer Function Representations

In small-signal analysis, particular input/output relations (transfer functions) are needed to construct the basic building blocks necessary to fully describe the power stage model. To find the input-to-state variable $\underline{\hat{x}}$ and input-to-output transfer functions, one assumes the ac duty-ratio variation is zero. The dynamic model described in equations (4.2.2.12) and (4.2.2.13) can be simplified as follows:

$$\dot{\underline{\hat{x}}} = A\underline{\hat{x}} + b\underline{\hat{u}}$$

$$\underline{\hat{y}} = C\underline{\hat{x}} + D\underline{\hat{u}}$$

Taking the Laplace transformation of the previous equations, the following relations are obtained:

$$s\hat{\underline{x}}(s) - \hat{\underline{X}}(o) = A\hat{\underline{x}}(s) + B\hat{\underline{u}}(s)$$

And

$$\hat{\underline{y}}(s) = C[s\underline{I} - A]^{-1}B\hat{\underline{u}}(s) + D\hat{\underline{u}}(s)$$

$$= [C[s\underline{I} - A]^{-1}B + D]\hat{\underline{u}}(s) \qquad (2.2.14)$$

Leting $\hat{\underline{x}}(o) = o$, the first equation becomes $\hat{\underline{x}}(s) = [s\underline{I} - A]^{-1}B\hat{\underline{u}}(s)$.

To find the duty cycle-to-state variable $\hat{x}$ and duty cycle-to-output transfer functions, one assumes the ac variation of $\underline{u}$ is zero. Equations (4.2.2.12) and (4.2.2.13) yield the following:

$$\dot{\hat{\underline{x}}} = A\hat{\underline{x}} + [(A_1 - A_2)\underline{X} + (B_1 - B_2)\underline{U}]\hat{d} \qquad 2.2.15)$$

$$\hat{\underline{y}} = C\hat{\underline{x}} + [(C_1 - C_2)\underline{X} + (E_1 - E_2)\underline{U}]\hat{d} \qquad (4.2.2.16)$$

And the resulting duty ratio modulation $\hat{d}$ to state-variable $\hat{\underline{x}}$ and duty ratio modulation $\hat{d}$ to output $\hat{\underline{y}}$ transfer functions are:

$$\frac{\hat{\underline{x}}(s)}{\hat{d}(s)} = (SI - A)^{-1}\,[(A_1 - A_2)\underline{X} + (B_1 - B_2)\underline{U}] \qquad (4.2.2.17)$$

$$\frac{\hat{\underline{y}}(s)}{\hat{d}(s)} = C(SI - A)^{-1}\,[(A_1 - A_2)\underline{X} + (B_1 - B_2)\underline{U}] + [(C_1 - C_2)\underline{X} + (E_1 - E_2)\underline{U}] \qquad (4.2.2.18)$$

These transfer functions will be used as building blocks to construct the power stage transfer functions to be presented in the following sections.

4.2.3 Power Stage Analytical Model

The objective of the power stage model is to develop a group of transfer functions that describe the low-frequency behavior of the switching circuit. The model developed is comprised of three inputs and two outputs. From Fig. 4.2.3.1 the three inputs are the supply

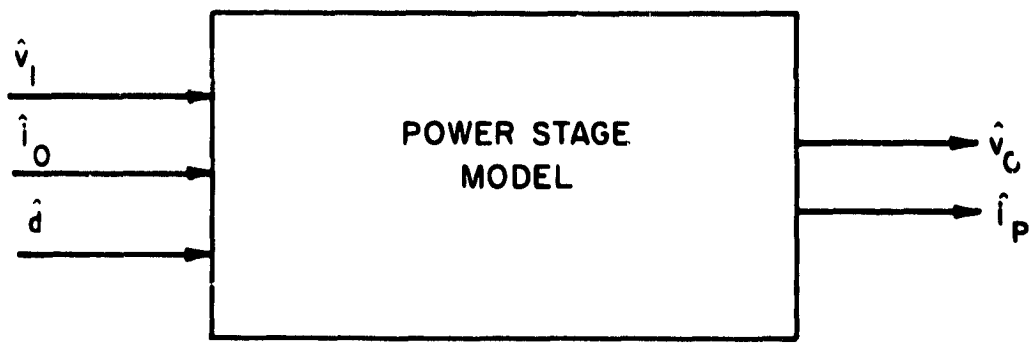


Fig. 4.2.3.1 Power stage input/output relationship.

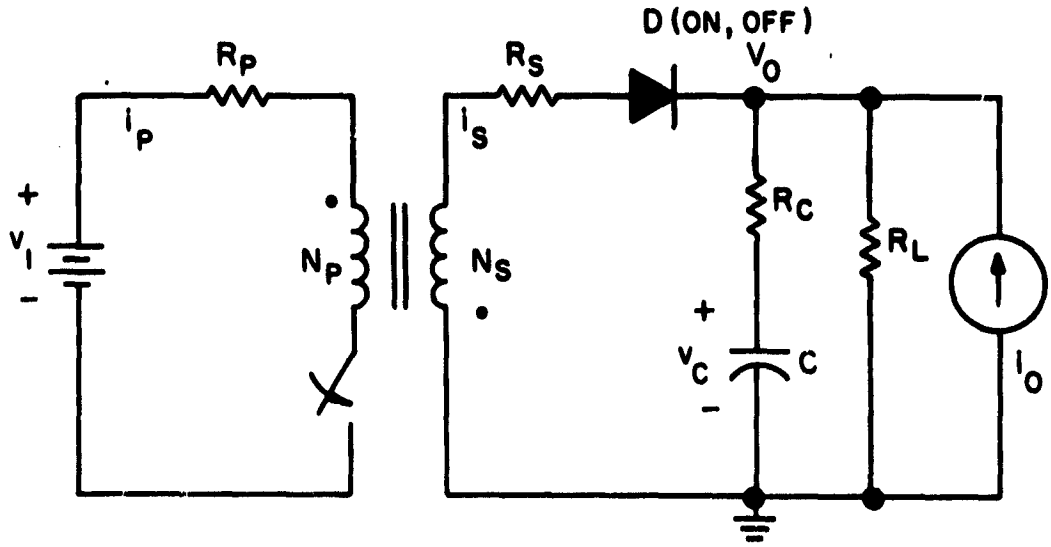
voltage $\hat{v}_i$, the output current $\hat{i}_o$, and the duty ratio $\hat{d}$. The two outputs supplied are the output voltage $\hat{v}_o$, and the switching current $\hat{i}_p$.

The two-winding buck/boost power stage is shown in Figure 4.2.3.2(a). The two linear equivalent circuit models for the continuous MMF case are illustrated in Fig. 4.2.3.2(b) and (c). The power stage model contains an ideal switch and a diode. The storage inductor is a linear core circumscribed by a primary and a secondary winding with inductances L_p and L_S respectively, where $L_p = (N_p/N_s)^2 L_s$. Also described by the model is the winding resistances R_p and R_s/ The output filter is represented by a capacitance and an equivalent series resistance, ESR. On the output a current source $\hat{i}_o$ is employed to represent a disturbance injected to the converter from the load.

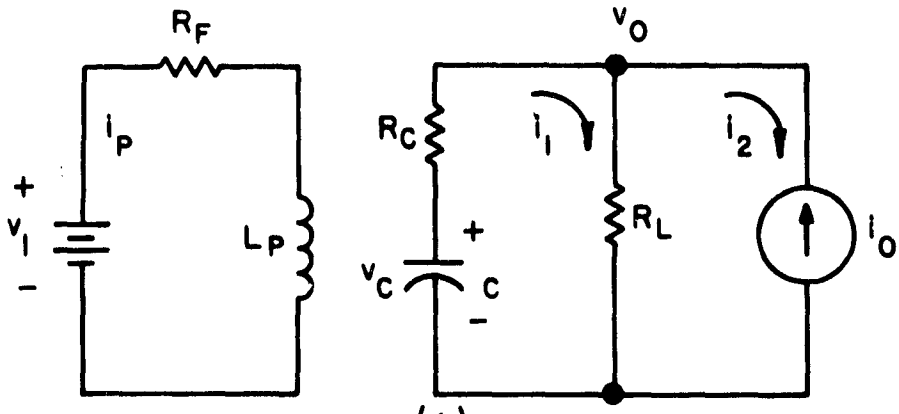
The power stage model is composed of two independent variables. The state variables for both linear circuit equivalents are the magnetic flux ϕ of the core shared by the primary and secondary windings N_p and N_s, and the capacitor voltage v_c. During the interval T_{on}, the power stage is described by the following:

$$\dot{\underline{x}} = A_1\underline{x} + B_1\underline{u} \qquad \underline{y} = C_1\underline{x} + E_1\underline{u} \tag{4.2.3.1}$$

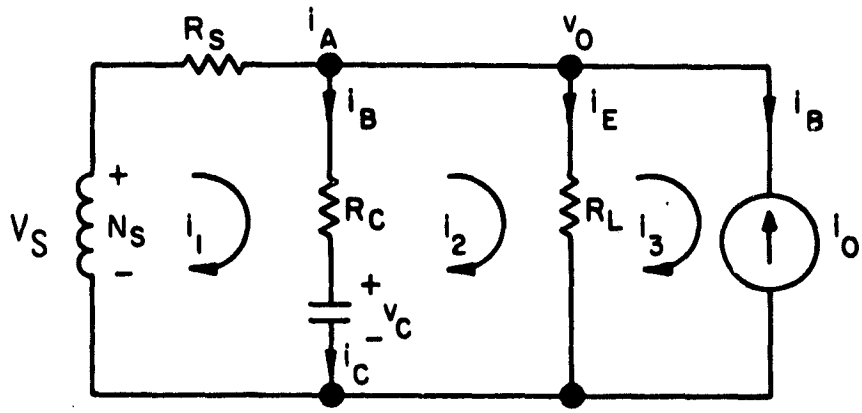
$$\text{where, } \underline{x} = \begin{bmatrix} \phi \\ v_C \end{bmatrix}, \quad \underline{u} = \begin{bmatrix} v_I \\ i_O \end{bmatrix}, \quad \underline{y} = \begin{bmatrix} v_O \\ i_p \end{bmatrix}$$



(a)



(b)



(c)

Fig. 4.2.3.2 (a) Two-winding buck/boost
(b) Equivalent circuit model during T_{ON}
(c) Equivalent circuit model during T_{OFF}

$$A_1 = \begin{bmatrix} -\frac{R_P}{L_P} & 0 \\ 0 & -\frac{1}{(R_C+R_L)C} \end{bmatrix} \qquad B_1 = \begin{bmatrix} \frac{1}{N_P} & 0 \\ 0 & -\frac{R_L}{(R_C+R_L)C} \end{bmatrix}$$

$$C_1 = \begin{bmatrix} 0 & \frac{R_L}{R_C+R_L} \\ \frac{N_P}{L_P} & 0 \end{bmatrix} \qquad D_1 = \begin{bmatrix} 0 & R_C//R_L \\ 0 & 0 \end{bmatrix}$$

For the interval T_{F1} the power stage takes the following form

$$\dot{\underline{x}} = A_2\underline{x} + B_2\underline{u} \qquad \underline{y} = C_2\underline{x} + E_2\underline{u} \qquad (4.2.3.2)$$

where,

$$A_2 = \begin{bmatrix} -\left(\frac{R_S + R_C // R_L}{L_S}\right) & -\frac{R_L}{R_C+R_L} \cdot \frac{1}{N_S} \\ \frac{R_L}{R_C+R_L} \cdot \frac{N_S}{L_S C} & \frac{-1}{R_C+R_L} \cdot \frac{1}{C} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} 0 & -R_C//R_L \cdot \frac{1}{N_S} \\ 0 & \frac{R_L}{R_C+R_L} \cdot \frac{1}{C} \end{bmatrix}$$

$$C_2 = \begin{bmatrix} R_c//R_L \cdot \frac{N_S}{L_S} & \frac{R_L}{R_C+R_L} \\ 0 & 0 \end{bmatrix} \qquad D_2 = \begin{bmatrix} 0 & R_C//R_L \\ 0 & 0 \end{bmatrix}$$

Appedix A gives the derivation of the two equivalent linear models used to describe the power stage during T_{on} and T_{F1}.

4.2.3.1 <u>Average Model</u>.

Continuing the process of characterizing the small-signal model needed to describe the dynamic, ac behavior of the power stage, the average model is:

$$\dot{\underline{x}} = A\underline{x} + B\underline{u} \qquad \underline{y} = C\underline{x} + E\underline{u} \tag{4.2.3.3}$$

$$A = \begin{bmatrix} \dfrac{-DR_P}{L_P} - D'\left(\dfrac{R_S + R_C//R_L}{L_s}\right) & \dfrac{-D'(R_C//R_L)}{N_S R_C} \\ \dfrac{D'(R_C//R_L)}{R_C L_S C} & \dfrac{-D}{(R_C + R_L)C} - \dfrac{D'}{(R_C + R_L)C} \end{bmatrix}$$

$$B = \begin{bmatrix} \dfrac{D}{N_P} & \dfrac{-D'}{N_S}(R_C//R_L) \\ 0 & \dfrac{D(R_C//R_L)}{R_C C} + \dfrac{D(R_C//R_L)}{R_C C} \end{bmatrix}$$

$$C = \begin{bmatrix} \dfrac{D'N_S(R_C//R_L)}{L_S} & \dfrac{D(R_C//R_L)}{R_C} + \dfrac{D'(R_C//R_L)}{R_C} \\ \dfrac{DN_P}{L_P} & 0 \end{bmatrix}$$

$$E = \begin{bmatrix} 0 & (D + D')\ R_C//R_L \\ 0 & 0 \end{bmatrix}$$

where D is the steady-state duty ratio and $D' = 1 - D$.

To simplify our matrix expressions, assume:

(i) $R_C << R_L$ so that $R_C//R_L \approx R_C$

$R_C + R_L \approx R_L$

(ii) $\dfrac{R_P}{L_P} = \dfrac{R_S}{L_S}$

Also by definition the following conditions are used:

(i) $L_e \triangleq \dfrac{L_S}{D'^2}$ (ii) $R_e \triangleq \dfrac{R_S}{D'^2}$

(iii) $\omega_o^2 \triangleq \dfrac{1}{L_e C}$ $\zeta \triangleq \dfrac{\omega_o}{2} \left[\dfrac{L_e}{R_L} + \left(R_e + \dfrac{R_C}{D'}\right)C\right]$

(iv) $D \triangleq \dfrac{T_{on}}{T_P}$ and $D' \triangleq \dfrac{T_{F1}}{T_P}$ where T_P is the switching period,

so that $D + D' = \dfrac{T_{on} + T_{F1}}{T_P} = \dfrac{T_P}{T_P} = 1$

Applying these simplifications the average model becomes:

$$A = \begin{bmatrix} \dfrac{-R_S - D'R_C}{L_e(D')^2} & -\dfrac{D'}{N_S} \\ \dfrac{N_S\omega_o^2}{D'} & \dfrac{-1}{R_L C} \end{bmatrix} \qquad B = \begin{bmatrix} \dfrac{D}{N_P} & \dfrac{-D'R_C}{N_S} \\ 0 & 1/C \end{bmatrix}$$

(4.2.3.4)

$$C = \begin{bmatrix} \dfrac{N_S R_C}{L_e D'} & 1 \\ \dfrac{DN_p}{L_p} & 0 \end{bmatrix} \qquad E = \begin{bmatrix} 0 & R_C \\ 0 & 0 \end{bmatrix}$$

4.2.3.2. Linearized Power Stage Model

Line voltage variation $\hat{v}_i$, duty cycle variations $\hat{d}$, and output current source disturbances $\hat{i}_o$, are now introduced into the circuit such that

$$v_I \triangleq V_I + \hat{v}_i \qquad d \triangleq D + \hat{d}$$
$$i_0 \triangleq 0 + \hat{i}_o \qquad d' \triangleq D' - \hat{d} \tag{4.2.3.5}$$

where V_I is the dc input voltage and D and D' is the steady-state on-time and off-time duty ratios. Employing the small-signal approximation as discussed in Section 4.2.2.2, the second-order nonlinear term may be neglected and a linear system obtained.

4.2.3.2.(a) Steady-state (dc) model.

Using method of section 4.2.2.3, the steady state output vector $\underline{Y}$ may be seen to be:

$$\underline{Y} = \begin{bmatrix} V_0 \\ I_p \end{bmatrix} = (E - CA^{-1}B)\underline{U}$$
$$= \begin{bmatrix} \dfrac{DN_S}{D'N_P} \\ \dfrac{D^2 L_e}{L_P R_L} \end{bmatrix} V_I \tag{4.2.3.6}$$

4.2.3.2(b) The Input-to-output transfer function.

The input-to-output transfer function due to an input variation $\hat{\underline{u}}$ assuming the duty ratio $\hat{d}$ (ac) variation is zero is as follows:

$$\hat{\underline{y}}(s) = \begin{bmatrix} \hat{v}_o(s) \\ \hat{i}_p(s) \end{bmatrix} = [C[SI-A]^{-1}B + E]\hat{\underline{u}}(s)$$

$$= \frac{\begin{bmatrix} \frac{N_s}{N_p}\frac{D}{D'}\omega_o^2\left(R_C Cs+1\right) & R_C\left(S^2 + z_1 S + \omega_o z_2\right) \\ \frac{D^2}{L_p}\left(S + \frac{1}{R_L C}\right) & \frac{-DD'N_p}{L_p N_S C}\left(R_C Cs + 1\right) \end{bmatrix}\begin{bmatrix} \hat{v}_i \\ \hat{i}_o \end{bmatrix}}{S^2 + 2\zeta\omega_o S + \omega_o^2} \qquad (4.2.3.7)$$

where $z_1 = 2\zeta\omega_o + \frac{1}{R_C C} - \frac{R_C}{L_e}$, $z_2 = \frac{R_e}{R_L} + \frac{D}{D'}$

4.2.3.2(c) Duty cycle-to-output transfer function

The duty cycle-to-output transfer function assuming $\hat{u} = 0$ is:

$$\frac{\underline{y}(s)}{d(s)} = \begin{bmatrix} \frac{\hat{v}_o(s)}{\hat{d}(s)} \\ \frac{\hat{i}_p(s)}{\hat{d}(s)} \end{bmatrix} = C(SI-A)^{-1}\,[(A_1 - A_2)X + (B_1 - B_2)U] + [(C_1 - C_2)\underline{X} + (E_1 - E_2)\underline{U}]$$

$$\frac{\hat{y}(s)}{\hat{d}(s)} = \begin{bmatrix} \dfrac{\omega_o^2 V_0}{DD'} \cdot \dfrac{(R_C C_S + 1)}{(S^2 + 2\zeta\omega_o S + \omega_o^2)} \left(1 - \dfrac{D}{R_L}\left(\dfrac{S}{\omega_o^2 C} + R_e + \dfrac{R_C}{D'}\right)\right) \\ \dfrac{V_0 N_S}{R_L N_P}\left(\dfrac{(R_L CS + D + 1)}{L_S C\,(S^2 + 2\zeta\omega_o S + \omega_o^2)} + \dfrac{1}{D'}\right) \end{bmatrix}$$

(4.2.3.8)

For detailed derivations of the transfer functions, refer to Appendix I.

Further simplifcations are made by letting $\Delta = S^2 + 2\zeta\omega_o S + \omega_o^2$ and then forming gain expressions. The gain blocks in matrix form due to a variation $\hat{\underline{u}} = [\hat{v}_i \quad \hat{i}_0]^T$ (4.2.3.7) results in the following:

$$\hat{\underline{y}}(s) \triangleq \frac{1}{\Delta}\begin{bmatrix} F_{u11} & F_{u12} \\ F_{u21} & F_{u22} \end{bmatrix}\begin{bmatrix} \hat{v}_i \\ \hat{i}_o \end{bmatrix} \qquad (4.2.3.9)$$

$$= \frac{1}{\Delta}\begin{bmatrix} \dfrac{N_s}{N_P}\,\dfrac{D}{D'}\,\omega_o^2\,(R_C CS + 1) & R_C\left[S^2 + z_1 S + \omega_o^2 z_2\right] \\ \dfrac{D^2}{L_P R_L C}\,(R_L CS + 1) & \dfrac{-DN_S\omega_o^2}{D'N_P}\,(R_C CS + 1) \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_i \\ \hat{i}_o \end{bmatrix} \qquad (4.2.3.10)$$

From the duty cycle-to-output transfer function (4.2.3.8), the matrix simplification yields the following:

$$\hat{\underline{y}}(s) = \begin{bmatrix} \hat{v}_o \\ \hat{i}_p \end{bmatrix} \triangleq \frac{1}{\Delta} \begin{bmatrix} F_{D1} \\ F_{D2} \end{bmatrix} \hat{d}(s) \qquad (4.2.3.11)$$

$$= \frac{1}{\Delta} \begin{bmatrix} \omega_o^2 \frac{V_O}{DD'} (R_C Cs + 1) \left(1 - \frac{D}{R_L} \left(\frac{S}{\omega_o^2 C} + R_e + \frac{R_C}{D'} \right) \right) \\ \frac{V_O N_S}{R_L N_P} \left(\frac{(R_L CS + D + 1)}{L_S C} + \frac{\Delta}{D'} \right) \end{bmatrix} \hat{d}(s)$$

(4.2.3.12)

The block diagram for the small-signal approximation of the power stage is shown in Fig. 4.2.3.3. The analytical expressions for the F_{u--} and F_{D-} functions are given in equations (4.2.3.10) and (4.2.3.12).

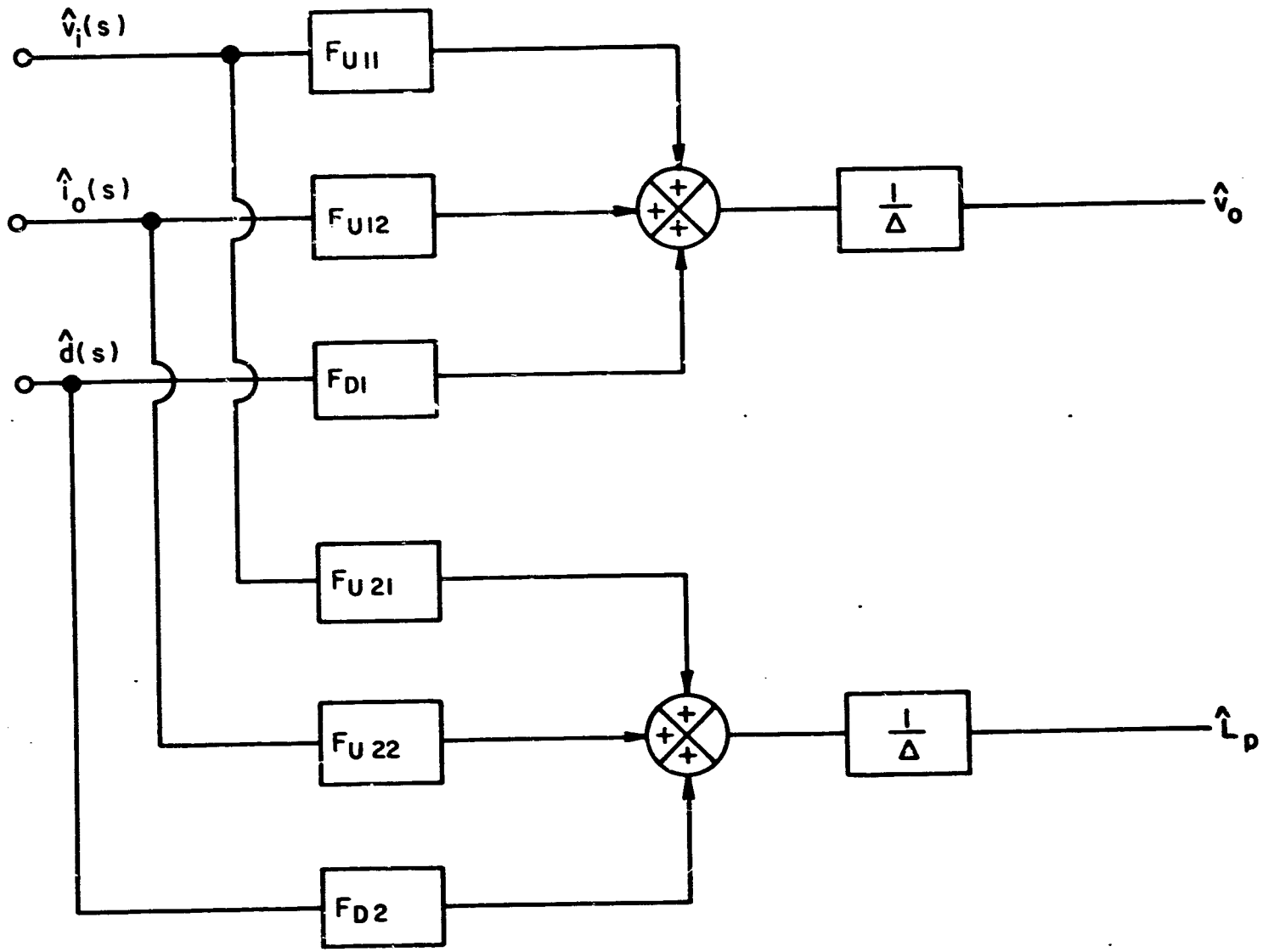


Fig. 4.2.3.3. Small signal averaged power stage block diagram.

4.3.0 ERROR PROCESSOR MODEL

4.3.1 Introduction

The error processor, EP, is a feedback compensation network, It processes multiple-input control signals derived from the power stage, and delivers the required analog information to the pulse modulator. Fig. 4.3.1.1. illustrates the analog-signal error processor employed in the present analysis. From a small-signal viewpoint, the EP is a linear network consisting of two control loops. The signals sensed in these two loops are the converter output-voltage v_o, and the primary switching-current i_p.

The loop sensing v_0 is the same as any conventional dc loop, where the sensed v_0 is processed by an amplifier with reference voltage E_R, to generate a dc error signal v_X. The dc error voltage after processing through an integral plus lead-lag compensation network establishes as the threshold level for the switching-current information derived from the ac loop.

The integral plus lead-lag compensation network is employed to shape the frequency response to improve the converter stability and dynamic response.

The ac loop which senses the collector current of the power transistor serves two functions. The first function is to transform the primary switching-current into a proportional voltage signal. This voltage signal v_{SW} is then compared with v_X resulting in a control that turns off the power switch when $v_{SW} = v_X$. The second function of the ac loop is to derive the low-frequency modulation signal or error signal for additional loop compensation.

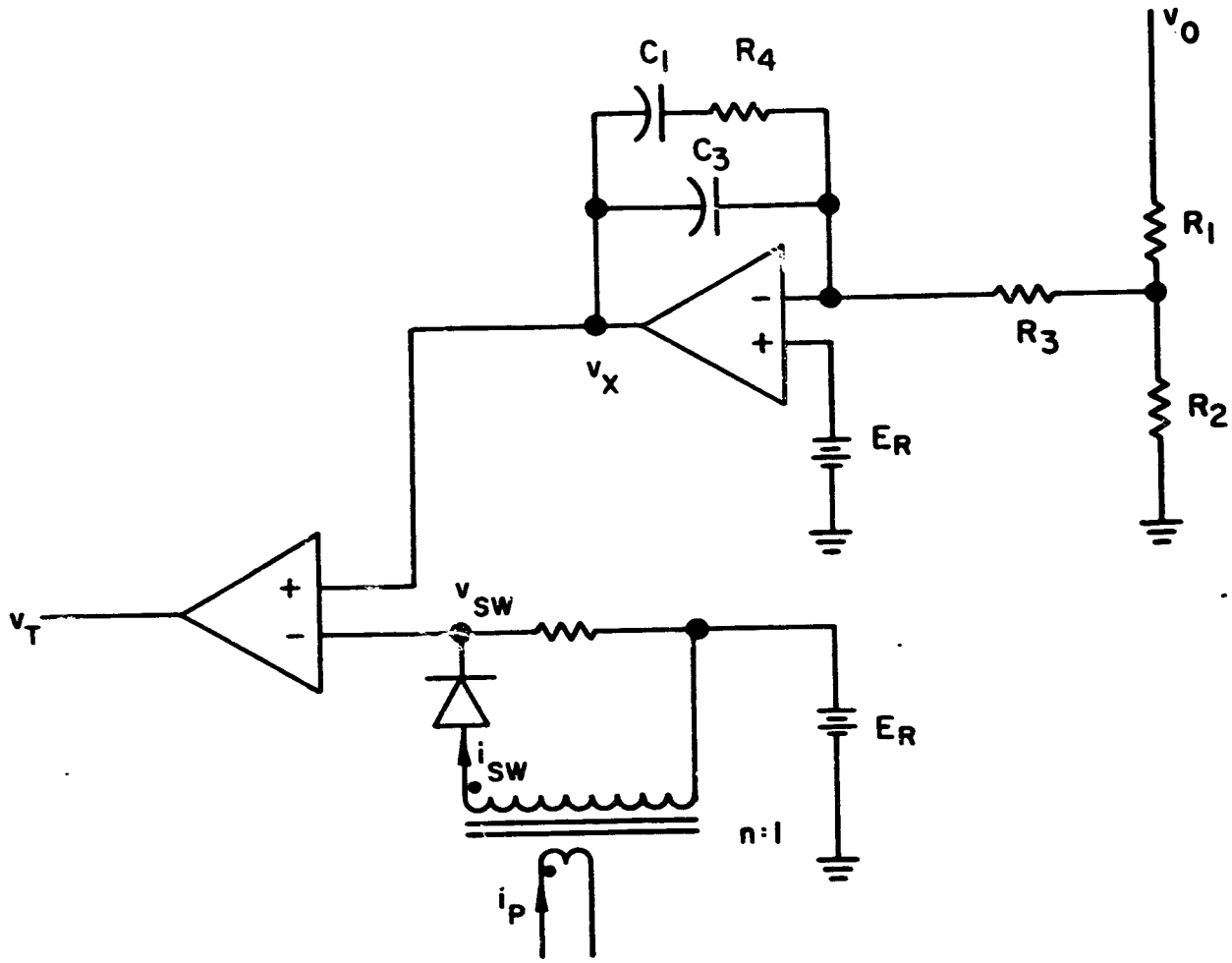


Fig. 4.3.1.1. Error processor.

4.3.2 Error Processor Ac and Dc Loop Gains

Fig. 4.3.2.1 is a functional equivalent of the circuit shown in Fig. 4.3.1.1. In Fig. 4.3.2.1. the two error signals, namely v_X and V_{SW} are subtracted to form the positive input to the threshold detector. The negative input of the error processor is now replaced by a zero reference.

The authors feel that the modified error processor better serves to perceive the modeling effect for the following reasons:

(1) As stated earlier, the ac loop contains two types of information: The large amplitude switching-current waveform is used to implement the analog-to-digital conversion. Such a function is considered part of the pulse modulator instead of the error processor. The small-amplitude low-frequency modulation signal (similar to the modulation signal sensed by the dc loop) is brought together with the error signal from the dc loop and compensation loop to provide the total state-feedback compensation for improved stability and dynamic responses. For the purpose of modeling of the EP, the large-amplitude switching-current information should be extracted from the ac loop and incorporated into the pulse modulation model (presented in Chapter 4.4).

(2) Modeling the EP is difficult because of the unconventional circuit implementation of the threshold detector. In the conventional design, the threshold detector is implemented with one fixed threshold voltage input, the other input containing the error

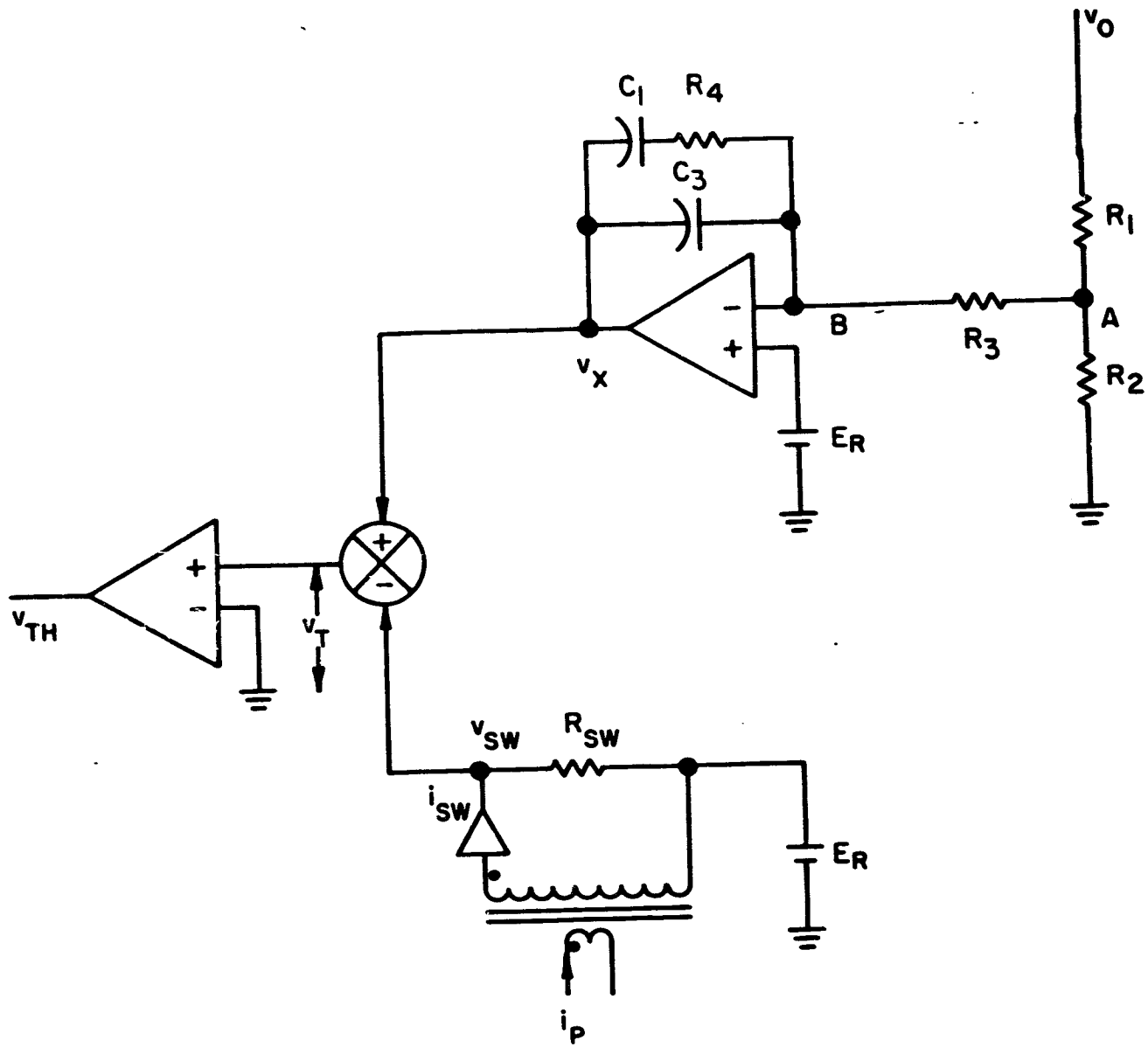


Fig. 4.3.2.1. Small-signal analytical error processor equivalent.

information. With the current-injected mode of control, both inputs to the threshold detector contain error signals or modulation signals. In order to model the whole converter system, the pulse modulator should take the combined error signal from the EP output and convert it into a pulse-width modulator duty-cycle signal. In order to implement such a "single-input single-output" pulse modulator model, various error signals derived from the multiple feedback paths should be combined to form a composite error signal containing error information from the dc, ac and compensation loops.

(3) For reasons mentioned above, the original EP circuit is modified to that of Fig. 4.3.2.1. where the positive input, v_T, to the threshold detector contains error signals from all three feedback loops. The error voltage v_T, is the output of the multi-loop EP and also serves as the input to the pulse modulator.

The functional equivalence of Fig. 4.3.1.1. and Fig. 4.3.2.1. can be justified in the following way. Mathematically for any v_X and v_{SW} waveform, the block diagram of the circuit in Fig. 4.3.2.2.(a) is equivalent to the analytical model in Fig. 4.3.2.2(b). The equivalence is proven through the following arguement. For the pulse modulator control, the following equations hold true:

$$\begin{aligned} &\text{If } v_X > v_{SW}, \text{ then } v_{TH} = 1 \\ &\text{If } v_X < v_{SW}, \text{ then } v_{TH} = 0 \end{aligned} \qquad (4.3.2.1)$$

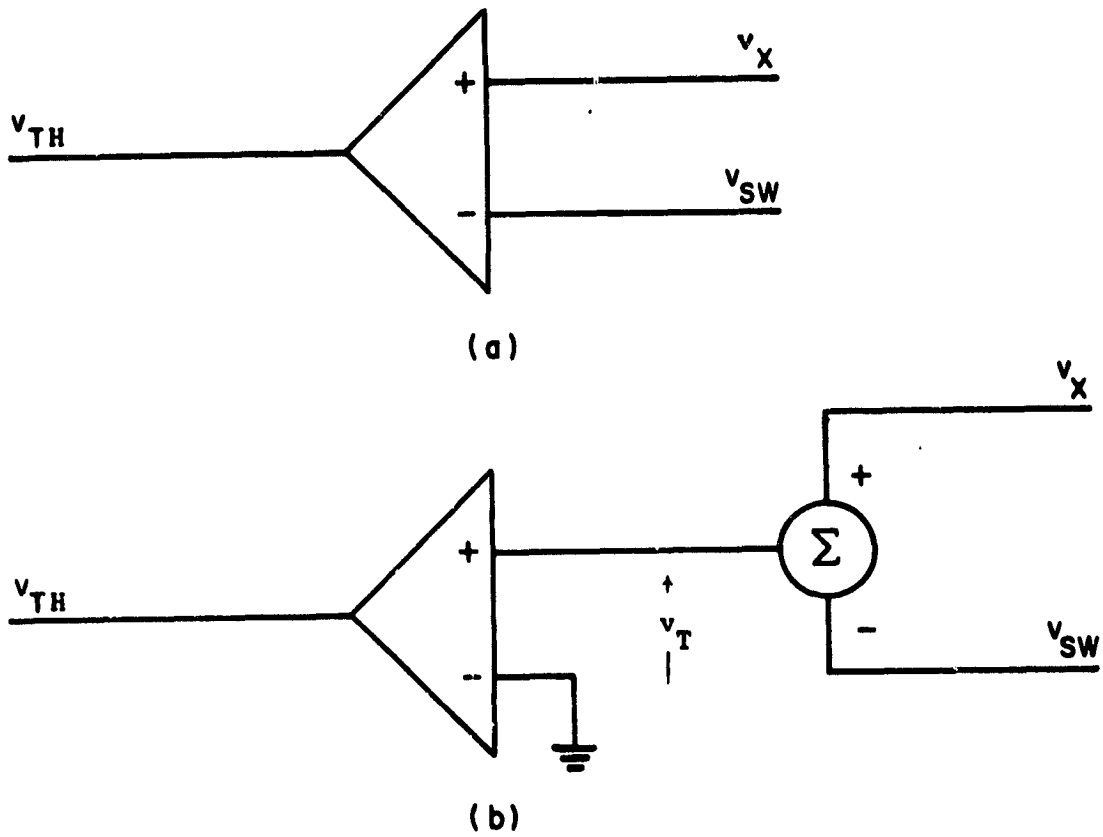


Fig. 4.3.2.2. (a) Actual circuit implementation, (b) Equivalent analytical model.

To form a composite error signal as the input to the threshold detector, the dc error voltage v_{SW} and voltage v_X are combined. The following relations hold for the modified circuit of Fig. 4.3.1.2:

$$\text{If } v_X - v_{SW} > 0 \text{ , then } v_{TH} = 1$$
$$\text{If } v_X - v_{SW} < 0 \text{ , then } v_{TH} = 0 \qquad (4.3.2.2)$$

Equations (4.3.2.1) and (4.3.2.2) are exactly the same; therefore, Fig. 4.3.1.1 and 4.3.1.2 are functionally equivalent.

In performing the small-signal analysis of the network shown in Fig. 4.3.1.2, the reference E_R is replaced by a short circuit. Applying Kirchhoff's current law at node A yields the following:

$$\hat{v}_a \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) = \frac{\hat{v}_o}{R_1} + \frac{\hat{v}_b}{R_3} \qquad (4.3.2.3)$$

where $\hat{v}_a$ is the voltage across R_2, $\hat{v}_b$ is the differential input voltage of the operational amplifier, and $\hat{v}_o$ is the output voltage.

As for node B the Kirchhoff equation is

$$\hat{v}_b \left(\frac{1}{z_X} + \frac{1}{R_3} + sC_3 \right) = \hat{v}_x \left(\frac{1}{z_X} + sC_3 \right) + \frac{\hat{v}_a}{R_3} \qquad (4.3.2.4)$$

where $z_X = R_4 + \frac{1}{sC_1}$. (4.3.2.5)

The open-loop response of the operational amplifier is A(s), where

$$\hat{v} = - A(s)\hat{v}_b , \qquad (4.3.2.6)$$

$$A(s) = \frac{-K}{1+s/Wn} \tag{4.3.2.7}$$

Substituting equation (4.3.2.6) into (4.3.2.3), and (4.3.2.4) results in the following set of equations:

$$\hat{v}_a \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) = \frac{\hat{v}_o}{R_1} - \frac{\hat{v}_x}{A(s)R_3} \tag{4.3.2.8}$$

$$-\hat{v}_x \left[\frac{1}{A(s)}\left(\frac{1}{z_X} + \frac{1}{R_3} + sC_3\right) + \left(\frac{1}{z_X} + sC_3\right)\right] = \frac{\hat{v}_a}{R_3} \tag{4.3.2.9}$$

Eliminate the node voltages $\hat{v}_a$ and $\hat{v}_b$ by simultaneously solving (4.3.2.8) and (4.3.2.9) for $\hat{v}_o$ and $\hat{v}_x$. A single expression in terms of $\hat{v}_o$ and $\hat{v}_x$ results:

$$\hat{v}_x \left[\frac{1}{A(s)R_3} \frac{1}{\left(1 + \frac{R_3}{R_1} + \frac{R_3}{R_2}\right)} - \frac{1}{A(s)}\left(\frac{1}{z_X} + \frac{1}{R_3} + sC_3\right) - \left(\frac{1}{z_X} + sC_3\right)\right] =$$

$$\frac{1}{\left(\frac{R_3}{R_1} + \frac{R_3}{R_2} + 1\right)} \frac{\hat{v}_o}{R_1} \tag{4.3.2.10}$$

Since the ac and dc expressions are low-frequency models, the operational amplifier gain is $A(s) \approx -K$. With a very large K, equation (4.3.2.10) can be simplified to the following form:

$$\hat{v}_x \approx \frac{-\left(\frac{1}{\left(\frac{R_3}{R_1} + \frac{R_3}{R_2} + 1\right) R_1}\right) \hat{v}_o}{\left(\frac{1}{z_X} + sC_3\right)} \tag{4.3.2.11}$$

The ac loop is described by the following:

$$\hat{i}_{sw} = \frac{\hat{i}_p}{n} \tag{4.3.2.12}$$

where n is the turn ratio of the current transformer.

$$\hat{v}_{sw} = \hat{i}_{sw} R_{SW} = \hat{i}_p \frac{R_{SW}}{n} \tag{4.3.2.13}$$

From Figure 3.1.2 the following equation is derived:

$$\hat{v}_t = \hat{v}_x - \hat{v}_{sw} \tag{4.3.2.14}$$

Substituting equations (4.3.2.11) and (4.3.2.13) into equation (4.3.2.14) yields the following:

$$\hat{v}_t = - \frac{\left(\dfrac{1}{\left(R_3/R_1 + R_3/R_2 + 1 \right) R_1} \right)}{\left(\dfrac{1}{Z_X} + sC_3 \right)} \hat{v}_o - \frac{R_{SW}}{n} \hat{i}_p \tag{4.3.2.15}$$

The dc loop gain for the EP is defined by the following:

$$F_{DC} = \left. \frac{\hat{v}_t}{\hat{v}_o} \right|_{\hat{i}_p = 0}$$

$$= \frac{1}{(C_1+C_3)s} \left(\frac{1 + sR_4C_1}{1 + sR_4 \left(\dfrac{C_1C_3}{C_1+C_s} \right)} \right) \left[\frac{GP}{R_1} \right] \tag{4.3.2.16}$$

where $GP = \dfrac{1}{\left(1 + \dfrac{R_3}{R_1} + \dfrac{R_3}{R_2} \right)}$.

The ac loop gain is given by the following:

$$F_{AC} = \left. \frac{\hat{v}_T}{\hat{i}_p} \right|_{\hat{v}_o = 0}$$

$$= \frac{R_{SW}}{n} \tag{4.3.2.17}$$

Fig. 4.3.2.3 illustrates the error processor block diagram.

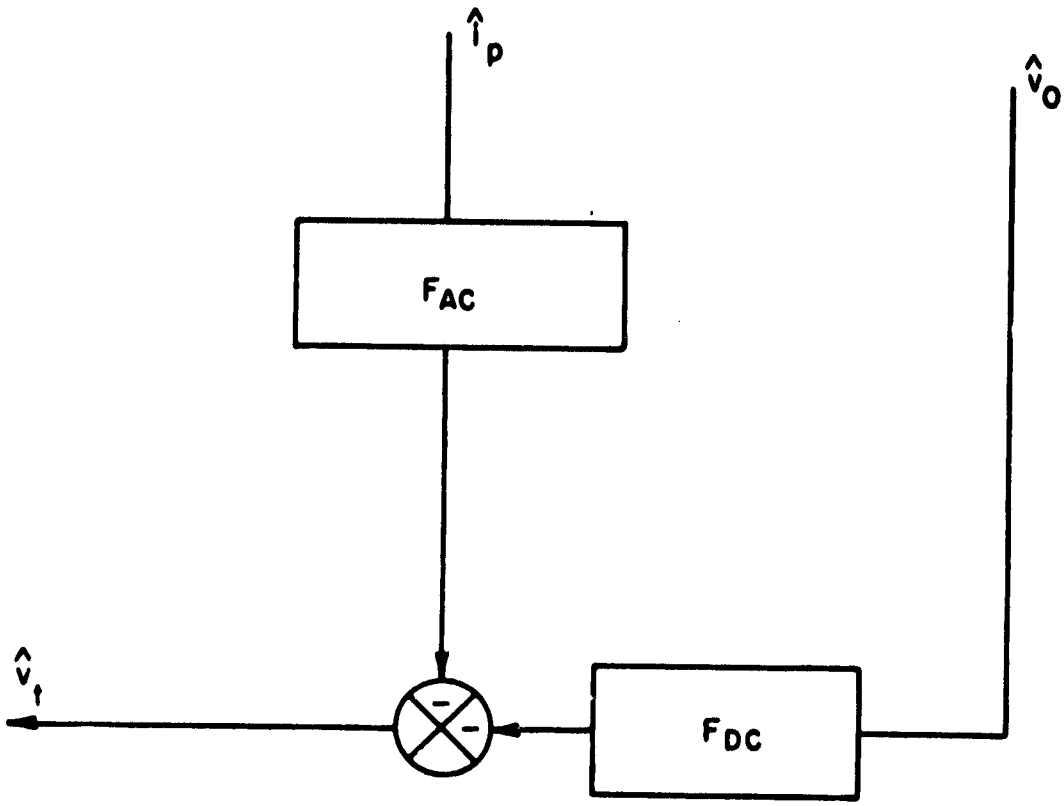


Fig. 4.3.2.3. Error processor block diagram.

4.4. PULSE MODULATOR CHARACTERIZATION

4.4.1 Pulse Modulator Descriptions

The pulse modulator converts the analog error signal from the output of the error processor into a modulated pulse-train in order to provide proper duty-ratio control of the power switch. The pulse modulator analyzed in the present chapter utilizes a constant off-time control.

Fig. 4.4.1.1 illustrates the pulse modulator (PM) in simplified block diagram form. The two inputs of the threshold comparator are the dc error voltage v_X, and the ac voltage signal v_{SW} (proportional to the current through the power switch). The dc error voltage v_X is a floating threshold level proportional to the difference between the desired and the measured output voltage. As the error between the desired and actual voltage increases, the level of the voltage v_X rises. Since the ac voltage v_{SW} is proportional to the current waveform through the power switch, peak current protection is an inherent feature of the current-injected control.

When the condition $v_{SW} > v_X$ is satisfied, the threshold detector output v_T is momentarily driven low. This signal instructs the digital signal processor (DSP) to turn off the power switch. Therefore by limiting the level of v_X, the peak current protection of the power switch can be achieved.

For constant off-time implementation the DSP output, D, is latched low for a predetermined amount of time. At the end of the off-time period, the power switch is commanded on and the cycle repeats.

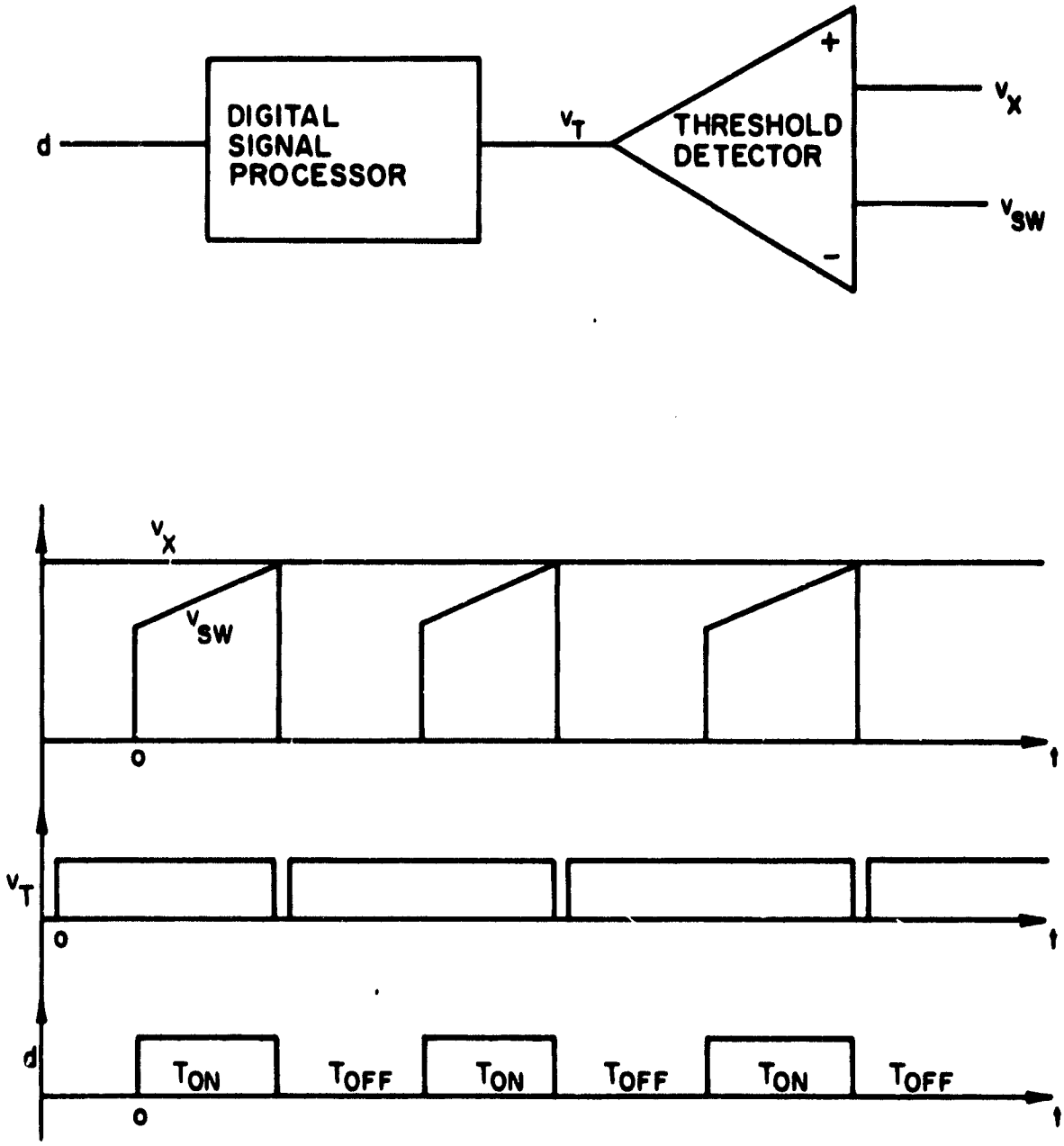


Fig. 4.4.1.1. Pulse modulator.

4.4.2 Small-Signal Model

To study the small-signal behavior of the pulse modulator, an analytical model is developed using the describing function technique.

Fig. 4.4.2.1 shows the block diagram of the analytical model at steady-state without a low frequency disturbance. As shown in Fig. 4.4.2.1.(b), when v_{SW} is greater than v_X, T_{OFF} commences. S_N is the rising slope of the switching-current signal v_{SW} during the period T_{ON}. S_F is the falling slope determined by the secondary current of the two winding inductor reflected back to the primary side during the period T_{OFF}. The trajectory formed by S_N and S_F is proportional to the inductor MMF and is used to determine continuous or discontinuous current operation.

Fig. 4.4.2.2 shows the equivalent circuit waveforms for the perturbed case. The small-signal disturbance is represented by an ac generator placed in the dc loop as illustrated in Fig. 4.4.2.2(a). For the perturbed case, the magnitude of the low-frequency ac signal is assumed to be sufficiently small and the rising slope S_N, and falling slope S_F, are considered constant and unaffected by the disturbance. With this assumption, the perturbed switching-current information v_{SW}, along with the error voltage v_X, can be modeled.

The development of Fig. 4.4.2.2(b) is as follows:

(i) Given a slope S_N determined by the power stage's supply voltage v_I, the primary inductance Lp, and an initial dc starting value large enough to guarantee continuous-current operation. From the starting point a line is drawn with the slope

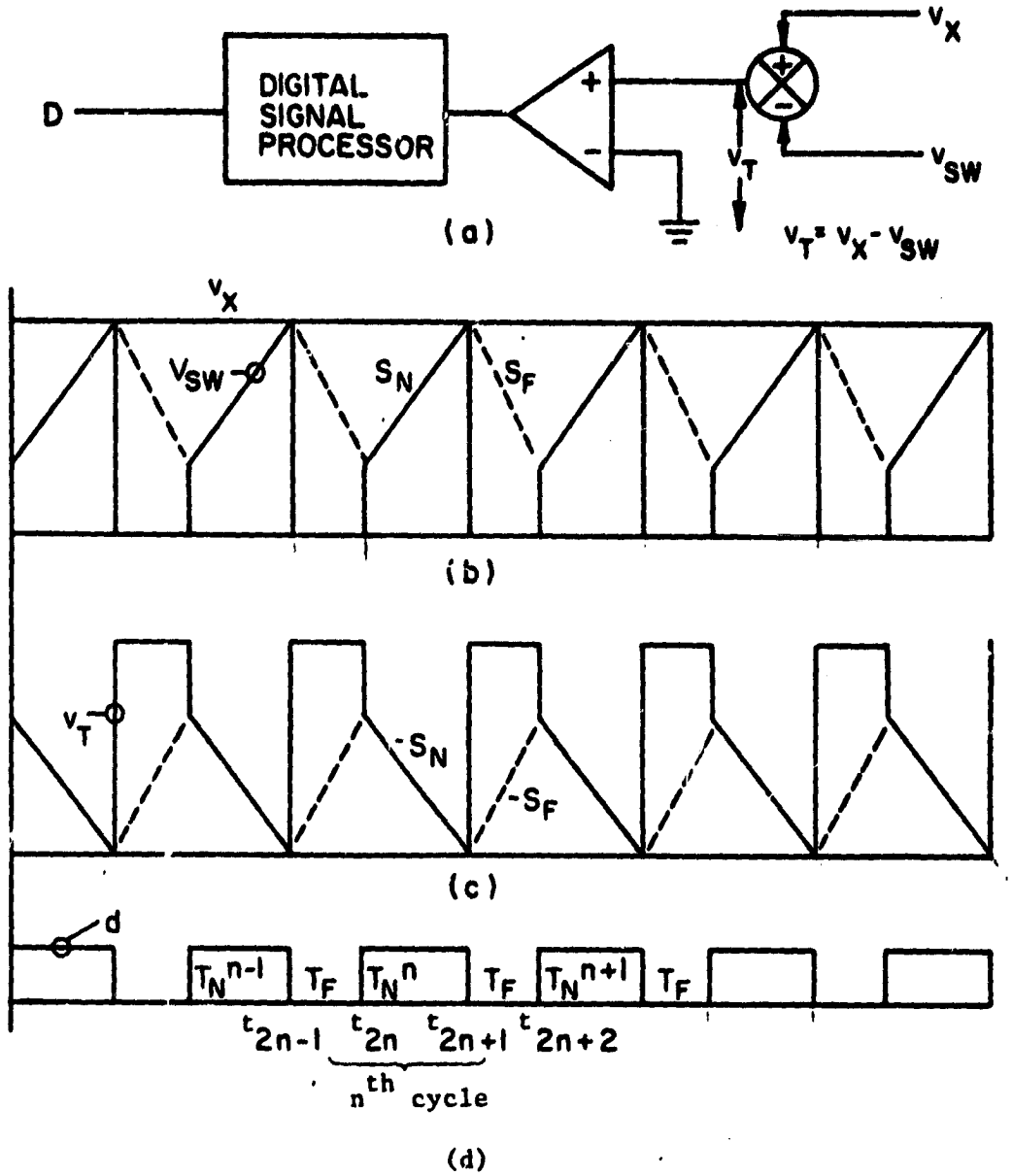


Fig. 4.4.2.1. Unperturbed analytical PM waveforms.

C-3

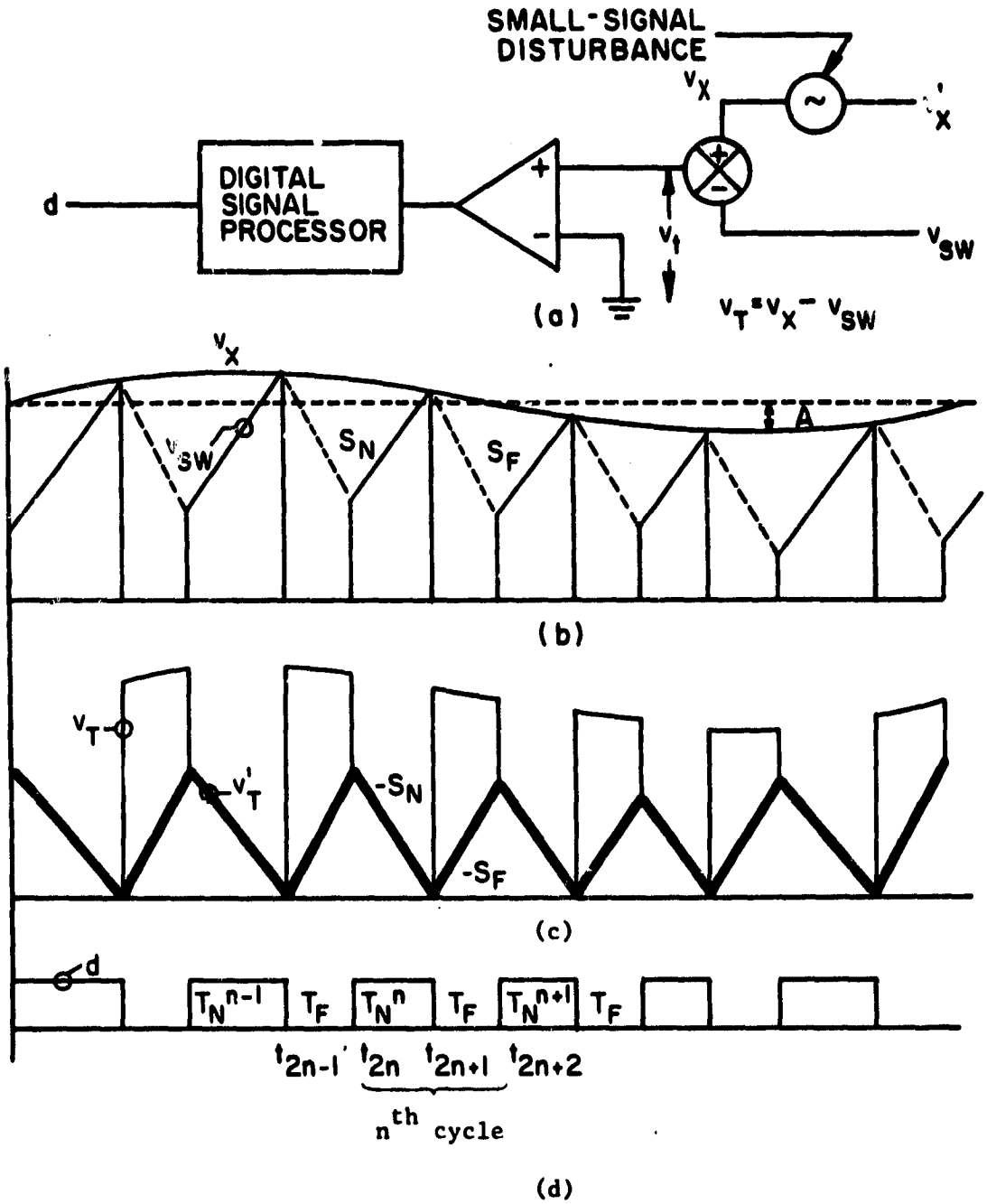


Fig. 4.4.2.2. Perturbed analytical PM waveforms.

S_N. At the intersection of the perturbed v_X and the switching-current information v_{SW}, T_{OFF} begins. After a set span of time equal to the period T_{OFF} expires, the cycle repeats.

(ii) The initial point for the next cycle is determined by subtracting the magnitude $S_F \cdot T_{OFF}$ from v_X at that particular point in time.

(iii) From the new initial values (i) and (ii) are repeated.

Fig. 4.4.2.2(c) shows the input v_T to the analytical threshold detector. Using the relation $v_T = v_X - v_{SW}$, the development of Fig. 4.4.2.2(d) can be understood. Fig. 4.4.2.2(d) illustrates the perturbed duty-cycle.

The small-signal behavior of the PM can now be modeled. A set of equations are developed for the darkened trajectory v_T' of Fig. 4.4.2.2(c). v_T' is used because the trajectory describes the low-frequency modulation affecting the PM gain. The additional information in v_T that deals with the dc component of the switching waveform of the converter is not relevant in the modulation of the duty cycle signal, and therefore has no contribution to the PM small-signal gain.

4.4.3 Formulation of the PM Transfer Function

The output of the PM can be expressed in a Fourier series in the form:

$$d(t) = D + a_1 \sin \omega t + b_1 \cos \omega t + \cdots$$

The input of the PM can also be expressed in a Fourier series in the form:

$$v_T'(t) = V + c_1 \sin \omega t + d_1 \cos \omega t + \cdots$$

The describing function F_M of the pulse modulator is defined as:

$$F_M \triangleq \frac{d(t)}{v_t'(t)} = \frac{(a_1^2 + b_1^2)^{\frac{1}{2}}}{(c_1^2 + d_1^2)^{\frac{1}{2}}} e^{j\left(\tan^{-1}\frac{b_1}{a_1} \cdot \tan^{-1}\frac{d_1}{c_1}\right)} \qquad (4.4.3.1)$$

The resultant waveform v_T' is a function of S_N and S_F (both assumed positive) and the sinusoidal disturbance A sin wt. During the period T_{OFF} at $(N-1)^{th}$ cycle v_T' has the form:

$$v_T'(t) = S_F(t - t_{2n-1}) + A \sin \omega t - A \sin \omega t_{2n-1}. \qquad (4.4.3.2)$$

During the period T_{ON} at the Nth cycle v_T' has the form:

$$v_T'(t) = S_N(t_{2n+1} - t) + A \sin \omega t - A \sin \omega t_{2n+1}. \qquad (4.4.3.3)$$

The on-time ΔT_N at the nth cycle $[t_{2n}, t_{2n+2}]$ can be expressed through the following development: ΔT_N can be derived from equations (4.4.3.2) and (4.4.3.3) by evaluating the equations at $t = t_{2n}$, where

$$v_T'(t_{2n}) = S_F(t_{2n} - t_{2n-1}) + A \sin \omega t_{2n} - A \sin \omega t_{2n-1} \qquad (4.4.3.4)$$

or

$$v_T'(t_{2n}) = S_N(t_{2n+1} - t_{2n}) + A \sin \omega t_{2n} - A \sin \omega t_{2n+1}. \qquad (4.4.3.5)$$

From Figure 4.2.2, $T_F \triangleq T_{OFF} = t_{2n} - t_{2n-1}$.

Let $\Delta T_N \triangleq t_{2n+1} - t_{2n-1}$.

Set (4.3.3) equal to (4.3.4) and solve for ΔT_N.

$$S_F T_F + A \sin \omega t_{2n} - A \sin \omega t_{2n-1} = S_N(t_{2n+1} - t_{2n}) + A \sin \omega t_{2n} - A \sin \omega t_{2n+1} \qquad (4.4.3.6)$$

$$(S_F + S_N)T_F - S_N \Delta T_N = -2A \sin \frac{\omega \Delta T_N}{2} \cos \omega\left(t_{2n-1} + \frac{\Delta T_N}{2}\right) \qquad (4.4.3.7)$$

$$\Delta T_N = \frac{(S_F + S_N)T_F}{S_N - A\omega \cos \omega t_{2n-1}}$$

$$= \left(1 + \frac{S_F}{S_N}\right) T_F \frac{1}{1 - \frac{A\omega}{S_N} \cos \omega t_{2n-1}} \qquad (4.4.3.8)$$

The duty-cycle output d, may be expressed in the following form:

$$d(t) \triangleq D + a_1 \sin \omega t + b_1 \cos \omega t + \cdots \qquad (4.4.3.9)$$

The coefficient of sin ωt in equation (4.4.3.9) can be expressed as:

$$a_1 = \frac{\omega}{\pi} \left[\int_0^{t_1} \sin \omega t \, dt + \int_{t_2}^{t_3} \sin \omega t \, dt + \cdots + \int_{t_{2n}}^{t_{2n+1}} \sin \omega t \, dt + \cdots \right]$$

$$= \frac{\omega}{\pi} \frac{1}{A} \left[\int_0^{t_1} A \sin \omega t \, dt + \int_{t_2}^{t_3} A \sin \omega t \, dt + \cdots \right]$$

$$= \frac{1}{\pi} \frac{1}{A} \sum_{n=0}^{N} A_{2n+1} \qquad (4.4.3.10)$$

where $A_{2n+1} = \frac{\Delta T_N - T_F}{2} (A \sin \omega t_{2n} + A \sin \omega t_{2n+1})$

$$= (\Delta T_N - T_F) A \sin \omega \left(t_{2n-1} + \frac{T_F + \Delta T_N}{2}\right) \cos \omega \left(\frac{\Delta T_N - T_F}{2}\right)$$

$$= A(\Delta T_N - T_F) \Big\{ \sin \omega t_{2n-1} [\tfrac{1}{2} \cos\omega\Delta T_N + \tfrac{1}{2} \cos\omega T_F]$$

$$+ \cos \omega t_{2n-1} [\tfrac{1}{2} \sin\omega\Delta T_N + \tfrac{1}{2} \sin\omega T_F] \Big\} \qquad (4.4.3.11)$$

A first-order approximation for A_{2n+1} is:

$$A_{2n+1} \simeq A(\Delta T_N - T_F) \sin \omega t_{2n-1} + \frac{A}{2} (\Delta T_N^2 - T_F^2) \cos \omega t_{2n-1} \qquad (4.4.3.12)$$

Eliminating second order effects:

$$A_{2n+1} \simeq \Delta T_N A(1 - \frac{T_F}{\Delta T_N}) \sin \omega t_{2n-1} \qquad (4.4.3.13)$$

From equation (4.3.7),

$$a_1 = \frac{1}{\pi} \frac{1}{A} \sum_{n=o}^{K} A(1 - \frac{T_F}{\Delta T_N}) \sin \omega t_{2n-1} \Delta T_N \qquad (4.4.3.14)$$

where K is the ratio between the switching frequency and the modulation frequency. In order to simplify the analysis, it is assumed that K is an integer.

If ΔT_N is small compared to the disturbance period, i.e. if K is very large, it follows that

$$a_1 \simeq \frac{1}{A\pi} \int_o^{2\pi/\omega} A(1 - \frac{T_F}{\Delta T_N}) \sin \omega t_{2n-1} \, dt$$

$$= \frac{1}{A\pi} \left\{ \int_o^{2\pi/\omega} A \sin \omega t \, dt - \int_o^{2\pi/\omega} AT_F \frac{\left(1 - \frac{A\omega}{S_N} \cos \omega t\right)}{\left(1 + \frac{S_F}{S_N}\right) T_F} \cdot \sin \omega t \, dt \right\}$$

$$= \frac{1}{\pi} \frac{1}{1 + \frac{S_F}{S_N}} \frac{A\omega}{S_N} \int_o^{2\pi/\omega} \cos \omega t \sin \omega t \, dt = 0 \qquad (4.4.3.15)$$

Equation 4.4.3.15 is orthogonal. Therefore the coefficient a_1 is zero.

The coefficient of cos wt in equation (4.3.6) is:

$$b_1 = \frac{\omega}{\pi} \left[\int_o^{t_1} \cos \omega t \, dt + \int_{t_2}^{t_3} \cos \omega t \, dt + \cdots + \int_{t_{2n}}^{t_{2n+1}} \cos \omega t \, dt + \cdots \right]$$

$$= \frac{1}{A\pi} \left[A \sin \omega t_1 + A \sin \omega t_3 - A \sin \omega t_2 + \cdots + A \sin \omega t_{2n+1} \right.$$

$$\left. - A \sin \omega t_{2n} + \cdots \right]$$

$$= \frac{1}{A\pi}\left[\sum_{n=0}^{N} B_{2n+1}\right] \qquad (4.4.3.16)$$

where,

$$B_{2n+1} = A \sin \omega t_{2n+1} - A \sin \omega t_{2n}$$

$$= 2A \cos \frac{\omega}{2}(t_{2n+1} + t_{2n}) \sin \frac{\omega}{2}(t_{2n+1} - t_{2n})$$

$$= 2A \cos \omega \left(t_{2n-1} + \Delta T_N - \frac{T_F}{2}\right) \sin \omega \left(\frac{\Delta T_N - T_F}{2}\right) \qquad (4.4.3.17)$$

A first order approximation for equation (4.3.15) is:

$$B_{2n+1} \cong 2A \left(\omega \frac{\Delta T_N - T_F}{2}\right) \cos \omega t_{2n-1}$$

$$= \frac{A\omega}{\Delta T_N}(\Delta T_N - T_F) \cos \omega t_{2n-1} \, \Delta T_N \qquad 4.3.18)$$

From equation (4.4.3.13)

$$b_1 = \frac{1}{A\pi}\left[\sum_{n=o}^{N} \frac{A\omega}{\Delta T_N}(\Delta T_N - T_F) \cos \omega t_{2n-1} \, \Delta T_N\right] \qquad (4.4.3.19)$$

With ΔT_N small compared to the modulation period equation (4.4.3.19) can be expressed as follows:

$$b_1 = \frac{1}{A\pi}\int_{o}^{2\pi/\omega} A\omega\left[1 - \frac{T_F}{\left(1 + \frac{S_F}{S_N}\right)T_F}\left(1 - \frac{A\omega}{S_N}\cos \omega t\right)\right] \cos \omega t \, dt$$

$$= \frac{\omega}{\pi}\frac{1}{1 + \frac{S_F}{S_N}}\int_{o}^{2\pi/\omega} \frac{A\omega}{2S_N}(1 + \cos 2\omega t)dt$$

$$= \frac{A\omega}{S_N + S_F} \qquad (4.4.3.20)$$

Again, when modeling the analog voltage v_T, the information that needs to be extracted is contained in v_T'. v_T' contains the low-frequency information necessary without the high-frequency switching signal of v_T. From equation (4.3.1) the small-signal input voltage to the pulse modulator is:

$$v_T'(t_{2n}) = S_F T_F - A \sin \omega t_{2n-1} + A \sin \omega t_{2n}$$

$$= S_F T_F + 2A \cos \frac{\omega}{2} (t_{2n} + t_{2n-1}) \sin \frac{\omega}{2} T_F \qquad (4.4.3.21)$$

In equation (4.4.3.21) $\sin \frac{\omega T_F}{2}$ can be approximated by $\frac{\omega T_F}{2}$ resulting in:

$$v_T' \cong S_F T_F + A\omega T_F \cos \omega(t_{2n-1} + \frac{T_F}{2}) \qquad (4.4.3.22)$$

From equation (4.4.3.22) the fundamental of the small-signal average of v_T' can be taken.

$$\hat{v}_t' \cong \frac{1}{2} A\omega T_F \cos \omega(t + \frac{T_F}{2}) \qquad (4.4.3.23)$$

The describing function F_M for the pulse-width modulator is:

$$F_M \triangleq \frac{\hat{d}(t)}{\hat{v}_t'} = \frac{(a_1^2 + b_1^2)^{\frac{1}{2}}}{\hat{v}_t'} e^{-j \tan^{-1}(b_1/a_1)} \qquad (4.4.3.24)$$

Substituting equations (4.4.3.15), (4.4.3.20) and (4.4.3.23) into (4.4.3.24) the PM gain is:

$$|F_M| = \frac{\frac{A\omega}{S_N + S_F}}{\frac{1}{2} A\omega T_F} = \frac{2}{(S_N + S_F)T_F} \qquad (4.4.3.25)$$

Phase $\angle F_M = \frac{\omega T_F}{2}$,

$$F_M = \frac{2}{(S_N + S_F)T_F} e^{j\omega T_F} \qquad (4.4.3.26)$$

The slopes S_N and S_F can be defined by the system parameters. During T_{on},

$$V_I = I_P R_P + L_P \frac{di_P}{dt} \tag{4.4.3.27}$$

Let $\frac{di_P}{dt} \triangleq S_N'$ where S_N' is the slope of i_p during T_{on}. Then:

$$V_I = I_P R_P + L_P S_N'$$

and

$$S_N' = \frac{V_I - I_P R_P}{L_P} \tag{4.4.3.28}$$

The magnitude of $I_P R_P$ is much less than V_I, so (4.4.3.28) is approximated by:

$$S_N' \simeq \frac{V_I}{L_P} \tag{4.4.3.29}$$

The current transformer used to sense the switching-current reduces the sensing current by a 1:n turns ratio resulting in the following expressions:

$$S_N'' = \frac{V_I}{nL_P} \tag{4.4.3.30}$$

The signal sensed by the comparator is a voltage proportional to the current passing through R_{SW}. Therefore

$$S_N = \frac{V_I R_{SW}}{nL_P} \text{ ,where, } S_N = R_{SW} \cdot S_N'' \tag{4.4.3.31}$$

During T_{OFF}, S_F may be found through the following:

$$|\Delta i T_{ON}| = |\Delta i T_{OFF}| \tag{4.4.3.32}$$

$$|\Delta i T_{ON}| = S_N' \, T_{ON} \tag{4.4.3.33}$$

$$|\Delta i T_{OFF}| = S_F' \, T_{OFF} \tag{4.4.3.34}$$

The substitution of equations (4.4.3.33) and (4.4.43.34) into equation (4.3.32) results in the expressions:

$$S_N' \, T_{ON} = S_F' \, T_{OFF} \tag{4.4.3.35}$$

$$S_F' = \frac{T_{ON}}{T_{OFF}} S_N' \tag{4.4.3.36}$$

Applying equation (4.4.3.31) to S_F', we obtain

$$S_F' = \frac{T_{ON}}{T_{OFF}} V_I \frac{R_{SW}}{nL_P} = \frac{N_P}{N_S} \frac{V_O}{nL_P} R_{SW} \tag{4.4.3.37}$$

Substituting equations (4.4.3.31) and (4.4.43.37) into the PM describing function the following can be obtained:

$$F_M = \frac{2}{\frac{V_I \, R_{SW}}{nL_P} \left(\frac{T_{ON}}{T_{OFF}} + 1 \right) T_{OFF}} e^{j\frac{\omega T_F}{2}} \tag{4.4.3.38}$$

$$e^{j\frac{\omega T_F}{2}} = e^{j\frac{\pi T_F}{T_M}} \approx 1 \tag{4.4.3.39}$$

where $T_F/T_M << 1$. T_F is the off-time period of the switch and T_M is the period of the low-frequency modulation. Therefore the F_M gain may be approximated by:

$$F_M \approx \frac{2nL_P}{V_I R_{SW}} \frac{1}{T_{ON} + T_{OFF}} \tag{4.4.3.40}$$

Expressing the F_M describing function in terms of the duty-ratio instead of T_{ON} and T_{OFF}, equation (4.4.3.40) becomes:

$$F_M = \frac{2nL_P}{V_I R_{SW}} \frac{1}{T_{OFF} \left(1 + \frac{N_P}{N_S} \frac{V_O}{V_I} \right)} \tag{4.4.3.41}$$

Fig. 4.4.2.3 is the block diagram for the small-signal gain from the composite error processor signal v_T to the pulse modulator output d.

Fig. 4.4.2.3. Pulse modulator gain block

4.5.0 PERFORMANCE ANALYSES AND TEST VERIFICATIONS

4.5.1 Small-signal Block Diagram

The objective of this section is to incorporate the power stage, analog error processor, and pulse modulator small-signal models into a closed-loop block diagram. The block diagram model will be used to examine the open-loop and closed-loop performances of the switching regulator. Fig. 4.5.1.1 shows the block diagram for the buck/boost regulator derived from Fig. 4.2.3.3, Fig. 4.3.2.3, and Fig. 4.4.2.3.

The small-signal analysis will include control-to-output response, dc open-loop behavior, system open-loop response stability, closed-loop response audiosusceptibility, and output impedance $\frac{\hat{v}_o(s)}{\hat{i}_o(s)}$

In this chapter, a Bode plot showing the gain and phase of each particular transfer function is presented. The analytical curves are compared with the experimental measurements to verify the small-signal model. The analytical curves are presented by solid lines and the experimental results by the following:

(i) Gain curve - x

(ii) Phase curve - ●

The gain and phase plots for the small-signal analysis employ the following converter parameters and operating conditions:

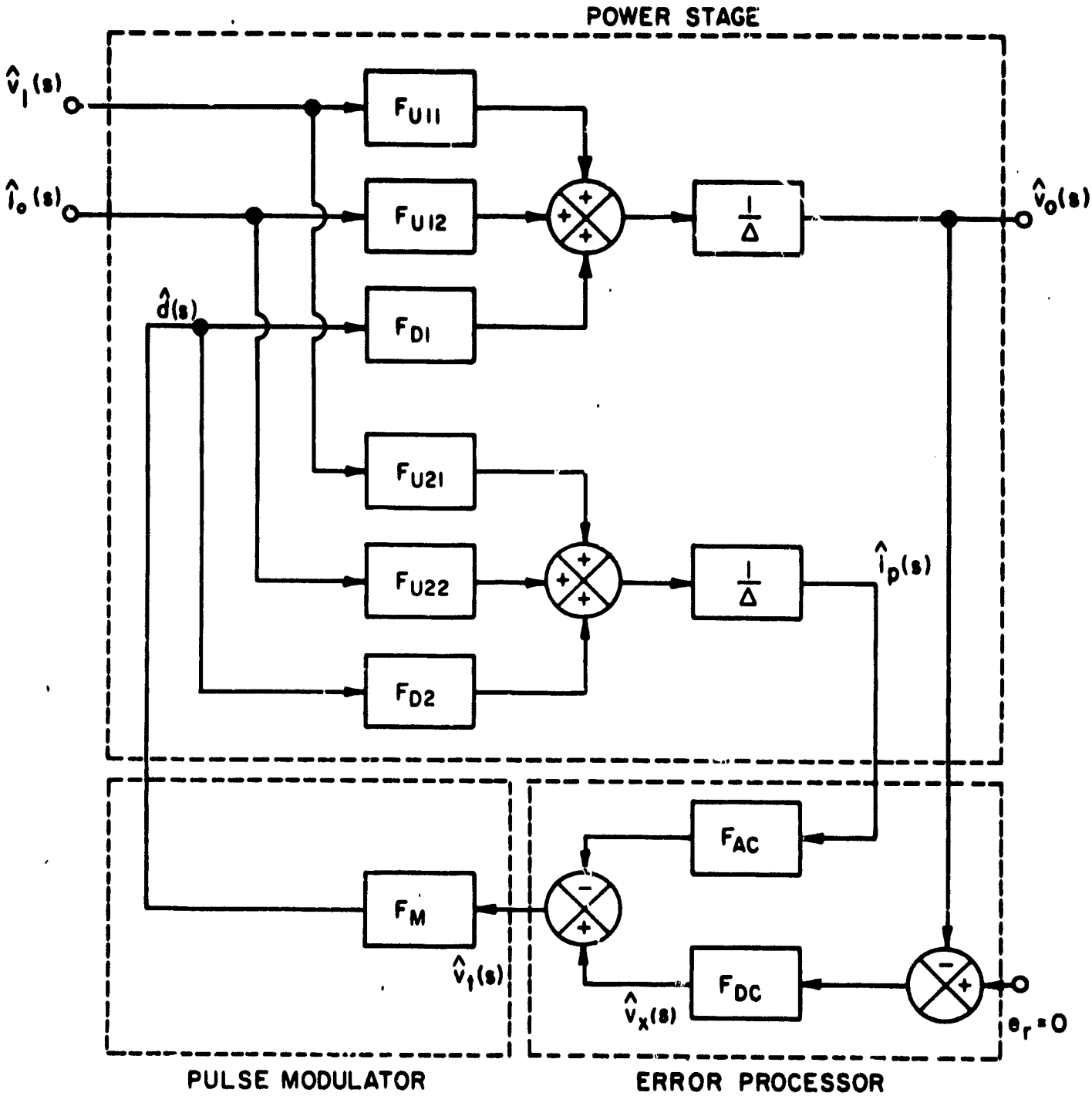


Fig. 4.5.1.1. Generalized small-signal block diagram for buck/boost converter.

Converter Parameters

L_P = 464.94 microhenries

L_S = 101.64 microhenries

R_S = .293 ohms

L_e = 549.70 microhenries

R_e = 1.58 ohms

C = 441 microfarads

R_C = .07 ohms

R_L = 15 ohms

N_P = 86 turns

N_S = 40 turns

R_1 = 11.47 kilo-ohms

R_e = 10.0 kilo-ohms

R_3 = 23.9 kilo-ohms

R_4 = 105.0 kilo-ohms

C_1 = 11.8 nanofarads

C_3 = 22.6 picofarads

CTN = n = 200 turns

R_{SW} = 250. ohms

ω_o = 2021 rad/sec

Operating Conditions

V_I = 18.5 volts

V_o = 11.4 volts

D = .57

D' = .43

T_{OFF} = 11.0 microsecs

4.5.2 Control-to-Output Response

The control-to-output response is the open-loop gain from $\hat{v}_x(s)$ to the output $\hat{v}_o(s)$ in Fig.4.5.1.1. The control-to-output transfer function denotes the power stage characteristics plus ac feedback. Figure 4.5.2.1 illustrates the gain block diagram for the control-to-output response, derived from the system block diagram.

From Fig. 4.5.2.1 the control-to-output transfer function is derived, yielding the following results:

$$\frac{\hat{v}_o(s)}{\hat{v}_x(s)} = \frac{+F_M F_{D1}}{\Delta + F_M F_{AC} F_{D2}} \qquad (4.5.2.1)$$

Where $\Delta = s^2 + 2\zeta\omega_o s + \omega_o^2$

Substituting equations (4.2.3.12), (4.3.2.17) and (4.4.3.41) into the control-to-output transfer function the following equations can be generated:

$$\frac{\hat{v}_o(s)}{\hat{v}_x(s)} = \frac{F_M \frac{V_0 \omega_o^2}{DD'} (R_C C s+1)\left[-\left(\frac{DL_e}{R_L} s + \left(R_e + \frac{R_c}{D'}\right)\frac{D}{R_L} - 1\right)\right]}{(s^2 + 2\zeta\omega_o s + \omega_o^2) + F_M F_{AC} \frac{V_0 N_s}{R_L N_P}\left(\frac{1}{L_s C}(R_L C s + D + 1) + \frac{(s^2 + 2\zeta\omega_o s + \omega_o^2)}{D'}\right)}$$

(4.5.2.2)

Employing the inequality $(R_e + \frac{R_c}{D'})\frac{D}{R_L} << 1$, equation (4.5.2.2) is simplified

$$\frac{\hat{v}_o(s)}{\hat{v}_x(s)} \simeq \frac{-F_M V_0 \omega_o^2}{DD'} \frac{(R_C C s+1)\left(\frac{DL_e}{R_L} s - 1\right)}{(1+\frac{F}{D'})s^2 + \left(2\zeta\omega_o + F\left(\frac{R_L}{L_S} + \frac{2\zeta\omega_o}{D'}\right)\right)s + \omega_o^2 + F\left(\frac{D+1}{L_S C} + \frac{\omega_o^2}{D'}\right)}$$

(4.5.2.3)

where $F = F_M F_{AC} \frac{V_0 N_s}{R_L N_P}$.

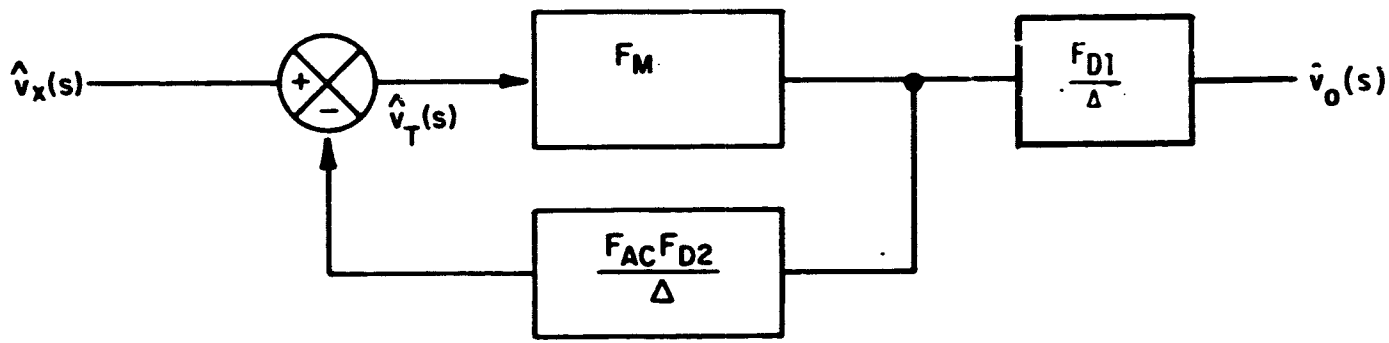


Fig. 4.5.2.1. Control-to-output response.

Equation (4.5.2.3) may be further simplified to read

$$\frac{\hat{v}_o(s)}{\hat{v}_x(s)} = \frac{-F_M V_0 \omega_o^2}{(D'+F)D} \frac{(R_C Cs+1)\left(\frac{DL_e}{R_L}s-1\right)}{s^2+\left(2\zeta\omega_o+\frac{FD'}{F+D'}\frac{R_L}{L_S}\right)s+\omega_o^2+\frac{FD'}{F+D'}\frac{(D+1)}{L_S C}} \qquad (4.5.2.4)$$

Equations (4.5.2.4) is the control-to-output transfer function with the angle expressed in phase delay.

4.5.2.1 Test Verification for Control-to-Output Response

Fig. 4.5.2.2 demonstrates the method used to measure the control-to-output response. An ac signal, A sin wt, is injected into the dc loop. The magnitude A is adjusted to provide the optimal signal-to-noise ratio (a clear and stable read out). Excessive amplitude of the injected signal could result in distortion of the modulation waveform and should be avoided. Channels A and B are connected as shown in Fig. 4.5.2.2. Channel B minus Channel A results in the desired control-to-output response.

Fig. 4.5.2.3 shows the gain and phase of equation (4.5.2.4) for the dc-dc converter. The solid-line projection represents the analytical solutions for the control-to-output response.

4.5.3 DC Open-Loop Behavior

The dc open-loop response is the open-loop gain derived from opening the dc feedback loop. Due to the nature of the current-injected mode of control, the true system open-loop response cannot be measured. The dc open-loop response can be used to indicate the

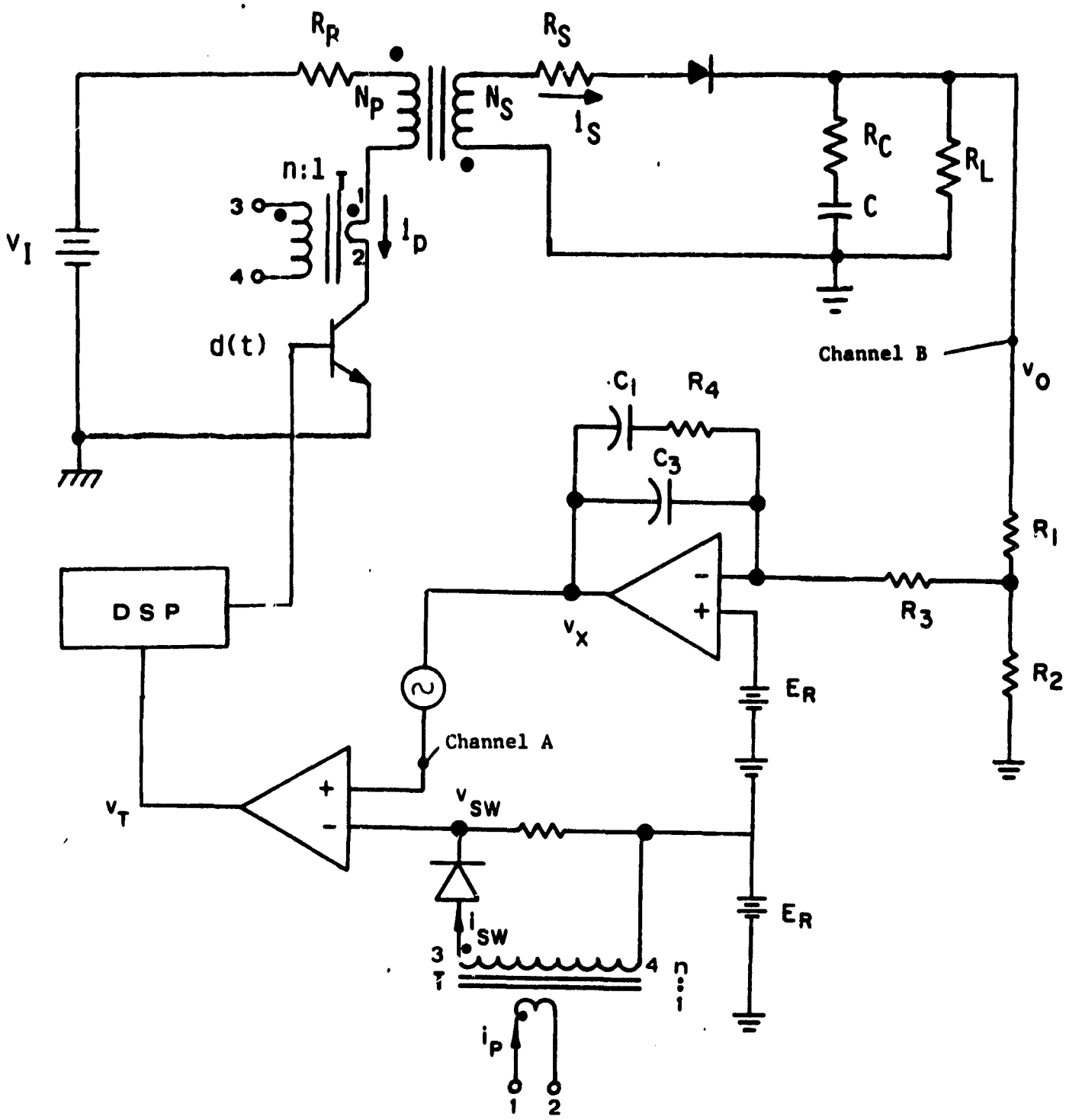


Fig. 4.5.2.2. Measurement technique for the control-to-output characteristics.

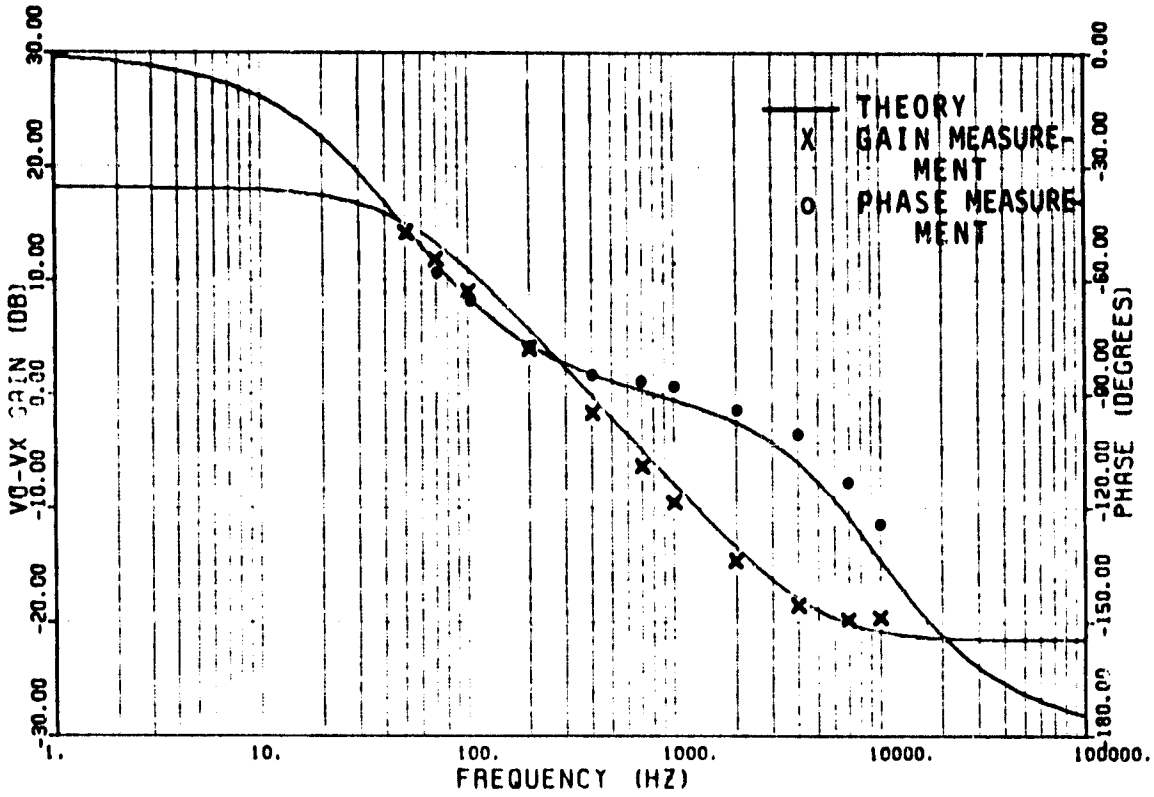


Fig. 4.5.2.3. Theory and measurement of control-to-output characteristics ($\hat{v}_o/\hat{v}_x$).

relative stability of the system. Fig. 4.5.3.1 illustrates the block diagram for the dc open-loop behavior.

Referring to Fig. 4.5.3.1 the dc open-loop transfer function can be expressed in the following form:

$$-G_{DL} = \frac{-F_M F_{DC} F_{D1}}{\Delta + F_M F_{AC} F_{D2}} \tag{4.5.3.1}$$

The general expression can be formulated by substituting equations (4.2.3.12), (4.3.2.16), (4.3.2.17) and (4.4.3.41) into equation (4.5.3.1). The following formulation yields:

$$G_{DL} = \frac{\dfrac{+F_M V_0 \omega_o^2}{DD'}(R_C Cs+1)\left(\dfrac{1}{(C_1+C_3)s}\left(\dfrac{1+sR_4C_1}{1+sR_4\left(\dfrac{C_1C_3}{C_1+C_3}\right)}\right)\right)\left(\dfrac{GP}{R_1}\right)\left(1-\dfrac{D}{R_L}\left(L_e s+R_e+\dfrac{R_C}{D}\right)\right)}{(s^2+2\zeta\omega_o s+\omega_o^2)+F_M F_{AC}\dfrac{V_0 N_S}{R_L N_P}\left(\dfrac{1}{L_S C}\left(R_L Cs+D+1\right)+\dfrac{s^2+2\zeta\omega_o s+\omega_o^2}{D'}\right)} \tag{4.5.3.2}$$

With $\left(R_e+\dfrac{R_c}{D'}\right)\dfrac{D}{R_L} << 1$ and $F = F_M F_{AC}\dfrac{V_o N_S}{R_L N_P}$, equation (4.5.3.2) becomes:

$$G_{DL} = \frac{\dfrac{F_M V_0 \omega_o^2}{(D'+F)D(C_1+C_3)}(R_C Cs+1)\left(\dfrac{DL_e}{R_L}s-1\right)\left(\dfrac{1+sR_4C_1}{1+sR_4\left(\dfrac{C_1C_3}{C_1+C_3}\right)}\right)\left(\dfrac{GP}{R_1}\right)}{s\left(s^2+\left(2\zeta\omega_o+\dfrac{FD'}{F+D'}\dfrac{R_L}{L_S}\right)s+\omega_o^2+\dfrac{FD'}{F+D'}\dfrac{(D+1)}{L_S C}\right)} \tag{4.5.3.3}$$

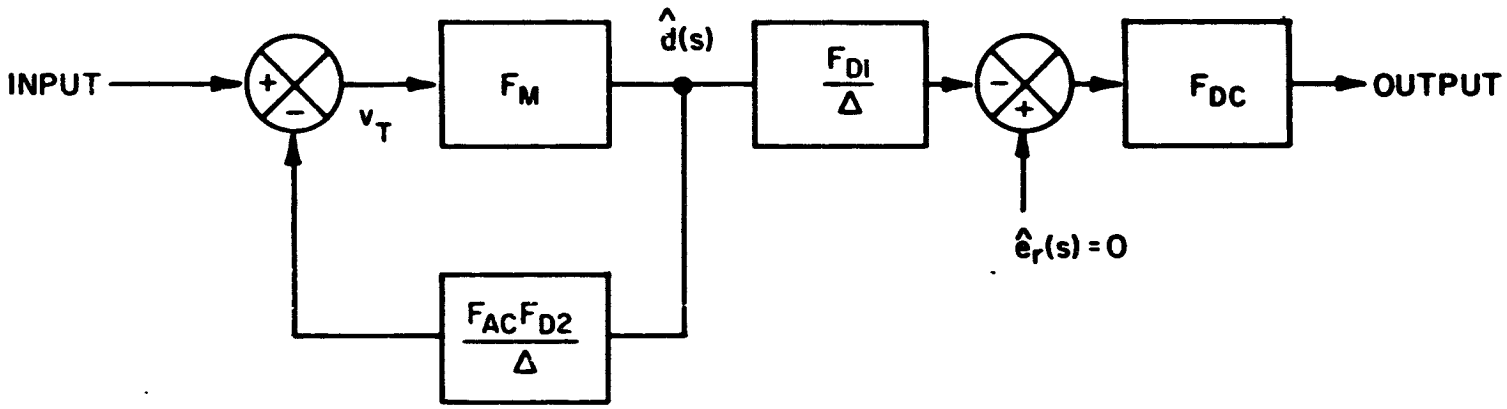


Fig. 4.5.3.1. DC open-loop block diagram.

Equation (4.5.3.3) is the dc open-loop transfer function for the current-injected converter.

4.5.3.1 Test Verification for DC Open-Loop

The dc-open-loop measurements are taken by injecting an ac signal into the dc loop. After traversing the loop, gain and phase of the ac signal is measured. Fig. 4.5.3.2 illustrates the measuring technique employed for the dc-open-loop response.

The analytical and experimental waveforms for the dc open-loop gain and phase are shown in Fig. 4.5.3.3. The analytical waveforms are represented by the solid line and the experimental gain measurements are denoted by the "×" sign. The phase measurements are represented by the "•" sign.

4.5.4 System Open-Loop Response

The system open-loop response characterizes the converter's stability. Because of the multiple feedback paths of the converter, the loop is opened at a node common to all the feedback paths. Analytically, the loop can be opened in this fashion. However, experimentally this characteristic can not be measured. In current-injected control the ac signal and dc information are fed into a comparator. Physically, the only location common to the dc and ac loop is the output of the threshold detector. Unfortunately the comparator output is a

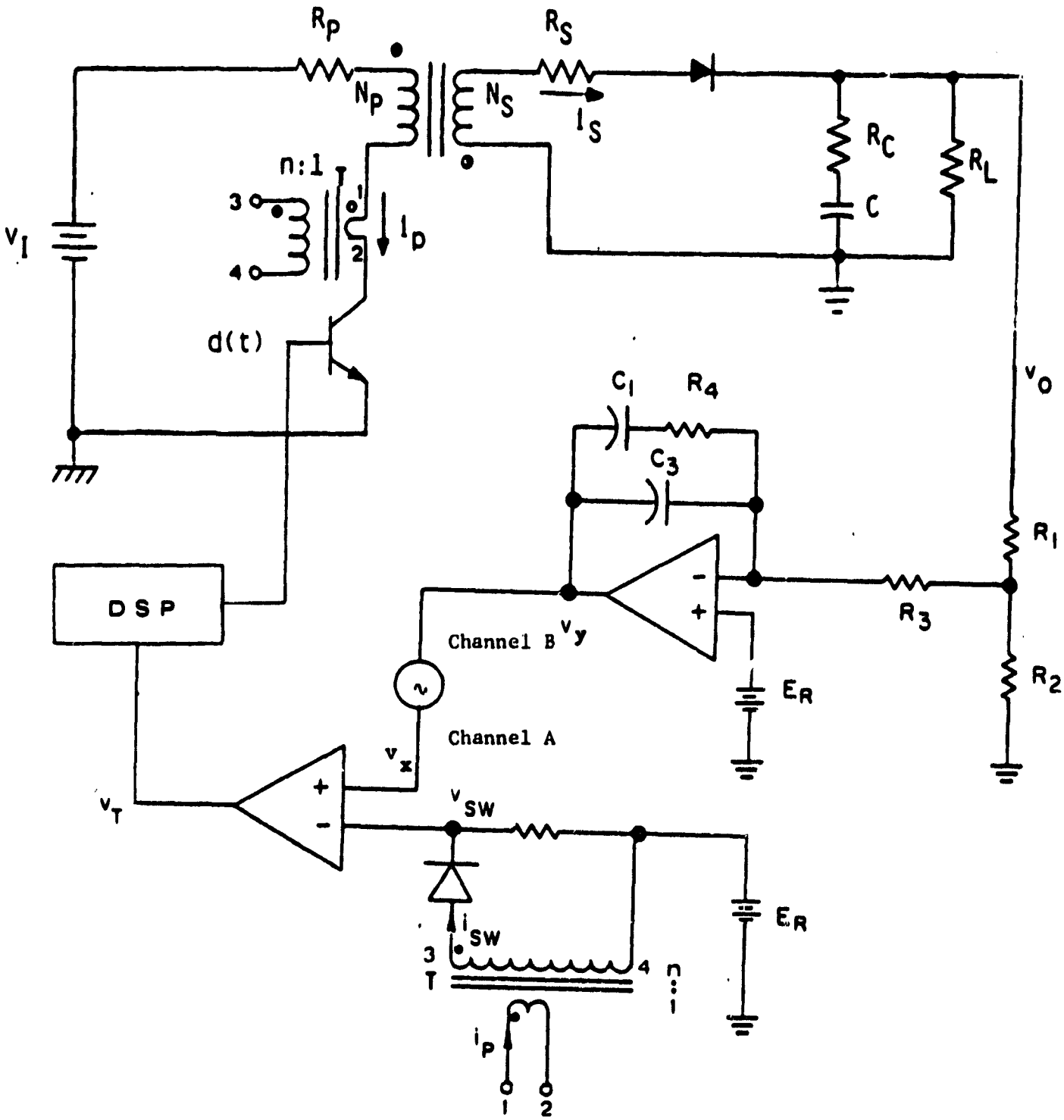


Fig. 4.5.3.2. Measurement technique for dc open loop response.

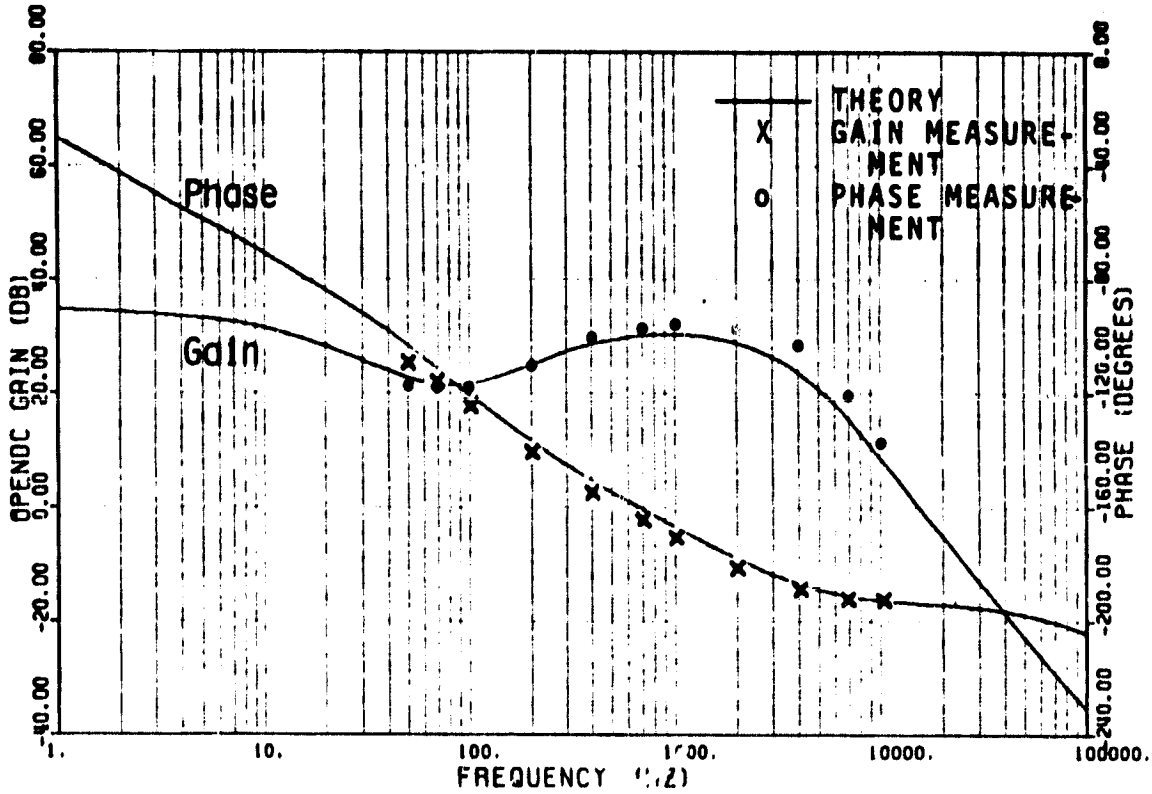


Fig. 4.5.3.3. Theory and measurement of dc open loop characteristics.

logic level signal. Even for the modified equivalent circuit as shown in Fig. 4.3.2.1, the signal v_T' contains both digital and analog information. By opening the loop at v_T of Fig. 4.3.1.1 or v_T' of Fig. 4.3.2.1 the measurement of small-signal gain and phase would lose its physical meaning. For this reason, only the analytical solution for the system open-loop response is given. Fig. 4.5.4.1 shows the block diagram for the system open-loop response.

From the Fig. 4.5.4.1 the system open-loop response can be derived. The resulting equation is given below:

$$G_{OL} = \frac{F_M}{\Delta} [F_{DC}F_{D1} + F_{AC}F_{D2}] \tag{4.5.4.1}$$

Substituting the converter gain expressions (4.2.3.12), (4.3.2.16), (4.3.2.17) and (4.4.3.41) into (4.5.4.1), the following formulation results:

$$G_{OL} = \frac{F_M}{s^2+2\zeta\omega_o s+\omega_o^2} \left\{ \frac{1}{(C_1+C_3)s} \left[\frac{1+sR_4C_1}{1+sR_4\left(\frac{C_1C_3}{C_1+C_3}\right)} \right] \left[\frac{GP}{R_1} \right] \right.$$

$$\frac{V_0\omega_o^2}{DD'} (R_CCs+1) \left[1 - \frac{D}{R_L} (L_es+R_{eq}) \right] + F_{AC} \frac{V_0N_S}{R_LN_P} \left[\frac{1}{L_SC} (R_LCs+D+1) \right.$$

$$\left. \left. + \frac{s^2+2\zeta\omega_o s+\omega_o^2}{D'} \right] \right\} . \tag{4.5.4.2}$$

with $\frac{DR_{eq}}{R_L} << 1$, equation (4.5.4.2) is simplified yielding:

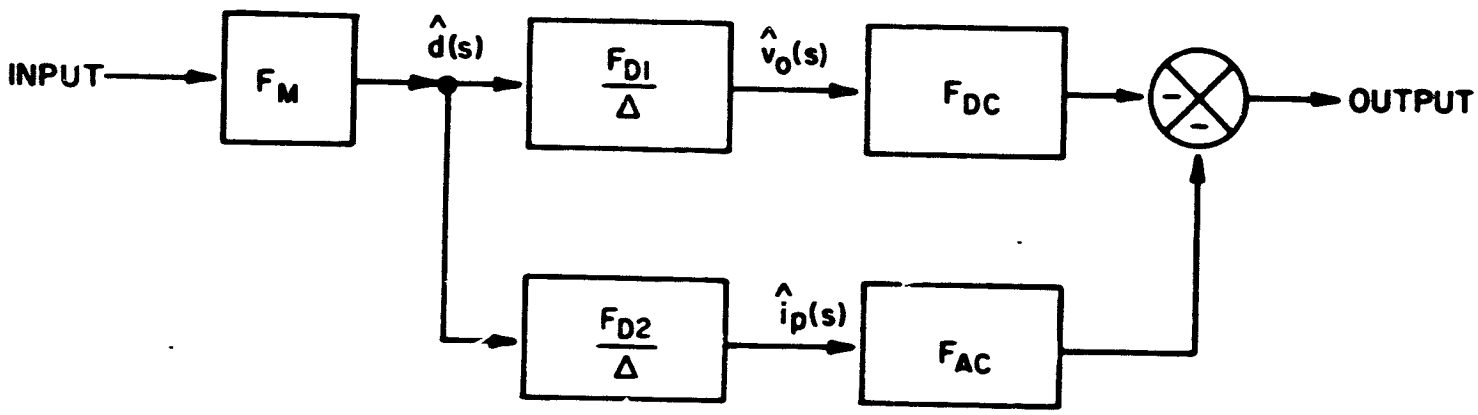


Fig. 4.5.4.1. System open-loop block diagram.

$$G_{OL} = \frac{F_M V_0 \omega_o^2}{DD'} \frac{1}{s^2+2\zeta\omega_o s+\omega_o^2} \left\{ \frac{-\zeta P}{(C_1+C_3)R_1 S} \left(\frac{1+sR_4C_1}{1+sR_4\left(\frac{C_1C_3}{C_1+C_3}\right)} \right) \right.$$

$$\left. \left(\frac{DL_e}{R_L} s - 1 \right) + \frac{F_{AC} N_S D}{R_L N_p \omega_o^2} \left(s^2 + \left(\frac{R_L D'}{L_S} + 2\zeta\omega_o \right) s + \frac{2D'}{L_S C} \right) \right\}$$

(4.5.4.3)

Equation (4.5.4.3) is the system open-loop transfer function in general form. The expression will be further simplified in chapter six.

The analytical waveforms for the gain and phase response are shown in Fig. 4.5.4.2. It is interesting to point out that the system open-loop gain approaches a constant value and the phase delay approaches zero as frequency increases to a high value. This characteristic has made the current injected control unique in comparison with any other type of control. High-gain, wide-bandwidth and stable operation could be accomplished simultaneously. In the analytical model, the pulse modulator gain is assumed constant with no phase delay. However, it is pointed out in reference [ ] that the reduction of pulse modulator gain together with an increase of the phase delay was observed in laboratory measurement. Having incorporated the non-constant gain and phase delay of pulse modulator model in the system open-loop characteristic, the gain characteristic would carry a certain slope and the phase delay would not be approaching zero.

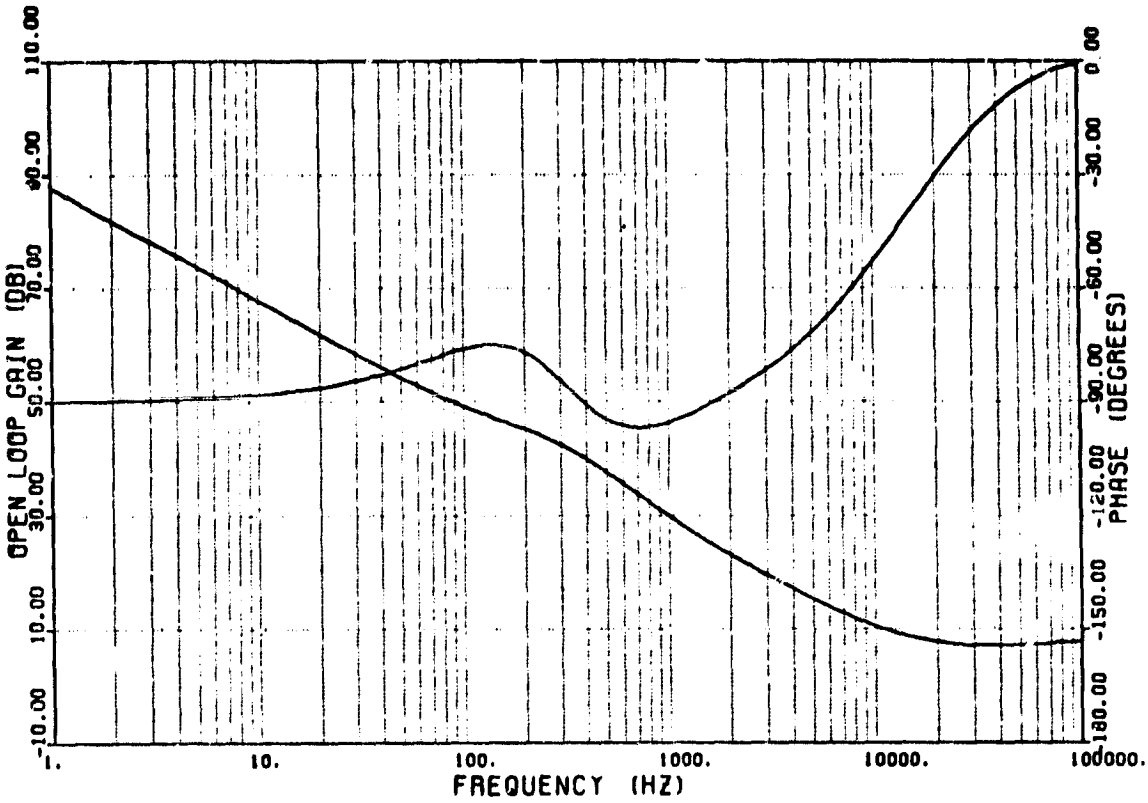

110.00
90.00
70.00
50.00
30.00
10.00
-10.00
OPEN LOOP GAIN (DB)
0.00
-30.00
-60.00
-90.00
-120.00
-150.00
-180.00
PHASE (DEGREES)
1.
10.
100.
1000.
10000.
100000.
FREQUENCY (HZ)

Figure 4.5.4.2

4.5.5 Audiosusceptibility

Audiosusceptibility is the closed-loop, input-to-output response for the dc-dc converter. The audiosusceptibility characteristic is used to evaluate the rejection rate of the propagation of a sinusoidal disturbance from converter input to output. Figure 4.5.5.1 illustrates the block diagram for the closed-loop analysis of the current-injected regulator. The expression obtained by examining Fig. 4.5.5.1 is the following:

$$\frac{\hat{v}_o(s)}{\hat{v}_i(s)} = \frac{\frac{F_{u11}}{\Delta}\left[1+\frac{F_M F_{AC} F_{D2}}{\Delta}\right] - \frac{F_{D1} F_M F_{AC} F_{u21}}{\Delta^2}}{1+\frac{F_M F_{AC} F_{D2}}{\Delta}+\frac{F_{D1} F_M F_{DC}}{\Delta}} \qquad (4.5.5.1)$$

In equation (4.5.5.1), the denominator can be expressed in terms of the system open-loop response G_{OL}. After substituting equation (4.5.4.1) into (4.5.5.1) the following expression is given:

$$\frac{\hat{v}_o(s)}{\hat{v}_i(s)} = \frac{F_{u11}(\Delta + F_M F_{AC} F_{D2}) - F_{D1} F_M F_{AC} F_{u21}}{\Delta^2\,(1+G_{OL})} \qquad (4.5.5.2)$$

The general form for the closed-loop transfer function can be expressed by substituting equations (4.2.3.12), (4.3.2.16), (4.3.2.17) (4.4.3.41) and (4.5.4.3) into equation (4.5.5.2).

$$\frac{\hat{v}_o(s)}{\hat{v}_i(s)} = \left\{ \frac{N_S D}{N_P D'}\,\omega_o^2\,(R_C Cs+1)\left[s^2+2\zeta\omega_o s+\omega_o^2+F_M F_{AC}\frac{V_o N_S}{R_L N_P}\left(\frac{1}{L_S C}(R_L Cs+D+1)+\frac{s^2+2\zeta\omega_o s+\omega_o^2}{D'}\right)\right] + \frac{F_M F_{AC} V_O D\,\omega_o^2}{D' L_P R_L C}(R_C Cs+1)\left(\frac{DL_e}{R_L}s-1\right)(R_L Cs+1)\right\} \cdot$$

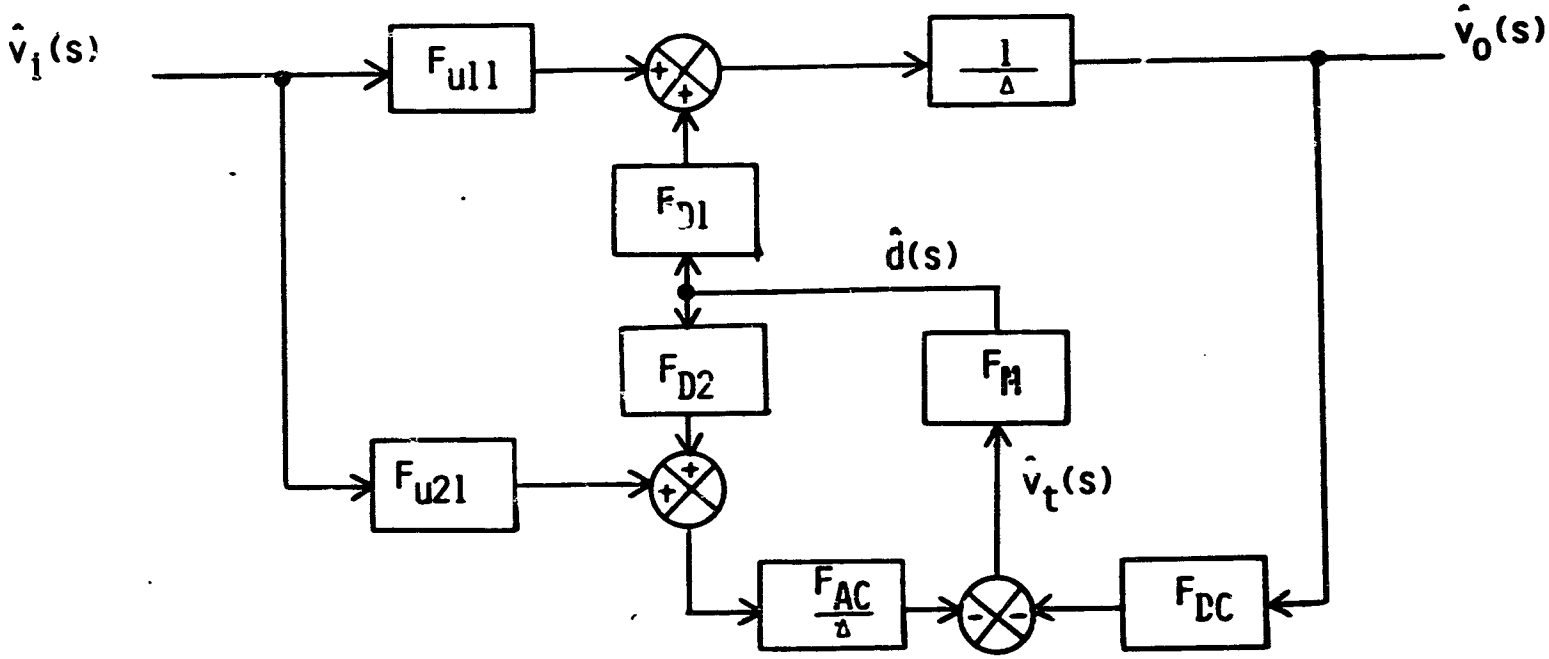


Fig. 4.5.5.1. Audiosusceptibility block diagram.

$$\frac{1}{\Delta^2 + \frac{F_M V_0 \omega_o^2}{DD'}(s^2 + 2\zeta\omega_o s + \omega_o^2)\left\{\frac{-GP}{(C_1+C_3)R_1 S}\left(\frac{1+sR_4C_1}{1+sR_4\left(\frac{C_1C_3}{C_1+C_3}\right)}\right)\left[\frac{DL_e}{R_L}s-1\right]\cdot\left[R_cCS+1\right] + \frac{F_{AC}N_S D}{R_L N_P \omega_o^2}\left[s^2 + \left(\frac{R_L D'}{L_S} + 2\zeta\omega_o\right)s + \frac{2D'}{L_S C}\right]\right\}} \qquad (4.5.5.3)$$

Equation (4.5.5.3) will be simplified in chapter six.

4.5.5.1 Test Verification for Audiosusceptibility

The audiosusceptibility measurements are taken by injecting an ac signal in series with the input voltage of the converter, accomplished by injecting the perturbation through a transformer whose secondary winding is in series with the supply voltage. Figure 4.5.5.2 demonstates how the measurement technique is implemented.

Fig. 4.5.5.3 illustrates the gain curves for equation (4.5.5.3) for the current-injected regulator. The analytical curves are portrayed by the solid lines and the experimental result is represented by the × curve.

4.5.6 Output Impedance

The output impedance is employed to measure the dynamic performance of a switching regulator subjected to sinusoidal load disturbance. A switching regulator with zero output impedance represents an ideal voltage source. In a linear system, the output impedance is often used to analyze transient response. When a switching regulator is subjected to a small step-change in load, the output voltage normally varies only

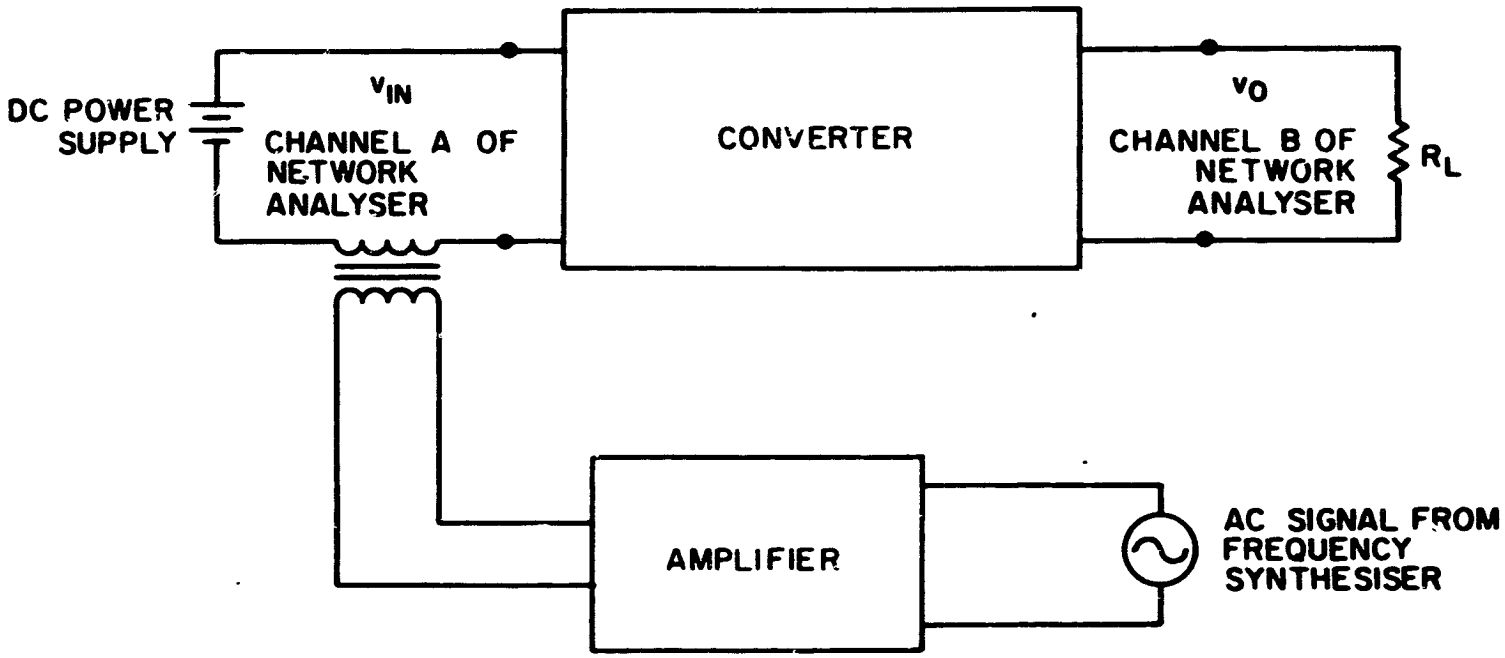


Fig. 4.5.5.2. Measurement technique for audiosusceptibility.

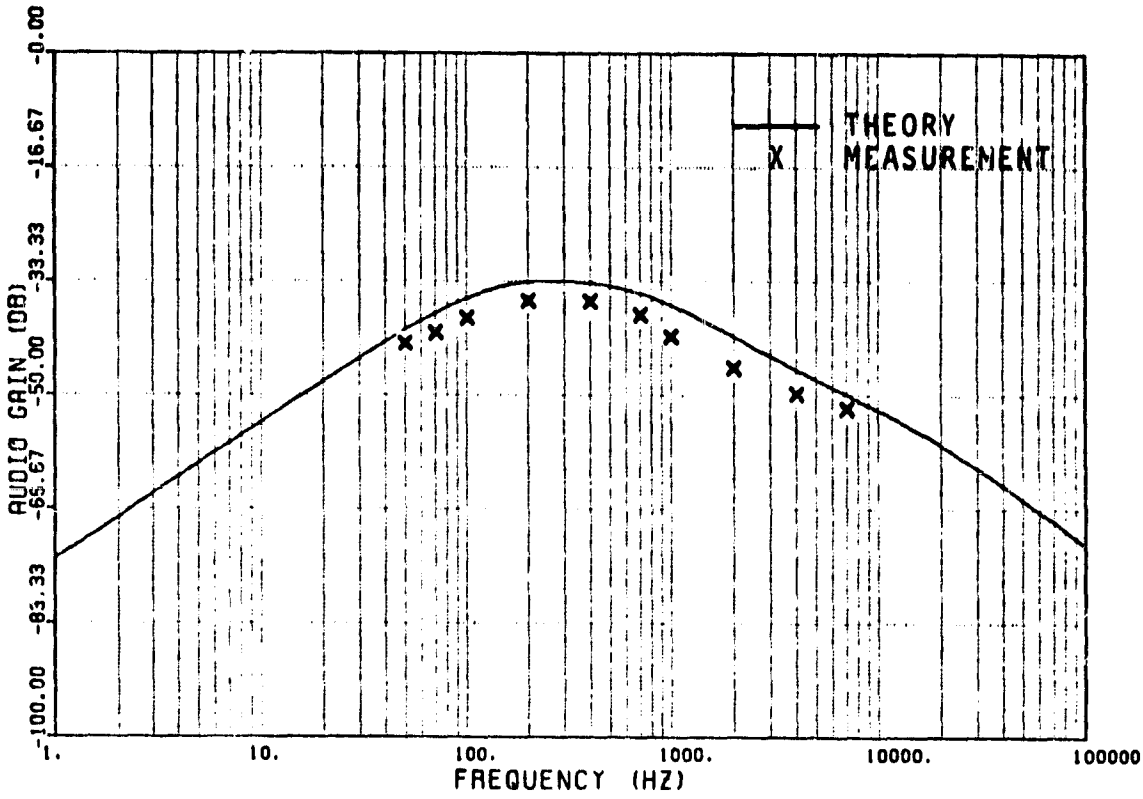


Fig. 4.5.5.3. Theory and measurement of audiosusceptibility characteristics.

slightly. If the duty ratio is regarded as a constant during the load transient, the linear average model that characterizes the converter at a given quiescent point remains valid. [24,25,26].

The output impedance of the converter is defined as the ratio $\frac{\hat{v}_o(s)}{\hat{i}_o(s)}$, where $\hat{i}_o(s)$ is the sinusoidal disturbance at the converter output. The output impedance characteristic of an open-loop regulator usually has its maximum value at the output filter resonance frequency. This undesirable result can be reduced by effectively designing the feedback parameters of the control loop as will be shown in chapter six. The block diagram for the output impedance is illustrated in Fig. 4.5.6.1.

Using Mason's gain formula or a block reduction method the ratio $\frac{\hat{v}_o(s)}{\hat{i}_o(s)}$ reduces to the following form:

$$\frac{\hat{v}_o(s)}{\hat{i}_o(s)} = \frac{F_{u12}\,(\Delta + F_M F_{AC} F_{D2}) - F_M F_{AC} F_{u22} F_{D1}}{\Delta\,(\Delta + F_M(F_{D1} F_{DC} + F_{AC} F_{D2}))} \tag{4.5.6.1}$$

The general form for the output impedance transfer functions can be evaluated by substituting equations (4.2.3.12), 4.3.2.16), (4.3.2.17), (4.3.41), and (4.5.4.3) into equation (4.5.6.1).

$$\frac{\hat{v}_o(s)}{i_o(s)} = \frac{R_C(s^2+z_1 s+z_2\omega_o^2)\left[\Delta+F_M F_{AC}\frac{V_O N_S}{R_L N_P}\left(\frac{R_L Cs+D+1}{L_s C}+\frac{D}{D'}\right)\right.}{\Delta^2+\frac{F_M V_O \omega_o^2}{DD'}\left[\frac{-GP}{(C_1+C_3)R_1 S}\left[\frac{1+SR_4C_1}{1+SR_4(C_1/\!/\,C_3)}\right](R_C Cs+1)\left[\frac{DL_e}{R_L}s-1\right]\right.}$$

$$\frac{\left.-F_M F_{AC}\frac{V_O N_S}{D'^2 N_P}\omega_o^4(R_C Cs+1)\left(\frac{DL_e}{R_L}s-1\right)\right]}{\left.+\frac{F_{AC}N_S D}{R_L N_P \omega_o^2}\left(s^2+\left[\frac{R_L D'}{L_S}+2\zeta\omega_o\right]s+\frac{2D'}{L_S C}\right)\right\}} \tag{4.5.6.2}$$

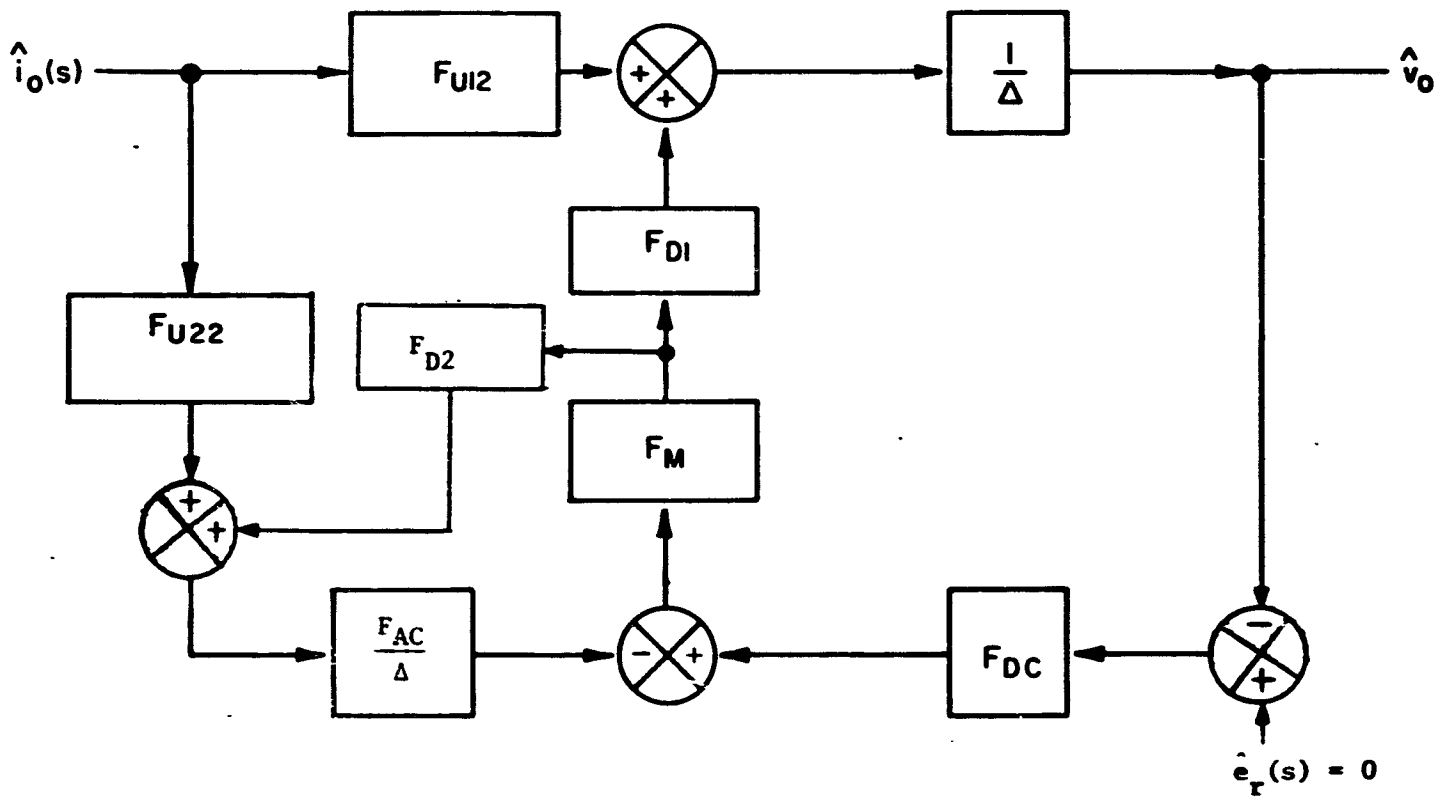


Fig. 4.5.6.1. Output impedance block diagram.

4.5.6.1 Test Verification for Output Impedance

Fig. 4.5.6.2 illustrates the method implemented to measure the output impedance. A voltage source with a one-hundred ohm resistor in series stitutes the current source equivalent. Channel A reads the input disturbance current $\hat{i}_o$, and channel B measures the perturbed response $\hat{v}_o$. In generating the theoretical response, the symble R_{LOAD} is used for the load impedance instead of R_L. R_{LOAD} is defined by the following:

$$R_{LOAD} = R_L//101.0 \qquad (4.5.6.3)$$

The theoretical and measured response are shown together in Fig. 4.5.6.3. The solid curve is the theoretical output impedance and the curve marked "x" is the measured response.

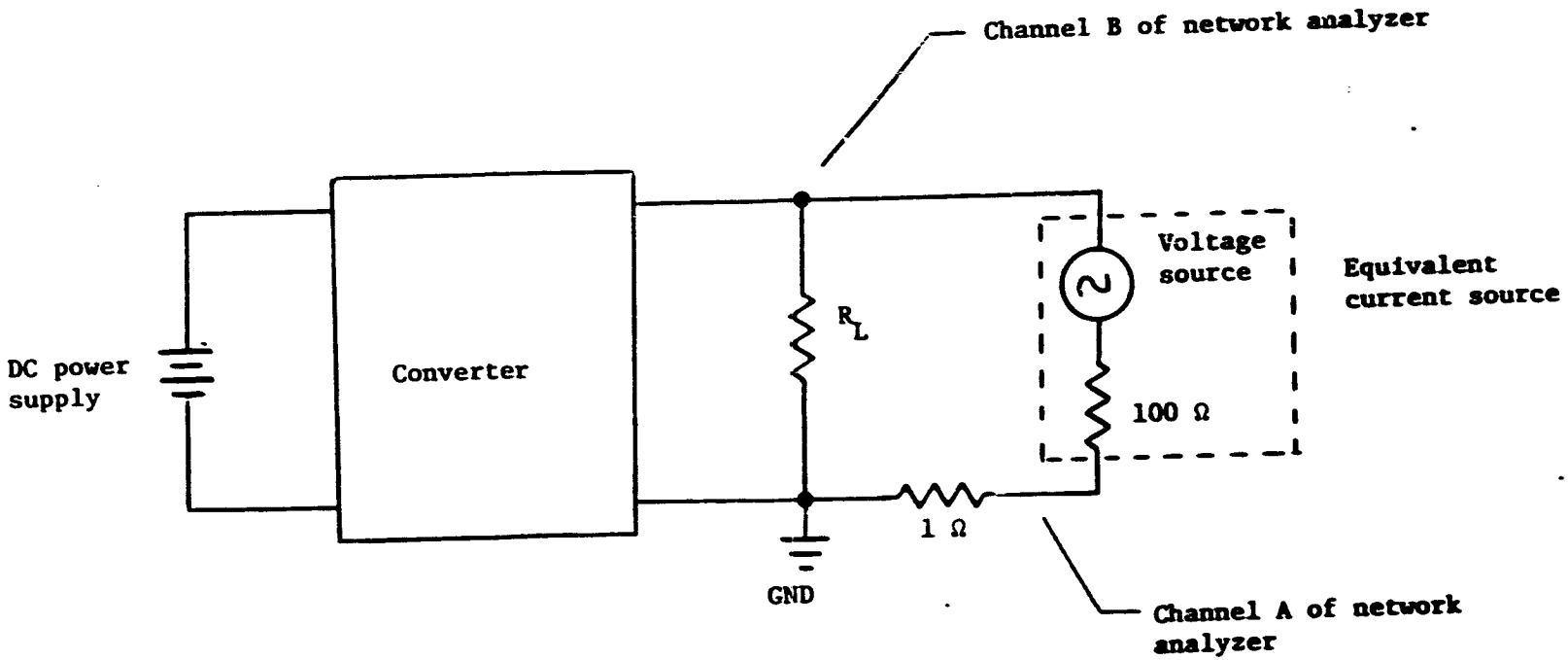


Fig. 4.5.6.2. Measurement technique for the output impedance.

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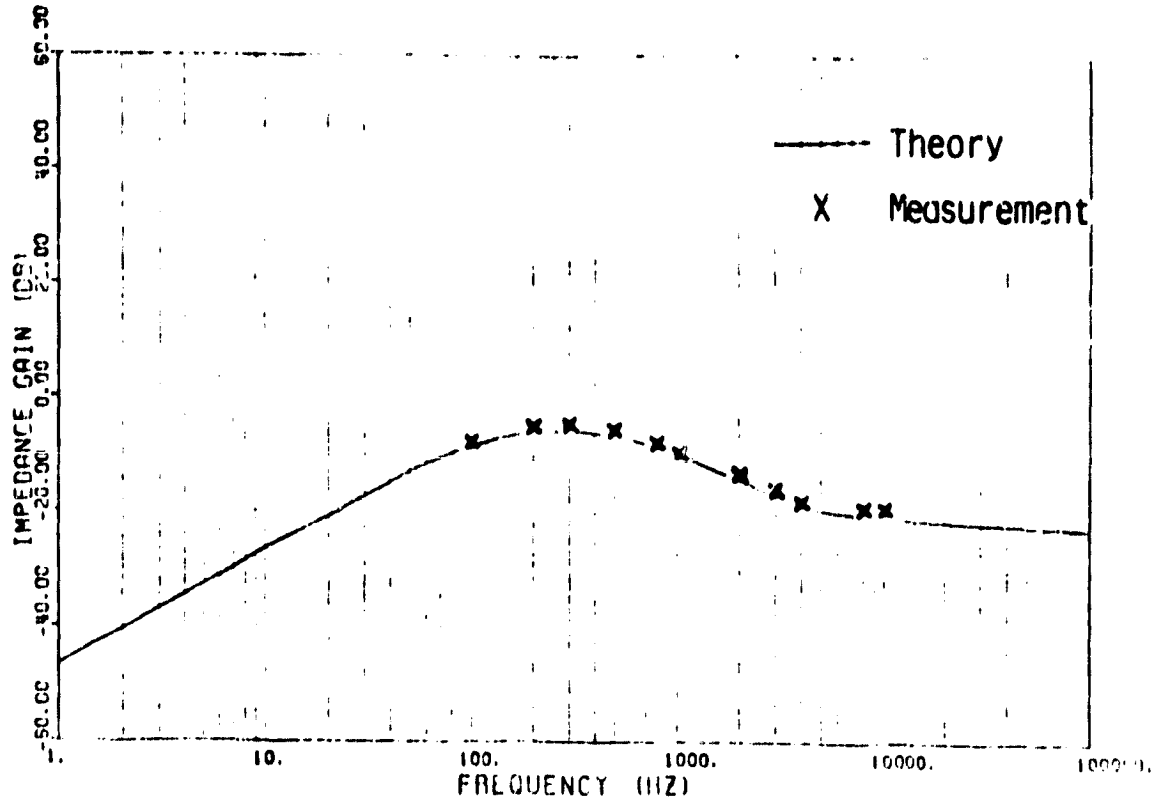

Figure 4.5.6.3 Theory and measurement of the output impedance characteristic.

4.6. PERFORMANCE EVALUATIONS AND CONTROL DESIGN

4.6.1 Introduction

The stability and dynamic performance of the current-injected switching regulator are examined. A critical look at the small-signal, open-loop, and closed-loop responses allows for a qualitative and quantitative understanding of the control-to-output transfer function $\frac{\hat{v}_o}{\hat{v}_x}$, dc open-loop response G_{DL}, system open-loop characteristics G_{OL}, and the close-loop behavior $\frac{\hat{v}_o}{\hat{v}_i}$. Also presented in this chapter are parametric studies on the behavior of system responses by varying certain "key" control variables in the feedback loops. These studies in turn egnerate information on how the ac and dc feedback-loops effect the stability, audiosusceptibility, andother important design features. After collating all the above mentioned information, some design guidelines are set forth for the dc and ac feedback-loop parameters.

4.6.2 Discussion of the Control-To-Output Characteristic

Referring to equation (4.5.2.4), the following expression can be written:

$$\frac{\hat{v}_o(s)}{\hat{v}_x(s)} = -\frac{F_P R_L N_P \omega_o^2}{F_{AC} N_S} \frac{(R_C C s + 1)\left(\frac{DL_e}{R_L} s - 1\right)}{s^2 + \left(2\zeta\omega_o + F_P \frac{R_L}{L_S}\right) s + \omega_o^2 \left(1 + F_P \frac{(D+1)}{D'^2}\right)}$$

$$\text{where} \quad F_P = \frac{1}{\frac{1}{D'} + \frac{R_L T_F}{2L_S}\left(1 + \frac{D'}{D}\right)} \triangleq \frac{FD'}{F + D'} \qquad (4.6.2.1)$$

Equation (4.6.2.1) is reduced in the following manner, assume the second order polynomial of equation (4.6.2.1) is represented by:

$$(s + \alpha)(s + \beta) = s^2 + (\alpha + \beta) \cdot s + \alpha\beta \qquad (4.6.2.2)$$

If $\alpha >> \beta$ then equation 4.6.2.2 yields the following approximation:

$$(s + \alpha)\ (s + \beta) \simeq s^2 + \alpha s + \alpha\beta \tag{4.6.2.3}$$

With the resulting approximation, the second order polynomial simply factors into the following:

$$s + \alpha = s + 2\zeta\omega_o + \frac{F_P R_L}{L_S} \tag{4.6.2.4}$$

$$s + \beta = s + \frac{\omega_o^2 \left(1 + F_P \frac{(D+1)}{D'^2}\right)}{2\zeta\omega_o + \frac{F_P R_L}{L_S}} \tag{4.6.2.5}$$

Substituting equations (4.6.2.4) and (4.6.2.5) for the second order polynominal generates the simplified version given by,

$$\frac{\hat{v}_o(s)}{\hat{v}_x(s)} = \frac{-F_P R_L N_P \omega_o^2}{F_{AC} N_S} \quad \frac{(R_C C s + 1)\left(\frac{DL_e}{R_L} s - 1\right)}{\left(s + 2\zeta\omega_o + \frac{F_P R_L}{L_S}\right)\left(s + \frac{\omega_o^2 \left(1 + F_P \frac{(D+1)}{D'^2}\right)}{2\zeta\omega_o + \frac{F_P R_L}{L_S}}\right)} \tag{4.6.2.6}$$

The justification for the approximation is proven by substituting the parameter values of the tested model into equation (4.6.1.6)

$$\frac{\hat{v}_o(s)}{\hat{v}_x(s)} = .021 \quad \frac{(s + 32.394K)(s - 47.873K)}{(s + 49.376K)(s + 304.86)} \tag{4.6.2.7}$$

with α=49.376K and β=304.86, $\alpha >> \beta$, equation (4.6.2.6) is a good approximation. The pole/zero plot for equation (4.6.2.7) is given in Fig. 4.6.2.1. For small-signal analysis the power stage parameters are given in Chapter 4.5.

The control-to-output characteristic does not include the dc feedback-loop parameters and com[illegible]ion network parameters: however, it does include the

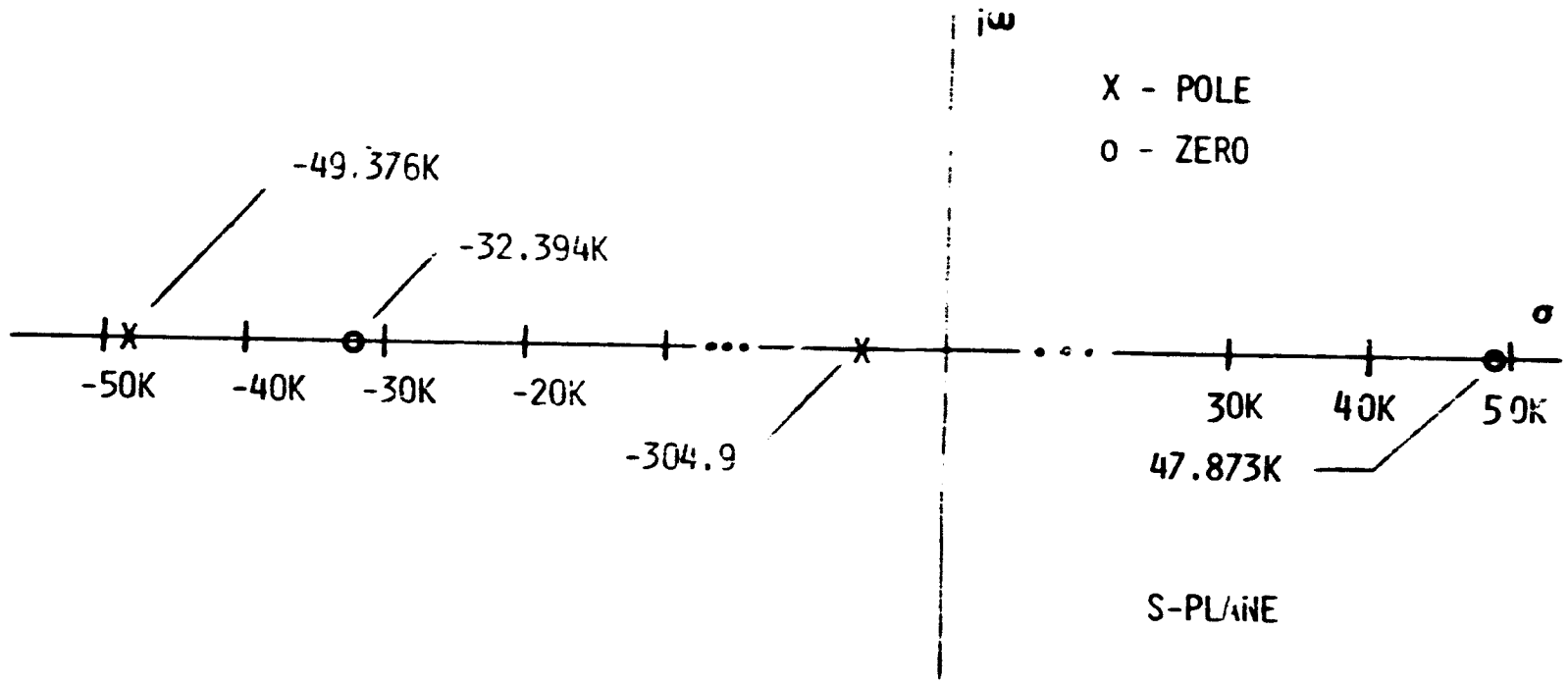

Fig. 4.6.2.1 $\hat{v}_o/\hat{v}_x$ POLE/ZERO PLOT

ac feedback loop parameters. The control-to-output transfer function consists of two poles and two zeros. It is interesting to compare this transfer function with that developed at Caltech (following a different modeling approach) which consists only of a single pole and single zero [20]. Although these two transfer functions are similar in the qualitative nature, yet there exists an important difference which can be illustrated by examining the asymptotic curves of the bode plots. In Fig. 4.6.2.2, notice the dip in the gain curve around 6KHz before leveling off as the frequency increases. This second-order effect could become more pronounced with a greater pole/zero separation. A similar effect can be seen in the phase plot of the control-to-output expression. This second order effect is demonstrated as the load parameter R_L increases forcing the current to approach the discontinuous mode; a noticeable change in the phase response of the control-to-output response occurs. Fig. 4.5.2.3 illustrates the control-to-output response for $R_L = 15\Omega$. With $R_L = 40\Omega$ the theoretical and phase as shown in Fig. 4.6.2.4 definitely has a second zero which is pulling the phase up. This second order effect around six to eight kilohertz cannot be explained by a single zero/single pole system. From the above discussion, one can conclude that the first-order approximation may be valid for a given range of parameter values. It however, could produce gross error under other parameter values or operating conditions.

4.6.3 DC Open Loop Characteristic and Compensation Network

The dc open-loop response is simply the control-to-output response multiplied by the dc loop gain (F_{DC}). The model for F_{DC} given by equation (4.3.2.16) is a general integral-plus-lead/lag network.

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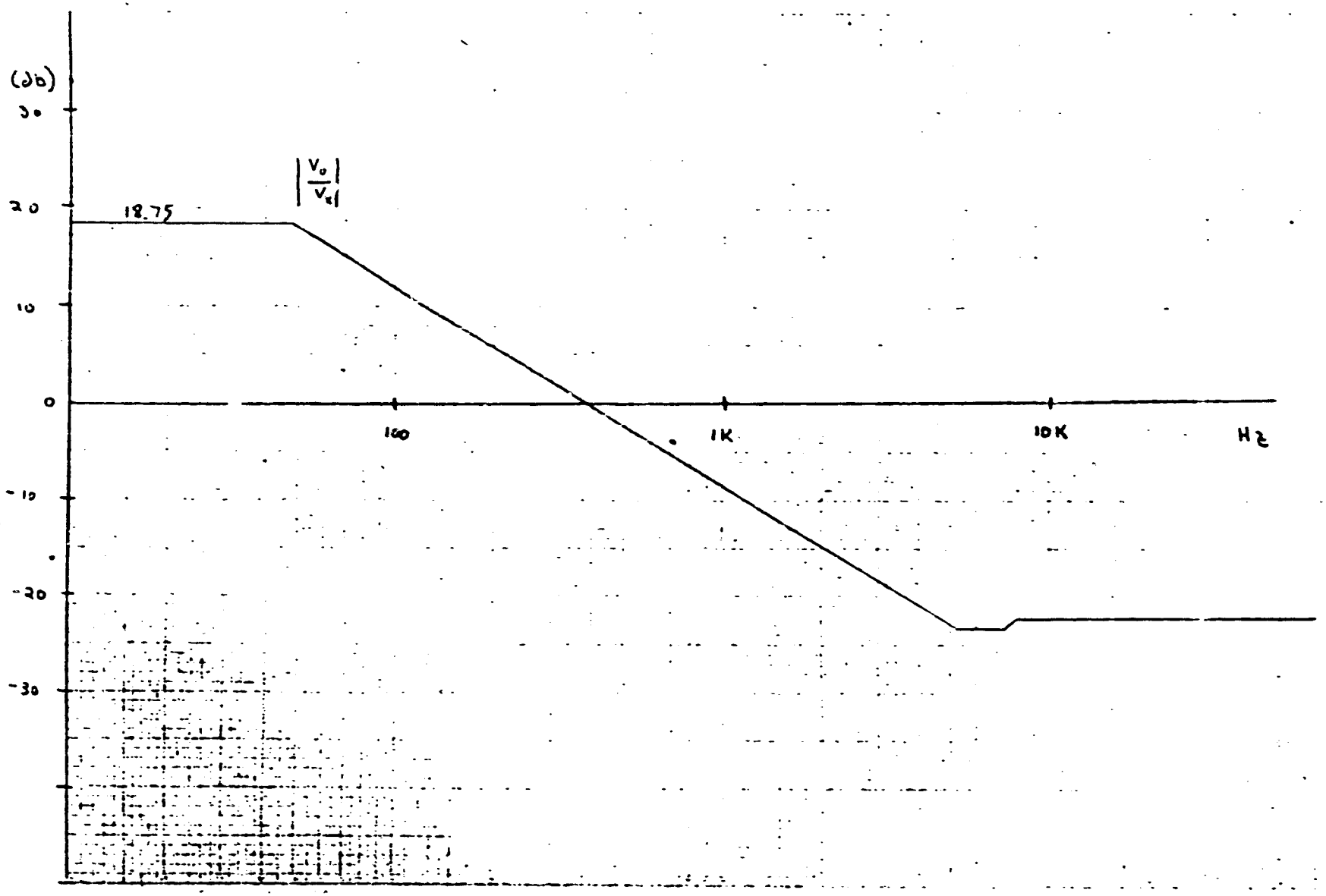

Fig. 4.6.2.2(a) $\frac{\hat{v}_o}{\hat{v}_x}$ Gain Plot

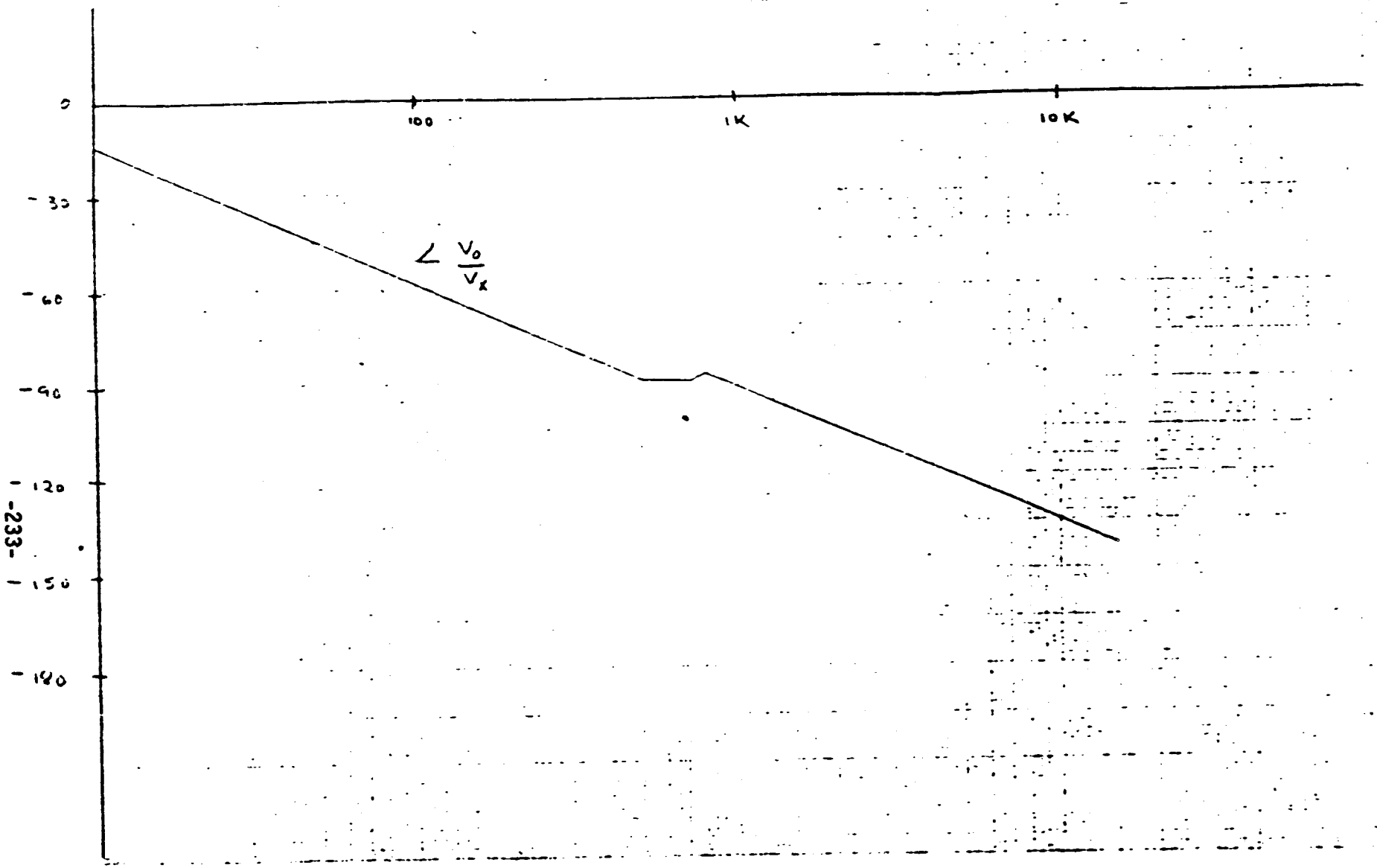

Fig. 4.6.2.2(b) $\frac{\hat{V}_o}{\hat{V}_x}$ Phase Plot

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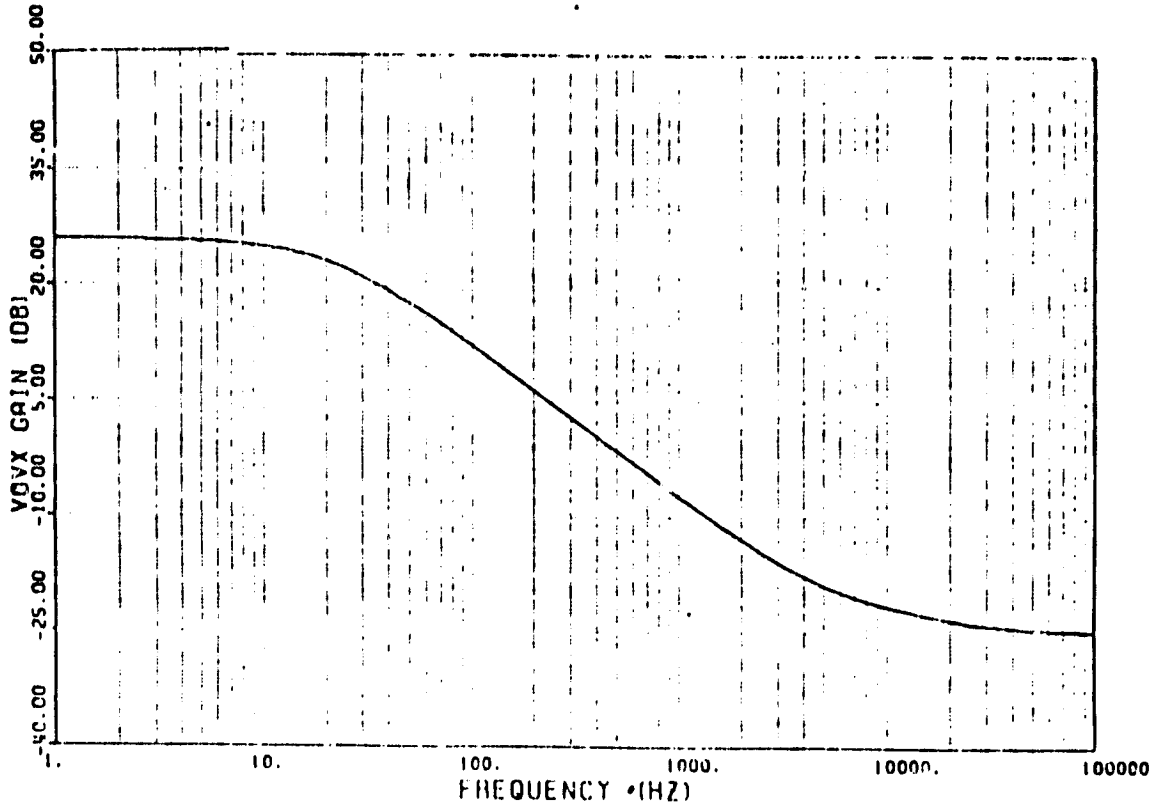
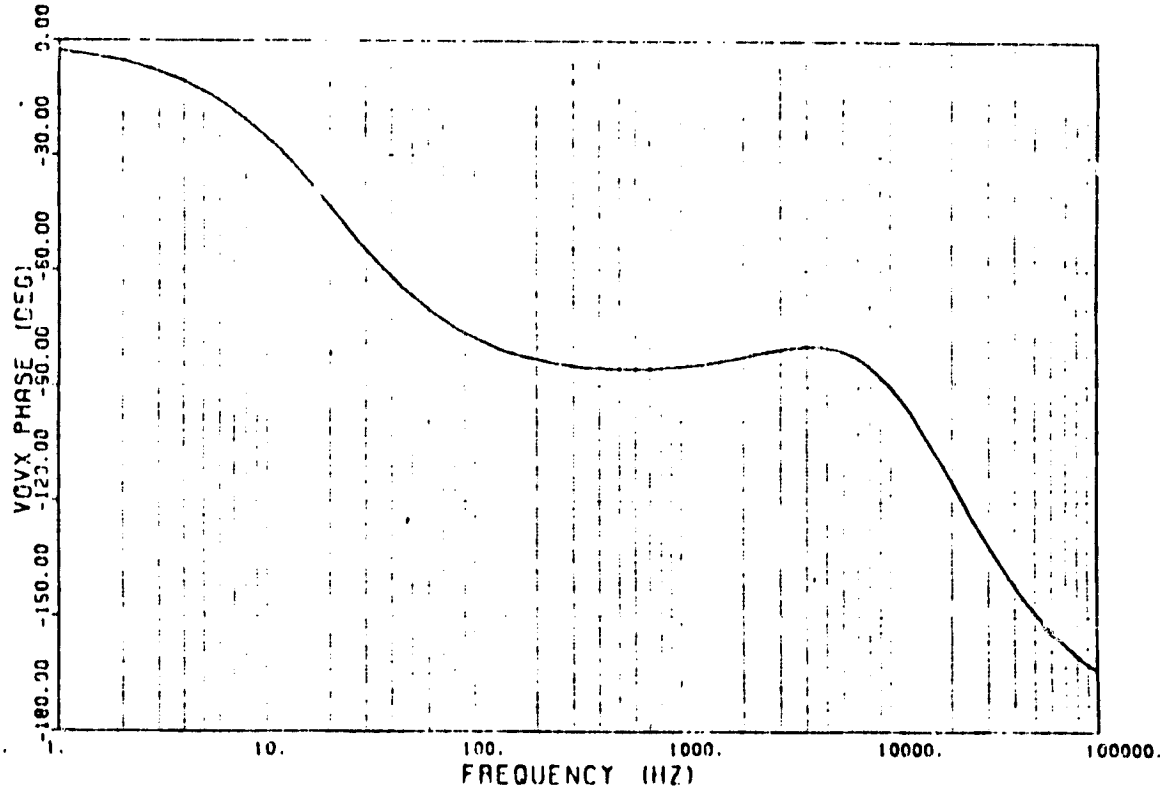


(a)



(b)

Fig. 4.6.2.3 (a) Gain and
(b) Phase Response for The Control- Input-Output Characteristics

Illustrated in Figures 4.6.3.1 (a) and (b) are two commonly used integral-plus-lead/lag networks derived from Fig. 4.3.1.1. Fig. 4.6.3.1 (a) and (b) are quivalent dc loop compensation networks. The transfer function for compensation network A, as derived from the generalized expression, is

$$F_{DC}\Big|_A = \frac{GP}{R_1}\,\frac{1}{(C_1 + C_3)\,s}\,\frac{1 + sR_4C_2}{1 + sR_4C_2//C_3} \qquad (4.6.3.1)$$

$$\simeq \frac{GP}{R_1C_1s}\,\frac{1 + sR_4C_2}{1 + sR_4C_3}$$

if $C_3 << C_2$,

Where $G_P = \left(1 + \frac{R3}{R_1} + \frac{R3}{R_2}\right)^{-1}$

and compensation network B can be modeled by the following expression:

$$F_{DC}\Big|_B = \frac{GP}{R_1\,C_1\,s}\,\frac{1 + sC_2\left(\frac{R_1}{G_P} + R_5\right)}{1 + sR_5C_2} \qquad (4.6.3.2)$$

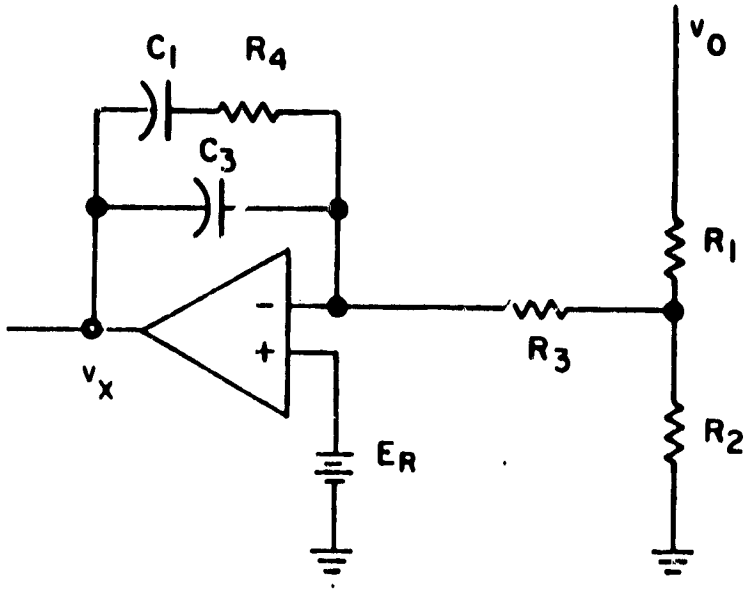
$$\simeq \frac{GP}{R_1\,C_1\,s}\,\frac{1 + sC_2\,\frac{R_1}{G_P}}{1 + sR_5C_2}$$

if $\frac{R_1}{GP} >> R_5$.

With network A the lead/lag corner frequencies are independently adjusted by changing the capacitance values C_1 and C_3; in network B the same is accomplished by varying the resistive values $\frac{R_1}{GP}$ and R_5. Neither network has any particular advantage over the other. For the discussion of the dc open loop characteristics network A is chosen.

Compensation network A has a single-zero/two-pole transfer characteristic which provides an integral plus lead/lag compensation. Fig. 4.6.3.2 shows the gain response of network A with respect to parameter variations in resistor R_4 and capacitors C_1 and C_3. Capacitor C_1 alters the lead-

COMPENSATION NETWORK A



COMPENSATION NETWORK B

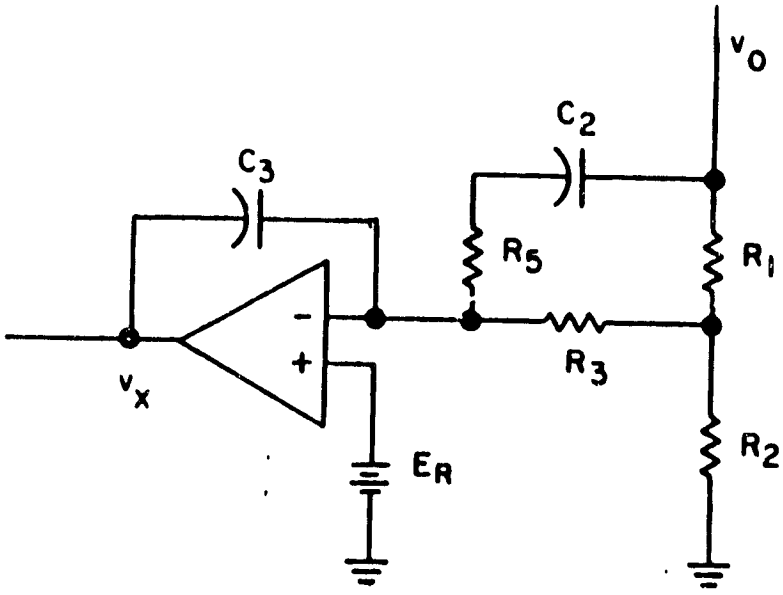
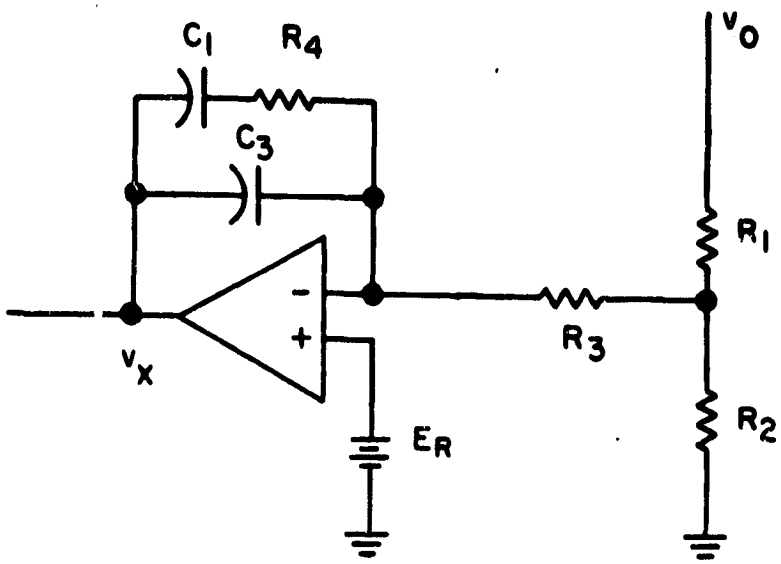


Fig. 4.6.3.1. Current-injected control modeling approach.

COMPENSATION NETWORK A



$$F_{DC} \simeq \frac{G_P}{R_1 C_1 S} \; \frac{1 + SR_4 C_1}{1 + SR_4 C_3} \quad (\text{if } C_1 >> C_3)$$

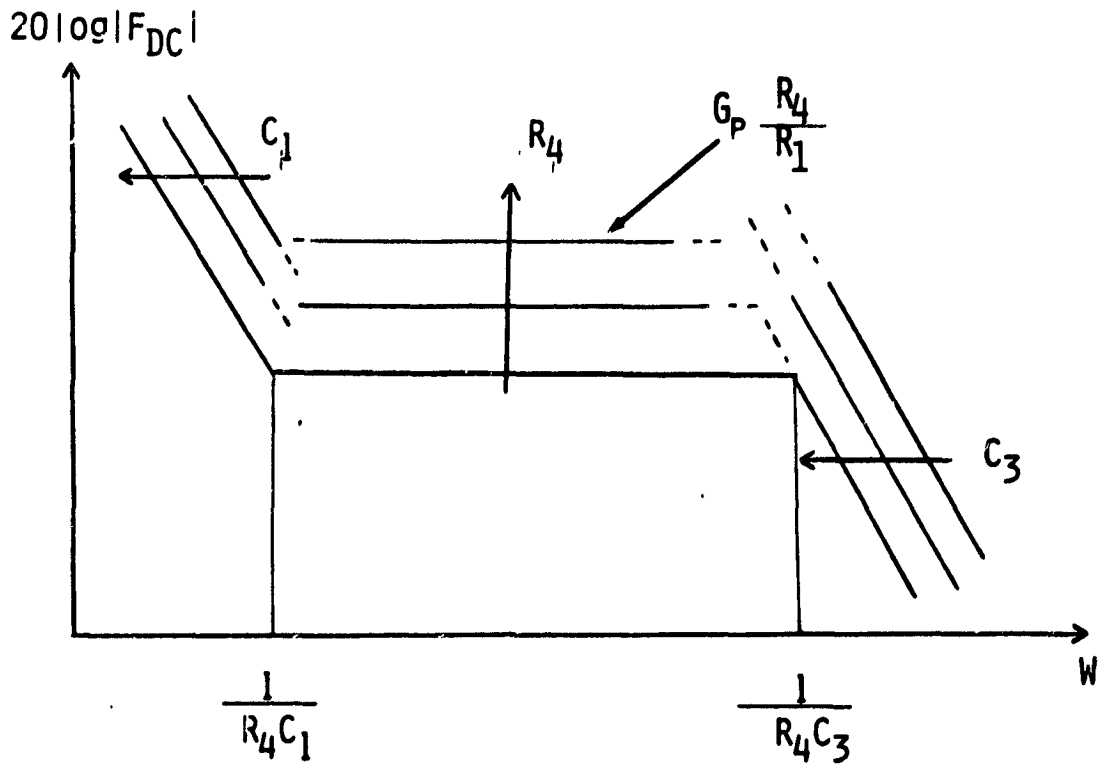


Fig. 4.6.3.2. Dc loop compensation.

corner frequency. Larger values of C_1 generate a lower crossover frequency as indicated by the arrow in Fig.4.6.3.2. Increasing R_4 forces the mid-frequency gain to increase while decreasing values of C_3 reduces the lag crossover frequency. Similarly, increasing G_P (or reducing R_3) causes the overall dc loop gain to increase. The dc loop response can be reshaped to any desirable characteristic by varying these parameters. The relationship of the open dc loop characteristic to the closed-loop system response will be discussed in section 4.6.6.

Using equation (4.6.3.1) as the expression for F_{DC}, the dc open-loop response described by equation (4.5.3.2) is simplified as follows:

$$G_{DL} \simeq \text{CONST} \frac{(R_C C\ s + 1)(R_4 C_1 s + 1)(\frac{DL_e}{R_L} s - 1)}{s(R_4 C_3 s + 1)\left(s + 2\zeta\omega_o + \frac{F_P R_L}{L_S}\right)\left(s + \frac{\omega_o^2(1 + F_P \frac{D+1}{D'^2})}{2\zeta\omega_o + \frac{F_P R_L}{L_S}}\right)} \qquad (4.6.3.3)$$

$$\text{where CONST} = \frac{F_P \omega_o^2 G P R_L N_P}{F_{AC} D D' R_1 C_1 N_S}$$

The pole/zero plot for the DC open loop transfer function with the converter parameter values given in section 4.5.1 is shown below in Fig. 4.6.3.3.

4.6.4 System Stability and Its Interpretation

As discussed in section 4.5.4, the <u>true</u> system open-loop response cannot be experimentally measured, but the dc open loop response can be measured. In Caltech's modeling approach [20], the ac loop is lumped into the power stage and a small-signal system model is derived which consists of a "new" power stage and a dc feedback loop as shown in Fig.4.6.4.1. While the dc feedback loop remains in its original form, the "new" power stage in effect incorporates both the original power stage and the current-injected loop.

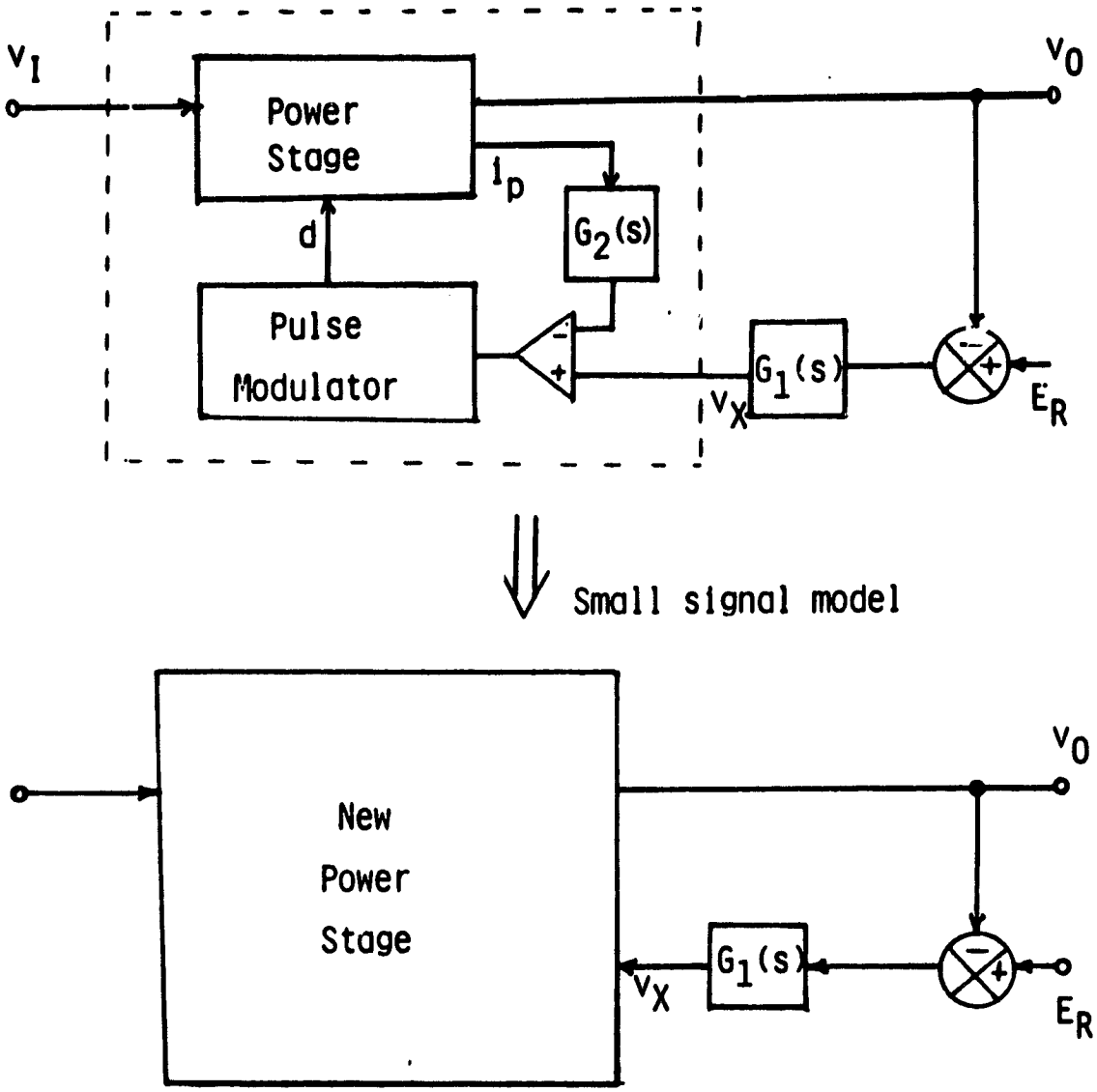


Fig. 4.6.4.1. Current-injected control modeling approach.

Caltech's modeling approach was legitimate and was experimentally verified. Nevertheless, the interpretation of the model has to be exercised with great caution. It is obvious that the open loop response of Fig. 4.6.4.1 is merely the dc open loop characteristics of the original system and not the true open-loop response since the ac loop is embedded in the "new" power stage model. The effect of opening the ac loop cannot be examined using their model. To illustrate, Fig. 4.6.4.2 demonstrates a two-loop system illustrated in a general block diagram fashion. assume that the loop containing H_1 is the ac feedback loop and the loop containing H_2 is the dc feedback loop. The following transfer functions can be easily derived.

Close loop gain: $$\frac{v_0}{v_I} = \frac{GH_2}{1 + G\,(H_1 + H_2)} \qquad (4.6.4.1)$$

Open loog gain at A: $$G_A = G\,(H_1 + H_2) \qquad (4.6.4.2)$$

Open loop gain at B: $$G_B = G\,H_2/\,(1 + G\,H_1) \qquad (4.6.4.3)$$

The system is unstable when the following Nyguist stability criterion is satisfied:

$$G(H_1 + H_2) = -1 \qquad (4.6.4.4)$$

The left-hand side of (4.6.4.4) is identical to the open-loop gain at point A. Examining equation (4.6.4.2), G_A provides both the conditon for stability, and information concerning the relative stability of the system (the phase margin and the gain margin). Examining the open-dc loop characteristic G_B, only when $G_B = -1$ is the condition for instability as given in (4.6.4.4) revealed. Therefore, only at the point of stability is the following expression valid:

$$G_A = G_B = -1$$

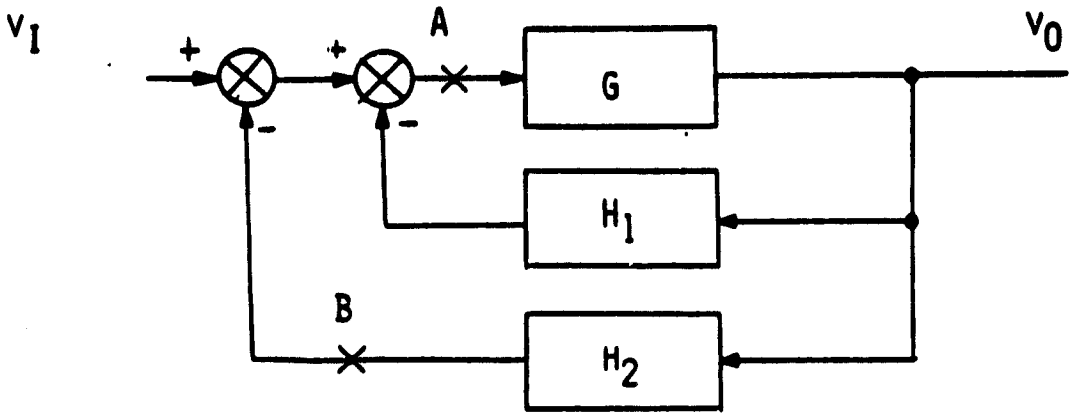


Fig. 4.6.4.2. Generalized two-loop control scheme.

If, however, one employed the open-dc-loop gain G_B to investigate the relative stability of the system (gain margin and phase margin) the conclusions could be very misleading. The point becomes obvious if one examines the dissimilarity of the open-dc-loop response vs. the system open loop response as illustrated in Fig. 4.5.3.3 and Fig. 4.5.4.2, respectively.

In conclusion, although the system open loop response could not be measured experimentally, it provides the only proper way of measuring the relative stability of the system via Bode analysis. It should be noted that, the characteristic equation for system open loop and open-dc loop are, however, the same i.e.

$$1 + G_A = 0 \qquad (4.6.4.5)$$

$$1 + G_B = 0 \qquad (4.6.4.6)$$

Equation (4.6.4.5) and (4.6.4.6) are identical. Therefore the stability could be examined via characteristic roots or eignevalues using either (4.6.4.5) or (4.6.4.6).

4.6.5 System Open Loop Response

The system open loop characteristics can be examined by the small-signal model, but experimental verification of that response is not permissible with the control hardware currently used. The problem is due to the inability to retrieve the ac-modulation-signal information from a "logic level" signal produced by the output of the comparator in the error processor with currently available instrumentation. The comparator output, determined by the control inputs (switching current and the dc error voltage), is the only location where both dc and ac loops can be opened to examine the system response. To check the system open-loop characteristics, the various gain blocks formulating the analytical expression are examined via the control-to-output response and the dc open loop behavior. The expression for the system open loop response G_{OL} as given by equation (4.6.5.1) utilizes the compensation network "A: represented by equation (4.6.3.1).

$$G_{OL} = \frac{F_M}{\Delta}(F_{DC}\,F_{D1} + F_{AC}\,F_{D2})$$

$$= \frac{F_M V_0 \omega_o^2}{DD'}\left(\frac{\dfrac{-GP}{(C_1 + C_3)R_1 s}}{s^2 + 2\zeta\omega_o\, s + 1}\right)\left(\frac{1 + sR_4C_1}{1 + sR_4(C_1//C_3)}\right)\left(\frac{DL_e}{R_L}\, s - 1\right)$$

$$+ \frac{F_{AC}N_S D}{R_L N_P \omega_o^2}\left(\frac{s^2 + \left(\dfrac{R_L D'}{L_S} + 2\zeta\omega_o\right) s + \dfrac{2D'}{L_S C}}{s^2 + 2\zeta\omega_o\, s + \omega_o^2}\right) \qquad (4.6.5.1)$$

A unique characteristic of equation (4.6.5.1) is that the number of zeroes is always equal to the number of poles regardless of the form of compensation network used. Equation (4.6.5.1) has four poles and four zeroes; but if the order of the system changes due to the addition of a pole or a zero in the compensation network, the open loop transfer function G_{OL} will carry five poles and five zeroes since the second term of (4.6.5.1), $\frac{F_{AC}F_{D2}}{\Delta}$, has an equal number of zeroes and poles (two zeroes and two poles). This second order expression is determined solemnly by the power stage and is independent of the form of the dc feedback loop. Equation (4.6.5.1) can be expressed in the following form:

$$G_{OL} = \frac{F_M F_{AC} V_0 N_S R_4 C_3}{D' R_C N_P} \cdot \frac{s^4 + \alpha s^3 + \beta s^2 + \gamma s + \mu}{s(R_4C_3 s + 1)(s^2 + 2\zeta\omega_o S + \omega_o^2)} \qquad (4.6.5.2)$$

where,

$$\alpha = \frac{R_L D'}{L_S} + \frac{1}{C_3}\left(\frac{1}{R_4} - \frac{N_P}{N_S}\,\frac{GPR_C}{F_{AC}R_1}\right)$$

$$\beta = \frac{GP\ N_P R_C}{F_{AC} R_1 N_S C_3} \left(\frac{R_L}{DL_e} - \frac{1}{R_4 C_1} - \frac{1}{R_C C} \right) + \frac{R_L D'}{R_4 C_3 L_S} + \frac{2D'}{L_S C}$$

$$\gamma = \frac{1}{R_4 C_3 L_e} \left[\frac{GPR_L N_P}{R_1 C_1 F_{AC} N_S D} \left(\frac{DL_e}{R_C} - R_C C - R_4 C_1 \right) + \frac{2}{D'} \right]$$

$$\mu = \frac{GPR_L N_P \omega_o^{\ 2}}{F_{AC} D N_s R_1 C_1 R_4 C_3}$$

In the general form, equation (4.6.5.2) is too difficult to factorize. Possibly if bounds are given on parameter values, some simplification can be done. Due to the complexity of the fourth order expression and not to take from the generality, a parametic study of the system open-loop response along with other system behaviors will be discussed in the next section.

Another salient feature of the system open-loop characteristic is the gain which approaches a constant value at high frequency. A simplified expression for the constant gain at high frequency can be attained. From equation (4.6.5.2) assuming $s \to \infty$, equation (4.6.5.3) yields:

$$G_{OL} \Big|_{s \to \infty} = \frac{F_M V_0 N_S}{D' R_L N_P} F_{AC} \qquad (4.6.5.3)$$

In reality, however, the gain is expected to decrease at high frequency. This is because the pulse modulator gain can no longer be regarded constant at such high frequencies. The analytical model presented here fails to take the high frequency effect of the pulse modulator into account. Due to the complicated describing function modeling employed here, the pulse modulation is simply represented by a constant gain.

4.6.6 Parametric Evaluations

A parametric study is performed on the small-signal behavior of the current-injected converter. The purpose of the parametric examination is to key on particular salient features of the control characteristics and design strategy for the current-injected control. Due to the complexity of each small-signal models, especially the audiosusceptibility and the output impedance characteristics, the analytical expressions could not be simplified without a loss in generality. For this reason, parametric study by ways of changing certain key design parameters including the duty-cycle variation, $\frac{T_{ON}}{T_P}$, ac loop-gain, F_{AC}, dc loop-gain via GP and the dc loop-gain via R_4 are applied to the small-signal expressions. These results can be used to establish design guidelines for the control loops in order to optimize the regulator performances. The small-signal characteristics examined are the following: control-to-output response, dc open-loop characteristic, G_{DL}; system open-loop characteristic G_{OL}; audiosusceptibility $\hat{v}_o/\hat{v}_i$; and output impedance, z_o.

4.6.6.1 Duty-cycle variation

Figure 4.6.6.1 and 4.6.6.2 demonstrate the control-to-output and dc open-loop response with respect to changes in the steady-state duty-cycle ratio. As expected, an increase in the duty-cycle ratio forces the control-to-output gain and the dc open-loop gain downward.

As shown in Fig. 4.6.6.3 the duty-cycle has no drastic effect on the system open-loop phase delay. Therefore, a wide variation in duty cycle operation should not disturb the stability of the system. The duty-cycle

does have a more appreciable effect on the high frequency gain of the system open-loop response. The larger duty-cycle forces the crossover-frequency to a higher value. Caution must be exercised when examining the high frequency behavior since the accuracy of the model degenerates when the modulation frequency approaches one-half the switching frequency.

The quality of the system's audiosusceptibility demonstrates the converter's ability to reject input noise. Figure 4.6.6.4 shows the lower the duty-cycle the better the audiosusceptibility. Intuitively this is understandable, because a lower duty-cycle allows a smaller percentage of the total input noise to propagate to the output.

Similar effect is shown when one examines the output impedance characteristic as a function of duty-cycle. The output impedance reduces with the lowering of the duty-cycle as shown in Fig. 4.6.6.5.

4.6.6.2 Variation in ac loop gain

The ac-loop-gain block is comprised of a resistor, R_{sw}, and a turn ratio n, a current transformer in series with the power switch. $F_{AC} = R_{SW}/_n$. In Fig. 4.6.6.6 the ac loop gain, F_{AC}, forces the control-to-output gain to reduce for larger values in R_{sw}/n. With either lower or higher F_{AC} the effect of two-pole/two-zero characteristic becomes more pronounced. Examining the phase curve for $F_{AC} = 3.0$, one notices the phase curve rises after approaching -90°. This phenomenon will not be observed in the simplified single-zero/single-pole approximation with the present model, a second zero in the left-half-plane causes the phase to rise after reaching -90° and then the second pole cancels the LHP zero's effect allowing the phase to continue downward to -180°.

Increasing the ac loop gain decreases the dc open-loop gain as shown

in Fig. 4.6.6.7. The higher dc-open-loop gain, in general, results to better closed-loop responses such as audiosusceptibility and output impedance as will be discussed later.

Illustrated in Fig. 4.6.6.8 is the effect of the ac-loop gain to the system open-loop characteristics.

The ac loop gain F_{AC} has a very dominating effect on the system open-loop characteristic at high frequencies and virtually no effect at frequencies below the output filter resonant frequency. By decreasing the ac feedback two of the system open-loop zeros move from the LHP toward the imaginary axis. Further reduction in the ac gain results in a complex conjugate pair of zeros as exemplified by the second-order effect of the gain curve with $F_{AC} = 0.3$. Continuing even further the conjugate pair changes into two positive zeros. The open-loop phase drastically changes when the zeros migrate to the right-half-plane. This detrimental phase characteristic which approaches -360° has a very undesirable effect on the system stability. With positive zeros adding to the phase delay the phase margin is reduced to a negative value which results to an unstable system.

The audiosusceptibility characteristic as a function of the ac loop gain is plotted in Fig. 4.6.6.9. The ac feedback loop provides an excellent parameter to adjust the low-frequency response of the audiosusceptibility. Since the passive filters in the regulator generally can provide adequate attenuation of disturbances at higher frequencies, the lower frequency range within, say, zero to ten-times the output filter resonant frequency is the frequency range to control. For this reason the ac-loop gain will play a significant role in optimizing the regulators ability to attenuate a

small-signal sinusoidal disturbance propagating from the regulator input to its output.

For smaller values of F_{AC}, the audio response reduces particularly at low frequencies. The ac feedback gain can be reduced to the point where second order peaking effect appears around 5-6 KHz. The second-order peaking effect is caused by the emergence of two poles of the closed-loop response into a complex-conjugate pair. This condition causes severe degradation in the audiosusceptibility performance of the system. As discussed earlier, the system becomes unstable under this condition. The optimal condition for the audiosusceptibility response occurs when $F_{AC} = 0.6$ prior to the occurrence of the two zeros forming a complex conjugate pair. Similar effect is shown when the output impedance characteristic is plotted as a function of F_{AC} in Fig. 4.6.6.10.

4.6.6.3 DC loop gain variation via GP

GP contains the dc gain resistor, R_3, as shown in the following expression:

$$GP = \frac{1}{1 + {}^{R_3}/_{R_1} + {}^{R_3}/_{R_2}}$$

As R_3 decreases, GP increases, forcing the dc-open-loop gain upward as demonstrated in Fig. 4.6.6.11. The dc open-loop phase is not effected.

Variations in GP have a significant effect on the low frequency end of the system open-loop gain as shown in Fig. 4.6.6.12. As GP approaches its theoretical limit of one, the system gain increases. The second-order peaking effect occurred around 30KHz exceeds the theoretical bound of the model, since the model is only good up to half of the switching frequency (40KHz/2). Examining the phase characteristics of the system open-loop in Fig. 4.6.6.12 no zero migration to the right-half plane is noticed as

mentioned previously with a variation in the ac-loop gain.

Approaching the theoretical limit of GP improves the audiosusceptibility. Again GP has a notable effect on the low frequency section of the audio. Fig. 4.6.6.13 shows a 25 db improvement over the range of GP. Therefore by decreasing the dc gain resistor, R_3, the attenuation of noise from the input to the output is improved.

Fig. 4.6.6.14 shows the output impedance characteristics as a function of GP.

4.6.6.4 DC-loop gain variation via R_4

The dc-loop gain can also be varied by changing the gain feedback resistor, R_4. But when R_4 is varied the corner frequencies of the pole and zero produced by the transfer function, F_{DC}, changes. Therefore, the parametric study of R_4 has been constrained to only take in the gain effect and not a shift the corner frequencies. This is done by holding the expressions R_4C_1 and R_4C_3 constant for any change in R_4. Two sets of data are provided for variations in R_4. The first set varies R_4 from 10KΩ to 150KΩ while the second set examines variations of R_4 from 100KΩ to 2MΩ.

Figure 4.6.6.15(a) and (b) demonstrate for an increase in R_4 the dc-open-loop gain increases. The phase does not change because the constraints set previously inhibit the corner frequency of the compensation network from changing.

From Fig. 4.6.6.16(a) the variation in R_4 has no degrading effect on the phase and affects the system open-loop gain only in the low frequency range. Apparently, the variation from 10K to 150K of R_4 has a negligible effect on the system's stability. As R_4 is increased further ($R_4 \rightarrow 1M\Omega$),

two zeros migrate to the RHP forming a complex-conjugate pair and forcing the phase to approach -360° instead of 0° as shown in Fig. 4.6.6.16(b). This drastic change of the phase has detrimental effect on the system stability. In fact, for large R_4, the branch formed by R_4C_1 can be regarded as open circuit. Figure 4.6.6.17(a) shows the switch current waveform of the stable converter employing the set of circuit parameter values given in Chapter 5, page 53. Figure 4.6.6.17(b) illustrates the switch current waveform of the unstable system when the branch R_4C_1 is opened.

The effect of R_4 to the audiosusceptibility curves is given in Fig. 4.6.6.18(a) and (b). Notice as R_4 increases the audiosusceptibility steadily improves until the two positive zeros are felt causing second-order peaking in the high frequency range. The complex zeros in the RHP eventually turn into real zeros. As $R_4 = 2M\Omega$, the peaking effect is no longer shown and the audiosusceptibility is greatly improved. Nevertheless, the system becomes unstable due to the excessive phase delay. Similar characteristics are displayed for the output impedance curves as shown in Fig. 4.6.6.19(a) and (b).

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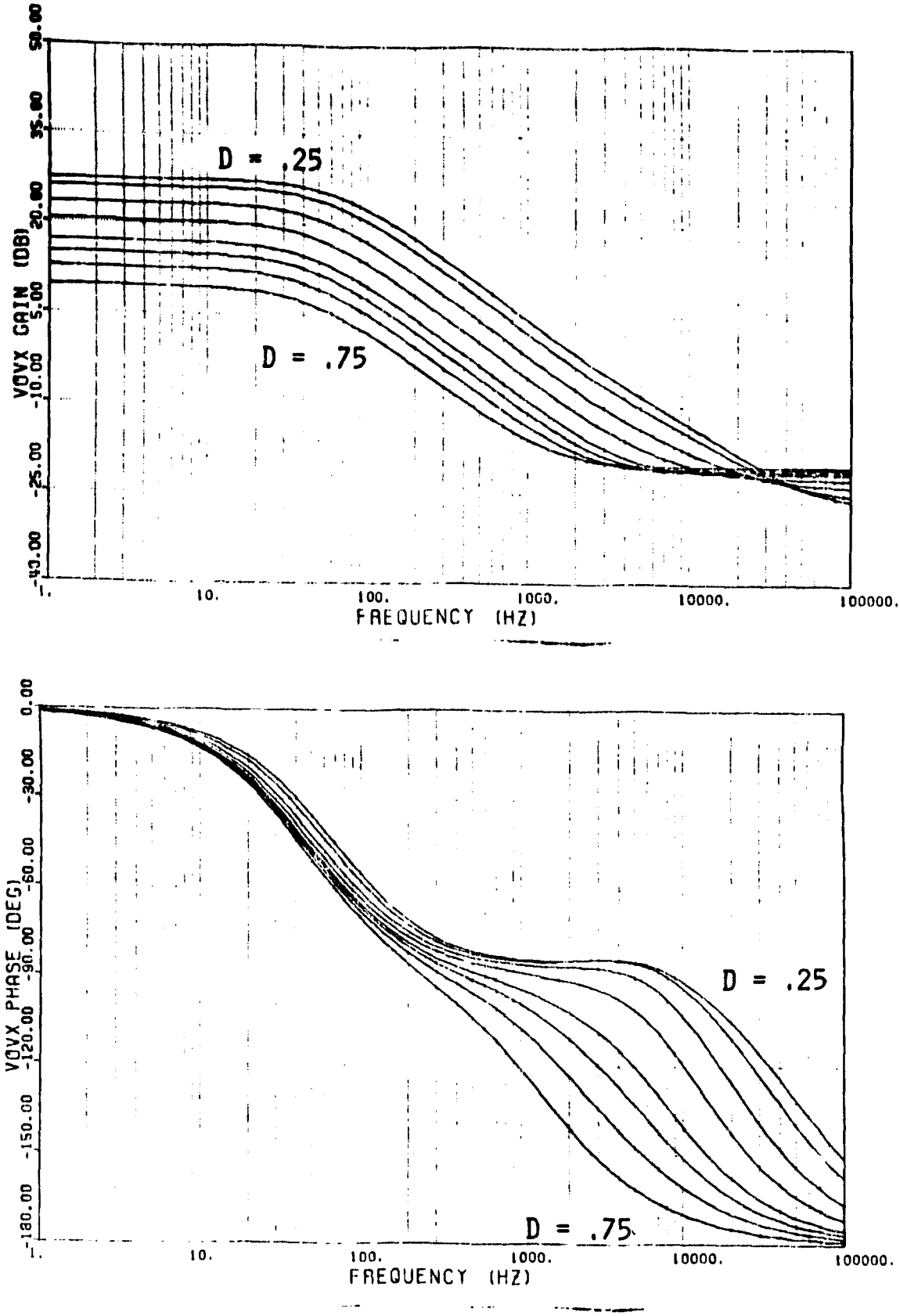

Fig. 4.6.6.1 Control-to-output gain and phase characteristics for D = 0.25, 0.3, 0.4, 0.5, 0.6. 0.65, 0.7, 0.75.

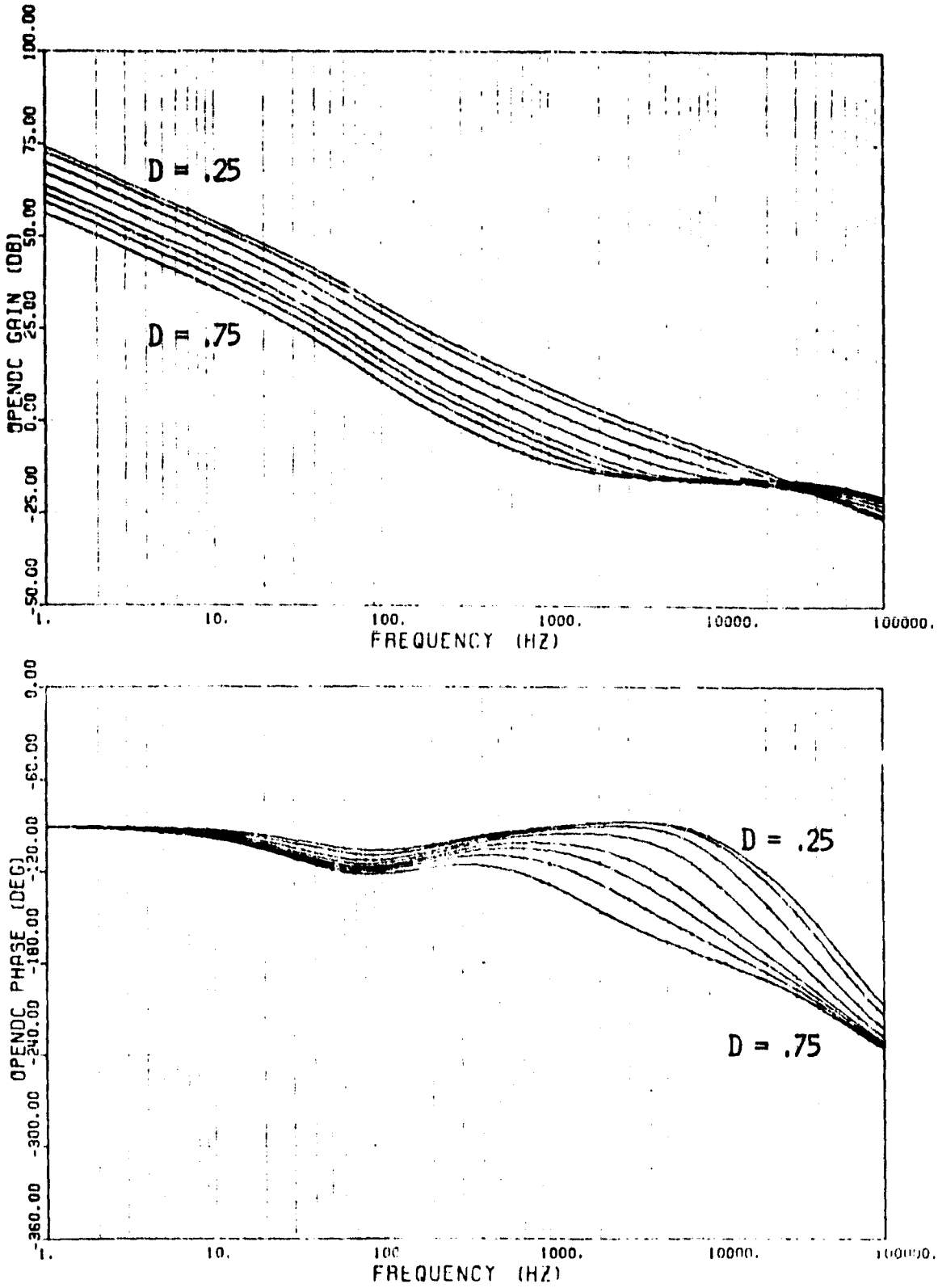

Fig. 4.6.6.2 Dc-open-loop gain and phase characteristics for D - 0.25, 0.3, 0.4, 0.5, 0.6, 0.65, 0.7, 0.75.

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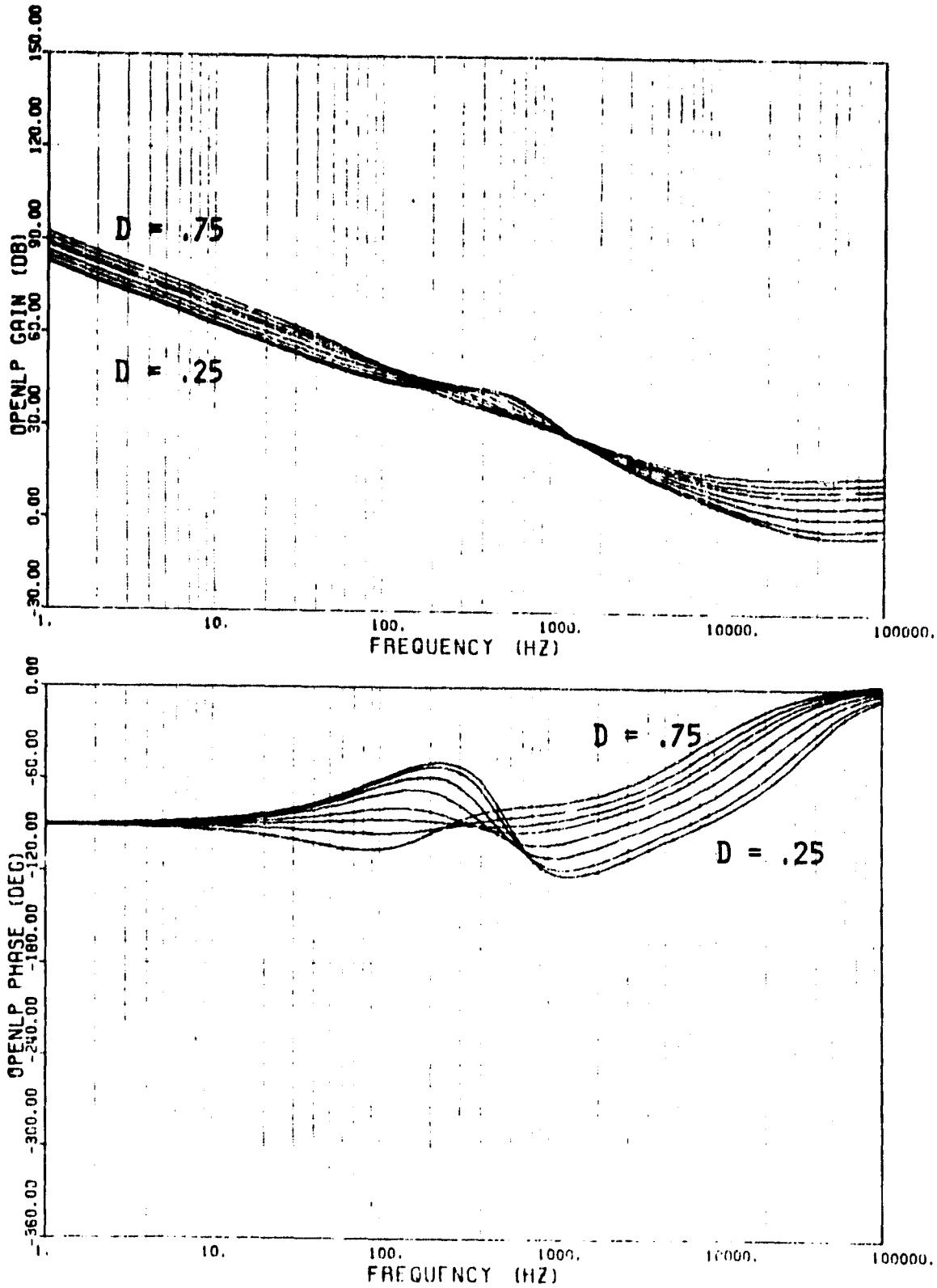

Fig. 4.6.6.3 System open-loop gain and phase response for D = 0.25, 0.3, 0.4, 0.5, 0.6, 0.65, 0.7, 0.75.

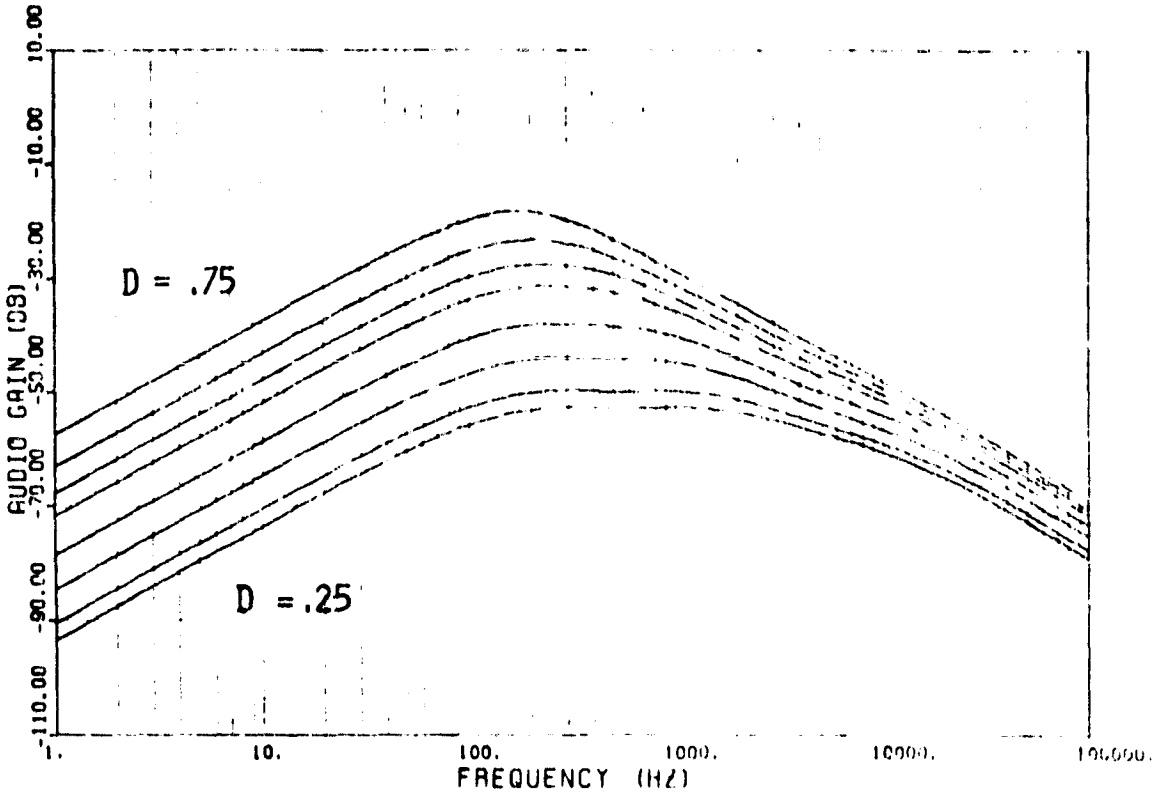

Fig. 4.6.6.4 Audiosusceptibility gain and phase characteristics for D = 0.25, 0.3, 0.4, 0.5, 0.6, 0.65, 0.7, 0.75.

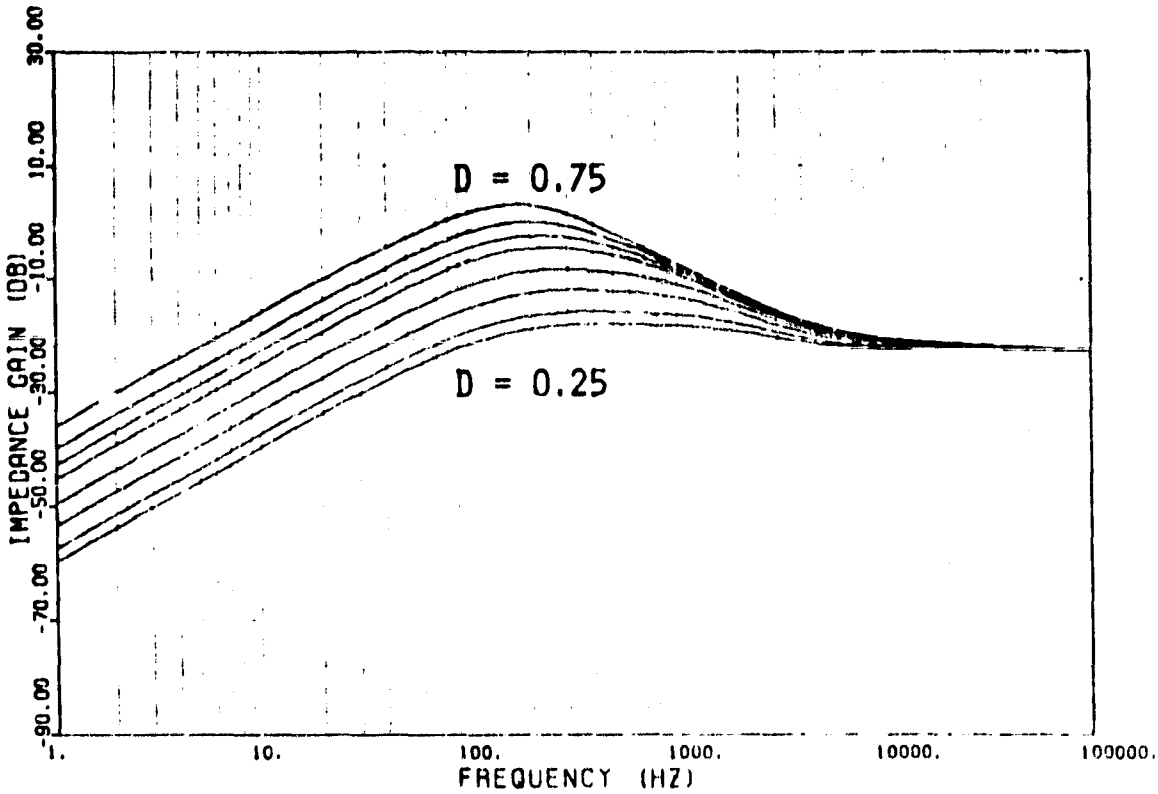

Fig. 4.6.6.5 Output impedance characteristics for
D = 0.25, 0.3, 0.4, 0.5, 0.6, 0.65, 0.7, 0.75.

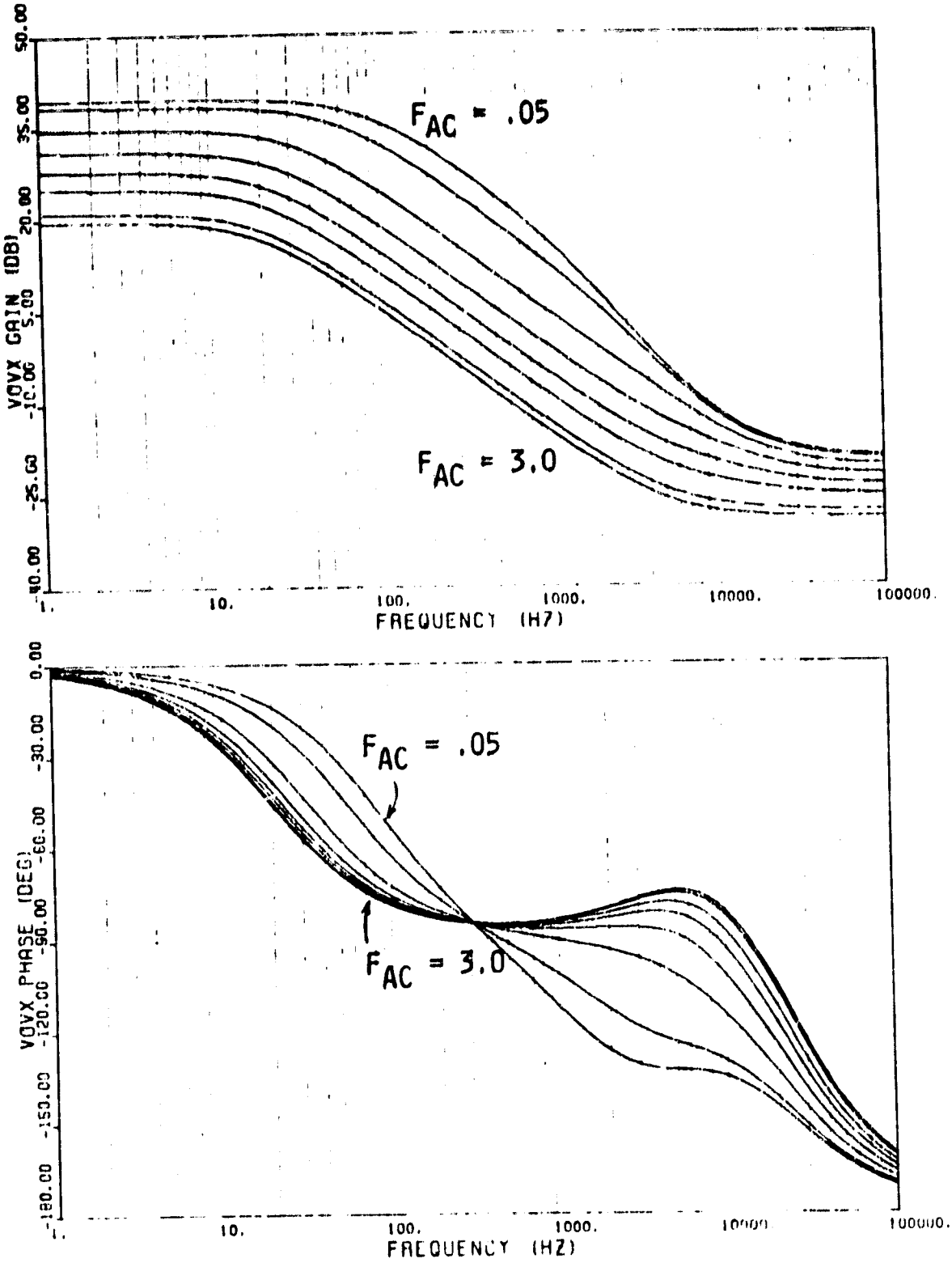

Fig. 4.6.6.6 Control-to-output gain and phase response for F_{AC} = 0.05, 0.1, 0.3, 0.6, 1.0, 1.5, 2.5, 3.0.

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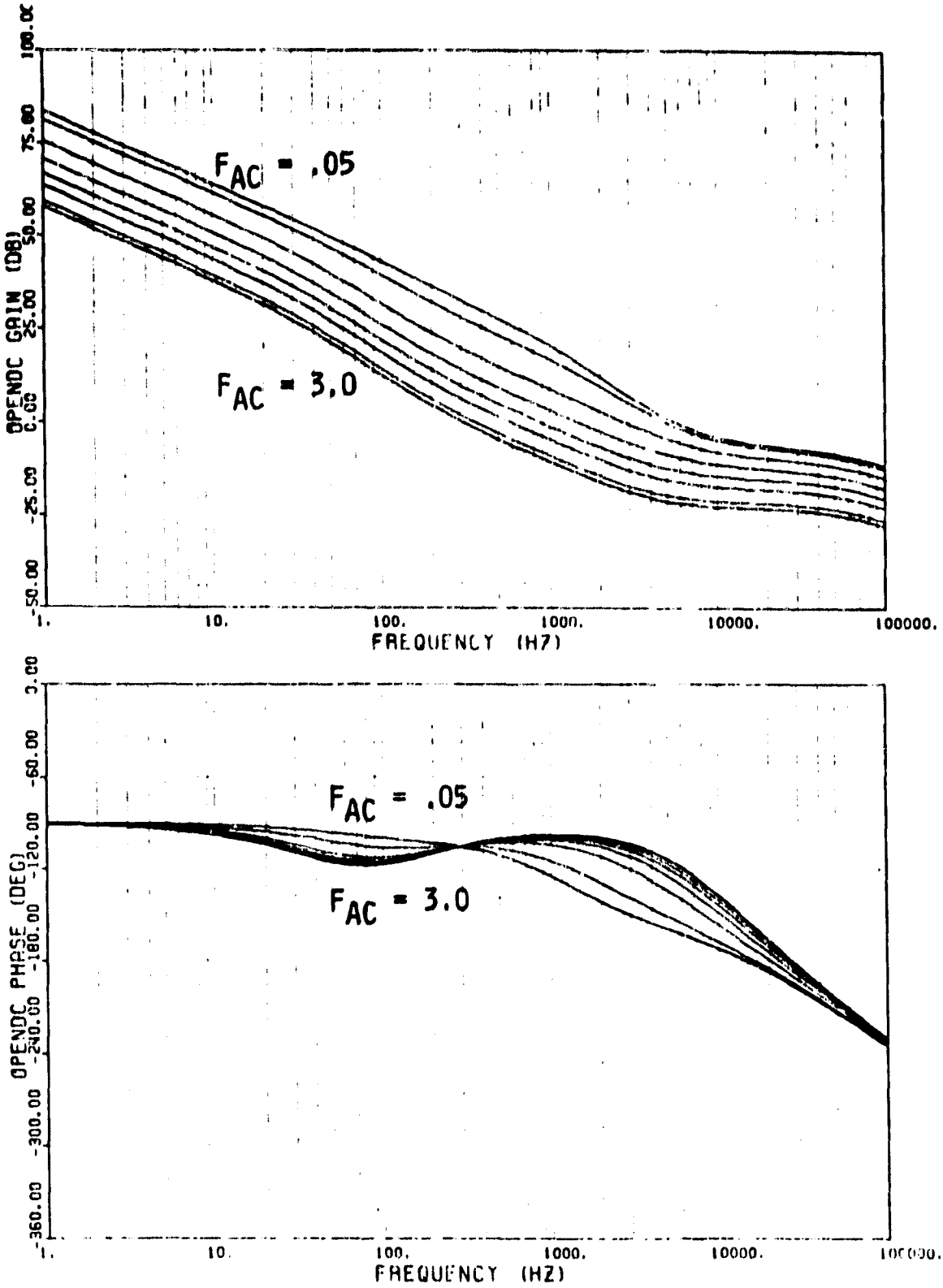

Fig. 4.6.6.7 Dc-open-gain and phase characteristics for F_{AC} = 0.05, 0.1, 0.3, 0.6, 1.0, 1.5, 2.5, 3.0.

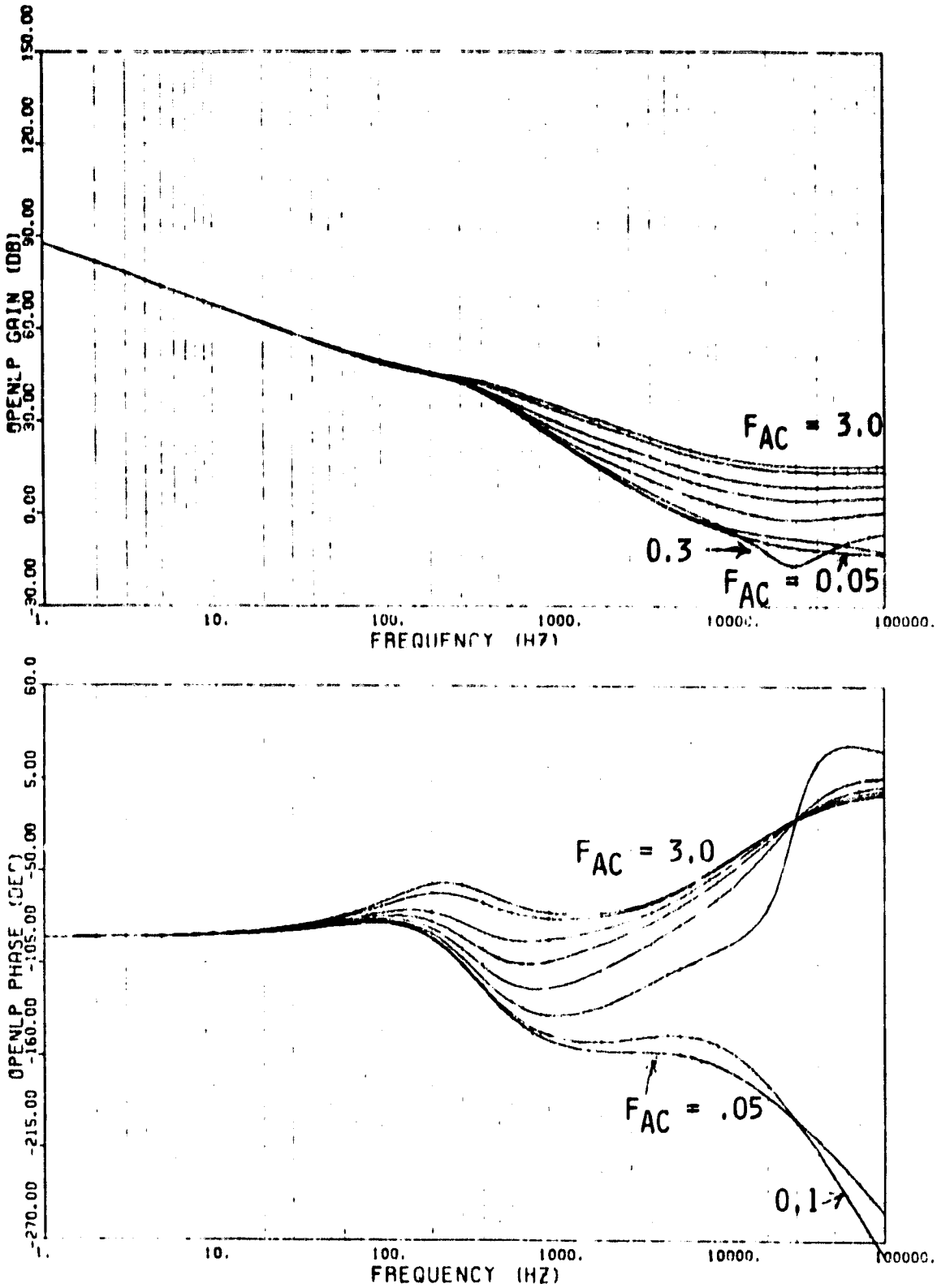

Fig. 4.6.6.8 System open-loop gain and phase characteristics for F_{AC} = 0.05, 0.1, 0.3, 0.6, 1.0, 1.5, 2.5, 3.0.

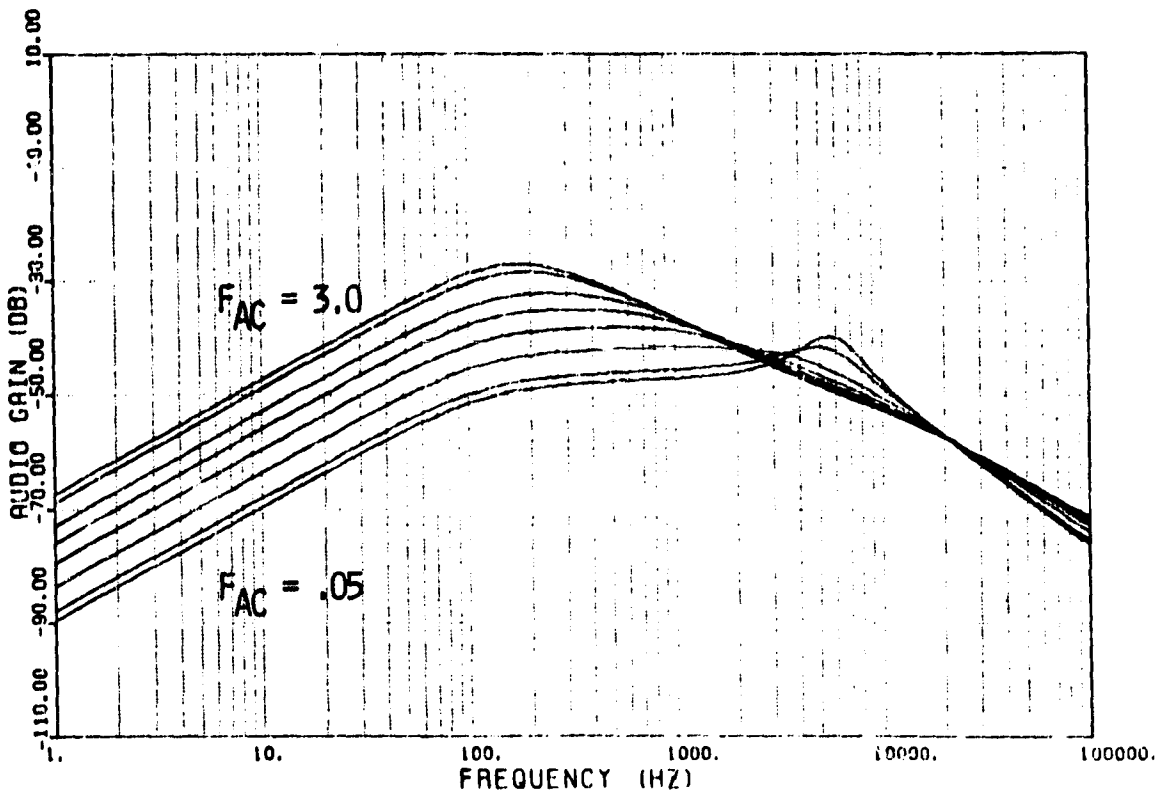

Fig. 4.6.6.9 Audiosusceptibility gain response for F_{AC} = 0.05, 0.1, 0.3, 0.6, 1.0, 1.5, 2.5, 3.0

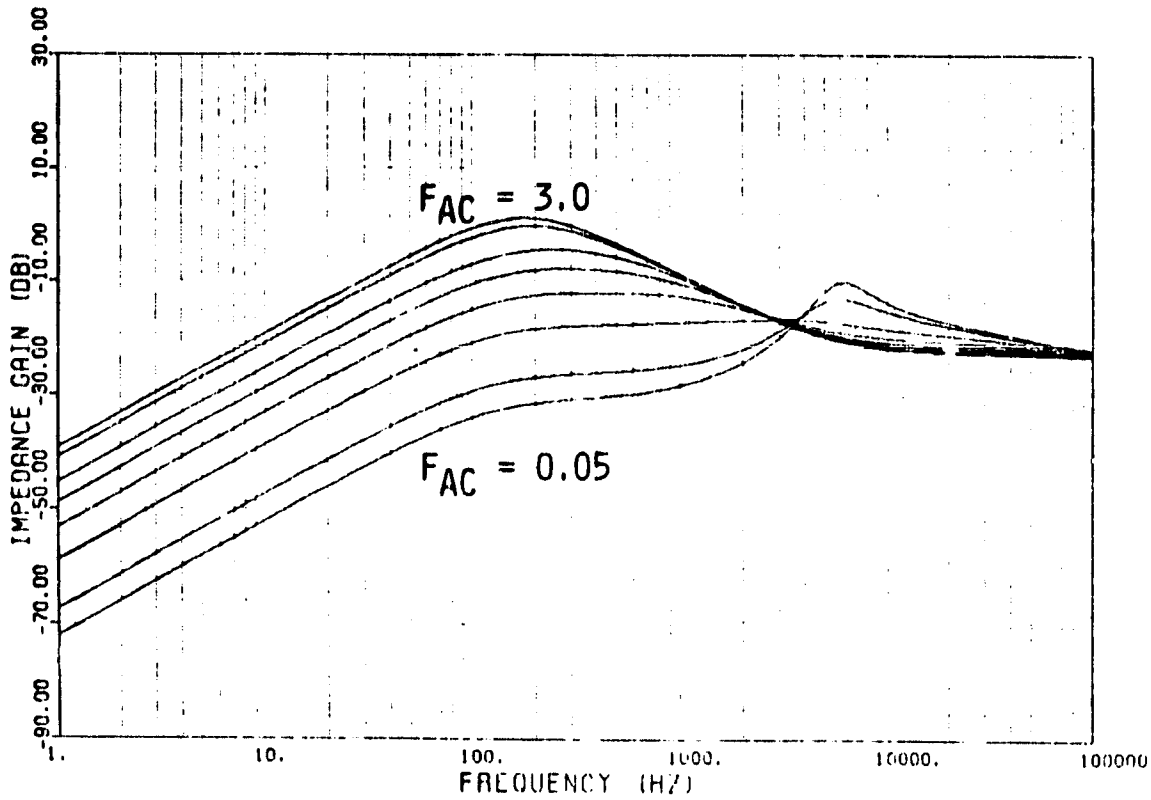

Fig. 4.6.6.10 Output impedance characteristics for

F_{AC} = 0.05, 0.1, 0.3, 0.6, 1.0, 1.5, 2.5, 3.0 .

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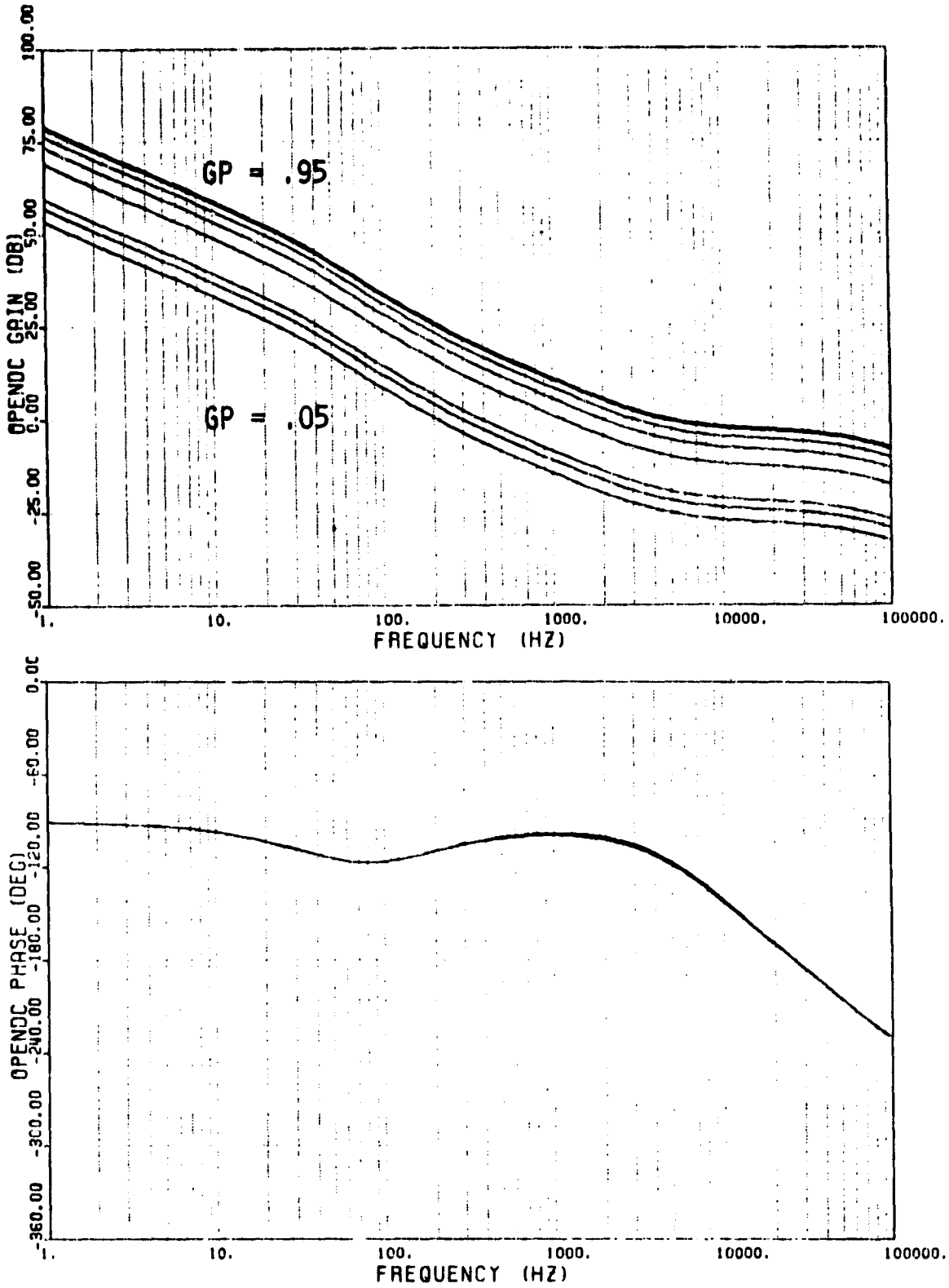

Fig. 4.6.6.11 Dc-open-loop gain and phase characteristics for GP = 0.05, 0.075, 0.1, 0.3, 0.5, 0.7, 0.9, 0.95.

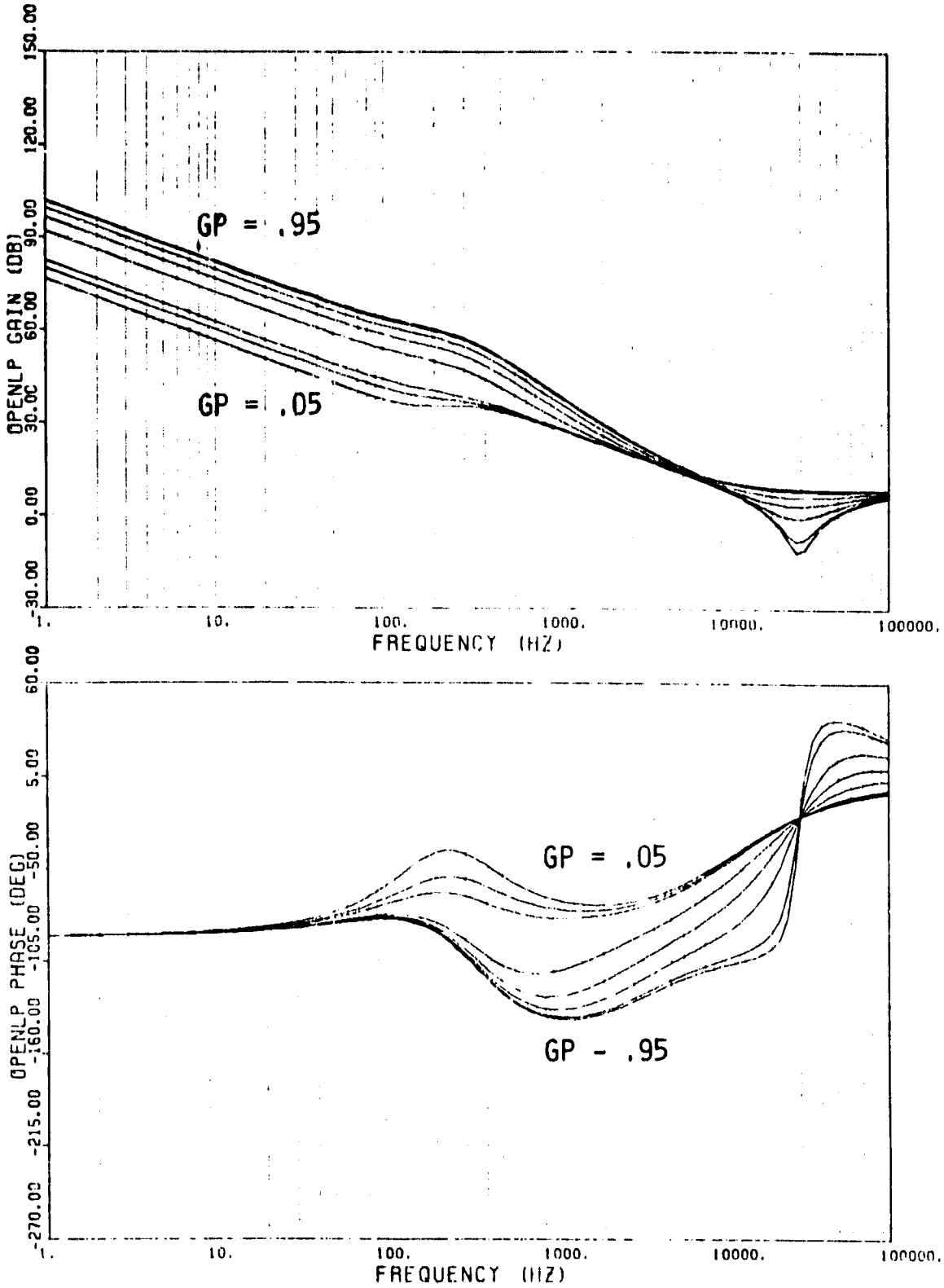

Fig. 4.6.6.12 System open-loop gain and phase characteristics for GP = 0.05, 0.075, 0.1, 0.3, 0.5, 0.7, 0.9, 0.95.

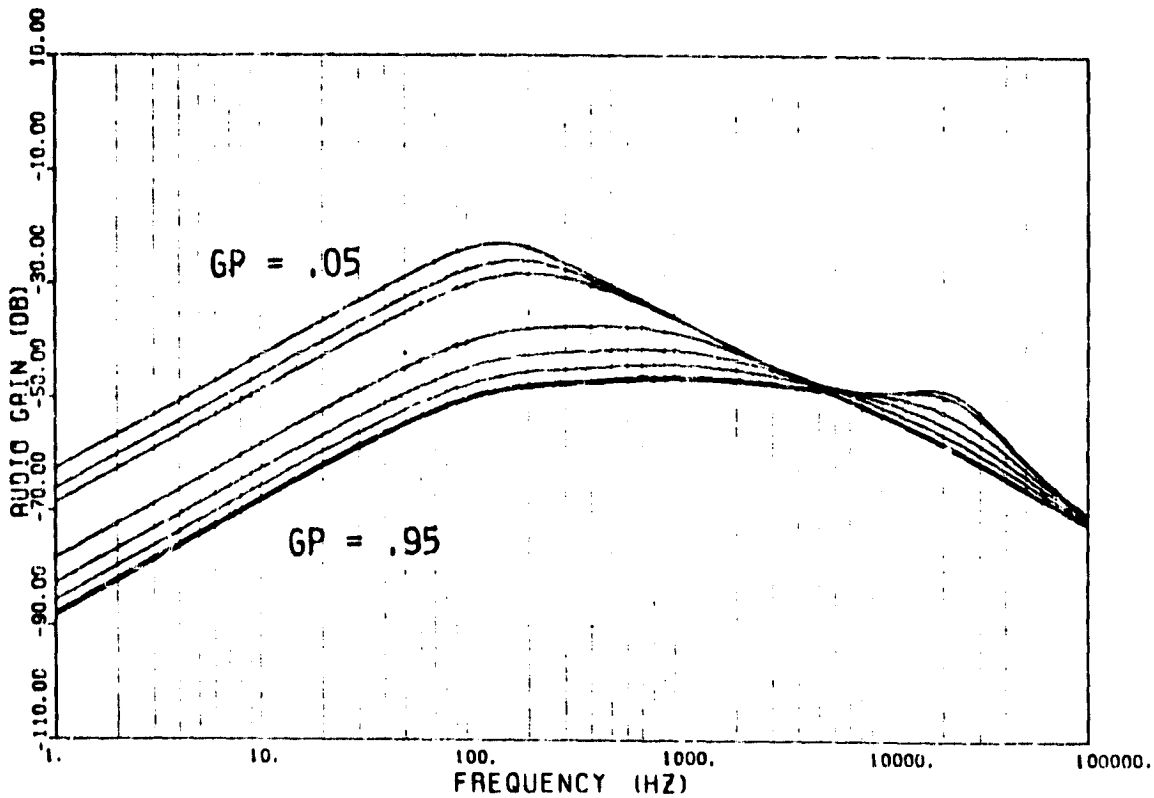

Fig. 4.6.6.13 Audiosusceptibility characteristics for GP = 0.05, 0.075, 0.1, 0.3, 0.5, 0.7, 0.9, 0.95

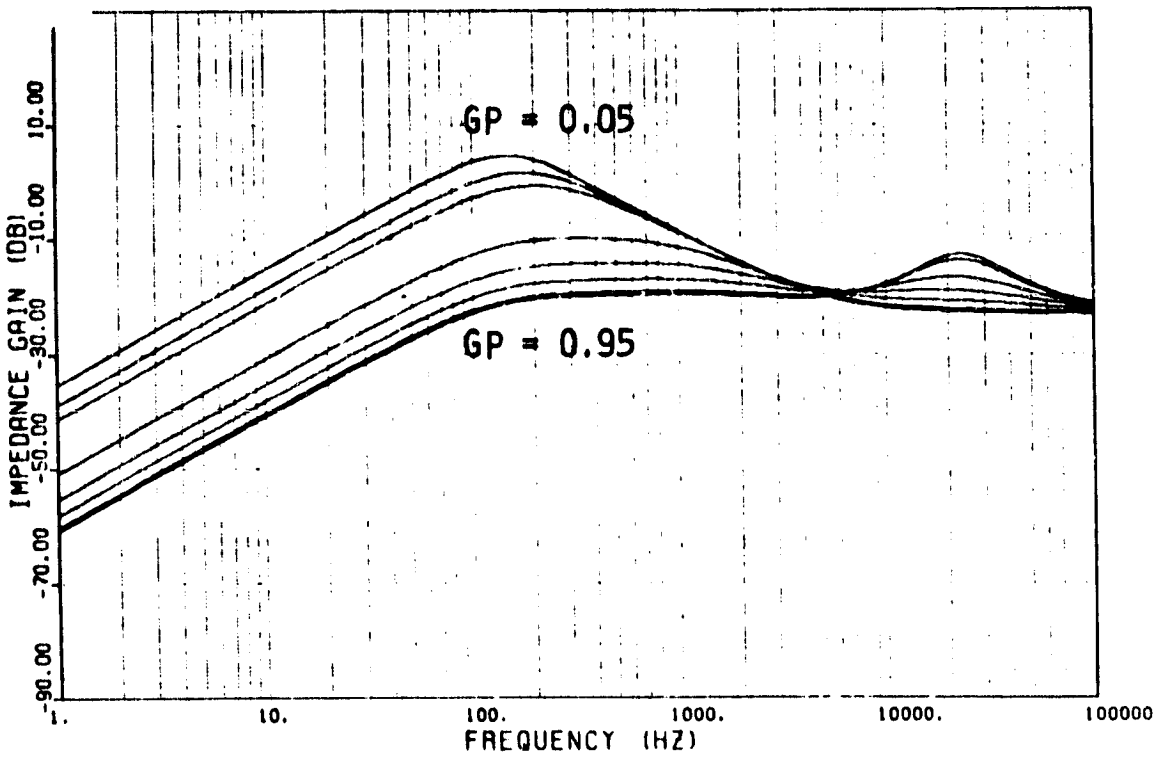

Fig. 4.6.6.14 Output impedance characteristics for
GP = 0.05, 0.075, 0.1, 0.3, 0.5, 0.7, 0.9, 0.95.

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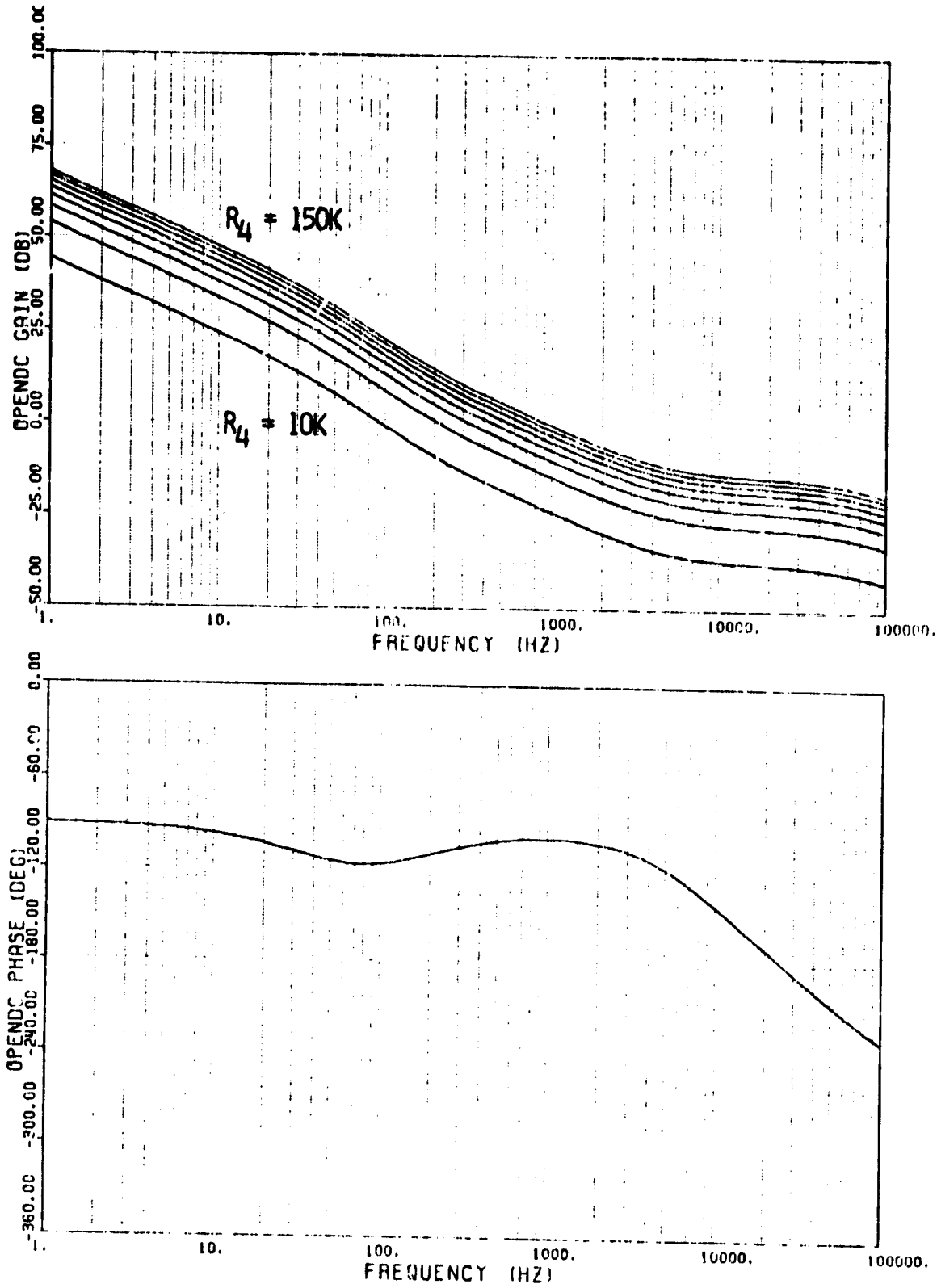

Fig. 4.6.6.15(a) Dc-open-loop gain and phase characteristics for R_4 = 10K, 30K, 50K, 70K, 90K, 110K, 130K, 150K.

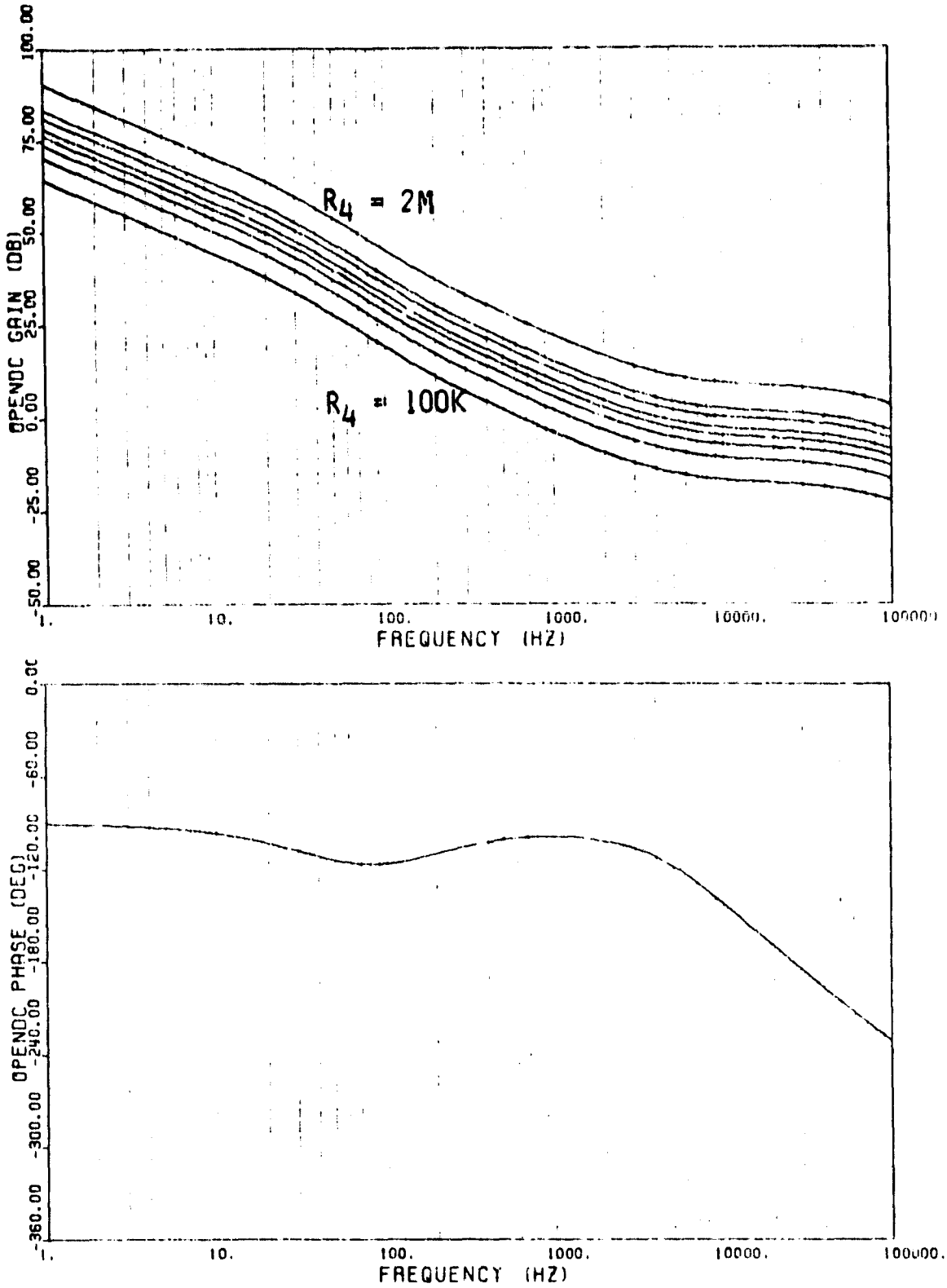

Fig. 4.6.6.15(b) DC-open-loop gain and phase characteristics for R_4 = 100K, 200K, 300K, 400K, 500K, 700K, 900K, 2MΩ.

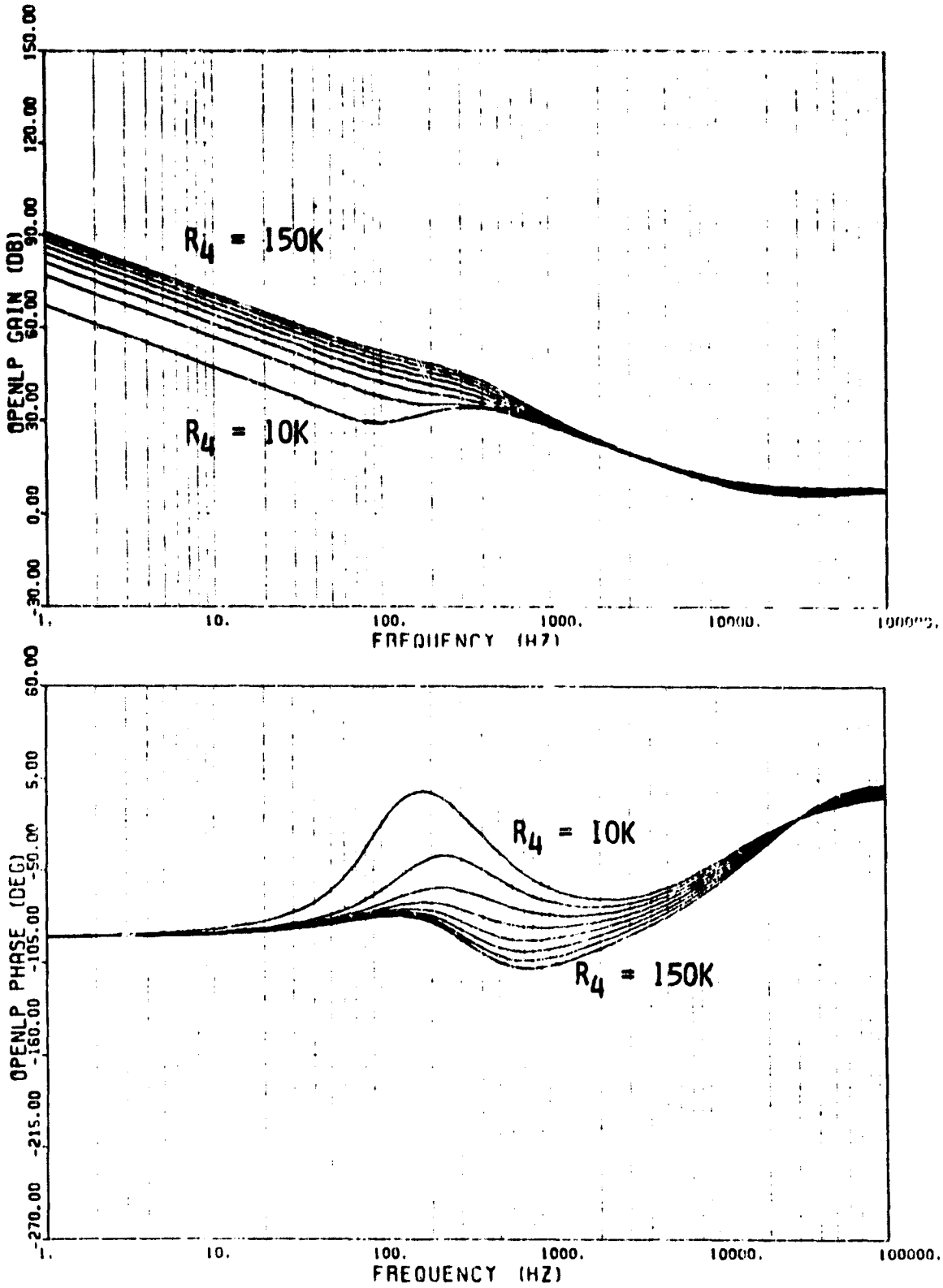

Fig. 4.6.6.16(a) System open-loop gain and phase characteristics for R_4 = 10K, 30K, 50K, 70K, 90K, 110K, 130K, 150KΩ.

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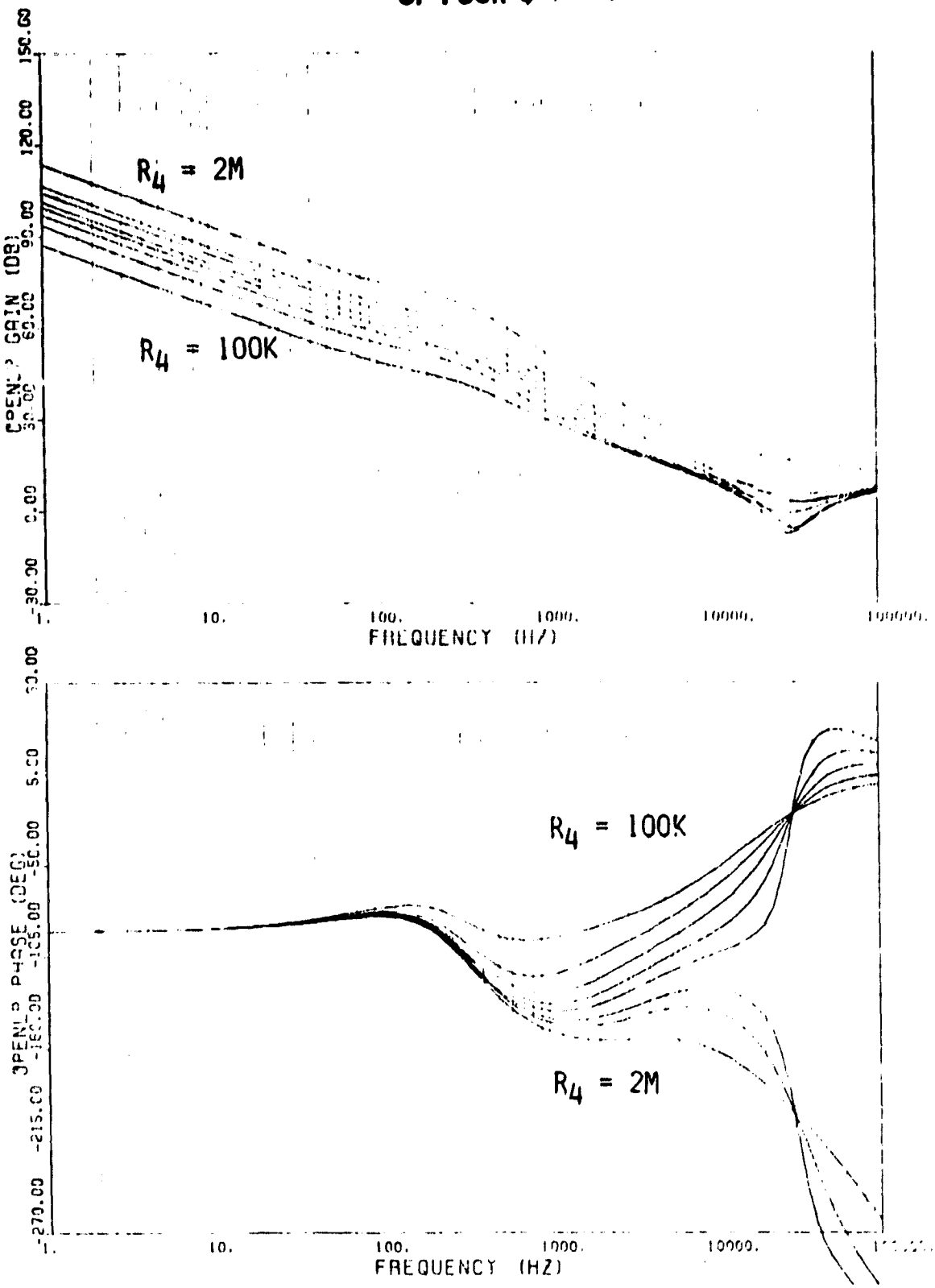

Fig. 4.6.6.16(b) System open-loop gain and phase characteristics for R_4 = 100K, 200K, 300K, 400K, 500K, 700K, 900K, 2MΩ.

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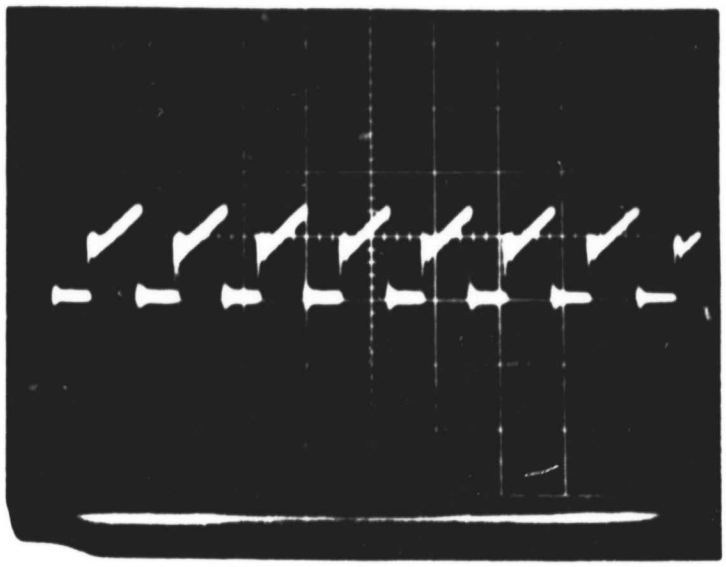
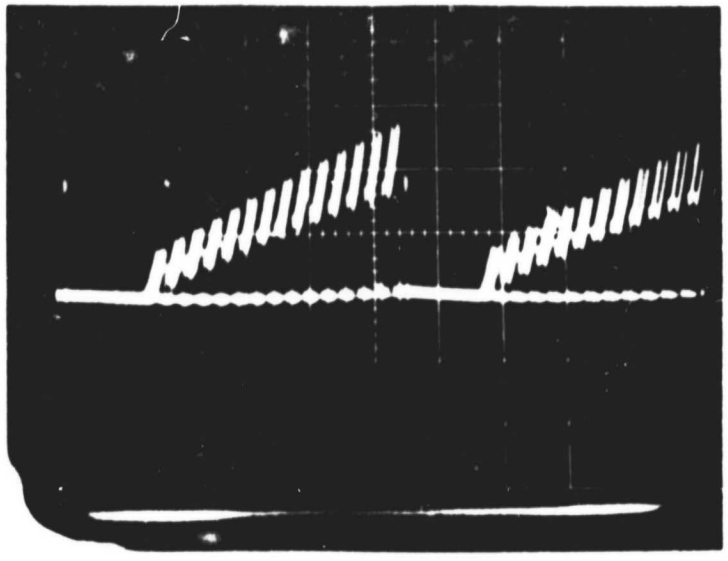


(a)



(b)

Fig. 4.6.6.17(a) Transistor collector-current waveform for a stable system with R_4C_1 branch. Vertical: 1A/div., Horizontal: 20 ms/div.

(b) Transistor collector-current for an unstable system when R_4C_1 is removed. Vertical: 1A/div., Horizontal: 0.1 ms/div.

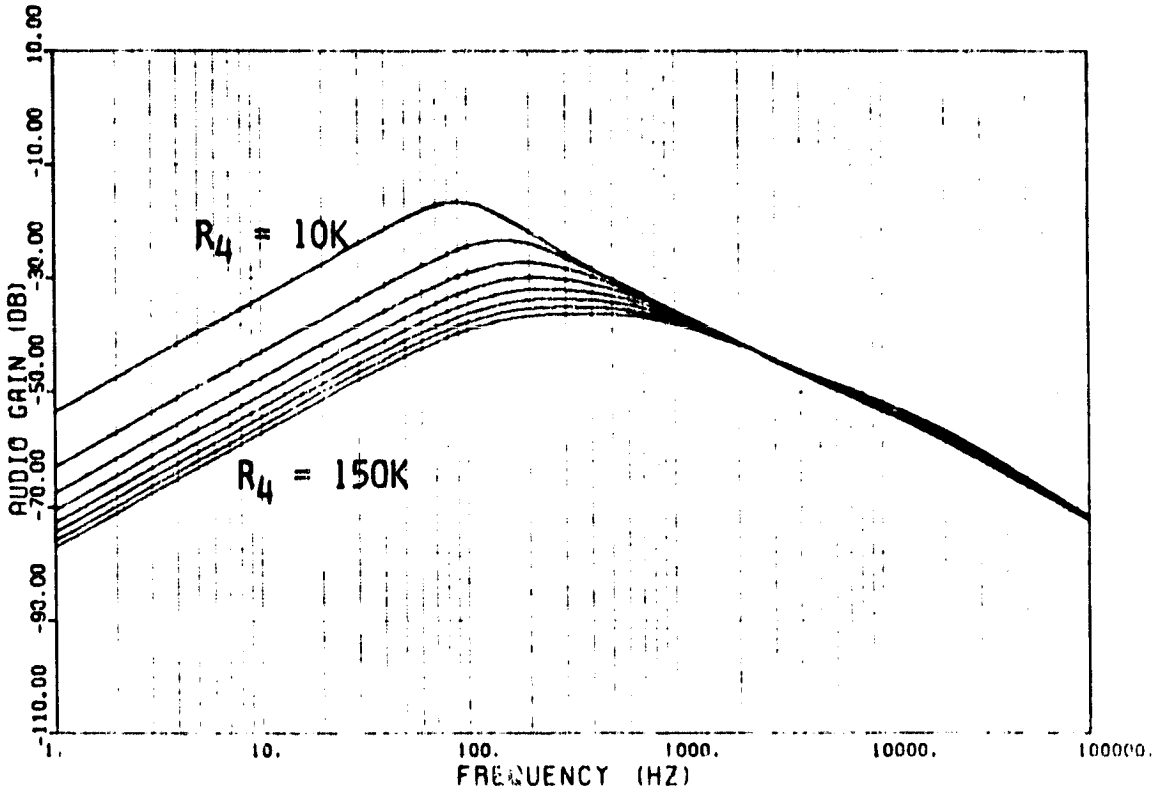


Fig. 4.6.6.18(a) Audiosusceptibility characteristics for R_4 = 10K, 30K, 50K, 70K, 90K, 110K, 130K, 150K. The product R_4C_1 and R_4C_3 remain constant.

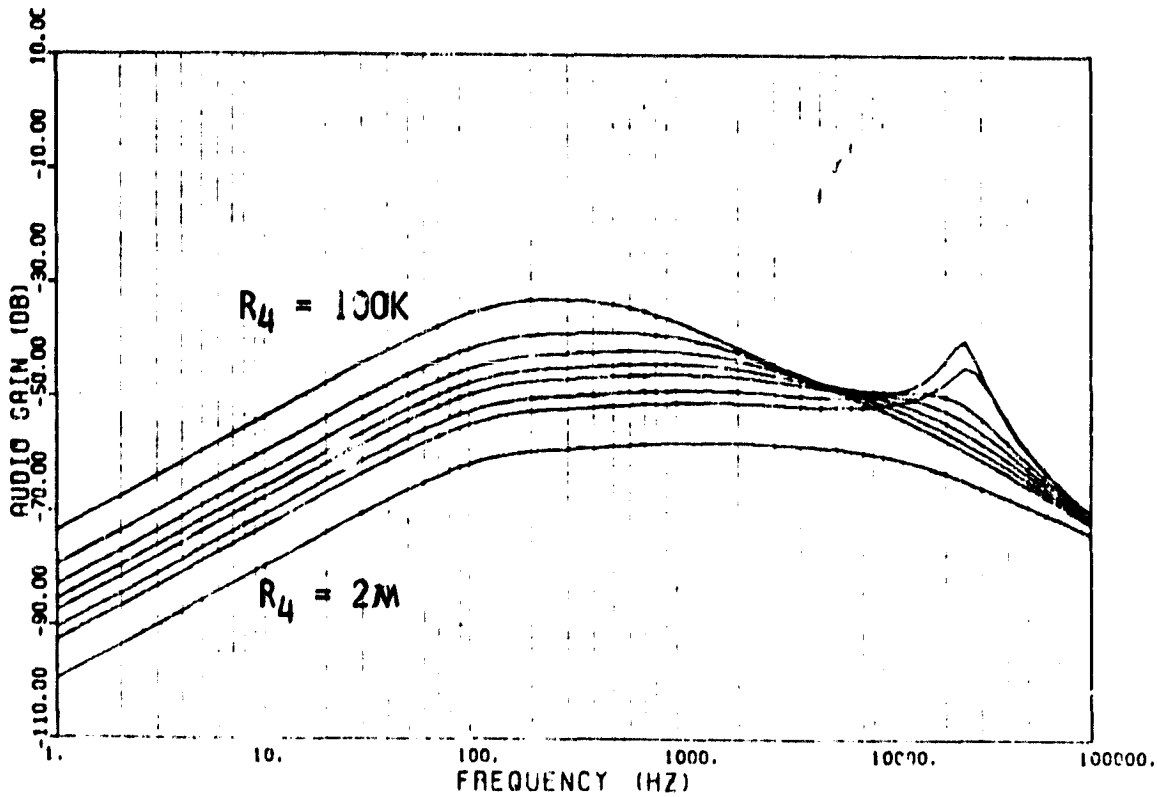


Fig. 4.6.6.18(b) Audiosusceptibility characteristics for R_4 = 100K, 200K, 300K, 400K, 500K, 700K, 900K, 2MΩ.

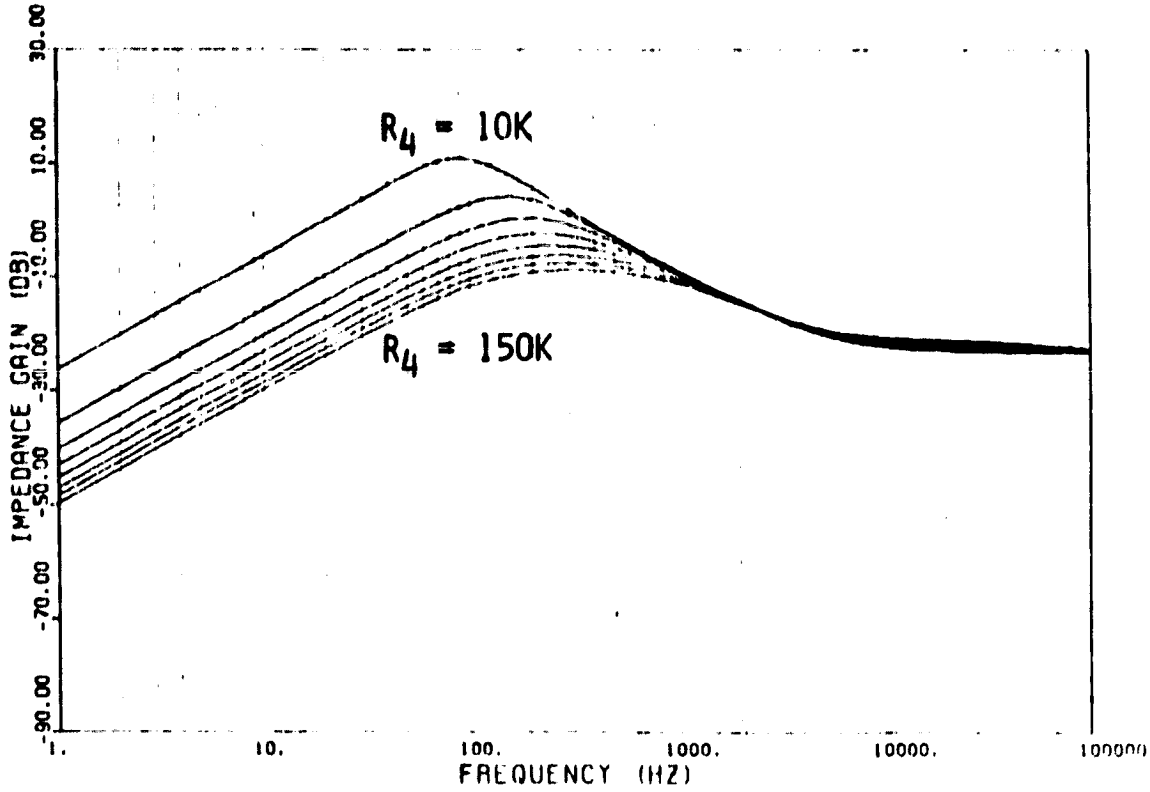


Fig. 4.6.6.19(a) Output impedance characteristics for R_4 = 10K, 30K, 50K, 70K, 90K, 110K, 130K, 150K. The product R_4C_1 remain constant.

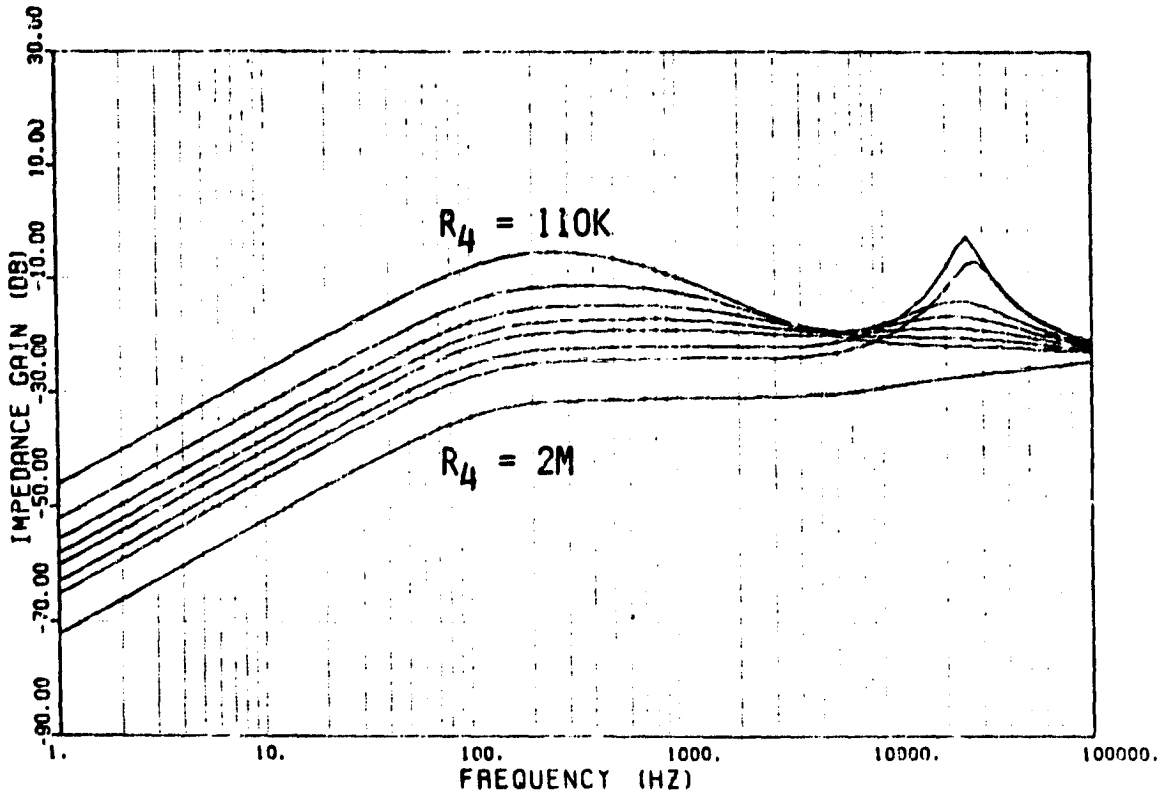


Fig. 4.6.6.19(b) Output impedance characteristics for R_4 = 100K, 200K, 300K, 400K, 500K, 700K, 900K, 2MΩ.

4.7 CONCLUSIONS

Modeling and Analysis of a buck/boost regulator employing the current-injected (current-programmed) control is presented. The objective is to examine the small-signal dynamic performance of the switching regulator including:

- Open-loop characteristics and system stability.
- Closed-loop characteristics and audiosusceptibility.
- Response due to load disturbances and output impedance characteristics.
- Features of the current-injected control and design guidelines.

In order to gain insights of the performance characteristics of various parts of the switching regulator employing the current-injected control, the regulator is modeled according to the three basic functional blocks: power stage, error processor, and duty-cycle pulse modulator. The power stage model presented in Chapter 4.2 consists of three inputs: disturbances from the line $\hat{v}_i$, the load $\hat{i}_o$, and the duty-cycle control loop $\hat{d}$; and two outputs: the output voltage $\hat{v}_o$, and the switch current $\hat{i}_p$. The error processor (EP) model as presented in Chapter 4.3 contains the dc feedback, current-injected loop and the compensation network. The EP processes and compensates the signals from both the dc and ac feedback loops and provides the necessary error signal to the duty cycle pulse modulator (PM). The PM takes the analog error signal from the EP and converts the error signal into a series of pulse-width modulated duty-cycle signals. Presented in Chapter 4.4 is the low-frequency model of the duty-cycle pulse modulator employing the describing function techniques.

In Chapter 4.5, the small-signal model for the power stage, the error processor and pulse modulator, derived from Chapters 4.2, 4.3 and 4.4, respectively, are assembled. Employing this small signal model, the following open- and closed-loop characteristics are examined:

- The control-to-output characteristic $\hat{v}_o/\hat{v}_x$.
- The dc open-loop characteristic. (The dc feedback loop is opened, while the current-injected loop is intacted.)
- The system open-loop characteristics. (Both the dc feedback loop and the current-injected loop are opened.)
- The closed-loop input-to-output response - audiosusceptibility.
- The closed-loop response due to a load disturbance - output impedance characteristic,

Experimental verifications are also provided for the above described analytical models with good correlations.

In Chapter 4.6, various regulator open-loop and closed-loop performance characteristics are examined in further detail. Effects of various key control parameters to the regulator performance characteristics are investigated. Features of the current-injected control are discussed. In particular, comparisons are made between the results derived in the current modeling and analysis efforts and the earlier works presented by Caltech (which followed a different modeling approach).

Many interesting characteristics are unveiled upon careful examination of the small-signal model derived in this report. Among those findings, the following ones are particularly noteworthy:

(1) The ac feedback loop is imbedded in the control-to-output transfer function which exhibits two-pole and two-zero characteristic instead of a single-pole single-zero. However, the two-pole

two-zero transfer function can be approximated by a single-pole single-zero transfer function without encountering gross errors under most circumstances.

(2) When the system open-loop characteristic is examined with both dc and ac loops opened, the two-pole two-zero (or single-pole single-zero approximation) characteristic ceases to exist. In fact the system open-loop transfer function exhibits astonishingly different characteristics. Very little resemblance can be found when one compares the open-loop characteristic G_T with the open-dc-loop characteristic G_{DL}.

(3) The stability characteristic for the current-injected control is quite unique comparing to other types of multi-loop control systems [22,23]. The stability margin could extend beyond 90° with very high cross-over frequency. The stability of the system is particularly sensitive to certain control parameter values. A positive zero could be observed in the open-loop characteristic if the control parameters are not properly selected.

5.0 MAPPS DEMONSTRATION PROBLEM FOR VSTOL EMERGENCY POWER SYSTEM

5.1 INTRODUCTION

The VSTOL Emergency Power System is shown in Figure 5.1. A Ni-Cd battery source with an effective series resistance R_e is processed by a boost converter to provide the bus power for emergency use when the generator failed. The battery voltage level depends on the number of Ni-Cd cells connected in series, with the number yet to be determined. The boost-converter power circuit consists of inductance L with winding resistance RL, power switch Q, power diode D, and output capacitor C having an equivalent series resistance (ESR) RC. Since the losses in the converter are supplied from the battery source, and since the converter packaging weight (heat sink included) increases with converter losses, it follows that the combined battery and converter mechanical-structure weight becomes heavier if more converter loss is allowed for a given output power. On the other hand, the converter component weights, i.e., those of magnetics and capacitors, tend to diminish with more allowable losses. Consequently, for a given output power, there must exist an optimum converter efficiency at which the combined system weight including battery, packaging, and converter components, is at its minimum. The essence of the optimization is to identify the battery voltage level along with the detailed boost converter design so that the total system weight of the battery and the packaged converter can be minimized.

The optimization effort starts with the identification of key operating waveforms of the boost converter as functions of line/load conditions, from which the voltage and current expressions are derived for all power-handling components. These expressions are then used to formulate component losses as well as other converter design constraints including input EMI, output ripple, and the proper design of the inductor. The optimization objective of minimizing the system weight is then defined analytically.

At this juncture, two approaches become possible. One is to rely on an established nonlinear programming routine such as the SUMT (Sequential Unconstrained Minimization Technique) to numerically seek the optimum design and the attendant minimum system weight. Two basic variables in this approach are the input voltage to, and the switching frequency of, the converter. They are treated as unknowns, to be determined along with other variables in a single, large-scale numerical optimization. A second approach, less ambitious and thus perhaps more practical, breaks the single large-scale optimization into many smaller optimizations. The two aforementioned variables are given as known values, thereby greatly simplifying the problem and allowing a closed-form optimum VSTOL design for all other variables. Without resorting to nonlinear programming, optimum designs for other sets of known input voltages and switching frequencies can then be similarly calculated, from which the true global optimum corresponding to a specific set can be identified among calculated optimum designs by mapping the data of optimum designs for different sets of voltages and frequencies. A decision was made to adopt the second approach to the VSTOL system optimization, with the purpose of establishing an alternate means to nonlinear programming in achieving optimization. The chosen approach was successfully implemented, and closed-form optimum system designs for any given set of input voltage and switching frequency were obtained. A computer program was generated to perform the straightforward numerical calculations of the analytically-derived closed-form solutions. A 3000-Watt, 0.5-hour emergency application was used as a demonstration example. The closed-form solutions, the computer program, the calculated results and graphical representations, the discussion and the conclusion regarding the VSTOL emergency power system, are presented.

5.2. CURRENT AND VOLTAGE WAVEFORMS

The relevant boost converter waveforms are given in Figure 5.2. The power switch operates with an on-time TN and an off-time TF. The switching between the two time intervals are exaggerated in length for both switch Q and diode D to illustrate for the switching-loss modeling to be formulated in a later section.

The power-switch current iQ and diode current iD are shown in Figures 5.2A and 5.2B. The midpoint of each pulse current has a level of Ii. The

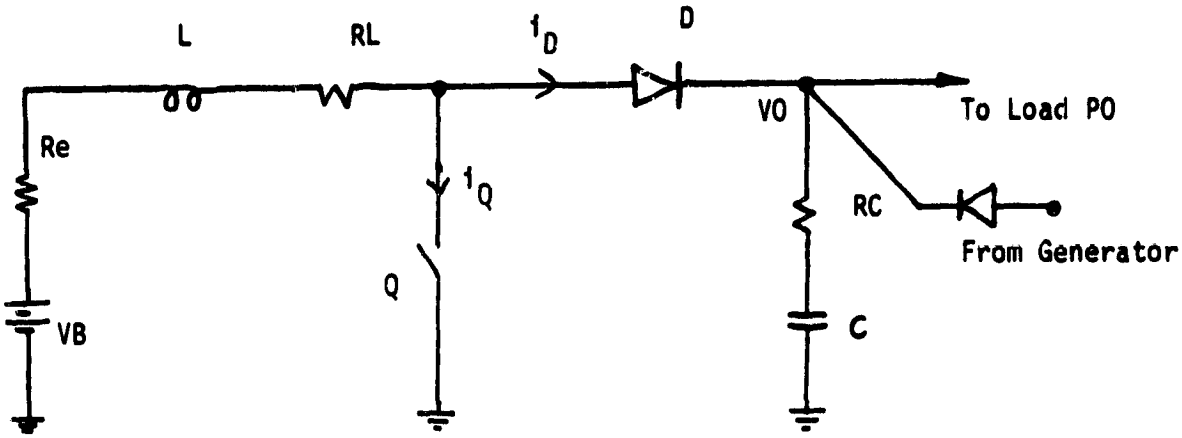


Figure 5.1 VSTOL Emergency Power System

average diode current is identical to the output load current Io. The composite waveform of Figure 5-2A and 5-2B is given in Figure 5-2C which reresents the inductor current iL as well as the converter input current. The average converter input current is therefore Ii. The difference between iD and I_0 becomes the capacitor current iC, as is shown in Figure 5-2D. The switch and diode voltage waveforms are given in Figures 5-2E and 5-2F.

5.3. BASIC VOLTAGE AND CURRENT EXPRESSIONS

Let the following designations be made:

- D: duty cycle defined as (TN)/T
- di: peak to peak ac component in the input current
- F: switching frequency
- iC: output capacitor current
- iD: diode current
- iL: input (or inductor) current
- iQ: power-switch current
- Ii: the midpoint pulse current shown in Figure 5-2A
- L: inductance in boost converter
- PL: total loss in the converter
- PO: output power to the load
- TN: on-time of the power switch
- VI: input voltage to the converter
- VO: output voltage to the load

The following expressions can be formulated:

$$(iD)ave = \frac{PO}{VO} \tag{5-1}$$

$$Ii = \frac{PO}{VO*(1-D)} \tag{5-2}$$

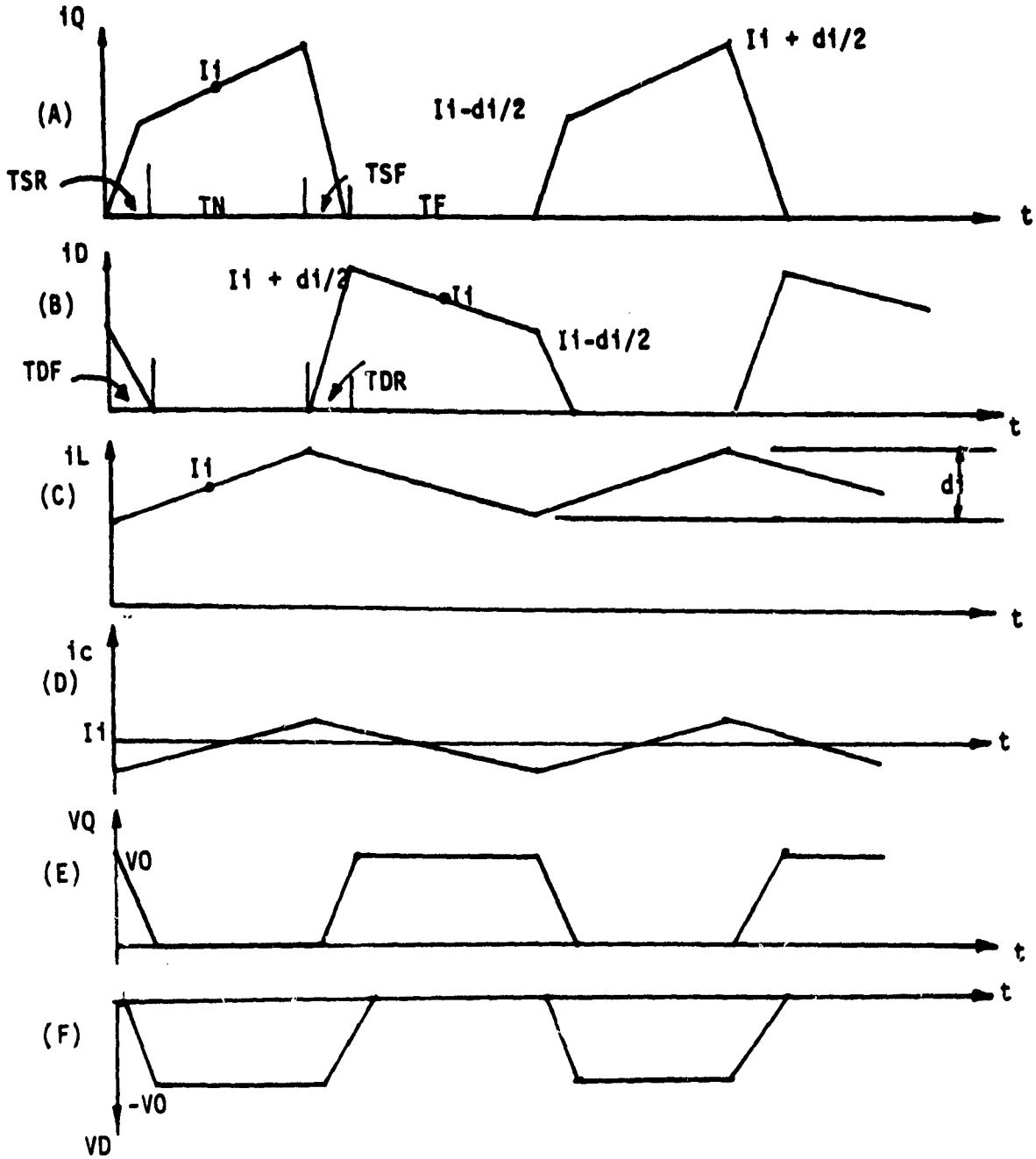


Figure 5.2 Boost Converter Key Waveforms

$$(iQ)ave = \frac{PO*D}{VO*(1-D)} \tag{5-3}$$

$$(iL)ave = Ii = \frac{PO}{VO*(1-D)} \tag{5-4}$$

$$di = \frac{VI*D}{L*F} \tag{5-5}$$

$$(iL)rms = \sqrt{\left[\frac{PO}{VO*(1-D)}\right]^2 + \left[\frac{VI*D}{L*F}\right]^2} \tag{5-6}$$

$$(iC)rms = [(Ii)^2*(1-D) - (PO/VO)^2]^{0.5} = \frac{PO}{VO}*\left[\frac{D}{1-D}\right]^{0.5} \tag{5-7}$$

Since the total input power (VI) (Ii) is equal to the sum of output Po and loss PL,

$$PO + PL = \frac{PO*VI}{VO*(1-D)} \tag{5-8}$$

From which one obtains:

$$D = 1 - \frac{PO*VI}{VO*(PO+PL)} \tag{5-9}$$

$$1 - D = \frac{PO*VI}{VO*(PO+PL)} \tag{5-10}$$

Substituting (5-9) and (5-10) into (5-2) through (5-7) one has:

$$Ii = \frac{PO+PL}{VI} \tag{5-11}$$

$$(iQ)ave = \frac{PO+PL}{VI} * \left[1 - \frac{PO*VI}{VO*(PO+PL)}\right] \tag{5-12}$$

$$(iL)ave = \frac{PO+PL}{VI} \tag{5-13}$$

$$di = \frac{VI}{L*F} * [\ 1 - \frac{PO*VI}{VO*(PO+PL)}\ ] \tag{5-14}$$

$$(iL)rms = [(iL)^2_{ave} + (di)^2]^{0.5} \approx \frac{PO+PL}{VI} \tag{5-15}$$

$$(iC)rms = \frac{PO}{VO} * [\ \frac{V\ *(PO+PL)}{VI*PO} - 1\ ]^{0.5} \tag{5-16}$$

5.4. FORMULATION OF CONVERTER LOSSES

Let: A = Cross sectional area of inductor core

AC = Winding area per turn of inductor

BDC = Intended maximum dc operating flux density level
ac flux-density excursion in the inductor core

C = Capacitance at output

F = Switching frequency

FC = Pitch factor of inductor winding

FW = Inductor core fill factor

L = Inductance

N = Number of times used in inductor

RC = ESR of C

RHO = Resistivity of inductor winding

RI = Peak-peak allowable ripple at the output

TDF = Fall time of diode during switching

TDR = Rise time of diode during switching

TSF = Fall time of power switch during switching

TSR = Rise time of power switch during switching

VB = Forward base-emitter voltage of transistor

VD = Forward drop of the diode

VS = Saturation voltage drop of the power switch

Z = Mean length of inductor core

With these descriptions defined, the following losses can be formulated.

5.4.1 INDUCTOR LOSS

The inductor loss consists of copper loss and iron loss. Based on the assumption of a toroid inductor and a square cross section for the core, the copper loss becomes:

$$PLC = (II)^2 * \text{inductor winding resistance}$$

$$= \left[\frac{PO+PL}{VI} \right]^2 * 4 * RHO * \frac{FC*N*A^{0.5}}{AC} \qquad (5\text{-}17)$$

The iron loss per switching cycle can be expressed by the area of the minor BH loop. Such a characteristic is shown in Figure 5-3. The flux excursion, Ø, can be expressed as:

$$Ø = (VO-VI)*(1-D)/(N*F)$$

$$= \frac{(VO-VI)*PO*VI}{VO*N*F*(PO+PL)} = BAC * A \qquad (5\text{-}18)$$

where

$$BAC = \frac{(VO-VI)*PO*VI}{VO*(PO+PL)*N*F*A} \qquad (5\text{-}19)$$

The ampere-turns NI corresponding to the BH loop-width H of the inductor core can be expressed as NI=Hz, where H is normally expressed in oersteds.

Since H is a nonlinear function of the switching frequency F, it can be

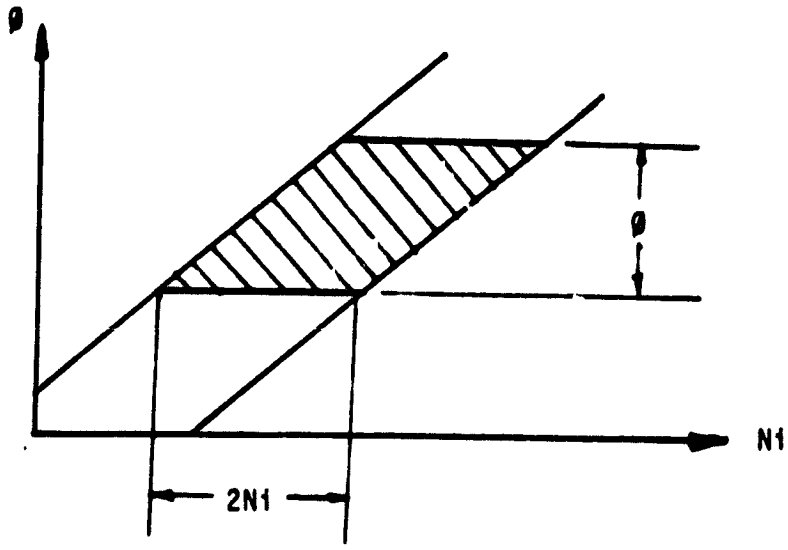


Figure 5-3 Inductor Case Characteristic

Shaded Area Represents Energy Loss Per Cycle

Since H is a nonlinear function of the switching frequency F, it can be related to F as the following:

$$H = 0.089 * F^{0.6} \quad \text{(For Permalloy powder core only)} \tag{5-20}$$

where H and F are in amp-turns/meter and hertz, respectively. The loop width is 2 Ni, or

$$2Ni = 2*H*Z \tag{5-21}$$

The iron loss becomes:

$$PLI = 2*(Ni)*\emptyset*F = 2*BAC*H*A*Z*F \tag{5-22}$$

where (BAC) and H are given in 5-19 and 5-20, respectively.

The total inductor loss is therefore:

$$PL = PLC + PLI \tag{5-23}$$

where PLC and PLI are respectively given in (5-17) [illegible] 22).

5.4.2 <u>POWER SWITCH</u>

Losses in the transistor include the con[illegible] loss, the base loss, and the switching loss. The conduction loss PTC is:

$$PTC = Ii*VS*D = \frac{PO + PL}{VI} * VS * [\ 1 - \frac{PO*VI}{VO*(PO+PL)}\ ] \qquad (5\text{-}24)$$

Assuming a 10 to 1 base current drive, the base loss is:

$$PTB = 0.1 * Ii * D * VB = 0.1 * \frac{PO+PL}{VI} * VBE * [\ 1 - \frac{PO * VI}{VO*(PO+PL)}\ ] \qquad (5\text{-}25)$$

The switching losses during turn-on and turn-off can be formulated with aid of Figure 5-2D. During turn-on, the voltage across the power switch decreases from (Vo + VD) to VS, and the current through the switch increases from zero to [(PO+PL)/VI - (di/2)]. Assuming the rate of voltage or current change during the switching interval TSR is constant, it can be shown easily that the turn-on switching loss is:

$$PTR = (1/6) * (VO+VD-VS) * (\frac{PO+PL}{VI} - \frac{di}{2}) *TSR *F \qquad (5\text{-}26)$$

During turn-off, the voltage across the power switch increases from VS to (Vo + VD), and the current decreases from [(PO+PL)/VI + di/2] to zero. Therefore, during switching interval TSF, one has:

$$PTF = (1/6) * (VO+VD-VS) * (\frac{PO+PL}{VI} + \frac{di}{2}) * TSF * F \qquad (5\text{-}27)$$

Realizing the opposite signs associated with the di/2 term in (5-26) and (5-27), one makes the simplifying assumption of equal TSR and TSF, and the

C-4

sum of switching losses becomes:

$$PTR + PTF = (1/6)*(VO+VD-VS)*\frac{PO+PL}{VI}*(TSR+TSF)*F \qquad (5\text{-}28)$$

By summing up (5-24) (5-25) and (5-28) the total loss in the power switch becomes:

$$PT = PTC + PTB + PTR + PTF$$

$$= \frac{PO+PL}{VI}\left[1-\frac{PO*VI}{VO*(PO+PL)}\right]*(vs+0.1*VBE)+(VO+VD-VS)*(TSR+TSF)*F/6 \qquad (5\text{-}29)$$

5.4.3 <u>DIODE LOSS</u>

The diode conduction loss is:

$$PDC = Ii * VD * (1-D) = PO * VD/VO \qquad (5\text{-}30)$$

Essentially following the same derivation for the power-switch switching loss, the diode switching loss becomes:

$$PDR + PDF = (1/6)*(VO+VD-VS)*\frac{PO+PL}{VI} * (TDR+TDF)*F \qquad (5\text{-}31)$$

The total diode loss is:

$$PD = PDC + PDR + PDF$$

$$= \frac{PO*VD}{VO} + (VO+VD-VS)\frac{PO+PL}{VI}*(TDR+TDF)*F/6 \qquad (5\text{-}32)$$

5.4.4 CAPACITOR LOSS

The capacitor loss PC is:

$$PC = (iC)^2_{rms} * RC = \left(\frac{PO}{VO}\right)^2 * RC * \left[\frac{VO*(PO+PL)}{VI*PO} - 1\right] \qquad (5\text{-}33)$$

5.4.5 OTHER CONVERTER LOSSES

The total converter loss in the control circuit, housekeeping circuit, wires and connectors is assumed to be 1.5% of the total output power, i.e.,

$$POT = 0.015 * PO \qquad (5\text{-}34)$$

5.4.6 TOTAL CONVERTER LOSS

The total converter loss can be obtained by summing up (5-17), (5-22), (5-29), (5-32), (5-33) and (5-34):

$$PL = \left(\frac{PO+PL}{VI}\right)^2 * 4 * RHO * \frac{FC * N * A^{0.5}}{AC}$$

$$+ 2 * \frac{(VO-VI)*PO*VI}{VO*(PO+PL)*N*A*F} * 0.089*F^{1.6} *A *Z$$

$$+\frac{PO+PL}{VI} \left[1- \frac{PO*VI}{VO*(PO+PL)}\right]*(VS+0.1*VBE)+(VO+VD-VS)*(TSR+TSF)*F/6$$

$$+ \frac{PO * VD}{VO} + (VO+VD-VS) * \frac{PO+PL}{VI} * (TDR+TDF) *F/6$$

$$+ \left(\frac{PO}{VO}\right)^2 * \left[\frac{VO*(PO+PL)}{VI*PO} - 1\right] * RC$$

$$+0.015* PO \qquad (5\text{-}35)$$

With PO much greater than PL, very little error will be induced if the following simplifying approximations are made:

$$PO/(PO+PL) = 0.93$$

$$(PO+PL)^2 = 1.156 * PO^2 \qquad (5\text{-}36)$$

Substituting these approximations into(5-17)and(5-19) eq.(5-32)becomes:

$$PL = PL1/PL2$$

where:

$$PL1 = 4.624*RHO*\frac{FC*N*A^{0.5}}{AC}*\left(\frac{PO}{VI}\right)^2 + \left(\frac{PO}{VI} - \frac{PO}{VO}\right)*(VS+0.1*VB)$$

$$+ \frac{PO}{6*VI}*(VO+VD-VS)*(TSR+TSF+TDR+TDF)*F + \frac{PO*VD}{VO}$$

$$+ \left(\frac{PO}{VO}\right)^2 * RC * \left(\frac{VO}{VI} - 1\right) + 0.015 * PO$$

$$+ 0.165 * F^{0.6} * \frac{(VO-VI)*VI}{A*N*VO} *A * Z$$

$$PL2 = 1 - \frac{VS+0.1*VBE}{VI} - \frac{PO*RC}{VO*VI}$$

$$- \frac{VO+VD-VS}{VI*6} * (TSR+TSF+TDR+TDF) * F \qquad (5\text{-}37)$$

5.5. FORMULATION OF CONSTRAINTS

The following constraints are to be observed:

- The input current ac component must be limited to below a certain peak-to-peak amplitude.
- The inductor should not operate in the saturation region.
- The output voltage ripple must be limited to below a certain peak-to-peak amplitude.
- The core must have sufficient window area to accomodate all the windings.

These constraints are formulated as follows:

5.5.1 PEAK-TO-PEAK INPUT AC COMPONENT

The peak-to-peak ac component has been expressed as di in eq.(5-14). Let the maximum amplitude be specified as IAC, then,

$$IAC \geq \frac{VI}{L*F} * [1 - \frac{PO*VI}{(PO+PL)*VO}] \qquad (5\text{-}38)$$

5.5.2 BELOW INDUCTOR SATURATION FLUX DENSITY

This constraint specifies that at the peak inductor current, the corresponding flux density in the core should be below a certain predetermined level, (BDC). Consequently,

$$N * A - L * IP/BDC \geq 0$$

$$IP = Ii + di/2 = \frac{PO+PL}{VI} + \frac{VI}{2*L*F} * [1 - \frac{PO * VI}{VO*(PO+PL)}] \qquad (5\text{-}39)$$

where N and A are the turns and the area of the inductor core.

5.5.3 OUTPUT VOLTAGE RIPPLE

The peak-to-peak output-voltage ripple is caused by two components: the capacitive component due to the ampere-second processed by C and the resistive component due to the ESR RC of C. It can be shown that the constraint concerning the sum of these two components can be expressed as:

$$RI \geq (I1 + d1/2) * RC + PO*D/(2*VO*C*F)$$

$$RI \geq \frac{PO+PL}{VI} * RC + \frac{1}{2*F} * [1 - \frac{PO*VI}{VO*(PO+PL)}]*(\frac{VI*RC}{L} + \frac{PO}{VO*C})$$

where RI is the peak-to-peak ripple specification. In actual design, series-parallel combination of capacitors may be needed in order to meet the voltage and ripple requirements. However, the product (RC * C) will always remain a constant value regardless of the combination used. For example, three different combinations of capacitors are given in Figure 5-4. Capacitance C and resistance RC are associated with each individual capacitor. It can be easily proved that the equivalent RC product for all three connections are identical, and are equal to RC * C. Let this constant value be designated G for a given capacitor type, one has:

$$RI \geq \frac{PO+PL}{VI} * \frac{G}{C} * \frac{1}{2*F} * [1 - \frac{PO*VI}{VO*(PO+PL)}] * (\frac{VI*G}{L*C} + \frac{PO}{VO*C}) \qquad (5\text{-}40)$$

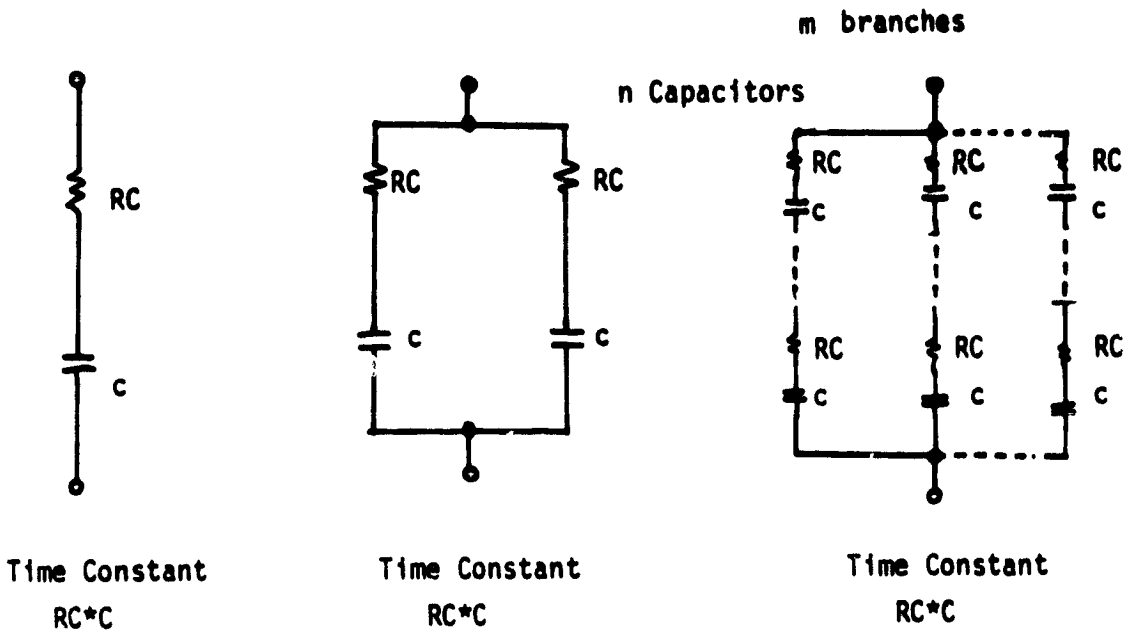


Figure 5-4 Different Capacitor Connections with identical time constant RC*C.

5.5.4 SUFFICIENT WINDOW AREA

Assuming a toroid core and a square cross-sectional core area, then, for a mean length Z, the window radius will be $(Z/(2*3.1416) - A^{0.5}/2)$.

The window area becomes $3.1416*[Z/(2*3.1416) - A^{0.5}/2]^2$. This area, multiplied by window fill factor FW, must be sufficient for all the inductor windings, which has a total area of N*AC. Consequently,

$$N*AC \leq \pi * FW * \left(\frac{Z}{2*\pi} - \frac{A^{0.5}}{2} \right)^2$$

$$\left(\frac{N * AC}{\pi * FW} \right)^{0.5} - \frac{Z}{2*\pi} + \frac{A^{0.5}}{2} \leq 0 \qquad (5\text{-}41)$$

5.6. SIMPLIFICATION OF CONSTRAINTS FOR CLOSED-FORM OPTIMIZATION

In equations (5-38) to (5-40), power loss PL is always associated with an output power PO. Admittedly, PL is a highly complicated function of many variables, as indicated in eq. (5-37). If one seeks a closed-form optimization using the aforementioned constraints, the parameter PL must not be treated in accordance with (5-37). Rather, and indeed

fortunately so, little error will be introduced to these constraints if PL is given a reasonable numerical value, and used to derive variables such as L, C, RC, N, A, etc. These known values can then be substituted into(5-37)to represent a more precise PL. In essence, an iteration of PL based on a reasonable approximation will be utilized for the sake of enhancing closed-form optimization. Numerically, the iterative approximation is justified by considering that from (5-38) to (5-40), PL is always associated with PO in the form of (PO + PL)/PO, which is close to unity due to the fact that PO is generally much greater than PL. For example, a 10% error in assigning a numerical PL would only result in about 1% error for (PO + PL)/PO. Consequently, the variables to be thus obtained are only subjected to a rather insignificant error, which in turn, will introduce only a relatively small error for the precise expression for PL when the various variables are eventually deployed in(5-37). Consequently, a numerical PL = 0.07 * PO will be used in(5-38)to(5-41)in quest for closed-form optimization, and equations(5-38)to(5-40)become:

$$L \geq \frac{VI*[1-VI/(1.07*VO)]}{IAC * F} \tag{5-42}$$

$$N*A \geq \frac{L}{BDC} * [\frac{1.07*PO}{VI} + \frac{VI}{2*L*F} * (1 - \frac{VI}{1.07*VO})] \tag{5-43}$$

$$C \geq \frac{1}{RI} * [\frac{1.07*PO*M}{VI} + \frac{1}{2*F} * (1- \frac{VI}{1.07*VO})*(\frac{VI*M}{L} + \frac{PO}{VO})] \tag{5-44}$$

In eqs. (5-42) to (5-44), the terms IAC, BDC, and RI, Voltage VO, and power PO, are specified parameters. Consequently, given an input voltage VI and frequency F, both L, N*A, C, and RC can be determined numerically. Substituting these values into (5-37) reduces it into the following:

$$PL = \frac{K1*N*A^{0.5}}{AC} + K2*A*Z + K3 \tag{5-45}$$

where constants K1, K2, and K3 are:

$$K1 = \frac{4.624 * RHO * (PO/VI)^2 * FC}{K4} \tag{5-46}$$

$$K2 = \frac{0.165 * F^{0.6} *(VO-VI)*VI/(VO*A*N)}{K4} \tag{5-47}$$

$$K3 = \frac{\left(\frac{PO}{VI} - \frac{PO}{VO}\right)*(VS+0.1*VB)+\frac{PO}{6*VI}(TSR+TSF+TDR+TDF)*F*(VO+VD-VS)+0.015*PO + \frac{PO*VD}{VO} + \left(\frac{PO}{VO}\right)^2*RC*\left(\frac{VO}{VI} -1\right)}{K4} \tag{5-48}$$

$$K4 = 1 - \frac{VS+0.1*VBE}{VI} - \frac{VO+VD-VS}{6*VI} * (TSR+TSF+TDR+TDF)*F - \frac{PO*RC}{VO*VI} \tag{5-49}$$

5.7. BATTERY WEIGHT

In order to formulate battery weight, let the following parameters be defined:

n : Number of Ni-Cd cells in series within the battery

RE : Total effective resistance internal to battery

re : Effective resistance of each cell, i.e., RE=n(re)

T : Anticipated emergency power utilization time

VB : Battery voltage before the internal drop across RE

Vk : Individual cell voltage, i.e., VB=n(Vk)

With reference to Fig. 5-1,

$$VB = VI + \frac{PO+PL}{VI} * n * re = n * Vk \tag{5-50}$$

$$n = \frac{VI}{Vk} * [\, 1 - \frac{re * (PO+PL)}{VI*Vk} \,]^{-1}$$

The total power drawn from the battery becomes

$$PB = PO + PL + (\frac{PO+PL}{VI})^2 * n * re$$

$$= PO + PL + \frac{(PO+PL)^2 * re}{VI*Vk} * [\, 1 - \frac{(PO+PL) * re}{VI*Vk} \,]^{-1} \tag{5-51}$$

The voltage required from the battery is:

$$VB = PB/Ii = VI + \frac{(PO+PL) * re}{Vk} * [1 - \frac{(PO+PL)*re}{VI*Vk} \,]^{-1}$$

$$= VI + \frac{0.015*m*VI}{Vk} * [1 - \frac{0.015*m}{Vk} \,]^{-1} \tag{5-52}$$

(see eq. (5-56) later)

The battery ampere-hour capacity required is:

$$AH \geq \frac{PB * T}{VI*m} \qquad \begin{array}{l} m = 1.0 \text{ for } T=1 \\ m = 0.9 \text{ for } T=0.5 \end{array} \qquad (5\text{-}53)$$

where m represents the reduction of cell capacity due to more than 1C discharge. Using the General Electric Ni-Cd Handbook as a reference, the individual cell weight is essentially a linear function of its ampere-hour (AH) rating. Let Wk be the individual cell weight, then,

$$Wk = K * AH = \frac{K*T*PB}{VI*m} \qquad (5\text{-}54)$$

where $K \simeq 42$ grams/(amp-hr) for Ni-Cd cells. Combining(5-50)and (5-54) the total battery weight is therefore:

$$WB = n * Wk = \frac{K*T*PB}{VI*m} * \left[1 - \frac{(PO+PL)*re}{VI*Vk}\right]^{-1} \qquad (5\text{-}55)$$

Since it is also known that resistance (re) is inversely proportional to the cell size, and is within a range of 10 - 15 millivolts per C rate of discharge, one has

$$re \approx \frac{0.015*VI*m}{PB} \tag{5-56}$$

Substituting (5-56) to (5-55) gives the total cell weight as:

$$\frac{K*T*PB}{m*Vk} * \left[1 - \frac{0.015*m*(PO+PL)}{Vk*PB}\right]^{-1}$$

The total battery weight is greater than the cell weight by an amount depending on battery packaging, with the difference likely to increase with the number of cells used in series. Modeling the packaging weight by by $n^{0.02}$, the battery weight becomes:

$$WB = \frac{K*T*PB}{m*Vk} * \left[1 - \frac{0.015*m*(PO+PL)}{Vk*PB}\right]^{-1} * n^{0.02} \tag{5-57}$$

5.8. OPTIMIZATION OBJECTIVE FUNCTION

As previously stated, the objective of the optimization is to minimize the weight of the battery-converter system shown in Figure 5-1. The total system consists of the following three weight contributors:

- Converter: magnetic and capacitive components
- Battery
- Converter mechanical structure incorporating thermal design

5.8.1 CONVERTER COMPONENT WEIGHT

The converter magnetic weight is:

$$WM = 4 * FC * AC * DC * N * A^{0.5} + DI * A * Z \qquad (5\text{-}58)$$

where these parameters were all defined in Section 4, with the two terms on the right hand side of (5-58) representing copper weight and iron weight of the inductor, respectively. The converter capacitor weight is:

$$WC = KCAP * C \qquad (5\text{-}59)$$

where KCAP is a constant expressed as grams per microfarad of capacitance for a specified capacitor type and voltage rating at a prescribed temperature. For this application, foil-tantalum capacitor is tentatively chosen. Taking into consideration the 400V rating required to provide a proper derating for a 270V working dc voltage, the KCAP for this application is taken as 3 grams /microfarad. From (5-58) and (5-59) the total converter component weight becomes:

$$WCON = 4*FC*AC*DC*N*A^{0.5} + DI*A*Z + KCAP*C \qquad (5\text{-}60)$$

5.8.2 BATTERY WEIGHT

The battery weight, WB, was defined in (5-57).

5.8.3 CONVERTER MECHANICAL STRUCTURE WEIGHT

For the first order of approximation, the converter mechanical structure weight, taking thermal design into consideration, is assumed to be directly proportional to the converter output power PO and loss PL.

$$WP = KMEC*PO + KTHE*PL \tag{5-61}$$

KMEC and KTHE are proportionality constants. For this application, KMEC is estimated at 5 grams/watt, and KTHE at 10 grams/watt.

5.8.4 OPTIMIZATION OBJECTIVE FUNCTION

The objective function "OBJF" is the sum of eqs.(5-57) (5-60) and (5-61). Analytically,

$$\begin{aligned} OBJF &= WB + WCON + WP = WT \\ &= \frac{K*T*PB}{m*Vk} * \left[1 - \frac{0.015*m*(PO+PL)}{Vk*PB}\right]^{-1} * n^{0.02} \\ &\quad + 4*FC*AC*DC*N*A^{0.5} + DI*A*Z + KCAP*C \\ &\quad + KMEC*PO + KTHE*PL \end{aligned} \tag{5-62}$$

Strictly for convenience, the parameters in(5-62)are clarified again as follows:

K : Proportionality constant between individual cell weight and its ampere-hour rating (42 grams/ampere-hour).

KTHE: Weight constant for thermal design (10 grams/watt of loss).

T : Anticipated emergency power utilization time (hours).

PO : Required emergency output power (watts).

PL : Converter losses (watts).

m : Cell capacity reduction when discharging more than 1C, where C in amperes is equivalent to the ampere-hours rating of the cell.
For a half-hour discharge application, m= 0.9.

Vk : Individual cell voltage (volts, 1.00V for a Ni-Cd cell).

FC : Winding pitch factor (assumed to be 2.0).

AC : Inductor winding area (square meters).

DC : Conductor density (8900 kg/m^3 for copper, or, 8.9×10^6 g/m^3)

N : Number of turns of the inductor winding (dimensionless).

A : Cross-sectional area of inductor core (square meters).

DI : Core density (7800 kg/m^3 for iron, or, 7.8×10^6 g/m^3)

Z : Mean core length (meters).

KCAP: Weight constant for capacitors (3 grams /microfarad).

C : Output capacitance (microfarads).

KMEC: Weight constant for mechanical structure (5.0 grams/watt of converter output power).

Having clarified these parameters, they can be catagorized as follows:

- Specified system requirements: T, PO, m.
- Given cell characteristics: K, Vk.
- Assumed constants: FC, DC, DI, KCAP, KMEC.
- Previously calculated parameter: C (see eq. (5-44).
- Unknowns : PL, AC, N, A, Z.

Separating (62) into known and unknown terms, one has:

$$WT = \left[\frac{K*T*PO*n^{.02}}{m*Vk}\left[1-\frac{.015*m*(PO+PL)}{Vk*PB}\right]^{-1} + KCAP * C + KMEC*PO\right]$$
$$+ \left[\frac{K*T*n^{0.02}}{m*Vk}\left(1-\frac{.015*m*(PO+PL)}{Vk*PB}\right)^{-1} + KTHE\right] * PL \qquad (5\text{-}63)$$
$$+ 4*FC*AC*DC*N*A^{0.5} + DI*A*Z$$

$$WT = [CONST\ 1] + [CONST\ 2]*PL + 4*FC*AC*DC*N*A^{0.5} + DI*A*Z \qquad (5\text{-}64)$$

where CONST 1 and CONST 2 are two constants representing, respectively, the quantities in the two square brackets on the right-hand side of (63).

It is recalled that PL of(5-63)was expressed as a function of the other unknowns in(5-45). Combining(5-45)and(5-64)and simplifying the resultant equation, one has:

$$WT = (CONST\ 1 + K3 * CONST\ 2)$$
$$+ CONST\ 2 * K1 * N * A^{0.5}/AC$$
$$+ 4*FC*DC*AC*N*A^{0.5} + (DI + K2*A*Z*CONST\ 2) \qquad (5\text{-}65)$$

where K1, K2, and K3 were given in (5-46) to (5-49). Equation (5-65) is the objective function to be optimized. The unknowns in (65) are N, A, AC, and Z. For simplicity in programming, (PO+PL)/PB in (5-63)is treated as unity.

5.9. REVIEW OF OPTIMIZATION CONSTRAINTS

It is recalled that in Section 5.5 there were four constraints.

For a given VI and F, one constraint concerning the input current ripple resulted in the numerical identification of inductance L in (5-42). Another constraint regarding the output-voltage ripple made possible the design for the capacitance C in (5-44). The two remaining constraints on core window and output ripple are listed below for convenience:

$$\left(\frac{N*AC}{\pi*FW}\right)^{0.5} - \frac{Z}{2*\pi} + \frac{A^{0.5}}{2} \leq 0 \qquad \text{(repeat of (5-42))}$$

$$N*A \geq \frac{L*IP}{BDC} \qquad \text{(repeat of (5-43))}$$

Here, the known parameters are:

FW : Core window fill factor (assumed 0.35).

BDC : Maximum operating flux density (0.35 Weber/meter^2).

L : Inductance in Henries as calculated from the equal sign of (5-42).

VI : Converter input voltage in volts.

PO : Converter output power in watts.

F : Converter switching frequency in Hertz.

IP : Peak inductor current in amperes defined in eq. (5-39).

The unknowns are N, A, AC, and Z, which are the same ones in (5-65). Notice that the permeability of the inductor core has yet to be defined. The reason for this seeming remission is that it is really not an independent variable;

$$\text{Permeability} = U = \frac{L*Z}{N^2*A} \qquad (5\text{-}66)$$

5.10. CLOSED-FORM OPTIMIZATION SOLUTIONS

Concisely stated, for a given set of VI and F, the purpose of this optimization is to identify all variables N, A, AC, and Z such that eqs. (5-41) and (5-43) can be satisfied, and concurrently the OBJF of eq. (5-65) can be minimized. The identification of these variables numerically defines the particular power loss PL per (5-45) that will result in a minimum emergency power system weight for a given set of VI and F. The calculation can be repeated for other sets of VI and F, from which the global minimum for one particular set of VI and F can be numerically obtained along with the specific PL corresponding to this set. Substituting these values into (5-52) and (5-53) will then yield the optimum battery voltage level VB and the precise minimum battery ampere-hour rating AH.

For simplification purposes, let

$$KA = CONST\ 1 + K3 * CONST\ 2 \tag{5-67}$$

$$KB = K1 * CONST\ 2 \tag{5-68}$$

$$KC = 4 * FC * DC \tag{5-69}$$

$$KD = DI + K2 * CONST\ 2 \tag{5-70}$$

$$KE = L * IP / BDC \tag{5-71}$$

$$KF = (\pi * FW)^{-0.5} \tag{5-72}$$

$$KG = 1/(2 * \pi) \tag{5-73}$$

$$KH = 0.5 \tag{5-74}$$

$$x = A^{0.5}, \quad y = N^{0.5}, \quad v = (AC)^{0.5}, \quad z = Z \tag{5-75}$$

Then, equation(5-65)becomes:

$$WT = KA + KB * \frac{y^2 * x}{v^2} + KC * xy^2v^2 + KD * x^2z \tag{5-76}$$

Equations(5-41)and(5-43)become:

$$KF * yv - KG * z + KH * x \leq 0 \tag{5-77}$$

$$x^2y^2 - KE \geq 0 \tag{5-78}$$

Using the method of Lagrange Multipliers, the optimization function h (x, y, z, v) becomes:

$$h(x,y,z,v) = KA + KB*y^2xv^{-2} + KC*xy^2v^2 + KD*x^2z - \alpha(x^2y^2 - KE) - \beta(KF*yv - KG*z + KH*x)$$

where α and β are the Lagrange Multipliers.

$$\frac{\partial h}{\partial x} = KB*y^2v^{-2} + KC*y^2v^2 + 2*KD*xz - 2*\alpha*xy^2 - \beta*KH = 0 \tag{5-79}$$

$$\frac{\partial h}{\partial y} = 2*KB*yxv^{-2} + 2*KC*xyv^2 - 2*\alpha*x^2y - \beta*KF*v = 0 \tag{5-80}$$

$$\frac{\partial h}{\partial z} = KD*x^2 + \beta*KG = 0 \tag{5-81}$$

$$\frac{\partial h}{\partial v} = -2*KB*yxv^{-3} + 2*KC*xyv - \beta*KF = 0, \quad y \neq 0 \tag{5-82}$$

The six equations, (5-77) to (5-82), can be used to solve for the six variables, x, y, z, v, α and β:

$$N = \left(\frac{\pi*L*IP*FW}{BDC*AC} \right)^{0.5} * S^{-1} \tag{5-83}$$

$$A = \left(\frac{L*IP*AC}{\pi*BDC*FW} \right)^{0.5} * S \tag{5-84}$$

$$Z = 2*\pi*\left(\frac{L*IP*AC}{\pi*BDC*FW} \right)^{0.25} * \left(\frac{S^{0.5}}{2} + S^{-0.5} \right) \tag{5-85}$$

$$U = 2*\pi*\left(\frac{AC}{\pi*FW} \right)^{0.75} * \left(\frac{BDC}{IP} \right)^{1.25} * L^{-0.25} * S * \left(\frac{S^{0.5}}{2} + S^{-0.5} \right) \tag{5-86}$$

$$AC = \left[\frac{-b \pm (b^2 - 4*a*c)^{0.5}}{2*a} \right]^{0.5}, \quad AC < \left(\frac{CONST\ 2 * K1}{4*FC*DC} \right)^{0.5} \tag{5-87}$$

$$S = \frac{FW*[K1*\ CONST\ 2/(AC)^2 - 4*FC*DC]}{DI + K2*CONST2} > 0 \tag{5-88}$$

$$a = 12*FC*DC*\left(4*FC*DC - \frac{DI+K2*CONST2}{FW}\right) \tag{5-89}$$

$$b = CONST2*K1* \left(\frac{DI+K2*CONST2}{FW} - 24*FC*DC\right) \tag{5-90}$$

$$c = 3 * (K1 * CONST\ 2)^2 \tag{5-91}$$

Values thus obtained for N, A, Z, and AC can be used in eq(5-45) to numerically determine the power loss PL.

5.11. APPROACH FOR OVERALL OPTIMIZATION

At this juncture it is perhaps worthwhile to review briefly what has been accomplished. First, one has to realize that the optimization study so far has been predicated by a given set of VI and F. Based on such a given set, the progression includes the following:

- The numerical identification of inductance L through eq. (5-42).
- The numerical identification of capacitance C through eq. (5-44).
- The detailed design for inductance L through eqs. (5-83) to (5-91). Details include N, A, Z, and AC.
- The determination of loss PL through eqs. (5-45) to (5-49). Such a PL will give a minimum total system weight.
- The battery voltage VB can be found from eq. (5-52).
- The battery ampere-hour rating AH can be found from eq. (5-53).
- The minimum total system weight is prescribed by eq. (5-64).

It is iterated that the minimum weight of (5-64) applies only to the given set of VI and F. Different minimum weights corresponding to different sets of VI and F can be similarly generated. By plotting this weight as a function of F, with VI as the varying parameter, a family of curves can be displayed to identify the global minimum for one specific set of VI and

F. The global minimum represents the optimum design for all battery and converter parameters, and the corresponding battery voltage level can be determined from the specific VI.

5.12. COMPUTER PROGRAM FOR DESIGN OPTIMIZATION CALCULATION

The foregoing design optimization equations are transcribed into a computer program for numerical processing. The program is given as Appendix K. A total of 28 parameters are given to the program in statements 2200 to 2230. Their corresponding numerical values are provided in statements 2000 to 2030. For a cost-effective program,no tolerances are assumed for these parameters as was indicated in statements 2100 to 2130. The program is designated as "VSTOL" in 2300. The output data of the design optimization program, as specified in 2400, include the following:

L	:	inductance in henries
C	:	capacitance in farads
RC	:	equivalent series resistance of C in ohms
IP	:	peak inductor current in amperes
N	:	number of turns of L
A	:	cross-section area of the core for L in meter^2
Z	:	mean core length in meter
U	:	core permeability in gauss/oersted
AC	:	winding area per turn in meter^2
PL	:	total converter loss in watts
PLC	:	copper loss of inductor in watts
PLI	:	iron loss of inductor in watts
PM	:	total inductor loss in watts
PT	:	total loss of transistor switch in watts
PD	:	total diode loss in watts
PC	:	total capacitor loss in watts

P	:	Other converter losses in watts
NB	:	number of cells in series
VB	:	minimum battery voltage near end of discharge in volts
WM	:	inductor weight in grams
WP	:	converter packaging weight in grams (excluding power components)
WC	:	converter component and packaging weight in grams
WB	:	battery weight in grams
WCON	:	converter weight in grams
WT	:	total power system weight in grams
AH	:	ampere-hour capacity required of the battery

From statements 3000 to 3064, the program essentially reproduces the various equations presented in the text, with the following correspondences:

Statement in Program	Equation in Text
3000	5-42
3002	5-44
3004	RC*C=G
3006	5-49
3008	5-46
3010	5-43
3012	5-47
3014, 3016, 3018	5-48

3020	CONST 1 of (5-64)
3022	CONST 2 of (5-64)
3024	5-89
3026	5-90
3028	5-91
3030	5-87
3032	5-88
3034	5-39
3036	5-83
3038	5-84
3040	5-85
3042	5-66
3044	5-45
3045	5-17
3046	5-50, 5-56
3047	5-19
3048	5-52
3049	5-18,5-19 5-20, 5-21, 5-22
3050	5-58
3052	5-59
3053	5-65
3054	5-23
3056, 3058	5-29
3060	5-32
3062	5-33

The numerical inputs to the computer are given as follows:

VI	A0	150	0	TDR	B4	.15E-06	0
F	A1	5000	0	TDF	B5	.15E-06	0
VO	A2	270	0	RHO	B6	.1728E-07	0
PO	A3	3000	0	FC	B7	2	0
T	A4	.5E+00	0	FW	B8	.35E+00	0
G	A5	.188E-04	0	BDC	B9	.35E+00	0
IAC	A6	4	0	K	C0	42	0
RI	A7	6	0	M	C1	.9E+00	0
VS	A8	1.8	0	VK	C2	1	0
VBE	A9	1.2	0	KCAP	C3	3	0
VD	B0	1.2	0	KNEC	C4	5	0
PI	B1	3.1416	0	DC	C5	6700000	0
TSR	B2	.35E-06	0	DI	C6	7800000	0
TSF	B3	.35E-06	0	KTHE	C7	10	0

As previously outlined, a set of VI and F will be assigned for each computer run, and the corresponding printout represents the optimum-weight design for that particular set of VI and F.

5.13. COMPUTER PRINTOUTS

A sample printout is shown in Figure 5-5. The aforementioned twenty-six parameters are printed under the heading of "X-AXIS", and their numerical values under "OUTPUT". Since tolerances have not been given to the program, the number "0" will appear under "+ TOL" and "- TOL", and the lower limit "- LIM" and upper limit "+ LIM" will exhibit identical numerical values as those displayed under "OUTPUT".

A summary of arguments and tolerances accompanies each printout. For example, in the sample printout the output voltage VO is designated A2, and has a specified value of 270V with zero tolerance. The particular run is based on an input voltage VI of 150V, switching frequency F of 10 kHz, output power PO of 3000W, and power utilization time T of 0.5 hour. (See underlined portion of Figure 5-5). The total optimum system weight, WT, is calculated to be 103.9 kilograms.

Computer printouts for other sets of VI, F, PO, and F.

VI = 25, 50, 100, 150, 200 V

F = 5, 10, 20, 30, 40, 50, 100 kHz for each VI

PO = 3000W

T = 0.5 hr.

The calculated results for total system weight WT are presented in Figure 5-6. A family of curves showing weight versus frequency, with the input voltage as the varying index, are plotted. These results will be discussed in the next section.

WORST CASE ANALYSIS	OUTPUT	-TOL.	<	+TOL.	-LIM.	LIM.
L	1.80296E-03	.00		.00	1.8030E-03	1.8030E-03
L	1.17838E-04	.00		.00	1.1784E-04	1.1784E-04
RC	1.59542E-01	.00		.00	1.5954E-01	1.5954E-01
IR-AX	2.34000E+01	.00		.00	2.3400E+01	2.3400E+01
N	1.36572E+02	.00		.00	1.3657E+02	1.3657E+02
A	8.82619E-04	.00		.00	8.8262E-04	8.8262E-04
Z	2.44638E-01	.00		.00	2.4464E-01	2.4464E-01
U	2.13209E+01	.00		.00	2.1321E+01	2.1321E+01
AL	4.66877E-06	.00		.00	4.6688E-06	4.6688E-06
FL	1.65200E+02	.00		.00	1.6520E+02	1.6520E+02
FLC	5.34931E+01	.00		.00	5.3493E+01	5.3493E+01
FLI	5.06073E+00	.00		.00	5.0607E+00	5.0607E+00
FM	5.85538E+01	.00		.00	5.8554E+01	5.8554E+01
FT	2.58134E+01	.00		.00	2.5813E+01	2.5813E+01
FD	1.61757E+01	.00		.00	1.6176E+01	1.6176E+01
FC	1.77095E+01	.00		.00	1.7710E+01	1.7710E+01
F	4.50000E+01	.00		.00	4.5000E+01	4.5000E+01
WB	1.52053E+02	.00		.00	1.5205E+02	1.5205E+02
VB	1.52053E+02	.00		.00	1.5205E+02	1.5205E+02
WM	3.03294E+03	.00		.00	3.0329E+03	3.0329E+03
WF	1.66520E+04	.00		.00	1.6652E+04	1.6652E+04
WL	3.53513E+02	.00		.00	3.5351E+02	3.5351E+02
WB	8.39119E+04	.00		.00	8.3912E+04	8.3912E+04
WCON	2.00384E+04	.00		.00	2.0038E+04	2.0038E+04
WT	1.03950E+05 grams	.00		.00	1.0395E+05	1.0395E+05
WW	1.18634E+01	.00		.00	1.1883E+01	1.1883E+01

THE ARGUMENTS AND TOLERANCES ARE:

VI	A0	150	0	TOR	B4	.15E-06	0
F	A1	10000	0	TOF	B5	.15E-06	0
VO	A2	270	0	RHO	B6	.1728E-07	0
FO	A3	3000	0	FC	B7	2	0
I	A4	.5E+00	0	FW	B8	.35E+00	0
G	A5	.188E-04	0	BOC	B9	.35E+00	0
IAC	A6	4	0	K	C0	42	0
RI	A7	6	0	M	C1	.9E+00	0
VS	A8	1.8	0	VK	C2	1	0
VBE	A9	1.2	0	KLAP	C3	3	0
VD	B0	1.2	0	KMEC	C4	5	0
PI	B1	3.1416	0	DC	C5	8900000	0
TSR	B2	.35E-06	0	DI	C6	7800000	0
TSF	B3	.35E-06	0	RTHE	C7	10	0

Figure 5-5 A Sample Computer Printout

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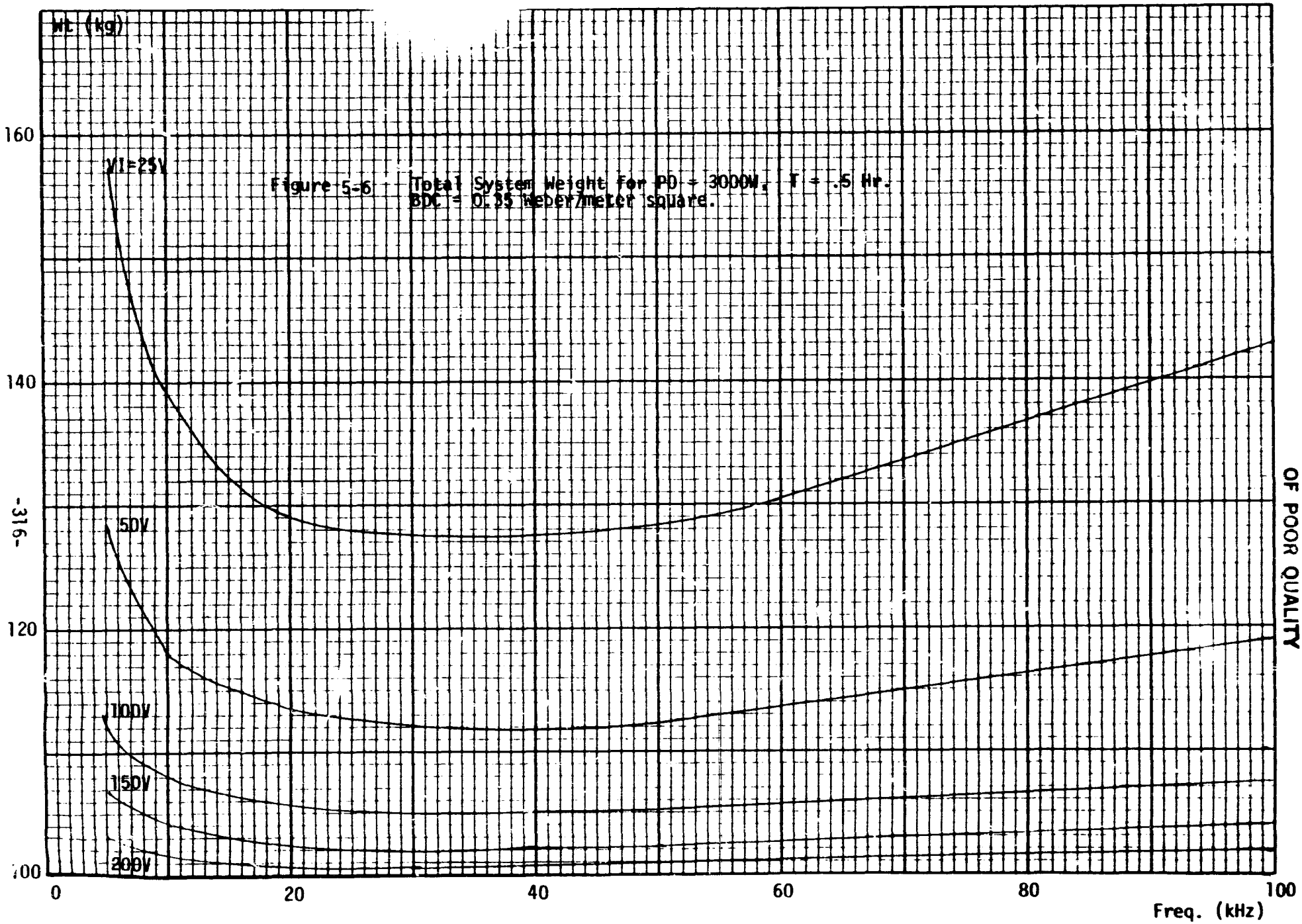

Figure 5-6 Total System Weight for PD = 3000W, T = .5 Hr.
BDC = 0.35 Weber/meter square.

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5-14. DISCUSSION OF CALCULATED RESULTS

The following observations can be made based on Figure 5-6:

1. The weight vs. frequency curves generally exhibit U-shape characteristics, with the shape more pronounced at lower input voltages. Within quite a wide frequency range, from 20 to 60 kHz, the total system weight is relatively constant for a given input voltage.

2. For each frequency, the weight reduces with an increase of input voltage. The weight reduction is most pronounced for voltage increments at lower VI's. The reduction becomes diminished for voltage increment at higher VI's. For example, at 30 kHz, a 16 kg reduction is realized when VI is increased from 25 to 50V. The corresponding reduction is only 4.5 kg for a 100-to-200V increase.

These observations are discussed as follows:

THE U-SHAPE WEIGHT VERSUS FREQUENCY

The U-shape weight versus frequency can be understood by plotting the corresponding loss versus frequency and weight distribution characteristics for all power components including the inductor, capacitor, transistor, and diode, which are part of the computer printouts. These characteristics are shown in Figures 5-7 and 5-8. It is clear from Figure 5-7 the loss versus frequency curve also exhibits the U-shape. The diminishing total loss at lower frequencies is caused by the copper loss of the inductor, which decreases as frequency increases due to the smaller inductor size for a given source-current ripple requirement. The increasing

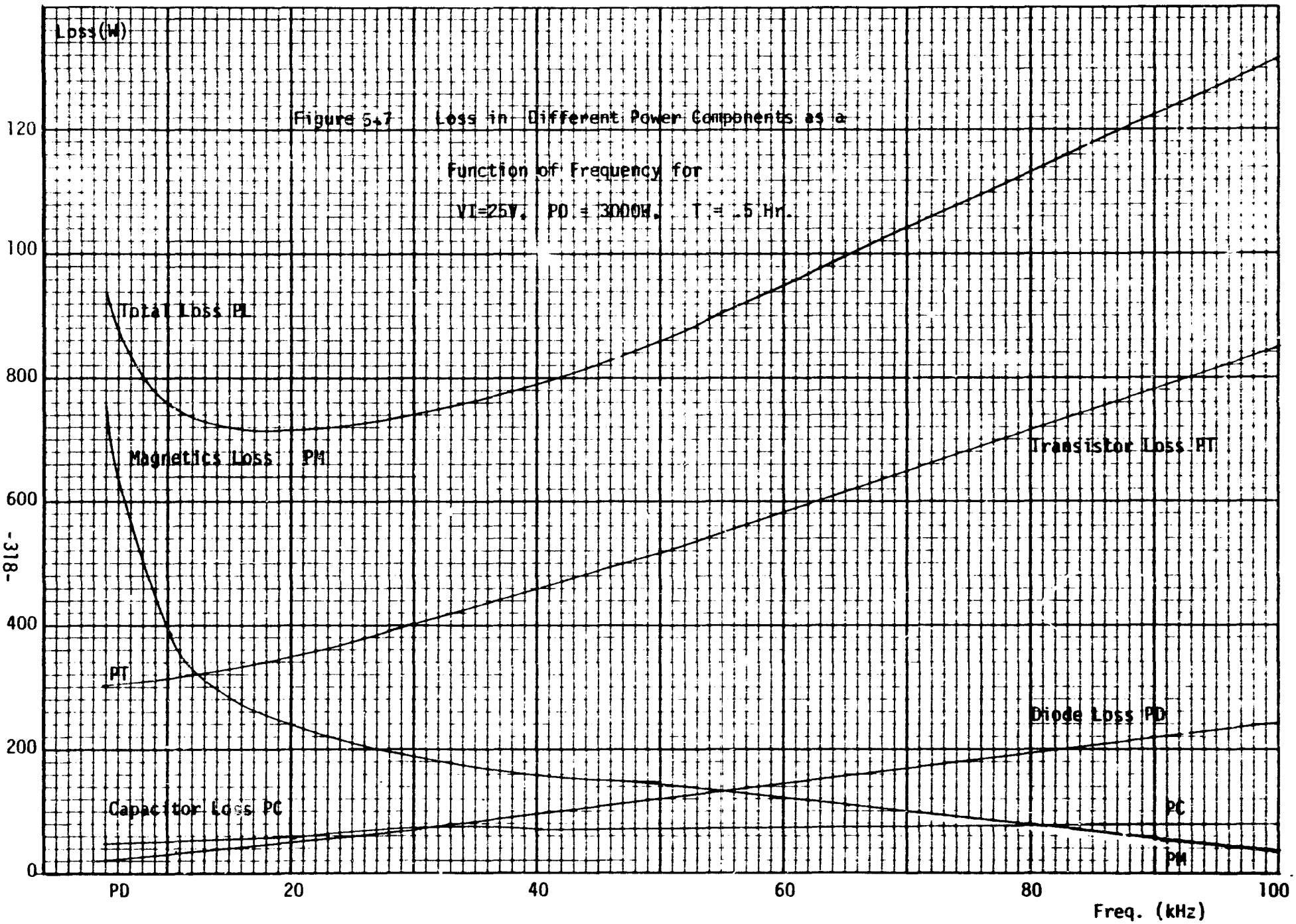

Figure 5.7 Loss in Different Power Components as a Function of Frequency for VI=25V. PO = 3000W. T = .5 Hr.

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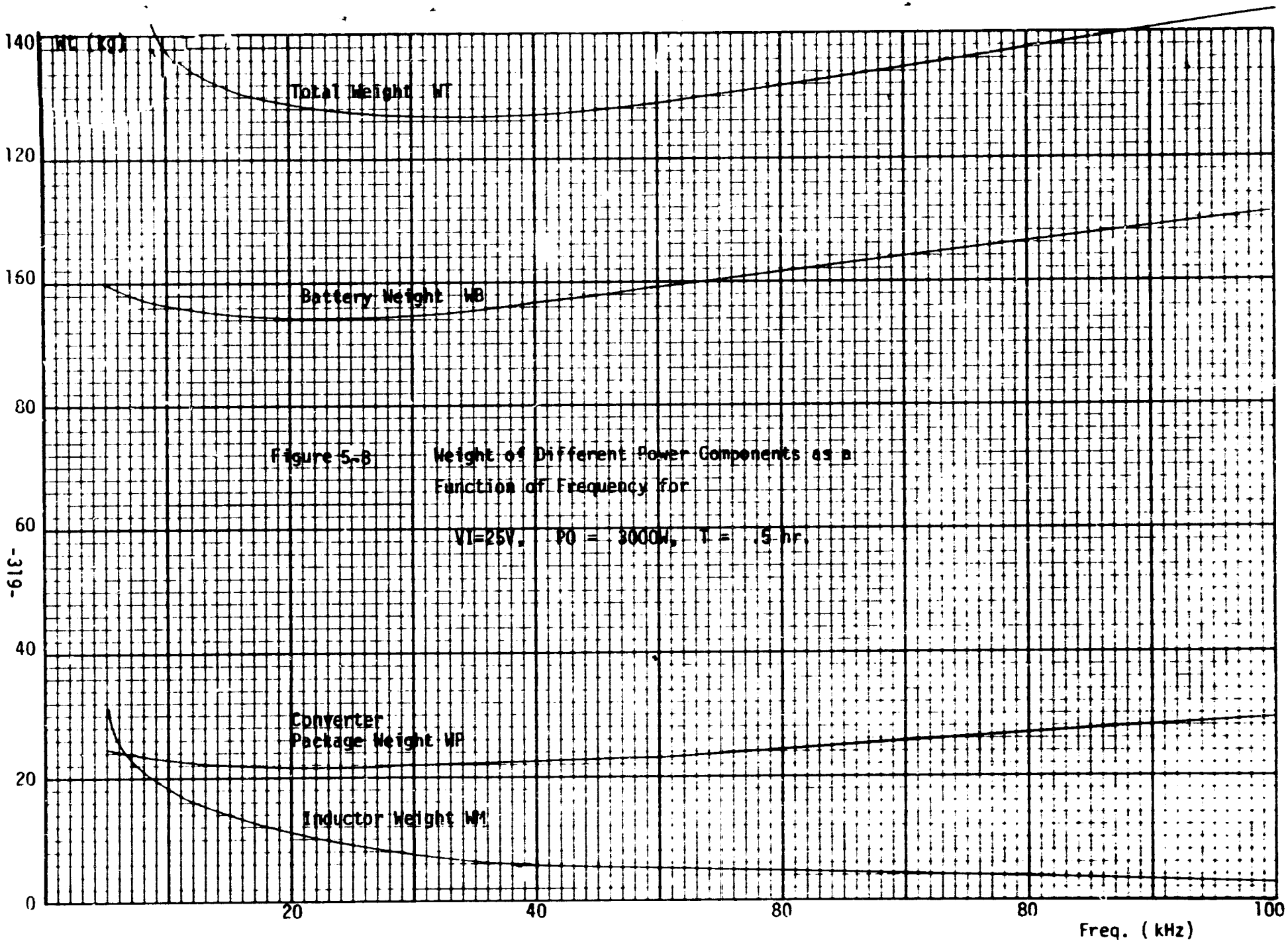

Figure 5-8 Weight of Different Power Components as a Function of Frequency for VI=25V, PO = 3000W, T = .5 hr.

total loss at higher frequencies is caused by the higher switching losses associated with the transistor and diode switches. The opposing loss trends for the inductor and the semiconductor switches as a function of frequency leave a minimum total loss in the 10 - 30 kHz frequency range. The weight profiles shown in Figure 5-8 is directly influenced by the corresponding losses. A monotonically reducing inductor weight as a function of frequency is argumented by increasing weights from both the battery and the converter packaging, thus explaining the aforementioned U-shape. Since the inductor losses and the semiconductor switching losses are more pronounced when the input voltage is low and the corresponding rms and peak current in the inductor as well as the semiconductors are high, the U-shape is also more pronounced at lower input voltages. The opposing trends of weight versus frequency for the inductor and the battery plus converter packaging leave a relatively constant total system weight in the middle frequency range, from 20 to 60 kHz.

WEIGHT REDUCTION WITH INPUT VOLTAGE

The converter loss and battery internal loss are much higher at lower input voltages. Consequently, greater weight reduction can be realized in all system components including magnetics, capacitors, battery, and converter packaging when a given voltage increment is added to a lower input voltage. As the loss-related system weight diminishes, the battery and converter packaging weights, which are constant functions of the output power, become dominant in their weight contributions to the system. Consequently, little weight saving can be realized by increasing VI when the efficiency gain is no longer an important factor. This fact is amply substantiated by curves exhibited in Figure 5-6, where the weight reduction from VI=100V to VI=200V is rather meager.

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5-15. IMPACT OF DIFFERENT CORE MATERIAL ON TOTAL SYSTEM WEIGHT

In the analysis presented so far, the inductor core is assumed to be made of the molypermalloy powder material to achieve a minimum core loss, with an operating flux-density limit of 0.35 weber/meter^2. However, in view of the high ration of copper loss PLC to core loss PLI, it becomes apparent that a different core material with a higher operating flux density level will result in saving of total system weight even though the attendent core loss will be higher. A Cut-C core of Deltamax (orthonol) laminations, with a conservative flux-density limit of 1.2 wever/meter^2 is selected to replace the power core in the computer run to assess its impact on the total system weight. This change is accomplished in the computer program through the following program edition:

```
< E,2030
  2030 DATA .35,42,.9,  1.3,5.8.9E6,7.8E6,10
  2030 DATA 1.2,42,.9,  1.3,5,8.9E6,7.8E6,10
< E,3012
  3012 Y6=.165*A1^.60*(A2-A0)*A0/Y3/A2/Y5
> 3012 Y6=4.84*A1^.26*(A2-A0)*A0/Y3/A2/Y5
< E,3049
  3049 X1=2*X0*.089*A1^.6*Z9*K0*A1
  3049 X1=2*X0*2.60*A1^.26*Z9*K0*A1
```

The flux density BDC in statement 2030 is changed from 0.35 to 1.20. The core-loss description in statements 3012 and 3049 are also changed to reflect the core-loss profile of the new material. Runs were executed. A weight versus frequency plot is given in Figure 5-9. Comparing the curve for a given VI in Figure 5-9 and Figure 5-6, it is clear that a 10 kg weight saving is accomplished for VI=25V when BDC is increased from 0.35 w/m^2 to 1.2 w/m^2 that the U-shape of weight versus frequency is not as pronounced at the low frequency end of Figure 5-9 as that of Figure 5-6. For a given VI, the inductor weight saving as a result of a higher frequency is less in Figure 5-9 in relation to that in Figure 5-6.

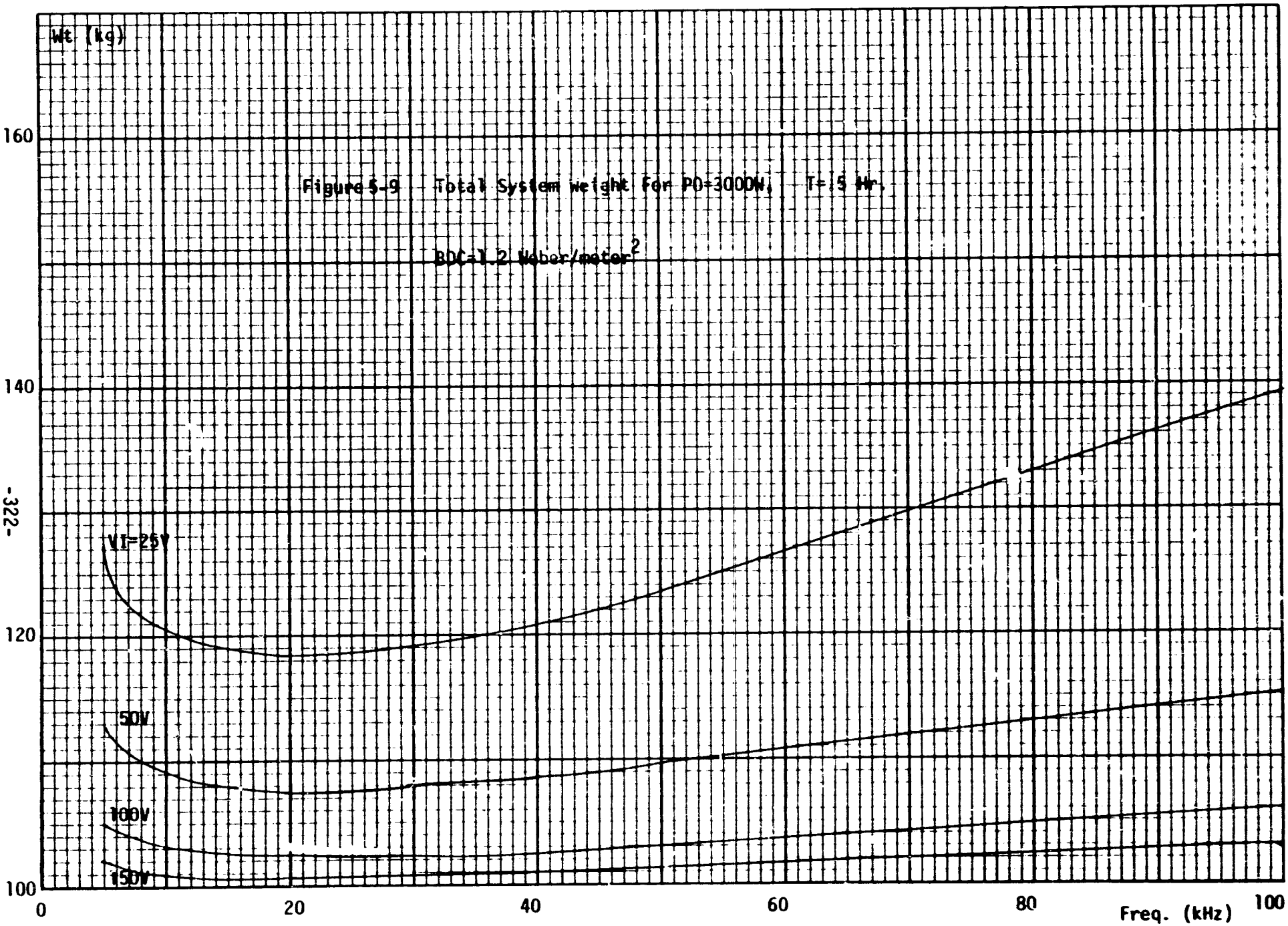

Figure 5-9 Total System weight For PO=3000W, T=.5 Hr.

BDC=1.2 Weber/meter^2

5-16. Justification For All Input Parameters

Justifications for numerical values of all input parameters to the computer are given in Appendix K. These parameters are defined in the previous sections.

5-17. CONCLUSION

From analysis presented in this report, the following design-related conclusions can be made regarding the VSTOL emergency power system:

1) As expected, the total system weight reduces with the converter input voltage. However, a level of diminishing return is soon reached for VI $\geq$ 100V.

2) For a given watt-hour rating, connecting more cells in series to effect a higher battery voltage is more costly than connecting fewer series cells. In view of the significant weight saving that can be realized by raising VI from 25V to 30V, and the rather meager weight saving that is realizable by using a higher-than-100V input voltage VI, it is recommended that the battery voltage VB be set within a 50-100V range.

3) Depending on the required output power PO, which determines the power-switch current for a given VI, a 25V battery may be used in smaller power applications, e.g., PO $\leq$ 1000 W.

4) With the present availability of power switches and magnetic core materials, the total system weight WT for a given VI stays nearly constant within a wide frequency range. The range covers from 20 to 60 kHz in Figure 5-6 and 15 to 40 kHz in Figure 5-9. A recommendable operating frequency is in the vicinity of 30 kHz.

5) For a core with BDC=1.2 weber/meter^2, the optimum system weight in kilograms can be read from Figure 5-9 as follows for PO=3 kw and T=0.5 Hr:

Switching Frequency (kHz)	Weight (kg)			
	VI=25V	50V	100V	150V
5	127kg	113kg	105kg	102kg
10	121	109	103	101
20	118	108	103	101
30	119	108	103	101
40	121	109	103	101
50	123	110	103	101
100	13[illegible]	115	106	103

6) The use of higher flux-density core material reduces the inductor copper loss by an amount much greater than the attendant increase in core loss, thus reducing the total system weight.

7) While the impact of core material is not to be overlooked, the major weight contributor in the system is the battery. Except at very low frequencies (5 kHz), the battery generally is responsible for more than 80% of the total system weight.

6. CONCLUSIONS AND RECOMMENDATIONS

The Modeling and Analysis of Power Processing Systems (MAPPS) Project has developed the mathematical models and computer software program to perform the calculation for Buck, Boost, and Buck-Boost DC-DC Converters in order to determine:

- Performance Analysis
- Design Optimization

A computer-aided discrete time domain modeling and analysis technique for Performance Analysis has been presented which is applicable to all types of switching regulators using any types of duty cycle controllers and operating with continuous, as well as discontinuous, inductor current. State space techniques are employed to characterize coverters exactly by the nonlinear discrete time domain equations in vector forms. Newton's iteration method is employed to solve for the exact equilibrium state of the converter. The system is then linearized about its equilibrium state to arrive at a linear discrete time model. The stability nature and transient responses are studied by examining the eigenvalues of the linear system. Changes in eigenvalues due to system parameter changes can be plotted in the complex z-plane yielding an excellent design tool very similar to conventional root-locus plots. The analysis is also extended to determining the frequency related performance characteristics such as the closed loop input-to-output transfer function used to determine the audiosusceptibility of the converter. The modeling and analysis approach makes extensive use of the digital computer as an analytical tool, replacing highly complex and tedious analyses by numerical method and making automation in power converter design and analysis possible.

6. CONCLUSIONS AND RECOMMENDATIONS (Cont'd)

In addition to its particular utility at analyzing high-frequency control-loop related phenomena, the analysis also serves as a useful design tool which provides design guidelines for such important control parameters as the dc loop gain, the ac loop gain, and the R-C compensation network of a two loop converter to optimize its transient response and to stabilize the system.

To those working with switching regulators, converters, and systems comprised of these equipment, certain design and analysis intricacies invariably make themselves felt throughout the equipment and system design and development stages. Empirical and intuitive reliances often intercede with the designer's desire to be "more scientific" and his commitment of being "on schedule". Handicapped by a general lack of established modling, analysis, design, and optimization tools, it has not been uncommon for a power processing designer to fulfill very little of the desire and/or the commitment.

The cost and schedule plights that most equipment and system designers find themselves in have to do with at least one of the following entities: power circuit weight/efficiency, control-related performance requirements, and trial-and-error power and control design iterations. While power processing as a technology has reached the level of sophistication where the modeling, analysis, design, and optimization of these entities should have been established, a survey of literatures conducted at the initiation of the MAPPS program had proved the contrary. In addition, the recent evolving trend of higher power and equipment standardization has further heightened the need for analytically-based design and optimization.

In this regard, the program has accomplished the following objectives:

- The methodologies of power processing modeling, analysis, design, and optimization, are all established.

6. CONCLUSIONS AND RECOMMENDATIONS (Cont'd)

- Application-oriented analysis, design, and optimization subprograms for power-circuit design, control circuit design, and control performance analysis are becoming available.
- Cost-effective system configuration study and system disturbance propagation are now feasible.

Being government sponsored, all softwares are available without proprietary complications.

Continued MAPPS effort will aim at the following goals:

- Analyze performance for commonly-used power processing equipment and selected systems.
- Detailed power circuit design optimization to meet given power-related performance requirements for most commonly-used power circuit configurations.
- Standardize control-circuit design to meet control-related performance requirements.
- Provide cost-effective tools for the identification of optimum system configurations and system failure-mode analysis.

The following is a list of basic tasks for future work:

- Application Handbook for Performance Analysis.
- Application Handbook for Design Optimization.
- Continued Current Injection Multiloop Control Modeling.
  - (a) Single Power Stage.
  - (b) Parallel Modular Power Stages.
- Continued Power Subsystem Optimization Techniques.
- Development of Performance and Design Optimization for Series Resonant Inverter Power.

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