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Interconnect Fatigue Design for Terrestrial Photovoltaic Modules

G.R. Mon
D.M. Moore
R.G. Ross, Jr.

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Prepared for
U.S. Department of Energy
Through an Agreement with
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by
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Pasadena, California

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ABSTRACT

Fatigue of solar cell electrical interconnects due to thermal cycling has historically been a major failure mechanism in photovoltaic arrays; the results of a comprehensive investigation of interconnect fatigue that has led to the definition of useful reliability-design and life-prediction algorithms are presented. Experimental data gathered in this study indicate that the classical strain-cycle (fatigue) curve for the interconnect material is a good model of mean interconnect fatigue performance, but it fails to account for the broad statistical scatter, which is critical to reliability prediction. To fill this shortcoming the classical fatigue curve is combined with experimental cumulative interconnect failure rate data to yield statistical fatigue curves (having failure probability as a parameter) which enable (1) the prediction of cumulative interconnect failures during the design life of an array field, and (2) the unambiguous--i.e., quantitative--interpretation of data from field-service qualification (accelerated thermal cycling) tests.

Optimal interconnect cost-reliability design algorithms are derived based on minimizing the cost of energy over the design life of the array field. This procedure yields not only the minimum break-even cost of delivered energy, but also the required degree of interconnect redundancy and an estimate of array power degradation during the design life of the array field. The usefulness of the design algorithms is demonstrated with realistic examples of design optimization, prediction, and service qualification testing.

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SECTION I

INTRODUCTION

Comprehensive investigations of failure modes affecting photovoltaic module performance and reliability are a major effort of the Engineering Sciences Area of the Jet Propulsion Laboratory's Flat-Plate Solar Array Project. The objective of this research is to define means of reducing the cost and improving the utility and reliability of photovoltaic modules for the broad spectrum of terrestrial applications. It is in this light that this report addresses the interconnect failure problem.

In a photovoltaic module, solar cell interconnects, made of metallic mesh or shaped ribbons, provide electrical continuity between adjacent solar cells (common terminology used throughout this report is presented in Figures 1 and 2).

Two performance considerations govern interconnect design. The first is that the voltage drop across the interconnect must not exceed a tolerable maximum value; this is achieved by sizing the cross-sectional area of the interconnect. The second is that interconnects must withstand the mechanical

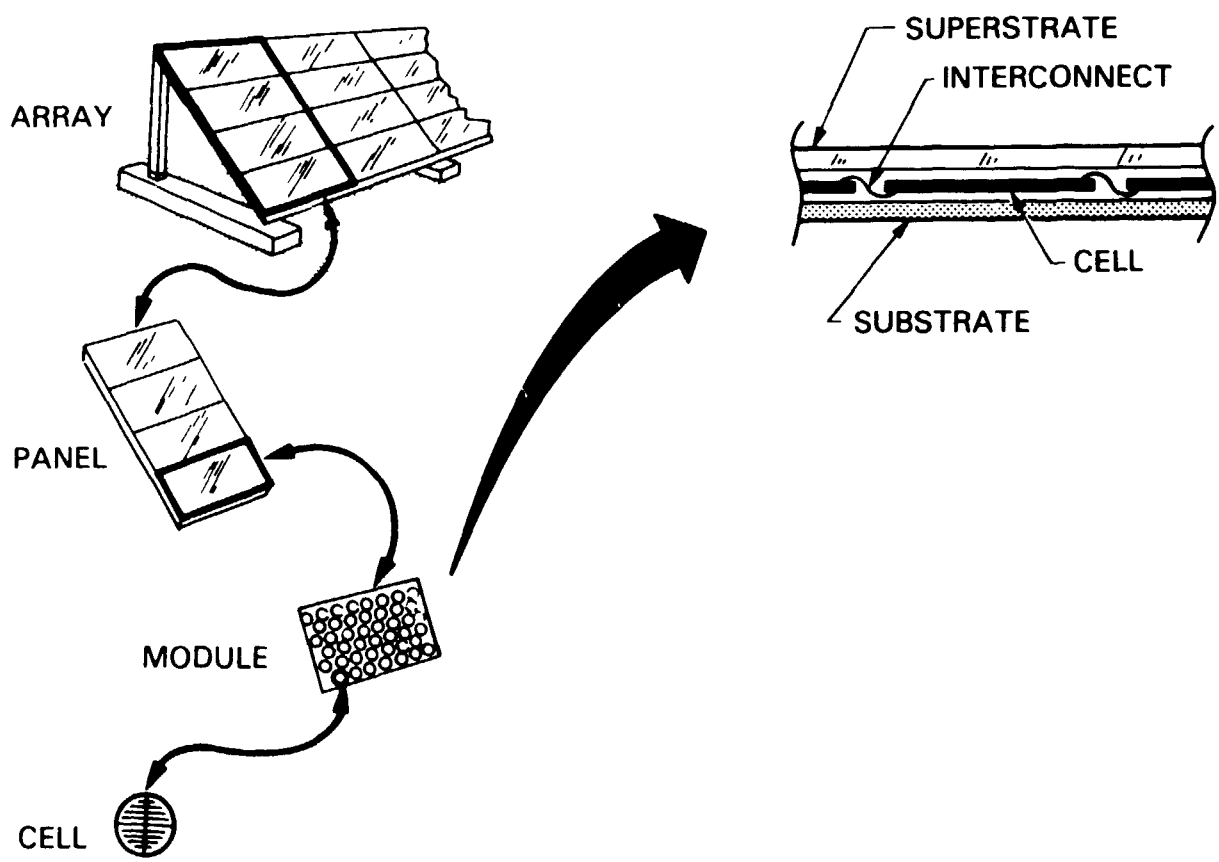

Figure 1. Photovoltaic Array Nomenclature

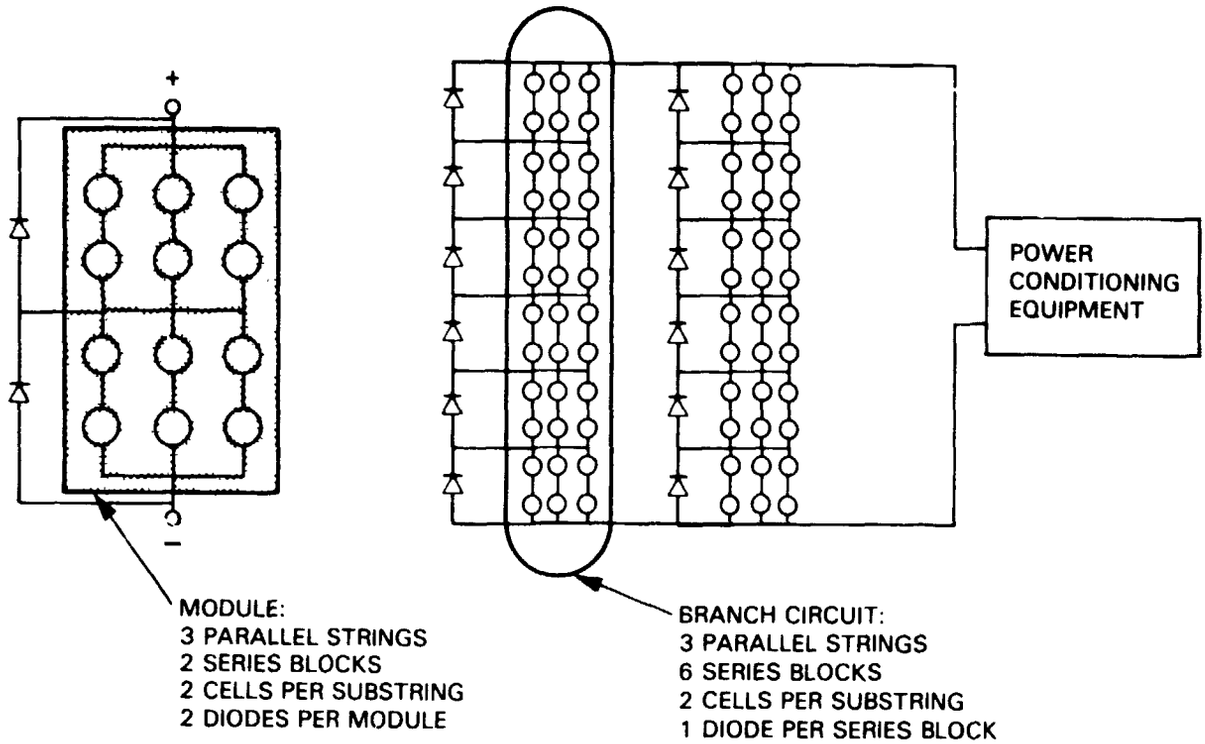

Figure 2. Series-Parallel Nomenclature

stresses of module assembly and qualification testing and of site-specific wind loads, and the thermally induced strains resulting from cyclic temperature changes. The latter problem--the design of interconnects to withstand thermally induced diurnal strain cycles for the intended life of the array of which they are a part--is the fundamental engineering design problem treated in this report.

Diurnal thermal cycles cause the distance between adjacent cells to increase and decrease, straining the interconnect(s) joining them. After a number of such cycles, depending upon the strain levels induced in each interconnect, microcracks develop and eventually propagate across the width of the interconnect until separation (open circuit) occurs. Thus the underlying failure mechanism is mechanical fatigue.

Metallurgists characterize fatigue by means of empirical strain-cycle (fatigue) curves that define the mean number of cycles to failure versus the strain level in the subject material. However, the life of any individual interconnect is governed by its particular flaw strength, as determined by such considerations as metallurgical defects and manufacturing variations in shaping and attachment. The result is that each interconnect fails randomly, yet the fraction of equally strained interconnects that fail in an arbitrarily chosen time interval is statistically predictable.

When every interconnect connecting an adjacent cell pair has failed, the substring containing that cell pair can no longer deliver its energy to the

load; thus, the result of interconnect failures is degradation of array power output. The use of redundancy in the deployment of interconnects can decrease the rate of degradation and, in fact, a sufficiently high degree of redundancy can reduce the degradation to negligible levels. Excessive interconnect redundancy, however, is costly. Economic considerations dictate a tradeoff between the degree of redundancy (cost) and the rate of power reduction (performance). This tradeoff is achieved by minimizing the cost of energy generated over the life of the array.

Module-interconnect reliability design and life-prediction procedures are presented herein that enable the module manufacturer to:

(1) Calculate interconnect strain levels for a particular module-interconnect design configuration.

(2) Predict the cumulative interconnect failure fraction at the end of array life, assuming interconnect fatigue to be the only active failure mechanism.

(3) Estimate array power degradation.

(4) Determine the degree of interconnect redundancy necessary to achieve minimum life-cycle cost of energy over the intended life of the array.

(5) Establish the maximum allowable fraction of interconnect failures, and hence a non-arbitrary pass-fail threshold, in an accelerated thermal cycling test.

Realistic examples of design, prediction, and service qualification testing are presented to demonstrate the use of the developed algorithms and service qualification criteria.

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SECTION II

MODULE-INTERCONNECT DESIGN PROCEDURE

Interconnect analysis and design for photovoltaic arrays, particularly for space applications, are well documented (Reference 1). It is known that good interconnect design practice requires:

(1) Minimizing the thickness.

(2) Maximizing the expansion loop height.

(3) Maximizing the length, i.e., the distance between interconnect-to-cell attachment points.

(4) Avoiding solder and/or adhesive overflow onto the interconnect, which effectively shortens its active length, thereby overstraining the interconnect material.

Each of these techniques reduces the effective strain range (i.e., the maximum peak-to-peak strain in the interconnect material, hereinafter called the strain), thereby prolonging interconnect life.

An effective process of module-interconnect design involves comparing the predicted end-of-design-life cumulative interconnect failure probability, calculated for a definite module-interconnect design and site-specific temperature and insolation history, with a table of maximum allowable interconnect failure probabilities determined from considerations of end-of-life array power reduction and circuit and interconnect redundancy, for which minimum life-cycle energy costs have been determined. In addition to minimum cost, this comparison yields the required interconnect redundancy and provides an estimate of the end-of-life array power reduction. The overall design schematic is presented as a flow chart in Figure 3.

In the following three sections of this report the analytical procedures represented by the rectangles in Figure 3 will be presented in detail and demonstrated by examples.

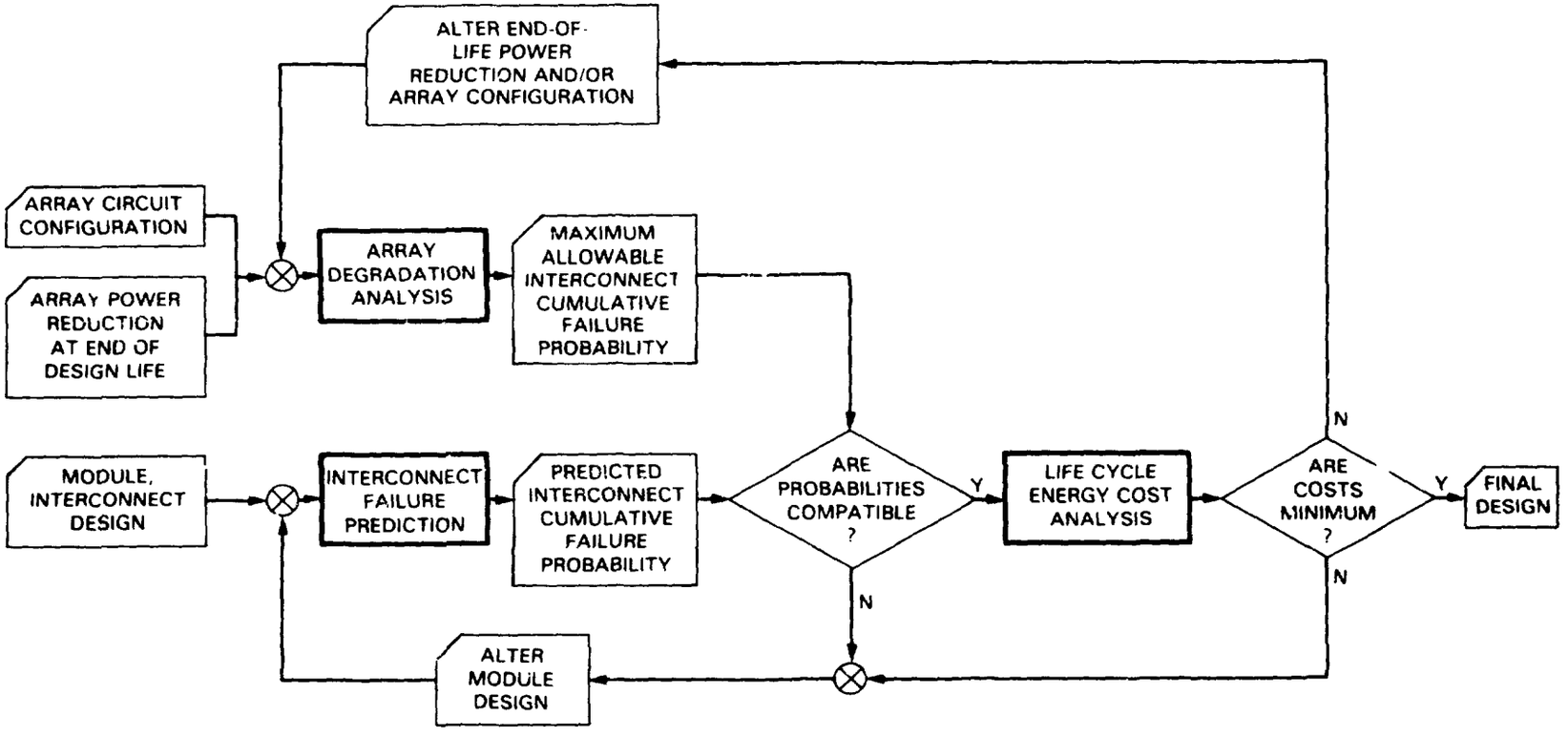

Figure 3. Module-Interconnect Design Procedure

SECTION III

INTERCONNECT FAILURE PREDICTION

This section demonstrates how to determine cumulative interconnect failure probability at end of life starting with a specific module-interconnect design concept and deployment site temperature history. The procedure is outlined in the block diagram shown in Figure 4. Steps include computing interconnect displacement, computing interconnect material strain, and computing interconnect failure probability. An example problem is presented at the end of this section.

A. COMPUTING INTERCONNECT DISPLACEMENT

The first step is to determine the effective thermally induced change δ in the distance g between points where the interconnect is attached to adjacent cells (Figure 5). This effective thermal displacement δ is determined from module design, geometry, and material properties, and site-dependent average diurnal temperature variations.

The total diurnal temperature change may be taken as

$$\Delta T = \Delta T_D + \Delta T_{OP} \tag{1}$$

where

ΔT_D = difference between daily high and low ambient temperatures

ΔT_{OP} = module operating temperature above ambient (about 30°C for most module designs at 100 mW/cm^2 irradiation)

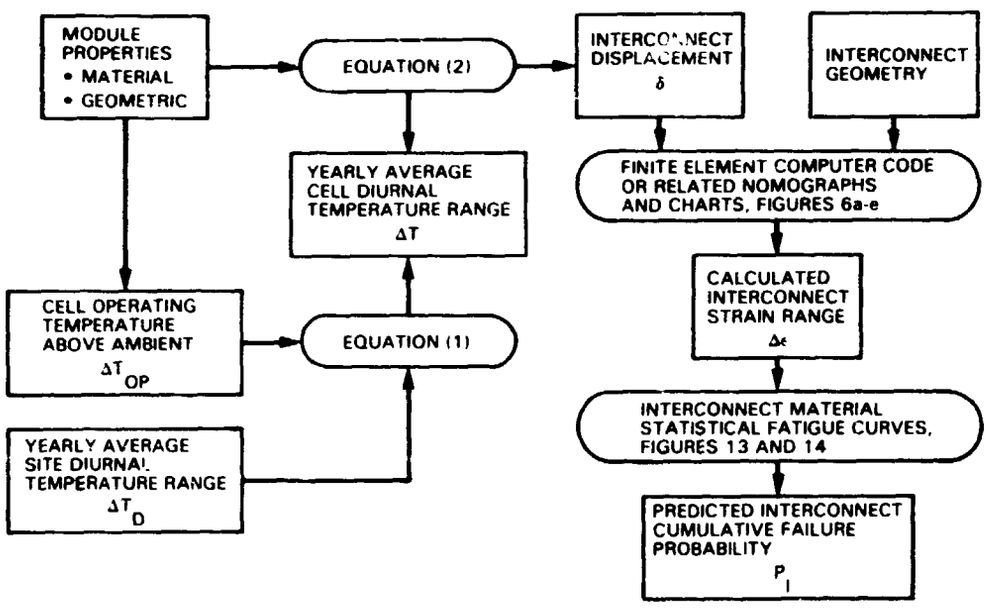

Figure 4. Interconnect Failure Prediction Algorithm

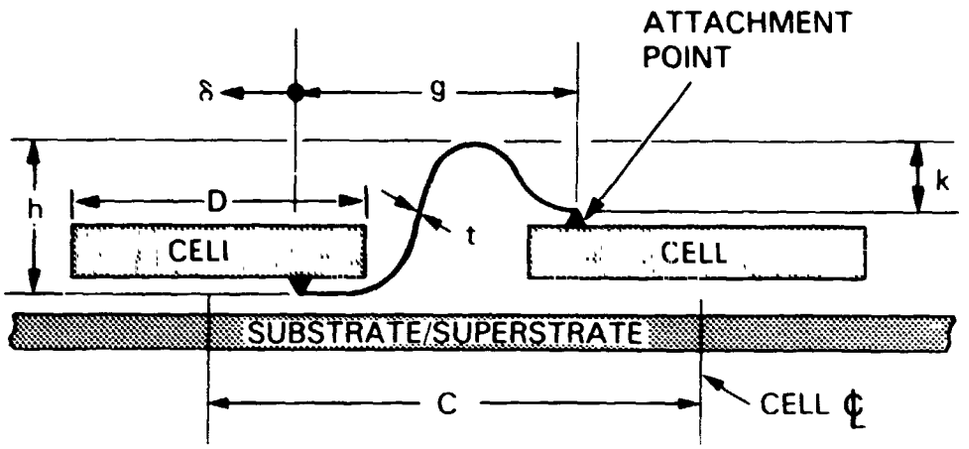

Figure 5. Module-Interconnect Geometry

The effective change in the distance between attachment points, i.e., the effective interconnect displacement, is given by

$$\delta = \left[(\alpha_S - \alpha_C)C + (\alpha_C - \alpha_I)g\right]\Delta T \tag{2}$$

where

δ = effective change in the distance between attachment points

C = center-to-center distance between cells

D = solar cell diameter

g = distance between attachment points of the interconnects

α_S = thermal expansion coefficient of the substrate or superstrate

α_C = thermal expansion coefficient of the solar cells

α_I = thermal expansion coefficient of the interconnect material

ΔT = diurnal temperature variation

B. COMPUTING INTERCONNECT MATERIAL STRAIN

Having determined the interconnect displacement δ from temperature variations, the next step is to calculate the total strain range $\Delta\epsilon$ induced in the interconnect material by the displacement δ. For complex interconnect configurations this step requires computer assistance using finite element modeling techniques of structural analysis. To circumvent the time and cost inherent in computer use, nomographs have been developed in this study to permit rapid graphical determination of strain levels in some important geometric configurations; these are presented in Figures 6a through 6e.

The nomographs were developed by transcribing non-dimensionalized finite element computer modeling results to graph paper. The T-interconnect nomograph (Figure 6a) was generated from 288 independent point designs (different numerical assignments to the geometric variables); the G-interconnect nomograph (Figure 6b) from 144 point designs, and the Z-interconnect nomograph (Figure 6c) and the SC-interconnect nomograph (Figure 6d) from 48 point designs each.

In each case the maximum strain in the interconnect can be expressed as

$$\Delta\epsilon = f \cdot F \cdot \left(\frac{t}{h}\right) \cdot \left(\frac{\delta}{g}\right) \tag{3}$$

where

$\Delta\epsilon$ = maximum strain in the interconnect

t = thickness of interconnect

h = height of interconnect from lowest point of attachment to top of loop, measured perpendicular to the plane of the module

k = height of interconnect from highest point of attachment to top of loop, measured perpendicular to the plane of the module

δ = effective change in attachment-point-to-attachment-point dimension

g = attachment-point-to-attachment-point dimension

F,f = shape factors computed using the nomograph, Figures 6a through 6e

Use of the Z-interconnect and SC-interconnect nomographs is straightforward. For these configurations, $f = 1$ and F is determined in the usual fashion by entering the nomograph with the appropriate abscissal value, proceeding to the appropriate curve, and then reading the F-value on the ordinate.

Use of the T-interconnect and G-interconnect nomographs, being somewhat involved, is best demonstrated by example. Consider a T-interconnect with $t = 0.051$ mm, $h = 1.016$ mm, $k = 0.254$ mm, $g = 1.905$ mm, and $\delta = 0.046$ mm. Then $h/g = 0.533$, $t/h = 0.050$, $k/h = 0.250$, and $\delta/g = 0.024$. Referring to Figure 6e--a worksheet reproduction of Figure 6a--proceed in the following steps:

Step 1. Enter the F-chart on the abscissa at $h/g = 0.533$ and extend a vertical line to a point on the curve labeled $t/h = 0.050$ (visual interpolation may be required).

Step 2. Extend a horizontal line from this point to the ordinate; read the value, $F = 5.45$.

Step 3. Extend the original vertical line ($h/g = 0.533$) up to and through the f-chart above the nomograph.

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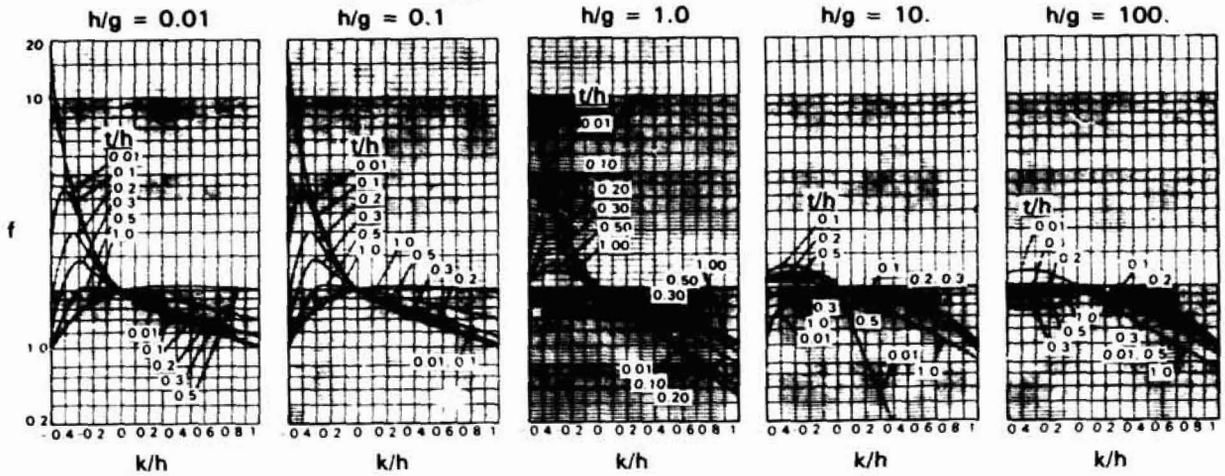

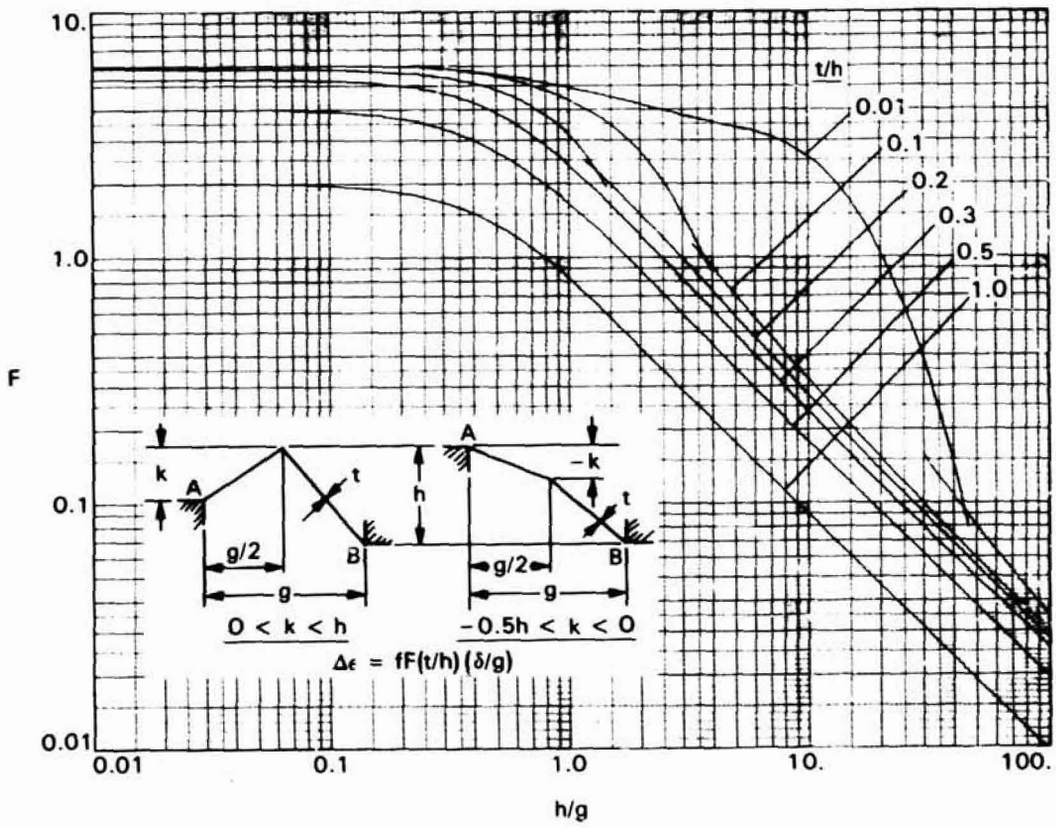

Note: 1. g is the Horizontal Distance Between Interconnect Attachment Points.

2. Maximum Strain Above Break in Curves Occurs at Point A, Below Break in Curves at Point B.

Figure 6a. T-Interconnect Nomograph

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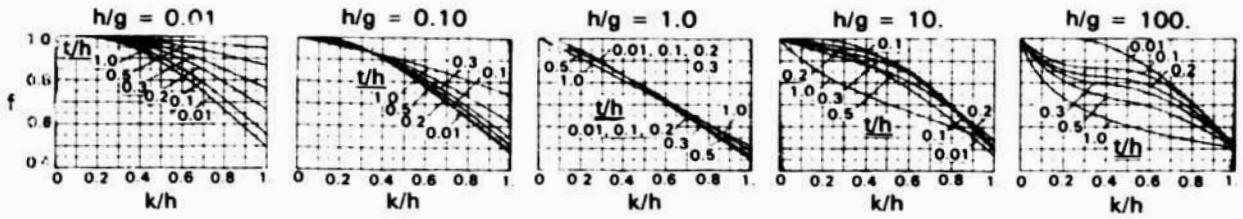

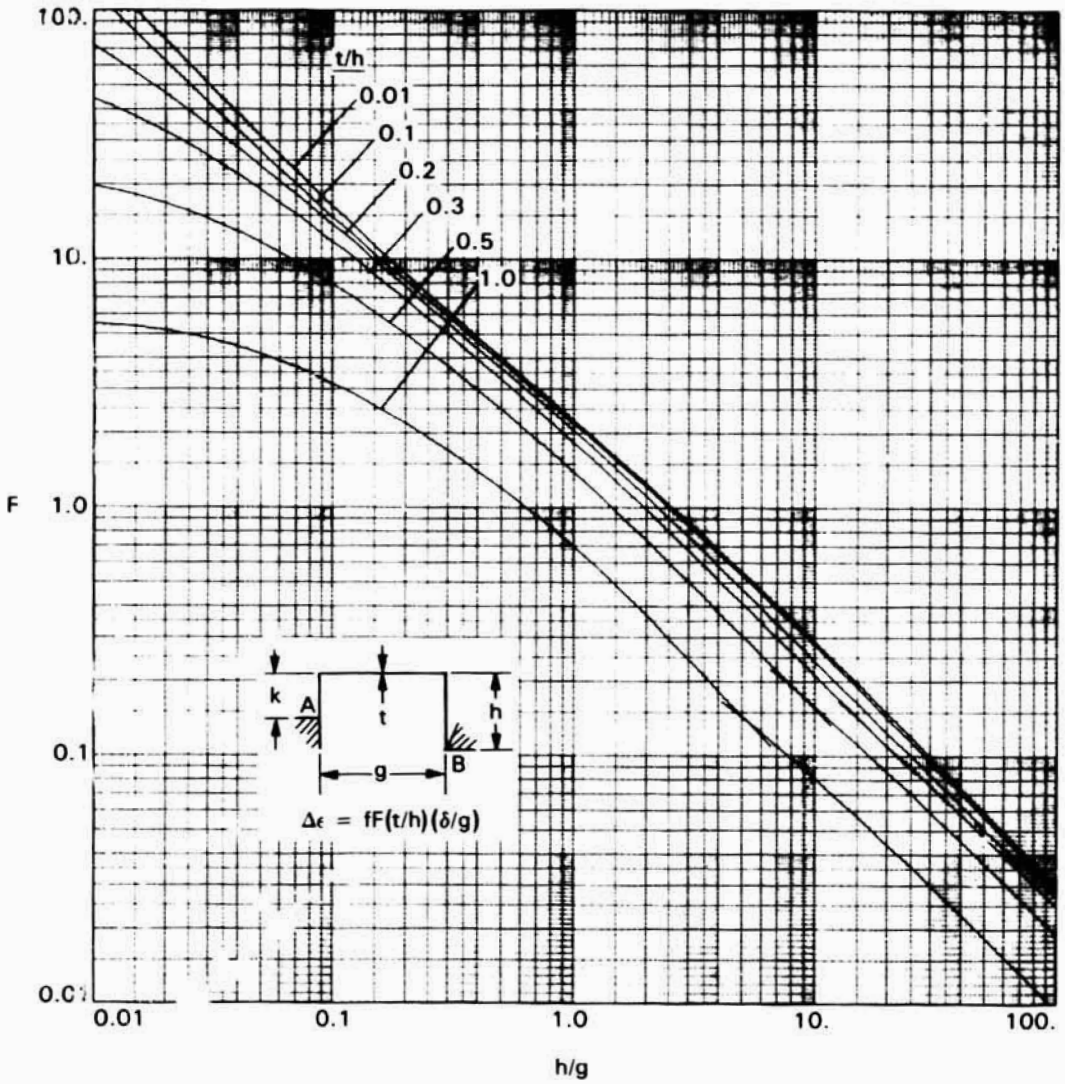

Notes: 1. g is the Horizontal Distance Between Interconnect Attachment Points

2. Maximum Strain Above Break in Curves Occurs at Point B, Below Break in Curves at Point A

Figure 6b. G-Interconnect Nomograph

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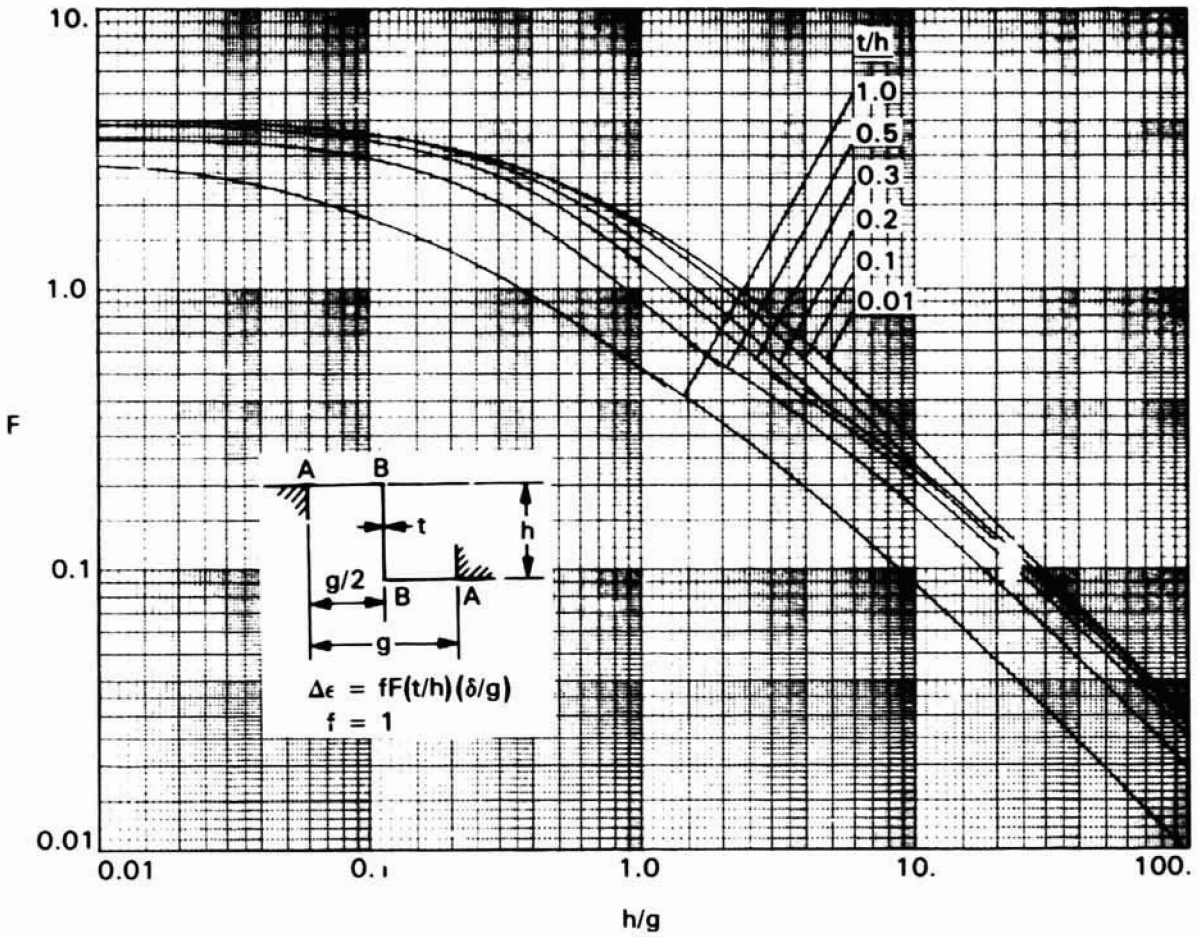

Notes: 1. g is the Horizontal Distance Between Interconnect Attachment Points.

2. Maximum Strain Above Break in Curves Occurs Between Points B, Below Break in Curves Between Points A and B.

Figure 6c. Z-Interconnect Nomograph

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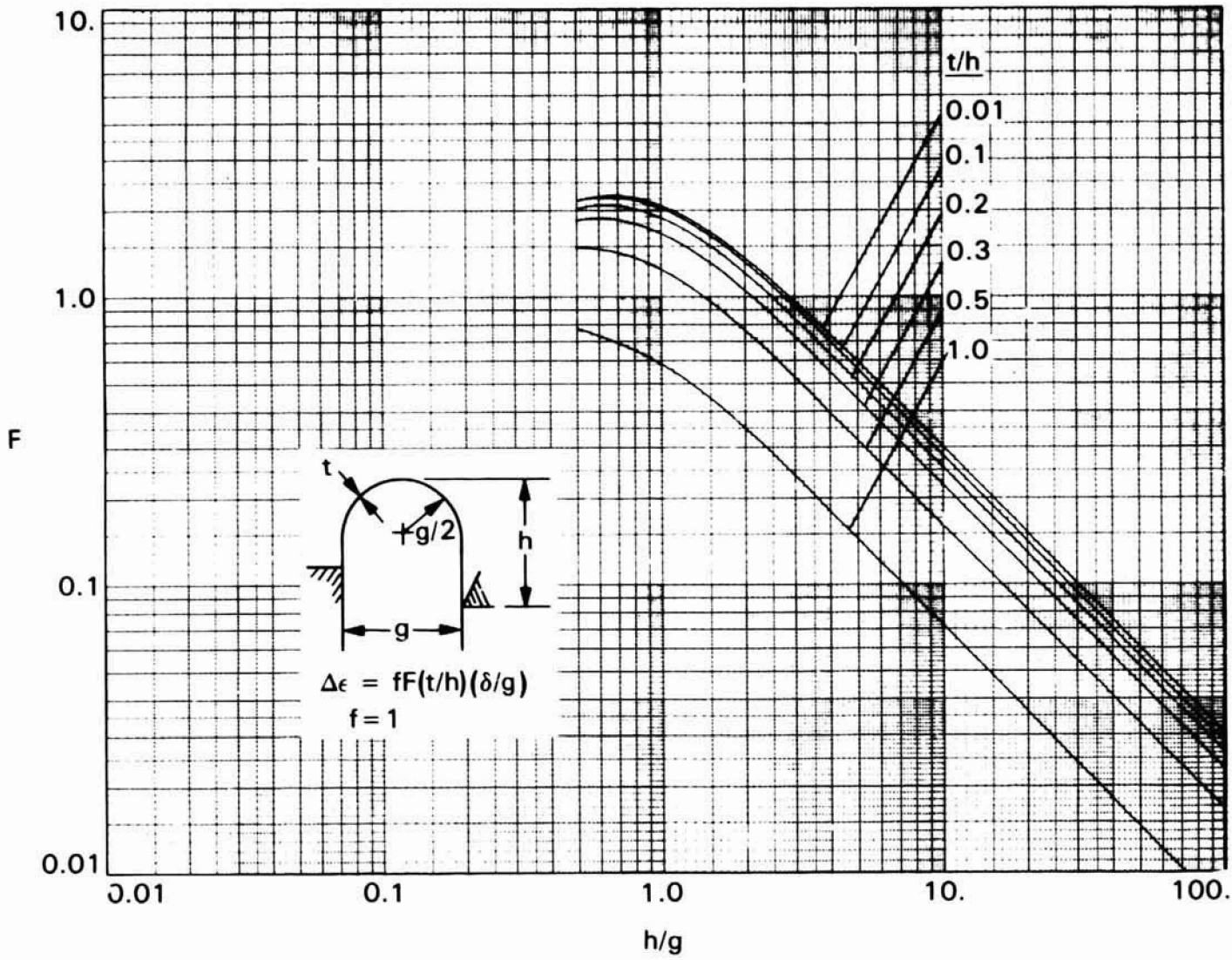

Note: g is the Horizontal Distance Between Interconnect Attachment Points

Figure 6d. SC-Interconnect Nomograph

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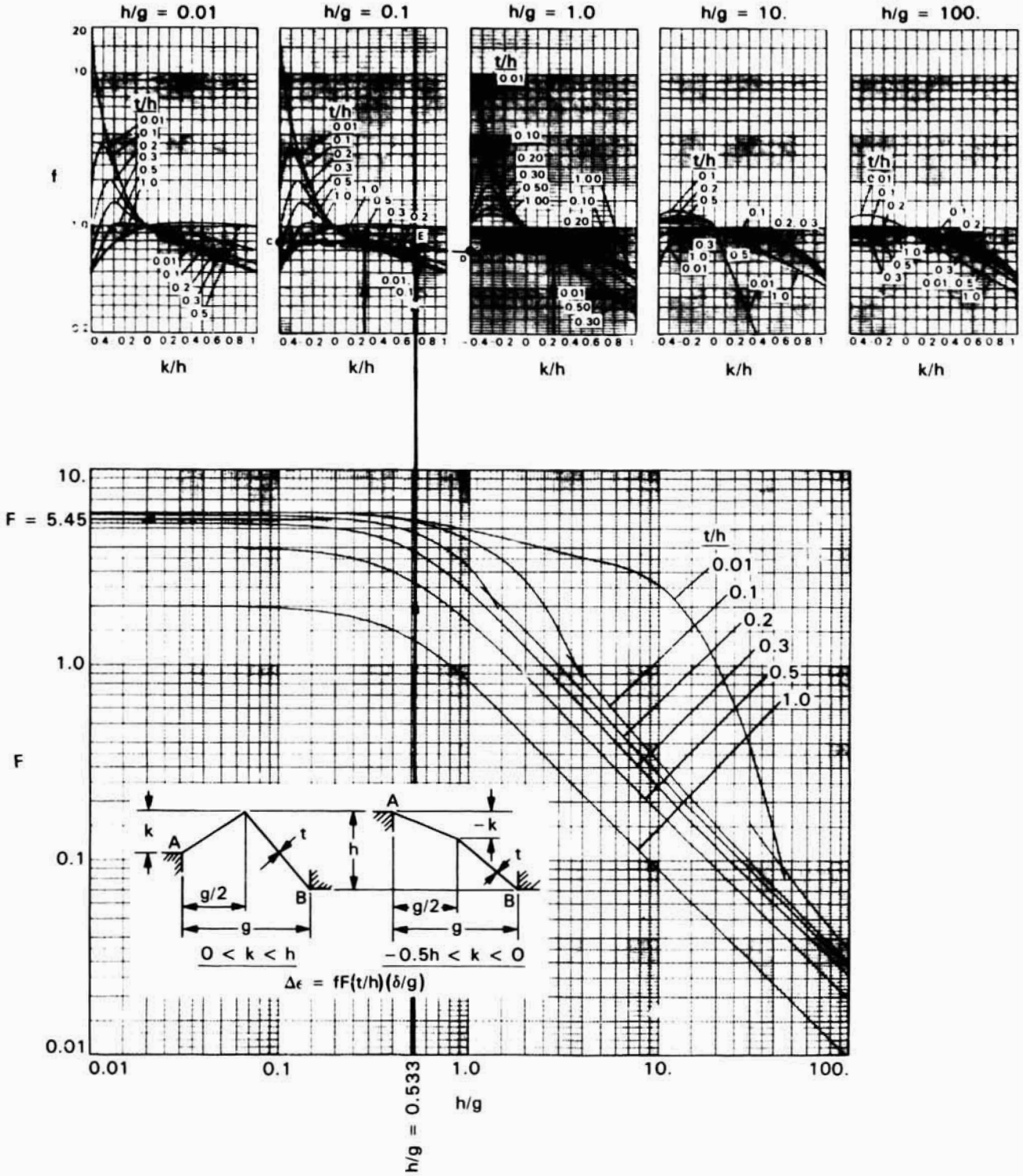

Note: 1. g is the Horizontal Distance Between Interconnect Attachment Points.

2. Maximum Strain Above Break in Curves Occurs at Point A, Below Break in Curves at Point B.

Figure 6e. T-Interconnect Nomograph: Example of Use

Step 4. Enter the two f-charts labeled h/g = 0.10 and h/g = 1.00 (0.10 < 0.533 < 1.00) at their abscissal values k/h = 0.250; proceed to the appropriately labeled curves (t/h = 0.050) and mark the f-values on the ordinates (points C and D).

Step 5. Connect points C and D with a straight-line segment. This segment will intersect the vertical line from the F-chart at point E.

Step 6. Read the ordinate value of point E, in this case f = 0.72.

Step 7. Compute the strain range $\Delta\epsilon$ using Equation 3:

$$\Delta\epsilon = f \cdot F \cdot \left(\frac{t}{h}\right) \cdot \frac{\delta}{g}$$

$$\Delta\epsilon = 0.72 \times 5.45 \times 0.05 \times 0.024$$

$$\Delta\epsilon = 0.0047$$

C. COMPUTING INTERCONNECT FAILURE PROBABILITY

Having determined maximum interconnect strain from displacement δ, the final step is to calculate the expected life Y of the interconnect and/or the predicted fraction p_I of interconnects (the interconnect failure probability) that will fail in a specified number of cycles. This is achieved through the use of statistical fatigue curves, a set of standard strain-cycle curves parameterized by the interconnect cumulative failure probability. Statistical fatigue curves have been generated by combining experimental cumulative interconnect failure rate data with the interconnect material empirical fatigue curve.

1. Empirical Fatigue Curve

The interconnect material fatigue curve provides the basis for computing interconnect life. This curve is given by an empirical formula suggested by Manson (Reference 2), who demonstrated its universality in describing the fatigue behavior of 29 different metals and alloys:

$$\Delta\epsilon = 3.5 \frac{\sigma_u}{E} N^{-0.12} + \left(\ell n \frac{1}{1 - RA}\right)^{0.6} N^{-0.6} \qquad (4)$$

where

$\Delta\epsilon$ = total interconnect strain range (elastic plus plastic)

σ_u = ultimate tensile strength of material

E = Young's modulus

RA = reduction in area (from tensile test)

N = number of cycles to failure

For OFHC 1/4-hard copper, the interconnect material studied in this investigation, property values used (Reference 3) are

σ_u = 0.262 GPa

E = 117.2 GPa

RA = 0.70

giving

$$\Delta\epsilon = 0.0078\ N^{-0.12} + 1.1178\ N^{-0.60} \qquad (5)$$

This curve is plotted in (A) of Figure 7.

Various experimental data are also plotted in Figure 7. Several modules of diverse design were thermal-cycle tested to as much as 575 cycles (see Section VI). At the end of the test, broken interconnects were counted, their shapes were measured, and the strains in them were calculated using the nomographs.

These data are plotted in (B) of Figure 7 as a cloud of points between N = 47 cycles and N = 575 cycles. Their distribution about the fatigue curve is evidence supporting the argument that the empirical fatigue curve adequately represents interconnect fatigue behavior.

The shaded points (C) in Figure 7 represent conventional mechanical fatigue data for OFHC copper in widely varying metallurgical conditions (Reference 4). Manson's curve also agrees well with these data.

To achieve further understanding of interconnect fatigue statistics, a large number of interconnects were fabricated and tested to failure in this study. Test specimens are 0.051-mm-thick OFHC 1/4-hard copper interconnects shaped by precisely machined dies to the configurations shown in Figure 8. In each test 30 specimens of the same configuration are carefully mounted to the test fixture shown in Figure 9. This device consists of two horizontal plates vertically offset 0.254 mm to simulate the thickness of a typical solar cell and horizontally separated by a nominal 1.905-mm gap to simulate a typical cell-to-cell gap in a module. One plate is then made to move horizontally back and forth relative to the other at a constant (but adjustable) cycle rate and amplitude, the effect being achieved through a motor-driven cam-follower and spring loading of the plates. The interconnects are series-wired such that when a break occurs the cycling ceases. The number of cycles to failure is read from a counter, a long thin wire is used to jump the terminals of the failed interconnect, and testing continues until the next failure or the end of the test.

The raw data obtained from this testing procedure are presented in Figure 10 as a plot of cumulative interconnect failure probability vs the number of cycles to failure. The data curves are labeled with the number of interconnects of the particular configuration tested and with the strain range $\Delta\epsilon$ calculated using a finite-element program or the nomographs developed in this study (Figures 6a through 6e). Each unshaded data point (D) in Figure 7 is obtained from a single one of the test curves in Figure 10, giving a plot

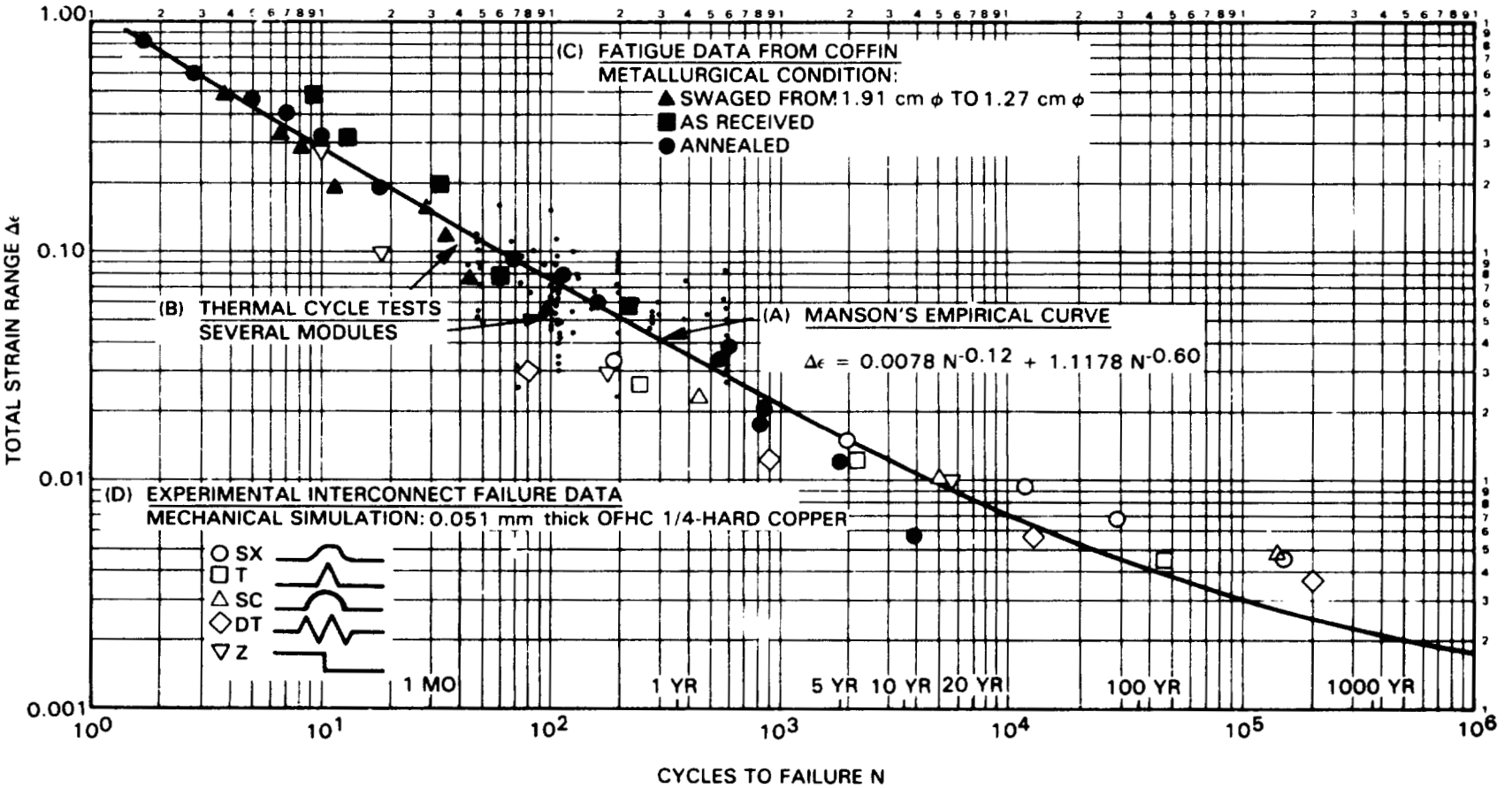

Figure 7. Fatigue Information: OFHC Copper

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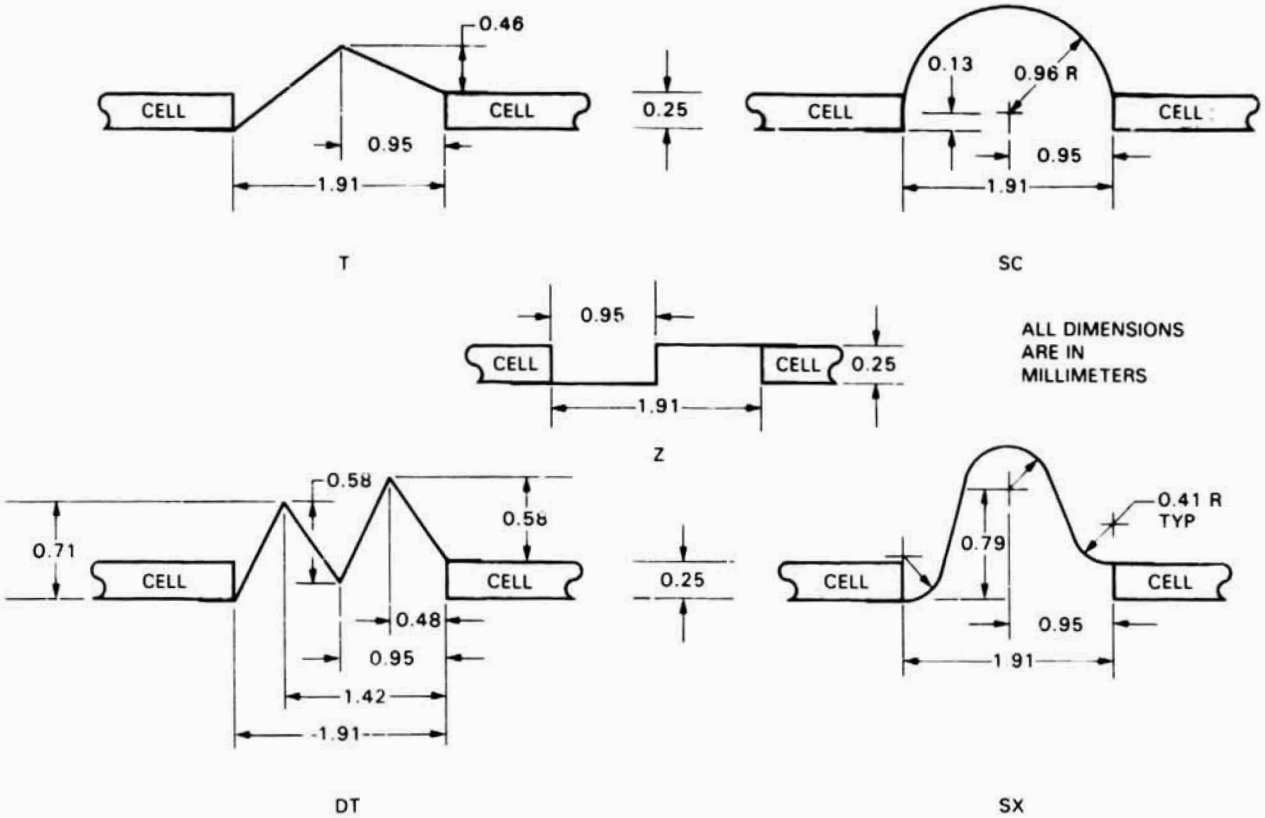

Figure 8. Geometry of Interconnects Mechanically Cycled to Failure and Their Code Designations

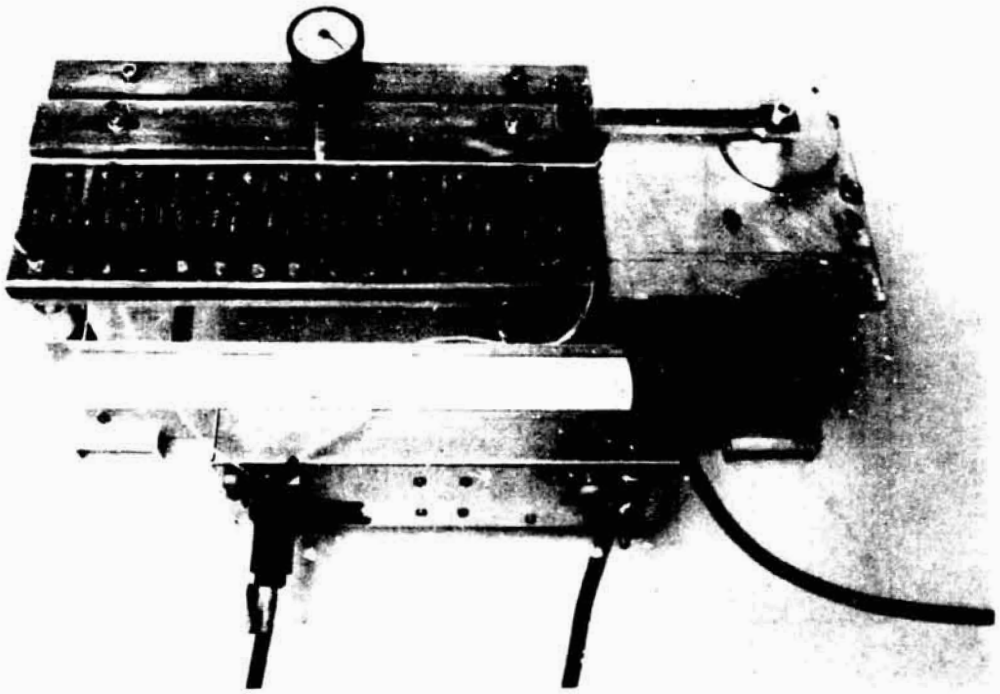

Figure 9. Interconnect Strain-Cycle (Fatigue) Apparatus

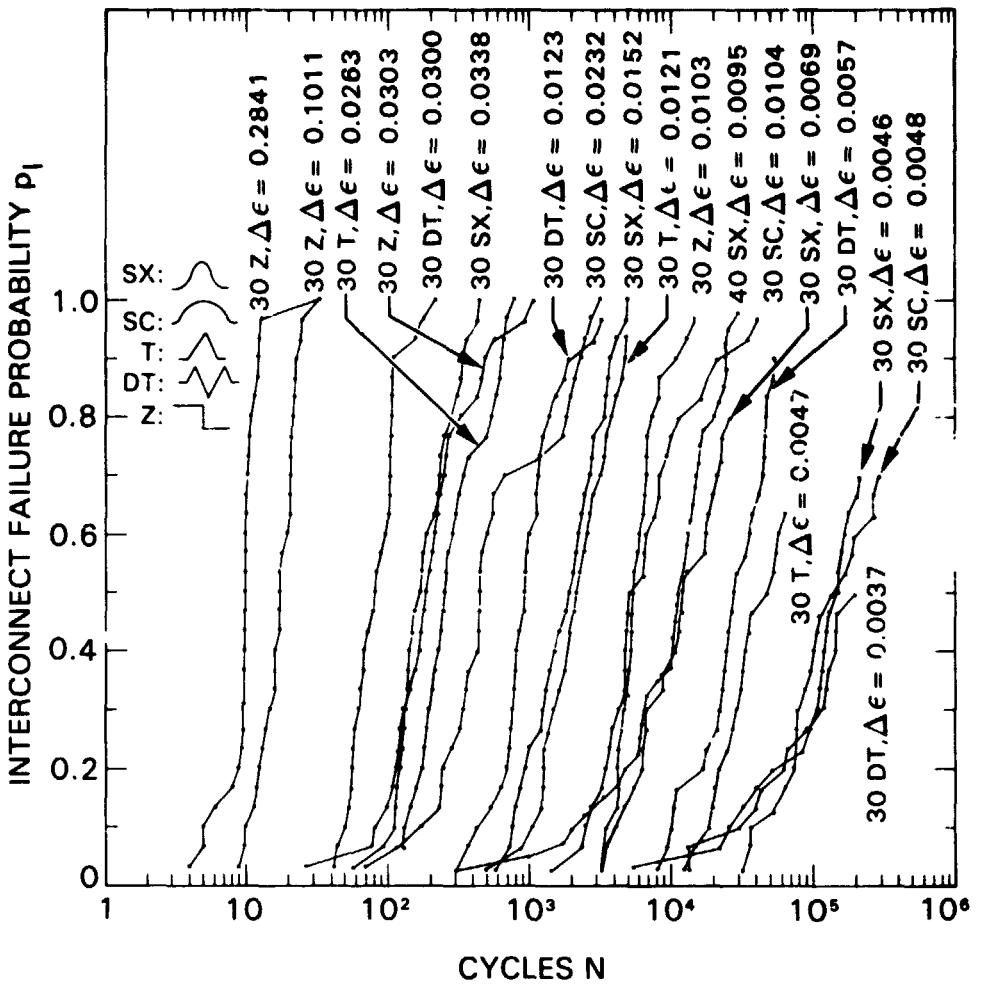

Figure 10. Experimental Failure Probability vs Number of Cycles to Failure for 0.051-mm-Thick OFHC Interconnect Configurations

of strain range $\Delta\epsilon$ vs the number of cycles at which the cumulative interconnect failure probability is 0.50. Manson's curve can thus be regarded as a 50% failure-probability curve. For periods of present interest to module designers (5 to 30 years), the curve underestimates experimentally observed interconnect longevity; this conservatism makes the curve useful as a predictive and design tool.

2. Statistical Fatigue Curves

Manson's empirical fatigue curve relates interconnect strain level to the number of cycles at which the cumulative interconnect failure fraction is 0.50. For interconnect and array field life prediction, it is of greater value to have a set of curves relating strain level to cycles-to-failure for a wide range of cumulative interconnect failure fractions. Such a set of curves can be obtained by combining failure rate data from the mechanical simulation tests with the empirical fatigue curve.

This is achieved by first superposing all of the Figure 10 data curves at the $p_I = 0.50$ point, Figure 11, and observing that all curves have approximately the same slope (failure rate) in the region of high cumulative failure probability, $0.2 \leq p_I \leq 1.0$, and that the curves for some interconnect configurations exhibit long tails in the region of low cumulative failure probability, $0.0 \leq p_I \leq 0.2$. Then fitting the failure data from each region to a two-parameter Weibull cumulative failure distribution function, Figure 12, yields

$$\frac{N_p}{N_{0.50}} = 2.621 \left(\ell n \frac{1}{1 - p_I} \right)^{1.214} \qquad 0 < p_I < 0.2 \tag{6}$$

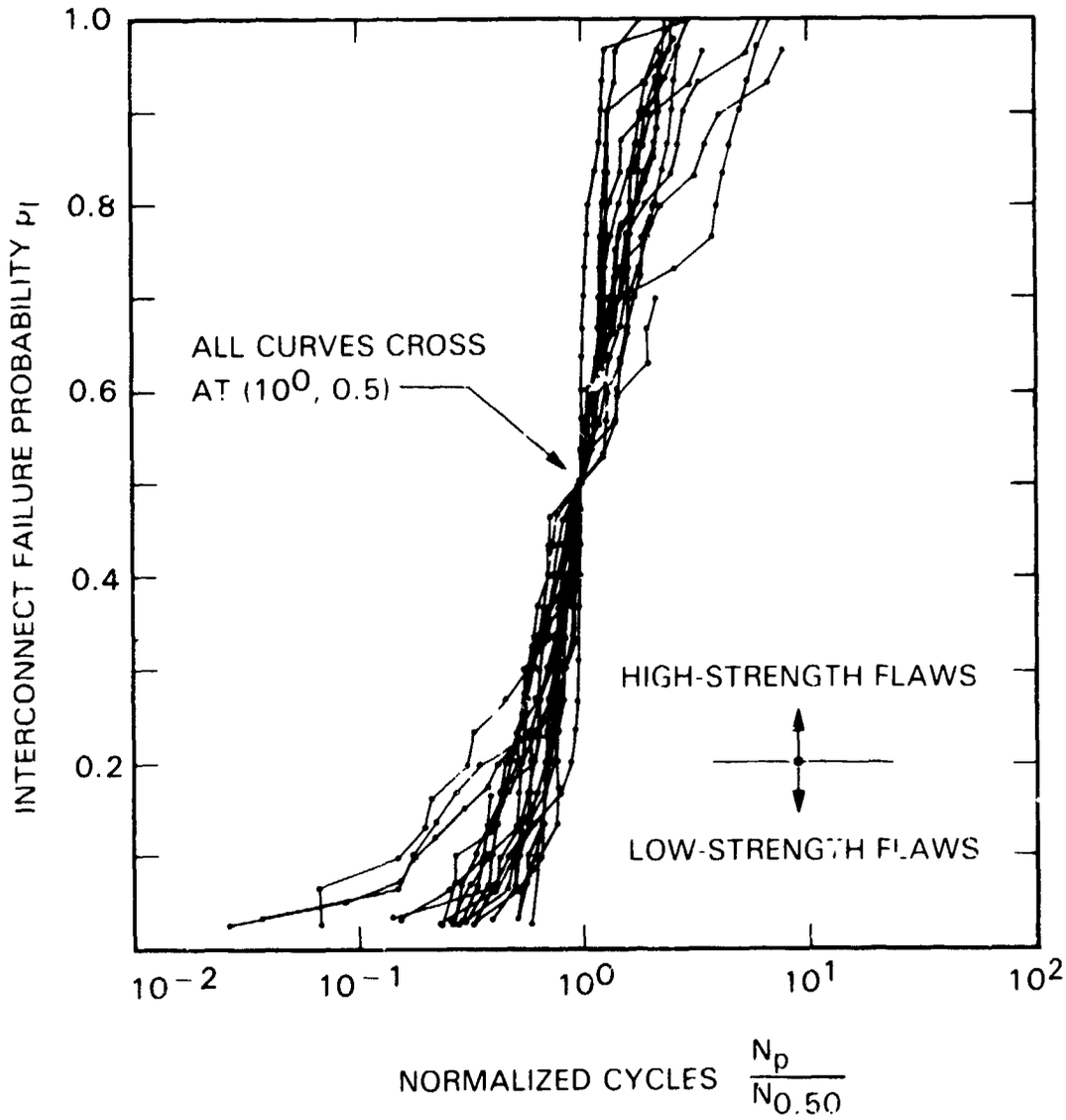

Figure 11. Superposition of Test Data Curves for Failure-Rate Determination

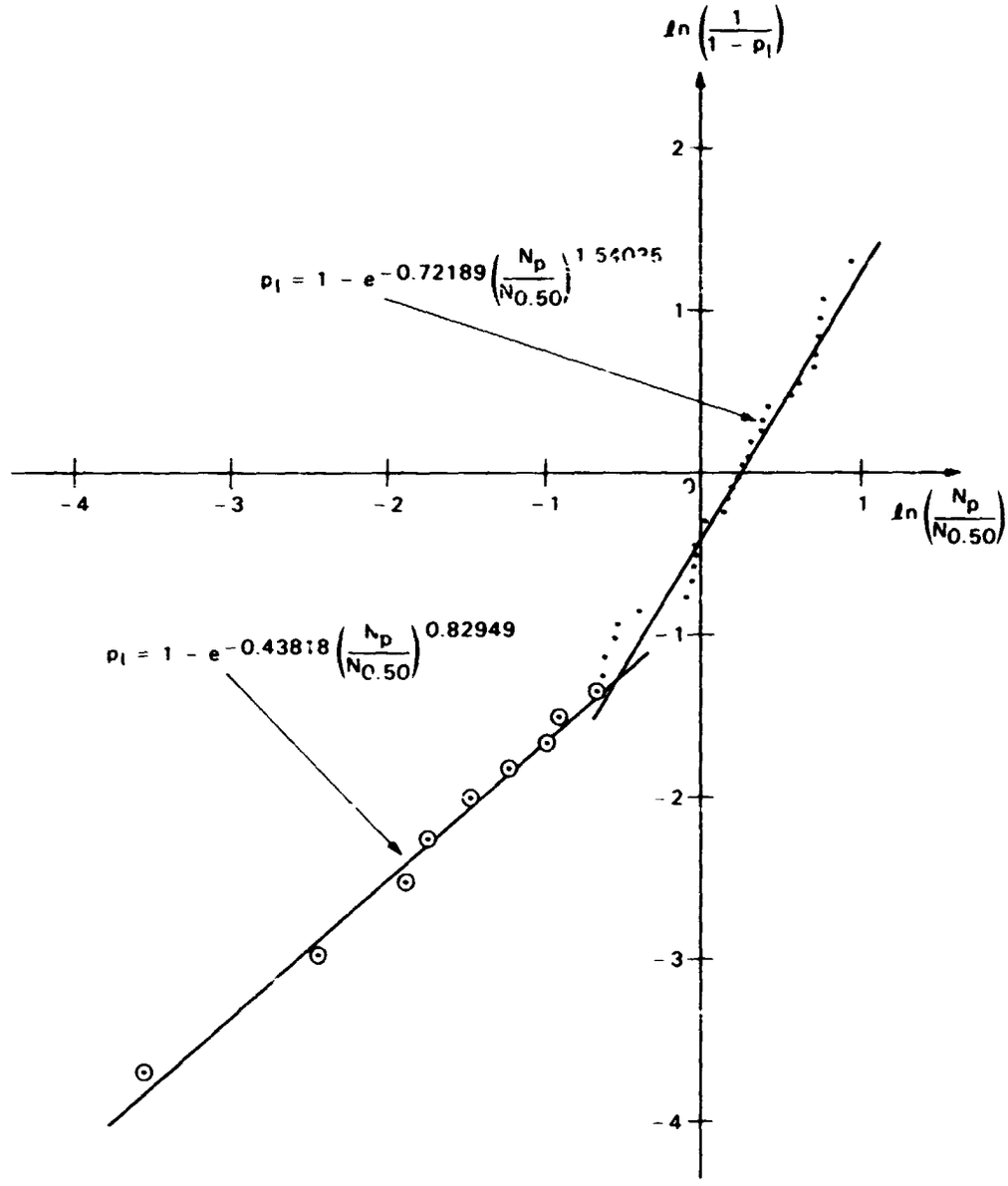

Figure 12. Weibull Analysis of Interconnect Failure Data

and

$$\frac{N_p}{N_{0.50}} = 1.224 \left(\ln \frac{1}{1 - p_I}\right)^{0.537} \qquad 0.2 < p_I < 1.0 \tag{7}$$

In these equations

p_I = cumulative interconnect failure probability

N_p = number of cycles to achieve a cumulative failure probability p

$N_{0.50}$ = number of cycles to achieve a cumulative failure probability of 0.50

Substituting these equations into the Manson formula, Equation (5) gives, for $0.0 \leq p_I \leq 0.2$,

$$\Delta\epsilon = 0.0088 \left[N_p \left(\ell n \frac{1}{1 - p_I} \right)^{-1.214} \right]^{-0.12} + 1.9929 \left[N_p \left(\ell n \frac{1}{1 - p_I} \right)^{-1.214} \right]^{-0.6} \quad (8)$$

and, for $0.2 \leq p_I \leq 1.0$,

$$\Delta\epsilon = 0.0080 \left[N_p \left(\ell n \frac{1}{1 - p_I} \right)^{-0.537} \right]^{-0.12} + 1.2616 \left[N_p \left(\ell n \frac{1}{1 - p_I} \right)^{-0.537} \right]^{-0.6} \quad (9)$$

These last equations are used to generate the statistical fatigue curves of Figures 13 and 14, which relate the variables strain range, life, and

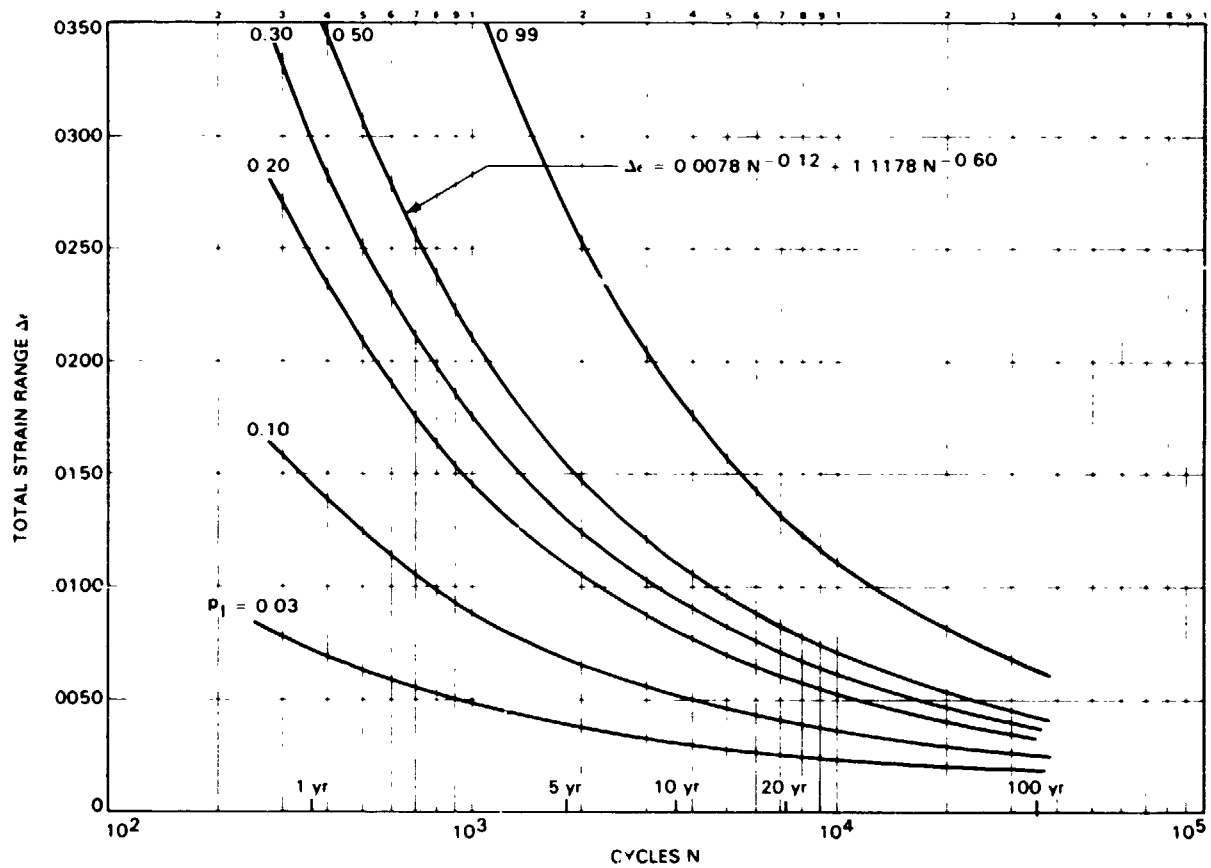

Figure 13. Statistical Fatigue Curve for OFHC Copper Interconnects With Failure Probability as Parameter

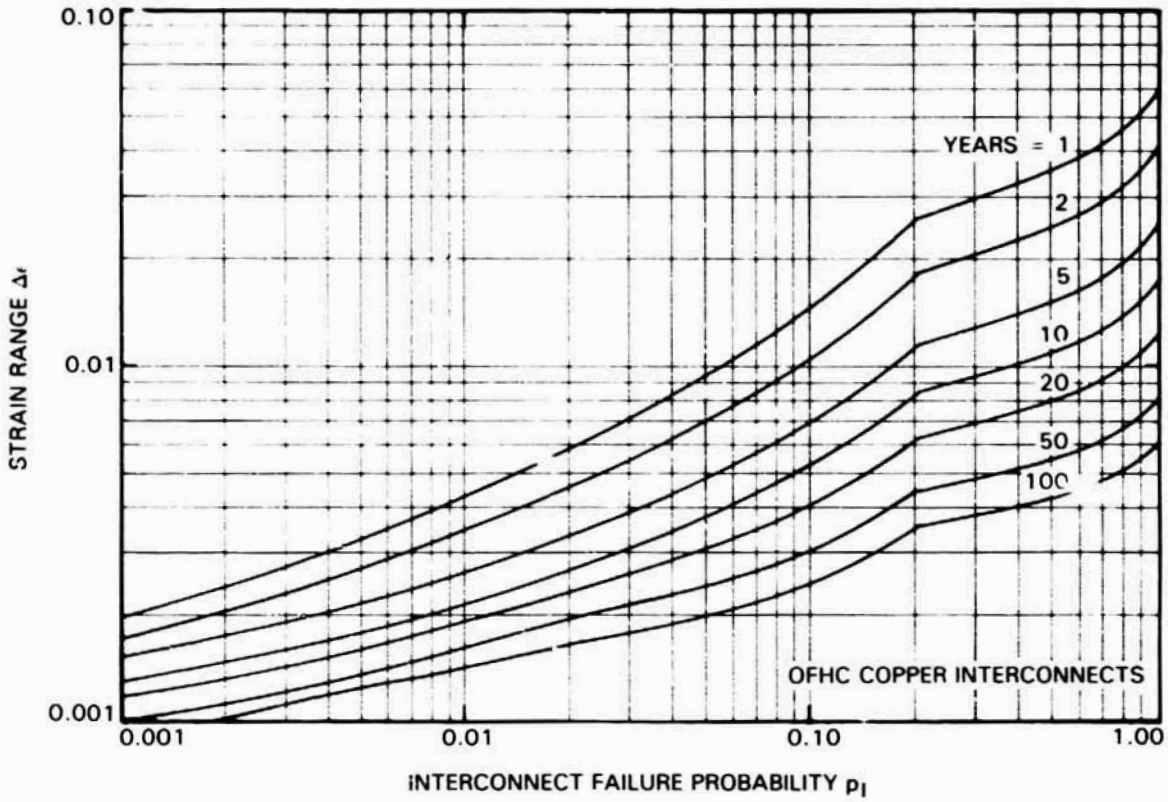

Figure 14. Interconnect Strain Range $\Delta\epsilon$ vs Interconnect Failure Probability p_I With Array Life (years) as Parameter

failure probability. It is assumed that early interconnect failures can be attributed to low-strength flaws, and later failures to high-strength flaws; this provides the rationale for the designation of the two failure ranges in Figure 11.

Figure 14 can now be used to complete the interconnect failure prediction calculation. Having previously computed the interconnect strain range $\Delta\epsilon$, one enters the graph in Figure 14 with this strain value as ordinate. The appropriate end-of-life curve is then used to determine the abscissal value p_I of interconnect failure probability.

D. AN EXAMPLE

Consider as an example a module having the following design properties:

$C = 7.70$ cm

$D = 7.57$ cm

$g = 1.905$ mm

$\alpha_S = 15.8 \times 10^{-6}$ cm/cm/°C

$\alpha_C = 2.9 \times 10^{-6}$ cm/cm/°C

$\alpha_I = 5.3 \times 10^{-6}$ cm/cm/°C

The module is to be deployed at a site near New River, Arizona, for which the temperature data given in Table 1 is available. It is also assumed that the operating temperature of this module above ambient temperature depends upon insolation, as depicted in Figure 15. At an assumed level of insolation of 100 mW/cm^2, the module operating temperature above ambient is $\Delta T_{op} \approx 32$°C. From Table 1 the yearly average diurnal temperature swing is $\Delta T_D = 14$°C. Using these values in Equation (1) gives $\Delta T = 46$°C. Now Equation (2) yields $\delta = 0.0046$ cm.

The module is now assumed to have T-interconnects (Figure 6a) with h = 1.016 mm and k = 0.254 mm. The strain for this interconnect was calculated in Section III B; it is $\Delta\epsilon = 0.0047$. Now, using Figure 14, the cumulative interconnect failure probability at 20 years is $p_I = 0.13$, i.e., 13% of the interconnects in this module are expected to fail within 20 years. If the array field at the New River site were composed only of modules of this type, then 13% of the interconnects in the entire array would be expected to fail within 20 years.

Consider as a second example a module-interconnect design more representative of present module construction: a glass-superstrate module with Z-interconnects. The design parameters are: $\alpha_S = 9.2$ cm/cm/°C (glass), C = 10.16 cm, D = 9.96 cm, g = 2.54 cm, t = 0.051 mm, and h = 0.305 mm.

Table 1. 1979 Monthly Average High and Low Temperatures for New River, Arizona (Provided by DSET, Inc.)

Month	Temperature, °C		
	Avg. High	Avg. Low	ΔT_D
January	11.7	2.8	8.9
February	18.3	5.0	13.3
March	20.6	7.8	12.8
April	27.2	10.6	16.7
May	31.1	16.7	14.4
June	38.9	22.8	16.1
July	41.1	25.0	16.1
August	38.9	23.3	15.6
September	38.9	24.4	14.4
October	30.6	16.1	14.4
November	20.0	7.2	12.8
December	19.4	6.7	12.8
		Average ΔT_D =	14.0 °C

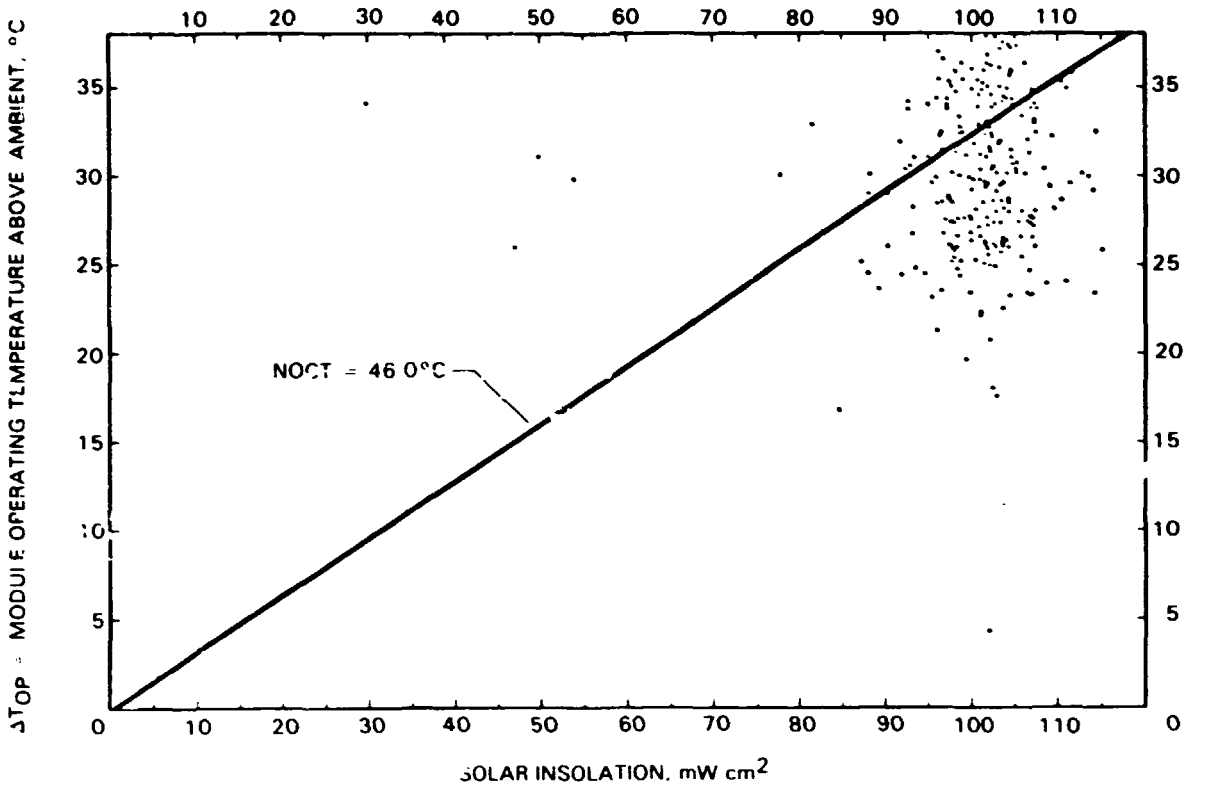

Figure 15. Module Operating Temperature Above Ambient vs Insolation for a Typical Module at JPL's Pasadena Test Site

Compared with the module of the first example, the structural element of this module has a lower coefficient of thermal expansion and the distance between interconnect-to-cell attachment points is considerably larger. The interconnects in this module are expected to experience lower strain levels and hence exhibit longer life. Calculations verify these expectations. Equation (2) with $\Delta T = 46^{\circ}C$ gives $\delta = 0.0027$ cm and the Z-interconnect nomograph gives $F = 4.0$. It follows from Equation (3) that $\Delta\epsilon = 0.0007$. The life-prediction curves (Figures 13 and 14) predict virtually no failures during a 20-year life.

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SECTION IV

ARRAY DEGRADATION ANALYSIS

The module-interconnect design procedure presented in Figure 3 enables the designer of photovoltaic modules to determine the degree of interconnect redundancy required to achieve minimum cost and acceptable end-of-design-life array power reductions. The interconnect failure prediction algorithm outlined in Figure 4, and presented in detail in the previous section, provides a means of predicting the fraction of failed interconnects at end-of-life for a particular module-interconnect design.

In this section a companion algorithm, outlined in Figure 16, is used to generate the interconnect failure fraction p_I associated with a specified end-of-life array power-loss fraction f_Y and degree of interconnect redundancy r. The designer can compare his predicted failure fractions with a table of failure probabilities generated from considerations of array power degradation to determine the degree of interconnect redundancy that will result in acceptable array power reductions.

The dependence of array power degradation on circuit redundancy (series-paralleling) has been illuminated by Ross (Reference 5). Figure 17 illustrates this dependency for a limited range of array series-parallel-diode configurations. A voluminous parametric analysis (References 6 and 7) has yielded many such curves, which (with additional array circuit design considerations) are collected in Reference 8.

The substring and interconnect failure probabilities are numerically related as follows:

$$p_c = p_I^{\,r} \tag{10}$$

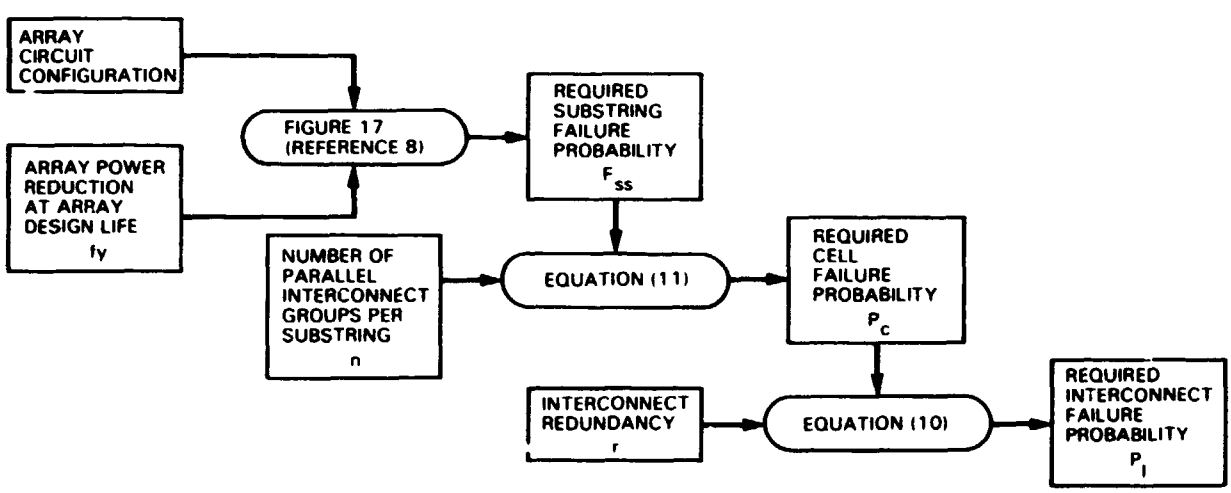


Figure 16. Array Degradation Analysis Algorithm

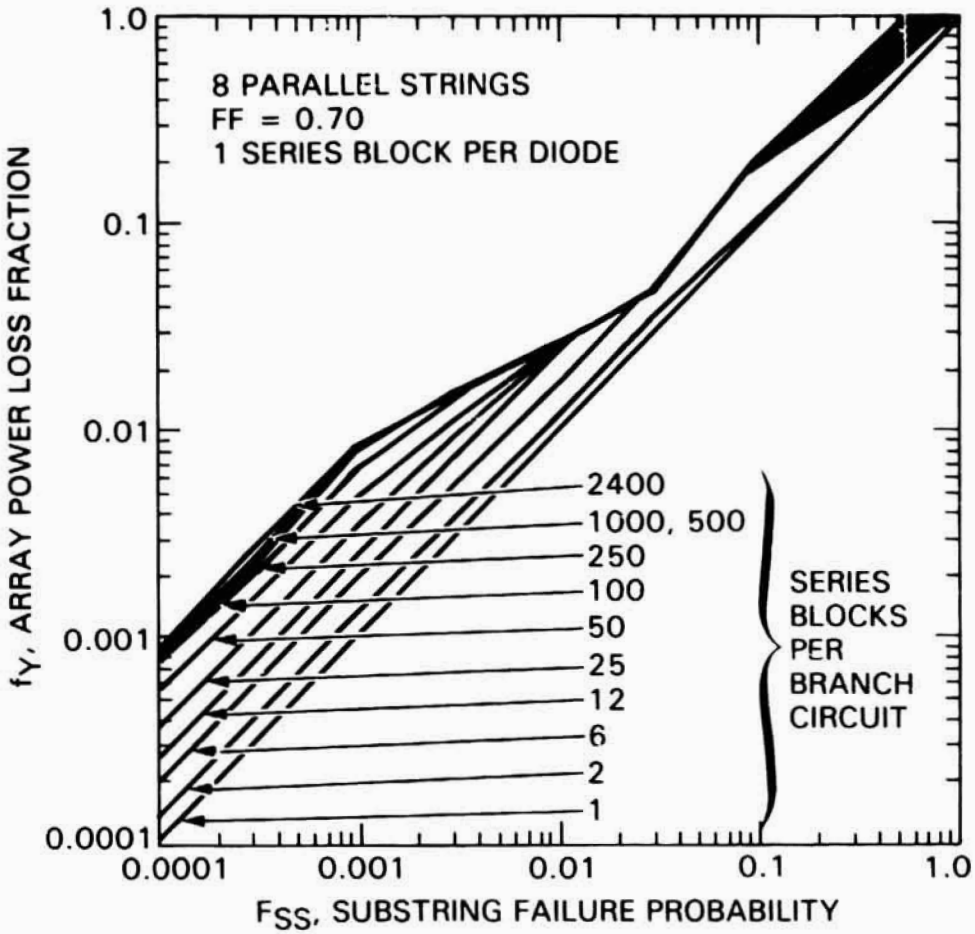


Figure 17. Array Power Loss

and

$$F_{SS} = 1 - (1 - p_c)^n \tag{11}$$

where

F_{SS} = substring failure probability

n = number of parallel interconnect groups per substring (see Figure 18)

p_c = cell failure probability

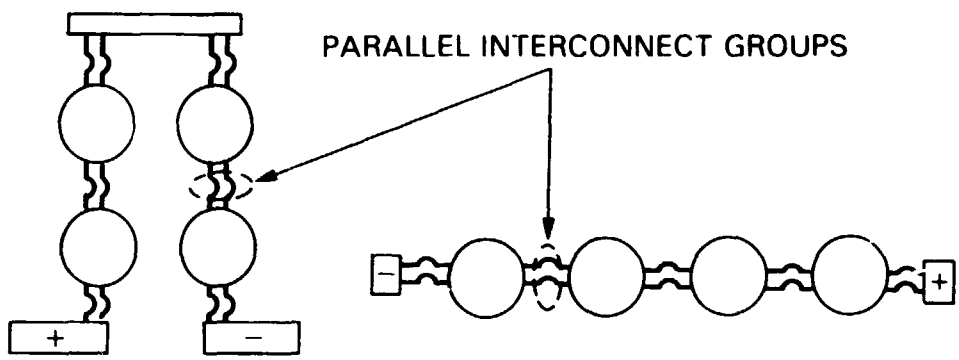
r = degree of interconnect redundancy

F_I = interconnect failure probability

The array power-loss fraction (the fraction of initial power output no longer deliverable to an external load) is assumed to result from substring failures caused by interconnect failures only.

$$F_{SS} = 1 - (1 - p_c)^n$$

F_{SS} = SUBSTRING FAILURE PROBABILITY
p_c = CELL FAILURE PROBABILITY
n = NUMBER OF PARALLEL INTERCONNECT GROUPS PER SUBSTRING



EXAMPLE: 4 CELLS,
r = 2
n = 6

EXAMPLE: 4 CELLS,
r = 2
n = 5

Figure 18. Relation Between Substring and Cell Failure Probabilities

A. AN EXAMPLE

To demonstrate the use of the array degradation algorithm, consider the example array design presented in Table 2. This table defines the detailed series-parallel circuit arrangement of a possible array using the nomenclature presented earlier in Figure 2.

The array degradation will be determined for a 20-year cumulative interconnect failure fraction $p_I = 0.150$ and an interconnect redundancy $r = 3$. Using these figures in Equation (10) gives a cumulative cell failure probability $p_c = 0.0034$. Then Equation (11) with $n = 12$ (see Figure 18) gives a substring failure probability $F_{SS} = 0.0398$. Entering Figure 17 with this value as abscissa and using the curve corresponding to 57 series blocks per branch circuit (interpolation required), it is determined that the array power loss fraction at 20 years is $f_Y = 0.054$ (power down 5.4%).

In this fashion an entire table (Table 3) of power reductions associated with specific failure probabilities and interconnect redundancies has been generated. The strain values listed in Table 3 were determined from the probabilities using the 20-year curve of Figure 14.

Table 2. Example Design Parameters

Array configuration:

(1) OFHC copper interconnects
(2) 8 parallel by 11 series cells per series block
(3) 57 series blocks per branch circuit
(4) One series block per diode
(5) V_{array} = 250 volts

Design objectives:

(1) 20-year array power reduction
(2) Interconnect failure probability
(3) Minimum life-cycle energy cost
(4) Required interconnect redundancy

Table 3 suggests two generalizations:

(1) Adding interconnects, i.e., increasing redundancy, dramatically reduces the array power loss rate over the 20-year array life.

(2) Allowing a higher maximum strain results in considerably larger power loss rates.

These observations are not surprising, but the high sensitivity of array power-loss to variations in strain is.

Table 3. Array Power Reduction at 20 years

20-Year Interconnect Failure Probability	Maximum Allowable Strain	Array Power Reduction at 20 years f_Y					
P_I	$\Delta\epsilon$	r = 1	2	3	4	5	6
0.005	0.0016	0.125	0.0018	0	0	0	0
0.010	0.0019	0.240	0.0059	0	0	0	0
0.050	0.0031	0.71	0.05	0.0070	0.0004	0	0
0.100	0.0040	0.96	0.24	0.029	0.0055	0.0007	0
0.150	0.0049	1.00	0.31	0.054	0.019	0.005	0.0013
0.200	0.0062	1.00	0.57	0.19	0.038	0.013	0.003
0.300	0.0069	1.00	0.90	0.46	0.20	0.048	0.023
0.400	0.0075	1.00	1.00	0.90	0.45	0.26	0.085
0.500	0.0081	1.00	1.00	1.00	0.80	0.53	0.32

SECTION V

LIFE-CYCLE ENERGY COST ANALYSIS

As was indicated in the previous section, the end result of interconnect failures is degradation of array power output. It was also shown that design techniques such as redundant interconnects can decrease the rate of degradation to negligible levels. Excessive interconnect redundancy, however, is costly. Economic considerations dictate a tradeoff between the degree of redundancy (cost) and the rate of power reduction (performance). This tradeoff is described in this section; it is achieved by minimizing the cost of energy generated over the life of the array.

Following the work of Ross (References 5 and 9), the cost of energy over the lifetime of the array field is determined by equating the worth of delivered energy with the cost of obtaining that energy. Letting R represent the (constant) cost of energy, it follows that

$$\sum_{n=1}^{Y} RE_n \, (1 + k)^{-n} = \sum_{n=o}^{Y} C_n \, (1 + k)^{-n} \tag{12}$$

or

$$R = \frac{C_o + \sum_{n=1}^{Y} C_n \, (1 + k)^{-n}}{E_o \cdot \sum_{n=1}^{Y} \epsilon_n \, (1 + k)^{-n}} \tag{13}$$

where

R = constant break-even energy cost, \$/kWh

C_o = initial plant cost, \$

C_n = operating cost in year n, \$

E_o = initial annual energy production, kWh

ϵ_n = fraction of initial energy in year n

k = present value discount rate

Y = end of array life, years

Noting that

$$E_o = I_o \cdot A \cdot \eta$$

where

I_o = annual solar insolation, kWh/m^2/year

η = initial plant efficiency (100 mW/cm^2, NOCT)

A = array area, m^2

and defining life-cycle energy fraction ϵ_{LC} as

$$\epsilon_{LC} = \sum_{n=1}^{Y} \epsilon_n (1 + k)^{-n} \tag{14}$$

allows Equation (13) to be written as (5, 9)

$$R = \frac{C_B + \dfrac{C_A + C_I + C_M}{\eta}}{I_o \epsilon_{LC}} \tag{15}$$

where

C_B = balance of plant costs, \$/kW

C_A = initial array costs less redundant interconnects, \$/m^2

C_I = estimated add-on cost of interconnects per square meter of module area, \$/m^2

C_M = life-cycle operation and maintenance costs, \$/m^2

Equation (15) provides the basis for determining the economic tradeoffs among interconnect fatigue life, interconnect redundancy, array degradation, and the fabrication costs associated with the various interconnect options.

A. AN EXAMPLE

To illustrate the detailed application of Equation (15), consider again the example design problem defined in Table 2. The assumed system cost and performance parameters that are independent of the interconnect design are presented in Table 4. Assumed add-on costs for the interconnects alone are presented in Table 5 as a function of interconnect redundancy alternatives. The objective of the analysis is to determine the appropriate choice of interconnect redundancy in light of costs, array degradation, and interconnect failure probabilities.

Appealing to Equation (15), the only undefined parameter is the life-cycle energy fraction ϵ_{LC}, which is determined by the expected array degradation versus time. Twenty-year array power reductions have already been presented in Table 3. For the same strain levels as in Table 3, array power fractions have also been calculated for 10, 5, and 2 years. Figure 19

Table 4. Design Example Cost Parameters

Balance of plant costs	C_B = 250 \$/kW
Initial array costs less redundant interconnects	C_A = 113 $\$/m^2$
Operation and maintenance costs	C_M = 0
Total plant efficiency	η = 0.092
Annual solar insolation	I_o = 2000 $kWh/m^2/yr$

Table 5. Add-On Costs for Interconnects

Interconnect Redundancy	Estimated Costs for Interconnects C_I, $\$/m^2$ of Module Surface
2	4.22
3	5.05
4	6.18
5	7.75
6	9.99

presents an example plot of array degradation versus time for a strain level of $\Delta\epsilon$ = 0.0049 and for various interconnect redundancies. With a zero discount rate [k = 0 in Equation (14)], the life-cycle energy fraction is the area under the curve representing the appropriate degree of interconnect redundancy; it is tabulated in Figure 19. Degradation curves and life-cycle energy fraction tabulations have been generated for each of the strain levels and associated 20-year cumulative interconnect failure probabilities listed in Table 3. The results of these calculations are summarized in Table 6.

Given the life-cycle energy fractions ϵ_{LC} in Table 6, it is now possible to use Equation (15) to calculate the life-cycle economics for the various cases. The results of doing this are displayed in Table 7. It is evident from Table 7 that life-cycle costs increase with increasing failure probability. Minimum costs for a given maximum allowable failure probability are boxed. It is noted that cost optimization requires that modules be designed for operation at low strain levels, although the variation in costs over the two-order-of-magnitude range of interconnect failure probabilities is small. It is also

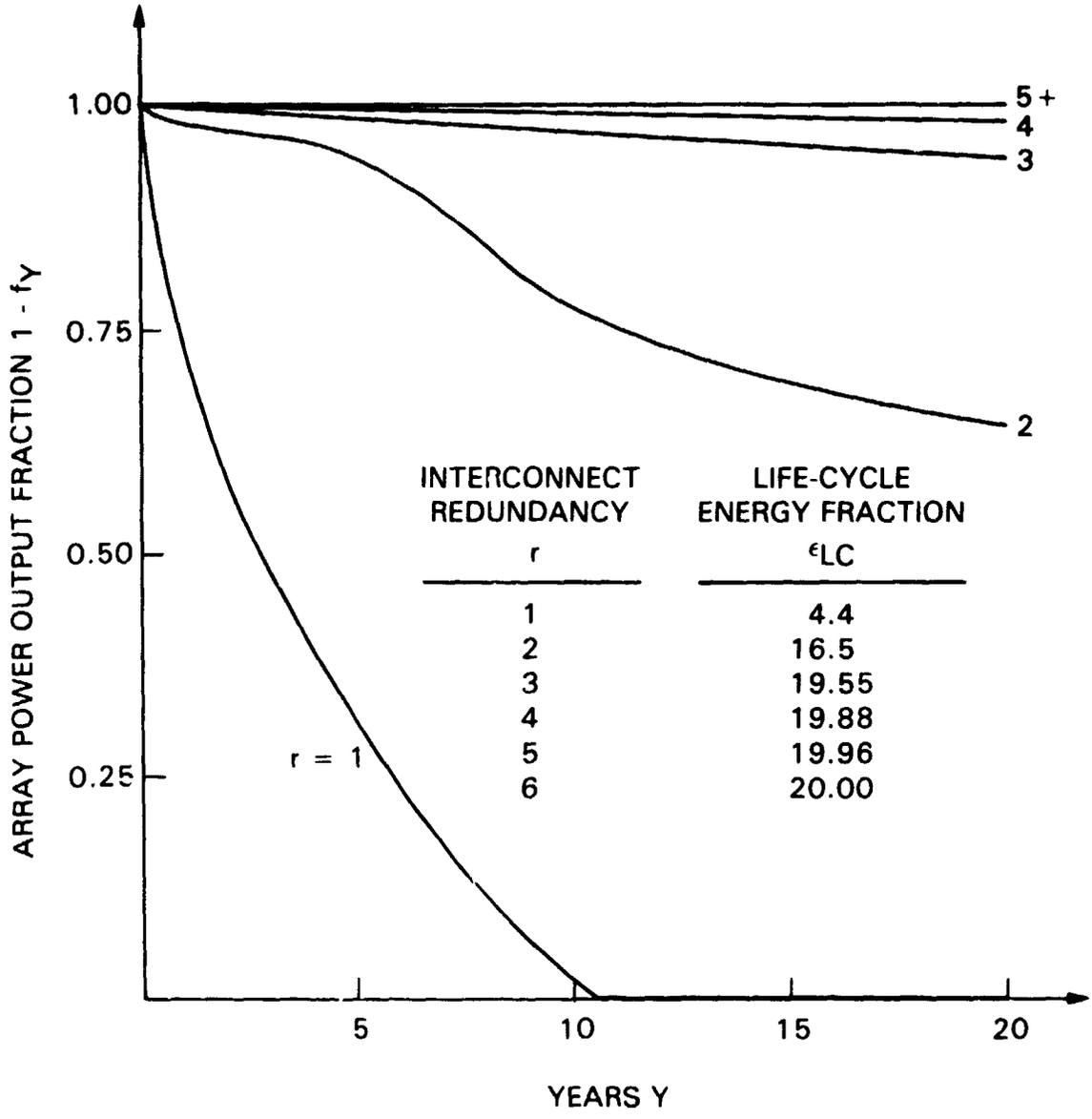


Figure 19. Array Power Output Fraction vs Years of Operation at an Interconnect Strain Level of $\Delta\epsilon = 0.0049$

noted that the various cost minima are relatively flat; e.g., at $p_I = 0.05$, the cost difference is using three, four, or five interconnects is negligible This is surprising, considering the extremely large variation in array power reduction for these degrees of redundancy (Table 3).

For the example module of Subsection III D., for which $p_I = 0.13$, the degree of interconnect redundancy and associated 20-year array power reduction can now be determined for the example array field under consideration. Table 7 suggests four interconnects per parallel interconnect group, giving a minimum cost of delivered energy of $0.0389/kWh. The array power loss fraction at 20 years (Table 3) is a very acceptable 0.0136.

Table 6. Life-Cycle Energy Fractions

20-Year Cumulative Interconnect Failure Probability	Maximum Allowable Strain	Life-Cycle Energy Fraction ϵ_{LC}					
P_I	$\Delta\epsilon$	r = 1	2	3	4	5	6
0.005	0.0016	17.8	19.95	20	20	20	20
0.010	0.0019	16.6	19.90	19.96	20	20	20
0.050	0.0031	11.7	19.45	19.89	19.98	20	20
0.100	0.0040	7.7	18.2	19.76	19.92	19.98	20
0.150	0.0049	4.4	16.5	19.55	19.88	19.96	20
0.200	0.0062	2.25	13.2	18.47	19.55	19.88	20
0.300	0.0069	1.74	11.2	17.1	18.65	19.66	19.91
0.400	0.0075	1.60	9.9	15.17	17.1	18.7	19.15
0.500	0.0081	1.5	8.9	13.2	15.6	17.4	17.9

Table 7. Life-Cycle Energy Costs

20-Year Cumulative Interconnect Failure Probability	Maximum Allowable Strain	Life-Cycle Energy Cost R, $/kWh					
P_I	$\Delta\epsilon$	r = 1	2	3	4	5	6
0.005	0.00160	0.0415	0.0382	0.0383	0.0386	0.0391	0.0397
0.010	0.00188	0.0445	0.0383	0.0384	0.0386	0.0391	0.0397
0.050	0.00305	0.0632	0.0392	0.0385	0.0387	0.0391	0.0397
0.100	0.00404	0.0960	0.0419	0.0388	0.0388	0.0391	0.0397
0.150	0.00487	0.1680	0.0462	0.0392	0.0389	0.0391	0.0397
0.200	0.00624	0.3285	0.0577	0.0415	0.0395	0.0393	0.0397
0.300	0.00693	0.4284	0.0680	0.0448	0.0414	0.0397	0.0399
0.400	0.00752	0.4620	0.0770	0.0505	0.0452	0.0418	0.0414
0.500	0.00808	0.4928	0.0856	0.0581	0.0495	0.0449	0.0443

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SECTION VI

THERMAL-CYCLING TESTING

As has been demonstrated, the algorithms developed in this study are useful in predicting end-of-life interconnect cumulative failure fractions for various module-interconnect design concepts. But when these design concepts are translated into hardware, sample modules from a manufactured lot must undergo testing to ascertain whether or not predicted failure fractions are indeed physically realistic expectations.

Thermal-cycling testing of modules is performed to qualify modules for field use. To date, however, practical interpretation of test results has been more an art than a science. But pass-fail judgments based upon thermal-cycling test results can be given a quantitative foundation, for corresponding to a maximum permissible field failure level at end of life, the generalized fatigue curves can be used to define a unique maximum permissible test failure level at a specified number of test cycles.

The thermal-cycling test is an accelerated test. One test profile in common use (Reference 10) is shown in Figure 20; the most recent test specifications require N = 200 test cycles. For this test profile, $\Delta T_{test} = 130^{o}C$. Then for a site for which $\Delta T_{field} = 46^{o}C$, it follows from the proportionality between the quantities $\Delta\epsilon$ and ΔT implied by Equations (2) and (3) that the test strain is given by

$$\Delta\epsilon_{test} = \frac{\Delta T_{test}}{\Delta T_{field}} \Delta\epsilon_{field} = 2.83\,\Delta\epsilon_{field} \qquad (16)$$

The test accelerates the interconnect strain range by a factor of 2.83 and the cycle rate by a factor of 4.

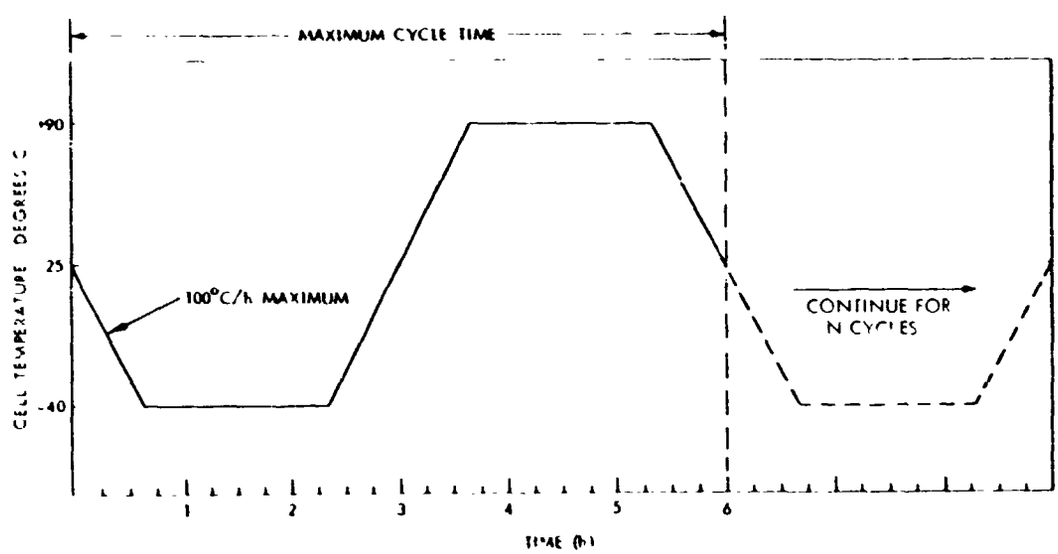

Figure 20. Thermal Cycling Test Conditions

In order to determine the maximum allowable number of interconnect failures in the test, use is made of the statistical fatigue curve, Figure 13, reproduced in Figure 21a. An example in Figure 21a shows that qualification for 20-year service at a 10% cumulative interconnect field-failure level requires that there be less than 4.2% failures at 200 test cycles. This type of calculation is continued to generate Figure 21b, which gives the maximum allowable interconnect test failure level for a specified number of test cycles to qualify a module for 20-year service at a typical field site for which $\Delta T \simeq 40^{\circ}C$. The example in Figure 21b indicates that the test failures should not exceed 4.2% at 200 cycles to qualify a module for 20-year service at a 10% field-failure level.

Table 8 presents thermal cycling test data and results from several differently designed modules. Pass-fail judgments are based on the criteria established in Figure 21b. The field-failure level for which the module is being qualified is seen to be an important factor in making pass-fail judgments.

Finally, because the purpose of thermal cycling testing is to provide type approval of a particular module design, a number of modules from the same lot--enough to provide at least 300 interconnects--should be tested in order to present a believable statistical picture of interconnect failures for that design.

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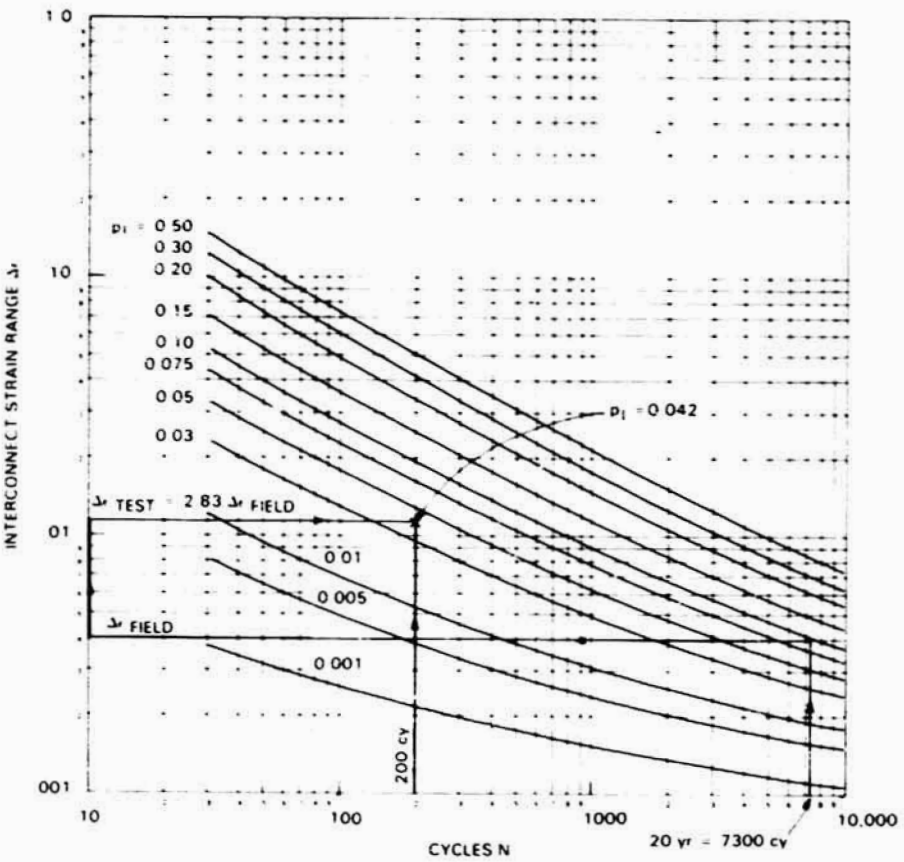

Figure 21a. Thermal Cycle Test Design for 20-Year Qualification at Typical Site ($\Delta T = 46^{o}C$)

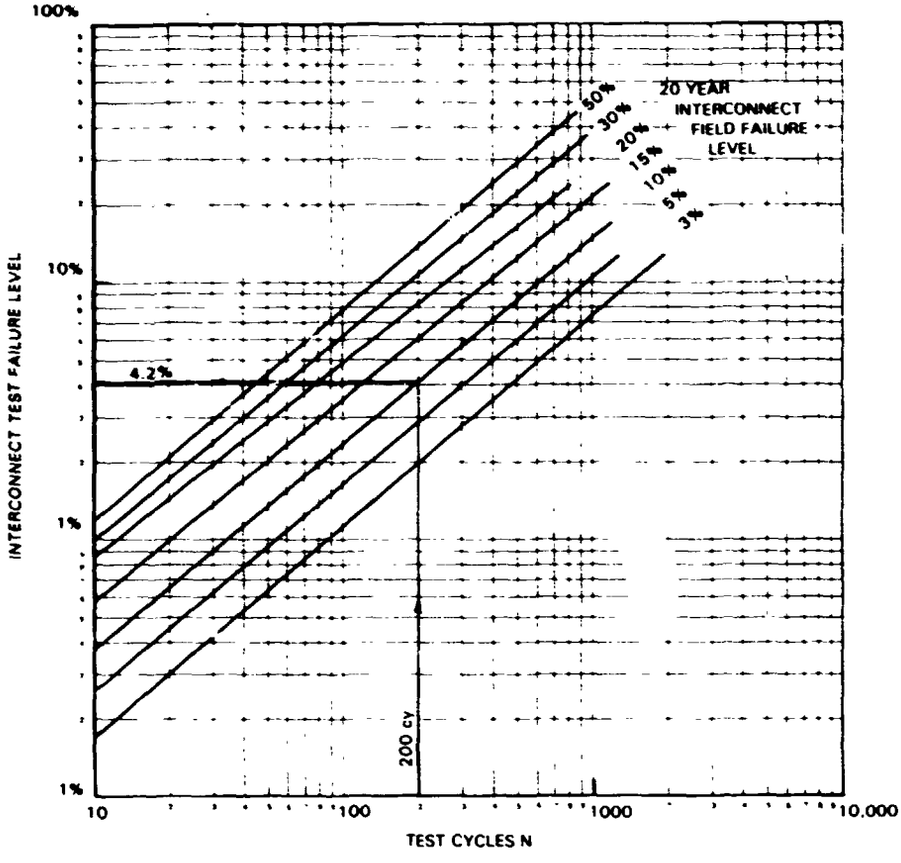

Figure 21b. Maximum Allowable Interconnect Test Failure Level for a Specified Number of Test Cycles With Field Failure Level as Parameter (Qualification for 20-Year Service at $\Delta T \approx 46^{o}C$)

Table 8. Module Qualification: 20-Year Service at $\Delta T \simeq 46^{o}C$

Thermal Cycle Test Results

Type of Module	Number of Thermal Cycles (ΔT = 130°C)	Observed Interconnect Test Failure Level, %	Qualification for 10% Field Failure Level: Max. Allowable Test Failure Level, %	Qualification for 10% Field Failure Level: Judgment	Qualification for 5% Field Failure Level: Max. Allowable Test Failure Level, %	Qualification for 5% Field Failure Level: Judgment
Randomly	297	67	5.9	Failed	3.8	Failed
Oriented	575	69	9.8	Failed	6.3	Failed
Glass	297	36	5.9	Failed	3.8	Failed
Fiber	575	69	9.8	Failed	6.3	Failed
Substrate	297	31	5.9	Failed	3.8	Failed
Superstrate	247	0	5.0	Passed	3.2	Passed
Superstrate	446	3	8.0	Passed	5.2	Passed
Superstrate	397	0	7.3	Passed	4.7	Passed
Substrate	547	6	9.3	Passed	6.2	Marginal
	547	10	9.3	Failed	6.2	Failed
Substrate	497	0	8.7	Passed	5.6	Passed
	497	7	8.7	Passed	5.6	Failed

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SECTION VII

DISCUSSION

Some caveats and discussion underlying the test and design philosophy, and some directions for future research are enumerated below.

(1) This investigation focused upon the thermally induced mechanical-fatigue failure of interconnects. The design and cost optimization algorithms are based on the assumption that array power-loss is attributable solely to interconnect failures, to the exclusion of such other contributing effects as cell breakage, encapsulation discoloration, electrical insulation failure, etc. A logical extension of this work is the incorporation of these and other factors into the design and cost algorithms.

(2) Although the fatigue curves presented in this report are limited to copper interconnects, the procedures developed are completely general. Another phase of this research involves the study of aluminum and clad metals. Aluminum exhibits fatigue behavior similar to that of copper and is much less expensive. Limited weldability and solderability may, however, restrict its use in this application. Clad metal interconnects, on the other hand, although more expensive to manufacture, exhibit none of the fabrication problems associated with aluminum interconnects and in addition may offer improved resistance to fatigue failures.

(3) Care must be exercised in comparing candidate interconnect materials to account for differences in electrical performance. This is particularly essential when comparing interconnects having different lengths, widths, thicknesses or electrical conductivities. In addition to affecting the electrical resistance of the interconnect, the width of the interconnect may also affect the metallization pattern on the cell and thereby the cell efficiency. The life-cycle cost analysis (Equation 15) explicitly deals with differences in electrical losses via the plant efficiency term η. An alternative strategy to avoid calculating the detailed electrical losses is to compare alternative interconnect designs adjusted to equalize electrical resistances and widths.

(4) The nomographs presented in Figure 6 are completely general and have application to structures other than interconnects--e.g., arches, walkways, cylindrical ribbing of aircraft fuselages and submarine hulls, pipeline expansion loops, etc.

(5) Elastic behavior on the part of the interconnect has been assumed in this study in using the finite element modeling procedure to calculate interconnect strains. In reality, however, interconnect behavior is largely plastic. Two factors justify using elastic analysis to determine strain in interconnects behaving plastically in service. The first is cost--the cost of performing plastic analysis is prohibitive. The second factor is that elastic

analysis yields good results (it works), as is evident from the data of Figure 7. In that figure, the plotted experimental data points for which strain levels have been computed agree well with the empirical elastic-plastic fatigue curve of the interconnect material.

(6) The large temperature range of the module thermal cycling test and the rapid cycling of interconnects in the mechanical simulation tests--both contrary to existing field conditions--may be questioned. Most investigators seem to disregard cycle rate and moderate temperature extremes as influential factors in the mechanical fatigue of metals. The various experimental data presented in Figure 7 agree well with each other despite considerable variation in cycle rate. The mechanical simulation tests are conducted at 30 cycles per minute, the thermal cycling test at 4 cycles per day. The data of Coffin and Tavernelli (Reference 4) were obtained at 7 to 16 cycles per minute, and field cycles are 1 per day.

The fundamental requirement of an accelerated test is that it not introduce degradation modes not active in the intended application. Enhanced temperature range (thermal-cycling tests) or lack thereof (mechanical simulation test) were not observed to violate this requirement. In fact, many degradation modes are suppressed in such tests, e.g., hail impact, wind loading, etc., but these modes do not generally contribute substantially to interconnect failures. The major interconnect failure mechanism is thermally induced strain cycling (Reference 2), i.e., fatigue, and the primary cause of premature interconnect failure is faulty module-interconnect design.

SECTION VIII

SUMMARY

Interconnect fatigue performance has been characterized by the interconnect material fatigue curve. Nomographs have been developed to facilitate the computation of interconnect strain. Based on the interconnect material fatigue curve and experimental failure rate data, array life prediction has been demonstrated. A design algorithm has been developed enabling the selection of minimum cost redundant interconnect systems. Thermal-cycling testing of modules for the purpose of characterizing interconnect performance has been given a quantitative foundation--particularly in regard to acceptance-rejection threshold levels.

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