IMAGE PROCESSING VIA VLSI

A Concept Paper

Robert Nathan, Ph.D.
19 January 1981
Image Processing via VLSI

Abstract

The general purpose digital computer is not able to handle the data rates and subsequent throughput requirements of data systems in the mid-80's and early 90's. In particular vast quantities of image data will have to be calibrated, geometrically projected, mosaicked and otherwise manipulated and merged at rates that far exceed the capacities of present systems. Even the "super" computers, some of which have been designed explicitly for image processing, promise insufficient throughput capacity. Implementing specific image processing algorithms via Very Large Scale Integrated systems offers a potent solution to this perplexing problem. Two algorithms stand out as being particularly critical -- geometric map transformation and filtering or correlation. These two functions form the basis for data calibration, registration and mosaicking. VLSI presents itself as an inexpensive ancillary function to be added to almost any general purpose computer and if the geometry and filter algorithms are implemented in VLSI, the processing rate bottleneck would be significantly relieved. This work develops the set of image processing functions that limit present systems to deal with future throughput needs, translates these functions to algorithms, implements via VLSI technology and interfaces the hardware to a general purpose digital computer.

Objectives

* Design and fabricate special purpose VLSI chips to perform specific image processing algorithms.
* Integrate such chips into interface systems which are under the control of a central general purpose processor assigned to image processing.
* In particular, design and test filter system and a cubic spline geometric reprojection system.

* Examine and develop VLSI design concepts for other image processing requirements.

**Motivation**

Bracken (1) has spelled out the need for improving the processing speed of image data collected from an ever increasing array of satellites each with a larger information bandwidth than its predecessor. The processing problem has several dimensions.

* In order to enable the end user to use new information, the data must be restructured to match a previous information base. A common requirement is to reproject and register images taken from an oblique satellite view to a normal projection on the surface. This reprojection along with the need to correct for any systematic camera distortions requires that images be stretched like a "rubber sheet" to fit the desired reprojection. This shift which entails many rotations and magnifications within each image requires relocation of interpolated data to locations which may be far distant from some original position.

* In order to determine the precise shift which will bring two images into registration, match points must be determined. Modified cross correlation calculations can be used to maximize the best fit of these match points. Correlation and filtering have similar mathematical structure and both can be implemented with a special purpose VLSI system. The filtering operation is also used to smooth noisy data or enhance fine image detail. Image enhancement has been applied rather infrequently in spite of image improvement because
it is an expensive process. VLSI operation can reduce the cost and time of processing. Filtering also enables certain feature detection and extraction algorithms.

* Another dimension of image processing relates to where in the data stream the processing is to be performed. Our present technology thus far requires transmission of unprocessed images. As high speed compact processing technology evolves, processing can be moved on to the satellite and transmission bandwidth reduced by several orders of magnitude.

* Pipeline processing implies placing simultaneous hardwired algorithms in tandem. Other image processing functions such as sorting maximum values, change detection, developing time dimensions on accumulated data bases become accessible in near real time when thinking in terms of modular hardware.

**Background**

Digital image processing became a working reality in the early 1960's with the advent of JPL's Ranger, Surveyor and Mariner series. We (Nathan-2) had effectively established the requirements for various processing algorithms from pragmatic pressures. Filtering was performed to remove systematic noises from the camera and geometric corrections also were required to correct camera distortion. Filtering further evolved to enhance fine image detail without stretching low frequency data to cause image saturation. In those early missions it was generally possible to keep up with the data load with the processing power of computers available at the time. No real attempt was made to do more than refine those algorithms using commercially available machines. Since that time the situation has dramatically changed in terms of volume while the algorithms have remained relatively static.
Several attempts at creating special parallel processors have proven expensive and unwieldy. A comparison of several "super" computers was performed by Mitre Corporation (3). They were given several classes of very limited tests against which to measure processing effectiveness. Some of the computers compared were the Cray I, the DAP (English), the PEPE (Army), the Illiac IV, the Cyber 203, the AP-120B, the CLIP 3 and the MPP (Goddard-Goodyear). All but the AP-120B are extremely expensive (several millions of dollars each) whereas the AP-120B is very much slower. Mitre judged the MPP to be the best as determined from the given conditions. But the filter and geometric test problem was much too constrained and just fit the 128x128 area of parallel memory in MPP. Only a kernal of 20x20 can be filtered against a 128x128 image. Only a shift of 8 pixels using linear interpolation is allowed for geometric remapping. These restrictions have been hardwired and only slow software can overcome them. The heart of the MPP is a general purpose VLSI processing unit. The direction of the concept is still in terms of multiple function performance by a particular hardware unit.

VLSI is a general tool which can be viewed as an extension of software in the sense of the next generation of computing power. These concepts have been under development at Caltech under Mead (4). JPL has a very close relationship with the campus. We have recently been working with Mead to aid in the rapid evolution of the software techniques for designing VLSI circuitry and have, in addition, been developing filtering hardware concepts following a data flow algorithm from Cohen (5) which allows successive multiplier-accumulators to be pipelined. A modification in memory handling allows an extension to two dimensions and is being breadboarded to fit the VLSI design. As a seed effort we have started to
design a VLSI chip which will allow us to create a 31x31 element kernal that will compete favorably timewise and dollarwise against the MPP.

**Approach**

VLSI design is still a rapidly evolving field. Computer languages are under development which will eventually allow high level statements to be made which establish functional criteria and these statements would be converted to n-channel metal oxide semiconductor (n-MOS) or complementary c-MOS wire lists. These lists are in turn converted by computer to drawings of different overlays of metal and metal oxides. The drawings are then photo-reduced and photo-etched onto silicon or sapphire wafers which are then cut and wired to form individual chips.

The amount of logic that can be placed on a single chip is also evolving rapidly. Today many tens of thousands of transistors can be stored on a surface 7x7 mm sq. Within three to five years that number is expected to increase by 2 to 3 orders of magnitude. At JPL we are experimenting with ways to develop languages which will allow variation of parameters, number of multipliers, number of bits/multipliers, serial or parallel additions/multiply and other parameters which will allow us to tailor fit to customer need without massive redesign effort.

As we contemplate the marriage of VLSI technology with image processing requirements, not all the pieces are yet in place. Some of the designing effort is still initiated by manual drawings to meet VLSI design rule requirements. The logic for multiplication is still not finalized as competition for area (on the chip) and speed (minimum clock cycles per multiply) is under study. Conceptual design for the geometry operation is under rapid restructuring as various experts are consulted (Billingsley-6). Projects like these are studied by Caltech students in

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Prof. Mead's classes and valuable interchange is derived from those discussions. The whole idea is to be able to upgrade design concepts and create new VLSI chips as though debugging computer software.

In parallel with the actual chip development hardware is being developed to interface the VLSI to existing computer structures. A not too surprising result emerges as this effort progresses. VLSI allows an improvement in throughput over a serial general purpose computer by a factor of 2 to 3 orders of magnitude. We very quickly become I/O bound in terms of magnetic tape or disk. Consideration must be given to grabbing the data once from mass (serial) storage, and performing all processes at once (pipeline serial) before sending the restructured data or extracted information back on to tape or out to the customer.

We have spent some time with the initial development of a VLSI chip which presently has four multipliers each of which stores 20 bits and multiplies an 8-bit pixel by a 12-bit weight. The chip has been submitted for fabrication external to JPL. Turnaround is about two months. JPL's role is not to compete with the commercial fabrication process, but we are more interested in developing more versatile VLSI design tools.

Some effort has gone into the concept of a pipelined geometry remapping chip. An initial concept designed by us (Nathan) was tried successfully by Northrup for the Air Force. But that was only a nearest neighbor design. We have developed many software algorithms over the years, and recently thought is being given to a four point modified cubic spline which should not degrade the image as does nearest neighbor or linear interpolation. The concept is to perform two orthogonal stretches (or contractions) along each axis as serial operations (pipelined in two VLSI functions) while have direct access to several megabytes of random
access memory from the computer main frame. The proposed speed of transformation is many times that presently available.

Expected Results

Two sets of hardwired algorithms are to be produced. One algorithm will perform two dimensional filtering or correlation on an arbitrarily large image using a 31x31 kernel (at present design -- a modifiable parameter). The other algorithm is a pair of one dimensional cubic spline geometry remapping functions which under software control will "rubber sheet" one image to another according to pre-established pass points. It is expected that these systems will be installed for use in JPL's Image Processing Laboratory (IPL) and be used in their image processing production mode.

Progress is anticipated in the development of software which utilizes the filter hardware to establish "pass points" and these in turn will generate the correction grid for the geometry hardware.

Also investigation into class extraction using the filter hardware will be started. Studies of this sort exist as software only. It is desired to explore increased dimension of class search once a fast hardware filter becomes available.

Another product which can be expected is the ability to reproduce other VLSI configurations with minor changes in design parameters. This ability gives us the power to update new hardware without major mechanical redesign as customer needs change.

As concepts develop regarding the utility of other imaging operations, these too shall be pursued.
References


3. MITRE Corp. (1979) - "Parallel Processor Technology Trade-off Study for the NASA End-to-End Data System (NEEDS)."


DATA SYSTEM DRIVER

DATA VOLUME

BITS PER YEAR

YEAR

DATA DELIVERY TIME (HOURS)

YEAR
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VL$1

VERY LARGE SCALE INTEGRATED SYSTEMS

PARALLEL/PIPELINE PROCESSING

CONCURRENT VS. SERIAL

MANY (> 10,000 TRANSISTORS) ON A SINGLE CHIP

INEXPENSIVE WHEN COMPARED TO DISCRETE LOGIC

NEXT EVOLUTIONARY STEP BEYOND SOFTWARE

COMPUTERS GENERATING COMPUTERS

HIGH LEVEL LANGUAGE USED TO CONVERT
ALGORITHMS INTO HARDWARE

COST EFFECTIVE COMPARED TO SERIAL PROCESSORS
(a) NAND gate layout geometry.

(b) NAND gate topology (schematic diagram).

(c) NAND gate equivalent logic symbol.
(a) Stick diagram of one row of a shift register array.
DIGITAL MULTIPLIER

- TYPICAL IC MULTIPLIERS CONTAIN REGISTERS FOR MULTIPLIER AND MULTIPLICAND OPERANDS.
- AN ADDITIONAL REGISTER IS PROVIDED FOR THE PRODUCT.
- MODERN LSI MULTIPLIERS PERFORM ADDITIONS IN A RIPPLE FASHION. THAT IS, EACH SUM IS PASSED ON FROM ONE ADDER TO THE NEXT WITHOUT THE USE OF CLOCKED SEQUENTIAL CIRCUITS. THEREFORE, THE MULTIPLIER IS COMPRISED OF AN ARRAY OF GATES AND ADDERS.
CLOCK
START/LOAD \( p \) AND \( 0 \) SET
FIRST PRECHARGE/DECODE
CARRY SAVE ADD
SHIFT CARRY SAVE RESULTS
LOAD CARRY SAVE
LOAD FULL ADDER
SECOND PRECHARGE
LOAD \( \omega_p \)
\( \omega_p \) SHIFT TO FULL ADDER
\( \Sigma \omega_p \) LOAD
\( \Sigma \omega_p \) HOLD

\[ \text{START} \quad \text{PAUSE} \quad \text{START} \]
LOCATION OF LANDSAT SCENES
GEOMETRIC REPROJECTION
RESAMPLING

\[ N = p_1 w_1 + p_2 w_2 + p_3 w_3 + p_4 w_4 \]

\( f \) FRACTIONAL DISTANCE BETWEEN POINTS

FOR LINEAR INTERPOLATION OF NEW SAMPLE VALUES

\[ w_1 = w_4 = 0 \]
\[ w_2 = 1 - f \]
\[ w_3 = f \]

THEREFORE \( N_1 = p_2 (1-f) + p_3 f \)

FOR CUBIC INTERPOLATION ALL FOUR \( w_i \) ARE A TABLE LOOK UP FUNCTION OF \( f_i \).

THE NEW INTERSAMPLE DISTANCE \( (d) \) CAN ALSO BE NONLINEAR.
ALLOWANCE IS MADE FOR CUBIC SPLINE ADJUSTMENT FOR NON-LINEAR SAMPLING.

RNATHAN
MARCH 1982
Mass Memory
(70 megabytes for 8000² pixels)

Memory
(2 lines in and 2 lines out)

VLSI
Samples and fraction calculation;
Sample number

VLSI
Ni = \sum_{i=1}^{4} w_i p_i
(resembles filter chip)

Weight Tables Wi

(data flow control and parameter generation)

DISK or Mag Tape

GEOMETRIC REPROJECTION

R. NATHAN
3/82
SELECT & COUNT

load parameters

COUNTER SET 2's COMP

LOAD CLOCK

START

CLOCKS

POWER

No feedback during load parameters

LOAD PARAMETERS

INCR 1 2 3

WHOLE FRACTION

SPLINE WEIGHT SELECT

PIXEL MEMORY SELECT

A inc (linear)

B inc Δ (quadratic)

C inc Δ² (cubic)

0 test
FUNCTIONAL ELEMENTS OF CAMPUS DESIGN SYSTEM

Circuit Logic

Switch-Level Simulator

Layout Program

Design-Rule Checker

Circuit-Node Extractor

CIF File

To Fabrication Broker

Notes:
1. At JPL, system will run using MAINSAIL compiler on VAX 11/780 with VMS Operating System
2. Switch-Level simulator is based on MIT work of Bryant and Temans.
FUTURE

INDUSTRY DOES NOT WISH TO DEVELOP CUSTOM CHIPS INTERESTED IN MASS MARKET

JPL AND OTHER USER INSTITUTIONS NEEDED TO DEVELOP HIGH LEVEL SOFTWARE TO CONVERT ALGORITHMS TO PARALLEL HARDWARE

POTENTIAL APPLICATION AREAS

PATTERN EXTRACTION

SAR

I/O PARALLEL DATA FLOW

OTHER DATA BOTTLENECKS
Mass Memory
(70 megabytes
for 8000^2 pixels)

Memory
(2 lines in
and 2 lines out)

Weight Tables
Wi

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Samples and fraction calculation;
Sample number

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POTENTIAL APPLICATION AREAS
PATTERN EXTRACTION
SAR
I/O PARALLEL DATA FLOW
OTHER DATA BOTTLENECKS
MIXTURE PIXELS
P. Swain

I. HISTORICAL PERSPECTIVE
II. ORIGINS OF THE PROBLEM
III. INDUCED PROBLEMS
IV. APPROACHES TO SOLVING THE PROBLEM AND "STATE OF THE ART"
V. DISCUSSION: RELEVANCE IN THE PRESENT CONTEXT
Adapted from Nalepka & Hyde (ERIM)