General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.

- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.

- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.

- This document is paginated as submitted by the original source.

- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

Produced by the NASA Center for Aerospace Information (CASI)
NORTH CAROLINA AGRICULTURAL AND TECHNICAL STATE UNIVERSITY

Department of Electrical Engineering
Greensboro, N.C. 27411

ANNUAL REPORT
ON
MATERIAL GROWTH AND CHARACTERIZATION
FOR SOLID STATE DEVICES

Report Period: October 1, 1982 to November 30, 1983

Submitted to
National Aeronautics and Space Administration
Langley Research Center

Research Grant No. MSG 1390

Submitted by:

E. K. Stefanakos
W. J. Collis
A. Abul-Fadl
S. Iyer
MATERIAL GROWTH AND CHARACTERIZATION FOR SOLID STATE DEVICES

SUMMARY

During the reporting period, InGaAs was grown on Fe-doped (semi-insulating) (100) InP substrates by CCLPE at 640°C and current densities of 2.5A/cm² to 5A/cm² for periods from 5 to 30 minutes. Special efforts were made to reduce the background carrier concentration in the grown layers as much as possible. The best layers exhibited carrier concentrations in the mid-$10^{15}$ cm⁻³ range and up to 10,900 cm²/V-sec room temperature mobility. InGaAsP quaternary layers of energy gap corresponding to wavelengths of ≈1.5μm and 1.3μm were grown on (100) InP substrates by CCLPE. In the device fabrication area, work was directed toward processing MISFET's using InGaAs. SiO₂, Si₃N₄ and Al₂O₃ were deposited by ion beam sputtering, electron beam evaporation and chemical vapor reaction on Si, GaAs, and InGaAs substrates. SiO₂ and Si₃N₄ sputtered layers were found to possess a high density of pinhole defects that precluded capacitance-voltage analysis. CVD-deposited Al₂O₃ layers on Si, GaAs and InGaAs substrates also exhibited a large number of pinhole defects. This prevented achieving good MIS devices over most of the substrate surface area.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Summary</td>
<td>i</td>
</tr>
<tr>
<td>Introduction</td>
<td>1</td>
</tr>
<tr>
<td>Growth and Characterization of InGaAs</td>
<td>1</td>
</tr>
<tr>
<td>Growth and Characterization of InGaAsP</td>
<td>2</td>
</tr>
<tr>
<td>Processing for MISFET Devices</td>
<td>8</td>
</tr>
<tr>
<td>- Silicon dioxide</td>
<td></td>
</tr>
<tr>
<td>- Silicon nitride</td>
<td></td>
</tr>
<tr>
<td>- Aluminum oxide</td>
<td></td>
</tr>
<tr>
<td>References</td>
<td>14</td>
</tr>
<tr>
<td>Appendix A</td>
<td>16</td>
</tr>
</tbody>
</table>
The main research objectives for the period of the grant (October 1, 1982 to November 30, 1983) were:

(a) Growth and characterization of InGaAs and InGaAsP, lattice matched to InP, by current controlled LPE (CCLPE)
(b) Study of methods of depositing insulating materials such as Al2O3, SiO2 and Si3N4 on InGaAs for device structures and
(c) Growth of multilayers of InP, InGaAs and InGaAsP by CCLPE for fabrication of devices.

During the reporting period objectives (a) and (b) were mainly pursued. A new system specifically designed to be used for the growth of multilayers, has presented problems that have caused a delay in the pursuance of task (c). In what follows results primarily on objectives (a) and (b) will be presented.

A. Growth and Characterization of InGaAs

InGaAs was grown on Fe-doped (100) InP substrates by CCLPE at 640°C and current densities of 2.5A/cm² to 5 A/cm² for periods from 5 to 30 minutes. The experimental apparatus and procedure have been described previously. The InGaAs epilayers were characterized for surface morphology and epilayer uniformity, electrical characterization using Hall measurements at 300K and 11K temperatures, and room temperature photoluminescence measurements. To protect the substrate surface from degradation during melt bakeout a remote loading technique was utilized. The lattice mismatch between the epilayer and substrate was determined
by X-ray measurements and found to vary from -0.04% to -0.12%\(^1\). The growth velocity of the InGaAs layers was determined to be 0.06\(\mu\)m/A-min at 640°C. The carrier concentration and carrier mobility of the epilayers were determined by Hall measurements. The best samples had background carrier concentrations in the mid -10\(^{15}\) cm\(^{-3}\) range and room temperature mobilities up to 10,900 cm\(^2/V\text{-sec}\)\(^1\). The energy gap of the grown layers was determined by photoluminescence measurements and varied between 0.74 and 0.75 eV\(^1\).

B. Growth and Characterization of InGaAsP

The growth of quaternary layers by current controlled liquid phase epitaxy (CCLPE) has been carried out in a horizontal slider boat system described in detail elsewhere\(^1\). Quaternary layers of energy gaps corresponding to the wavelengths of ~1.5\(\mu\)m and ~1.3\(\mu\)m have been grown by this technique. They will be referred to as A- and B-epilayers, respectively, in the report for simplicity.

The growth melt consisted of 6N pure In, undoped InP, undoped GaAs and InAs. The weights of these components are based on the liquidus composition reported by Hsieh\(^2\). However, it is found necessary to add GaAs in slight excess to the reported values, for the growth of quaternary layers by the CCLPE technique. InP was also added in excess to minimize any variation in the liquidus temperature of the melt due to the loss of P by evaporation.

Initially In, GaAs and InAs were baked for approximately 12 hours in a hydrogen ambient followed by another 12 hours after the addition of excess InP. It was ensured that there was no temperature overshooting either during baking or saturation period, thus eliminating the possibility of any supersaturation during the growth cycle. <100>-oriented InP wafers 16 mil thick and of area 0.6 x 0.6 cm were used as substrates. In a typical growth run, the melt was saturated for ~14-16 hours at the growth temperature (~647°C). The thermal degradation of the substrate was minimized by sliding the substrate underneath the basket containing an In-Sn-P melt. The CCLPE growth was accomplished by passing a dc current across the substrate-melt interface and advancing the back-contact melt to establish electrical contact.
Nomarski phase contrast microscopy has been used to examine the surface morphology and thickness profile. Some layers were terraced, being more pronounced at higher current densities as indicated in Figs. 1 and 2. Lateral edge growth, often twice the thickness of the epilayer, has been observed in A-layers. Further, the area over which the layer is uniform, decreased with increase in layer thickness. No such edge growth has been observed in B-layers. However, the roughness of the B-layers increased with thickness. We believe that this may be due to a depletion of solutes at the interface. The thickness of epilayers characterized in the work were typically in the range of 1.4 - 5.0μm and 1.4 - 3.0μm for A- and B-layers, respectively.

Figures 3 and 4 indicate the linear dependence of current density on the growth rate. The thickness of the A-layers corresponds to that measured in the middle of the substrate, neglecting the edge growth. In the absence of current, spotty growth was obtained for A-layers, while no growth was observed for B-layers. These observations confirm that the quaternary layer growth was current controlled.

Figure 5 indicates the variation in the growth rate of the epilayers at a current density of 10A/cm² over the entire composition range from In₀.₅₃Ga₀.₄₇As to InP (the composition of the quaternary layers is an estimation based on our photoluminescence spectra discussed in detail later). In order to compare our results with the reported values of growth rate by conventional LPE, the data reported in the literature for step-cooling techniques are also plotted in Fig.5. It may be observed that, unlike in the case of CCLPE, the growth rate is not as strongly dependent on the composition.

Photoluminescence spectra have been taken for quaternary layers at room temperature. A systematic shift in the photoluminescence peak from 1.54μm to 1.49μm has been observed for A-layers when the same melt is used for a number of growth runs, indicating a change in the composition of the epilayer. However, for
Figure 1. Nomarski contrast photomicrograph of 1.7μm thick quaternary layer, grown with a current density of 2.8A/cm² for 25 minutes.

Figure 2. Photomicrograph of a 2.2μm thick quaternary layer, grown with a current density of 14.9A/cm² for 7 minutes.
Figure 3. Variation of growth rate with the current density for A-layers grown at a constant temperature of ≈ 648°C.
Figure 4. Variation of growth rate with current density for B-layers grown at a constant temperature of \( \approx 647^\circ C \)
Figure 5. Growth rate as a function of alloy composition. The dotted line represents the growth rate of epilayers by CCLPE technique at a current density of 10A/cm². The solid line is the published results on the growth rate by step-cooling techniques at a growth temperature range of 620-650°C with a step cooling temperature \( \Delta T = 10°C \). (\( \Delta \) Ref. 2a, (x) Ref. 2b, (•) Ref. 2c, Ref. 2d and (□) Ref. 2e.
B-layers, a maximum shift of \(-16\)Å from 1.326Å to 1.310Å has been observed using the same melt.

C. Processing for MISFET Devices

The goal of this task is to fabricate elementary insulated gate field effect transistors (MISFET's) using the CCLPE InGaAs material and techniques which can be accommodated in this laboratory. The interfacial properties of the semiconductor-insulator system are the primary factor in the choice of the insulator materials. These interface properties may also be significantly altered by the insulator deposition technique. Certainly, thermally grown SiO\(_2\) on Si would be the standard for comparison of other systems.

A variety of materials for eventual application as gate insulators were investigated. The results of several deposition techniques are discussed here. The ultimate requirement, for a MISFET device, is a gate insulator which presents a stable interface with the semiconductor such that inversion and accumulation of the surface can be achieved. The capacitance-voltage characteristic should not exhibit hysteresis looping or an excessive flatband voltage shift.

The three insulator materials studied were SiO\(_2\), Si\(_3\)N\(_4\), and Al\(_2\)O\(_3\). These were deposited by ion beam sputtering, electron beam evaporation and chemical vapor reaction. Silicon, GaAs, and CCLPE GaInAs were used as substrates.

**Silicon dioxide**

A quartz target was used in the ion beam sputtering system with the substrate at room temperature. Aluminum gated MIS capacitors were formed by evaporation of Al through a dot mask. For both the Si and GaAs substrates, the capacitors were found to be short circuited to the substrate. Probes pressed on the SiO\(_2\) surface, on the other hand, did not exhibit observable leakage currents on a transistor curve tracer. This, it was assumed that the sputtered SiO\(_2\) layers had a high density of pinhole defects.
**Silicon nitride**

Again, the ion beam sputtering system was used to deposit Si$_3$N$_4$ from a pressed target. The deposition conditions are described in Appendix A, and in the Semi-Annual Report$^1$. In general, the pinhole difficulty was encountered with these sputtered layers on GaAs and GaInAs. Some Al-Si$_3$N$_4$-nSi capacitors were achieved, but the capacitance was essentially constant over a ±20 volt bias range.

**Aluminum oxide**

This insulator has been used to form MIS capacitors and FET devices on Si, GaAs, InP, GaInAs and InGaAsP. The deposition techniques include electron beam evaporation, chemical vapor deposition (CVD) and anodic oxidation. Table I indicates some literature references for this material.

The InP FET's$^{3,4}$ exhibited a slow drift in the drain current. This drift is caused mainly by trapping centers in the native oxide on the InP prior to the Al$_2$O$_3$ deposition. By performing an in situ vapor etching with HCl, the density of surface states was reduced$^{11,12}$. The aluminum oxide was deposited by the pyrolytic decomposition of aluminum isopropanoxide.

In this present work aluminum oxide was deposited by electron beam evaporation using a sapphire boule source, and by the pyrolytic decomposition of Al(OC$_3$H$_7$)$_3$ vapor in argon. The Al$_2$O$_3$ was evaporated onto Si, GaAs and InGaAs substrates. With Al capacitor electrodes the GaAs and InGaAs samples exhibited short-circuiting pinhole defects. The one successful Al-gated nGaAs capacitor possessed a relatively constant 1 MHz capacitance over a ±20 volt bias range. The Al-nSi capacitors exhibited a typical high frequency
<table>
<thead>
<tr>
<th>TABLE  I.  LITERATURE REFERENCES UTILIZING ALUMINUM OXIDE IN DEVICE APPLICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference</td>
</tr>
<tr>
<td>3 4 5 6 7 8 9 10</td>
</tr>
<tr>
<td>MIS Capacitors</td>
</tr>
<tr>
<td>FET's</td>
</tr>
<tr>
<td>Si</td>
</tr>
<tr>
<td>GaAs</td>
</tr>
<tr>
<td>InP</td>
</tr>
<tr>
<td>InGaAs</td>
</tr>
<tr>
<td>InGaAsP</td>
</tr>
<tr>
<td>E-beam evaporation</td>
</tr>
<tr>
<td>Chemical vapor deposition</td>
</tr>
<tr>
<td>Anodic oxidation</td>
</tr>
</tbody>
</table>
C-V characteristic with a hysteresis loop about 6 volts wide. These results are presented in Appendix A. Since a system for performing low frequency capacitance measurements was not available, the existence of an inversion regime could not be demonstrated. Annealing the Si capacitors at 350°C in nitrogen, reduced the width of the hysteresis loop to about 3 volts.

The previously indicated reports of MIS capacitors and FET's formed on InP by the chemical vapor deposition of Al₂O₃ prompted an interest in developing this technique. The system employs a graphite susceptor heated by a light source external to the reaction tube. A diagram of the Al₂O₃-CVD system is shown in Fig. 6. The deposition occurs in the range of 300-400°C and the temperature can be maintained quite constant in this range. Argon has been used as the carrier gas. The flow through the aluminum isopropoxide (AIP) bubbler is about 100 cm³/min and the main argon flow is about 3 l/min. There is a problem with the AIP vapor condensing on the tubing walls between the bubbler and the susceptor. Heater tape has been used to attempt to alleviate this problem but some portions of the path remain cool and continue to condense the vapor. This results in an unpredictable AIP concentration at the substrate region. By placing the susceptor closer to the inlet of the reactor tube, less condensation loss occurs. However, if dₛ (see Fig. 6) becomes too small, the film thickness uniformity suffers. The thickness uniformity has been inferred by observing the interference color distribution of the Al₂O₃ layers deposited upon polished 1 cm² n-Si substrates. There is a considerable variation over the substrate area, depending upon the location of the substrate on the susceptor, the susceptor surface angle (θₛ in Fig. 6), the gas flow rates, and the temperature. The thickness was characterized by etching holes in the Al₂O₃ layer with a buffered HF etch and scanning the surface with a stylus surface profiler (Tencor Alpha-Step). Typical one hour growths at 350°C yield an oxide thickness of approximately 3000 Å (50 Å/min).
Figure 6. System for pyrolytically depositing Al$_2$O$_3$. 
The CVD-deposited layers also exhibited a large number of pinhole defects. This again prevented achieving good MIS devices over most of the substrate surface area. One non-leaky silicon MIS capacitor exhibited a very sluggish C-V hysteresis loop, requiring several minutes to achieve equilibrium after small incremental changes in gate voltage. It is assumed that the pinhole defects are due to particulate contamination of the substrate surface during deposition. The density of these defects, as observed with an optical microscope, varies greatly from one deposition run to another. There is a considerable deposition of a white powdery material (assumed to be Al$_x$O$_3$) on the reaction tube in the vicinity of the susceptor and downstream from it. This material may influence the integrity of the deposited dielectric layer.

Once relatively pinhole-free layers can be achieved, then dielectric layers will be deposited on GaAs, InP and InGaAs for the purpose of studying the C-V behavior. This will require semiconductor layers with carrier concentrations in the 10$^{16}$ cm$^{-3}$ range. It is also planned to incorporate some form of in situ etching of the substrate surface oxides utilizing HCl vapor and a hydrogen ambient, as suggested in Refs. 11 and 12.
REFERENCES


APPENDIX A

METHODS OF DEPOSITING INSULATING FILMS
ON III-V SEMICONDUCTORS FOR DEVICE APPLICATIONS

Excerpts from a M.S.E.E. Thesis by
Mr. Anthony Jackson
Department of Electrical Engineering
North Carolina A&T State University
Greensboro, NC 27411
1983
METHODS OF DEPOSITING INSULATING FILMS
ON III-V SEMICONDUCTORS FOR DEVICE APPLICATIONS

By Anthony Jackson
(Dr. W. J. Collis, Advisor)

Present high speed digital processing requirement projections demand signal processing of frequencies in excess of a few Giga-Hz or more, which seems to surpass that which is achievable on silicon devices. Thus III-V compound semiconductors with their high electron mobility, low impurity diffusivity and large high field velocity have attracted considerable attention as candidates for future electronic devices used in memory, logic, microwave, etc., applications.

In this thesis, methods of depositing insulating films on GaAs and InGaAs substrates are investigated. Silicon substrates were also used for comparative purposes. The methods employed and the insulators used were: sputtering of silicon nitride (Si$_3$N$_4$), electron beam evaporation of aluminum oxide (Al$_2$O$_3$), and wet chemical anodization of native oxides. Aluminum electrodes were evaporated onto the surface of the insulators to form MIS capacitors. High frequency capacitance-voltage (C-V) measurement were used to characterize the electrical properties of the insulators.

Also, the development and initial testing of a system for a pyrolytic deposition of Al$_2$O$_3$ was performed.
METHODS OF DEPOSITING INSULATING FILMS ON III-V SEMICONDUCTORS FOR DEVICE APPLICATIONS

A Thesis
Presented in Partial Fulfillment of the Requirements for the

DEGREE OF MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

NORTH CAROLINA AGRICULTURAL AND TECHNICAL STATE UNIVERSITY

By
ANTHONY JACKSON

1983
METHODS OF DEPOSITING INSULATING FILMS ON III-V SEMICONDUCTORS FOR DEVICE APPLICATIONS

By

Anthony Jackson

A thesis submitted to the Graduate Faculty of the North Carolina Agricultural and Technical State University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

Greensboro
1983

Approved by:

[Signatures]

Advisor
Chairperson of the Department
Dean of the Graduate School
# Table of Contents

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Introduction</td>
<td>1</td>
</tr>
<tr>
<td>II</td>
<td>Review of Literature</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>Basic MIS Structure Theory</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Effect of Interface States on Ideal MIS Structure</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Interface Trapped Charges</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Methods of Insulating Film Formation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Present State Technology</td>
<td></td>
</tr>
<tr>
<td>III</td>
<td>Experimental Procedure</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>Silicon Nitride (Si$_3$N$_4$) Deposition</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sample Preparation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Aluminum Oxide (Al$_2$O$_3$) Deposition</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sample Preparation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Anodic Oxidation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sample Preparation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MIS Structures</td>
<td></td>
</tr>
<tr>
<td></td>
<td>System for Pyrolytic Deposition of Al$_2$O$_3$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gold Electroplating</td>
<td></td>
</tr>
<tr>
<td>IV</td>
<td>Results and Discussion</td>
<td>52</td>
</tr>
<tr>
<td>V</td>
<td>Conclusions and Recommendations</td>
<td>63</td>
</tr>
</tbody>
</table>

## Appendices

<table>
<thead>
<tr>
<th>Appendix</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Organic Cleaning and Etching</td>
<td>65</td>
</tr>
<tr>
<td>B</td>
<td>High-Frequency Capacitance Measurements</td>
<td>67</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>70</td>
</tr>
</tbody>
</table>
CHAPTER III
EXPERIMENTAL PROCEDURE

To keep the density of interface states low it is important to prepare the insulating film at a low temperature because of the volatility of some elements in III-V semiconductors. An inert atmosphere is also beneficial to protect the surface from any undesirable reactions. In this chapter we discuss silicon nitride ($\text{Si}_3\text{N}_4$) films deposited by reactive and non-reactive ion beam sputtering, aluminum oxide ($\text{Al}_2\text{O}_3$) films by electron beam evaporation, native oxide films by anodic oxidation, and the development of a system for the deposition of $\text{Al}_2\text{O}_3$ by a pyrolytic deposition process.

Silicon Nitride ($\text{Si}_3\text{N}_4$) Deposition

Deposition of $\text{Si}_3\text{N}_4$ layers was accomplished by low energy ion beam sputtering using a 7.5 cm diameter silicon nitride target (99.9% pure) and a 5 cm diameter beam of argon ions neutralized with electrons from a hot wire filament. The silicon nitride target was pre-sputtered with the substrated covered by a shutter. This step cleans the target surface in order to minimize the impurities in the deposited insulator film. The resulting $\text{Si}_3\text{N}_4$ films were formed on substrates held at room temperature. Some details of the ion beam sputtering unit are described below.
A schematic diagram of the ion beam sputtering unit is shown in Figure 3.1. Ions are produced in the discharge chamber when electrons accelerated from a hot cathode collide with neutral atoms of the gas in use and establish the basic plasma. This plasma is confined within the volume enclosed by the cylindrical anode, the rear cathode filament and the front cathode grid. The positive ions are accelerated out of the gun by applying a voltage that biases the plasma positively with respect to the grounded vacuum chamber. To enhance the ionization process, a weak magnetic field is established with longitudinal flux lines. The ionized beam after emerging from the gun passes the neutralizing filament. This entrains electrons with the beam to the extent necessary for charge neutrality.

The beam energy can be varied by changing the internal voltages. The beam intensity (current density) can be varied by adjusting the cathode current and the magnetic field. The typical ion beam current density used in this investigation was 1.5 mA/cm² at a beam energy of 1000 eV. Prior to sputtering, the sputter chamber was evacuated to about 3 x 10⁻⁶ Torr using a CTI cryopump. To enhance the deposition of the silicon nitride, high purity (99.99% pure) nitrogen gas was introduced into the chamber through a needle valve. The sputter deposition rate varied from 27.27 Å/min to 33.75 Å/min depending on the gas pressure in the sputtering chamber.
Figure 3.1. A schematic diagram of the ion beam sputtering system.

Figure 3.2. Electron beam evaporation system.
Sample Preparation

The semiconductor samples used in this investigation were n-type Si, GaAs, and epitaxially grown InGaAs on InP. Ohmic contacts to the GaAs and InGaAs were formed by sputtering Au-Ge and an overlay of Pd; except in one case of a n-GaAs sample where the overlay was Ni. Sputtering of the ohmic contact material was chosen over evaporation because it was more economical in the use of the precious metals. This was true for all samples except the one with the Ni overlay, where the ohmic contact was evaporated. These contacts were alloyed at 450°C for one minute in flowing hydrogen before insulator deposition. The current voltage (I-V) characteristics of these contacts appeared to be linear, although no measurement of the contact resistance was performed. The usual cleaning and/or etching steps, as described in Appendix A, were used before any process where an unintentional oxide layer or grease could cause undesirable contamination of the samples.

The thickness of the insulating layer was obtained by measuring the thickness of a step on a glass slide which was formed during insulator deposition with a Tencor surface profiler.

Aluminum Oxide (Al$_2$O$_3$) Deposition

The deposition of aluminum oxide films was accomplished by electron beam evaporation of a sapphire oule. A photograph of the electron beam evaporation system used in our laboratory is shown in Figure 3.2. Before
evaporation, the pressure in the chamber was about $5 \times 10^{-7}$ Torr. The deposition rate was $5 - 10$ Å/sec, and the substrates were held at room temperature.

**Sample Preparation**

Again, all samples prepared using this aluminum oxide insulator were n-type. Si, GaAs, and InGaAs were used as the substrate materials. Ohmic contacts (Au-Ge/Pd) were applied and alloyed as previously described for the silicon nitride samples. The samples were cleaned in organic solvents before evaporation.

**Anodic Oxidation**

This process was initially employed as an attempt to seal pinholes in a sample that had a leaky Si$_3$N$_4$ layer. The experimental setup employed for the anodization of GaAs is kept simple, because the aim is the development of a reliable, easily reproducible technique. The setup is shown in Figure 3.3. Pyrex glassware and a cathode of a platinum plate (2.5 x 5.0 cm) were used. The samples were attached to a pair of tweezers, which were also used to make electrical contact to the back surfaces of the samples. It was necessary to use a black wax to cover the back surface and edges that would be submerged in the electrolyte, and to isolate the region where the tweezers are in contact with the front surface. The generally small sample (Figure 3.3 is not to scale, the sample surface area being 15 mm$^2$) was submerged into the electrolyte as far as possible such that the electrolyte did not rise above the wax. For illumination of the samples during anodization, a
Figure 3.3. Experimental setup for anodic oxidation.
collimated light source was used which was a microscope illuminator lamp with a tungsten bulb.

The circuit for anodization is a simple one in which the electrodes are connected to a variable d-c constant current source. External circuit conditions are specified by the short-circuit current density $j_s = I_s/A_s$ where $I_s$ is the source current and $A_s$ is the area to be anodized. Anodization was performed for a fixed time of 15 minutes and fixed circuit condition of $j_s = 1\text{mA/cm}^2$ and $V_{\text{max}} = 100 \text{ Volts}$.

The electrolyte was a 3\% aqueous solution of tartaric acid, which was buffered by $\text{NH}_4\text{OH}$ to obtain a pH value of approximately 6.2, and ethylene glycol. The mixing ratio of the electrolyte was 1:2 by volume, acid solution (or water) to glycol.

**Sample Preparation**

There were two samples used in anodic oxide process, both were n-type GaAs and had backside ohmic contacts as previously described. One of the samples was a cleaved piece of n-GaAs that had previously been subjected to the silicon nitride deposition process. I-V measurements and observation under the microscope proved the insulator was leaky and had a high density of pinholes. Thus, the Az dots were removed, as described in Appendix A, and the sample was anodized in an attempt to produce a more stable insulator for a MIS device. A sketch of a sample, with black wax on front and back, ready for anodization is shown in Figure 3.4.
Figure 3.4. Sample with wax masking, ready for anodic oxidation.

(a) Front surface.  (b) Back surface.
MIS Structures

In order to understand the bulk and interfacial properties of the insulating films, MIS capacitance structures were fabricated on all the samples. Circular aluminum electrodes, with an area of $5.88 \times 10^{-4} \text{ cm}^2$ and approximately 3000 Å thick, were evaporated through a metal mask onto the insulators. The samples were placed onto a probe station where the back contact was the flat metal base plate. The adjustable metal probe could be brought into contact with any aluminum dot by means of a manipulator. Current-voltage (I-V) measurements were made using a Tektronix 576 curve tracer. The I-V characteristics were primarily used to determine if ohmic contacts were indeed "ohmic" and if the deposited insulators were leaky. If the I-V characteristics showed bad ohmic contacts or leaky insulators, capacitance-voltage measurements were not performed on the sample. This was the case in many of our samples. Capacitance-voltage (C-V) measurements at a frequency of 1 MHz were obtained using a MDC Automatic Doping Profiler in the C-V mode. Appendix B gives an overview of the high frequency C-V measurements. All measurements were performed at room temperature.

The MIS structures of which stable C-V curves were obtained were annealed at 350°C for 1 hour in flowing N₂. These devices were then polarized by applying a dc voltage between the metal and the substrate at an elevated temperature of 125°C for a period of 1 hour. The latter process was intended to determine the effect of mobile ion transport in the insulator 34.
The system for the pyrolytic deposition of Al₂O₃ was designed. The apparatus was similar to that used by other investigators. A diagram of the system is shown in Figure 3.5. A quartz tube, with a graphite susceptor as the substrate holder, will serve as the deposition chamber. Initially, in order to achieve the estimated 350°C deposition temperature, a 600 watt quartz lamp Sun Gun was used to heat the susceptor. The temperature was measured with a chromel-alumel thermocouple, with the junction inside the susceptor. Alumina lapping compound was used in the thermocouple well to insure good thermal contact between the junction and the susceptor. In achieving the desired temperature the quartz lamp was near 100% of its intensity. Therefore, a pair of 500 watt quartz filament lamps, from the electron beam evaporation system, were utilized to heat the susceptor. A Research Inc., temperature controller was used to control the susceptor temperature. The experimental circuit for the controller is shown in Figure 3.6. Another chromel-alumel thermocouple was inserted into the susceptor to monitor the temperature versus time response of the heated susceptor on a chart recorder. Aluminum isopropoxide (melting point 118°C), maintained in a pyrex bubbler at a temperature of 125°C, will provide the source vapor. It will be transported to the reaction zone with a hydrogen carrier gas where it will pyrolyze to form Al₂O₃.
Figure 3.5. Schematic of apparatus to be used for pyrolytic deposition of $\text{Al}_2\text{O}_3$ films: A - dry $\text{H}_2$; B - dry $\text{N}_2$ or $\text{O}_2$; C - flowmeters; D - constant temperature bath; E - $\text{Al}(\text{OC}_3\text{H}_7)_3$; F - deposition chamber; G - quartz lamps; H - susceptor; I - oil bubbler; J - exhaust.

Figure 3.6. Circuit diagram for temperature controller experiment.
Gold Electroplating

Gold (Au) plating was performed on one sample of n-GaAs which had previously been subjected to the Si$_3$N$_4$ deposition process. The sample, observed under a microscope, appeared to have a high density of pinholes in the insulator. Therefore it was believed that Au plating could be used to decorate the pinholes.

The experimental setup for the Au plating is identical to that of the anodic oxidation process, except the electrolyte is liquid Au and the cathode is a stainless steel wire.

The sample preparation for Au-plating is identical to that of anodic oxidation.
CHAPTER IV
RESULTS AND DISCUSSION

The silicon nitride deposition resulted in layers from 1300Å to 1200Å thick. The film color varied from metallic brown to light tan for the thinnest layer. A color comparison is given in Table IV-1 for silicon nitride and silicon dioxide films as a function of film thickness.

The I-V characteristics of the n-GaAs MIS structures indicated conducting Si$_3$N$_4$ layers. A typical I-V curve is shown in Figure 4.1. In contrast, the I-V characteristics of the n-Si MIS structures exhibited good insulating layers. These dielectric layers exhibited a breakdown electric field of $6 \times 10^6$ V/cm, the calculated dielectric constant was 16.14 using an insulator capacitance measurement of 42 pf. However, the C-V characteristic did not exhibit any variation in capacitance over the bias range (+20 V to -20 V). This Si sample was annealed at 350°C for one hour in flowing N$_2$, but this did not seem to improve its C-V behavior.

The attempt to decorate the pinholes of one of the leaky Si$_3$N$_4$ samples was successful. Figure 4.2 shows a photomicrograph of one of the GaAs MIS structures after two minutes of gold electroplating. No further testing was performed on this sample because of the highly visible pinhole defects still present on the surface. Another GaAs sample with a leaky Si$_3$N$_4$ layer was anodically oxidized in an attempt to seal the pinholes observed on its surface. Again this process was successful, however, it seems to damage the Si$_3$N$_4$ layer even more.
<table>
<thead>
<tr>
<th>Order</th>
<th>Color</th>
<th>$\text{SiO}_2$ Thickness Range $^a$</th>
<th>$\text{Si}_3\text{N}_4$ Thickness Range $^a$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$(\mu m)$</td>
<td>$(\mu m)$</td>
</tr>
<tr>
<td></td>
<td>Silicon</td>
<td>0.0-0.027</td>
<td>0.0-0.020</td>
</tr>
<tr>
<td></td>
<td>Brown</td>
<td>0.027-0.053</td>
<td>0.020-0.040</td>
</tr>
<tr>
<td></td>
<td>Golden Brown</td>
<td>0.053-0.073</td>
<td>0.040-0.055</td>
</tr>
<tr>
<td></td>
<td>Red</td>
<td>0.073-0.097</td>
<td>0.055-0.073</td>
</tr>
<tr>
<td></td>
<td>Deep Blue</td>
<td>0.097-0.110</td>
<td>0.073-0.077</td>
</tr>
<tr>
<td>First</td>
<td>Blue</td>
<td>0.10-0.12</td>
<td>0.077-0.093</td>
</tr>
<tr>
<td></td>
<td>Pale Blue</td>
<td>0.12-0.13</td>
<td>0.093-0.10</td>
</tr>
<tr>
<td></td>
<td>Very Pale Blue</td>
<td>0.13-0.15</td>
<td>0.10-0.11</td>
</tr>
<tr>
<td></td>
<td>Silicon</td>
<td>0.15-0.16</td>
<td>0.11-0.12</td>
</tr>
<tr>
<td></td>
<td>Light Yellow</td>
<td>0.16-0.17</td>
<td>0.12-0.13</td>
</tr>
<tr>
<td></td>
<td>Yellow</td>
<td>0.17-0.20</td>
<td>0.13-0.15</td>
</tr>
<tr>
<td></td>
<td>Orange-Red</td>
<td>0.20-0.24</td>
<td>0.15-0.18</td>
</tr>
<tr>
<td>First</td>
<td>Red</td>
<td>0.24-0.25</td>
<td>0.18-0.19</td>
</tr>
<tr>
<td></td>
<td>Dark Red</td>
<td>0.25-0.28</td>
<td>0.19-0.21</td>
</tr>
<tr>
<td>Second</td>
<td>Blue</td>
<td>0.28-0.31</td>
<td>0.21-0.23</td>
</tr>
<tr>
<td></td>
<td>Blue-Green</td>
<td>0.31-0.33</td>
<td>0.23-0.25</td>
</tr>
<tr>
<td></td>
<td>Light Green</td>
<td>0.33-0.37</td>
<td>0.25-0.28</td>
</tr>
<tr>
<td></td>
<td>Orange-Yellow</td>
<td>0.37-0.40</td>
<td>0.28-0.30</td>
</tr>
<tr>
<td>Second</td>
<td>Red</td>
<td>0.40-0.44</td>
<td>0.30-0.33</td>
</tr>
</tbody>
</table>

$^a n(\text{Si}_3\text{N}_4)/n(\text{SiO}_2) = 1.97/1.48 = 1.33$
Figure 4.1. Typical I-V characteristic of GaAs/Si$_3$N$_4$ MIS structures.

Figure 4.2. Photomicrograph of a GaAs/Si$_3$N$_4$ MIS structure after two minutes of gold electroplating.
The separate anodic oxidation of a GaAs sample also resulted in a leaky insulator as proven by I-V measurements. One peculiarity observed in the I-V curve of the anodic oxide layer was that it resembled that of an ideal p-n junction or Schottky barrier diode (Figure 4.3).

The aluminum oxide deposition resulted in layers from 1100Å to 1600Å thick. This insulator seemed to fair better than the two previously described insulators, especially on the silicon substrates. However, on both GaAs and InGaAs the insulator again proved leaky and we were unable to obtain any conclusive C-V measurements, except in one case where a GaAs/Al₂O₃ MIS structure was stable. However, this device's high frequency curve showed only slight variation over the bias range (Figure 4.4). Figures 4.5a and 4.5b are examples of the high frequency C-V curves of one of the Si-Al₂O₃ MIS structures before and after annealing for one hour at 350°C in flowing N₂, respectively. These curves exhibit a large hysteresis before treatment.

The hysteresis effect is due to electronic exchange by tunnelling between the semiconductor and the traps in the insulator. The density of these states can be estimated by using the expression:

\[ N_s = \frac{1}{q} \frac{C_i}{(V_{FB1} - V_{FB2})} \]  

where \( V_{FB1} \) and \( V_{FB2} \) are the flat-band voltages corresponding to positive and negative ramp rates, respectively. In order to determine the flat-band voltages, preliminary calculation of the flat band capacitance was carried out using a method described in Reference 17.
Figure 4.3. I-V characteristic of a GaAs/anodic oxide MIS structure with Al gate electrode.
Figure 4.5. High frequency C-V curves of MIS Si/Al₂O₃ structure (a) before annealing and (b) after annealing (1 hour, 350°C, N₂).
The flat band capacitance was 65 pf and 73 pf for MIS devices before and after annealing respectively.

Before annealing, the density $N_s$ of states is typically about $5.74 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. On annealing this value decreases to approximately $2.82 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, which is very high for MIS devices. Estimated values of state density before and after annealing for three MIS devices are listed in Table IV-2.

The results obtained from the polarization experiment seem to indicate that there is not much mobile ionic charge present in these insulating layers. As can be seen in Figure 4.5, there is not much drift of the C-V curve under negative or positive bias condition. These curves are compared to the original C-V curve Figure 4.5b. This result is expected since the $\text{Al}_2\text{O}_3$ insulator yields little to the penetration of alkali ions.

The design of the system for the pyrolytic deposition of $\text{Al}_2\text{O}_3$ has been completed. The two 500 watt quartz filament lamps provide adequate reserve intensity to easily achieve susceptor temperatures in the 300 - 400°C range. Since the temperature must be maintained over a period of time, the choice helped preserve the lifetime of the lamps. Table IV-3 shows the results of Research Inc. temperature controller experiment. These results proved that the control system is adequate for maintaining a constant temperature in the susceptor.
<table>
<thead>
<tr>
<th>MIS DEVICE NO.</th>
<th>STATE DENSITY $N_s \text{ cm}^{-2} \text{eV}^{-1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BEFORE ANNEALING</td>
</tr>
<tr>
<td>SiAO - 2</td>
<td>$5.99 \times 10^{12}$</td>
</tr>
<tr>
<td>SiAO - 3</td>
<td>$5.84 \times 10^{12}$</td>
</tr>
<tr>
<td>SiAO - 4</td>
<td>$5.40 \times 10^{12}$</td>
</tr>
</tbody>
</table>
Figure 4.6. High frequency C-V curves of MIS Si/Al2O3 structure after (a) +5 volts and (b) -5 volts polarization.
<table>
<thead>
<tr>
<th>Temperature Controller Set point</th>
<th>Approximate Temperature from Controller Table (°C)</th>
<th>Approximate Time for Stabilization (sec.)</th>
<th>Thermocouple Voltage (mV)</th>
<th>Approximate Temperature from T/C Table (°C)</th>
<th>Input Power (watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>384</td>
<td>390</td>
<td>start</td>
<td>16.47</td>
<td>402</td>
<td>---</td>
</tr>
<tr>
<td>368</td>
<td>392</td>
<td>350</td>
<td>-</td>
<td>-</td>
<td>444</td>
</tr>
<tr>
<td>384</td>
<td>390</td>
<td>390</td>
<td>16.46</td>
<td>402</td>
<td>442</td>
</tr>
<tr>
<td>375</td>
<td>381</td>
<td>270</td>
<td>16.10</td>
<td>393</td>
<td>422</td>
</tr>
<tr>
<td>373</td>
<td>379</td>
<td>120</td>
<td>16.00</td>
<td>391</td>
<td>420</td>
</tr>
<tr>
<td>330</td>
<td>338</td>
<td>New Range</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>320</td>
<td>328</td>
<td>295</td>
<td>13.84</td>
<td>339</td>
<td>318</td>
</tr>
<tr>
<td>330</td>
<td>338</td>
<td>240</td>
<td>14.25</td>
<td>349</td>
<td>328</td>
</tr>
<tr>
<td>334</td>
<td>342</td>
<td>280</td>
<td>14.39</td>
<td>352</td>
<td>330</td>
</tr>
<tr>
<td>332</td>
<td>340</td>
<td>230</td>
<td>14.32</td>
<td>351</td>
<td>328</td>
</tr>
</tbody>
</table>
CHAPTER V
CONCLUSIONS AND RECOMMENDATIONS

Methods of depositing insulating films on III-V semiconductors have been investigated. A review of existing literature concludes that InGaAs is the material for future MIS devices. In our experiments the rather expensive InGaAs material was not used in the Si$_3$N$_4$ deposition process because of the poor quality of the insulator on the Si and GaAs substrates.

The sputtering of Si$_3$N$_4$ resulted in bad surface properties of the insulator in the form of pinhole defects. These pinholes lead to conduction through the insulating layer when the metal gate is applied. These pinholes were decorated with a gold electroplating technique. Because of the poor insulating properties of the Si$_3$N$_4$ layer, no difference could be observed between insulators deposited with N$_2$ present during deposition and those without N$_2$ present.

The evaporation of Al$_2$O$_3$ was successful on Si substrates. The insulator was leaky on both GaAs and InGaAs substrates, or exhibited only a slight variation in capacitance over the bias range. Continued investigation into the surface properties of GaAs and InGaAs is necessary to insure a leakage-free insulator deposition on these materials. The Si/Al$_2$O$_3$ MIS structure's C-V curves exhibited very large hysteresis before heat treatment. This hysteresis is probably due to a high density of trap states in the insulator. In all cases, annealing in nitrogen
reduces these states, and hence hysteresis, but their density is still too high for MIS devices. These trap states are probably due to a native oxide layer present before insulator deposition. It is suggested that work toward the elimination of this layer be investigated. A bromine-methanol etchant in place of the Caro etch is suggested as a beginning for the III-V semiconductors.

Since the system has been designed and initial tests are completed, MIS devices with pyrolytically deposited Al₂O₃ insulators can be fabricated. This system can also be expanded to utilize the HC₂ vapor etching technique to eliminate the native oxide layer, therefore reducing the interface states.
APPENDIX A

ORGANIC CLEANING AND ETCHING PROCEDURES
APPENDIX A

ORGANIC CLEANING AND ETCHING PROCEDURES

The general GaAs sample cleaning and etching steps are outlined as follows:

1) Heat in trichloroethylene (TCE); using a Teflon beaker for approximately 5 minutes.
2) Heat in acetone for 5 minutes.
3) Heat in methanol until ready for use.
*4) Caro etch for 1 minute \((2m\alpha \ H_2O_2/H_2O: 5m\alpha \ H_2SO_4)\).
*5) Rinse in deionized water, soak for 20 min. (grows oxide).
*6) Etch to remove oxide \((50\% \ HCl: 50\% \ H_2O)\).
*7) Store in methanol until ready for use.

* Denotes steps employed before evaporation.

Removal of aluminum electrodes (prior to anodic oxidation):
1) Cleaning steps 1-3.
2) Etch Al in hydrochloric acid \((HCl)\) until dots are removed.
3) Rinse in methanol
4) Oven dry at 100°C for 20 minutes.
APPENDIX B
HIGH-FREQUENCY CAPACITANCE MEASUREMENTS [15]
APPENDIX B

HIGH-FREQUENCY CAPACITANCE MEASUREMENTS [15]

Figure B.1 shows the circuit used in measuring the high-frequency capacitance as a function of applied bias (C-V) of an MIS device. The capacitance is measured using a modified Boonton model 72-B solid state capacitance meter. For capacitance measurements, the test-signal frequency is 1MHz and its level is fixed at 15mV rms. This test voltage is low enough so that any error introduced into the MIS C-V characteristics may be neglected. There is a series of capacitance ranges, the smallest being 0-1pF full scale and the largest 0-3000 pF full scale, which is sufficient to cover most MIS structures.

To plot the C-V characteristics of the sample the probe station is connected to the capacitance meter using the plug-in with post connectors. The capacitance meter should be zeroed with the probe just out of contact with the sample. With the probe in contact with the sample and the recorder pen up, the bias voltage is increased to the desired maximum. After the desired maximum is reached, the recorder pen is placed down and the Reset-Sweep switch is moved to the Sweep position. The C-V data will then be plotted automatically.

Note that the capacitance of an excessively leaky sample, or one in avalanche breakdown cannot be plotted.
Figure B.1. Circuit diagram for making high-frequency capacitance-voltage measurements.
REFERENCES


