An integrating IR detector array for imaging is provided in a hybrid circuit with InSb mesa diodes (1, 2, . . . 128) in a linear array, a single J-FET preamplifier (30) for readout, and a silicon integrated circuit multiplexer (34). A reset switch (32) is also provided to reset (charge) all of the diodes to a predetermined level at the end of each line scan. Thin film conductors in a fan-out pattern deposited on an Al2O3 substrate (42) connect the diodes to the multiplexer, and thick film conductors also connect the reset switch and preamplifier to the multiplexer. Two-phase clock pulses (φ1 and φ2) are applied with a logic return signal to the multiplexer through a triax comprised of three thin film conductors deposited one over the other with silicate glass insulation between layers. A lens (14) focuses a scanned image onto the diode array for horizontal read out one line at a time while a scanning mirror (22) provides vertical scan. A cooler (20) maintains the hybrid circuit at a very low (liquid nitrogen) temperature.
INTEGRATING IR DETECTOR IMAGING SYSTEMS

ORIGIN OF THE INVENTION

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, Public Law 85-568 (72 Stat. 435; 42 USC 2457).

BACKGROUND OF THE INVENTION

This invention relates to an array of infrared (IR) detectors for imaging, and more particularly to a compact multiplexed array of integrating IR detectors for imaging.

Missions like Galileo to Jupiter in 1985 have created a need for a compact multiplexed array of integrating detectors for a near infrared imaging instrument. The object is to provide an array of very high quality detectors in a focal plane assembly with a mesa photovoltaic indium antimonide (InSb) diode mounted on a hybrid circuit board 18. These InSb diodes are produced using mesa fabrication technology so that it is possible to accomplish photocurrent charge integration right on the diode junction capacitance. The circuit board is thermally connected to a cooler 20. The circuit board 18 (shown in FIG. 5) includes an FET multiplexer for reading the integrated charges in sequence to produce a horizontal line of image at a time as a mirror 22 scans vertically. To successfully integrate charge on the diode junction capacitance, the multiplexer must have a leakage resistance in its off state much higher than the detector diode leakage resistance. Images produced by this system can be reproduced through a cathode ray tube (CRT) 24.

When cooled to liquid nitrogen temperatures, the multiplexer has a leakage resistance greater than 10^12 ohms. The multiplexer operates normally at liquid nitrogen temperatures (78° K.). Because the InSb diodes typically have a junction resistance of about 10^10 ohms at liquid nitrogen temperatures, the multiplexer with its 10^12 ohm “off” resistance allows integration times approaching one second with low background conditions (less than 10^10 photons/sec/cm^2). Thus, the key to obtaining useful charge storage in InSb diodes is low leakage paths on the diode surface and good diode characteristics (sharp breakdown knee and high reverse breakdown voltage). InSb mesa diodes made by Cincinnati Electronics display both of these characteristics.

FIG. 2 illustrates a portion of an array of 128 mesa diodes formed on a substrate 16a with channels 16b to a depth of about 10 microns to leave an array of 8 X 16c, each with a bonding pad 16d that is 3 X 5 mils connected by narrow strips 16e, as shown in FIG. 3. The substrate 16a is simply the base InSb material.

Useful charge integration has been achieved in high quality photovoltaic InSb diodes when combined with a FET multiplexing circuit. An exemplary detector assembly with a linear array of 128 InSb diodes coupled to a FET multiplexer will now be described with reference to FIGS. 4 and 5. A J-FET preamplifier 36, MOS FET reset switch 32, silicon integrated circuit multiplexer 34, and the InSb array 16 are contained on a thick film hybrid microcircuit board 18 of Al_{2}O_{3}. The board dimensions are 1.75" x 1.0" x 0.015". A low noise preamplifier topology is utilized, as shown in FIG. 5. It capitalizes on the low video line (44) capacitance inherent with hybrid fabrication techniques.

For convenience, the components just identified with reference to the circuit diagram of FIG. 4 are identified by the same reference numerals in FIG. 5. All of these components are placed in a standard 22-pin integrated circuit package 40. A thin film fan-out 42 connects the anodes of the diodes of the array 16 to the multiplexer.
34. All of these diodes are connected through their substrate to a pin for back bias voltage (+V). A video line 44 connects the output of the multiplexer 34 to the gate of the J-FET preamplifier 30. The source of that preamplifier is connected to one of the 22 package pins, while the drain is connected to a source of bias voltage $V_{ce}$ through another pin. The video line 44 is also connected to the drain of the MOS FET reset switch 32. The source of that MOS FET is connected to the voltage return for the detector bias via package pins. A video reset signal applied to the gate of the MOS FET 32 resets (charges) all of the diodes 1 through 128 to a predetermined level after each pixel is read out from individual InSb diodes through MOS FET gates 341, 342, . . . 34128.

To operate the multiplexer $\phi_1$ and $\phi_2$ clock pulses step a bit 1 entered into a shaft register 34A by a START signal. The three lines for the logic return and two clock signals are applied through package pins connected to the silicon multiplexer by a triax comprised of a thin film conductor coated with an insulating material (silicate glass) for one phase clock. A thin film conductor directly over the insulated first conductor, also coated with the same insulting material, and a third thin film conductor directly over the other two, as shown in FIG. 5c which is a cross section of the triax along a line A—A in FIG. 5. This triax on the thick film substrate provides a faraday shield to reduce coupling switching transients into the video output. The topology features low power dissipation (less than 5 mW for up to 256 diodes), a small number of electrical connections (fourteen) that is not dependent on the number of elements, and compact package size.

Photovoltaic InSb diodes using mesa fabrication technology, have emerged as the only developed IR photodetectors in the 0.6 to 5.4 micron region that is not plagued with either gold migration problems (lifetime) or uncontrollable surface leakage (reproducibility). Taken in this light, InSb is the only narrow bandgap detector material that can be considered seriously for the near-IR advanced focal plane assemblies being contemplated by this invention.

InSb detectors fabricated with true mesa technology have reached a state of development where it is possible to accomplish photocurrent charge integration right on the diode junction capacitance. This accomplishment is now possible because of the development of devices with both high reverse breakdown voltages (2-3V) and nonexistenw voltage dependent surface leakage.

The ability to provide charge integration in the photodetector itself is of great practical value. Since the photocurrent is integrated right where it is produced, the inevitable loss associated with charge transfer to another location for integration is eliminated. Another virtue of the process is the attainment of a large ($=1 \times 10^7$ electron) charge storage/integration capability for each pixel. This characteristic is of great importance for IR applications because of the large dynamic range inherent in planetary and astrophysical IR sources.

For large linear arrays to be practical (such as 256 or 512 diodes), a readout technology is required to interface the detector array to the readout system that does not require a preamp for each pixel. It is desirable to do this with a small number of connections, so as to minimize thermal input to the array. To accomplish this task, the present invention employs a well developed commercial silicon multiplexer manufactured by Reti-
means for focusing an IR image onto said diodes, multiplexing means for reading out an integrated IR detected signal, one diode at a time. said multiplexing means being comprised of a silicon integrated circuit having much higher leakage resistance in its off state than the leakage resistance of said InSb mesa diodes, and

amplifying means connected to said multiplexing means.

2. A system as defined in claim 1 wherein said amplifying means is a junction field-effect transistor.

3. A system as defined in claim 2, including a reset means for recharging all of said diodes to a predetermined level after reading out each image line.

4. A system as defined in claim 3 wherein said reset means is comprised of an MOS field-effect transistor.