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HIGH DENSITY

CIRCUIT TECHNOLOGY

PART I

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FORWARD

This report describes a portion of the work performed from July 1980 to March 1982 under Contract NAS8-33448 for the George C. Marshall Space Flight Center, National Aeronautics and Space Administration, Marshall Space Flight Center, Alabama. The technical managers for MSFC were Mr. B. R. Hollis, Jr., Mr. R. F. Dehaye and Mr. J. M. Gould. This report was prepared by the Microelectronics Research Laboratory of the Department of Electrical Engineering, Mississippi State University, under the direction of the principal investigator Dr. Thomas E. Wade. The principal participants in the program were Mrs. Rebecca A. Hamilton, Mr. Phu Hiep Luong and Mrs. Mildred N. Sellars. Typist was Mrs. Jerrie McIngvale.

This final report has been divided into four areas of emphasis, with a separate comprehensive report for each area. These four areas represent the following subject groupings:

PART I. Emphasis is on the realization of very dense metal interconnection for VLSI systems utilizing the lift-off process. Both a survey of lift-off techniques is presented as well as experimental and novel lift-off methods which have been investigated by the author.

PART II. Emphasis here is on multilevel metal interconnection system for VLSI systems utilizing polyimide as the interlayer dielectric material. A complete

characterization of polyimide materials is presented as well as experimental methods accomplished using a double level metal test pattern. A novel double exposure polyimide patterning process is also presented.

PART III. Emphasis is on dry plasma processing including a characterization of and an equipment survey for plasma etching, reactive ion etching, (reactive) ion milling and plasma deposition processes. Also included is an indication of future microelectronic trends, including patterning technology, lithography, materials deposition, packaging, etc.

PART IV. Emphasis here is on an evaluation of dielectric material for use in VLSI metal interconnection systems. A number of dielectric material types (or combination of materials) are experimentally evaluated using a second test pattern. Recommendations are presented based on these findings.

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INTEGRATED CIRCUIT INTERCONNECTION LIFT-OFF TECHNIQUES

I. INTRODUCTION

The increasing packing density of integrated circuits requires small conductor linewidths and small spaces between conductors. Aluminum and aluminum-based metals (Al alloys) are the most popular material for interconnection of large scale integrated circuits (LSI). These metals will continue to be used in very large scale integrated systems (VLSI) even though additional conducting materials like polysilicon, refractory metals and metal silicides will experience a growing usage in these systems.

The normal procedure for patterning the interconnection material consist of first depositing the interconnect material to be used on the surface of the wafer. A light sensitive material (photoresist) is then deposited and patterned, which in turn acts as a mask in etching the interconnection material. The lift-off process consist of depositing the light-sensitive material (or a substitute) onto the wafer and patterning first in such a manner as to form a stencil for the interconnection material. Then the interconnection layer is deposited and unwanted areas are "lifted-off" by removing the underlying stencil.

The lift-off technique of patterning the interconnection offers a number of advantages over the etching procedure, especially when dealing with small geometries as are encountered in the VLSI technology. The more predominant advantages may be indicated as follows:

i) Photoresist defects: When using the more conventional etching procedure, one relies heavily on the quality of the photoresist (or substitute layer) pattern to act as a mask in etching the underlying interconnection material, either using a wet chemical or dry plasma technique. Very often this photoresist masking layer will have defects in the form of pinholes in it (even for thick photoresist layers). These unintended 'openings' in the photoresist layer result from several causes, the most likely being dust particles or other foreign matter on the wafer surface. When etching the interconnection material, these pinholes allow etching of the interconnect material (and possibly other materials) in undesirable locations. This problem is essentially eliminated with the lift-off technique.

ii) Silicon residue: After delineation of alloy films such as Al/Si or Al/Si/Cu, silicon residues may remain in the field where these metals are etched away [1]. Removal of this silicon residue requires extra processing steps and could have detrimental effects on the remaining wafer surface. Employing the lift-off technique negates this residue and the need to remove it.

iii) Wet chemical etch: This etching procedure results in an isotropic etch. Thus, in etching interconnection material, a lateral etch attack is experienced resulting in the width of the conductors being reduced and the spacing between adjacent conductors being increased as per Figure 1. The undercutting

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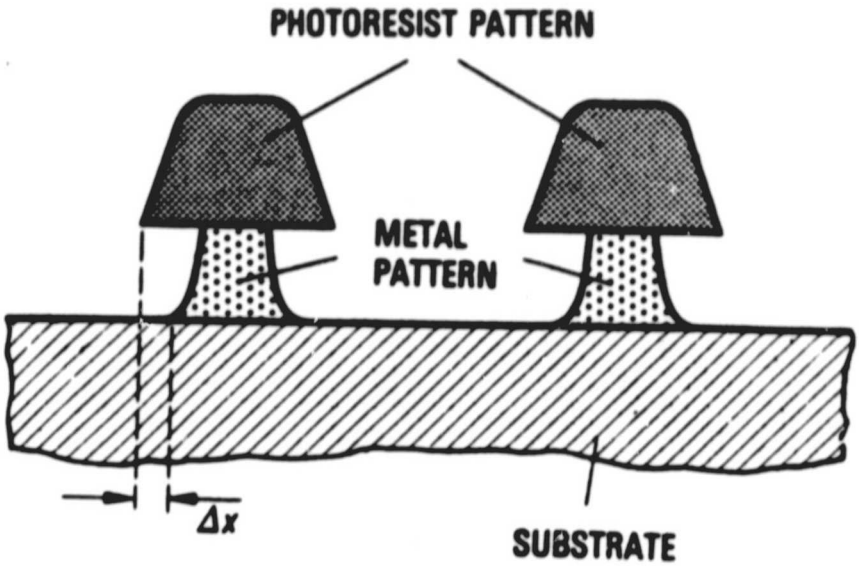

Figure 1. Schematic illustration of a typical cross section of metal conductors after chemical etching. The undercutting at the bottom of the conductor is ΔX.

Δ X per edge (see Figure 1) might be in the order of the conductor thickness. As long as the desired spacing between adjacent conductors is large enough, i.e., larger than about 3 μm for 1 μm conductor thickness and 1 μm minimum photoresist dimension, the undercutting effect can be compensated by proper dimensioning the corresponding geometries on the photomask. However, if spaces of about 1 μm are required between 1 μ thick metal conductors, the compensation procedure fails.

The edge contours of conductors delineated by wet chemical etching are conical [2], the upper portion of the edges being steep or even overhanging. Edge contours of this kind may lead to poor coverage of such edges by subsequently deposited layers such as passivation and metal layers. For VLSI circuitry, as the linewidths decrease to increase packing density, the metal

thickness will have to increase in order to maintain low resistivity per unit length. Especially under these conditions, the conical edge contours of the metal conductors becomes important.

In addition, it should be noted that chemicals used in the wet chemical etching process are very dangerous and costly. If an alternate process can be made safer to execute (alleviating law suits, etc.), less expensive, and render a similar or improved result, it should be seriously considered.

iv) Dry plasma etch: This etching procedure typically results in anisotropic etching. These procedures include plasma etching, reactive ion-etching, reactive ion milling and straight ion beam milling. While the dry etching processes possess the potential for patterning interconnection materials with very fine geometrics, they at present render several undersirable side effects. Generally, the steep, sharp edges of the metallization profile obtained by dry etching results in poor step coverage for subsequently deposited layers [3]. Dry etching processes can induce radiation damage into the VLSI circuitry (very sensitive in MOS gate regions) which must be annealed out when possible [4]. Also at present, the selectivity associated with dry etching processes for metallization layers is quite poor giving rise to severe etching of materials on the wafers which were not intended to be etched. And for some materials (i.e., Ni and Pt [5]) which are candidates for metallization interconnect, there are at present no good dry etching process which can adequately pattern these.

v) Nonconventional materials: Patterning of non-conventional interconnect materials is being pursued today in an attempt to locate a replacement for conductors like polysilicon and Al or Al/Si for VLSI applications. For many of the refractory metals and metal silicides being investigated, lift-off processes are the only reliable technique for delineation, especially in the micron and sub-micron range. Also, composite metal layers often used in bipolar and other VLSI applications like Al/Ti/W can be patterned with a single lift-off.

This technique is also not limited to metals, but can be used for many thin films which are deposited in a vaporous state as long as a compatible masking layer can be found. There are many considerations in developing a lift-off process for a specific application. A lift-off process must be tailored according to the material to be patterned, the required resolution, and other process and device restrictions. Thus, a great number of processes can be developed using lift-off technology.

Because of the above mentioned problem areas associated with delineating interconnection materials using wet chemical and dry plasma etching processes, the lift-off technique discussed in this section offers a very viable alternative for patterning small geometries with minimal undesirable side effects. In the following two sections, a survey of those lift-off techniques as reported in the literature will be presented as well as some experimental results and novel techniques developed at the Mississippi State University Microelectronics Research Laboratory.

II. SURVEY OF LIFT-OFF TECHNIQUES

A large number of different, though related, lift-off techniques have been reported in the literature within the past 10 to 12 years. These have been subdivided into the use of photoresist as a lift-off stencil, the use of an auxiliary layer for improved stencil formation, the formation of a metal stencil, and interspaced throughout, the use of plasma deposition and etching techniques for forming a lift-off stencil.

A. Photoresist as a lift-off stencil:

1. Thick Photoresist Applications

a. The Conventional Lift-Off Method:

The lift-off technique for metal pattern formation is shown schematically in Figure 2. This process was first used by Stelten in 1966 in the fabrication of chromium masks [6]. The key element in this process is to produce a distinct break in the metal film at the point where it leaves the substrate and begins to form a bridge over the photoresist relief pattern. To insure this, it is essential to produce a sharp vertical or slightly overhanging profile in the photoresist and to carry out the metal deposition so that atoms impinge at near normal incidence. In this way, the metal on the sides of the photoresist relief patterns is considerably thinner than the metal film on

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the substrate and the top of the photoresist, and the required removal of unwanted metal is readily effected by swelling the photoresist in an organic solvent.

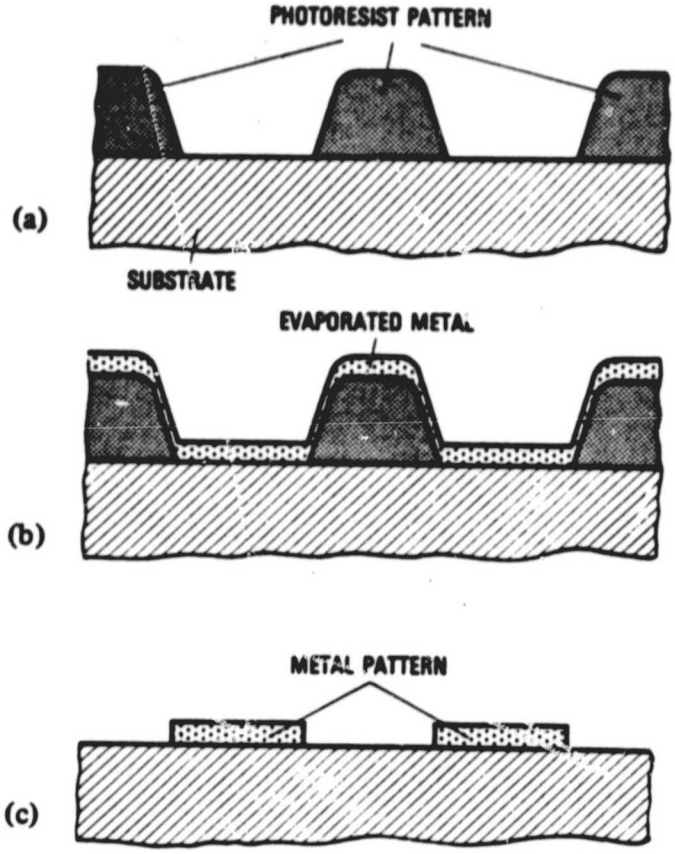

Figure 2. Schematic illustration of metal pattern definition using the original lift-off technique. (a) Photoresist pattern definition. (b) Metal evaporation. (c) Photoresist stripping, thereby lifting off the overlying metal. The spaces between the metal features are equal to the corresponding photoresist linewidths, as measured at the bottom of the photoresist bars.

The character of a photoresist profile depends critically on the exposure conditions, primarily on the avoidance of diffraction effects and to a lesser extent on the exposure time. It is generally believed that contact printing rather than projection exposure renders less diffraction effects [7]. For optimal results, intimate contact must be obtained between the mask and the photoresist at the time of exposure. Also, deposited metal film thickness should not exceed about 1/3 to 1/2 of the photoresist height. It should be noted that in the event defects or areas of residue form in the photoresist layer prior to metal deposition, it can easily be removed and reapplied and patterned without exposing the wafer surface to any type of harsh chemicals. Thus, the lift-off technique allows for mistakes in the process to be rectified whereas the etching technique does not.

Photoresist edges might also be realized with overhanding portions, for instance, due to interference effects during exposure of the photoresist [9] or due to poor adherence of the photoresist to the substrate. However, it is not very attractive to utilize these effects for lift-off metallization because they are difficult to reproduce.

The photoresist is not baked after pattern development because it is not required by the process, and runs the risk of rounding the photoresist profile through plastic flow. For the same reason, the substrates are not heated during deposition of the metal film. The softening point of Shipley AZ1350, for example, is about 130°C so that some preheating or glow discharge cleaning to enhance metal adhesion is permissible. Generally speaking, negative photoresist acts as a poor stencil for lift-off phenomena primarily because of the rounding of the photoresist profile [7].

Although thick photoresist films have many reports of being used successfully in patterning interconnect in LSI and VLSI circuitry, one of the most unique applications reported involved the use of thick narrow photoresist "walls" to shadow off radiation damaging ions during reactive plasma ion etching of MOS gate regions, and then used to lift-off undesired metals in realizing the basic MOS transistor structure [11]. This process involves some special fabrication techniques, but may prove to be very useful as device dimensions continue to decrease.

If a line-of-sight deposition process is used and some photoresist sidewall coverage is realized, lift-off can still be used successfully. If the resist side-walls are near vertical, the metal deposited on these sidewalls will be much thinner than that deposited on top of the substrate or the photoresist, as shown in Figure 3.

To facilitate resist stencil removal, the sample is first placed in a metal etch just long enough to remove the thin sidewall deposition (negligible effect on top metal thickness), and then placed in a suitable resist stripper for lift-off [12]. To optimize this sidewall metal etch-back process, rotation of the substrate during deposition will insure that the sidewall metal thickness will be essentially the same across the face of a wafer, allowing a uniform etch-back [13].

b. Lift-off Involving Sputtered Metals

For successful lift-off of metallic thin films using thick photoresist stencils, deposition techniques are normally limited to electron-beam or thermal filament methods. It has been shown [8] that metal deposited by means of a sputter gun can also be lifted off if the

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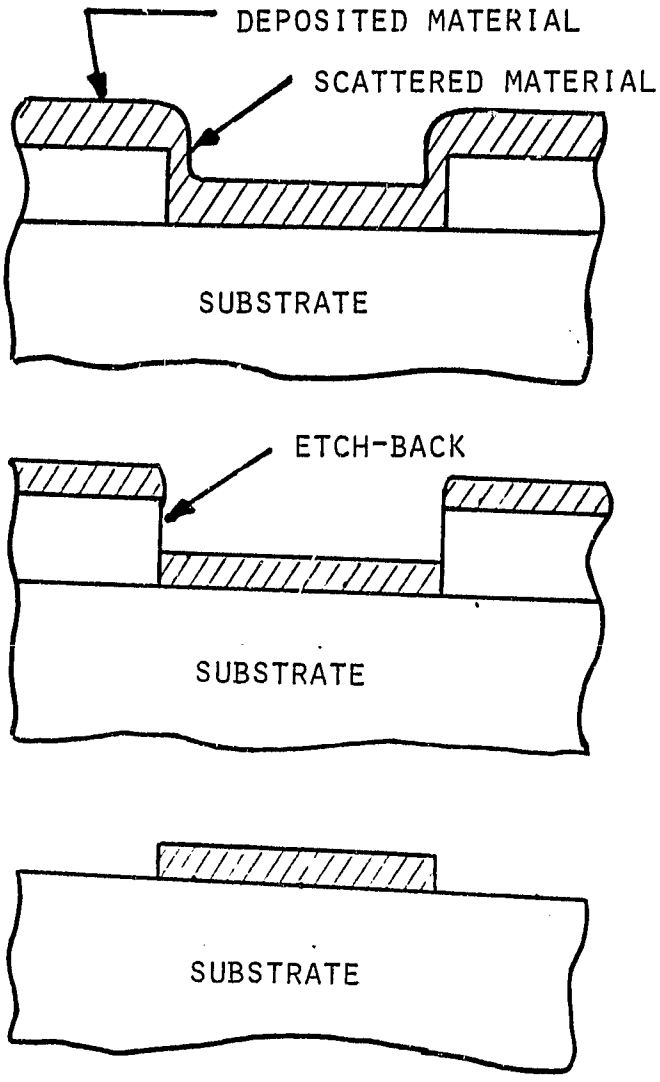

Figure 3. Lift-off using the etch-back process. (a) Metal is deposited on photoresist stencil having thin side-wall coverage due to scattering effects. (b) The deposited metal is partially etched (etch-back) to expose resist sidewalls. (c) After lift-off, the desired metal pattern is rendered.

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substrate is far enough from the gun so that a 'line-of-sight' deposition occurs (i.e., metal particles arrive at the substrate in a direction perpendicular to its surface), as shown in Figure 4. In a normal sputter deposition process, the sputtered metal coats the "sidewalls" of the photoresist stencil so well that they cannot be penetrated by the solvent needed to dissolve the under-lying photoresist, thus inhibiting lift-off.

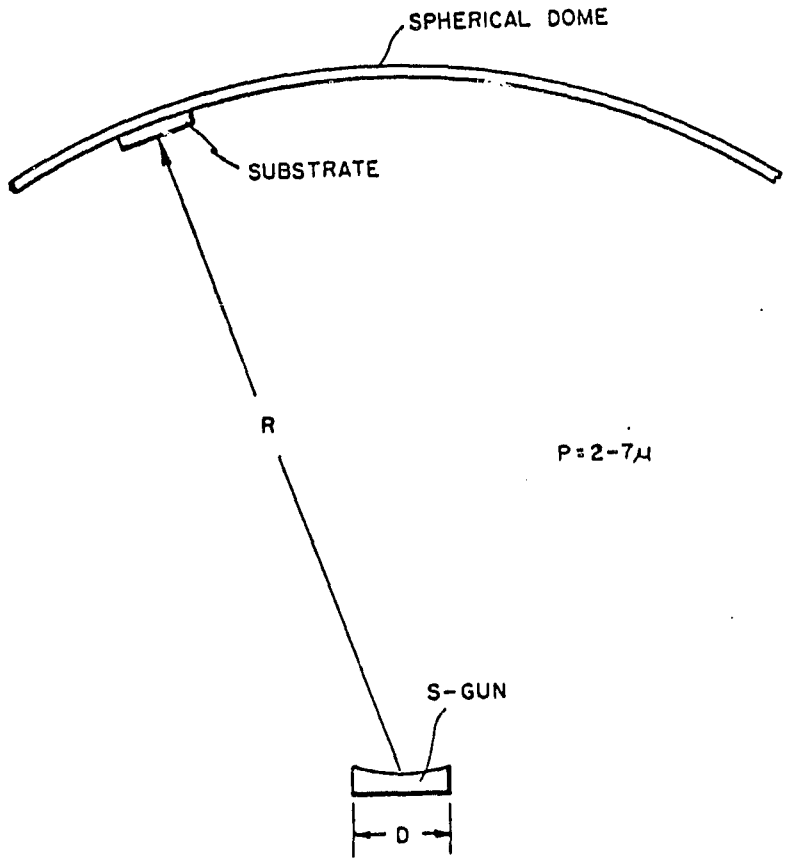

Figure 4. Simulating a 'line-of-sight' deposition process using a sputter gun. Typically, R is much greater than D.

The disadvantage in using this process is that typically, the distance of the substrate from the sputter gun, R, is much greater than the size of the sputter gun target, D, and most vacuum systems are unable to handle this. Also, the deposition rate is very slow.

It has recently been reported that even sputtered aluminum or aluminum alloy may be patterned using the lift-off technique if the photoresist stencil sidewalls are verticle or have a slight overhang [10] even when the substrate is close to the sputter-gun. In fact, it is claimed that narrow aluminum alloy lines having a greater thickness than the photoresist can be lifted off. The key to the success of this process involves maintaining the substrate at a low temperature (less than 100°C) during deposition to prevent (1) deformation of the photoresist pattern and (2) closing of the microcrack required for solvent penetration in order to accomodate lift-off. The microcrack formation results from the film growing perpendicular to the vertical sidewall of the photoresist pattern and the horizontal substrate surface, respectively. These films contact each other near the photoresist pattern edges, but do not fuse into one due to having different growth directions from each other at the low-deposition temperature as shown in Figure 5. Penetration through this microcrack by a suitable photoresist stripper allows the lift-off process to occur, resulting in the desired patterned metal. The sidewall of this resulting metal has a slope angle depending on the relative growth rates of the metal on the substrate surface and the photoresist sidewall during metal deposition. Also, since the photoresist sidewall deposition rate is a function of the argon ion concentration present at the time of deposition (i.e., the greater the

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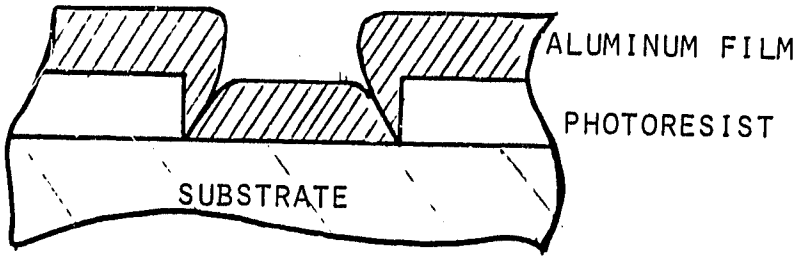

Figure 5. Profile of sputtered metal showing sidewall coverage and microcrack.

number of collisions the aluminum atoms have with the argon ions, the greater probability for sidewall deposition), the slope of the sidewalls of the resulting metal pattern is a function of the vacuum pressure at the time of deposition, which can easily be controlled. Figure 6 illustrates the variation in this slope angle as a function of vacuum pressure, where the slope angle of the metal line is given by

$$\theta = \tan^{-1} \left\{ \frac{\text{deposition rate normal to Si}}{\text{deposition rate normal to P.R. sidewall}} \right\}$$

The major disadvantage of depositing metals with the substrate at such a low temperature is the poor resistance against electromigration due to small-grain aluminum films resulting.

2. Double Layer Photoresist Applications

a. Double Layer of Same Photoresist Type

An overhanging photoresist stencil can be realized by using two applications of the same type of resist if the first layer is properly treated before applying the second layer [14]. In this process,

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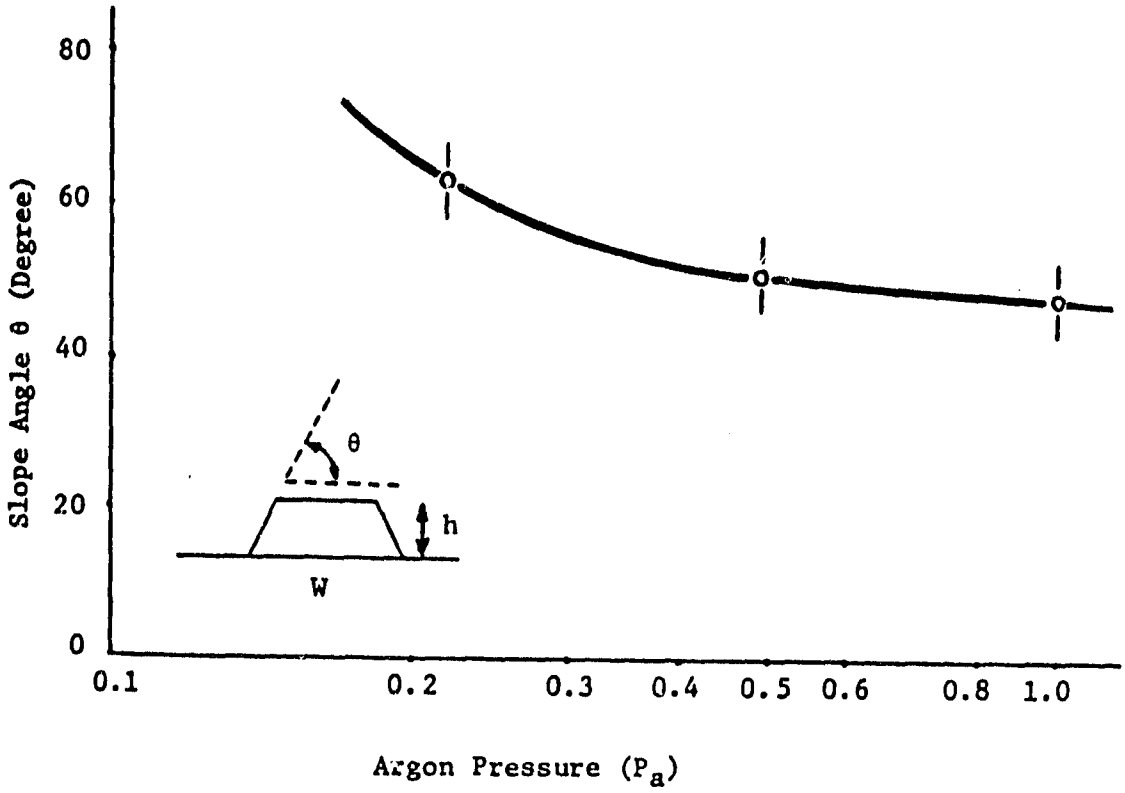

Figure 6. Variation of sidewall slope angle as a function of vacuum pressure for metal pattern deposited by sputter technique.

typically a positive acting photoresist is applied to the substrate at the desired thickness (typically one micron). This layer is pre-baked and their blanket exposed to ultra-violet (UV) radiation. This exposed layer is then treated with a gaseous plasma in an atmosphere of a fluorocarbon gas (as CF_4). The purpose of this surface treatment is to minimize interaction between the two layers of resist. A second layer of positive resist is then coated on top of the first layer, prebaked and pattern wise exposed to UV radiation. Both layers are then developed in an aqueous alkaline developer for such time that the bottom resist

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layer undercuts the top layer, resulting in a negative slope stencil as shown in Figure 7.

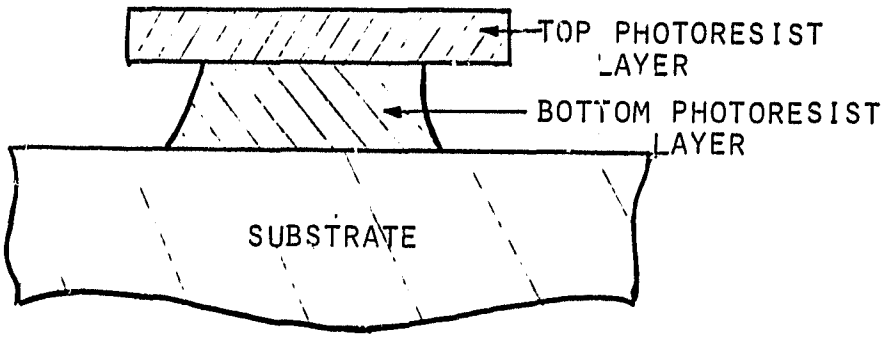

Figure 7. Negative slope stencil resulting from two layers of photoresist.

b. Two Layers of Different Photoresist Types

Several lift-off applications have been reported which utilize two separate resist layers using either an electron beam [15,16] or a deep UV [17] exposure system. When two dissimilar resist layers are used, the system has an advantage in that the image is defined on the top resist layer, by developing in a solution that does not attack the lower layer. Thus, better resolution and image size control is obtained than in a single resist process. After complete image development of the top layer, the developer solution is changed and the bottom layer is developed in a solvent that does not attack the top layer further. This assures that the image dimensions remain unchanged after complete development of the bottom layer, or even the slight over-development which is necessary to ensure adequate undercut of the resist structure for lift-off. During metal evaporation, the top resist layer provides shading of the substrate and consequently defines

the metal structure dimensions. For these reasons, the two layer resist system is somewhat more dose tolerant and therefore, is less sensitive to the proximity effect than a resist which depends on dose to control the lift-off profile. The sensitivity of this two-layer resist system is determined by that of the top layer.

There is an additional major advantage of this technique. During spinning of the bottom layer which is normally thick (at least one micron), topographical features due to previous wafer processing are largely planarized so that spinning of the top layer results in a level film of uniform thickness. This ensures that better image size control is obtained even over high topographical features.

Typical photoresist types used for the electron-beam lithography two-resist layer process includes poly-methyl methacrylate (PMMA) for the bottom thick resist layer and IBM copolymer resist [15], Hunt MPR resist [17] or Matsushita positive resist (MPR) [16] for the top layer.

A trilevel positive photoresist system has also been reported [17] which incorporates a thin separator layer of aluminum film between the two layers of resist. While this tends to prevent dissolution of the two layers of photoresist such that their properties become somewhat homogeneous throughout, it does add additional expensive processing steps. If dissolution can be prevented by "buffering" the first layer photoresist using a plasma CF_4 treatment mentioned earlier, or a thermal treatment, prior to applying the second layer, then the intermediate aluminum layer is not required.

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3. Chemical Treatment of Photoresist Stencil

Treatment of positive pohtoresist with chlorobenzene to obtain a negative sloped stencil was first reported in 1977 [18]. This consisted of depositing Shipley AZ1350J on a substrate and prebaking at 70°C for 20 minutes. The resist is then exposed to UV light using the desired pattern and then soaked in chlorobenzene for 5-10 minutes depending on the thickness of the photoresist and the desired thickness of the stencil overhang. After a develop and rinse cycle, the stencil shown in Figure 8 results.

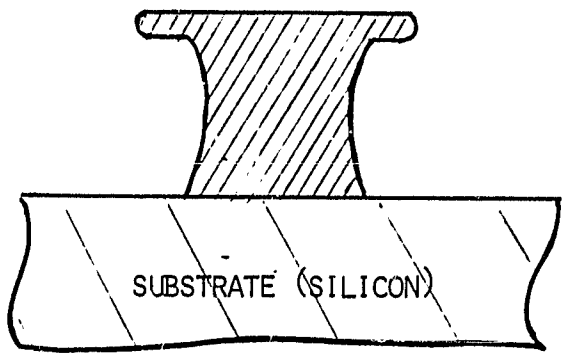

Figure 8. Cross-section of photoresist stencil having been treated with chlorobenzene.

The resulting structure occurs because the upper portion of the resist is modified during the soak process, thus causing a development rate different between the upper modified portion and the bulk resist film. As one might expect, the overhang thickness is also a function of photoresist prebake temperature.

Other solvents, such as toluene and xylene, can also be used as a soaking material [19] and form similar overhang structures. These

other organic solvents have slower penetration rates than chlorobenzene, thus requiring a longer processing soak time in order to modify a given depth within the photoresist material, unless additives like n-butyl acetate are added to the toluene or xylene solvents.

The use of this lift-off process has been reported in the fabrication of Josephson integrated circuits [20] using projection exposure. To promote adhesion of the photoresist stencil to SiO_2 substrate, hexamethyldisilazane (HMDS) was used prior to resist application in addition to depositing a layer of TiO_x on the substrate surface. It was reported that the stencil overhang was sufficient to withstand the sputtering during rf discharge cleaning prior to deposition of the metal layer.

The diffusion tendencies of this chemical treatment process, the effect of pre-bake temperatures and time, the use of alternate chemicals to generate a more stable overhang structure, etc. have been thoroughly investigated by Hatzakis, et al, [21] using optical UV exposure systems and Shipley AZ-type photoresist.

4. Use of Electron Resist

One of the first applications of lift-off utilizing a single layer of photoresist resulted from the (then) undesirable undercut of the resist when exposed using an electron beam [22]. This undercut feature was used to an advantage by the investigators, both for circuit and mask fabrication.

Electron beam lithography systems are being preferred over optical systems for the exposure of photoresist layers due to improved resolution, power density and deflection capabilities of the electron beam. Also, since practical optical systems are ultimately limited in

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resolution by the wave length of light, electron beams offer an attractive alternative for fabricating submicron structures. A typical electron-resist stencil is shown in Figure 9.

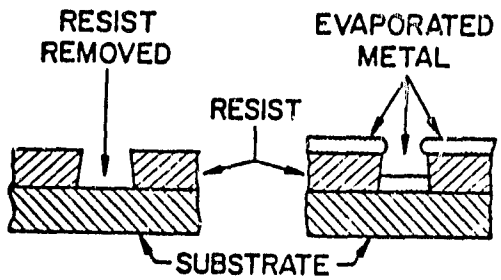

Figure 9. The use of an electron-resist to form negative sloped sidewalls.

Writing directly on wafers with an electron beam eliminates delays associated with making photo masks and allows easy pattern changes. In order to use e-beam lithography, however, a suitable lift-off process is required. It is generally easier to obtain undercut with electron exposure than with optical exposure. The electron beam spreads during passage through the resist, the exposure near the substrate is enhanced by back scattered electrons. It is also generally known that linewidth errors of several types are observed for e-beam lithography. The first is an overall linewidth bias, which can be sometimes corrected by adjusting the design dimensions. Since lines generally become wider than the width exposed, only a limited amount of correction can be applied before the exposed width becomes vanishingly small. In addition, electrons may be scattered from one shape to an adjacent one leading to linewidth

changes depending on the proximity of one shape to another (proximity effects). These errors can be reduced by proximity correction techniques [24]. Other linewidth errors include random variations from wafer to wafer and between sites on the same wafer. These errors can be caused, for example, by changes in resist thickness or properties, baking conditions, and development conditions. Reasonable processing variations must not cause excessive linewidth changes.

The combination of using an electron beam exposure system and a chlorobenzene soak to generate a lift-off stencil has also been reported [23], which uses Shipley AZ 1350J positive photoresist. With this process, the AZ 1350J performed well at the baking temperatures used and provides reproducible profiles. Adhesion of the stencil to the oxide is reported to be good and the exposure intensity is about three times lower than that necessary for normal electron resist like PMMA. The linewidth measured at the top of the resist accurately reproduces the exposed width, implying a tight control of dimensions. However, a greater variation is seen in width measured at the substrate. The most serious disadvantage reported is the large undercut of about 0.5 μm, which limits the minimum distance between developed pattern shapes to approximately 1.5 microns.

B. Use of an Auxiliary Layer to Form Lift-Off Stencil

This technique uses the effect of an undercut auxiliary layer. There are no limitations concerning the shape of the sidewall contours of the resist, and metal atoms are allowed to impinge on the substrate surface at various angles of incidence, as is the case, for instance, in vacuum systems with planetary rotation of the substrates.

Fine metal lines and spaces can be achieved with tapered sidewalls of the conductors, even if the metal layer thickness is on the order of 1 micron, which is the currently used thickness for integrated circuits.

Schematic illustration of the lift-off process using an auxiliary layer is shown in Figure 10. First, a thin auxiliary layer is deposited on the substrate. With the aid of conventional photolithography, those regions which shall be free of metallization are masked with photoresist. The auxiliary layer is etched and due to undercutting, the photoresist bars overhang the remaining portions of the auxiliary layer. The desired metallization layer is evaporated by moving the substrates in the vacuum chamber su h that the evaporated metal atoms impinge on the substrate surface at varying angles. The metal region deposited on the photoresist pattern are lifted off by dissolving the photoresist in a suitable stripper. It is important to note that in the undercut regions the bottom of the photoresist bars is always completely free of metal coverage even if the metal atoms arrive at angles near 90°. The stripper can thus reach the photoresist after having penetrated the microcracks. Finally, the auxiliary layer is removed selectively and the resulting metallization pattern is inverse compared to the original photoresist pattern.

A computer simulation of the metal la r buildup in the vicinity of the undercut photoresist edges assuming no diffusion of the metal atoms after deposition using this auxiliary layer approach has been reported [25]. This same author used an auxiliary layer of chromium before depositing a thick Shipley AZ 1350H photoresist layer on top and patterning the two to render an undercut.

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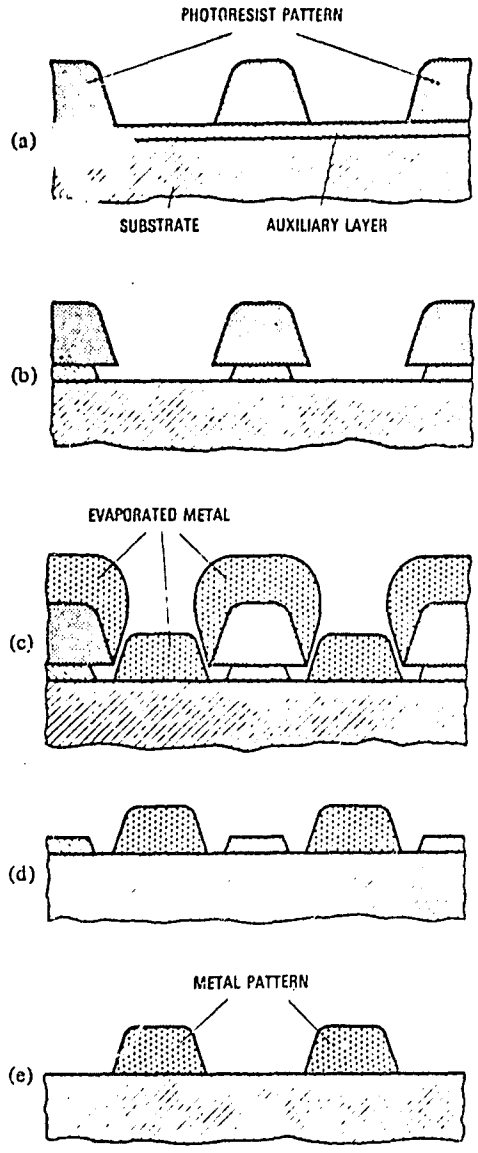

Figure 10. Schematic illustration of the investigated lift-off process using an auxiliary layer. (a) Deposition of a thin auxiliary layer followed by photoresist patterning. (b) Etching of the free portions of the auxiliary layer. (c) Metal evaporation. (d) Metal lift-off. (e) Removal of the auxiliary layer.

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1. Polyimide Auxiliary Layers

Recently, polyimide has been reported to act as an auxiliary layer [26] as shown in Figure 11.

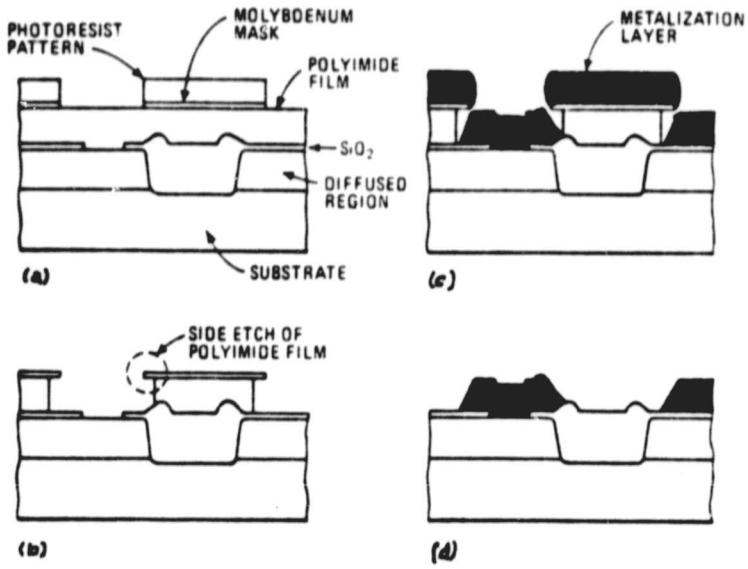

Figure 11. The use of polyimide and a molybdenum mask as a lift-off medium.

This approach permits deposition of the metals at high temperatures thereby allowing an increase in yield. These researchers claim that due to the poor heat resistance of standard photoresist, low temperature deposition of the metallization layer results. At low temperatures, adhesion of the metal to the wafer may be a problem. Polyimide resin PIQ (or polyimide isoindroquinazolinedione) can withstant temperatures up to about 450°C and are typically used as insulation for electric wires. The process begins by spin-coating the silicon wafer with a PIQ film. Then a layer of molybdenium is

deposited on this auxiliary lift-off layer and etched, as shown in part (a) of the Figure 11.

After removal of the photoresist pattern, the next step is to remove the parts of the auxiliary lift-off layer exposed during the etching. Removal is by reactive sputter etching, producing a precisely controlled side etch (b). The effect of this side etch is to separate the metallization layer on the polyimide from the same layer on the substrate (c). Electron-beam evaporation is used to deposite the metallization layer, composed of alloys like aluminum silicon or aluminum copper silicon. Then electrolysis removes the lift-off layer, the molybdenum mask, and the unwanted metal on top of them (d).

Since the metal layer is not etched during lift-off, many different materials may be used for this layer without changing the process.

Typically, the PIQ layer is fairly thick upon application, such that its surface becomes very smooth and nearly planar, almost irrespective of the underlying steep projections and depressions. Since the PIQ layer is nearly planar, this allows the thin molybdenum mask pattern to be very accurate.

Another multi-step lift-off process involving polyimide and dry etching processes has also been reported [27] for patterning the second level of a double layer metallization system. Even though the end result of this process has many desirable features (i.e., a layer of silicon nitride over the polyimide as part of the process, thus negating the passivation requirement), its process complexity will probably preclude its use in a production environment.

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2. Dielectric Auxiliary Layers

A number of dielectric materials may be used to form an undercut stencil acceptable for lift-off processes. The most common processes reported involves depositing a layer of chemically vapor deposited (CVD) silicon dioxide as the auxiliary layer [28,29]. Schematic illustration of a typical process is shown in Figure 12.

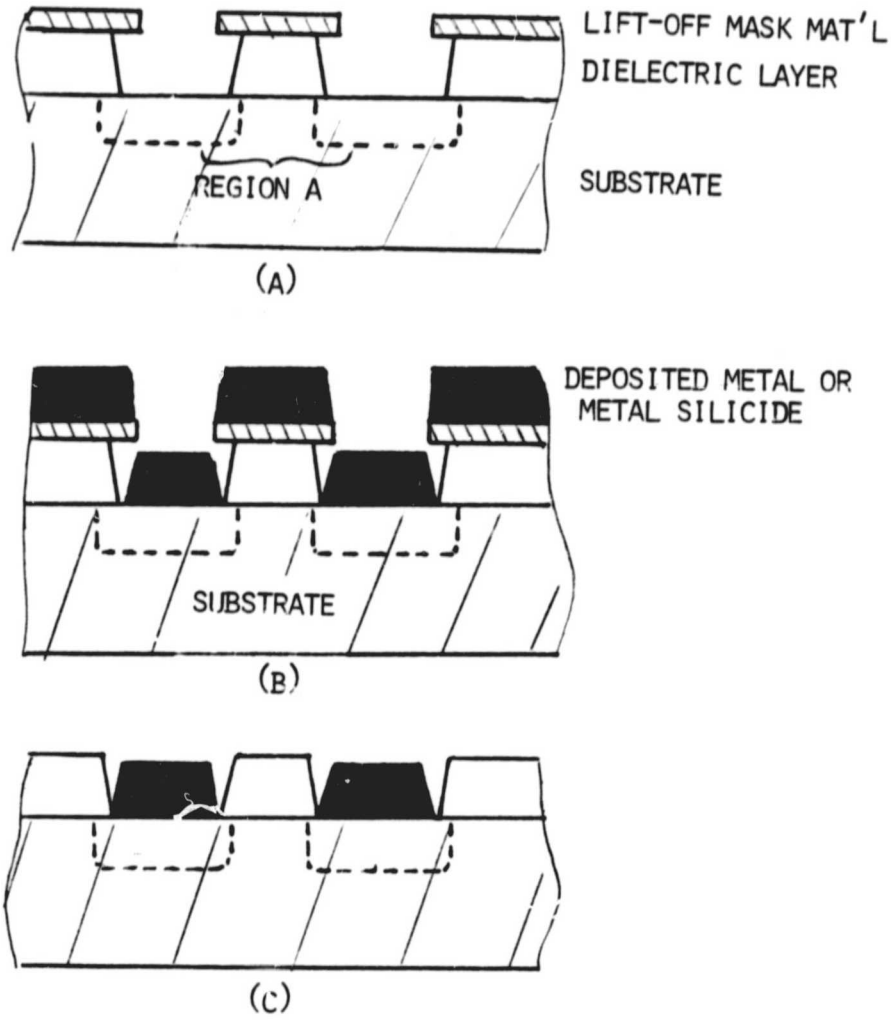

Figure 12. Typical process utilizing a dielectric layer as an auxiliary layer.

This technique also provides for the potential of having self-aligned diffusion and conductive contacts for semiconductor devices. Initially, a thick dielectric layer is realized on the substrate (which could be silicon dioxide for a silicon wafer), and then a thin lift-off masking layer is provided, which may be any material having either a lower etch rate, or which is capable of being selectively etched independent of the dielectric (or substrate) materials. The lift-off mask material and the dielectric material are selectively etched to expose the substrate using standard photolithography techniques in such a manner as to provide a stepped profile as shown in Figure 12a. If the lift-off mask material can withstand the temperatures, a diffusion or ion implantation step can follow, resulting in the dotted-line profile shown in (a). After a drive-in or anneal step, a metal-silicide or other high conductivity material is deposited as shown in (b), and then the mask material is selectively removed lifting off the undersired metallization regions as shown in (c). The dielectric layer can either be selectively removed or left to assist in planarizing the topography for any addition processing steps.

If the mask lift-off material of Figure 12 is a photoresist, then the slope of the dielectric layer sidewalls can be controlled by the dry process employed in forming them [29]. It has been found that for dielectric layers of vapox (CVD-SiO_2), phosphosilicate glass (PSG), thermally grown oxide (SiO_2) and arsenosilicate glass (AsSG), if these dielectric layers are exposed to plasmas of CF_4, CCl_4 or CF_4 - O_2 then their etching characteristics in a NH_4F solution are altered such that a tapered dielectric layer results

when using photoresist as the patterning vehicle. The amount of time the dielectric layer is exposed to the plasma effects the slope angle of the dielectric sidewalls, within limits.

As layout dimensions continue to decrease, then the amount of undercut realized in forming the lift-off stencil becomes very important. As seen in region A of Figure 12a, if an isotropic etching procedure is used to etch the dielectric layer as the dimensions are scaled down, a "mushroom" effect results due to an excessive thinning of the top portion of the dielectric layer and could cause the top lift-off layer (and deposited metal) to be broken off.

There is a process reported [30] which accurately controls the amount of undercut and the ratio of the width of the top to the bottom portions of the dielectric layer in region A. This process adds a thin reactive ion etch (RIE) mask on top of the metal lift-off layer and the dielectric layer is etched anisotropically through 70 to 95% of the dielectric layer, resulting in no undercut. Then the remaining 5-30% of the dielectric layer is etched using an isotropic (wet or dry) etch resulting in the desired controlled undercut.

3. Metal-Photoresist Auxiliary Layer

Another method, which was eluded to in discussing two-layer photoresist processes, uses a metal-photoresist layer as an auxiliary layer to form the stencil required for lift-off [32]. The method actually consists of a three layer photoresist-aluminum-photoresist sandwich as shown in Figure 13.

The top layer of photoresist defines the pattern, the bottom photoresist layer provides the undercut and the aluminum film merely provides an intermediate layer to keep the top layer of

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photoresist from dissolving the bottom layer of photoresist during application of the top layer.

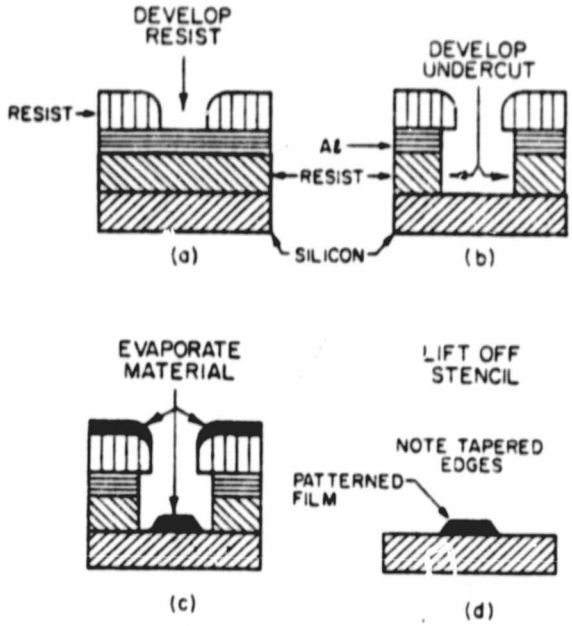

Figure 13. Lift-off technique using photoresist-aluminum photoresist stencil.

The resolution of this method is determined by the photoresist, the exposure equipment, or the mask used, and generally yields results that are very comparable to those obtainable with single layer resist patterning methods. With this particular method, the resolution is not greatly affected by the etching process or subsequent developments of the bottom photoresist layer. The intermediate layer of Al also causes good line uniformity because of the uniform reflection and absorption created by this layer. As a result, at points where a pattern crosses over a previously defined layer, no changes in linewidth are noticed.

Prior to depositing the thin metal layer, the bottom photoresist layer is exposed in a blanket fashion. A disadvantage of this method is the attainment of the undercut by developing a totally exposed film of photoresist which is not a self-limiting process. However, if a minimum exposure of the bottom resist is undertaken, such that all resist is completely exposed but developed at a slow to moderate rate, adequate control of the undercut can be achieved by moderately accurate timing of the development process.

Another process has been reported which makes use of only metal as the auxiliary layer [33]. This process, shown schematically in Figure 14, does not include photoresist in the lift-off stencil which is susceptible to thermal degradation, so that the substrate can support RF sputtering and high temperature evaporation processes.

Initially, a plasma etch mask is electroplated through a resist pattern (not shown) on to the lift-off metal layer. It may be noted that in this process the original resist pattern has the same polarity as the final metallized structure (typically, this is not the case). The lift-off metal is plasma etched such that a large undercut is realized. This undercut provides the overhang which prevents step coverage by the desired metal to be deposited and lifted off.

The desired metal is next deposited at a high temperature if desired, and the lift-off metal is removed chemically. Since RF sputter or evaporation at high substrate temperatures can be undertaken, the electrical, mechanical and magnetic properties of the final metal pattern are more easily tailored for device requirements.

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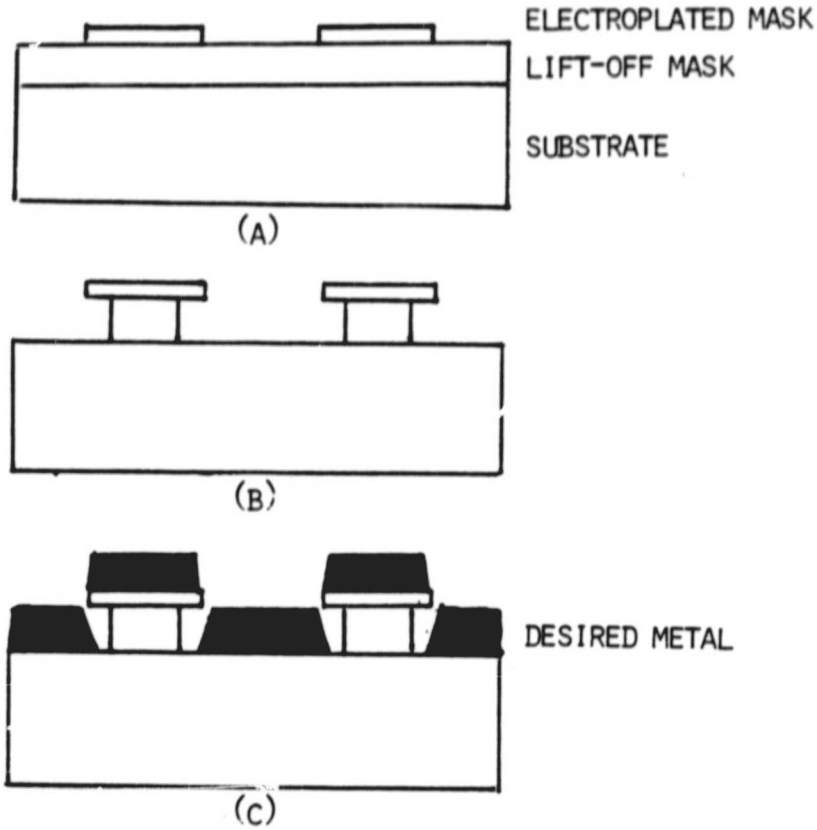

Figure 14. Using a metal for auxiliary layer for temperature stability

One parameter which impacts the success of any lift-off process, and one which has not yet been addressed, is the ductility of the metal being patterned. Unless there exist a very clean break between metal to be lifted and metal to remain, a ductile metal such as gold can cling tenaciously and give poor edge definition or no lifting at all. This problem is avoided by selecting proper relative thicknesses of the layers and by having a suitable cross-sectioned profile of the mask opening. Brittle metallizations tend to be more

forgiving of short comings of these parameters. A brittle metallization is one which tends to fracture at the edges of pattern steps, thereby causing discontinuity.

III. EXPERIMENTAL METHODS ATTEMPTED IN REALIZING LIFT-OFF PROCESSES

A. MSU Research Facilities

The Microelectronic Research Laboratory at Mississippi State University consists of approximately 6600 square feet of space located on the fourth floor of the recently built (1977) Simrall Electrical Engineering Building. With the space and facilities purchased with state funding (approximately $0.5 million) plus equipment acquired through industrial donations and research contracts, the total laboratory represents well over a $2 million dollar equivalent capital investment. Approximately 3,000 square feet consist of class 10,000 clean rooms. Within this space, facilities exist for mask-making and photolithography, for chemical preparation, oxidation, etching, diffusion of impurities, ion implantation, chemical vapor deposition of silicon dioxide and silicon nitride, epitaxy and polysilicon deposition, for metallization (E-beam, thermal evaporated or sputtered), die-bonding and lead attachment, wafer and package automated testing, and for the evaluation of device and integrated circuit parameters. In addition, the hybrid facilities allow fabrication of thick and thin film circuits and encapsulation. Additional diagnostic capabilities are acquired through the University's Scanning Electron Microscope Center.

Key pieces of equipment utilized in performing the research activities described in this report consist of the following:

- D.C. Sputter System. The vacuum system for the sputter chamber consists of a Welch Duo Seal model 1376 roughing

pump and a Varian M6 diffusion pump capable of generating pressures in the 10^{-3} to 10^{-9} torr range and at a pumping rate of 2400 liters per second (air). The DC sputter gun is a Sloan model S-310 which uses a target cathode in a hollow sleeve form, a disk-shaped anode, and a cylindrical permanent magnetic. The gun can use either 1/16 or 1/8 inch target material in an 18 inch circular system. Its DC operating voltage is -300 to -600 volts at an operating pressure of 5-15 microns. The deposition rate for aluminum is approximately 60, 130 and 180 Å/min. for a 1 KW, 2KW and 3 KW energizing source, respectively. Wafers are deposited with metal while rotating on a 10 inch round pallet under the sputter gun, which is approximately 5 inches above the wafers as they are rotated under the gun. This insures metal deposition from all angles resulting in excellent step coverage. Several aluminum targets were used in this investigation, including ultra pure Al, Al with 2% Si, Al with 1.5% Si and 3% Cu, and Al alloy 6061. This structural grade alloy contained the following impurities:

Si	0.4 - 0.8%
Cu	0.15 - 0.4%
Fe	0.7%
Mg	0.8 to 1.2%
Mn	0.15%
Cr	0.15 - 0.35%
Zn	0.25%
Ti	0.15%

The primary reason for using this Al alloy is for the prevention of hillock formation.

- Thermal Evaporator. This system consists of a Varian VI-221 model 932-00281 vacuum chamber having two Varian Vac Sorb roughing pumps and a Vac Ion Pump. This is a 100% clean pumping system having no hydrocarbons or other contaminants back-streaming. The Vac Sorb roughing pumps are capable of pumping at an 80 liter per second rate which is ultraclean and vibration free. The Ion Pump operates with a lower range of 10^{-7} to 10^{-10} torr. Evaporation is realized using ultraclean, ultrapure aluminum studs placed over an aluminum coated tungston filament.

- Mask Aligner. The majority of the work described in this report was accomplished using an Electroglas Model 500D Optical Mask Aligner for exposure up to 2-1/4 inch diameter wafers with 0.75 micron accuracy. The light source consists of a 200 watt mercury short arc lamp. Light intensity at the wafer is approximately 20 mJ/cm^2.

- Photoresist spinner. All photoresist coatings (both positive and negative) and polyimide coatings were accomplished on a Headway two-head spinner capable of spinning in an adjustable range of 200 to 12,000 rpm for specific time settings. All photoresist and related processes are carried out in class 100 laminar flow hoods which are both humidity and temperature controlled in a room that is class 1000 under amber lights.

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Film Thickness Measurements. Transparent films are measured with a Gaertner Scientific Corp. ellipsometer which is based on a helium-neon laser system. Metal films are monitored with a sodium light source interfermeter microscope. Also, the Hitachi HHS-2R scanning electron microscope available in the Electron Microscope Center is capable of rendering very accurate measurements.

Photographs of the photolithography room and the metal deposition room are shown in Figures 15 and 16.

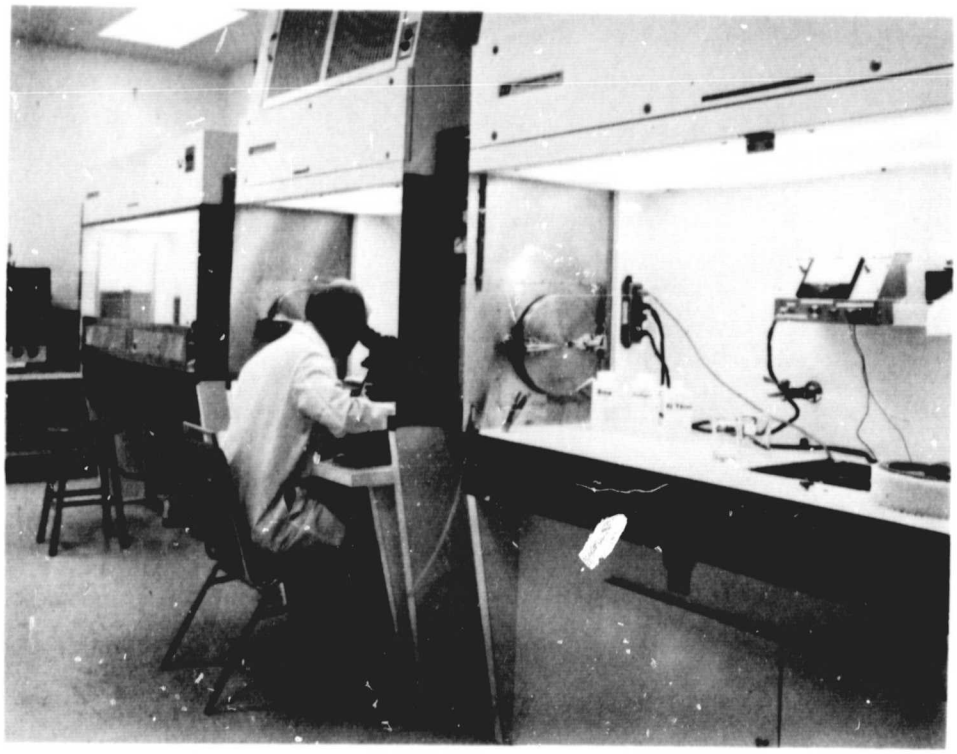

Figure 15. Photolithography Facility

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Figure 16. Metallization deposition equipment

B. Lift-Off Processes

All experiments were conducted using two-inch silicon wafers typically of <111> orientation and having a resistivity of 5-20 ohm-cm. Several photoresist types have been employed, the most frequent positive type being Shipley AZ1350J and AZ111, and negative type being Waycoat Type 3 Number 43. Figure 17 illustrates the thickness of the resulting post baked photoresist for these three types of resist as a function of final spin speed of application. The resulting resist thickness was measured using the calibrated scanning electron microscope. In most cases, all test wafers were thermally oxidized prior to conducting lift-off test using a

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combination of dry-wet-dry oxygen ambient at approximately 1000°C until approximately 2,500-10,000 Å oxide is realized.

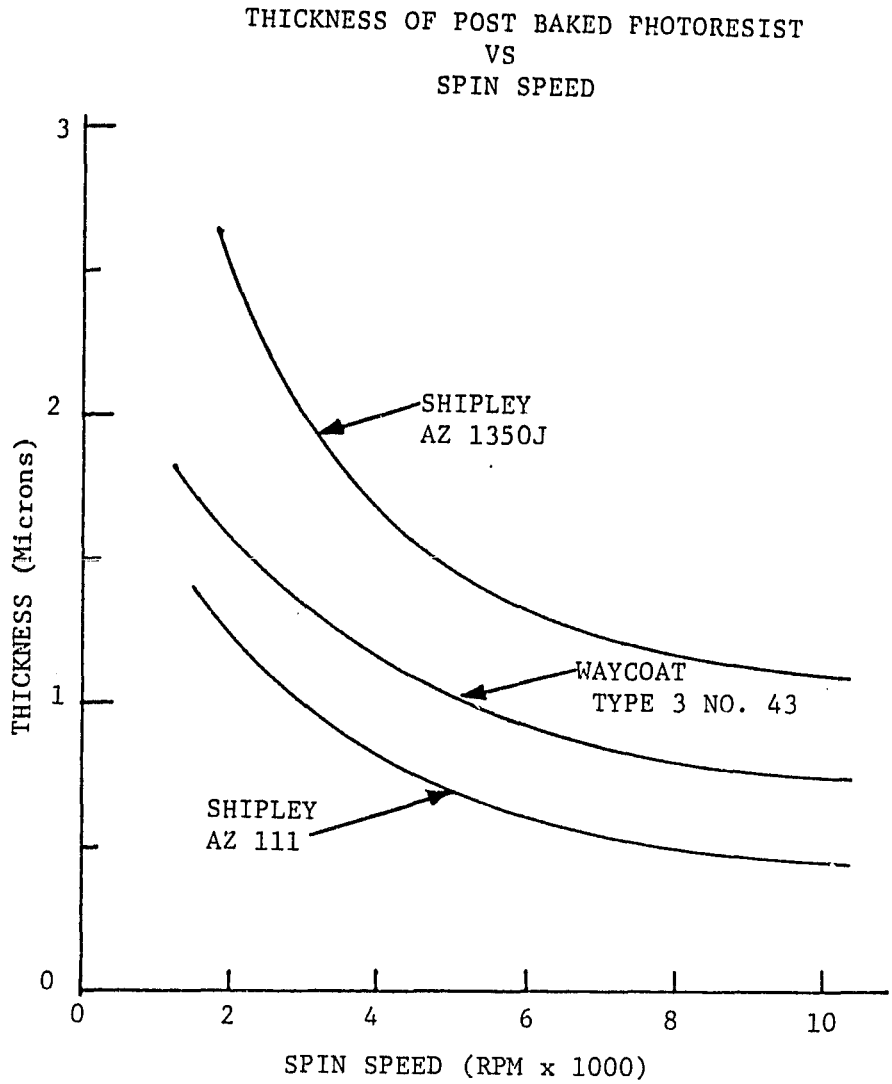

Figure 17. Thickness of post baked photoresist for Shipley AZ1350J and AZ111 positive resist, and Waycoat Type 3 negative resist as a function of application spin speed.

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1. The Conventional Photoresist Lift-Off Process.

The first attempt at patterning a deposited metal film consisted of the 'convention lift-off method' as illustrated in Figure 18. Both dc sputtered and thermal evaporated aluminum layers were investigated. Figure 18 illustrates the results obtained when 3500 Å aluminum alloy type 6061 film is dc sputtered onto an approximately 2 micron thick Shipley AZ 1350J patterned photoresist layer. An attempt to lift-off this metal using solvents of acetone and Shipley AZ Thinner was unsuccessful as can be seen. The AZ1350J was spun on the wafer at 3000 rpm. Each bar of Figure 18 is 0.7 mils wide and 5 mils long. Spacing between bars is also 0.7 mils.

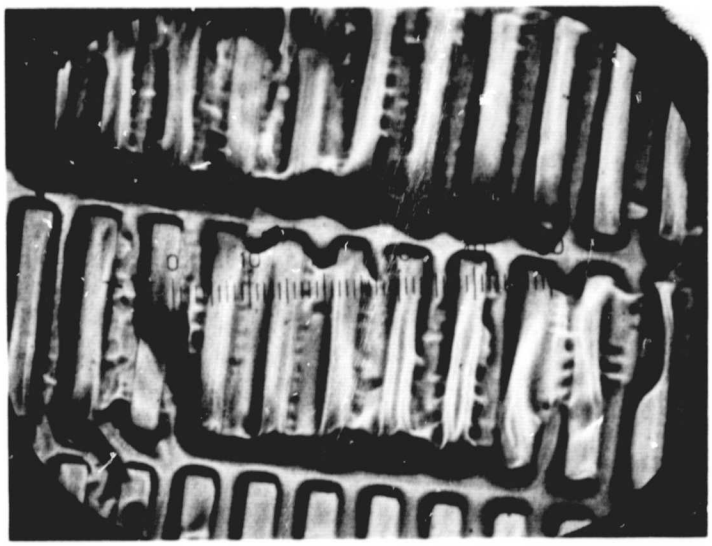

Figure 18. Lift-off attempt using dc sputtered aluminum alloy 6061 over 2 micron patterned AZ1350J.

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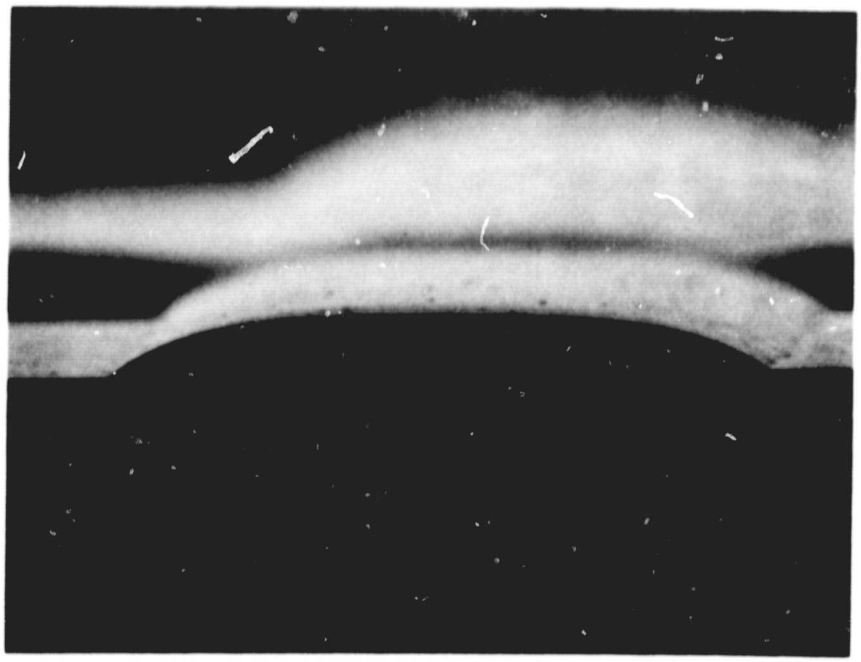

Figure 19. Scanning electron micrograph of dc sputtered metal over AZ1350J illustrating continuous metal over photoresist sidewalls (absence of microcrack).

A scanning electron micrograph of a cross-section for one of the bars shown in Figure 18 is illustrated in Figure 19. Notice the smooth sidewall slopes of the photoresist layer resulting in excellent stepcoverage. Due to the lack of desired steep photoresist side slopes, this metal did not lift-off as desired.

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Next, a 'line-of-sight' method of metal deposition was attempted. Again using AZ1350J positive photoresist spun on the wafer at 6000 rpm and patterned, pure aluminum approximately 4000 Å thick was deposited using the thermal (filament) evaporator. Again, acetone and AZ Thinner were attempted as solvents to lift the metal off in an ultrasonic bath, but the best results were obtained using Shipley AZ Remover 1112A as the solvent as illustrated in Figures 20 and 21. The lift-off of Figure 20 has very uneven edges as seen. The lift-off resolution for Figure 21 is somewhat better, however this pattern was observed near the edge of the wafer where the metal thickness was barely over 1000 Å thick.

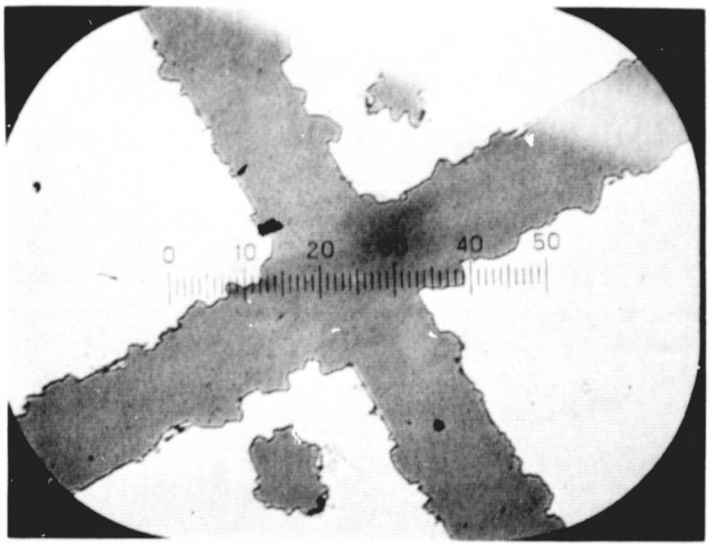

Figure 20. Lift-off of thermal evaporated pure Al 4000 Å thick over AZ1350J photoresist. The pattern is scribe lines and alignment marks.

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Figure 21. Improved resolution of thermal evaporated Al over AZ1350J, however, metal thickness is only approximately 1000 Å. Lift-off pattern width is 0.7 mils.

It was felt that an improved lift-off could be attained if the solvent used in the lift-off process was heated above room temperature in an ultrasonic bath. The heated solvent and ultrasonic action should allow better penetration of any microcrack of thin metal layer to assist in the lift-off process. Figure 22 shows the results of depositing 5000 Å aluminum using the thermal evaporation technique over AZ1350J positive resist which was deposited at 2000 rpm and patterned. The solvent was heated to 60°C and lift-off was performed

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in an ultrasonic bath. The solvent used was Shipley AZ Remover 1112A. The pattern consists of scribe lines and one mil wide alignment marks. Considerable improvement is seen over the results obtained in Figure 20 where room temperature solvent is used.

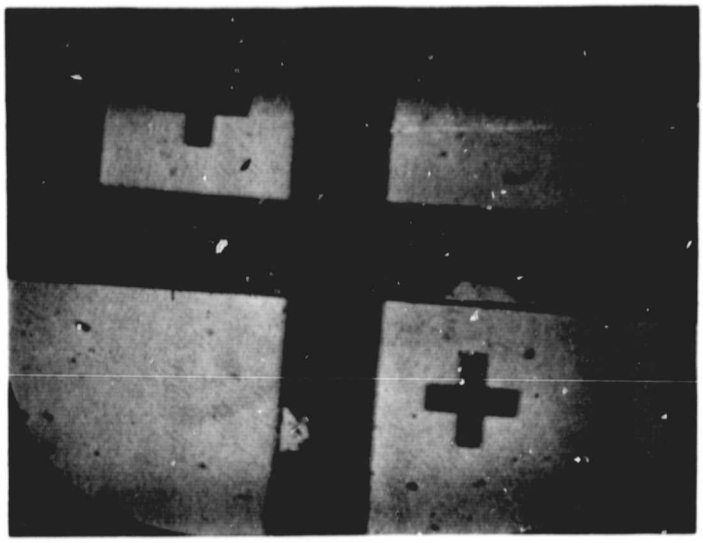

Figure 22. Lift-off of 5000Å thermal evaporated aluminum deposited over 2000 rpm AZ1350J using heated (60°C) AZ Remover 1112A in ultrasonic bath.

As a result of the considerable improvement obtained using a heated solvent for lifting off the aluminum layer, it was decided to extend this heat treatment effort. Next, a sample was prepared by spinning AZ1350J on a wafer at 4000 rpm and patterning using a photoresist test pattern. The thermal evaporated aluminum was then deposited to a thickness of 4500 Å and the wafer was placed in the

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mouth of a furnace tube (temperature at center of tube was 1000°C) having oxygen passing through it. The wafer was allowed to heat up for two minutes until the photoresist began to bubble under the metal (wafer temperature approximately 150-200°C). The wafer was then immersed in an ultrasonic AZ Remover 1112A solvent at 80°C for one hour. The results obtained are illustrated in Figure 23. The numbers indicate lines and spaces in tenths of a mil (i.e., '2' corresponds to 0.2 mils). Notice that lift-off of line and spaces down to 2-3 microns could be realized utilizing these heat treatment processes.

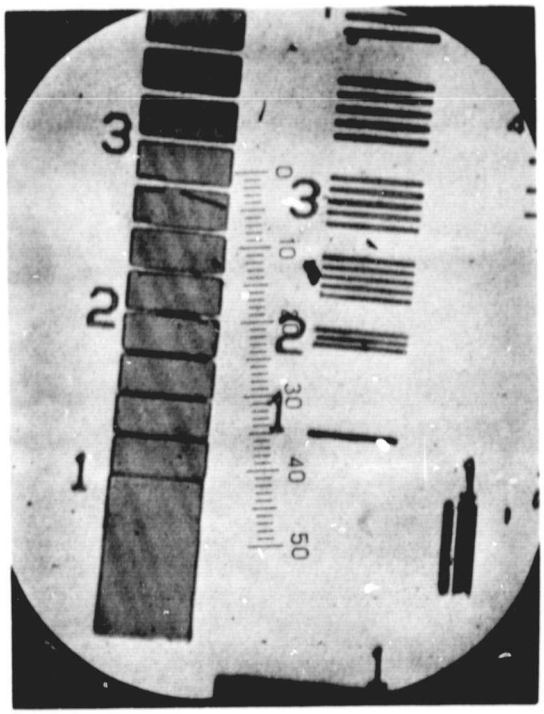

Figure 23. Lift-off of 4500 Å aluminum over AZ1350J photoresist after heating the wafer (to approximately 200°C temporarily) prior to immersing in ultrasonic agitated 80°C AZ Remover 1112 A solvent.

Since such good results were obtained using this latter process on thermally evaporated metal, it was decided to repeat the process for dc sputtered metal of approximately the same thickness. To insure a greater probability of success, the photoresist was made thicker by applying at 2000 rpm. However, as seen in Figure 24, the metal would not lift-off even for the larger area patterns.

Negative photoresist layers have been reported as rendering poor lift-off stencils due to side-slope 'rounding' tendency which allowed for good step coverage by the deposited metal [7]. However, an attempt to use Waycoat Type 3IC Resist 43, a negative photoresist, to lift-off thermally evaporated aluminum approximately 2500 Å thick was undertaken. The lift-off solvent used was Hunt "Micro-strip" and was heated to 90°C in an ultrasonic bath. The results obtained after a 15 minute immersion in this solvent is shown in Figure 25. Several other solvents were attempted in lifting off negative resist patterns but a suitable solvent could not be located, even using thermal cycling techniques.

Based on the experimental results obtained using this conventional photoresist lift-off process, the following statements and/or conclusions can be made:

i) A suitable solvent could not be found to lift-off metal when negative photoresist was attempted.

ii) Fairly good results were obtained using AZ1350J of 1.5 to 2 microns thickness if samples were heat treated and etched ultrasonically in 60-80°C AZ Remover 1112A for thermal evaporated metals, but not for sputtered metals.

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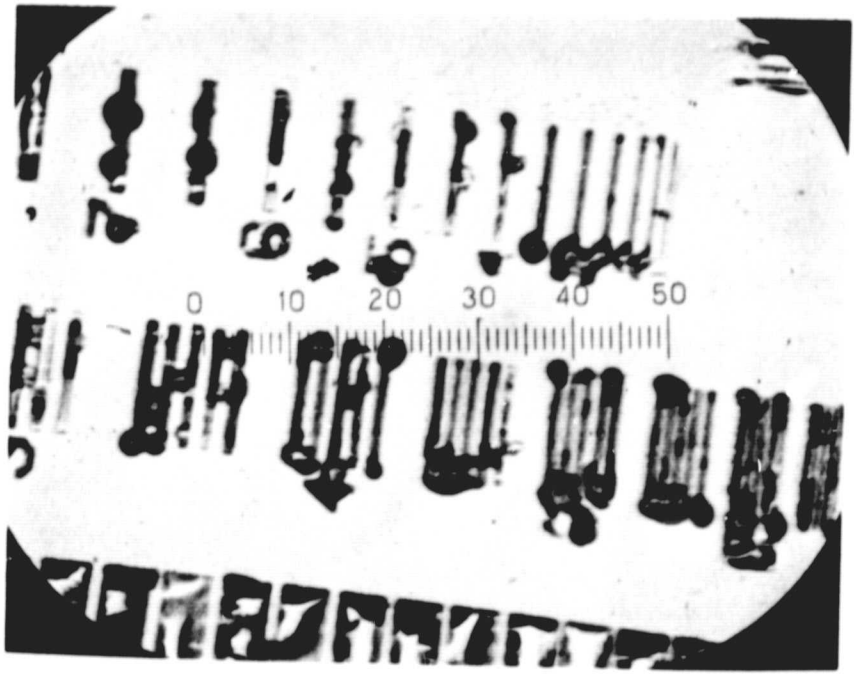

Figure 24. Lift-off procedure as described in Figure 23 except for dc sputtered aluminum.

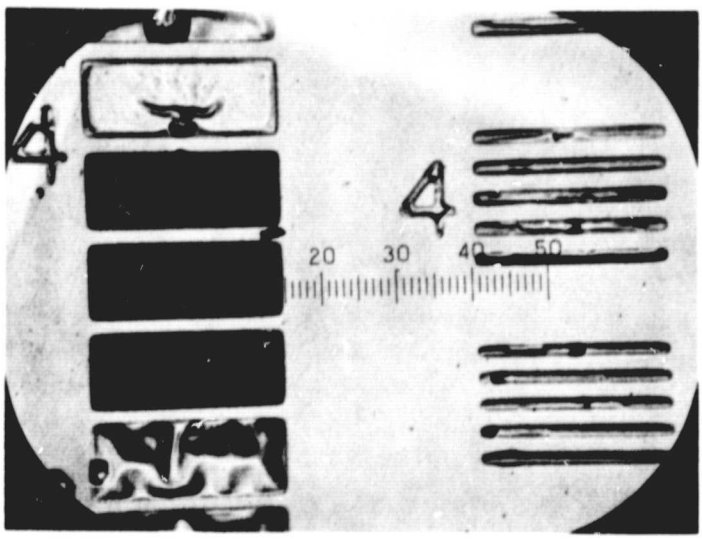

Figure 25. Lift-off using negative 4000 rpm Waycoat Type 3 I.C. Resist 43 and 2500 Å thermal evaporated Al after immersion in ultrasonic 90°C Hunt 'microstrip' photoresist stripper for 10 minutes.

iii) The deposited metal must be much thinner than the applied photoresist layer.

iv) At the photoresist base, the metal must be very thin (<100 Å) and brittle. Resist profiles which render a microcrack at the photoresist base should result in a superior lift-off.

2. The Photoresist Thermal Expansion Lift-off Technique

In light of the improved results obtained by thermal cycling in the conventional lift-off method discussed in the last section, it was felt that perhaps even greater improvements could be realized if this concept was expanded. Namely, if the metal was deposited on the substrate while the substrate (including the patterned photoresist layer) was below room temperature, and after removal of the substrate from the vacuum chamber induce the same heat treatment cycles used earlier, then a microcrack should be generated at the base of the metal (thinnest point) due to the thermal expansion properties of the photoresist layer.

The experimental set-up used to insure deposition of thermally evaporated aluminum while maintaining the substrate at temperatures below room temperature is illustrated in Figure 26. Temperature transfer from the liquid nitrogen container to the substrates (back-side) was through a rather massive aluminum disk plate as shown. Generally, the coolant holder containing only a small amount of liquid nitrogen was placed in position just prior to closing the vacuum chamber and roughing the system down. This prevented moisture from accumulating on the wafers and the surrounding parts undergoing

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this temperature decrease. The liquid nitrogen evaporated away during the roughing process, however the temperature transfer time constant was sufficiently short to cool the wafers before high vacuum levels were reached. A curve of the substrate temperature as a function of time in the vacuum chamber, as measured using a copper-constantine thermal couple in intimate contact with the substrate, is shown in Figure 27. At the time of metal deposition, the wafers were still below 0°C. This low temperature of the substrate at the time of metal deposition did not noticably alter the characteristics of the deposited metal in terms of adhesion, thickness, smoothness, etc.

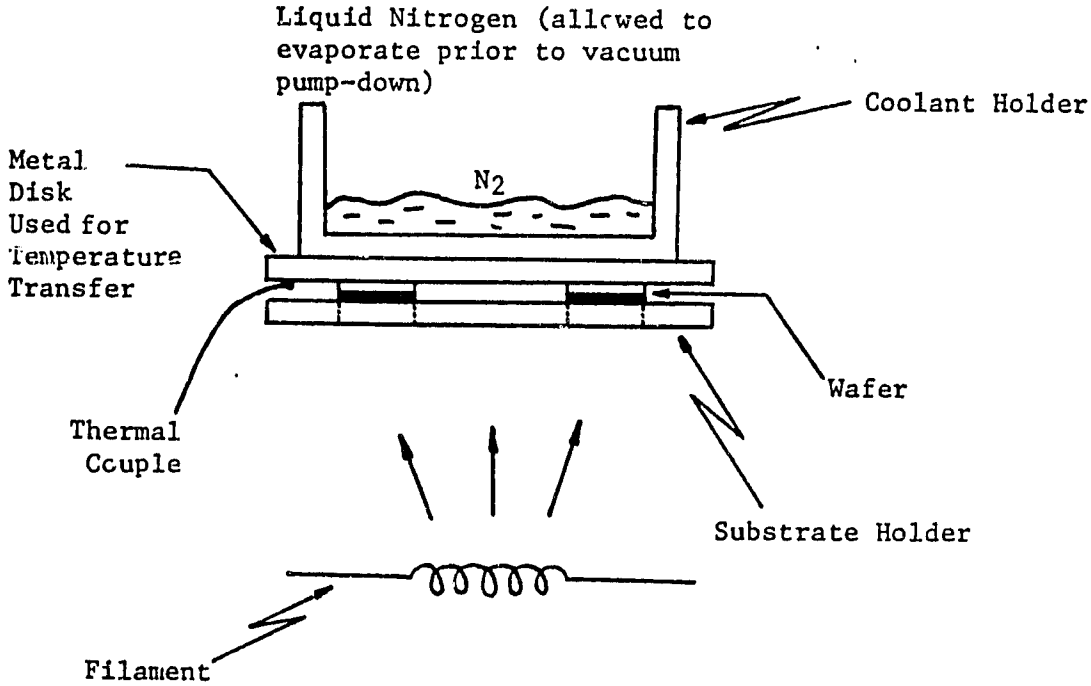

Figure 26. Experimental set-up used to deposit metal on wafers below room temperature.

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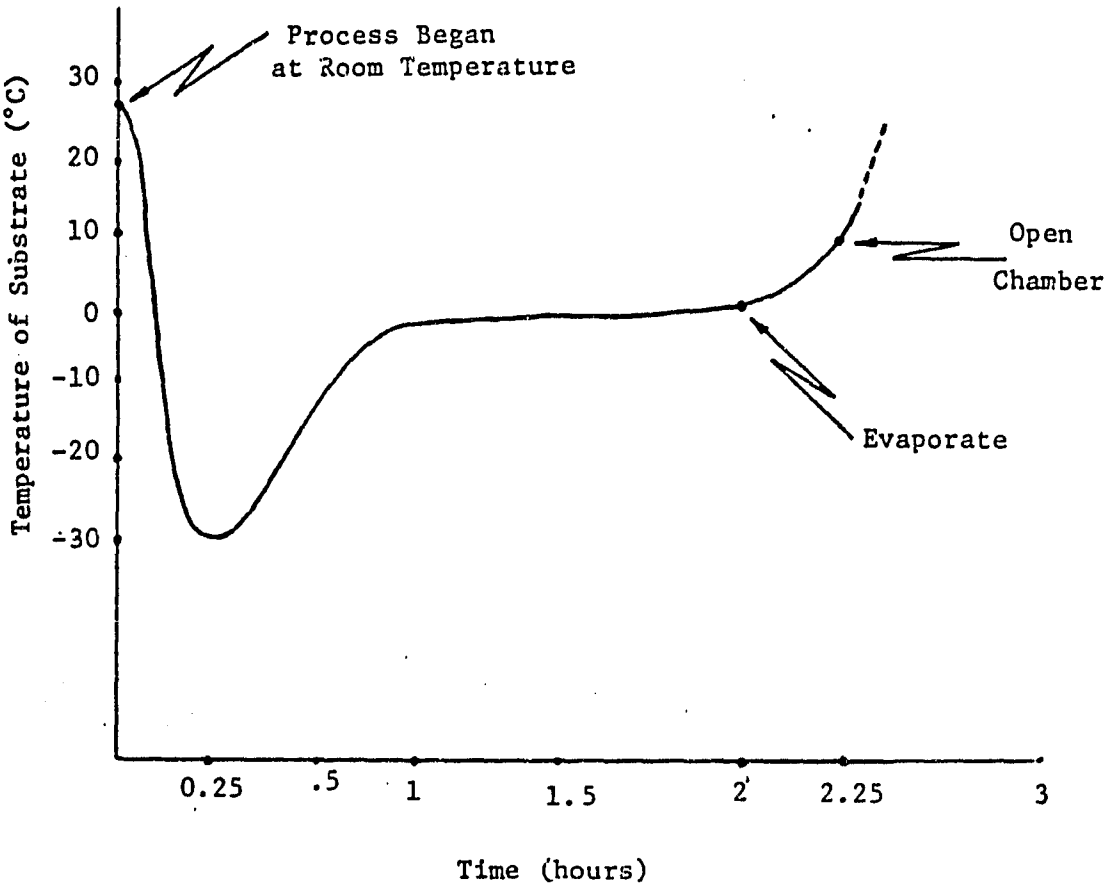

Figure 27. Thermal stress curve experienced by the wafers during below room temperature deposition.

Two Shipley positive photoresist were attempted, namely AZ1350J and AZ 111, at spin speeds of 2000, 4000 and 6000 rpm for 20 seconds. Metal deposited on the AZ 111 could not be lifted off in a patterned fashion, typically all metal was removed. Lift-off solvents attempted included AZ Remover 1112A, AZ Developers Number 311 and 351, and acetone. All attempts to lift-off sputtered metal were unsuccessful. Considerably improved results were obtained by not post-baking the

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positive photoresist layer after patterning, but instead, going directly to the metal deposition chamber.

Figure 28 illustrates the optimum results obtained by spinning AZ1350J on the wafer at 2000 rpm and patterning. No heat treatment was utilized after metal deposition and the metal was lifted ultrasonically in AZ Remover 351. Wafers having photoresist spun on them at 3000 and 4000 rpm could not be lifted.

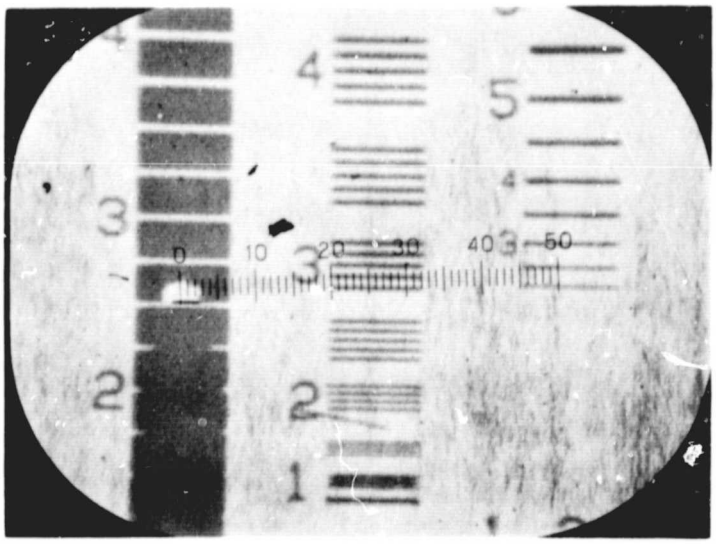

Figure 28. Lift-off of wafer having 2000 rpm AZ1350J cold metal deposition with no post heat treatment.

It was felt that a considerably better lift-off could be obtained if the cold metal deposited wafers were exposed to thermal heat cycling prior to immersion in the resist solvent. The wafer shown in Figure 29 used 2000 rpm AZ1350J resist and after cold metal deposition was placed in an oven at 230°C for 10 minutes in an air ambient.

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Notice how the photoresist bubbled and flowed under the metal layer. A better photograph illustrating this photoresist reflow is shown in Figure 30 for another wafer having undergone the same thermal process.

Figure 29. Metal distortion and bubbling effects due to placing wafer in oven at 230°C for 10 minutes after cold metal deposition.

A number of different procedures were attempted in order to render a good lift-off pattern. The "best results" were obtained using the following process:

- Use AZ1350J resist, spin speed at 2000, 4000 and 6000 rpm.
- Prebake at 80°C for 30 minutes
- Expose for 15, 12 and 10 seconds for resist applied at 2000, 4000 and 6000 rpm, respectively

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- Develop in 2 parts H_2O, 1 part AZ351 developer
- Deposit metal using cold thermal evaporation process
- Post bake for 30 minutes at 110°C in nitrogen ambient
- Lift metal ultrasonically in AZ Remover1112A at 40°C .

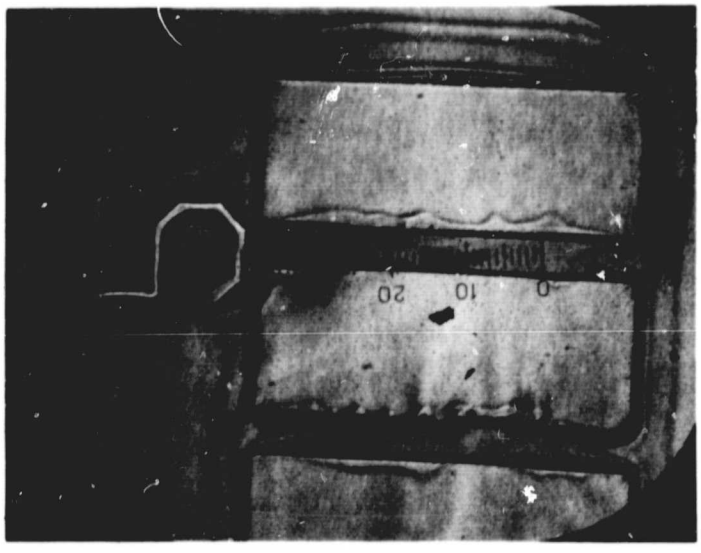

Figure 30. Wafer showing reflow of AZ1350J photoresist under cold deposited thermally evaporated metal after exposure to 230°C air ambient oven bake for 10 minutes.

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Typical results obtained using this procedure are shown in Figure 31 for metal thickness of 4000 Å. Also, a scanning electron micrograph is shown in Figure 32 of a cross-sectional view of a wafer just after metal deposition. The metal thickness here is approximately 2500 Å and the photoresist thickness is 2.8 microns. No microcrack is noticeable from this micrograph resulting from the cold metal depositon process. Microcrack generation therefore comes about as a consequence of the post heat treatment process and also lifting in a heated solvent.

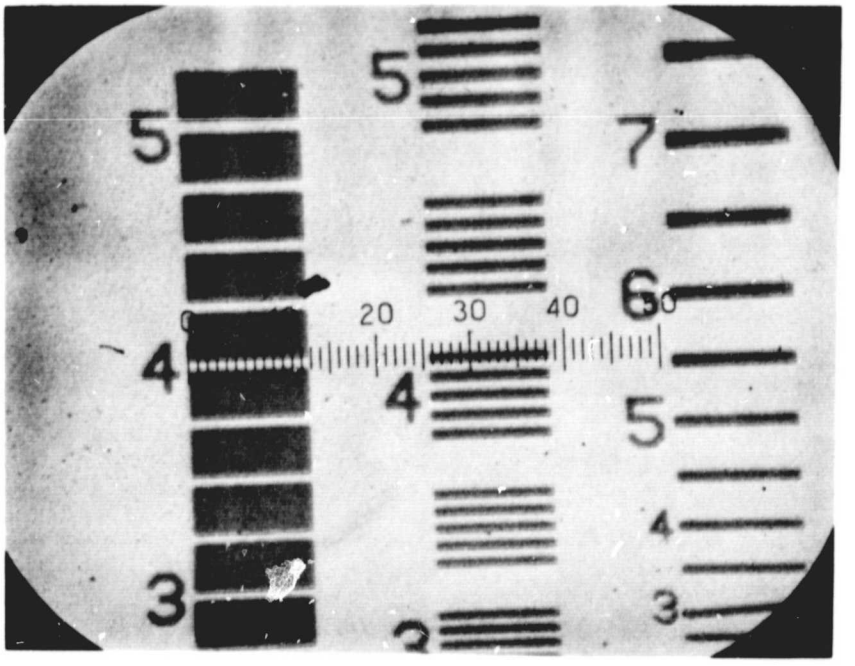

Figure 31. Wafer pattern obtained using "best results" procedure in the thermal expansion technique. AZ1350J was spun on at 4000 rpm.

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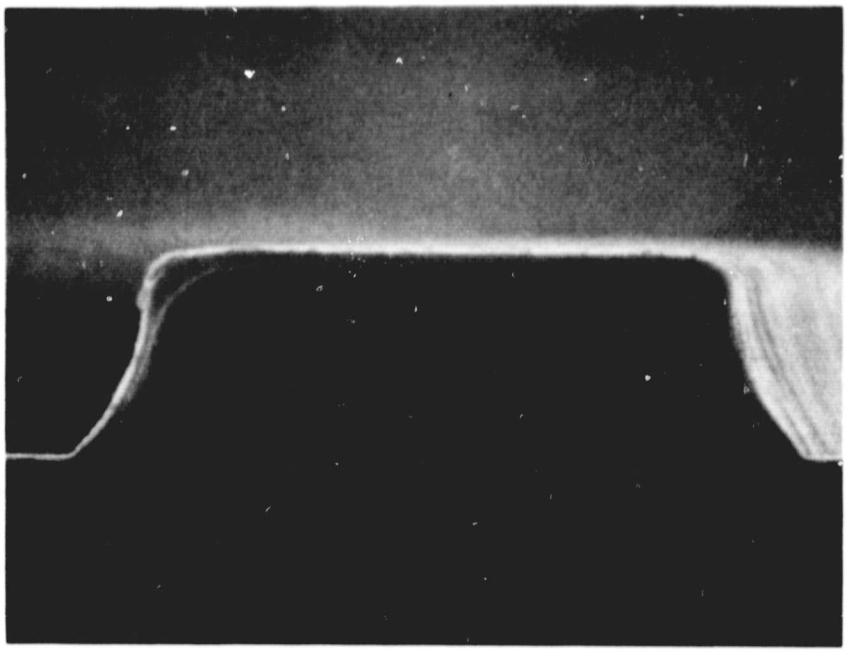

Figure 32. Scanning electron micrograph illustrating absence of microcrack after cold metal deposition and before heat treatments. Magnification 8500X.

The primary limitations associated with the thermal expansion lift-off technique include the following.

a. It is inconvenient to cool wafers during the metal deposition step

b. The thermal expansion of the photoresist due to cold metal deposition alone is insufficient to form a microcrack

c. Even after heat treatments and lifting in an ultrasonic solvent which is heated, the metal pattern is often not well defined or reproducible.

3. Photoresist Stencil with Negative Sidewalls Due to Chemical Treatment

As was discussed in the last section in connection with Figure 8, soaking a positive photoresist-coated substrate in chlorobenzene will modify the development rate of the upper surface from that of the bulk resist film thereby rendering a negative or overhanging slope. Using AZ1350J positive resist spun on the wafer at 2000 rpm, a 85°C prebake for 30 minutes is undertaken prior to exposure using the desired mask and soaking the wafer in chlorobenzene at room temperature. After a 15 minute soak, the wafer is then post-baked at 85°C for an additional 30 minutes and developed by dipping the wafer in AZ351:H_2O solution until the desired undercut pattern is obtained. The photoresist stencil obtainable using this technique is shown in Figure 33. Here, the resist is approximately 1.5 microns thick with 0.5 micron overhanging lips. In Figure 34, thermally evaporated metal has been deposited on another sample approximately 2500 Å thick. This metal lift-off yield excellent results.

4. Lift-off Using an Auxiliary Layer of Polyimide for Stencil Formation

The use of an auxiliary layer in forming a lift-off stencil was illustrated in Figure 10 of the last section. Since one of the tasks of this research effort is to evaluate polyimide as an inner layer insulator or dielectric in double layer metal systems, it was soon discovered in processing polyimide films that a photoresist stencil could be generated by over-etching the polyimide in attempting to pattern it. This process is shown schematically in Figure 35.

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Figure 33. Photoresist lift-off stencil resulting from chlorobenzene soaking process. Photoresist thickness is approximately 1.5 microns having 0.5 micron overhanging lip.

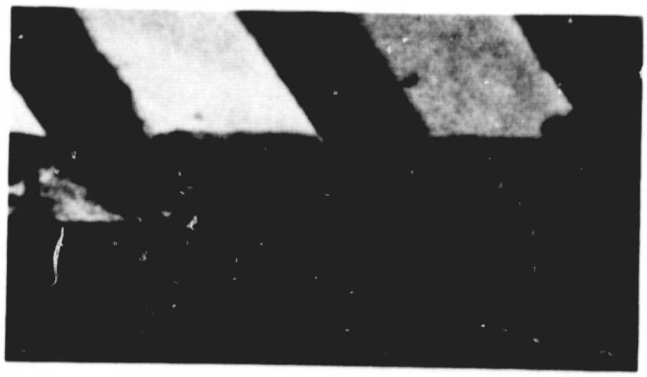

Figure 34. Metal deposition on a chlorobenzene soaked resist stencil. Metal thickness is approximately 2500 Å.

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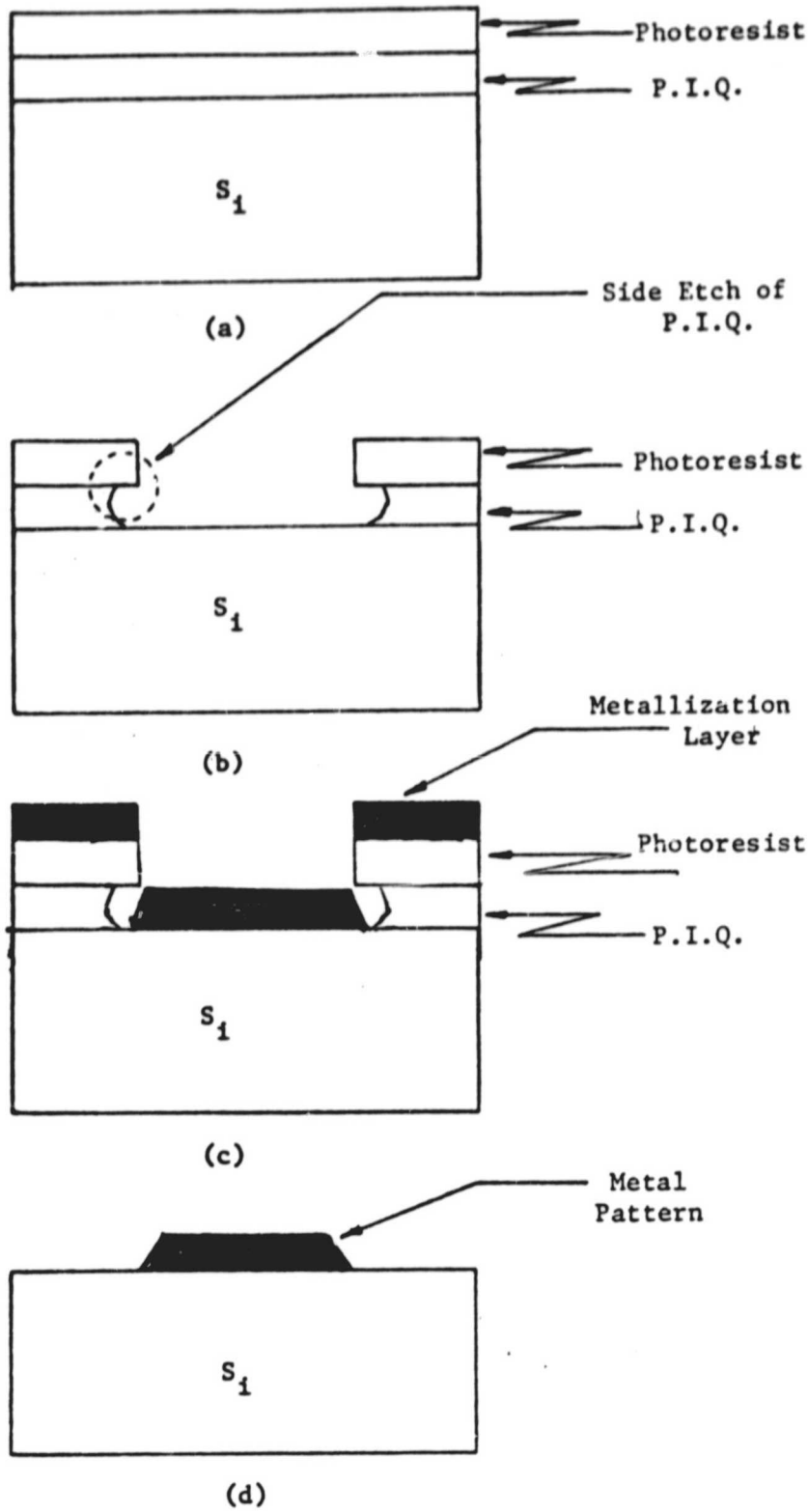

Figure 35. Process used in forming lift-off stencil by utilization of polyimide as an auxiliary layer.

Initially, the polyimide is applied to the wafer and partially imidized (precured). The thickness of the resulting polyimide layer is a function of the deposition spin speed, and the viscosity of the starting material which can be controlled using appropriate thinning or carrier solutions. Next, positive photoresist is applied to the polyimide layer which will act as a mask in patterning the polyimide and prebaked. The composit materials shown in (a) are then exposed in a mask aligner and developed. The photoresist developer is a strong basic solution and acts to etch the polyimide layer at the same time photoresist development is undertaken. If over development is allowed to occur, a negative stencil shown in (b) prevails. This stencil is then post baked prior to loading in the metal deposition chamber. After metal deposition occurs, the polyimide-photoresist stencil is removed in a suitable solvent as shown in (c) and (d).

Both Dupont (PI-2550, PI-2545 and PI-2555) and Hitachi (PIQ-13) varieties of polyimides were investigated. A detailed description of polyimides, including their properties, processing characteristics, strengths and weaknesses, etc., will be discussed in the next volumn of this report dealing with double layer metal processes. In order to promote adhesion of these polyimides to a silicon or silicon dioxide substrate, it is necessary to apply a coupling agent.

The first polyimide type investigated was Dupont PI-2550. The Dupont adhesion promoter consist of a very small percentage (0.01 to 0.02%) of the coupling agent VM651 in either methanol or water. This adhesion promoter is applied to the wafer on a spinner like photoresist

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and baked for 10-12 minutes at approximately 130°C. The polyimide's viscosity can be adjusted by using a Dupont thinner solution T-8035. The carrier solution for this polyimide is N-methl-2-pyrrolidone (NMP) and this may also be used as a thinner. The prebake (pre-imidization) process for the polyimide coating is very important and typically consisted of a 50, 80 and 120°C temperature cycling for 30 minutes each.

Initial problems were experienced with the coupling agent. A mixture of VM-651 in methanol had a tendency to bead under the polyimide layer as shown in Figure 36. Neither the polyimide nor the photoresist would adhere to these beaded areas. An attempt to mix the coupling solution in water also gave undesirable results as shown in Figure 37. The polyimide did not coat the wafer uniformly and had amplified beads as shown which had detrimental effects on the patterning process.

Figure 36. Beading effect in the polyimide coating due to small coupling agents droplets using VM651 in methanol.

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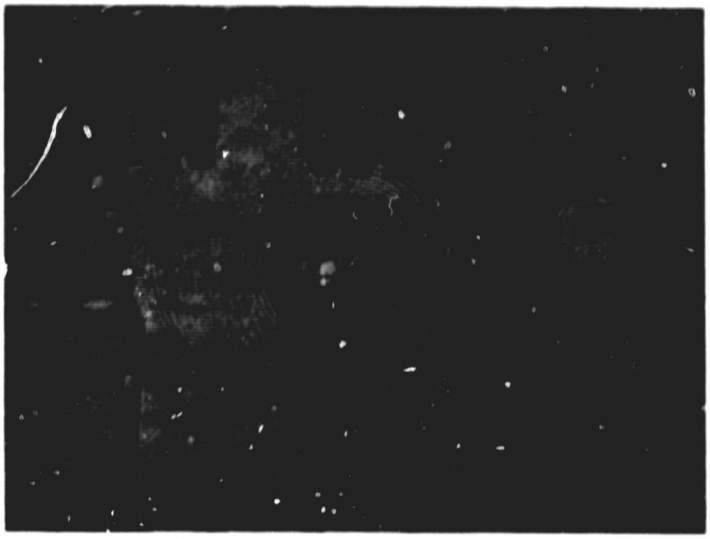

Figure 37. Amplified beads obtained when the coupling agent is mixed in water instead of methanol.

As will be indicated later, coupling agent problems of these type can be eliminated by proper mixture of the dilute agent solutions and also by using a pre and post cleaning process (ie, the wafer is first cleaned with methanol alone, then the coupling agent is applied, and lastly, another methanol clean is undertaken).

Another problem experienced in this early investigation of PI-2550 polyimide was the generation of a "fish-eyes". This localized mounding effect within the polyimide came about by allowing the wafers to sit in a wafer holder for several minutes after spinning the polyimide on, at room temperature and ambient.

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This "fish-eye" effect is shown in Figure 38, which appears to be a mound or collection of polyimide several microns in height as well as across its base and coming to a rather sharp peak at its top. The size of these "fish-eyes" varied considerably across the face of the wafer. A convection oven, IR lamp, or photoresist belt furnace when used to dry the polyimide immediately after spinning on and prior to applying the photoresist eliminated these fish-eyes.

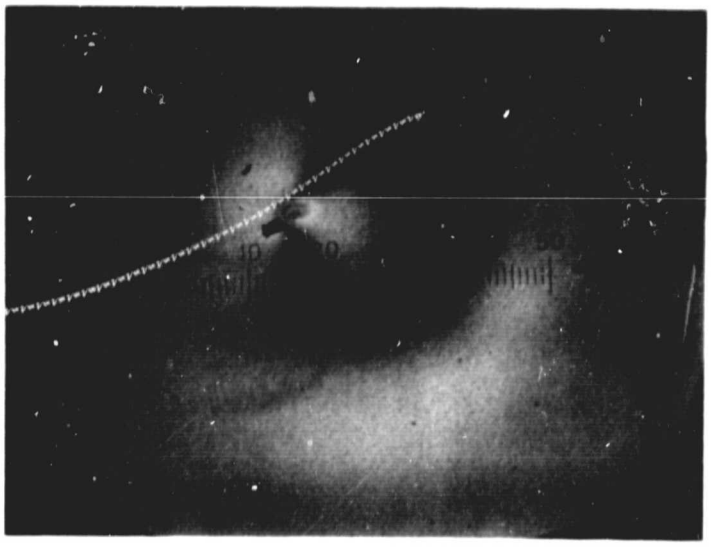

Figure 38. "Fish-eyes" observed in the polyimide layer.

Another problem encountered in patterning the polyimide layer had to do with the cleanliness of the initial substrate material. If the substrate did not undergo a cleaning procedure prior to polyimide deposition, the polyimide would adhere to these unclean

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spots on the wafer as shown in Figure 39. Simple steps such as a quick $HF:H_2O$ dip and dehydration just prior to depositing the polyimide would greatly assist in clearing up this problem

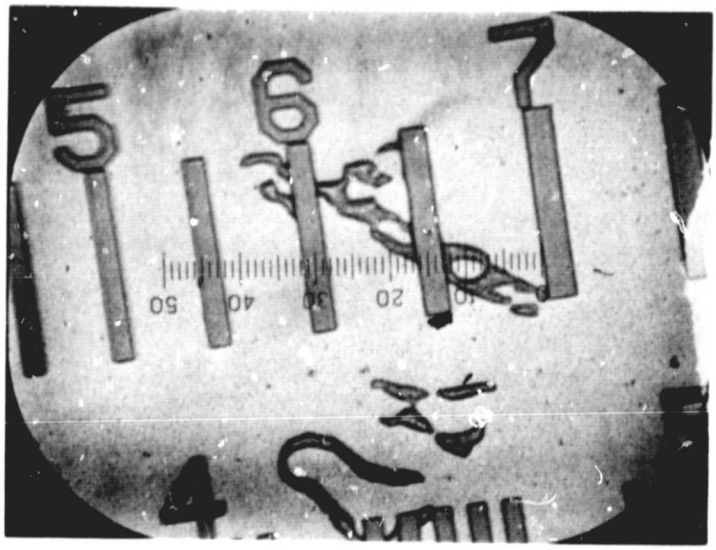

Figure 39. Residue of polyimide on wafer due to insufficient substrate pre-cleaning process.

The procedure used to produce the optimum undercut stencil using Dupont polyimide PI-2550 is as follows:

a. Mix equal parts Dupont polyimide PI-2550 and Dupont thinner T-8035 and spin coat the wafers at 6000 rpm for 20 seconds.

b. Pre-imidize the polyimide at 50°C for 15 minutes and then at 80°C for 30 minutes.

c. Spin coat Shipley AZ1350J on wafer at 4000-6000 rpm for 20 seconds

d. Prebake the photoresist at 80°C for 30 minutes

e. Expose the photoresist to ultraviolet light using the photoresist test mask in the contact mask aligner for 10 seconds.

f. Develop the photoresist and pattern the polyimide in 3 parts H_2O and 1 part Shipley AZ351 developer for break plus 8-10 seconds. ("Break" is the time required to clear the scribe line of photoresist and polyimide.)

g. Postbake the photoresist/polyimide coating at 110°C for 30 minutes.

An example of a wafer processed as described above is shown in Figure 40. This wafer was overetched more than necessary in order to form a good lift-off stencil, however, the over etching was required in order to demonstrate the effect in a photograph.

A wafer having this lift-off stencil was placed in the thermal (filament) evaporation metal deposition system and 5000 Å of pure aluminum was deposited. A photograph of the metal coated wafer is shown in Figure 41. Upon wafer removal from the deposition system, the metal was lifted off using Shipley AZ Remover 1112A in an ultrasonic bath at room temperature (25°C). The definition of the resulting metal was very good as illustrated in Figure 42.

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Figure 40. Photomicrograph illustrating the polyimide undercut resulting from over-developing the composit photoresist/polyimide layer. The width of each bar is 0.5 mils or 12.5 microns.

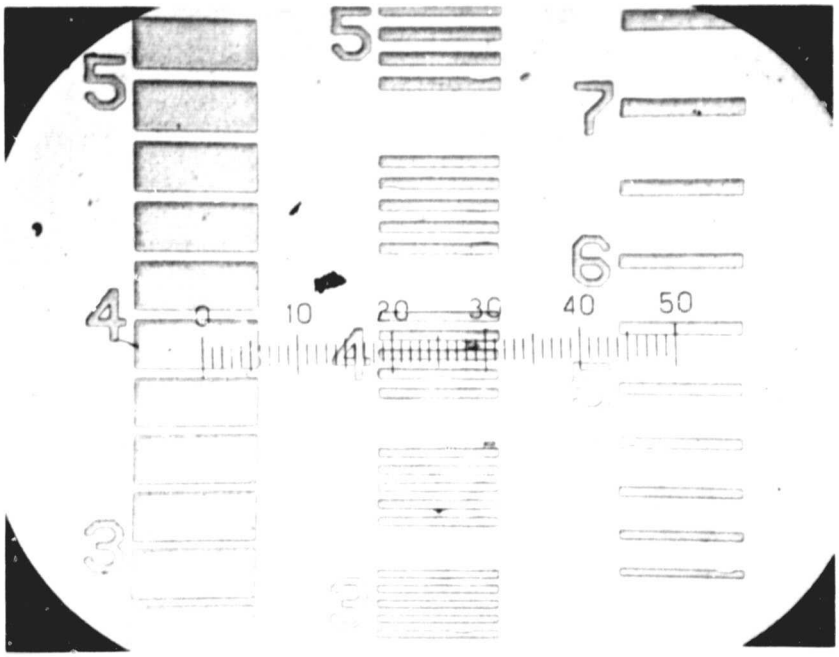

Figure 41. Thermally evaporated aluminum coated wafer over stencil prior to lift-off. Metal thickness is 5000 Å..

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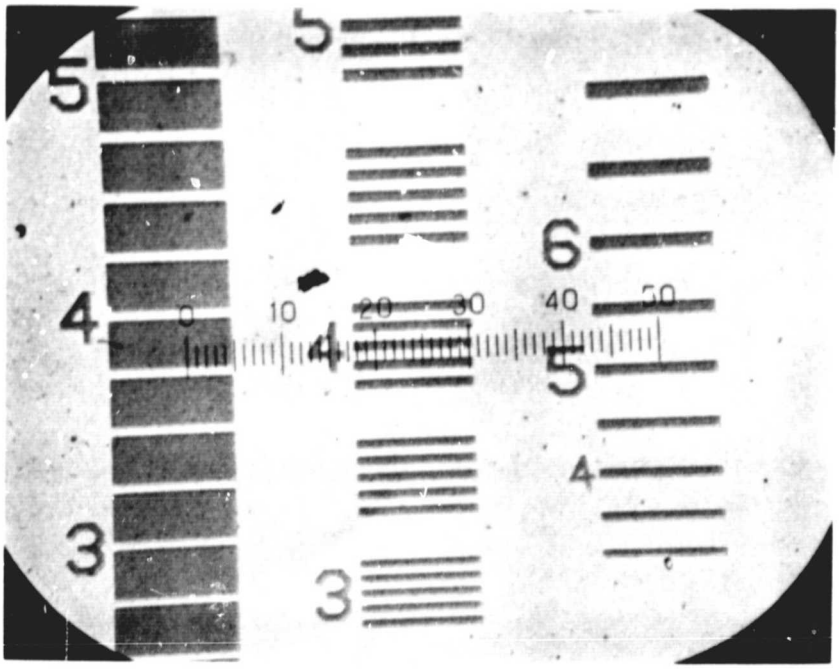

Figure 42. Same wafer shown in Figure 41 after lift-off using AZ Remover 1112A in ultrasonic bath at room temperature.

Since the results obtained using the thermal evaporation method exhibited such good definition, a wafer having the same stencil pattern was next coated with aluminum alloy 6061 to a thickness of 2500 Å using the dc sputter system. To insure minimum substrate heating during the deposition, the sputter gun was cycled on and off at a two minute rate until the desired metal thickness was obtained. Again, Shipley AZ Remover 1112A was used to lift-off the metal over the stencil, and the results obtained are shown in Figure 43.

A cross-section of a 0.2 mil stencil bar was mounted for SEM analysis. Figure 44 illustrates a scanning electron micrograph of

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this cross-section. The base polyimide layer is approximately 5000 Å thick for this particular sample and the masking photoresist layer is approximately 1.8 microns thick. The aluminum alloy shown on top of the stencil is about 2500 Å in thickness, but thin enough to generate a sizable microcrack for solvent penetration at the base of the stencil. For a thicker polyimide coating, a considerably thicker metal layer may be realized and still accomplish lift-off having excellent definition.

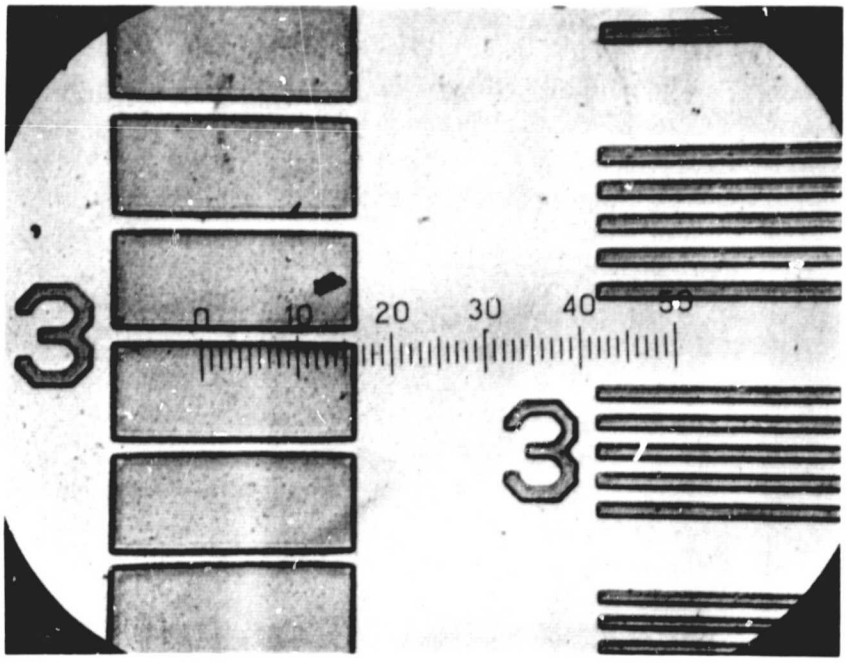

Figure 43. Lift-off pattern obtained using dc sputter deposited aluminum alloy. Metal thickness is approximately 2500 Å.

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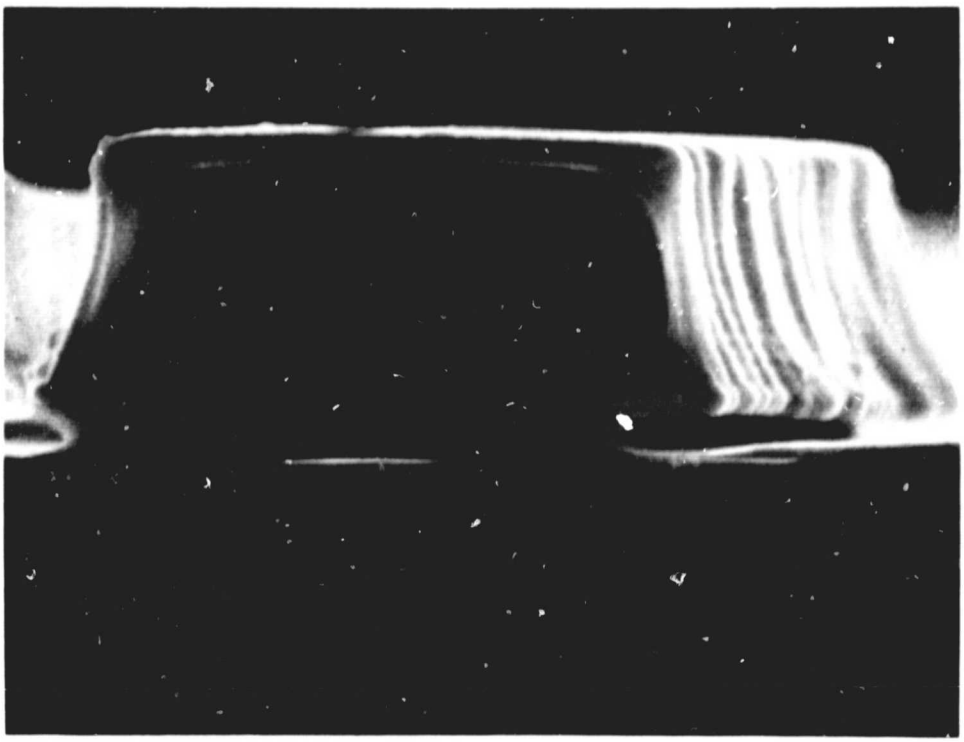

Figure 44. Scanning electron micrograph illustrating cross-section or dc sputtered aluminum alloy deposited over a photoresist/polyimide lift-off stencil. Notice the large (3000 Å) micro-crack at the base of the stencil.

At the same time SEM analysis of the sputter metal was being investigated, another sample having 5000 Å thermal evaporated patterned metal was observed as shown in Figure 45. Here, the metal thickness is approximately 0.5 microns. The width of the left-hand bar is 1.7 microns at the base, and 1.3 microns at the top. The metal side walls are sloped nicely which should allow excellent step-coverage in subsequent processes. The width of the right-hand

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bar is slightly less than 0.5 microns, at its base. Hence, it has been demonstrated that submicron metal lines can be realized using this lift-off technique.

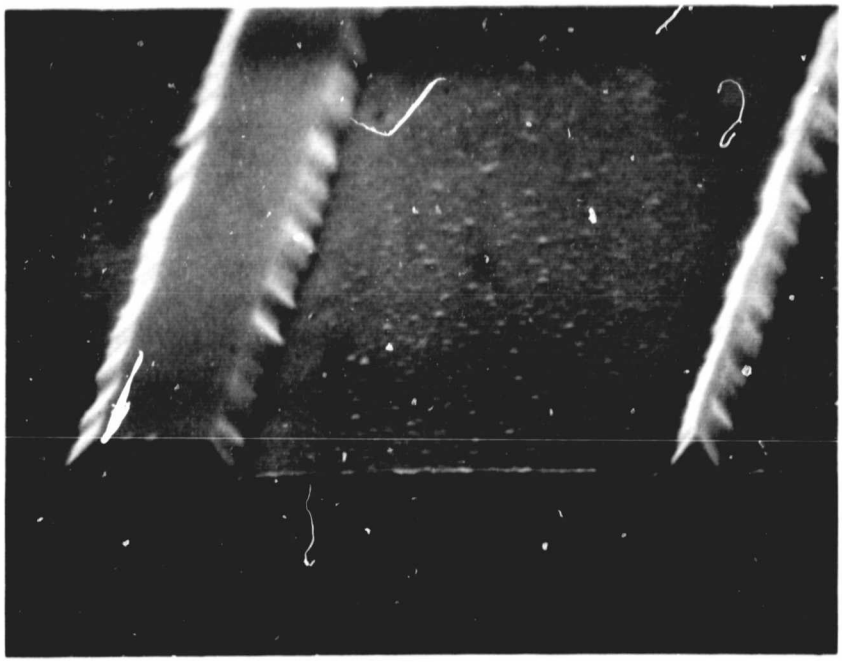

Figure 45. SEM micrcgraph of patterned thermal evaporated metal using photoresist/polyimide stencil technique. Magnification is 11,300X.

The main advantages in using the photoresist/polyimide stencil lift-off technique are that it involves only one additonal process step (deposition of the polyimide) over the conventional photoresist technique of section 1, either thermal evaporated or dc sputtered films can be used, and the allowable thickness of the resulting deposited film is a function of the polyimide layer thickness, which is a controllable parameter.

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5. Lift-Off Using An Auxiliary Layer of Silicon Dioxide for Stencil Formation

This lift-off procedure is very similar to that discussed in the last section except instead of using polyimide as an auxiliary layer, silicon dioxide is used. The silicon dioxide layer can either be thermally grown in a steam or dry oxygen ambient at elevated temperatures or deposited using a chemical vapor deposition (CVD) process. The photoresist layer is deposited over the SiO_2 layer and patterned. Then the oxide layer is etched using a buffered HF solution until the desired undercut is realized as shown in Figure 46.

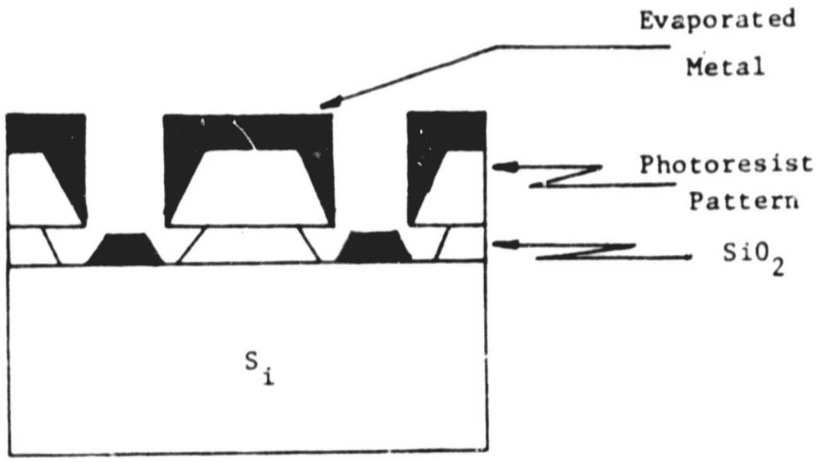

Figure 46. Schematic representation of photoresist/silicon dioxide stencil formation for metal lift-off.

Since in this stencil formation process, the silicon dioxide layer is removed from portions of the silicon substrate, this technique

would allow patterning metal layers which are to be used to make ohmic contact to the silicon in an integrated circuit realization. This method may be more desirable than patterning the metal layer using the conventional technique of depositing the metal over the whole wafer and then etching away the undesired areas through a photoresist mask. This metal etching involves harsh wet chemical or dry plasma processes which can prove detrimental to sensitive surfaces like the gate regions of MOS circuitry.

In this investigation, the silicon dioxide layer was thermally grown using a 10 minute dry O_2, 20 to 80 minute HCl steam and followed by an additional 10 minute dry O_2 process at 1100°C. Shipley AZ1350J positive photoresist was used to pattern the silicon dioxide, which was deposited at 6000 rpm. The oxide was etched using a buffered oxide etchant for 10-15 seconds beyond break (clearing the scribe lines) to insure adequate undercutting of the photoresist layer.

The thermally grown silicon dioxide growth curves for temperatures of 900, 1000 and 1150°C in both dry oxygen and steam (having HCl additive) are shown in Figures 47 and 48, respectively. Oxide thicknesses were monitored using a laser based ellipsometer.

Very good results were obtained using this auxiliary layer stencil for both thermal evaporated and sputtered metal films. The micrograph shown in Figure 49 illustrates the quality of the lift-off pattern obtained for 5000 Å sputtered aluminum alloys. Again, the metal was lifted using AZ Remover 1112 A in an ultrasonic bath for just over 5 minutes at room temperature.

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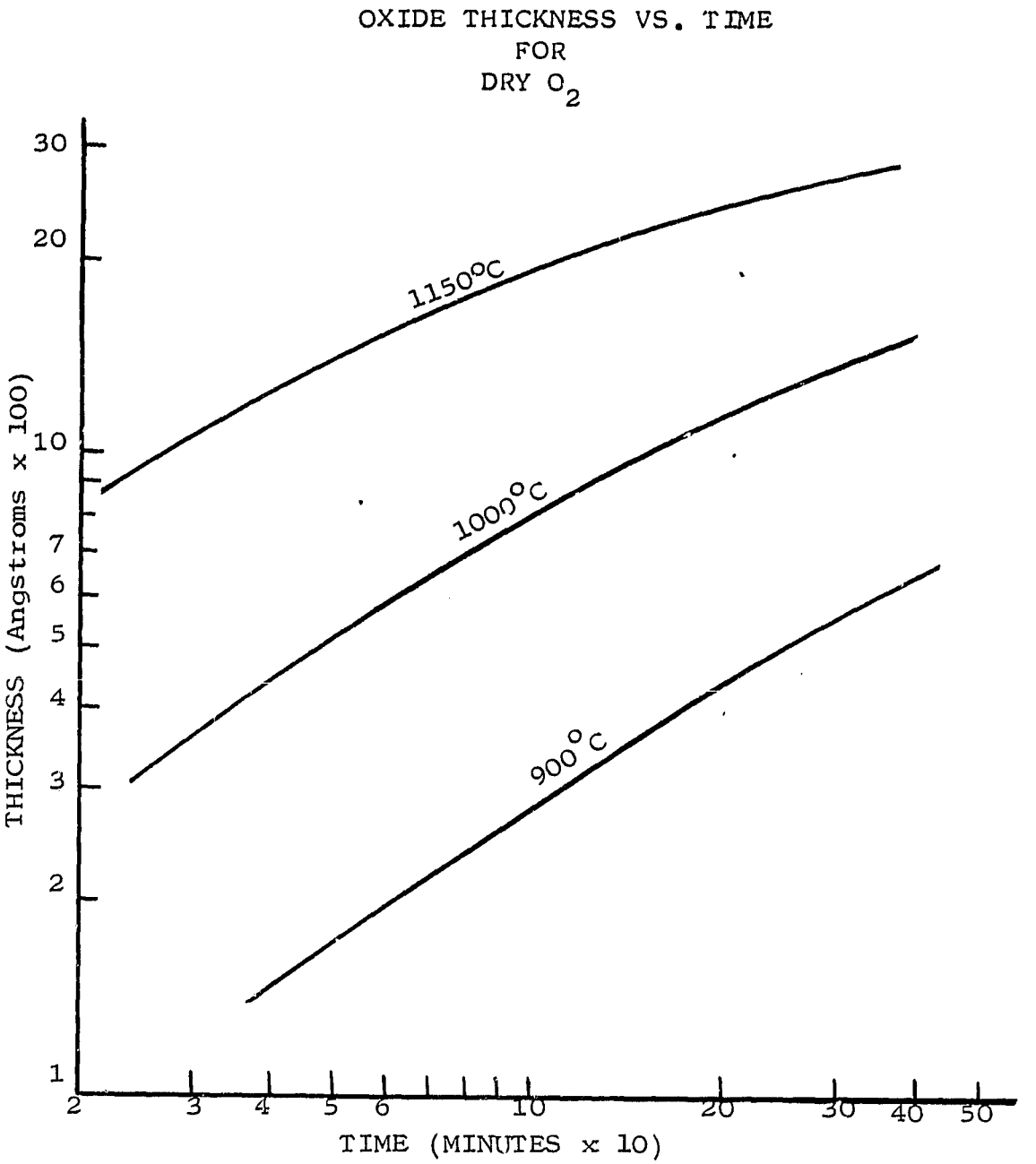

Figure 47. Silicon dioxide growth curves on <111> silicon for dry O_2 as a function of time and temperature.

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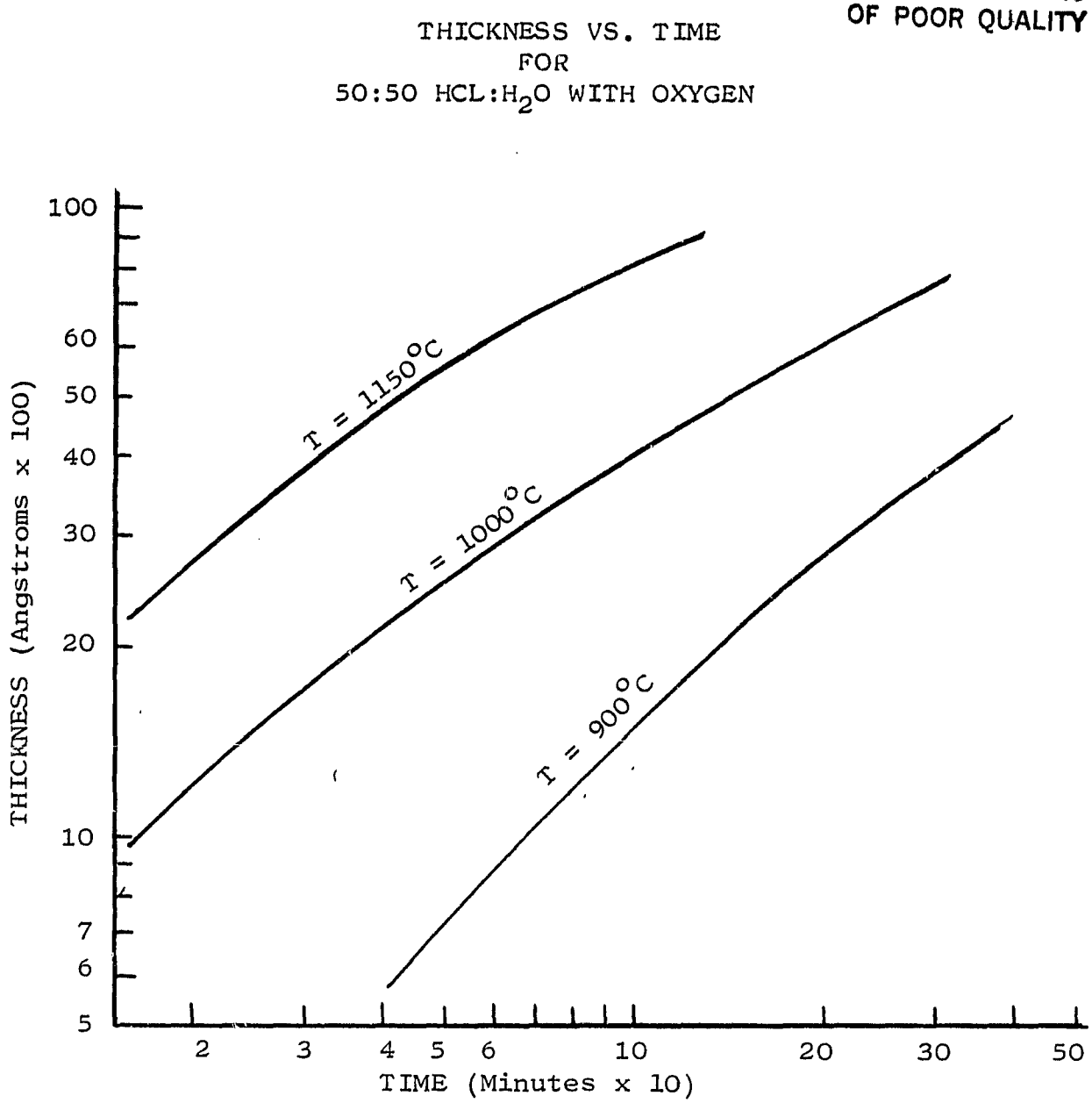

Figure 48. Silicon dioxide growth curves for HCl: steam on <111> silicon as a function of time and temperature.

Magnification of smaller dimension lift-off patterns are shown in Figure 50. The bars directly below the numbers (in tenths of a mil) correspond to that dimension. The bars between the numbers

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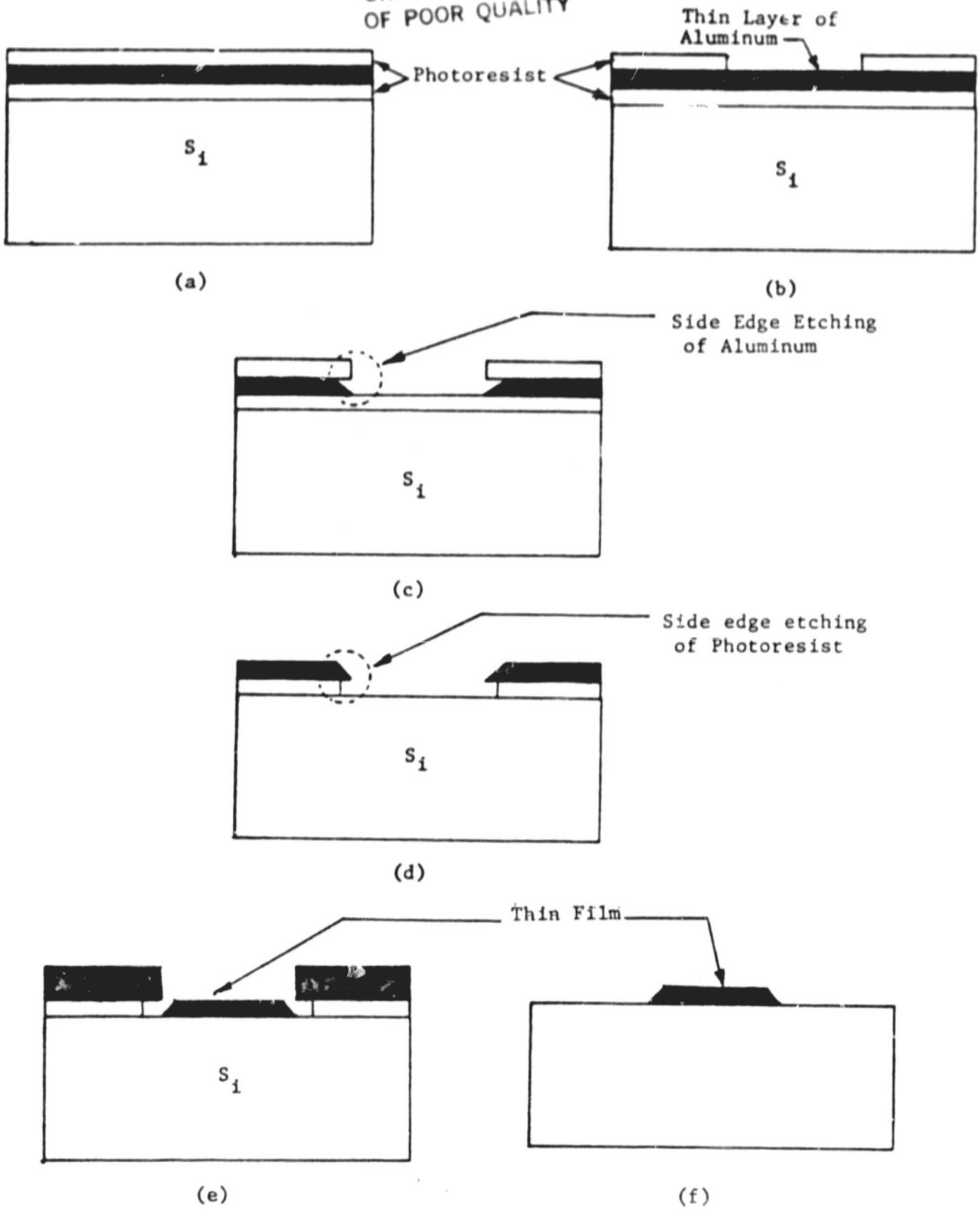

Figure 51. Process steps involved in yielding a photoresist-aluminum-photoresist stencil.

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IV. CONCLUSIONS

A thoroughal review of metal (or dielectric) lift-off processes as used in the semiconductor industry today to realize high density very large scale integrated systems has been undertaken. Some of these processes are quite simple in nature (ie, chlorobenzene soak cycle) while others involve the addition of several very costly prc ing steps. A simple, reliable and reproducible lift-off procedure is required to meet todays interconnection patterning needs.

Experimental realization of a few of these lift-off techniques was undertaken. In addition, several novel processes were attempted with varying degrees of success. While it appears that the photoresist thermal expansion lift-off technique will realize little to no impact on the semiconductor industry, at the same time, the use of an auxiliary layer of polyimide to form a lift-off stencil offers considerable promise.

At least a portion of the work reported here has been published or presented elsewhere with due credit given to NASA sponsorship (34,35,36).

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