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FINAL REPORT

AUTONOMOUS INTEGRATED RECEIVE SYSTEM (AIRS)

REQUIREMENTS DEFINITION

VOLUME II. DESIGN AND DEVELOPMENT

PREPARED FOR

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1.0 INTRODUCTION AND SUMMARY

1.1 Overview and Objective

The objective of this Phase I study effort is to develop the functional requirements and specifications for an Autonomous Integrated Receive System (AIRS) for use as an improvement in the current Tracking and Data Relay Satellite System (TDRSS), and as a receiving system in the future Tracking and Data Acquisition System (TDAS). The AIRS provides improved acquisition, tracking, bit error rate (BER), RFI mitigation techniques, and data operations performance compared to the current TDRSS ground segment receive system. This report and the accompanying specification and baseline design Vol. IV serve to document LinCom's effort in the AIRS Phase I study. A computer model of the AIRS as defined under the Phase I study is dveloped in a Phase II study. It is used to provide simulation results predicting the performance of AIRS. This effort is documented in Vol.III of this Final Report.

1.1.1 Current TDRSS Ground Segment Receive System

The current TDRSS ground segment receive system consists of a string of subsystems in four separate units as shown in Figure 1-1. Each subsystem in the chain serves a specific purpose and essentially functions independently of other subsystems. While this structure enables a simple partitioning for the implementation of the subsystems as black boxes, the end product is a system that frequently delivers suboptimal performance and operational inconveniences.

1.1.2 The AIRS Concept

In an integrated receiver concept, the subsystems are designed to functionally interface with one another. A conceptual approach of how this can be accomplished is depicted in Figure 1-2. The monitor and

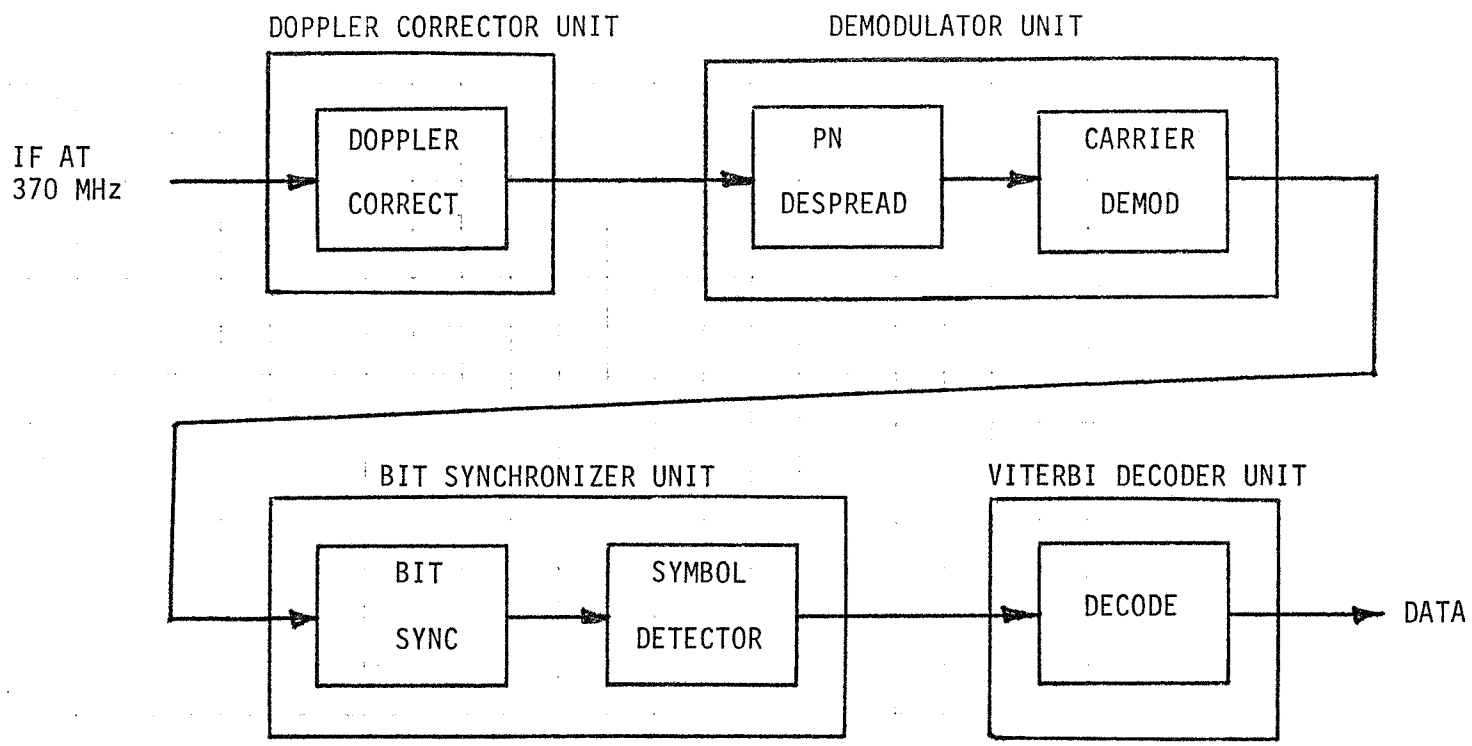

Figure 1-1. Functional Block Diagram of Current TDRSS Receive System.

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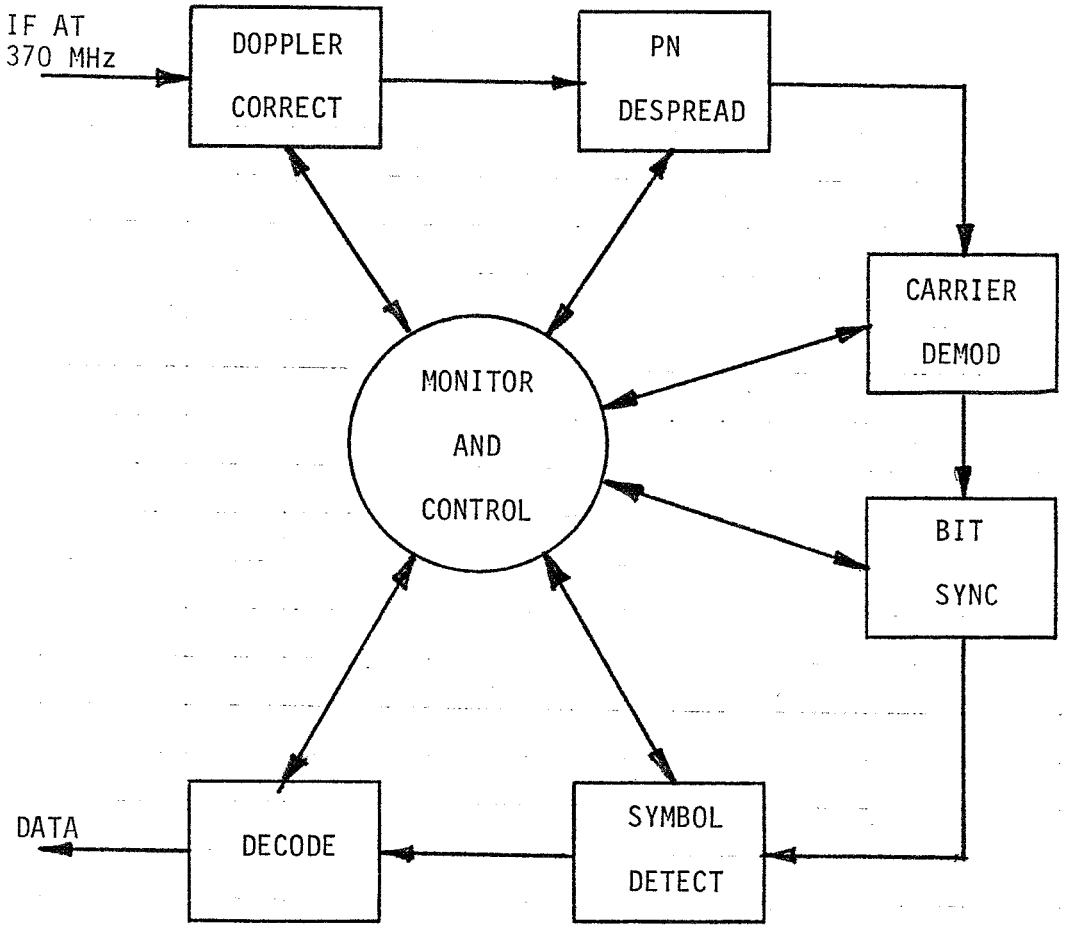


Figure 1-2. Conceptual Block Diagram of AIRS.

control center is basically an information clearing house for the operational status of each subsystem. It collects pertinent information from each subsystem, analyzes the information, and instructs the individual subsystems to set their modes and parameters accordingly so as to achieve desired performance.

Because of the increased interplay between the subsystems, the traditional blocking of distinct individual subsystems such as shown in Figure 1-2 will become less apparent. A more natural functional partitioning of the AIRS resembles Figure 1-3. In this model, the signal processor is subdivided into an analog and a digital portion. The received IF signal is first down-converted and (coarse) Doppler compensated to a suitable second IF. The bulk of the signal processing is performed digitally--the main driver being the versatility inherent with digital processing, which provides an opportunity for implementing nearly optimum algorithms with infinitely adjustable parameters. The analog signal processing is primarily used in the pre-processing of the IF signal into a form suitable for analog-to-digital conversion. Certain processing involving extremely high speed/wide bandwidth operations will have to be performed using analog techniques.

The operation of the signal processor is controlled by the autonomous monitor and control system (AMC) which is really the intelligence center of the AIRS. It receives monitor signals from the signal processor, processes these signals, makes decisions, and configures the signal processor for optimal receiver performance by selecting the appropriate moding and processor algorithms. Using this scheme, the AIRS is basically adaptive in nature. It continuously perceives the received signal conditions and adjusts the signal

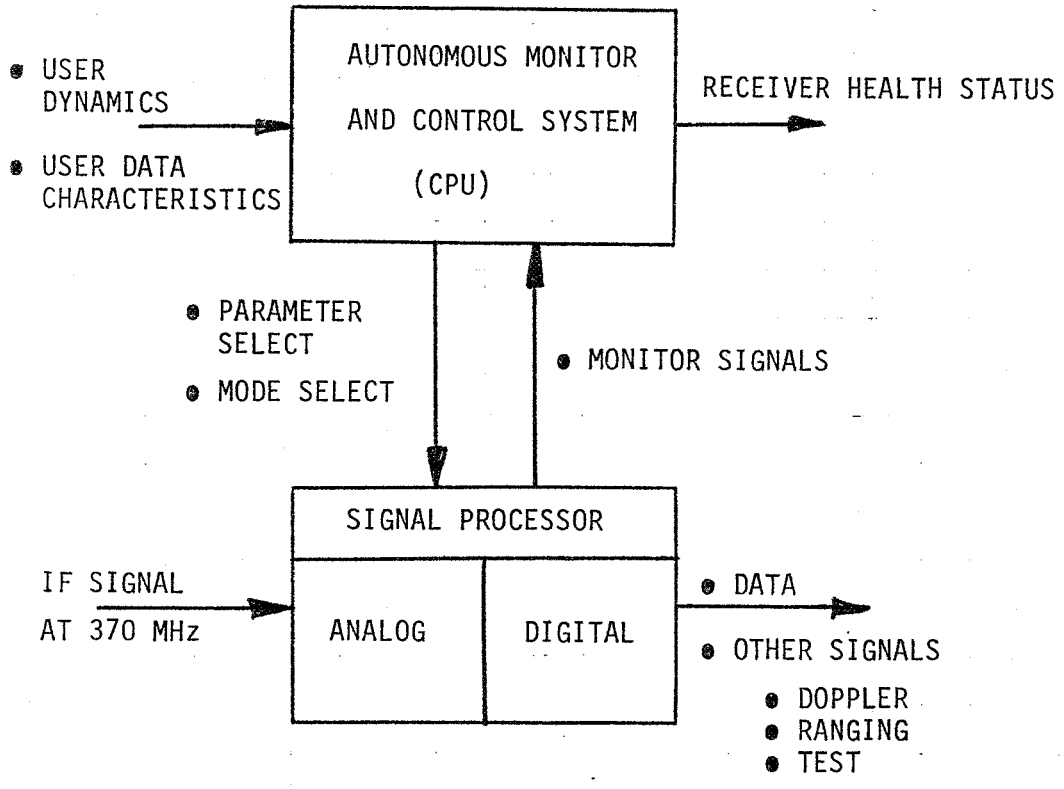


Figure 1-3. Simplified Functional Model of AIRS.

processing accordingly in a real time fashion; thereby, it is more tolerant to system anomaly. The AMC is also responsible for the hand shaking between the ground segment control and the receiver system. It accepts user dynamics predictions and designated receive data characteristics from the ground control on one hand and reports on the receive system health status on the other hand.

1.2 Key AIRS Features

The AIRS is designed to provide system peformance and data operations improvement over the current TDRSS capability. Performance improvement can be categorized as (a) relief from current TDRSS system waivers, (b) relaxation of some S-805 constraints and (c) additional capabilities not called for by S-805. Data operations improvement is achieved by the built-in intelligence and flexibility associated with a digital/CPU-based design. In this study, we concentrate on the AIRS concept as applied to the SSA link.

1.2.1 Performance Improvements

1.2.1.1 Relief From Current System Waivers and Exceptions

1.2.1.1.1 Waivers

Two current waivers can be eliminated by the AIRS design. They are addressed in Table 1.1 and are made possible by the coupled bit sync and carrier recovery implementation.

1.2.1.1.2 PN Code Acquisition Time

S-805 specified PN code time-to-acquire to be the mean time to search the entire PN code uncertainty. However, the TDRSS Users' Guide (STDN No.101.2) uses the following interpretation: "Time-to-acquire PN code assumes a Gaussian distribution of the predicted return link PN code epoch with the $\pm 3\sigma$ points defining the maximum PN search window

Table 1.1. Current System Waivers Relieved by AIRS.

WAIVER	PROBLEM	CAUSE	AIRS SOLUTION
• H-W 18: DG1 MODE 3 DATA FORMAT/I:Q POWER RATIO	• ACQUISITION • LOSS OF LOCK FOR I-CHANNEL	• SINGLE CHANNEL TRACKING (Q CHANNEL $<$600 Ksps, I OTHERWISE) • CROSS CHANNEL INTERFERENCE	• DUAL CHANNEL TRACKING IMPROVES EFFECTIVE LOOP SNR • DATA-AIDED LOOP SUPPRESSES INTERFERENCE AND REDUCES SQUARING LOSS
• H-W 19: SSA DG2 CODED USER MODULATION/ DATA FORMAT	• ACQUISITION PERFORMANCE • LOSS OF LOCK	• QUADRUPLING LOSS IN BALANCED QPSK CARRIER ACQUISITION/TRACKING LOOPS	• IMPROVED FLL IMPLEMENTATION EXTENDS FREQUENCY DETECTOR THRESHOLD • OPTIMUM ARM FILTER (I&D) IMPLEMENTATION MINIMIZES QUADRUPLING LOSS • THIRD-ORDER LOOP MINIMIZES STATIC PHASE SHIFT DUE TO DYNAMICS

corresponding to the user's maximum orbital uncertainty (±9 sec). Time-to-acquire performance for PN acquisition means n/2 of n acquisition attempts result in declared acquisition at the minimum acquisition EIRP within the time allocated for PN acquisition of the total acquisition time. The probability of correct acquisition for each of these n/2 declared acquisitions is 0.9." With the AIRS approach of parallel search, which provides a factor of 4-6 speed improvement, the original S-805 definition can be satisfied.

1.2.1.2 Relaxation of S-805 Constraints

1.2.1.2.1 DG-2 Unbalanced QPSK Data Rate Constraints

The S-805 (Table 9-2) DG-2 data rate requirement specifies that the higher power channel must be accompanied by higher data rate. This constraint results from the fact that the carrier demodulator operating independently of the data demodulator, must, on its own, differentiate between the I and Q channel by always tracking the strong channel. The data rate specification then simplifies the operating procedure and the demodulator implementation. In the AIRS scheme, the carrier loop is data-aided. Therefore, the demodulator can recognize the channels by their data rates as well as by their signal strengths. By the same token, the AIRS design eliminates the bit rate restriction that neither the I nor Q channel rate be within 25% of being an exact integer multiple of the other. In the proposed spec, the data rates need only be 5% apart.

1.2.1.2.2 Acquisition with Data Modulation

The current S-805 constraint requires carrier-only transmission for DG-2 for acquisition at data rates less than or equal to 20 Ksps. Since AIRS employs an improved FLL implementation which eliminates detector

threshold, this restriction can be removed.

1.2.1.2.3 Wide Dynamics Operation

AIRS is to employ a third-order loop for carrier tracking. This enables it to track through a typical user orbit manuever. The dynamics to be tolerated can be relaxed to equal or better the Wide Dynamics Demodulator (WDD) specification.

1.2.1.2.4 Maximum Data Rate

With a simple adaptive 3-tapped delay line equalizer, the maximum data rate for SSA can be doubled for AIRS.

1.2.1.3 Additional Performance Improvements

The AIRS design also provides additional performance capabilities in areas not spelled out explicity in S-805.

1.2.1.3.1 Reacquisition

Since the receiver has already been tracking the incoming signal before a loss of lock happens, it has a more accurate estimate of the signal characteristics (e.g. frequency and PN code phase) than it does during the initial acquisition. If the receiver can make use of this information, the average reacquisition time can be greatly improved. The AIRS design takes advantage of this information by introducing a wait state followed by a minisearch before reverting to a full initial acquisition.

1.2.1.3.2 RFI Mitigation

Because of the flexibility of its digital implementation, the AIRS can incorporate various RFI mitigation schemes with negligible impact on the receiver hardware. This typically involves reprogramming a Read Only Memory (ROM). This flexibility makes AIRS an excellent experimental receiver for evaluating different RFI mitigation schemes.

1.2.1.3.3 Digital Implementation

The selected digital approach can be simulated in a computer. Typically, very little additional hardware degradations will be encountered once the design has been verified with simulation. In addition, unit-to-unit performance variations can be virtually eliminated.

1.2.1.3.4 Frequency Stability

All frequency sources are phase locked to the station standard. This delivers the ultimate Doppler and ranging performance that is practically achievable.

1.2.1.3.5 General Improvements

The AIRS design closely resembles an optimum receiver for the SSA signals. In addition, the AIRS software can automatically match the receiver parameters to the real time signal characteristics (e.g. signal strength) by monitoring the link conditions. It therefore attains the best practically achievable receiver performance in terms of slip rates, threshold and fading margin. In addition AIRS incorporates the ability to estimate and correct for the delay in the orbit trajectory data. This narrows the specified frequency uncertainty during a stable orbit.

1.2.2 Operational Improvements

Since AIRS is a software-based digital receiver, it can provide many operational conveniences made possible by its built-in intelligence. This capability is reflected in its multimode operation, self test capability, and simplified ADPE interface requirements. In addition, since AIRS performs both the carrier and data demodulation functions, certain current demod/bit sync interface switching through the ADPE can be eliminated.

1.2.2.1 Multimode Operation

1.2.2.1.1 Autonomous Mode

In this mode the receiver configures itself automatically and selects the receiver parameters to achieve optimum performance based on pre-selected user data characteristics.

1.2.2.1.2 Flexible Data Format Mode

In this mode the receiver configures itself automatically and selects the receiver parameters that allow flexible user data characteristics such as real time data rate switching.

1.2.2.1.3 Test Mode

In this mode the receiver configuration and its parameters are selected via an external real time serial data interface (e.g. GPIB). In the test mode, the AIRS is then a general-purpose, dual-channel spread-spectrum BPSK/QPSK receiver.

1.2.2.2 Self Test Capability

Through its software based intelligence, the AIRS can provide an indication of operational readiness, warn of degraded performance and facilitate maintenance actions.

1.2.2.3 ADPE Interface Simplifications

The AIRS provides its own estimates on the received signal Doppler after initial acquisition. Since the AIRS is also capable of autonomous operation after an initial set up command procedure, it can be detached from the ADPE for normal operations.

1.2.2.4 I/Q Channel Ambiguity

Since both the carrier and data demodulation are performed by the AIRS, the I/Q channel ambiguity arising from certain data rate and power combinations can be resolved within AIRS (rather than via ADPE). The

AIRS resolves the ambiguity either by the presence of PN spreading (DG-1), data rate difference, or power split. In conjunction with the decoder, the AIRS can also resolve channel ambiguity by the presence of coding.

1.3 Organization of the Report

This report is divided into four sections and 4 appendices. Section 2 provides a closer examination of the requirements of AIRS in terms of rationale, approach and implementation. These requirements form a basis for the functional specification and drive the baseline design.

Section 3 examines the testing requirements in terms of the ancillary hardware and functional tests required to demonstrate the AIRS performance.

Section 4 describes a detailed preliminary hardware functional design for the AIRS baseline. Current state-of-the-art digital and signal processing technologies are assessed in terms of the AIRS requirements.

Finally, Section 5 gives a cost estimate of (a) the design, development and production of the protype AIRS (b) the acquisition of the ancillary demonstration hardware and (c) the test program necessary to demonstrate the AIRS.

2.0 AIRS REQUIREMENTS

In this section, AIRS requirements implementation techniques are examined in detail. These requirements form a basis for the AIRS functional specification and the accompanying baseline receiver structure [1]. The areas considered are:

- Acquisition
- Reacquisition
- Receiver configuration
- Flexible Data Mode
- Third-order loop for carrier tracking
- RFI mitigation
- Adaptive equalization
- Orbit delay estimation

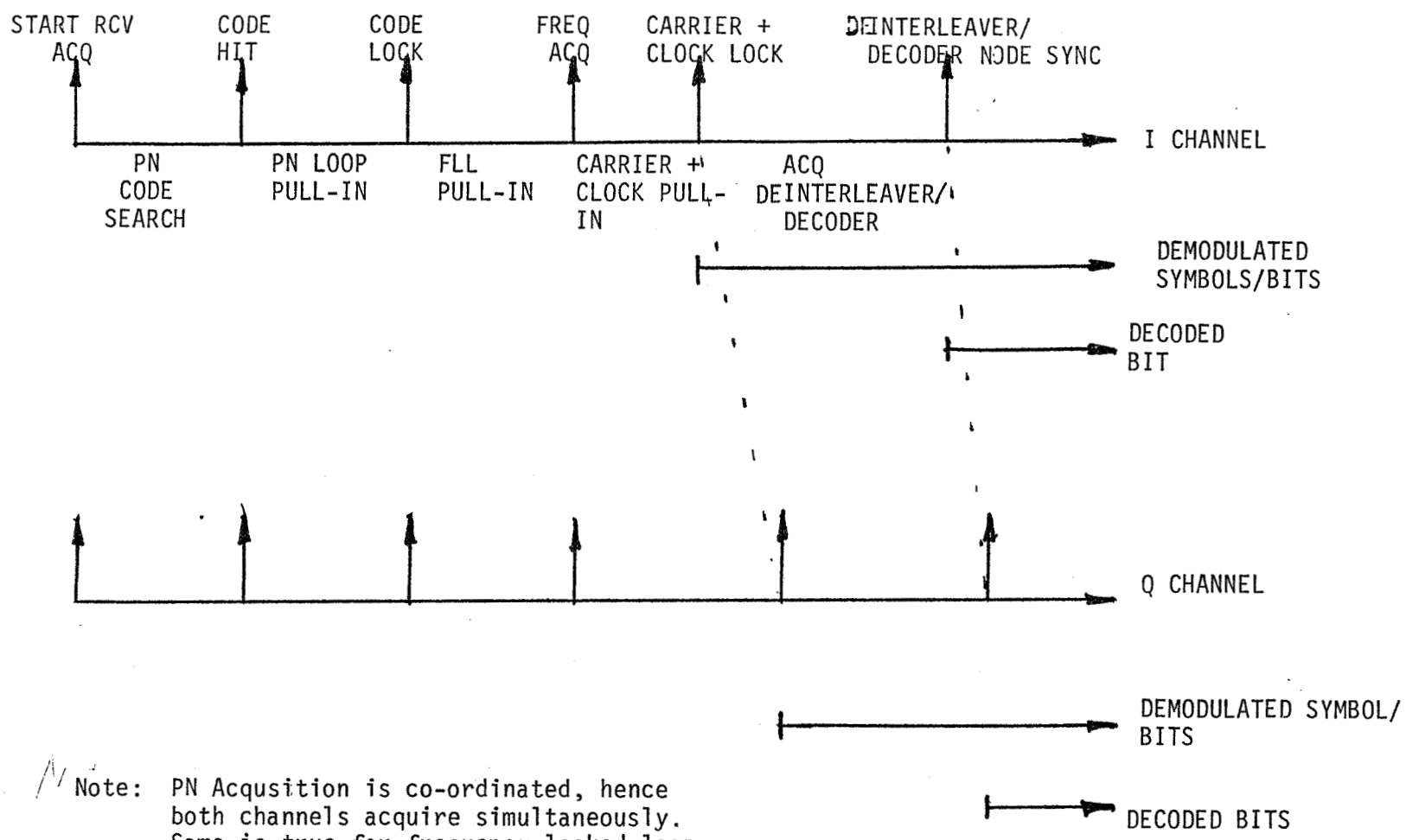
The study of adaptive equalization and RFI mitigation are rather lengthy. They are summarized here in this section and the technical details are deferred to Appendices A through C.

2.1 AIRS Acquisition Sequence

Depending on the data group and mode, the AIRS acquisition process consists of acquiring of the PN code, carrier and bit sync loops, and the deinterleaver/Viterbi decoder. Since the I and Q data channels can have different formats in general, the acquisition behavior of the quadrature channels are different. Figures 2.1-1 to 2.1-3 show typical acquisition sequences for DG1-1 and 2, DG1-3 and DG2 signals.

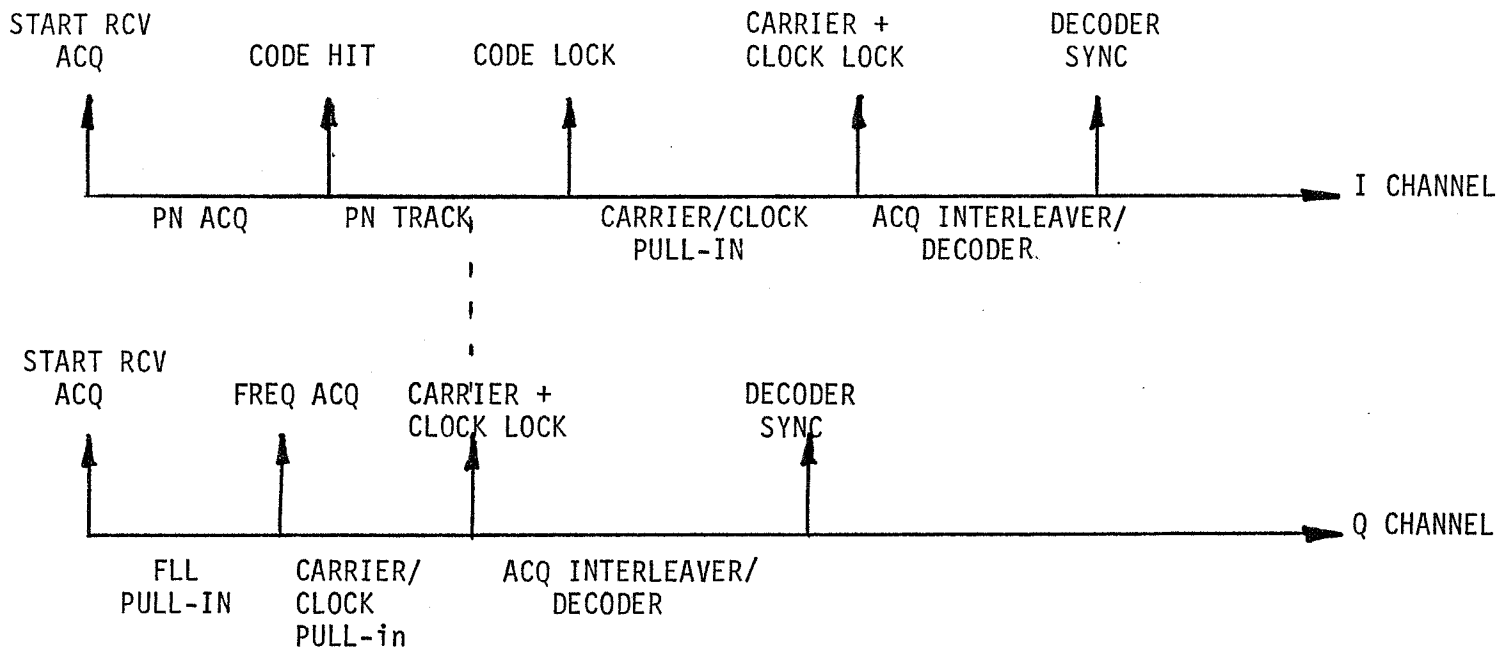
2.1.1 Coordinated PN Acquisition and Tracking

The AIRS employs a coordiated PN acqusiton and tracking technique to optimize performance and hardware utilization. Four parallel IF despread/envelope detect paths (one of which is shown in Figure 2.1-4)



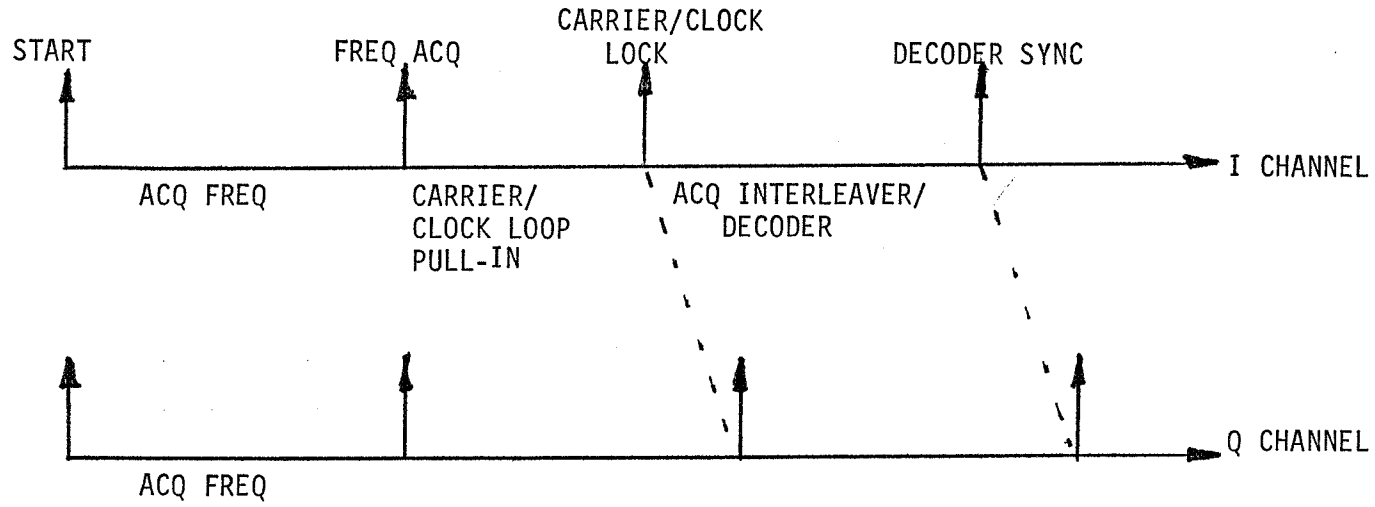
Note: PN Acqusition is co-ordinated, hence both channels acquire simultaneously. Same is true for frequency locked loop pull-in. However, the bit syncs acquire independently and do not declare lock simultaneously.

Figure 2.1-1. Acquisition Sequence for DG-1, Mode 1 and 2



Note: Q channel is not spread hence can proceed to acquire frequency. I channel as shown skips the frequency acquisition step.

Figure 2.1-2. Acquisition Sequence for DG1 Mode 3.



Note: FLL works off both signals.

Figure 2.1-3. Acquisition Sequence for DG2.

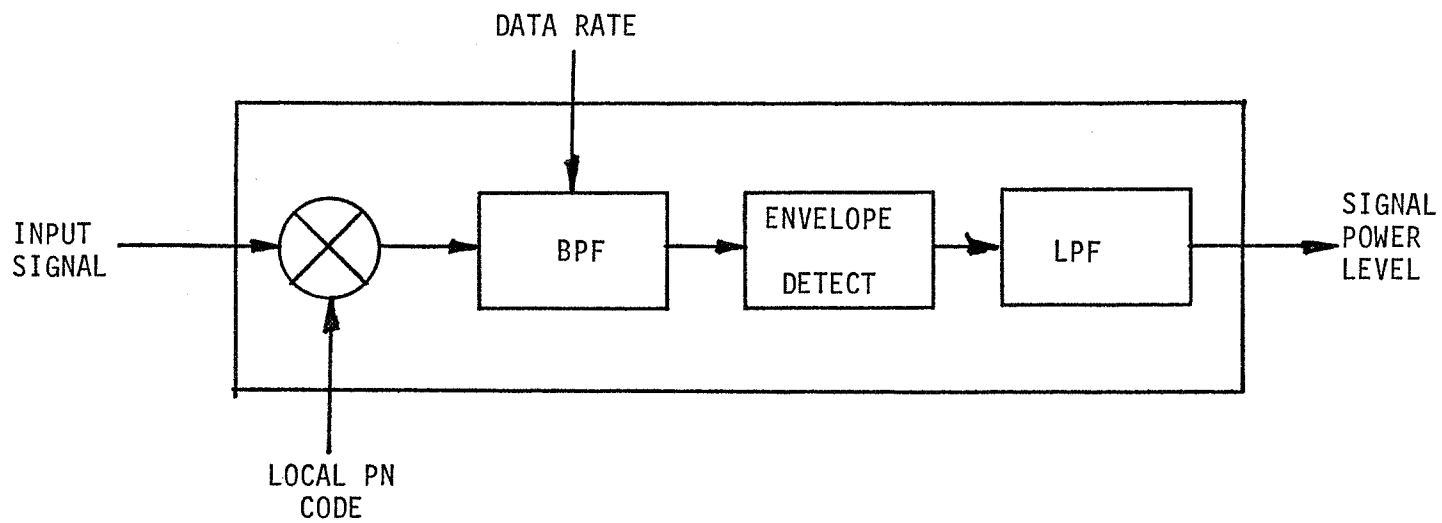


Figure 2.1-4. IF Despread/Envelope Detect Channel for PN Acquisition and Tracking.

are shared for PN acquisition and tracking puroses. A flow chart for the PN acquisition and tracking procedure and the allocation of the four IF paths is shown in Figure 2.1-5. In this figure, the number in the parentheses is the number of IF paths required to achieve the operation indicated in the box. As an example, a typical acquisition/tracking sequence for a DG1-1 signal based on the flowchart is shown in Figure 2.1-6. The use of charge-coupled device (CCD) speeds up considerably the acquisition at low signal levels and is considered in detail in Vol. III.

2.1.2 Frequency Lock Loop

The AIRS acquires its frequency to within ±25 Hz by means of a frequency lock loop whose error feedback signal is generated from a weighted sum of the I and Q channels as soon as unspread signals are present at its input.

2.1.3 Carrier and Bit Sync Loop

The carrier and bit sync loop shall normally be coupled.* Carrier recovery is achieved by a data-aided loop (DAL). This is coupled with the bit sync which is a data transition tracking loop (DTTL). The feedback error signal of the DAL is generated from a weighted sum of the I and Q channels. Both the DAL and the DTTL acquire simultaneously. After the DAL acquires the loop frequency estimate is used to aid the PN loop tracking. The carrier loop acquires as a second-order loop and tracks as a third-order loop.

2.2 Reacquisition

The reacquisition procedure for the AIRS is shown in Figure 2.2-1

*See Section 2.4 for flexible data rate mode operation.

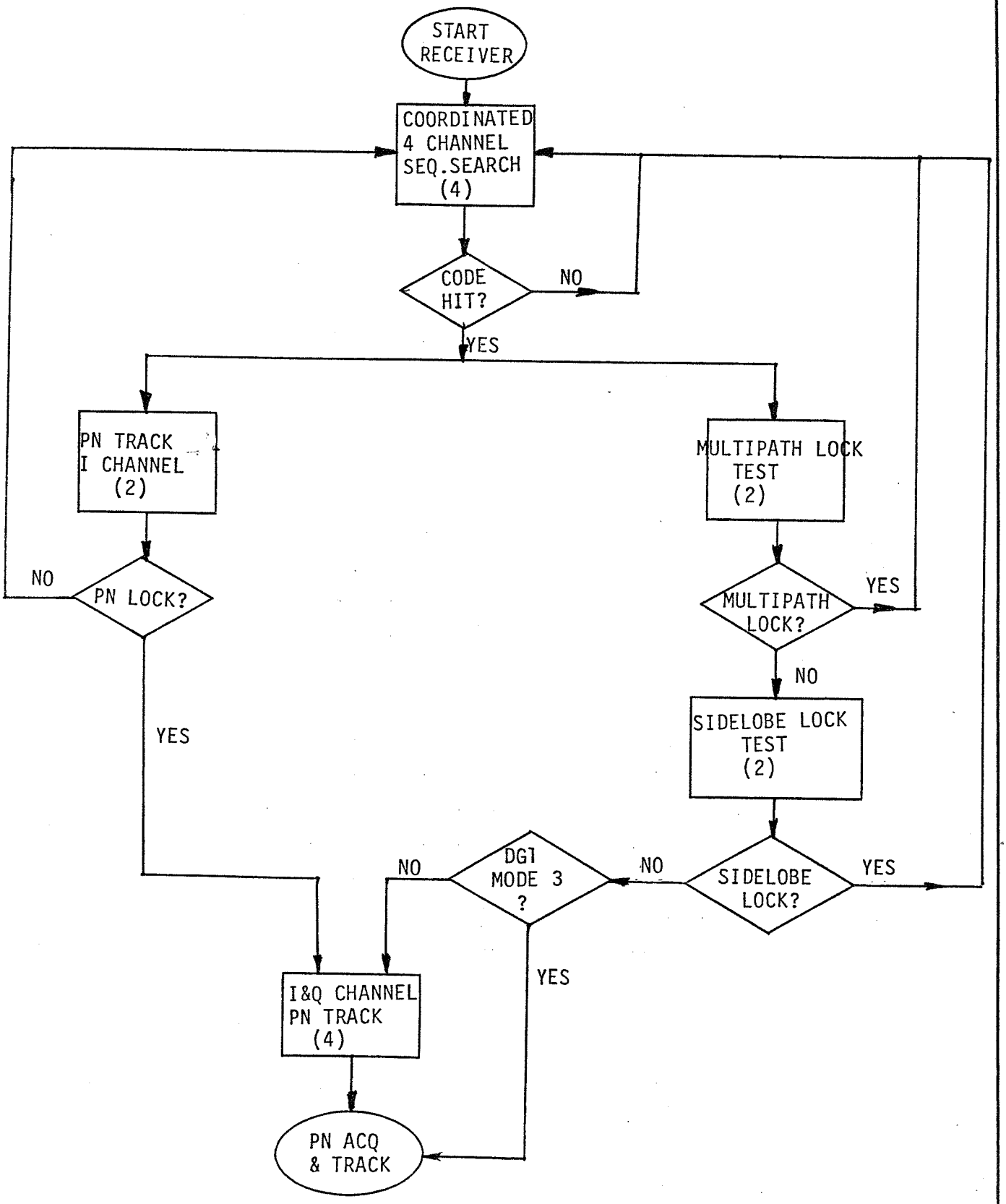


Figure 2.1-5. Flow Chart for PN Acquisition and Tracking

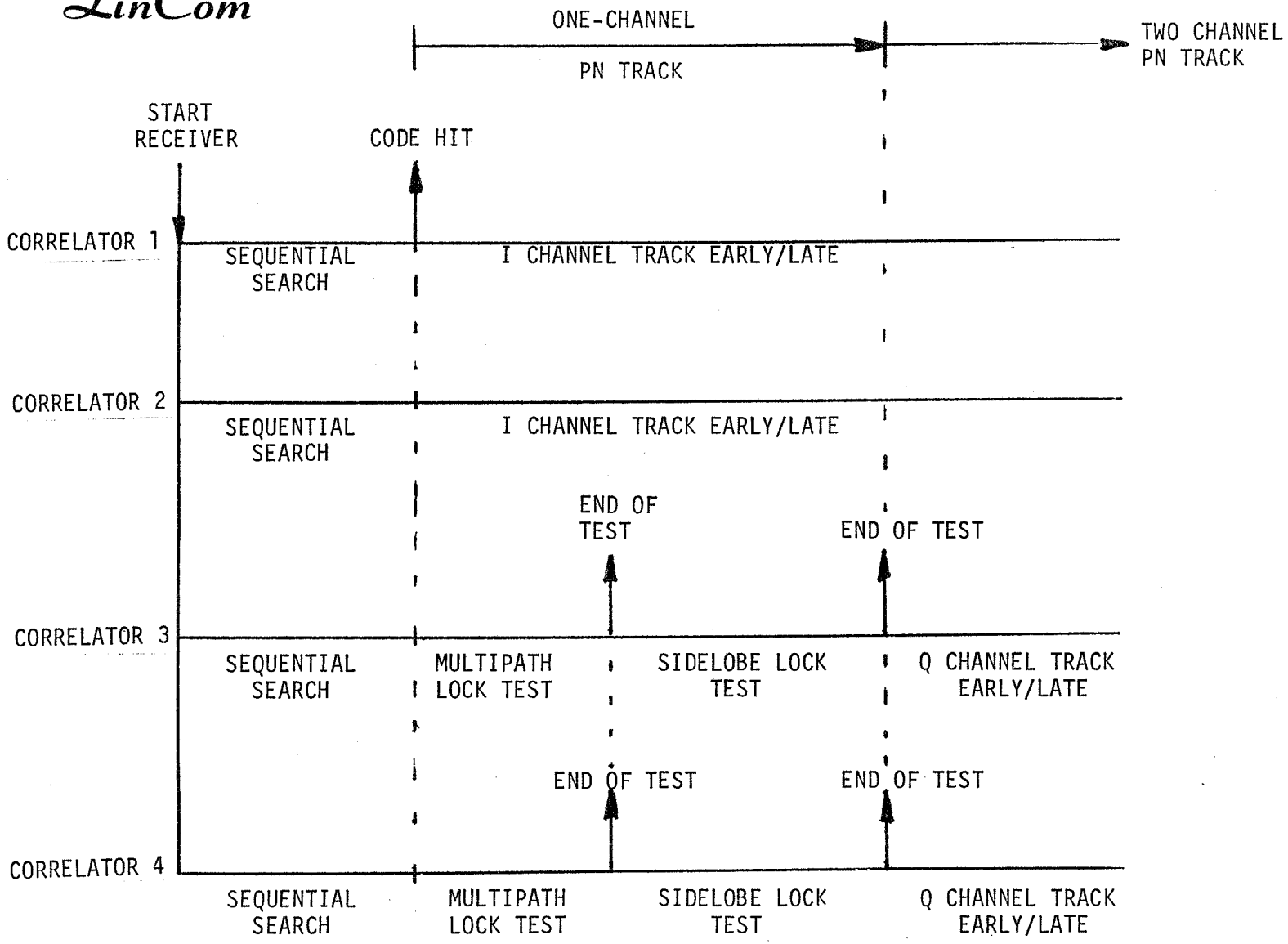
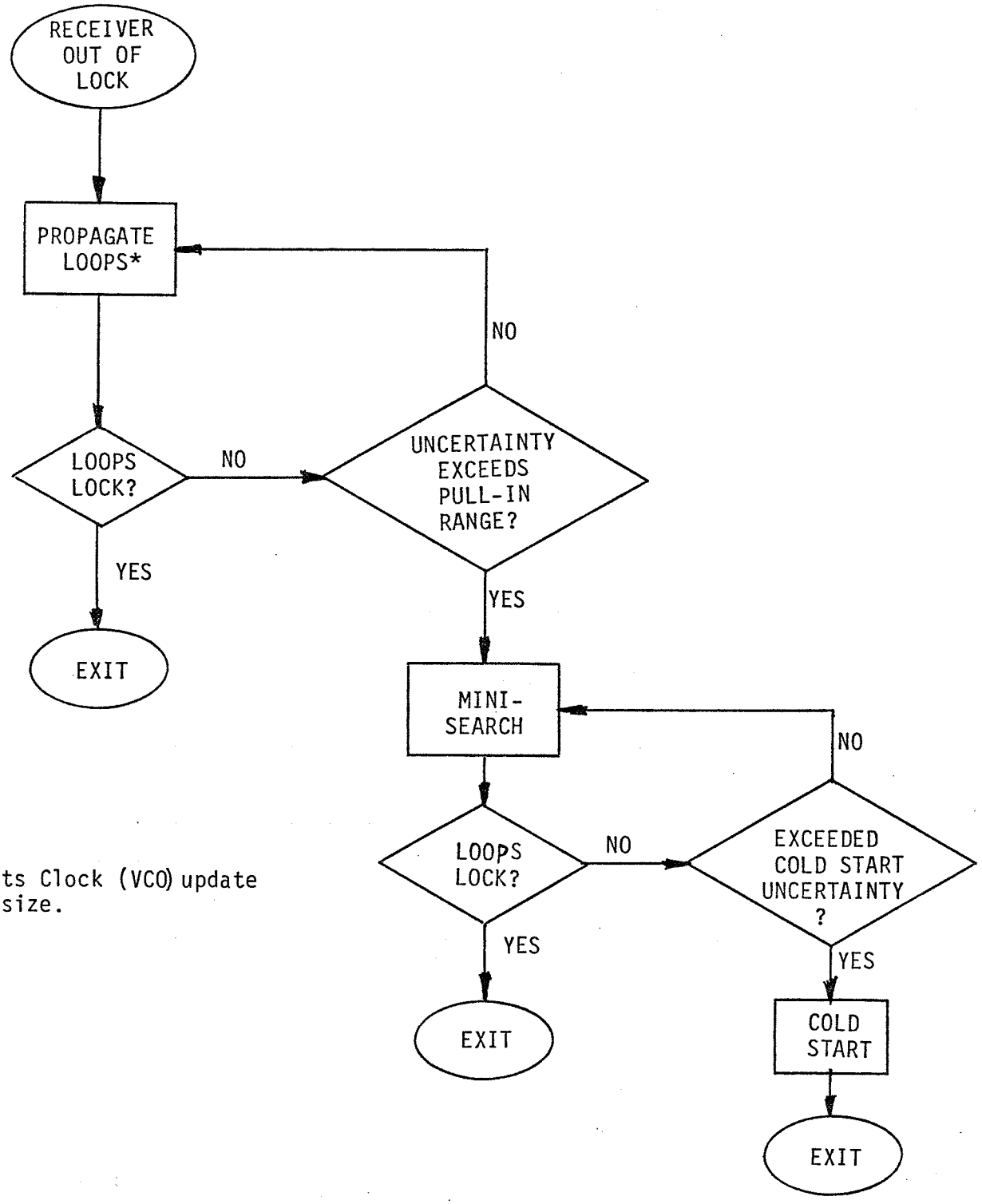


Figure 2.1-6. Typical PN Acq and Track Operation for DGl.



*Limits Clock (VCO) update stepsize.

Figure 2.2-1. Conceptual Reacquisition Procedure

in the event a loss of lock (PN, AGC, carrier, or bit sync) occurs. The receiver tries first to pull in the signal with the current loop configuration (wait state). After the attempt fails, the receiver enters a minisearch mode which is an acquisition mode with reduced code and frequency uncertainty. If it fails again, the AIRS reverts to a cold start. The ground segment control shall be able to interrupt this normal acquisition procedure and go directly to cold start.

If the decoder loses node sync, it reacquires without forcing the receiver into a cold start mode if the receiver is still in lock. This is shown in Figure 2.2-2.

2.2.1 Reacquisition Strategy

In the current receiver implementation, the full acquisition procedure is activated whenever the receiver drops lock. Since the receiver has already been tracking the incoming signal before this can happen it has a more accurate estimate of the signal characteristics (e.g. frequency and PN code phase) than during the initial acquisition. If the receiver can make use of this information, the average reacquisition time can be greatly improved.

A conceptual approach of a reacquisition scheme taking advantage of this "pre-dropped-lock" information is shown in Figure 2.2-3. At the onset of the loss of lock, the uncertainty is zero. As time progresses and if the receiver still has not acquired lock, the uncertainty grows until it reaches the boundary defined by the initial "cold-start" acquisition boundary. For a small uncertainty, the tracking-mode configuration is capable of self-acquisition and the receiver should therefore wait t_0 seconds in its current mode of operation. However after t_0 seconds the receiver is no longer capable of self acquisition

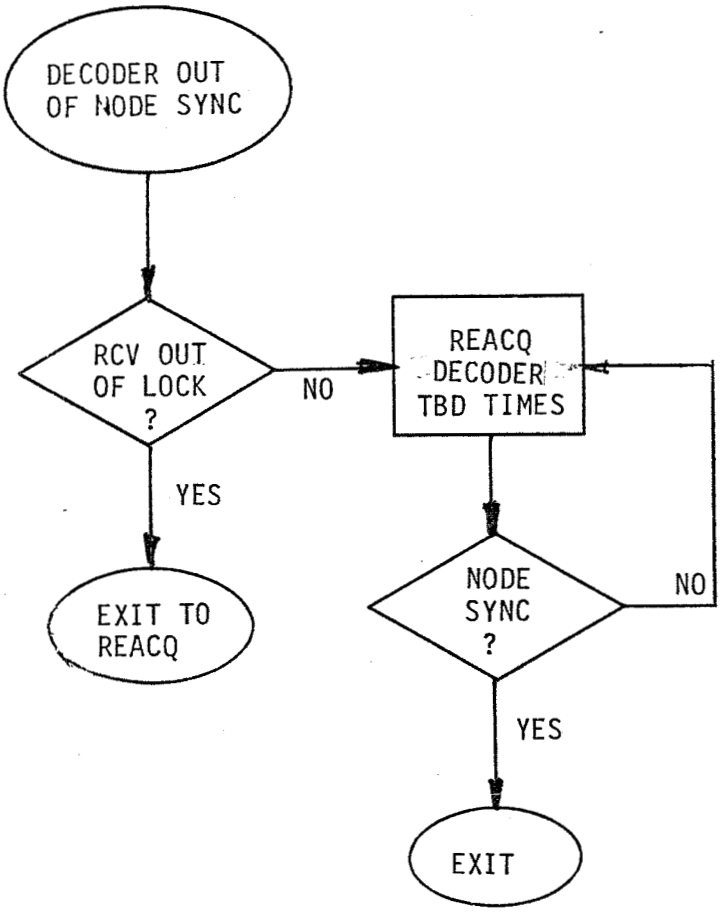


Figure 2.2-2. Decoder Reacquisition.

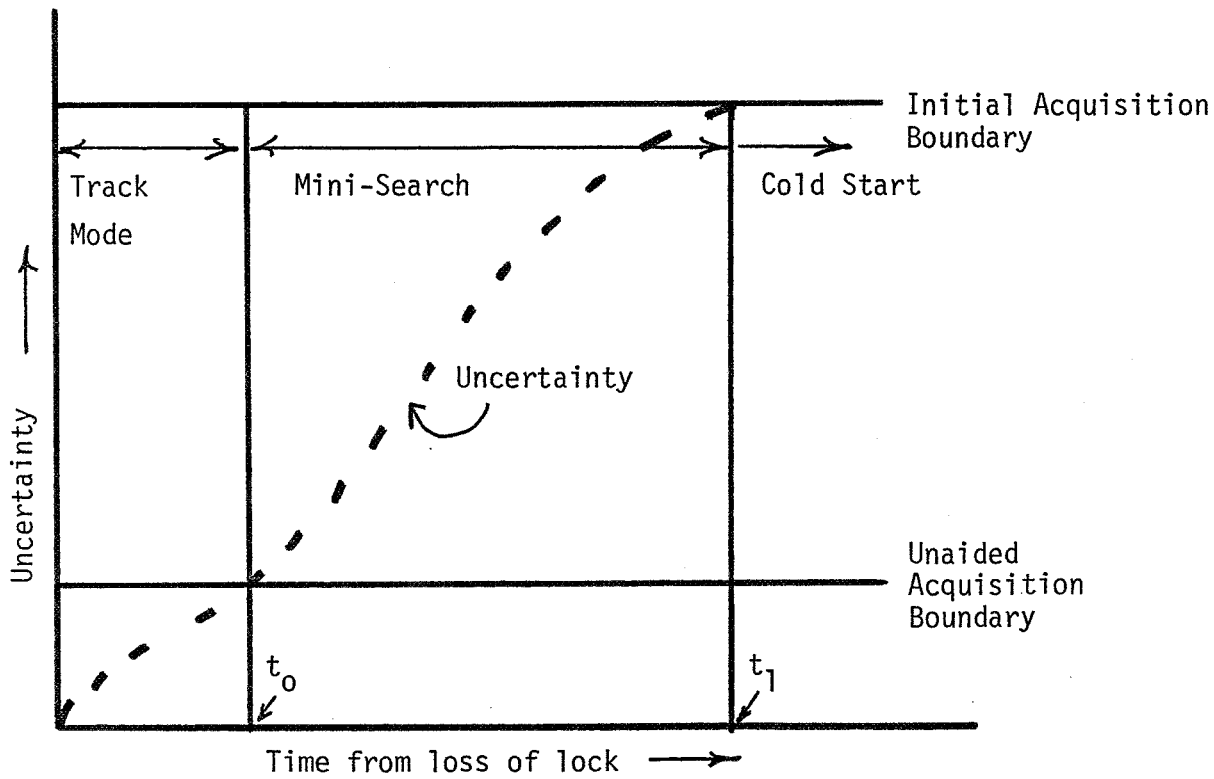


Figure 2.2-3. Conceptual Reacquisition Strategy.

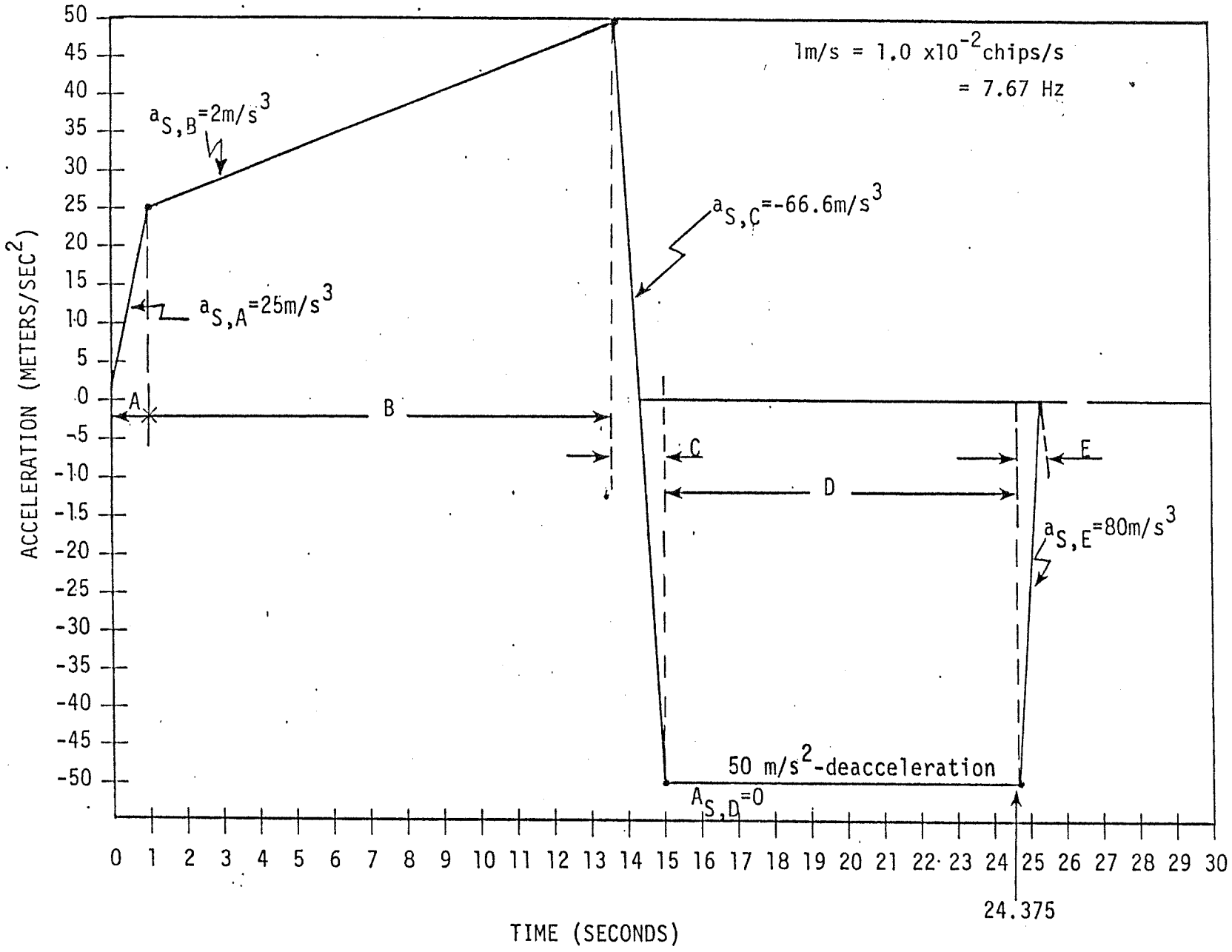


FIGURE 2.2-4. SATELLITE DYNAMICS PROFILE UTILIZED

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in the tracking mode and must acquire in the "search" mode (e.g. by stepping the PN chip position). However, until t_1 is reached the uncertainty region is not as high as the one defined by the initial "cold-start" operation. Therefore, a minisearch over a reduced uncertainty region is called for. After t_1 seconds, the uncertainty region has reached its maximum value and a cold-start search will have to be performed.

In order to quantify this strategy, we have to determine the uncertainty profile, the minisearch region, and the parameters t_0 and t_1.

2.2.2 Dynamics Profile

The dynamics profile defines the temporal diffusion of the uncerainty region. We consider two scenarios. The first one assumes that a loss of lock is caused by a user spacecraft manuever and the model used by the Wide Dynamics Demod (WDD) study [2] is employed. The user satellite dynamics profile utilized is shown in Figure 2.2-4. The second scenario is based on the AIRS specified worst case acceleration value of 50 m/s^2. (Note that 1 m/s=1.01 x 10^{-2} chip/s=7.67 Hz)

2.2.3 Tracking Mode Pull - in Range

Both the PN tracking loop and the carrier tracking loop have limited pull-in capability. During initial acquisition with worst case uncertainties, these loops must be aided by other means. Hence, the acquisition mode operation is usually different from that of the tracking mode operation. However for reacquisition, the uncertainly region is initially small and the loops are capable of reacquiring in the tracking mode. The acquisition range of the bit synchronizer is very large relative to the uncertainty region and thus can acquire without external aiding.

A PN loop tracking range is on the order of ±0.5 chips. A carrier tracking loop has a typical pull-in range proportional to the one-sided loop noise bandwidth B_L. For the purpose of determining the pull-in range we use the medium rate demodulator (MRD) bandwidth (B_L=500Hz). The time to reach the pull-in boundary can be computed based on the dynamics and is summarized as follows:

TIME TO REACHING TRACKING BOUNDARY, SEC

(BOUNDARY)	DYNAMICS PROFILE	WORST CASE ACCELERATION
PN LOOP (49.5m)	2.45	1.41
CARRIER LOOP (65.2m/s)	2.96	1.30

2.2.4 Mini-Search Boundary

In the proposed AIRS implementation, carrier acquisition is performed by a frequency locked loop. Its mechanization is not sensitive to the expected range of frequency uncertainty. Therefore, the minisearch option applies only to PN reacquisition.

For a baseline minisearch technique, we consider the STI strategy [2] of sweeping over a window of 600 chips (± 300 chips) for the WDD dynamic profile. This scheme is predicted by STI to acquire within 6 sec with a 90% probability. Note that the initial acquisition procedure requires the receiver to sweep over approximately 3800 chips (± 1900 chips). For the worst case acceleration of $50m/s^2$, the uncertainty range reaches the 600 chips window in 34.5 seconds.

Since the initial acquisition time is on the order of 20 seconds, a sweep over a window of 600 chips for 10 seconds for minisearch is recommended.

2.2.5 Reacquisition Strategy Summary

The reacquisition procedure affects mainly PN and carrier reacquisition.

2.2.5.1 PN Reacquisition

Upon loss of PN lock:

1. The PN loop remains in the tracking mode for 2s.
2. If the loop is still unlock after 2s, it switches to the minisearch mode for 10s. The minisearch mode is defined by a uniform search over a 600 chip window (± 300 chips).
3. The PN loop goes to "cold start" initial acquisition if it did not acquire after 10s of minisearch.

2.2.5.2 Carrier Reacquisition

We distinguish between spread and unspread signals. If the signal is unspread, upon loss of lock:

1. The carrier loop remains in the tracking mode for 2s.
2. If the carrier loop cannot reacquire in 2 secs, the frequency lock loop configuration takes over.

If the signal is spread and the receiver only loses carrier lock, proceed to reacquired as above. If the signal is spread and the receiver also loses PN lock, deactivates the carrier loop until the PN loop reacquires.

2.3 Receiver Configuration for Various Modes

The AIRS is designed to operate in three distinct modes--the normal mode, the flexible data format mode (FDM) and the test mode. In the normal mode (NM), the receiver configures itself and selects the receiver parameters to achieve optimum performance based on preseleted user data characteristics. In the FDM, the receiver configures itself

and selects the receiver parameters to accomodate maximum flexibility in the user data characteristics. In the test mode (TM), the receiver configuration and its parameters are selected via external real time serial data interface (e.g. GPIB). In the test mode, the AIRS is then a general purpose dual channel spread spectrum BPSK/QPSK receiver.

2.3.1 Receiver Functional Blocks

Figure 2.3-1 shows a simplified AIRS functional diagram. The incoming IF signal at 370 MHz is first down-converted and Doppler compensated to 35 MHz. This signal is then noncoherently AGC controlled. The signal is split into two (hardware-wise) identical channels (I and Q).

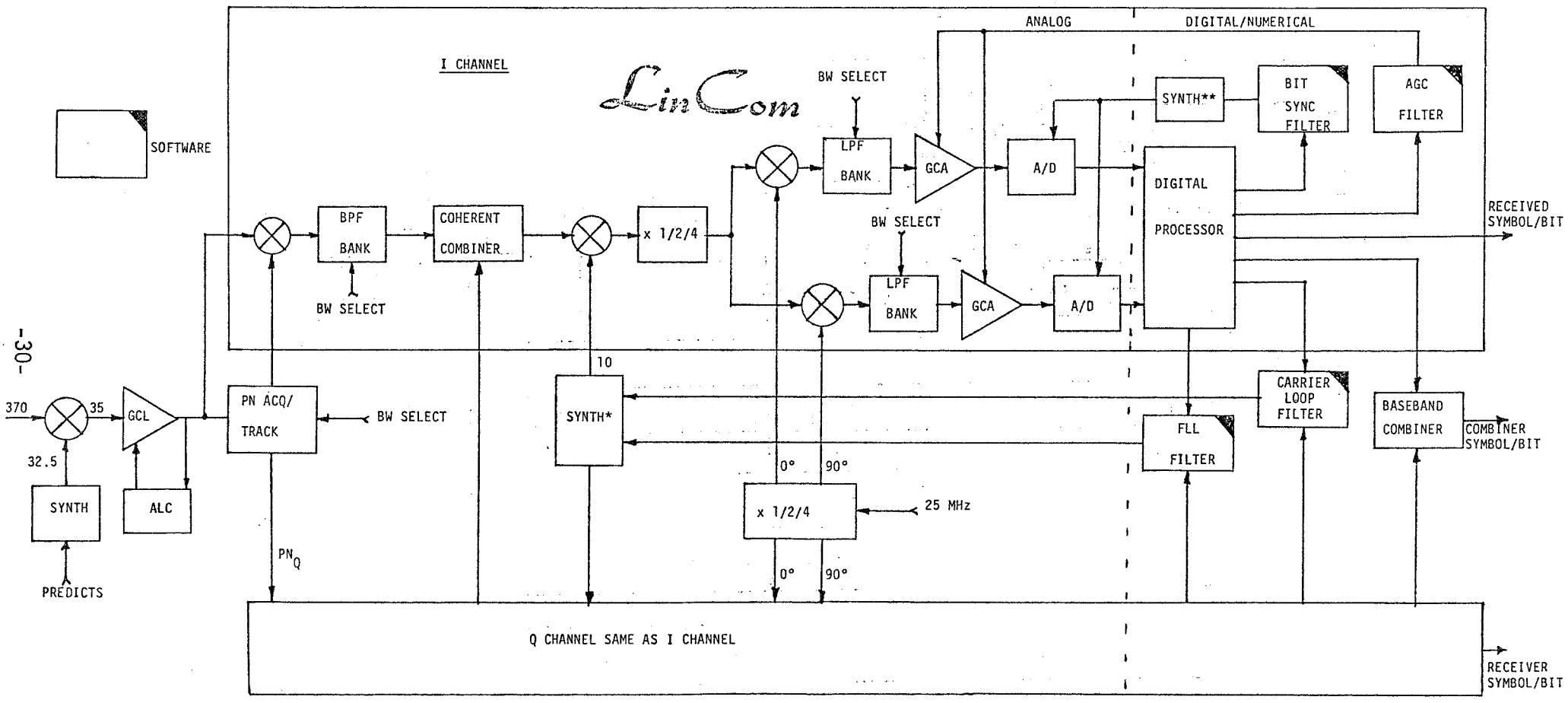
2.3.1.1 PN Despreader

In the channel (e.g. I shown in the figure), the signal is despread by a local replica of the PN code. If the signal is originally unspread, this stage is bypassed.

2.3.1.2 IF Processor

The despread signal then passes through a selectable BPF filter bank. The BPF bandwidth is chosen based on the data rate. It is to be wide enough to pass the data modulation undistorted yet narrow enough to limit the thermal noise passed along to subsequent stages of the receiver. For some user data characteristics, the I and Q channels contain the same signal and a coherent combiner is available to combine the two IF signals.

A long loop implementation for carrier recovery is used. The second LO at 10 MHz is generated by a synthesizer which serves to close the carrier loops (PLL and FLL). The second LO output at 25 MHz can be multiplied by 2 or 4 to wipe off data. The multiplication factor



* CARRIER DIGITALLY CONTROLLED OSCILLATOR (DCO)

**CLOCK DCO

Figure 2.3-1. Simplified AIRS Block Diagram.

selected depends on the type of modulation (BPSK or QPSK) and power split. The multiplication is only used during frequency acquisition (FLL mode). The signal is not multiplied during tracking (PLL mode). The output of the multiplier is I-Q demodulated by a correspondingly multiplied 25 MHz reference.

2.3.1.3 Baseband Processing

The quadrature baseband signals (I_I and I_Q) then pass through LPF banks before they are A/D converted. The LPF bandwidth is selected based on the data rate on that channel and the sampling rate of the A/D converter. The gain-controlled amplifier (GCA) in front of the A/D converter (ADC) matches the baseband signal strength with the ADC dynamic range and is controlled by the fine AGC. The fine AGC operates coherently when the receiver is in carrier lock. The sampled data are then processed by the digital processor whose outputs include the received symbols, AGC error, bit sync error, PLL error, and FLL error. The loop errors are then filtered by various computer (numerical) algorithms and the filtered outputs are used to control and close the various loops. For example, the bit sync filter output controls the bit sync synthesizer which generates the ADC sampling clock. Since the filtering is performed in software, an almost infinite selection of loop bandwidths are available. The digital processor also generates various lock indicators and link performance indicators.

2.3.1.4 PN Acquisition and Tracking

The PN acquisition and tracking block shown in Figure 2.3-1 is expanded in Figures 2.3-2 and 2.3-3. During acquisition, 4 channels are shown to search in parallel. (2 additional channels from the despread circuit may also be used.) Note that the BPF bank is selectable. The

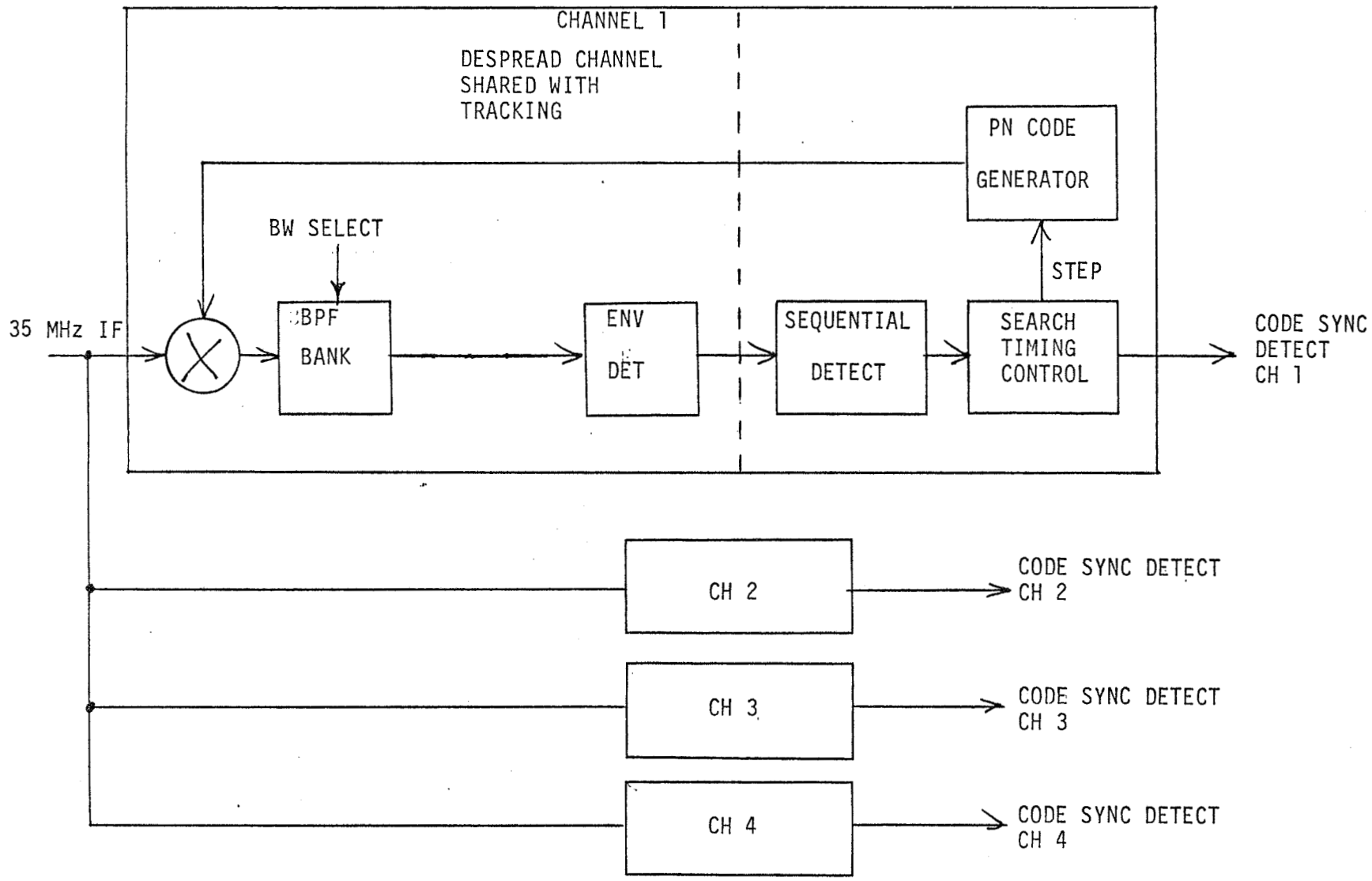


Fig. 2.3-2. Sequential PN Acquisition (4 Channel).

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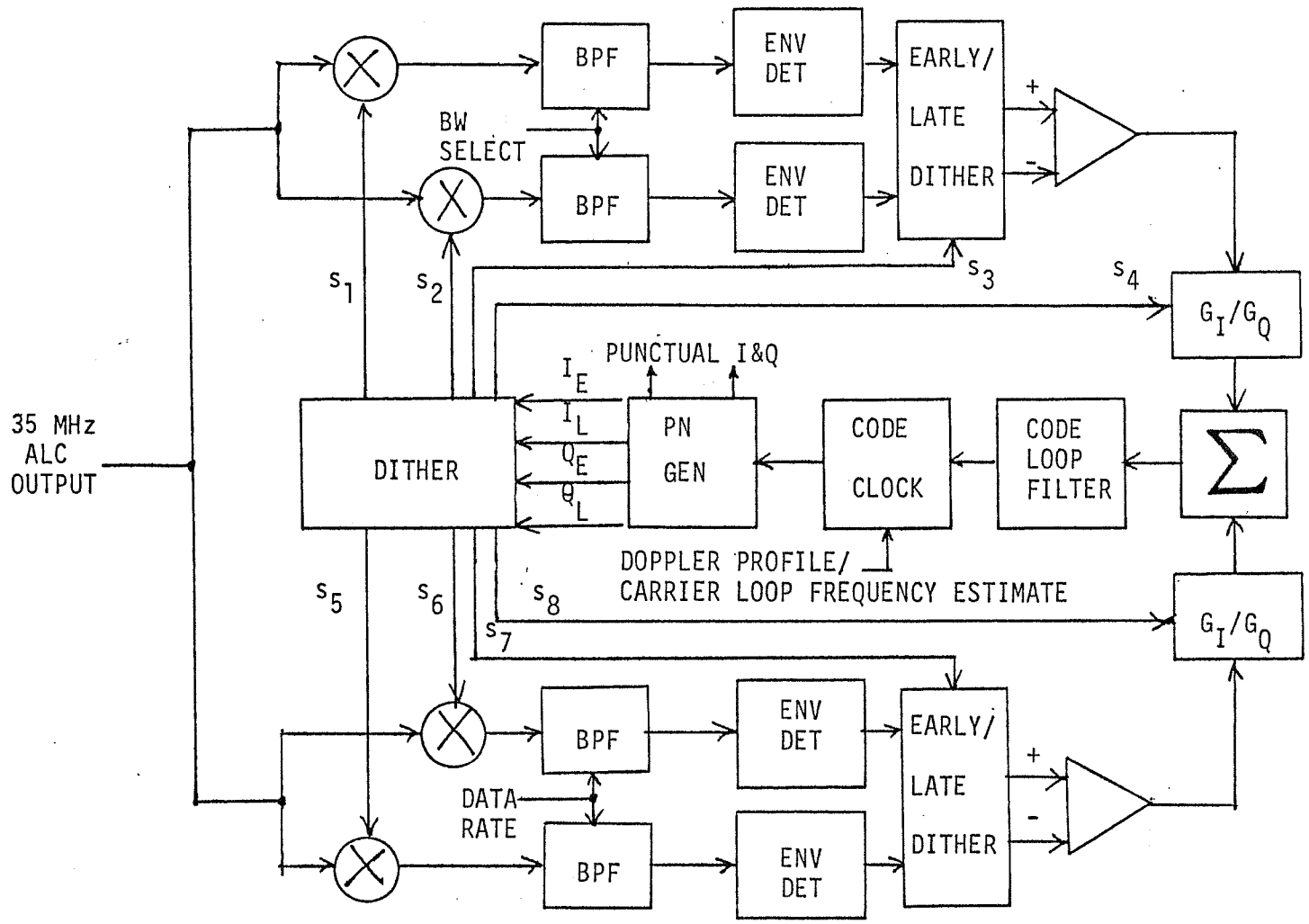

Fig. 2.3-3. 2-Channel Dithered Early/Late PN Tracking Loop.

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mixer, bandpass filter and envelope detector are common for both acquisition and tracking. Therefore they are to be shared. The PN tracking circuit is a modified 2 channel dithered early/late gated loop.

2.3.2 Configuration Based on Data Characteristics

In the autonomous mode, the receiver configuration is based on the selected user data characteristics. The different configurations are shown in Figure 2.3-4. A total of 9 different configurations are identified. These configurations are summarized in a configuration matrix in Table 2.3. Note that for configurations where both the I and Q channels are used, the loop errors are weighted sums of both channels based on the I:Q power split.

For the flexible data mode, the receive configurations will be a subset of Table 2.3. The particular configuration depends on the position of data characteristics to be designated flexible.

For the test mode, the receiver can be configured in any desirable manner.

2.3.3 Interfaces

The interface requirements for setting up the AIRS are different for the three receiver modes.

2.3.3.1 Data Characteristics Definition

The data characteristics definition is required for the autonomous mode and the test mode. This portion of interface commands include:

(a) Data Mode Select

- Data Group (1 or 2)
- Mode (1, 2 or 3)
- I:Q Power Ratio
- Baseband Waveform (NRZ or Manchester)

Figure 2.3-4. Receiver Configuration Based on User Data Characteristics

CONFIGURATION	DATA CHARACTERISTICS
• CONFIGURATION 1: • COORDINATED PN ACQ • 2 CHANNEL PN TRACK • 2 CHANNEL BPSK CARRIER ACQ/TRACK • BIT SYNCS DECOUPLED	DG1 MODE 1 AND 2 (NORMAL CONFIGURATION)
• CONFIGURATION 2: • COORDINATED PN ACQ • I CHANNEL PN TRACK • 2 CHANNEL BPSK CARRIER ACQ/TRACK • BIT SYNCS DECOUPLED	DG1 MODE 3
• CONFIGURATION 3: • QPSK CARRIER ACQ/TRACK (I+Q) • BIT SYNCS DECOUPLED	DG 2 QPSK

Figure 2.3-4. (continued)

CONFIGURATION	DATA CHARACTERISTICS
• CONFIGURATION 4:	
• BPSK CARRIER ACQ/TRACK (I or Q)	DG2 BPSK
• CONFIGURATION 5:	(SPECIAL CONFIGURATION) A,B
• COORDINATED PN ACQ	
• 2 CHANNEL PN TRACK	
• COHERENTLY COMBINED BPSK CARRIER ACQ/TRACK (I OR Q)	
• CONFIGURATION 6:	C_I, C_Q
• COORDINATED PN ACQ	
• 1 CHANNEL PN TRACK	
• BPSK CARRIER ACQ/TRACK (I OR Q)	
CONFIGURATION 7:	D,E
• QPSK CARRIER ACQ/TRACK (I+Q)	
• BIT SYNC COUPLED	
• COHERENTLY COMBINED SYMBOL OUTPUT	

Figure 2.3-4. (continued)

CONFIGURATION	DATA CHARACTERISTICS
• CONFIGURATION 8:	FI, FQ
• COORDINATED PN ACQ	
• 1 CHANNEL PN TRACK (EXCEPT MODE 3)	
• BPSK/CW CARRIER ACQ/TRACK (I+Q)	
• CONFIGURATION 9:	GI,GQ
• BPSK/CW CARRIER ACQ/TRACK (I+Q)	

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Table 2.3. Summary Configuration Matrix.

	DG1-1,2	DG1-3	DG2-QPSK	DG2-BPSK	A,B	C_I	C_Q	D,E	F_I	F_Q	G_I	G_Q
COORDINATED PN ACQ	X	X			X	X	X		X	X		
I CHANNEL PN TRACK	X	X			X	X			X			
Q CHANNEL PN TRACK	X				X		X			X**		
COHERENT COMBINER					X							
I CHANNEL FLL	X	X	X	X	X	X		X	X	X	X	
Q CHANNEL FLL	X	X	X				X	X	X	X	X	
I CHANNEL CARRIER TRACK	X	X	X	X	X	X		X	X	X*	X	X*
Q CHANNEL CARRIER TRACK	X	X	X				X	X	X*	X	X*	X
I CHANNEL BIT SYNC	X	X	X	X	X	X		X	X		X	
Q CHANNEL BIT SYNC	X	X	X				X	X		X		X
BASEBAND DATA COMBINER								X				

*CW CONFIGURATION
**EXCEPT DG1-3

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- Special Configurations (A-G)

(b) PN Kernel Select

- I Channel
- Q Channel

(c) Convolutional Encoding Select

- Rate

(d) Data Rate Select

For the flexible data mode, the data rate select must be set to the highest allowable value.

2.3.3.2 Receiver Parameters Definition

The receiver parameters definition is required for the test mode. For the AM and FDM, they will be determined internally by AIRS based on the desired characteristics (i.e. optimality or flexibility). The parameters commands include:

(a) Hardware Parameters Select

- BPF BW (Acquisition and Tracking)
- LPF BW (Acquisition and Tracking)
- Channel Combinations
  - Coherent Combiner
  - I-Q Channels (PN, IF, Baseband)

(b) PN Acquisition and Tracking Select

- Search Boundary
- Search Rate
- Acquisition Threshold
- PN Channels for Tracking (1 or 2)
- PN Loop Bandwidth

(c) Baseband Digital Processor Select

- Sampling (Rate, Coherent or Noncoherent)
- Matched Filter (NRZ or Manchester)
- RFI Mitigation Options
- Adaptive Equalizer

(d) Numerical Algorithms Select

- FLL BW
- PLL (BW and Loop-Order)
- Bit Sync BW
- Fine AGC BW

2.3.4 Intelligence

For the autonomous and flexible data mode of operation, the receiver parameters are set automatically. The selection of parametric values depends initially on the selected user characteristics. From these characteristics the minimum C/N_0 will be established. The loop bandwidths are then set to provide optimized* acquisition and tracking performance. As the receiver obtains a better estimate of the received C/N_0 through the fine AGC estimate, the loop bandwidths will be adjusted accordingly.

2.4 Flexible Data Mode

For low EIRP users, the AIRS is designed to provide improved threshold performance by coupling the carrier recovery and the bit sync loops. However, for users capable of providing sufficiently high EIRP, the AIRS also operates in a suboptimal mode called flexible data mode (FDM) that allows flexibility in terms of real time switching of data parameters during a user support period. Specifically, the AIRS is

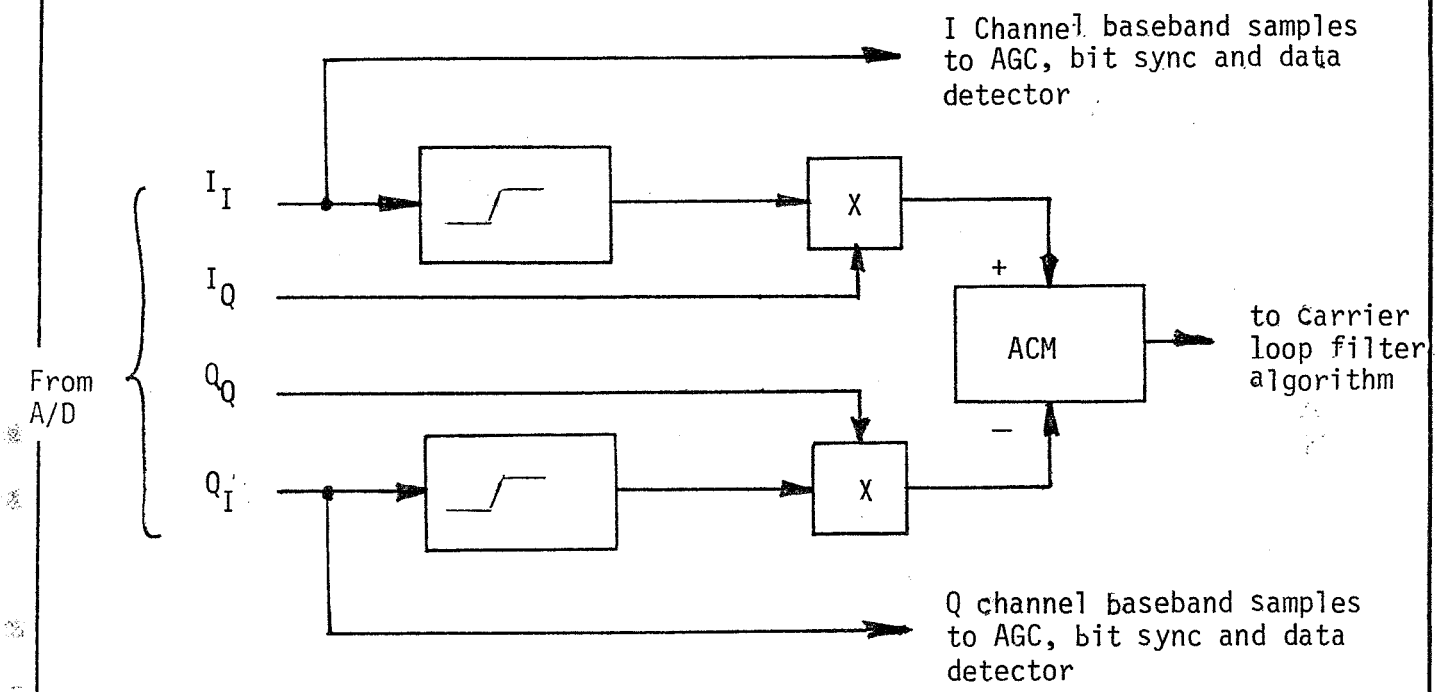
*Based on thermal noise, dynamics and oscillator phase noise.

designed to remain in PN and carrier lock while the user switches back and forth its data rate, data format, coding format, etc. The only requirement is that the user EIRP be commensurate with its data format and highest data rate. The advantage is that the AIRS receiver does not have to reacquire PN and carrier lock whenever the user chooses to switch its data format. Of course, the receiver is assumed to have knowledge of the upcoming data format switching in order to correctly synchronize and detect the baseband data. This can be done by prior scheduling or through real time downlink instructions from the user.

2.4.1 Receiver Implementation

The impact of the FDM on PN loop implementation is minimal. It only requires the data rate dependent bandpass filters in the PN tracking/despreading circuits default to the highest data rate supported by the user EIRP. However, in the FDM the carrier loop must be decoupled from the bit sync, i.e. the carrier loop must operate independently of the bit sync and vice versa.

The modification on the carrier tracking loop only involves the digital processing functions after the A/D converter (see Figure 2.3-1 in Section 2.3). Since the data rate information is to be ignored, the lowpass filter bandwidth in front of the A/D converter defaults to the one corresponding to the maximum allowable data rate commensurate with user EIRP. To generate the required error S-curve for carrier tracking the digital processing functions after the A/D are modified and are shown in Figure 2.4-1. The sampling rate is determined by the LPF bandwidth based on the Nyquist criterion and is not related to the bit sync loop. The operation described here is very similar to the two-channel Costas loop described in [3]. The clipper shown approximates



Note: Same as data-aided scheme except with I and D disabled (i.e. 1 sample I and D).

Figure 2.4-1. Carrier S-Curve Generation.

the optimum hyperbolic tangent nonlinearity. The loop error thus generated is further processed by a filtering algorithm that corrects the frequency and phase of the carrier loop synthesizer. The synthesizer serves as a conventional VCO.

The I and Q channel baseband samples are then processed by a bit synchronizer implementing the data transisiton tracking loop (DTTL) technique [4] as shown in Figure 2.4-2. The bit sync synthesizer is not tied to the A/D sampling clock.

2.5 Comparison of Second and Third Order Carrier Loops for Tracking Dynamics

The most stringent tracking requirement of the AIRS is the requirement to track a Doppler rate step of ±765 Hz/sec during orbit maneuver. Both the second-order and the third-order loops are capable of tracking this rate step. However, there is a major difference. The second-order loop tracks this step with a finite steady state phase offset whereas the third-order loop tracks it with a zero steady state error. Since a steady state phase offset degrades, for a prolonged period of time, both the tracking performance (rms phase jitter) and the slip performance (threshold) of the tracking loop, the third-order loop is the obvious choice.

2.5.1 Second-Order Loop

Consider a high gain second order loop with a closed loop transfer function given by

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{\zeta^2 + 2\zeta\omega_n s + \omega_n^2}$$

and one-sided loop noise bandwidth

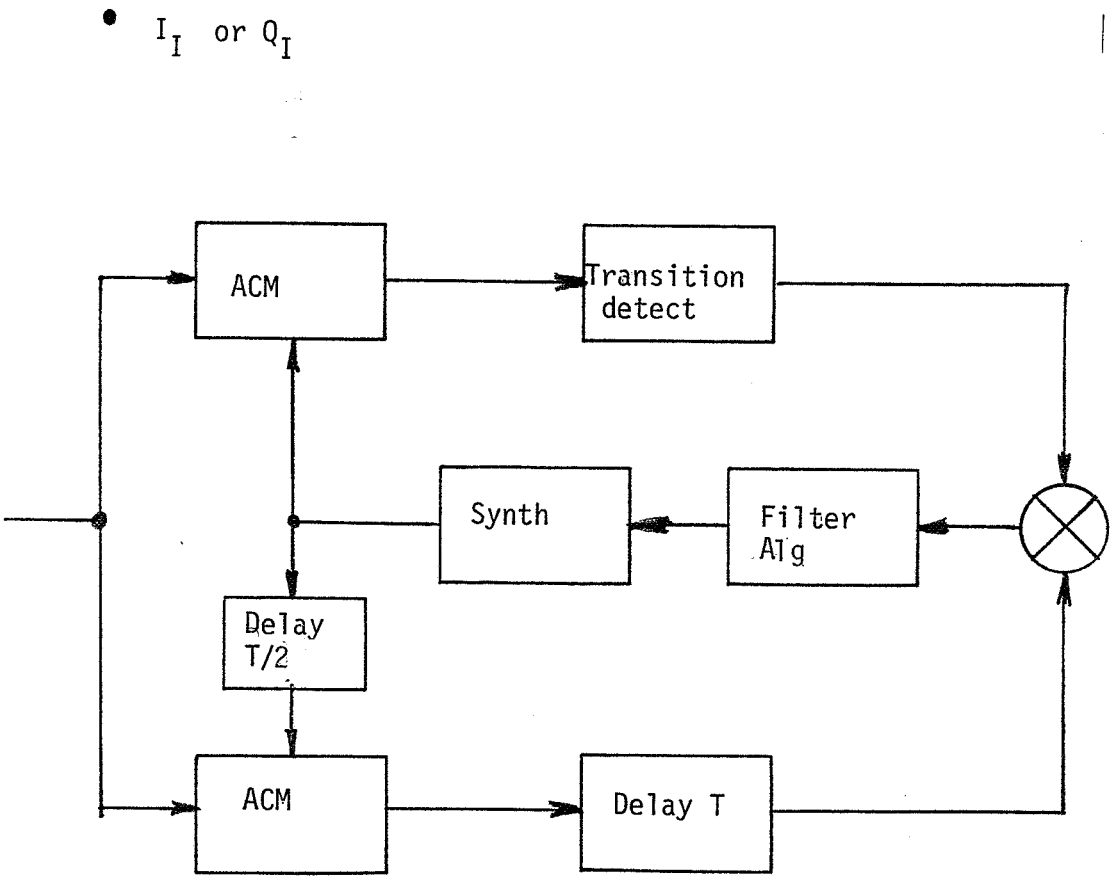


Figure 2.4-2. Bit Sync Implementation.

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)$$

For $\zeta = 0.707$, the loop phase error response to a Doppler rate step $\Delta\dot{f}$ is shown in Figure 2.5-1. Note that the steady state phase error $\phi_{ss} = 1.77\ \Delta\dot{f}/B_L^2$ is reached in less than $2/B_L$ secs. For all practical purposes, the loop phase offset will be ϕ_{ss} during the full period of the maneuver.

2.5.2 Third-Order Loop

For a third-order loop optimized for tracking a frequency ramp, the closed-loop transfer function is given by

$$H(s) = \frac{2\omega_3 s^2 + 2\omega_3^2 s + \omega_3^3}{s^3 + 2\omega_3 s^2 + 2\omega_3^2 s + \omega_3^3}$$

where the one-sided loop noise bandwidth is

$$B_L = \frac{5}{6}\,\omega_3$$

Its phase error response to the Doppler rate step is shown in Figure 2.5-2. However, even though the peak phase error is given by

$$\phi_p = 1.77\,\frac{\Delta\dot{f}}{B_L^2}$$

as in the second-order loop steady-state error, phase error is only of significance for the first $6/B_L$ secs.

2.5.3 Implications

Given a fixed noise bandwidth B_L, the third-order loop thus outperforms the second-order loop in terms of the ability to track out

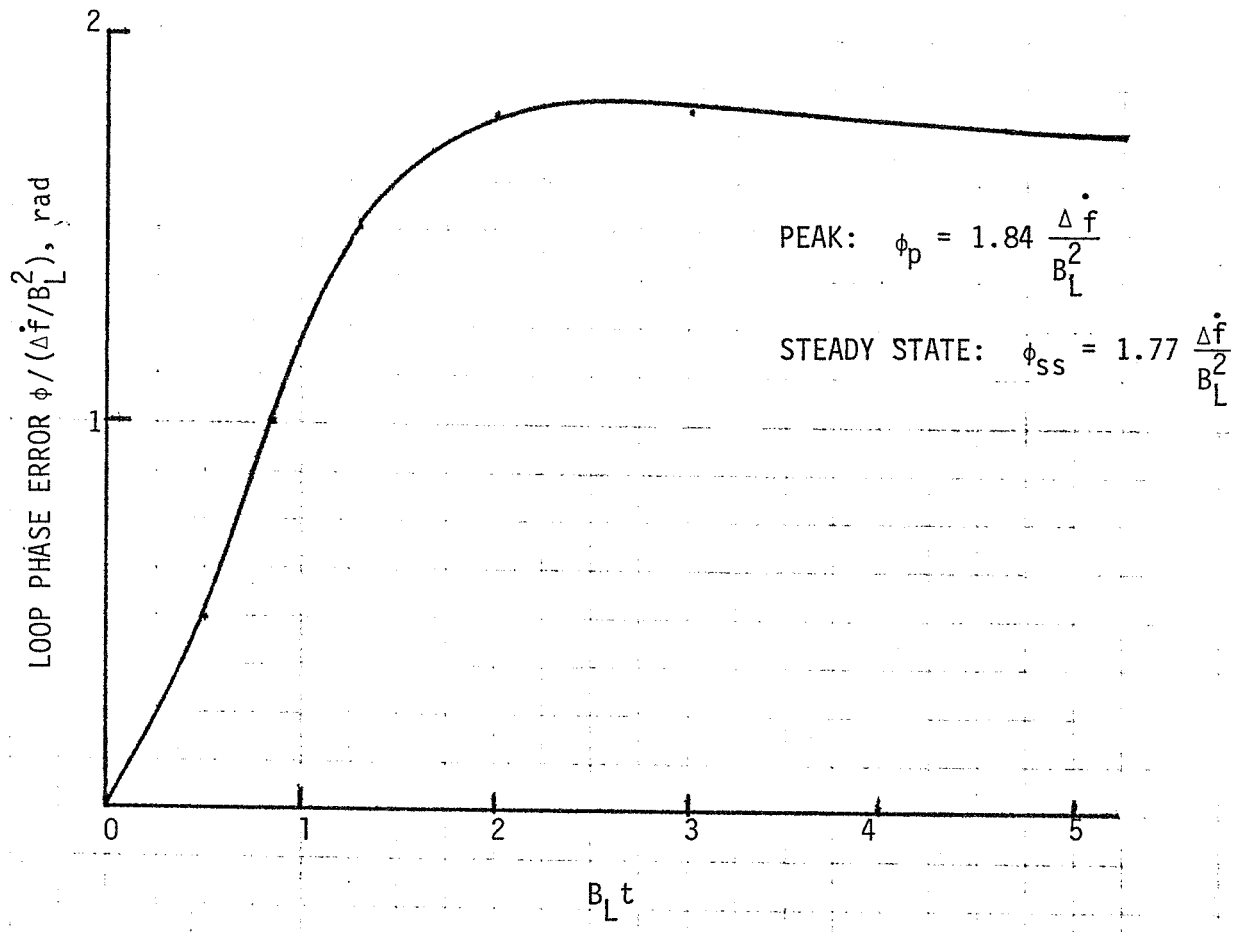


Figure 2.5-1. Loop Phase Error Response of a Second-Order Loop ($\zeta = 0.707$) to a Doppler Rate Step $\Delta\dot{f}$.

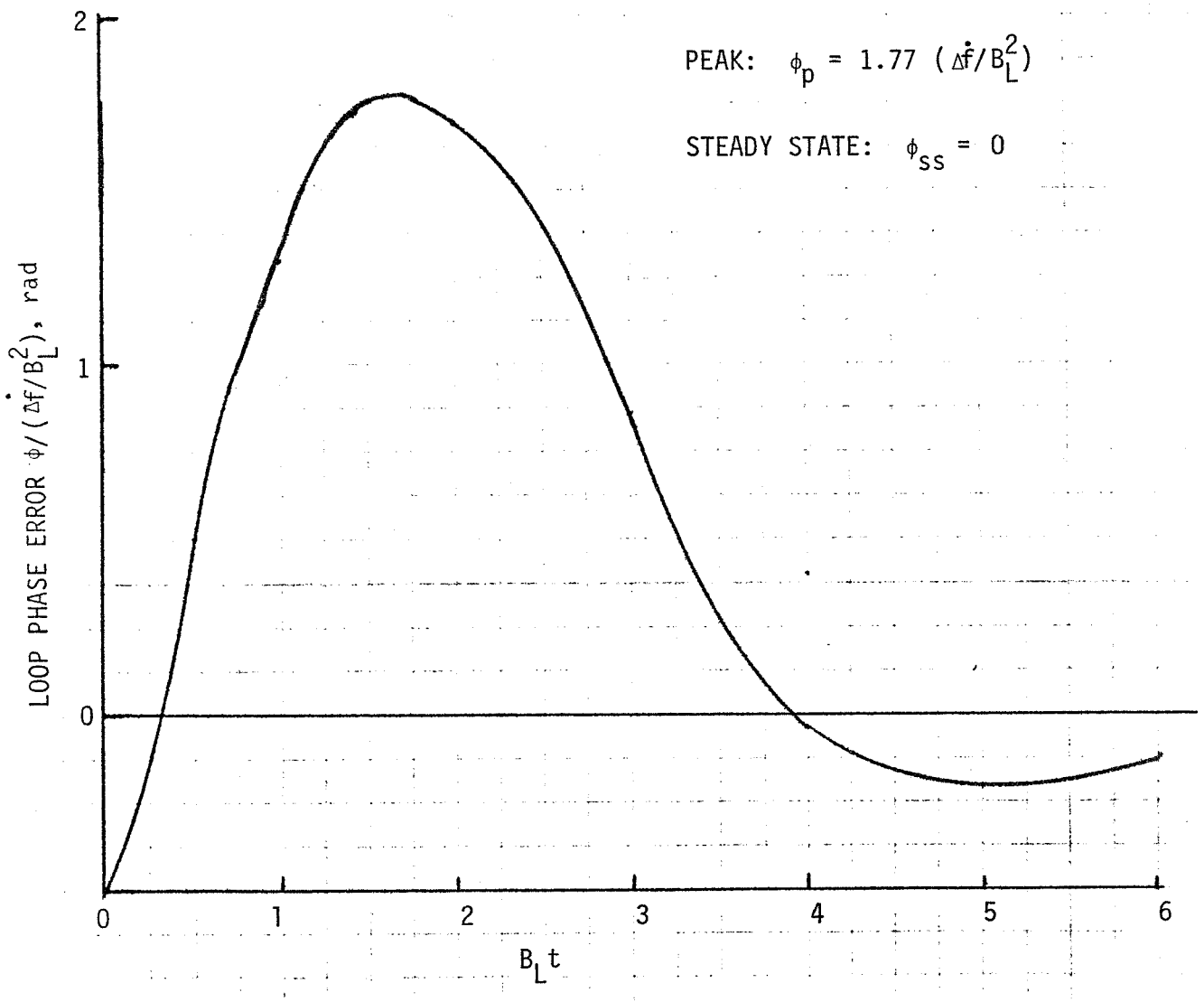


Figure 2.5-2. Loop Phase Error Response of a Third Order Loop to a Doppler Rate Step $\Delta\dot{f}$.

user dynamics. For the worst case Doppler rate $\Delta\dot{f}$ = 765 Hz/s, the peak phase error for a third-order loop (or steady state error for a second-order loop) is shown in Figure 2.5-3 as a function of the loop bandwidth B_L. However, B_L cannot be chosen arbitrarily. Assuming a worst case carrier-to-noise spectral density C/N_0 of 28 dB-Hz (i.e. 100 b/s coded operation with 8 dB E_b/N_0), the linearized loop phase error is given by

$$\sigma_\phi^2 = \frac{N_0 B_L}{C}$$

(Note that for cycle slipping consideration, the loop phase error of concern for BPSK is 2ϕ.) This is also shown in Figure 2.5-3. For acceptable BER degradation (~1 dB) and cycle slipping (~1 slip per minute) performance, the loop bandwidth must be chosen to yield a maximum rms jitter of $\sigma_{2\phi} \approx 30^o$. From Figure 2.5-1 B_L must be less than or equal to about 40 Hz. Since a steady state offset of 50° will significantly degrade the tracking and cycle slipping performance, it can only be tolerated temporarily (i.e., for a period small compared to the mean slip time). Therefore a third-order loop is needed.

2.6 RFI Mitigation Scheme

The link performance of alternative methods of quantizing received coded data for RFI mitigation was investigated as a part of the AIRS study. Each method was evaluated by a modified version of the LinCsim software package. Performance curves are based on a 1 megabit-per-second (Mb/s), rate-1/2, convolutionally coded, biphase modulated, binary-phase-shift-keyed (BPSK) signal passed through a TDRS East moderate radio frequency interference (RFI) environment.

Three alternative quantization methods were considered. They were

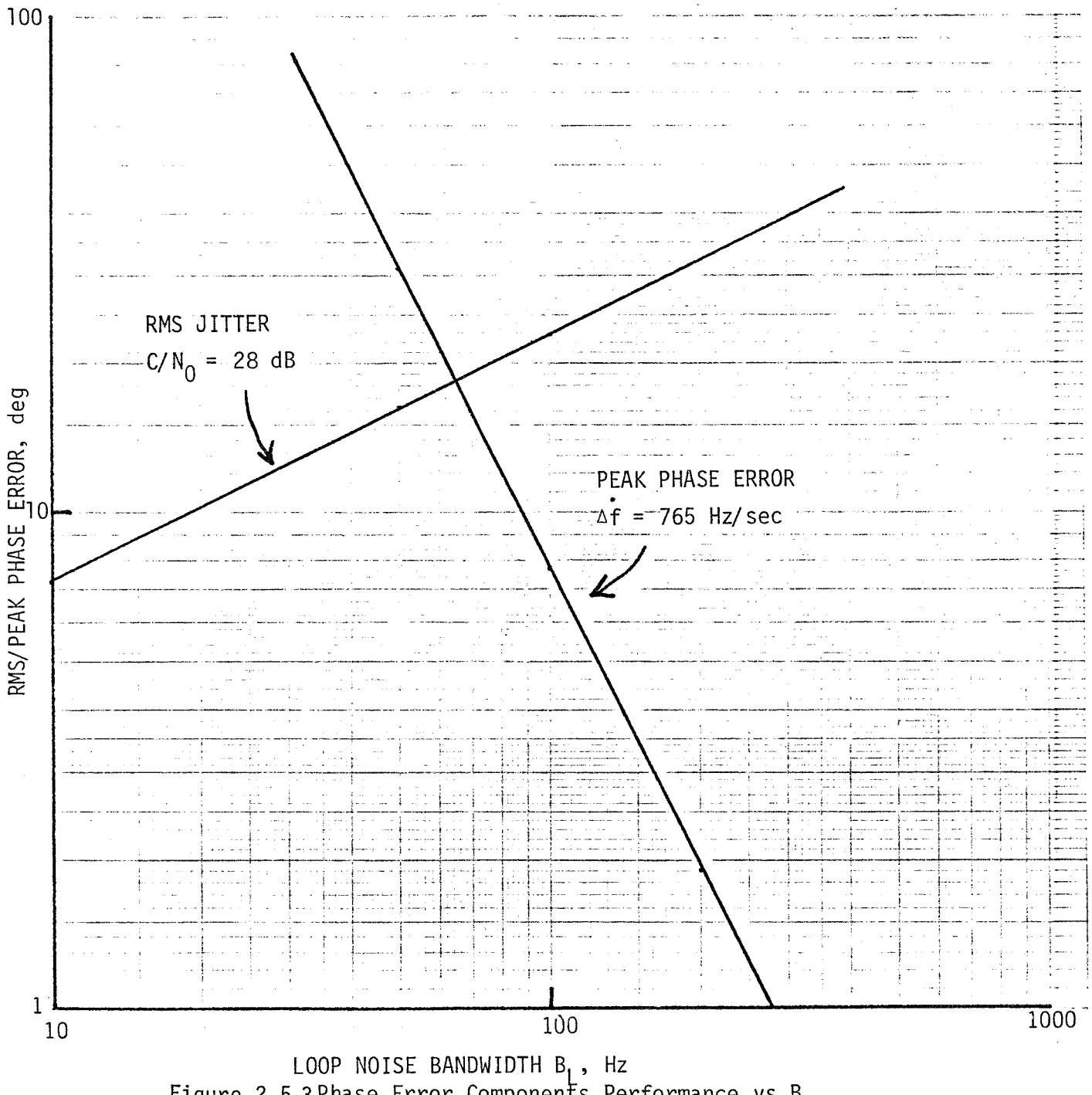


Figure 2.5-3. Phase Error Components Performance vs B_L.

chosen because they are easy to implement in hardware. The three options are:

Alternative 1: Hard limiting (2-level quantization).

Alternative 2: Variable step-size, uniform 8-level quantization.

Alternative 3: Variable step-size, uniform 8-level quantization with constant blanking.

Even a nearly optimal constant blanker fails to mitigate a significant amount of RFI. DEIRPØ, the transmitted signal's effective isotropic radiated power (EIRP) minus the EIRP needed in the absence of RFI, must be almost 4 dBW at a 10^{-5} bit error rate (BER). As Fig. 2.6-1 shows, this performance is only slightly better than that of the currently modeled quantizer.

The failure of Alternatives 1-3 to dominate the existing quantizer proves hard limiting, quantization step-size variation and constant blanking to be unsuitable quantization approaches. Some other technique of offsetting RFI is needed to clearly improve performance.

A follow-up study shows that no significant improvement of the exisiting quantizer is possible with the specified RFI environment. This conclusion conflicts with that of a previous study, primarily because it is based on a different continuous-wave (CW) RFI model. The LinCom model is compared with previous CW RFI models and the reasons for no significant improvement of the present quantizer on the TDRS East SSA return link are detailed in Appendix B.

Based on the findings (see detailed write-ups in Appendix A and B), a specific RFI mitigation scheme is not chosen for the AIRS. However, a general approach based on a Read Only Memory (ROM) implementation is

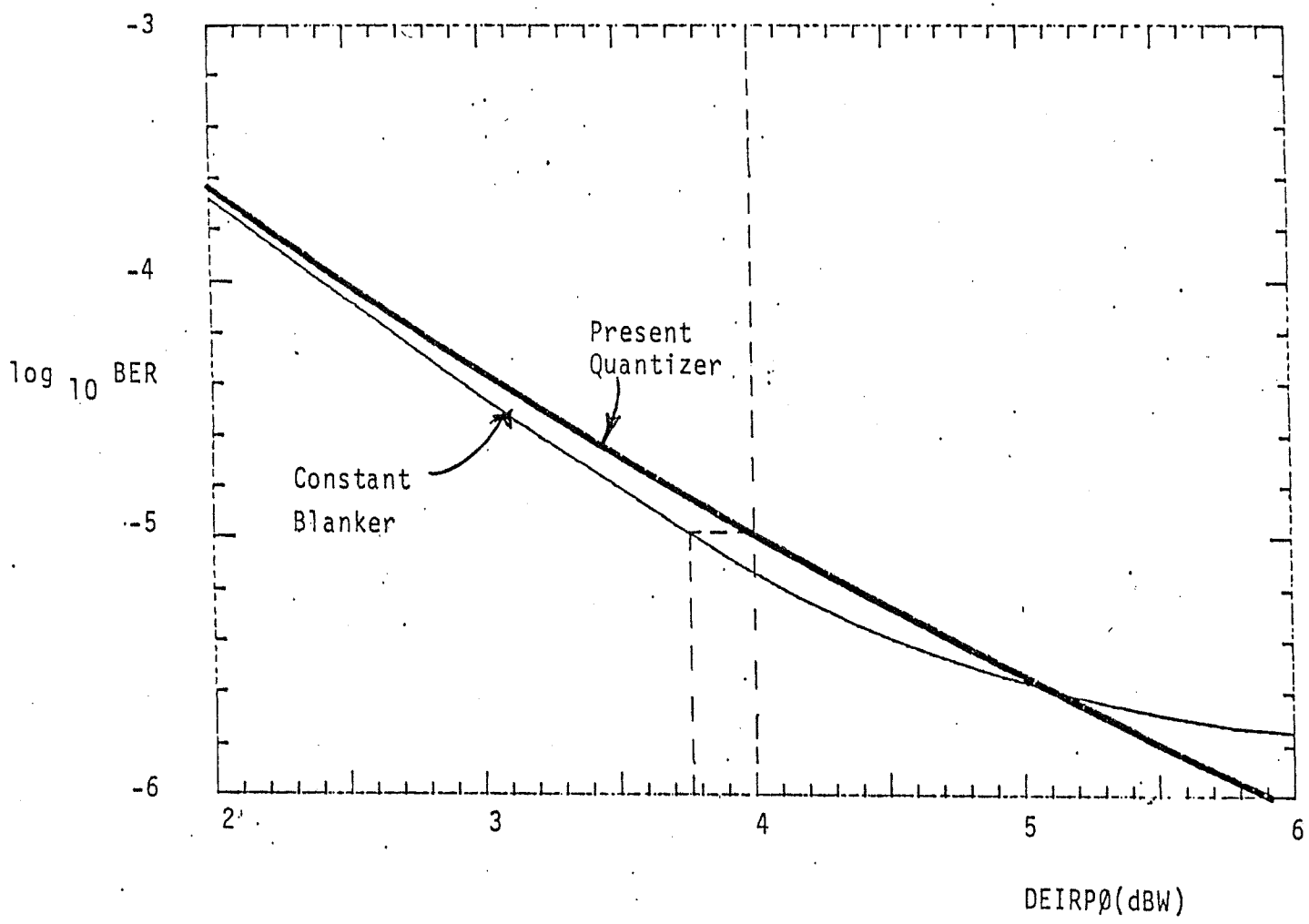


Figure 2.6-1. Performance Comparison of Nearly Optimal Constant Blanker with Present Quantizer.

prescribed for the baseline receiver. This allows hardware experimentation with other plausible mitigation schemes.

2.7 Adaptive Equalization

This section summarizes the performance improvement in terms of higher channel data throughput made possible by including an adaptive equalizer in the AIRS design. The detailed study is deferred to Appendix C. The present data rate limit is 6 Msps (per S-805) per quadrature channel for NRZ data and 3 Msps for biphase data. Since the measured 3 dB channel bandwidth of the spacecraft filter that sets the bandwidth of the SSA channel is approximately 16 MHz, one would expect it to be capable of supporting a higher data rate by employing equalization techniques.

To find out what is achievable, the SSA channel is modeled as shown in Figure 2.7-1. The performance of the tapped delay line equalizer is then simulated. The results are shown in Figure 2.7-2 and 2.7-3.

For a designed bit error rate of 10^{-5}, the performance degradation due to the channel bandwidth limitation is shown for NRZ data in Figure 2.7-2. The S-805 highest data of 6 Msps gives a $(BT)^{-1}$ of 0.38 for a 16 MHz RF channel. Without equalization, the signal loss due to filtering is approximately 1 dB. However,with a 3-tap tapped delay line (TDL) equalizer , one can more than double the data rate, specifically, achieving 13.6 Mbps with the same 1 dB loss. For biphase data, 3 Msps ($(BT)^{-1}$=0.19) operation yields a loss of approximately 0.6 dB. With the same loss, a 3-tap TDL improves the data rate to approximately 5.2 Msps.

It therefore appears that an adaptive equalizer improves the SSA channel throughput by a factor of approximately 2. However, other factors of the link such as signal distortions and channel

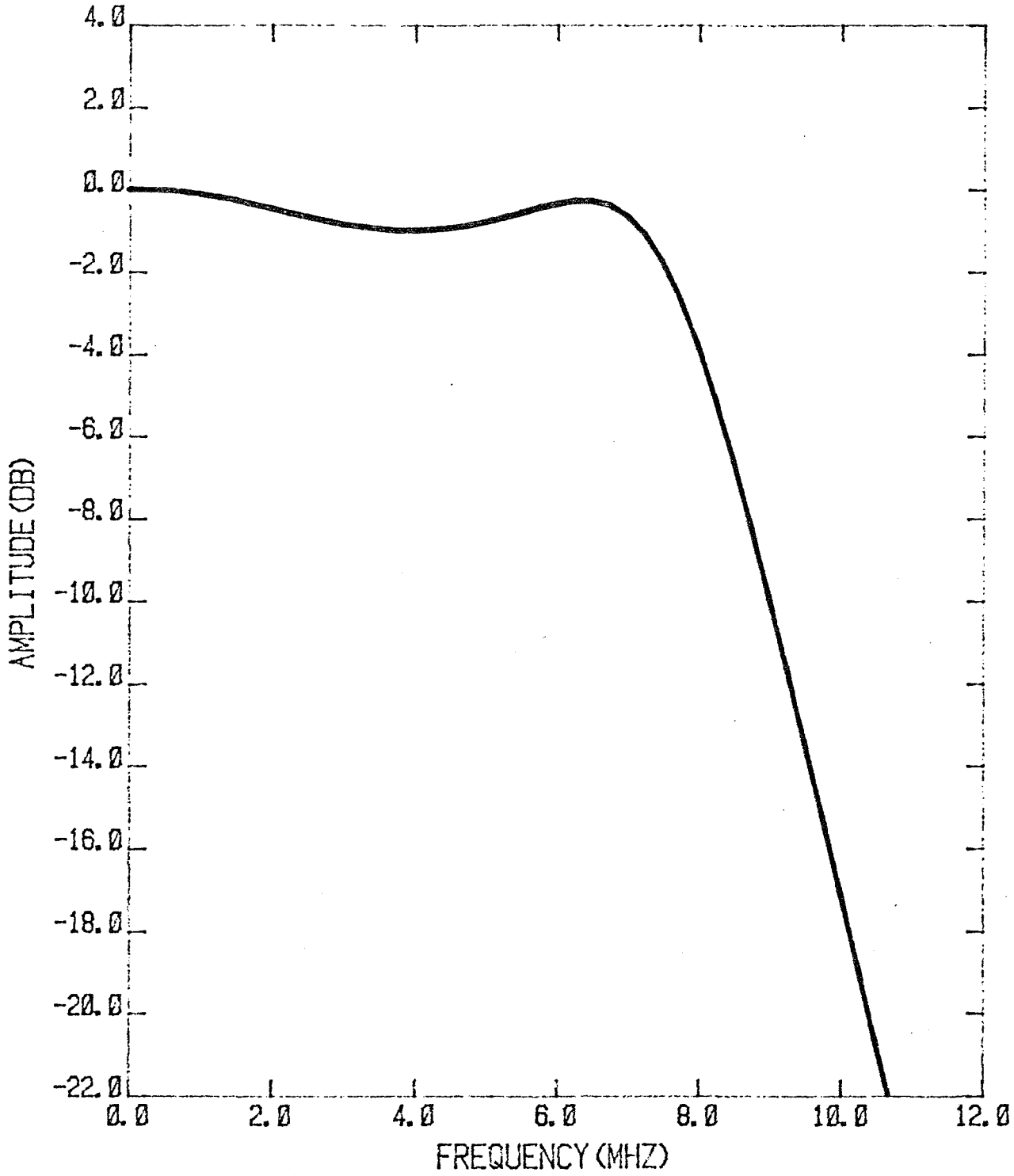


Figure 2.7-1. Simulated Channel: Cascade of a 5-Pole Butterworth and a 3-Pole Chebyshev with One dB Ripple, Both 16.5 MHz.

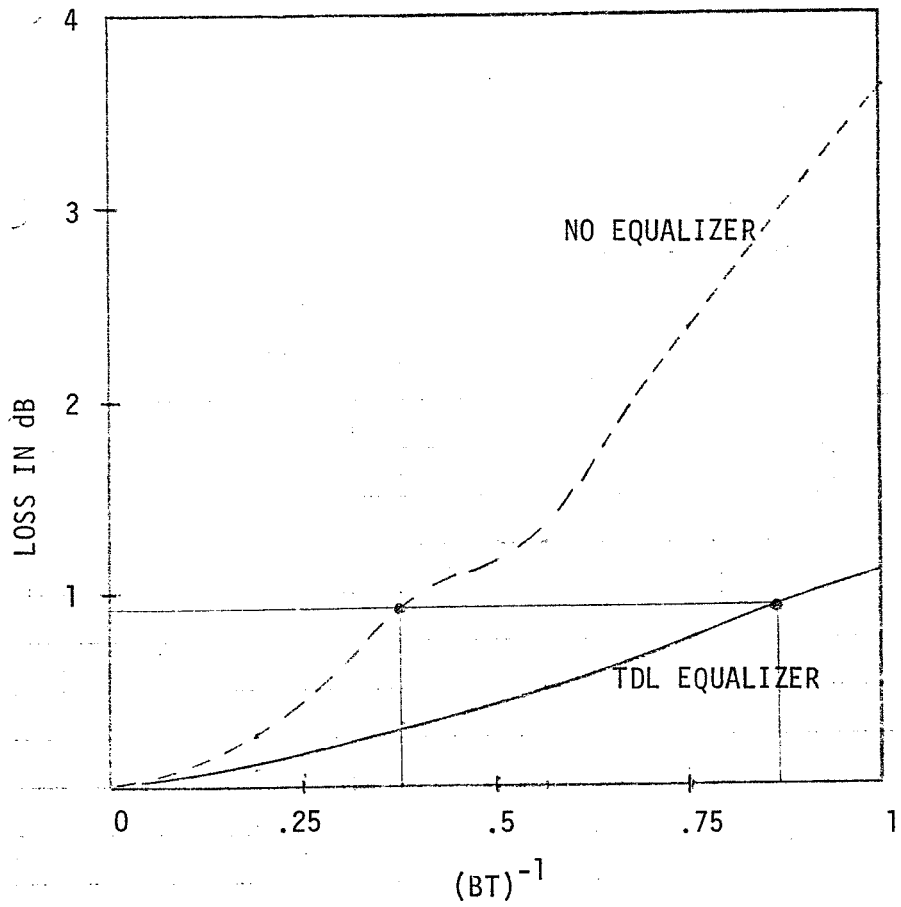


Figure 2.7-2. Performance Loss Due to Band Limited Channel.

- BPSK
- NRZ
- K=1 (3 TAPS)
- $P_E=10^{-5}$
- B=RF BANDWIDTH

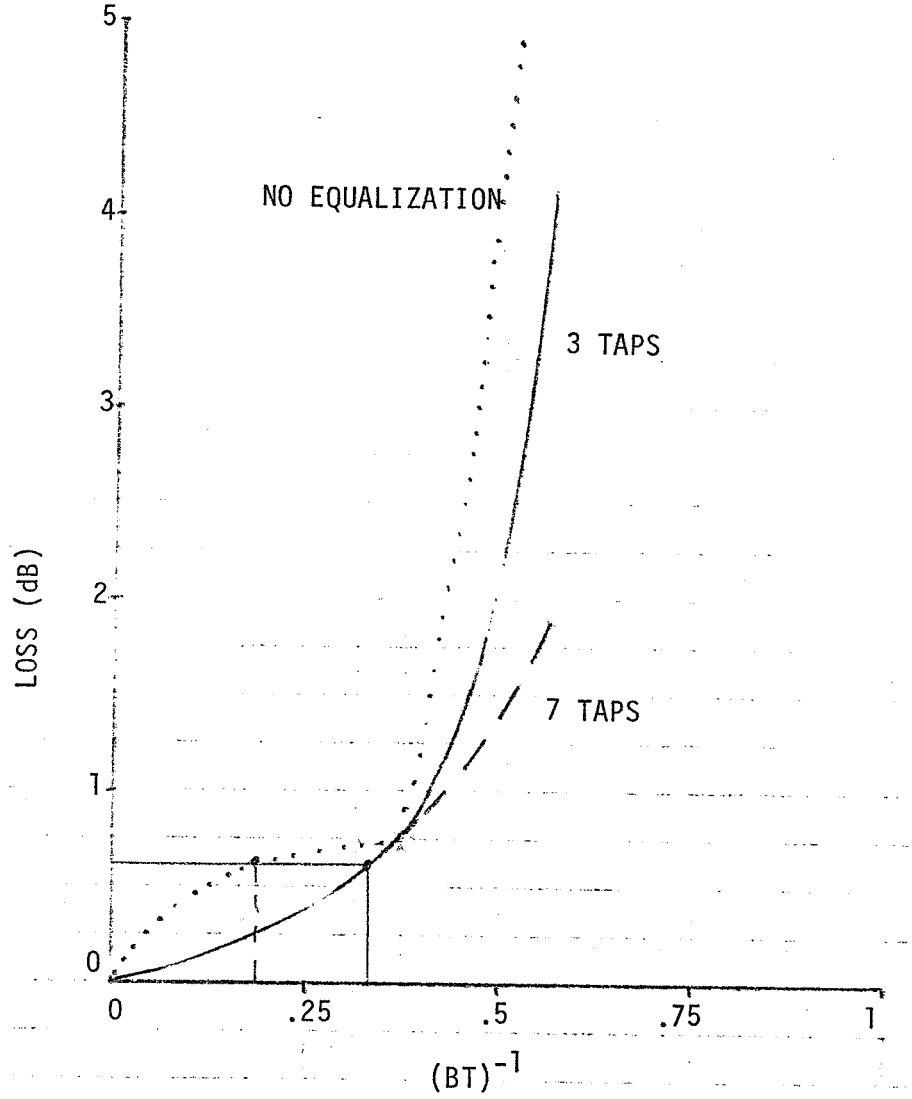


Figure 2.7-3. Performance Loss Due to Band Limited Channel

- BPSK
- BIPHASE
- $P_E=10^{-5}$
- B=RF BANDWIDTH

nonlinearities must be incorporated into the link simulation to obtain a more refined performance assessment.

2.8 Orbit Delay Estimate

The AIRS can refine its frequency predicts by estimating the orbit delay uncertainty associated with the state vector information provided as part of the set-up data*. The AIRS can accomplish this in a closed loop fashion as conceptually shown in Figure 2.8-1. A digital version of this scheme can be done easily with the computing capability of the AIRS. In what follows, the mathmetical model of this scheme is outlined.

The measured Doppler frequency f_m at the mth sampling time is the difference between the received and the nominal carrier frequency. The Doppler frequency predict f_{m-d} lags the measured frequency by dT_s, an integral multiple of the sampling period (T_s). In other words, the current Doppler predict is off by dT_s seconds. The delay/advance element uses the state vector information and the frequency prediction error ($f_m - f_{m-d}$) to compute a better estimate of the delay, $\hat{d}$. A new Doppler predict $f_{m-\hat{d}+1}$ is then generated from this estimate and a model of the Doppler frequency f as a function of time.

The key component of the loop is the adjustable delay/advance element. Its function can be characterized by a difference equation for the delay estimate $\hat{d}_{m+1}$, based on the last estimate $\hat{d}_m$,

$$\hat{d}_{m+1} = \hat{d}_m + \mu(f_m - f_{m-\hat{d}_m})(f_{m-\hat{d}_m-1} - f_{m-\hat{d}_m+1}) \qquad (2.8\text{-}1)$$

where μ is a convergence parameter defining the speed of the loop.

*A technique based on Doppler estimation which is easier to implement is described in Vol. III.

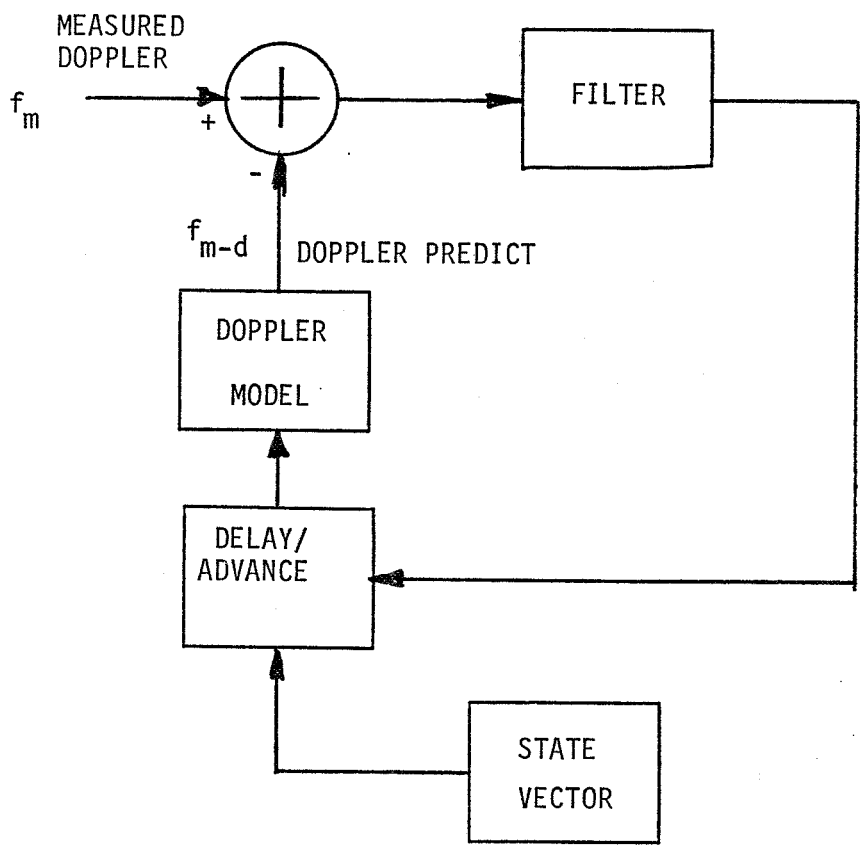


Figure 2-8.1. Orbit Delay Estimator

Equation (2.8-1) is based on an adaptive algorithm for deriving the least mean square (LMS) error estimate [8]. During each update of the delay estimate, the delay/advance algorithm attempts to minimize the frequency error $(f_m - f_{m-\hat{d}_m})$. The algorithm works well when the error has a single minimum and the Doppler frequency f does not change too rapidly.

Since the state vector information has only ±9 seconds delay uncertainty, the above conditions should be met for stable orbits. With a proper choice of the convergence parameter μ, the delay estimator can reduce the frequency uncertainty to 10 Hz in less than 45 seconds, assuming a sample is taken every second.

3.0 AIRS OPERATION AND PERFORMANCE DEMONSTRATION

The AIRS demonstration program consists of a set of functional tests designed to show its versatile operational capability and improved performance. The tests are designed to demonstrate the capability of AIRS to handle:

(a) Wide Dynamics - exceeds the dynamics specification requirement of the Wide Dynamics Demodulator (WDD).

(b) RFI - provides RFI mitigation. Techniques are selectable or can be modified via software modifications.

(c) Higher Data Rate - handles up to twice the present SSA service data rate.

(d) Low Data Rate - attains the low data rate operation (worst case C/N_0) specified by the SSA service (exceeds current equipment capability).

(e) Operational Constraints - relieves the restrictive constraints/advisories of the current SSA service.

(f) Stand Alone Operation - operates as a stand alone receiver after the initial set-up commands are received.

(g) Flexibility - allows user flexibility in switching baseband data characteristics during a user support period.

(h) Receiver Status - provides intelligent assessment of current receiver health status.

The tests are also designed to demonstrate the improved performance in various areas:

(a) Tracking - provides improved PN, carrier and bit sync tracking performance in terms of jitter, slip rate (bit slippage rate) Doppler and ranging performance.

(b) Fading Margin - provides improved receiver threshold.

(c) Acquisition - provides improved PN, carrier, bit sync and overall system acquisition time.

(d) Reacquisition - minimizes system reacquisition time by introducing selective subsystem acquisition, wait state and minisearch.

(e) Phase and Frequency Stability - uses synthesized frequency sources phase locked to station standard.

3.1 The AIRS Demonstration System

Figure 3-1 shows a high level block diagram of the AIRS demonstration system. The attenuators simulate space loss and antenna off-pointing. The RFI generator has already been acquired by NASA. One can replace the user S/C simulator with a NASA standard transponder for a real-life demonstration. The TDRS channel simulator and the SSA IF Service simulator, to be addressed shortly, are relatively simple to implement.

Figure 3-2 shows the SSA IF Service simulator, which is basically a down converter. The TDRS channel simulator, taken from Appendix A of the WDD specification, is slightly more complex and is shown in Figure 3-3 This simulator may have already been acquired by NASA/Goddard.* If not, it is relatively simple to build.

Figure 3-4 shows the user spacecraft simulator block diagram. Two data pattern generator (including convolutional encoder) output data streams are modulo-2 added to the PN generator outputs. The PN generator is capable of generating the appropriate I and Q PN codes.

*The Compatibility Test Van (CTV)/TDRSS User Transponder Test Set can be used, for example.

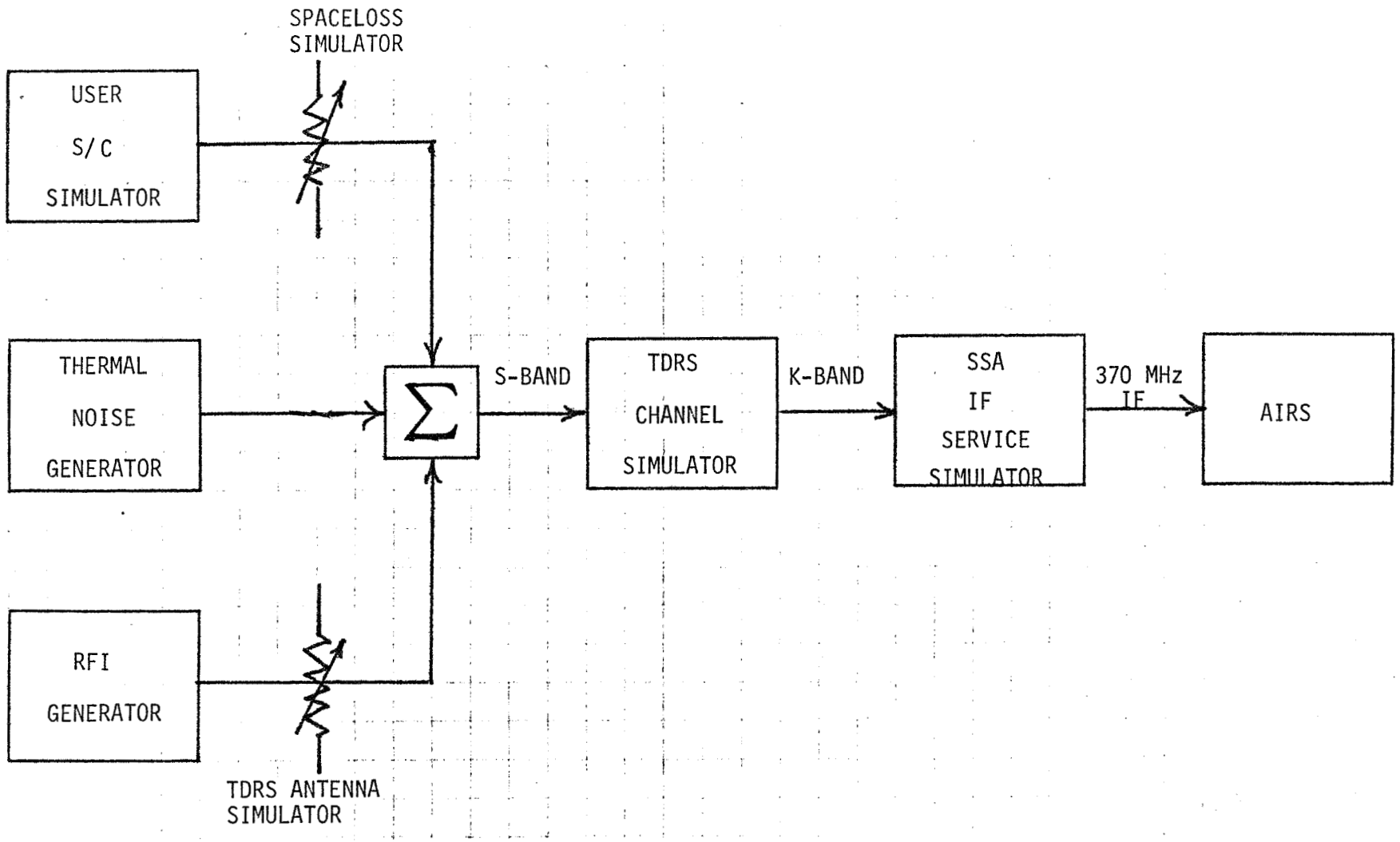


Figure 3-1. The AIRS Demonstration System.

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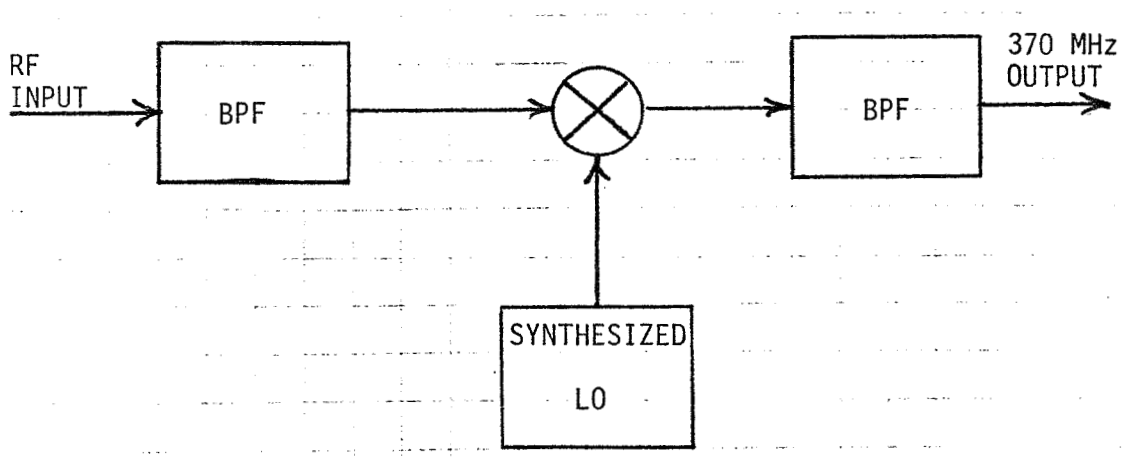


Figure 3-2. SSA IF Service Simulator.

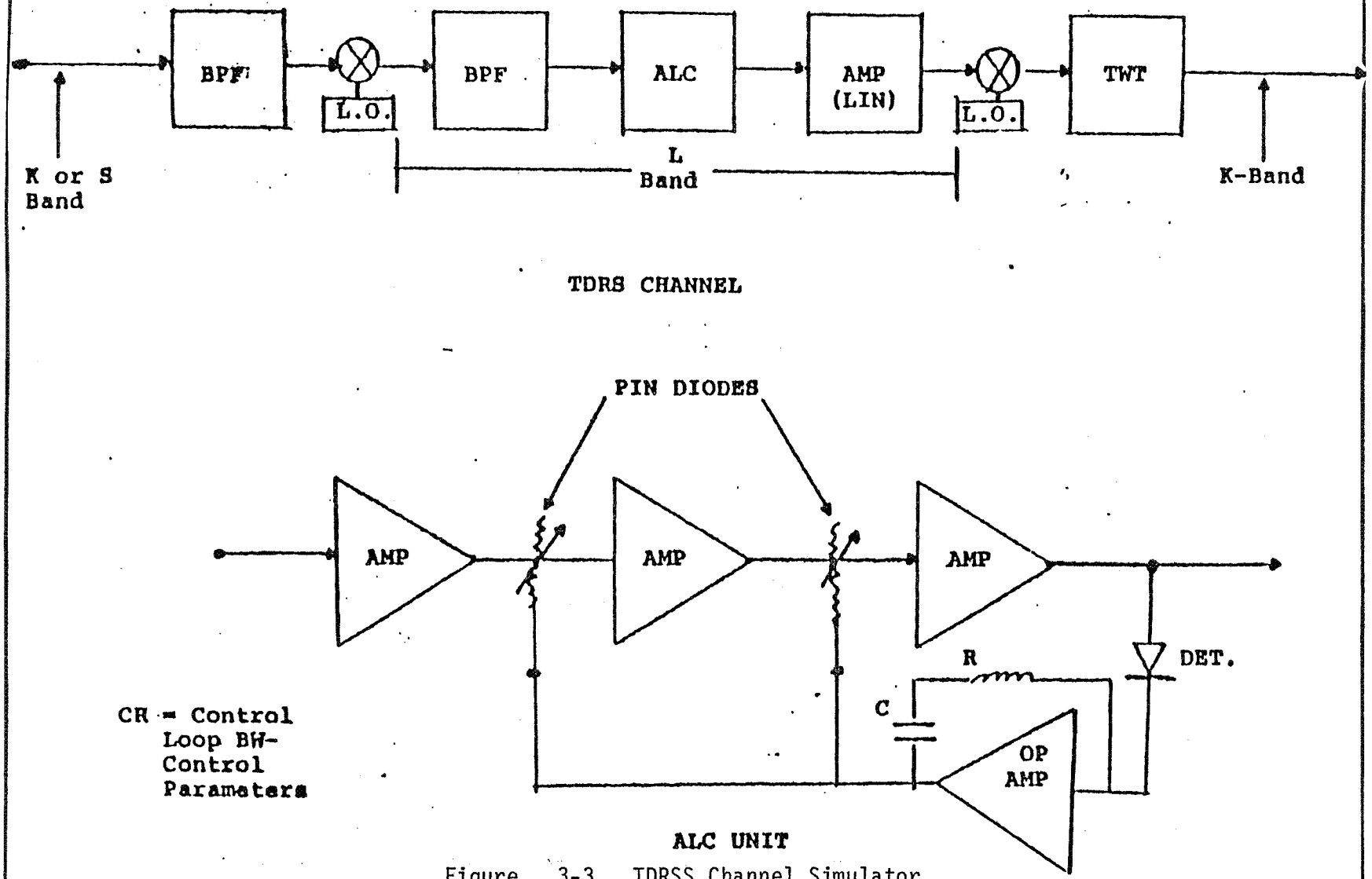
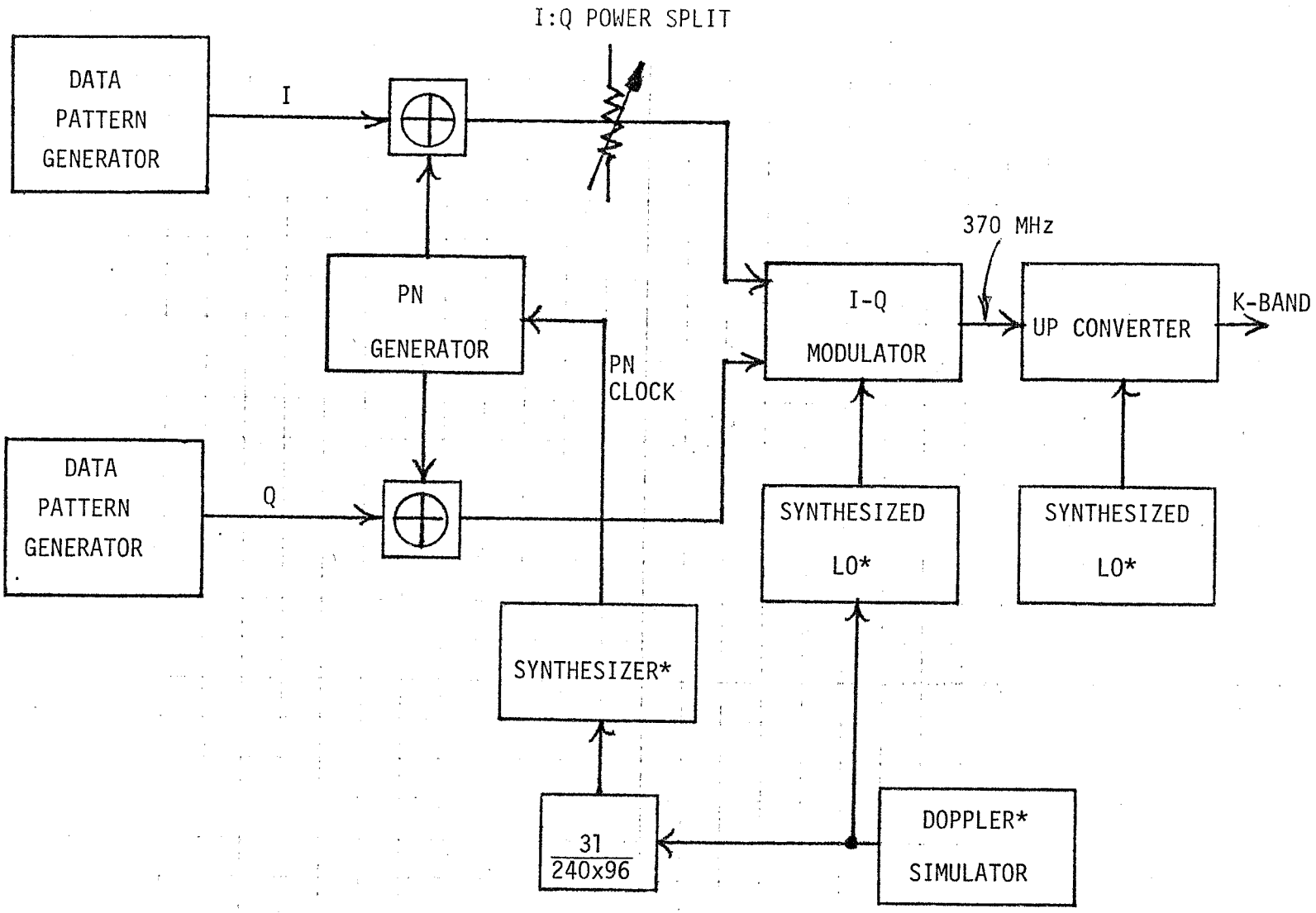


Figure 3-3. TDRSS Channel Simulator.



* COHERENT (LOCKED TO COMMON REFERENCE)

Figure 3-4. User S/C Simulator.

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The attenuator simulates the various I:Q power split. The I and Q channel baseband data then drives the I-Q modulator. The IF output is finally upconverted to the K-band. Notice that the synthesized frequency sources are coherently referenced to the same (station) reference. Channel Doppler can be simulated by a waveform generator. It is scaled for the PN code clock by the proper (carrier frequency to PN clock) ratio. An alternative way of simulating Doppler is to introduce it at the AIRS by modifying the carrier and code Doppler predictions (keeping the 31/(240x96) ratio). This can be achieved easily in software and simplifies the design of the S/C simulator.

The demonstration system described so far is based upon the assumption that one or more of the hardware subsystems are currently available to GSFC. If a completely new demonstration system is to be assembled, it is suggested that a common IF frequency of 370 MHz be used for the simulators. This approach is recommended because of its ease of implementation and cost savings. Specifically, this allows
(a) elimination of the IF service simulator, (b) elimination of the two frequency translation stages in the TDRSS channel simulator,
(c) replacement of RF amplifiers, TWT and BPF with cheaper IF units, and
(d) elimination of the last up-converter stage for the S/C simulator.

3.2 Functional Demonstration Tests

There are two types of tests for demonstrating AIRS operation and performance. The first one is the qualitative tests designed to demonstrate the AIRS intelligence. This can be accomplished visually by checking its design goals. This group of demonstrations includes: stand alone operation (autonomous modes), user flexibility (FDM), and receiver status reporting.

The other type of tests is quantitative in nature and is summarized in Table 3.1. The quantitative tests are divided into three categories: (a) Symbol/Bit Error Rate (SER/BER) tests, (b) Acquisition and Reacquisition Tests and (c) Tracking Tests. The acquisition/reacquisition tests measures are the (re)acquisition time (90% probability) for the PN, Carrier and Bit Sync loops as well as the system (re)acquisition time (PN + carrier + bit sync). During these tests, one should also check for the possibility of false locks. The tracking test measures are the slip rates and rms jitter of the PN, carrier, and bit sync loops.

The tests in Table 3.1 represent the minimum requirement to demonstrate the particular capability/performance. Since wide dynamics affects BER performance and carrier tracking performance most directly, they are recommended. It is also anticipated that RFI and higher data rate operations affects SER/BER more severely. The tracking tests quantify the performance of the Doppler and ranging system performance.

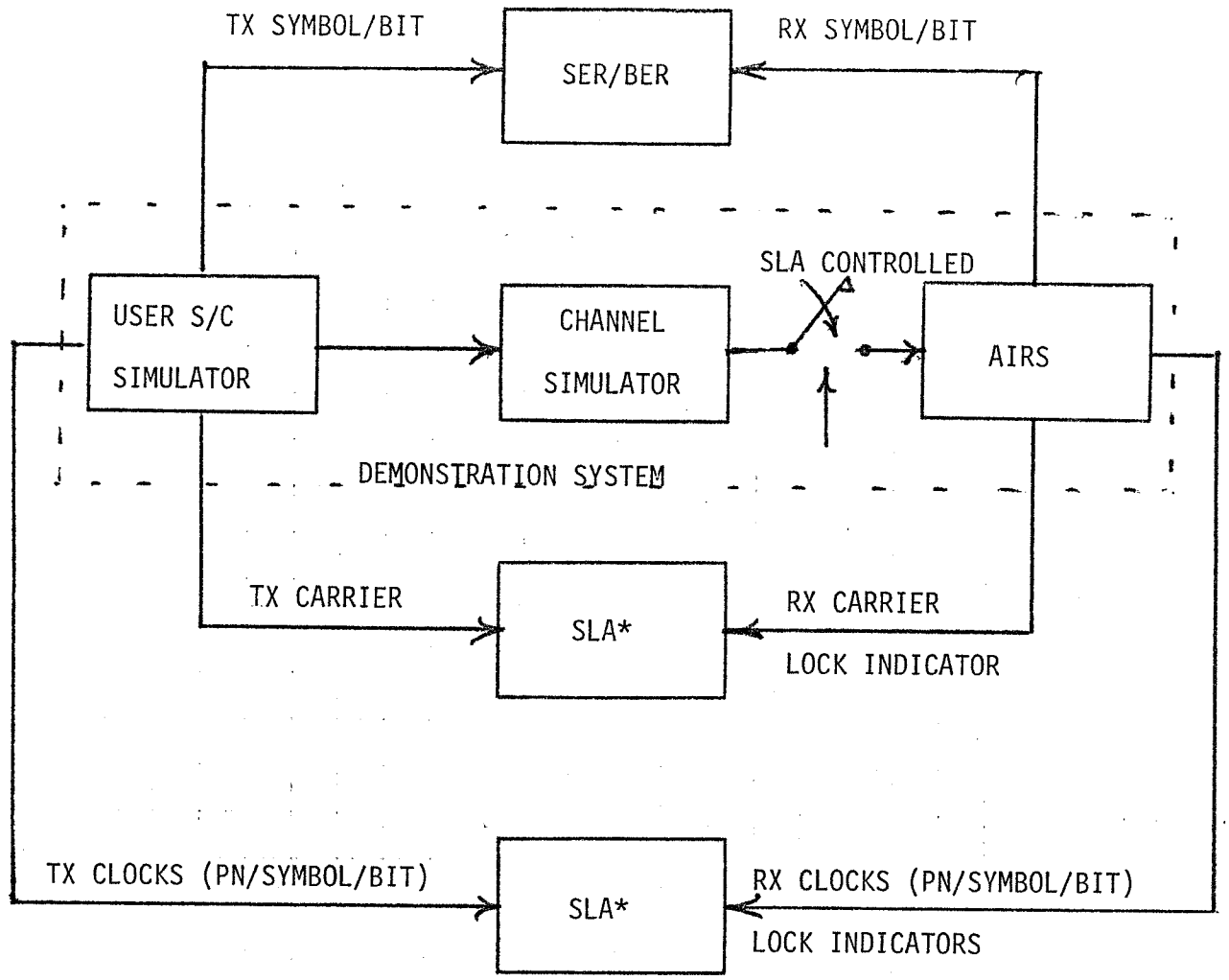
The spaceloss simulator attenuator can be manually adjusted to simulate channel fading. For reacquisition tests, the scenario for antenna switching or deep fades can be simulated by temporarily breaking the RF path.

3.3 AIRS System Test and Ancillary Hardware

Figure 3-5 shows the AIRS demonstration system and associated test hardware. The AIRS interfaces with the test operator through a terminal via GPIB. The dashed box is a simplified representation of Figure 3-1. The test hardware required are a BER test set and a Statistical Loop Analyzer (SLA). The SLA is capable of performing all the tracking and acquisition tests. A detailed description is given in Appendix D.

Table 3.1. Demonstration Tests and Measures

CAPABILITY/PERFORMANCE DEMONSTRATION	SER/ BER TEST	ACQUISITION/REACQUISITION TEST (ACQUISITION TIME, FALSE LOCK)			TRACKING TEST (SLIP RATE, JITTER)		
		PN	CARRIER	BIT SYNC	PN	CARRIER	BIT SYNC
WIDE DYNAMICS	X					X	
RFI	X						
HIGHER DATA RATE	X						
LOW DATA RATE	X	X	X	X	X	X	X
RELAXED CONSTRAINTS	X	X	X	X	X	X	X
TRACKING (DOPPLER RANGING, THRESHOLD)					X	X	
FADING MARGIN						X	
ACQUISITION		X	X	X			
REACQUISITION		X	X	X			
STABILITY			X			X	



* Note: Statistical Loop Analyzer (SLA) or Equivalent Instrument for Measuring Synchronization System Acquisition and Tracking (Carrier, Clocks) Performance.

Figure 3-5 AIRS System Tests Setup.

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Other standard laboratory instruments such as amplifiers and synthesizers may also be required.

3.4 Test Access Points

Table 3.2 shows all the test access points on the AIRS required for the acquisition and tracking tests. Receiver health status is available as part of the normal receiver serial data output.

Table 3.2. Performance Tests and Required Test Access Points.

TESTS	TEST ACCESS POINTS
BER/SER	DETECTED BIT/SYMBOL STREAMS
PN ACQUISITION	• CODE LOCK FLAG • CODE SEARCH FLAG • CODE 'all 1' EPOCH (RANGING) • CODE CLOCK
PN TRACKING	• CODE CLOCK
CARRIER ACQUISITION	• 35 MHz DOPPLER OUTPUT • 10 MHz DCO (2nd LO) • FLL LOCK FLAG • PLL LOCK FLAG
CARRIER TRACKING	• 35 MHz DOPPLER OUTPUT • 10 MHz DCO (2nd LO)
BIT SYNC ACQUISITION	• BIT SYNC SYNTHESIZER CLOCK • BIT SYNC LOCK FLAG
BIT SYNC TRACKING	• BIT SYNC SYNTHESIZER CLOCK
SYSTEM ACQUISITION (CODED DATA)	• DE-INTERLEAVER LOCK FLAG • DECODER LOCK FLAG

4.0 DETAILED DESIGN CONSIDERATIONS AND TECHNOLOGY ASSESSMENT

4.1 Hardware Design

A design study has been carried out to determine the degree of difficulty in implementing the AIRS baseline design [1]. The approach taken is to provide a receiver design that performs the functions specified in the referenced document, using currently available integrated circuits and power designs. This approach produces a low risk design that could be constructed and tested within 12 months of a go-ahead.

The block diagrams included in the following pages detail the design carried out. Figure 4-1 shows the first IF converter and automatic level control subsystem. A 335 MHz local reference is mixed with the received 370 MHz input, filtered, and amplified. After amplification, the signal level is detected and used to control the 35 MHz output level, by varying attenuators in the signal path. Amplifiers will be of the packaged, general purpose, wideband type. Gain control is provided by varying the DC current through shunt diodes used as a variable impedance sink to the signal. Two attenuator sections will be used, which will provide up to approximately 60 dB of gain control range.

The 335 MHz local signal is generated by multiplying a 5 MHz reference signal by 56 (to 280 MHz) and mixing the resulting signal with a 55 MHz signal to produce the desired 335 MHz signal. The 55 MHz signal, in turn, will be generated in a synthesizer capable of developing frequencies over a 55 ± 535 KHz range, with 10 Hz resolution.

Figure 4-2 illustrates the design of the 55 MHz Doppler compensation synthesizer. It consists of three phase lock loops. One

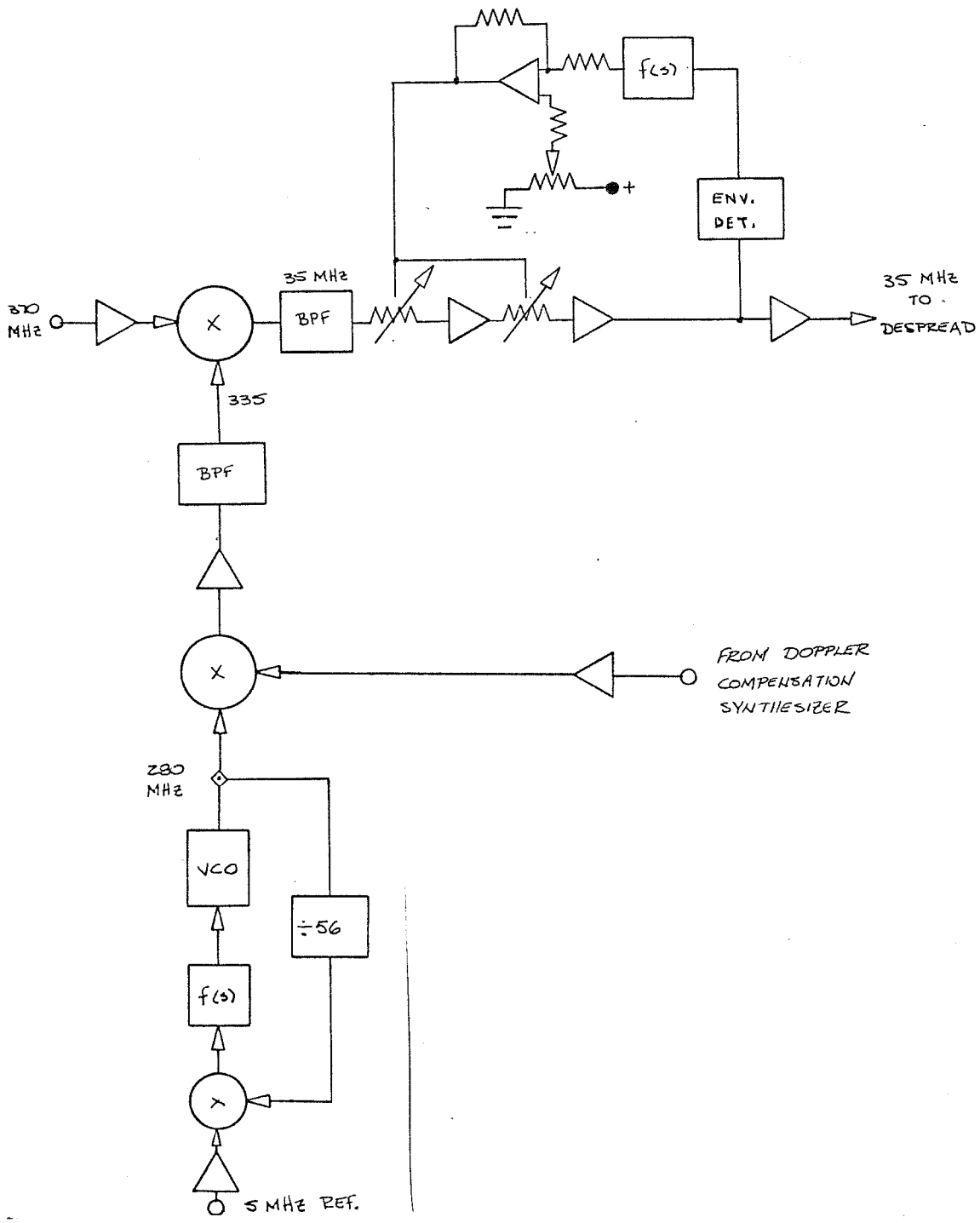

Figure 4-1. First IF Converter and ALC.

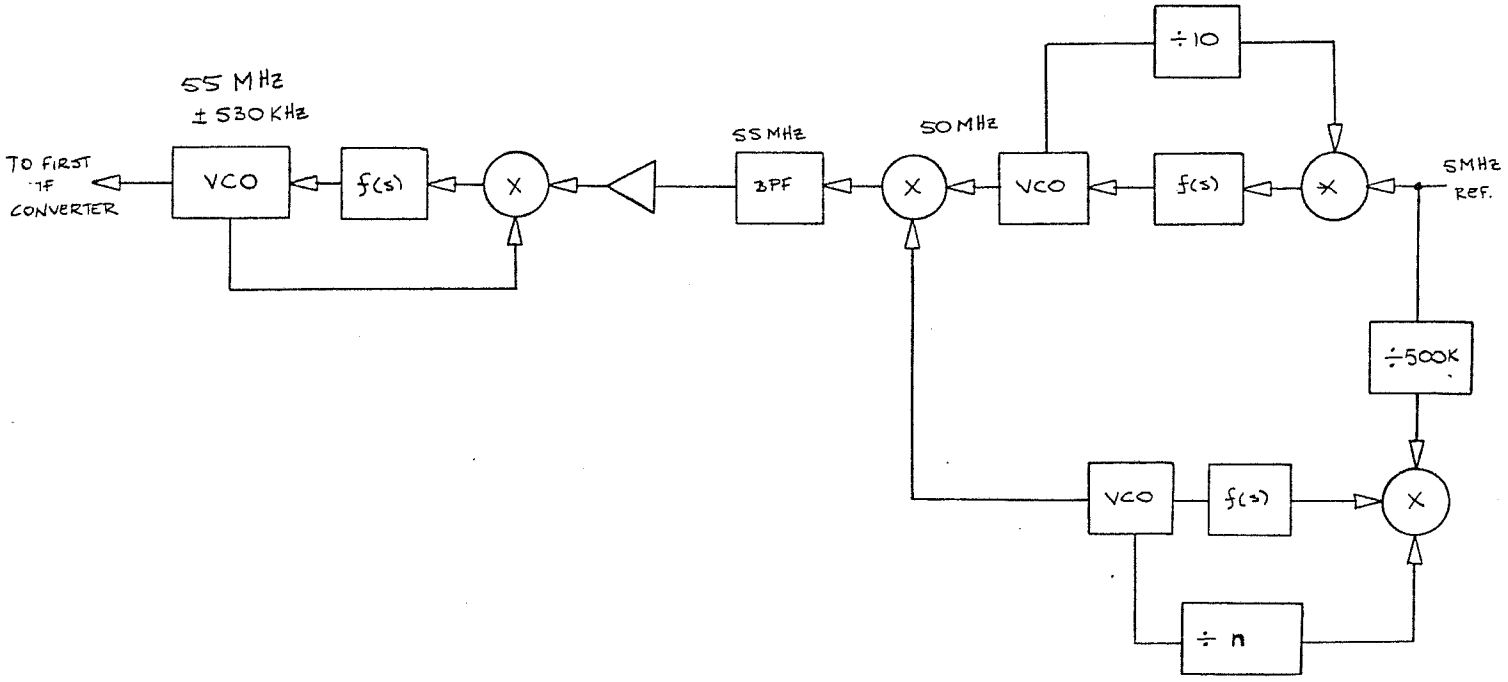

Figure 4-2. 10 Hz Doppler Compensation Synthesizer.

acts as a times 10 multiplier for the 5 MHz reference signal, which produces 50 MHz. The second phase lock loop employs a 10 Hz reference signal (derived by dividing the 5 MHz reference by 500,000) and multiplies it by the proper amount to produce a 4.465 to 5.535 MHz output signal. When mixed together, the 50 MHz and 5 MHz ± Δf signals produce the desired 55 MHz ± Δf output. A third phase lock loop at 55 MHz is used to filter the resulting 55 MHz (nominal) signal.

Acquisition is accomplished through the use of four parallel, time-offset acquisition channels like those shown in Figure 4-3. These will be controlled to operate in concert for fast synch acquisition, or they will operate independently to achieve simultaneous tracking, false lock detection, and multipath rejection.

The diagram of Figure 4-4 shows the essential elements of the logic required for searching the receiver's code in time, dithering the code generators, and providing early, prompt, and late code clocks. Thus a capability for either delay lock, dithered, or combined delay lock/dither tracking is provided.

A second down-conversion, from 35 MHz to 25 MHz, is accomplished by mixing the 35 MHz IF signal with a 10 MHz local synthesizer output. This 10 MHz synthesizer is corrected to provide fine Doppler correction, to 0.1 Hz. Figure 4-5 shows the 10 MHz ± 5 Hz synthesizer design. Here again, the implementation calls for three phase lock loops. The first is used to multiply the 5.0 MHz reference to 10 MHz, while the second is locked to a multiple of the 5 MHz reference divided by 25,000 (200 Hz). The VCO in the second phase lock loop varies between 400 Hz and 20,000 Hz, which after division by 1,000 produces a 0.4 to 20 Hz signal. This 0.4 to 20 Hz signal is then used to phase modulate the 10

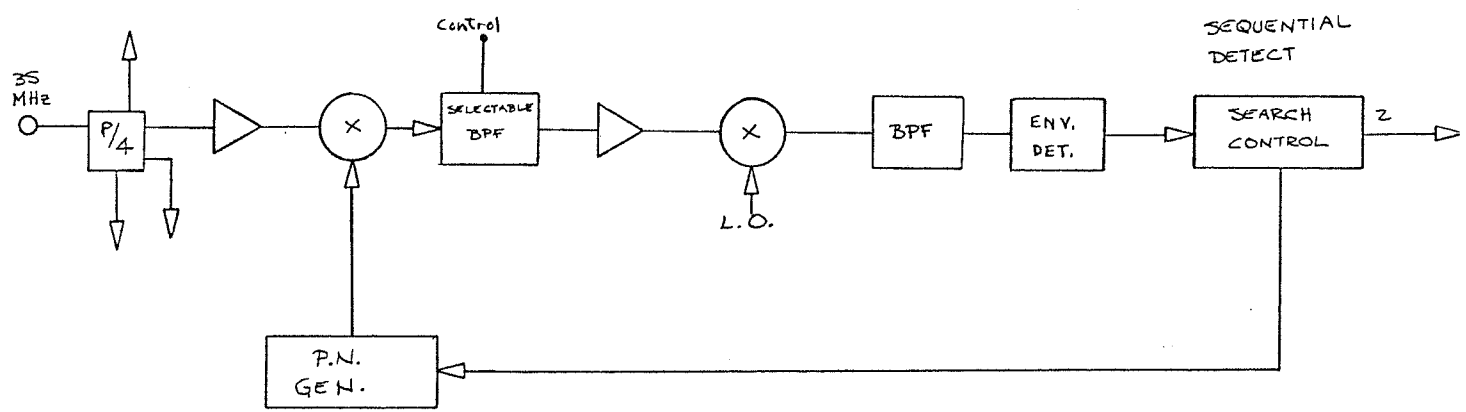

Figure 4-3. Four Channel Acquisition Subsystem (4 Units Required).

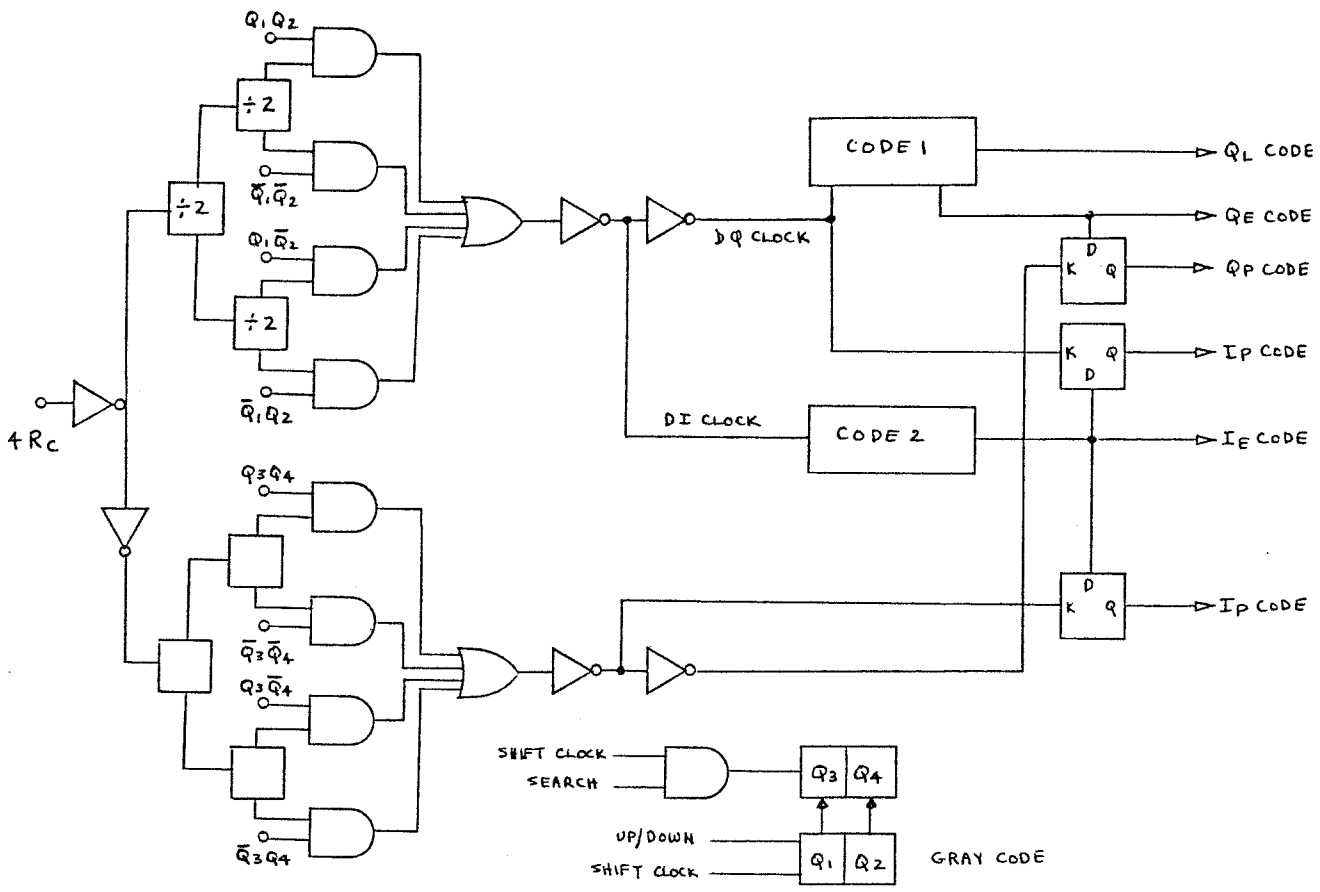

Figure 4-4. Clock Search, Dither, and Code Mechanism.

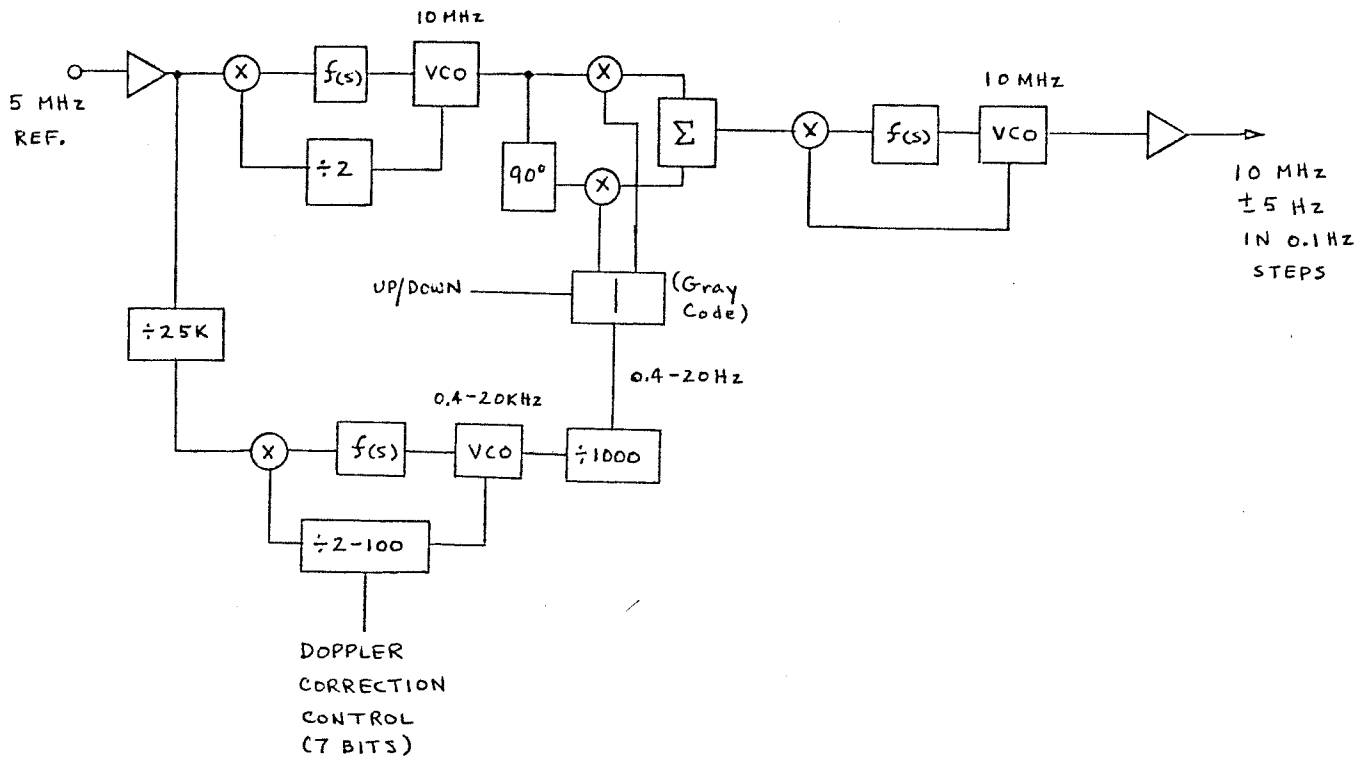

Figure 4-5. 0.1 Hz Doppler Correction Synthesizer.

MHz signal to produce 10 MHz ± 5 Hz in 0.1 Hz steps. Again, a cleanup or filtering phase lock loop is used to provide a clean output signal at 10 MHz ± 5 Hz.

The hardware implementation of the carrier acquisition subsystem is rather straightforward and is shown in Figure 4-6.

Implementation of the A/D converter subsystem in Figure 4-7 is also quite simple and straightforward. Controllable lowpass bandwidth, gain, and A/D sampling rate will be provided for maximum flexibility. Diode gain control will be used, with switched RC networks providing selectable lowpass bandwidths. The A/D converters will be standard, commercial integrated circuits, which are available with sampling rates up to 100 Ms/second and 6 bit resolution.

The remaining AIRS subsystems are less complex (though no less important) and do not at this time merit more detailed examination. The digital processor, though fast, is not overly complex in its requirements. Minimal risk is expected in developing an AIRS receiver, given that a 12-month development period is acceptable.

4.1.1 Integration

It is not recommended that any custom integrated circuits be contemplated for the AIRS receiver, for several reasons:

1. Satisfactory commercially-available circuits currently exist to permit implementation of all the functions required. The cost of custom circuits is not justified unless it is necessary to reduce the size and weight of a receiver for use in airborne or space-borne applications.
2. It is difficult if not impossible in today's industrial structure to find a manufacturer willing to devote his

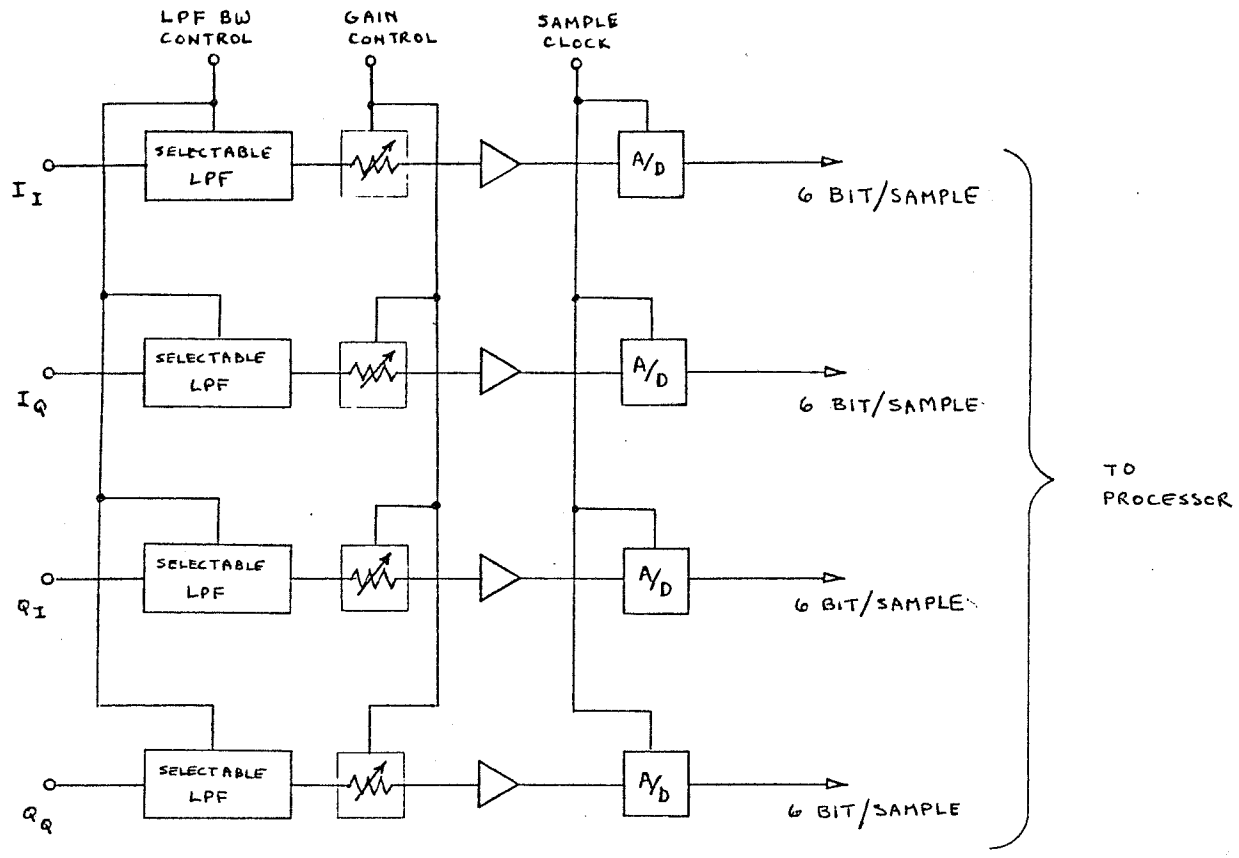

Figure 4-6. Carrier Acquisition Processing Subsystem.

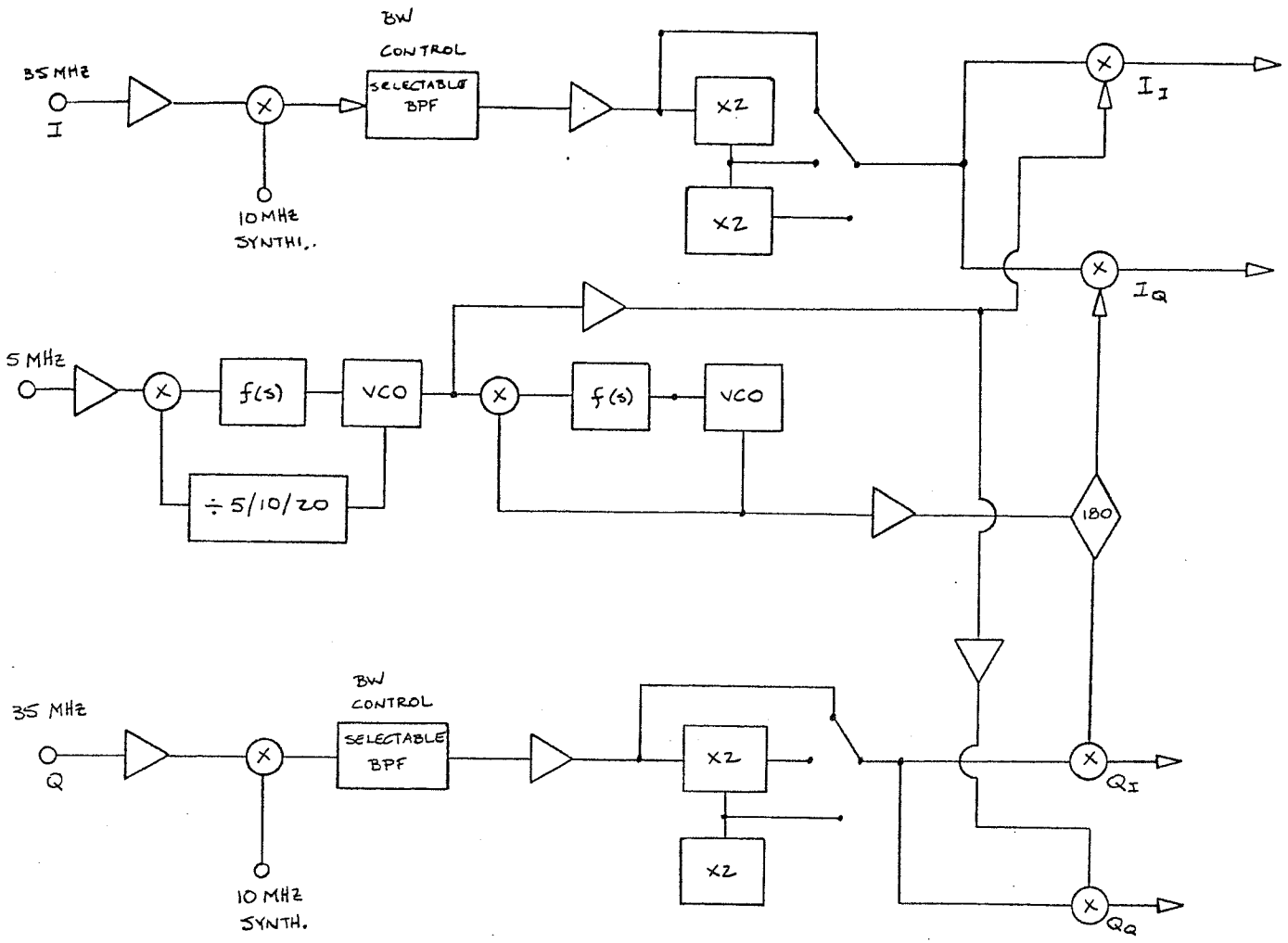

Figure 4-7. A/D Converter Subsystem.

resources to development of integrated circuits that do not have nearly universal commercial application.

3. The high cost of custom integrated circuit designs, including "master slice" approaches, together with the long time required.

4.1.2 Risk Elements

The following are risks associated with AIRS:

1. Synthesizer design for high resolution with minimal spurious signal generation.
2. Size.
3. Processor speed to handle 8x12 MHz sample rate.

These are not critical risk elements. Item 1, however, requires careful design and construction. Size is expected to be approximately 19"x12"x18".

4.2 Technology Assessment

Table 4.1 lists the more critical components and their associated performance requirements for the digital implementation of the baseline AIRS. The A-D converter and the accumulator speed are driven by a maximum 12 Mbps NRZ data rate requirement. The 4 bit ADC resolution represents a good compromise between performance degradation and the processing complexity. The multiplier/accumulator speed requirement is also driven by the data rate of 12 Mbps. The speed and size (16-bit) of the CPU are determined by the time constant of the filtering algorithms. The RAM is the primary memory system for the AIRS. This allows easy change of software--a desirable feature for prototype systems. It is also anticipated that less than 30% of the memory is to be allocated to the actual codes and data base, and the rest to be

Table 4.1. Critical Components Performance Requirements.

DEVICE	FUNCTION	REQUIREMENT
A-D CONVERTER	SAMPLING	• 96 Msps • 4 BIT
ACCUMULATOR	REDUCE DOWNSTREAM PROCESSING SPEED	• 10 ns
MULTIPLIER/ ACCUMULATOR	PREPROCESSING	• 83 ns
CPU	NUMERICAL PROCESSING (SOFTWARE)	• 1 MIPS • 16 BIT ALU
MEMORY (RAM)	SOFTWARE AND DATA BASE	•400 ns (ACCESS TIME)
MEMORY (ROM)	RFI	• 83 ns (ACCESS TIME)

allocated for possible future expansions. The high speed ROM is required for implementing the RFI mitigation processing techniques.

4.2.1 Signal Processing (Digital)

The signal processing functions to be carried out on the AIRS receiver will be implemented with a combination of hardware subsystems and microprocessor functions. The high speed analog-to-digital converters will be six bit, 100 megasample-per-second (maximum) integrated circuit units such as the TRW TDC-1029. Accumulators will be similar to the TRW TDC-1008, which is capable of a multiply-accumulate operation in 100 nsec.

It is estimated that, to carry out the functions necessary for implementing the phase lock and frequency lock operations, and the other software-implemented operations, approximately one million operations per second are required of the processor. Three currently available processors are available to meet the high rate: Signetics' 8X300, 8X305, and Digital Equipment Corporation's DCJ11. Each of these units has instruction time of 0.2 μsec, which means that the one million operation per second capability can be met if all operations can be carried out with five or fewer instructions. Then the total operation time is one microsecond or less, and one million operations can be performed per second.

Of the three micoprocessors mentioned, two (the Signetics units) are 8/16 bit units. The DEC microprocessor on the other hand is a 16/32 bit machine, which may make it much more capable, if it is available.

The processor (or processors) will output digital control signals for the local oscillator/synthesizer control, gain controls, as well as make sync decisions, estimate orbit uncertainty, and perform all other

non-hardware implemented functions listed baseline AIRS design [1].

4.2.2 Software, Hardware Timing Considerations

When determining the cycle time to perform the processors controlled functions defined in this program, one must consider both the selected hardware and the software instructions length. In selecting the hardware, it is necessary to determine which factors have the greatest impact on the overall system. The main parameter of the microprocessor selections is the time to process each instruction. When the processor has completed a function's instruction set, the output may require data in a ROM or RAM to be transferred to another location, making the ROM or RAM access time the main consideration. Obviously, for multipliers, the multiply-accumulate time is critical and for A/D convertors, the conversion rate is the key factor. These four parts, the processor, the RAM, ROMs, the multipliers and the A/D convertors form the heart of the digital signal processor. As a baseline, the following parts are being considered:

Function	Mfgr.	Part #	Key Parameter
Micro processor	Motorola	MC6800	0.375 μsec/instruction
RAM	Fairchild	100415	20 ns access time
ROM	Fairchild	93454	30 ns access time
Multiplier	TRW	TDC1008	100 ns
D/A	TRW	TDC1001	2.5 msps*

*MSPS = Mega Samples Per Second.

Below is a list of the software functions required for the AIRS system. For each function, the number of instructions has been

estimated and the cycle time calculated using the key hardware parameters listed above.

Function	Words of Inst	Cycle Time
Bit Sync	10	3.75 μs
Carrier Recovery	40	15 μs
RFI Mitigation	1000	375 μs
Doppler Compensation	5	1.88 μs
CAGC (Coherent Automatic Gain Control)	500	187.5 μs
LPI	10	3.75 μs
Adaptive Equalization	300	112.5 μs
Monitor and Control	100	37.5 μs
Self Diagnosis	200	75 μs
P/N Acquisition/Track	200	75 μs
Lock Detection	10	3.75 μs

The above estimates are based upon engineering judgments and descriptions of the functions in the proposal. To provide a more accurate analysis, it is necessary to generate computer flow diagrams and estimate the number of instruction words from this information.

5.0 COST ASSESSMENT

The cost assessment is based on the AIRS baseline [1] and Sections 3 and 4.

5.1 Prototype AIRS Estimate

The cost estimate for the prototype AIRS is divided into hardware and software cost estimates. The hardware cost total is $260,370. The detailed breakdown is shown in Figures 5-1 and 5-2. The software cost total is $194,480 and is detailed in Figure 5-3.

5.2 Ancillary Hardware

The cost estimate of the AIRS demonstration ancillary hardware is $19,401 and is detailed in Figures 5-4 and 5-5. This is based on the assumptions that a 370 MHz (RF) simulator is used and that the RFI test generator is available. It excludes $67,000 worth of standard test equipment that can be shared with other programs.

5.3 Demonstration

The cost estimate for the AIRS demonstration program is $26,180 and is detailed in Figure 5-6.

5.4 Cost Summary

The total cost estimate for the procurement and demonstration of the AIRS prototype is $499,000 and is summarized in Figure 5-7.

Cost Estimate

Engineer	
18 mm @ $25/Hr	$ 72,000
Technician	
18 mm @ $10/Hr	28,800
	100,800
Overhead @ 0.7	70,560
	171,360
Material	18,000
	189,360
G&A @ 0.25	47,340
	236,700
Fee @ 0.1	23,670
TOTAL	$260,370

Figure 5-1. Cost Estimate for AIRS Hardware.

1	5 MHz Master Clock		$ 650.00
4	High Speed A/C Conv.	$195.00	780.00
44	MWA10 WB Amplifier	15.00	660.00
3	High Frequency VCO's	300.00	900.00
50	SRA-1 Mixers	15.00	750.00
200	7400 Type I.C.'s	2.00	400.00
30	8504 Type I.C.'s	6.50	195.00
10	High Speed Accum.	200.00	2,000.00
16	35 MHz BPF	50.00	800.00
2	Chassis, Large	150.00	300.00
2	μP Card	400.00	800.00
30	PC Card	50.00	1,500.00
2	μP mem xtndr	300.00	600.00
2	Power Supply	150.00	300.00
2	Front Panel	50.00	100.00
10	Opamp I.C.'s	5.00	50.00
100	Misc Transistor	1.00	100.00
1	Set Panel Hardware		100.00
30	Chassis, Small	5.50	165.00
85	Coax Connector, Panel	2.50	212.50
100	Coax Connector, Male	2.50	250.00
500	Misc Resistor	.15	75.00
50	Misc Inductor	1.50	75.00
500	Misc. Capacitor	.35	175.00
			11,937.50
50% Contingency			5,968.75
			$ 17,906.25

Figure 5-2. Detailed Material List for AIRS Hardware.

Task Breakdown

Engineer

Algorithm Definition	3 mm
Computer Software Development	6 mm
Monitor and Control	4 mm
Verification and Simulation	3 mm

Programmer

Microprocessor Implementation	8 mm

Cost Estimate

Engineer	
16 mm @ $25/hr	$ 64,000
Programmer	
8 mm @ $15/hr	19,200
	83,200
Overhead @ .07	58,240
	141,440
G&A @ 0.25	35,360
	176,800
Fee @ .01	17,680
TOTAL	$194,480

Figure 5-3. Task Breakdown and Cost Estimate for AIRS Software Development.

Cost Estimate

Engineer	
1 mm @ $25/hr	$ 4,000
Technician	
1 mm @ $10/hr	1,600
	5,600
Overhead @ 0.7	3,920
	9,520
Material*	4,590
	14,110
G&A @ 0.25	3,528
	17,638
Fee @ 0.1	1,764
TOTAL	$19,401

*Does not include standard test equipment.

Figure 5-4. Cost Estimate for AIRS Demonstration Ancillary Hardware.

Material

1 -	BPF (370 MHz)	$2,000
4 -	Amplifiers (370 MHz) @ $30.00	120
2 -	Pin Diode Attenuator @ $60.00	120
2 -	PN Generators @ $100.00	200
1 -	Combiner	20
Miscellaneous		600
		3,060
50% Contingency		1,530
	TOTAL	$4,590

Standard Test Equipment*

1 -	SLA	$50,000
2 -	BER Test Set/Data Generator @ $6,000	12,000
1 -	Synthesizer (370 MHz)	5,000
	TOTAL	$67,000

*Rental at approximately 10% per month.

Figure 5-5. Detailed Material List for AIRS Demonstratation Ancillary Hardware.

Task Breakdown

Engineer

Test Procedure	1/2 mm
Interface/Integration	1 mm
Testing	1/2 mm

Technician

Technical Support	2 mm

Cost Estimate

Engineer	
2 mm @ $25/hr	$ 8,000
Technician	
2 mm @ $10/hr	3,200
	11,200
Overhead @ 0.7	7,840
	19,040
G&A @ 0.25	4,760
	23,800
Fee @ 0.1	2,380
TOTAL	$26,180

Figure 5-6. Task Breakdown and Cost Estimate for AIRS Demonstration.

AIRS Prototype Hardware	$260,000
AIRS Prototype Software	194,000
Demonstration Ancillary Hardware	19,000
Demonstration	26,000
TOTAL	$499,000
Standard Test Equipment	$67,000

Figure 5-7. Cost Summary for the Procurement and Demonstration of the AIRS Prototype.

APPENDIX A

ALTERNATIVE QUANTIZATION METHODS FOR IMPROVING TDRSS CODED PERFORMANCE IN A PULSED RFI ENVIRONMENT

1.0 SUMMARY

The link performance of alternative methods of quantizing received baseband data on an S-band single access (SSA) return link of the Tracking and Data Relay Satellite System (TDRSS) was derived. Each method was modeled in a modified version of LinCsim software package. Performance curves are based on a 1 megabit-per-second (Mb/s), rate-1/2 convolutionally coded, biphase modulated, binary-phase-shift-keyed (BPSK) signal passed through a TDRS East moderate radio frequency interference (RFI) environment.

Three alternative quantization methods were considered. They were chosen because they are easy to implement in hardware. The three options are:

Alternative 1: Hard limiting (2-level quantization)

Alternative 2: Variable step-size, uniform 8-level quantization

Alternative 3: Variable step-size, uniform 8-level quantization with constant blanking

Due to the flexibility of the software, a quantization method is simulated through two simple inputs to the modified program. Alternatives 1 and 2 are consequently defined as special cases of Alternative 3. The best possible constant blanker is therefore optimal among the three alternatives.

Even a nearly optimal constant blanker fails to mitigate a significant amount of RFI. DEIRPØ, the transmitted signal's effective isotropic radiated power (EIRP) minus the EIRP needed in the absence of RFI, must be almost 4 decibels (dBW) at a 10^{-5} bit error rate (BER). As

Fig. 1 shows, this performance is only slightly better than that of the currently modeled quantizer.

The failure of Alternatives 1-3 to dominate the existing quantizer proves hard limiting, quantization step-size variation and constant blanking to be unsuitable quantization approaches. Some other technique of offsetting RFI is needed to clearly improve performance.

2.0 INTRODUCTION

Pulsed radio frequency interference (RFI), emanating from certain geographic regions, has been identified by NASA as potentially degrading to communication from low orbiting user spacecraft (e.g., Space Shuttle, Space Telescope) to the Tracking and Data Relay Satellites (TDRS). The S-band return links, under the single access (SSA) and multiple access (MA) modes of operation, are of particular concern to NASA [1]. Although the impact of RFI on these links has been extensively analyzed since the problem was revealed, most of the previous RFI models have at least one underlying assumption that restricts their present applicability. Two obvious deficiencies are the assumption of infinite RFI power levels [2,3] and inadequate treatment of continuous-wave (CW) RFI [4-6]. STI [1,7,8] and ORI [9] have considered finite RFI power, but their models restrict the frequency of all in-band CW RFI to coincide with the carrier frequency of the signal. This restriction leads to pessimistic predictions of link performance, as explained in Section 2.2. In this study, we consider only finite RFI power levels and nearly uniform distributions of in-band CW RFI, so that the RFI will be modeled as accurately as possible.

The RFI model is part of the LinCsim software package [10] that will be used in comparing the performance of three alternative

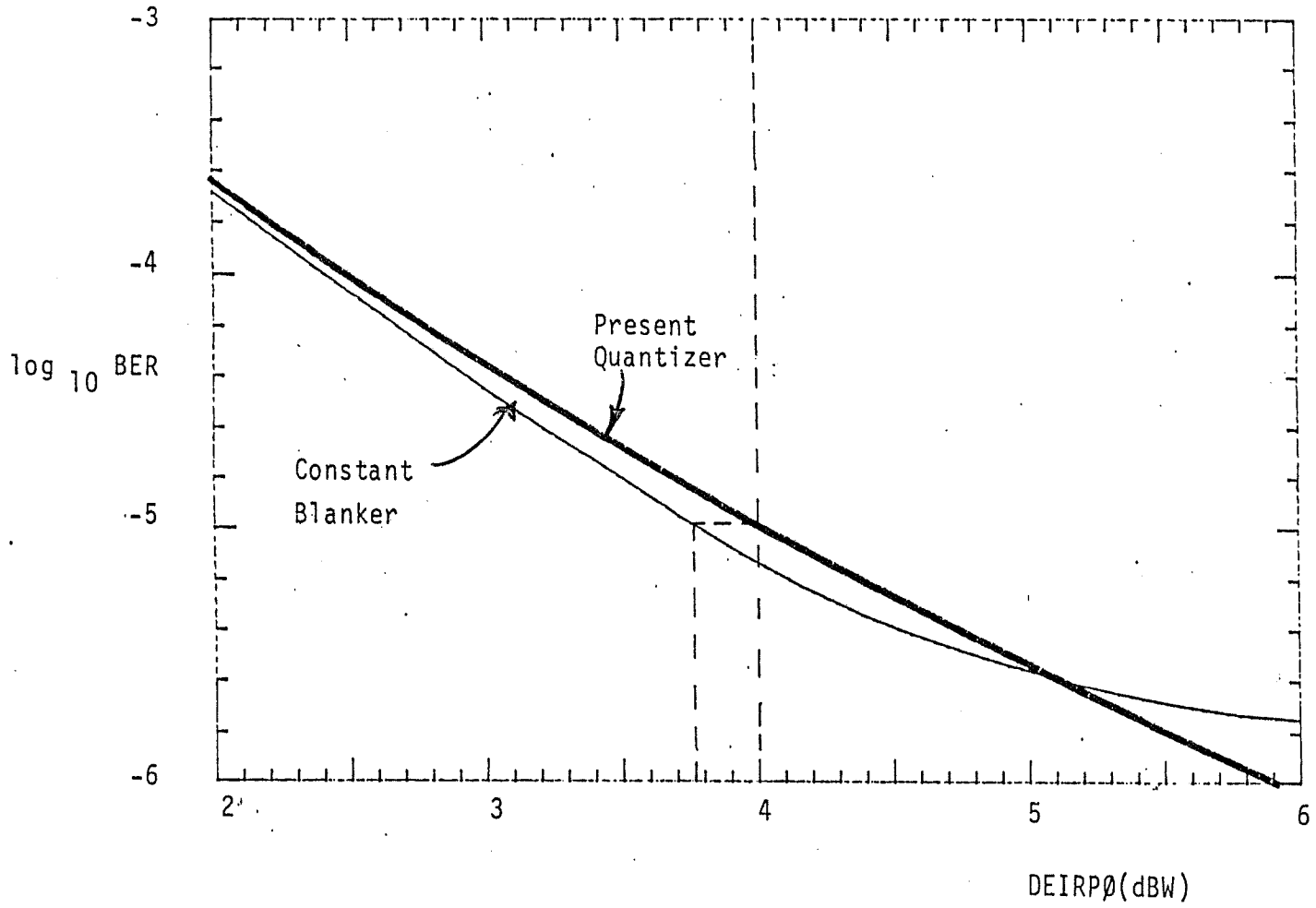

Figure 1: Performance Comparison of Nearly Optimal Constant Blanker with Present Quantizer.

quantization schemes (Section 4) and the present quantization model. By modifying the present 8-level quantizer, the TDRSS performance degradation due to RFI (Section 2.2) can be mitigated. This performance improvement is apparent only when link conditions (Section 2.1) permit a significant amount of RFI to enter the quantizer. The present study focuses on the particular SSA return link presented in 2.1, but LinCsim and the analytical procedures in Section 3 can be used to analyze the effects of quantization on a variety of TDRSS links for many different link parameters.

As described in Section 3, all three quantization options (hard limiting, uniform 8-level quantization, and 8-level quantization with constant blanking) involve equal quantization step sizes. Unequal step sizes, produced by nonlinear quantization [9], are not within the scope of this study.

2.1 SSA Return Link Model

The SSA return link consists of both an uplink and a downlink (Figure 2). A TDRS transponder relays user signals to a ground receiver. The downlink noise at the ground is assumed to be negligible, relative to uplink thermal noise and RFI.

Unless a significant amount of uplink RFI is passed into the quantizer, there is almost no difference between the present performance curve and those for the two alternative 8-level quantization schemes proposed in Section 3. In this study we investigate an SSA return link that suffers a significant performance degradation due to RFI, so that (a) communication on the link will be stressed and (b) the maximum benefit of the three alternative quantization methods will be approached. The SSA return signal characteristics shown in Table 1 were

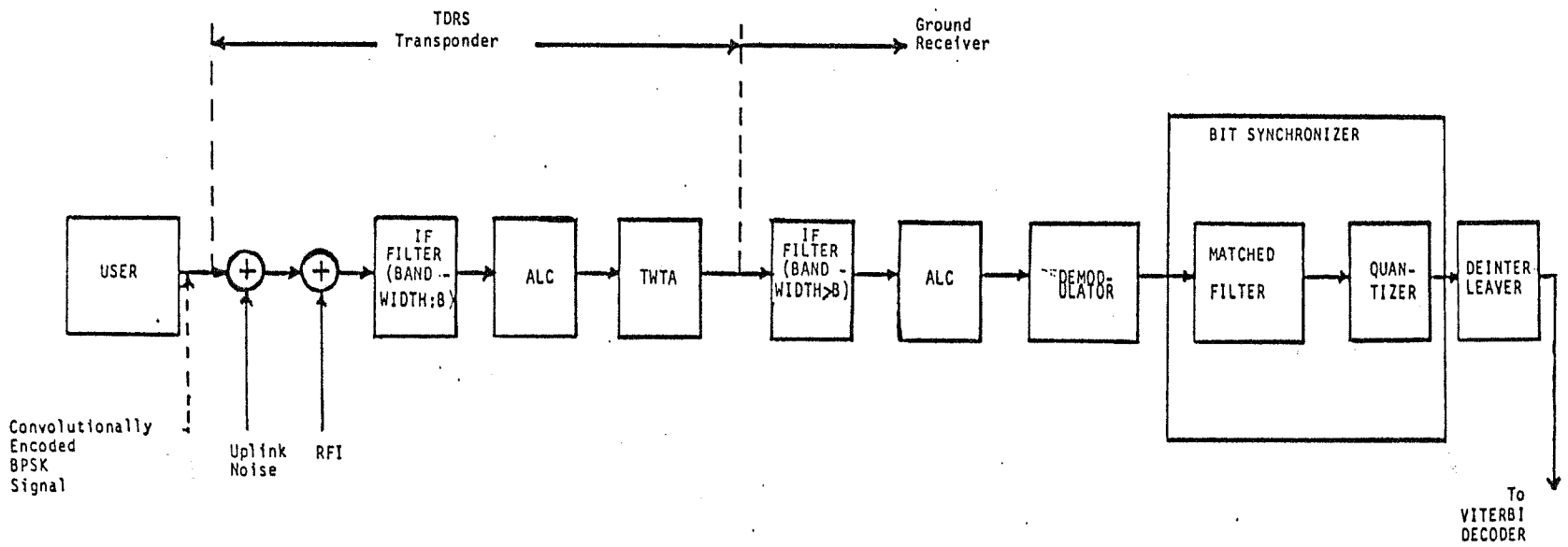

Figure 2: SSA Return Link Model.

Table 1. Characteristics of SSA Return Link Signal Used in This Study.

1. No pseudorandom-noise (PN) coding.

2. Binary phase-shift-keying (BPSK) modulation.

3. 1 megabit per second (Mb/s) data rate.

4. Rate-1/2 convolutional code.

5. No loss of RFI power due to transponder antenna offpointing.

6. Baseline bit-energy-to-thermal-noise-density ratio (E_b/N_0) of -0.680 dB at input to TDRS transponder nonlinearity.

7. Bandwidth of 20 megahertz in intermediate frequency (IF) filter of TDRS transponder.

8. Link nonlinearity consisting of 9-dB clipper and traveling-wave-tube amplifier (TWTA) with 18.5-dB input backoff in TDRS transponder and 3-dB clipper in ground receiver [13].

9. Ground station receiver loss of 5.27 dB is that necessary for a BER of 10^{-5} with baseline E_b/N_0 and no RFI.

chosen to ensure that link performance with the present quantizer is significantly, but still realistically, degraded when RFI is added to the link. Each of the link parameters (Table 1) can be directly input to LinCsim [10].

To simplify the performance analyses of alternative quantization methods (Section 4), we make several assumptions about the SSA return link (Figure 2). Only one data channel is considered, on which the modulation is binary phase-shift-keying (BPSK). Since the quantizer operates only on demodulated data, the number of channels and the modulation should only affect the absolute values of the performance curves (Section 4), not the trends illustrated by the curves. We also assume that the transmitted signal exhibits no gain or phase imbalance and no data asymmetry, as these are defined in the TDRSS Users' Guide [11].

The intermediate frequency (IF) filters in the transponder and receiver are ideal, and both filters have a bandwidth large enough to pass the signal without distortion. Nonlinearity is introduced by memoryless automatic level control (ALC) circuits [1]. The ALC circuit in the transponder is assumed to output voltages that allow for linear traveling-wave-tube amplifier (TWTA) operation, so the only pre-quantization nonlinearities are the two ALC circuits. After the rate-1/2, convolutionally encoded BPSK signal is output from ALC circuity in the receiver, it suffers multipicative losses in the demodulator, bit synchronizer, deinterleaver, and Viterbi decoder [10]. No change in these receiver losses is considered when the RFI environment changes.

2.2 RFI Problem Description

Radio frequency interference (RFI) in the SSA return uplink is

M.F. INPUT: $\cos(2\pi ft+\alpha)$, $0 \leq t \leq T$, where $\begin{cases} f = \text{frequency offset from NRZ signal frequency} \\ T = \text{symbol duration} \\ \alpha = \text{arbitrary phase} \end{cases}$

M.F. OUTPUT: $\frac{\sin(\pi fT)}{\pi fT} \cos(\pi fT+\alpha)$

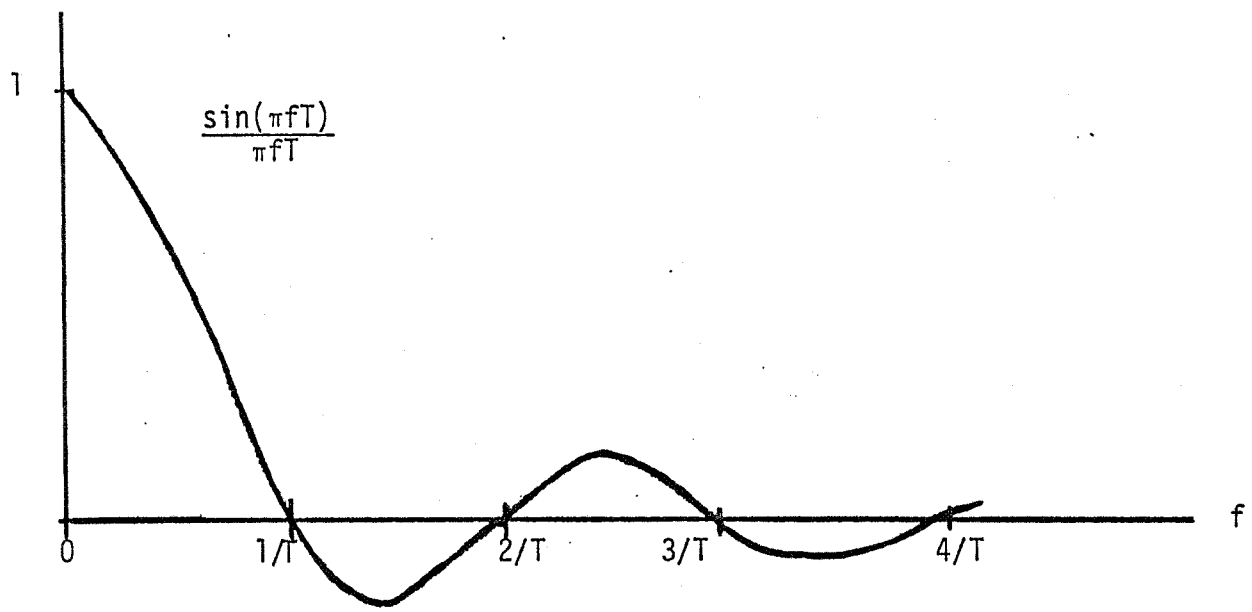

Figure 3: NRZ Matched-Filter Output When Input Is CW for Symbol Duration.

LinCom
LinCom

M.F. INPUT: $\cos(2\pi ft+\alpha)$, $0 \leq t \leq T$, where T = symbol duration

M.F. OUTPUT: $\frac{\sin^2(\pi fT/2)}{\pi fT/2} \sin(\pi fT+\theta)$

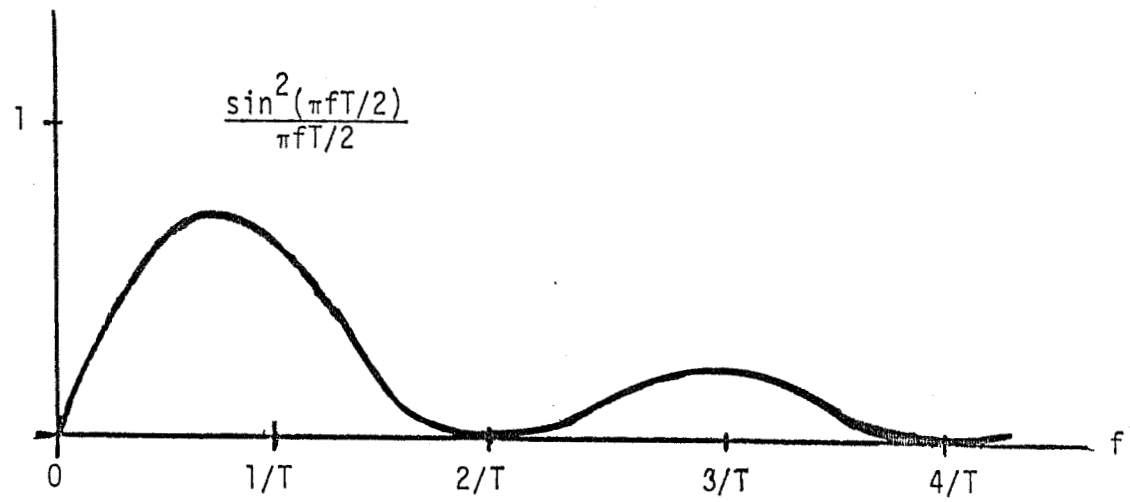

Figure 4. Biphase Matched-Filter Output When Input Is CW for Symbol Duration.

LinCom

characterized by the TDRS East RFI enviornment given in [12]. The RFI consists of three Gaussian noise processes and three CW processes. Each of the six RFI processes has a different duty cycle and power level, but every CW process has a smaller duty cycle and more power than any of the Gaussian noise processes.

All three noise components of the RFI are assumed to be Gaussian processes with flat power spectral densities in the entire passband of the TDRS IF filter. The phase of each CW component is considered to be purely random. Furthermore, the correlation time of the IF filter is less than the RFI pulse duration (3.5 microseconds (μsec)) in LinCsim [10]. The pulse arrivals of each RFI component at the transponder are assumed to be Poisson-distributed [1].

RFI pulses degrade the performance of the Viterbi decoder through their effect on the present 8-level quantizer. This effect is most apparent when the powerful RFI is received during a symbol reception. The quantizer may then assign the output the maximum decoder weight, even though the incorrect symbol may have been demodulated.

Errors of this nature may occur whenever RFI is received. Degradation on the SSA return link is particularly probable when the RFI consists of CW pulses that are long compared to the 0.5-microsecond duration of each biphase symbol (Table 1).

For non-return-to-zero (NRZ) symbol formats, the matched filter (M.F.) often outputs a large amplitude when the frequency of a CW pulse coincides with the signal frequency (Figure 3) [10]. The assumption that all CW RFI coincides with the signal frequency [1,7-9] is therefore a pessimistic assumption. In this study, we use the LinCsim CW RFI model (Section 2 of Appendix B).

3.0 ALTERNATIVE QUANTIZATION METHODS

The coded performance of the SSA return link in Table 1 can be improved by modifying the present 8-level quantizer. In the current design, a series of automatic gain control (AGC) circuits keeps the matched-filter output at a relatively constant voltage, which is used in deriving the boundaries between the eight different quantization levels [8]. The quantization boundaries, or thresholds, are modeled in LinCsim as a fraction of the mean amplitude of the matched-filter output when no RFI is received. In the absence of RFI, the thresholds are separated by $\sigma/2$ (where σ is the variance of the matched-filter output), which is the optimal separation or quantization step size for this additive white Gaussian noise channel [10].

Neither the quantizer nor its model, however, perform optimally in the RFI environment of the TDRS East return link [12]. The AGC circuits combine to form a very narrowband device, which was designed to combat only white Gaussian noise. Consequently, the quantization thresholds in the model are not directly related to the RFI on the link.

If the quantizer could prevent dominant RFI amplitudes from receiving maximum decoder weight (Section 2.2), link performance would be significantly enhanced. Ideally, the quantizer should "blank" its input whenever RFI induces a large amplitude (Figure 5). Unfortunately, little progress has been made toward a reliable method of detecting the presence of RFI. We therefore analyze three non-ideal quantization methods for the purpose of mitigating the RFI performance degradation. These are:

Alternative 1: Hard limiting (2-level quantization)

Alternative 2: Variable step-size, uniform 8-level quantization

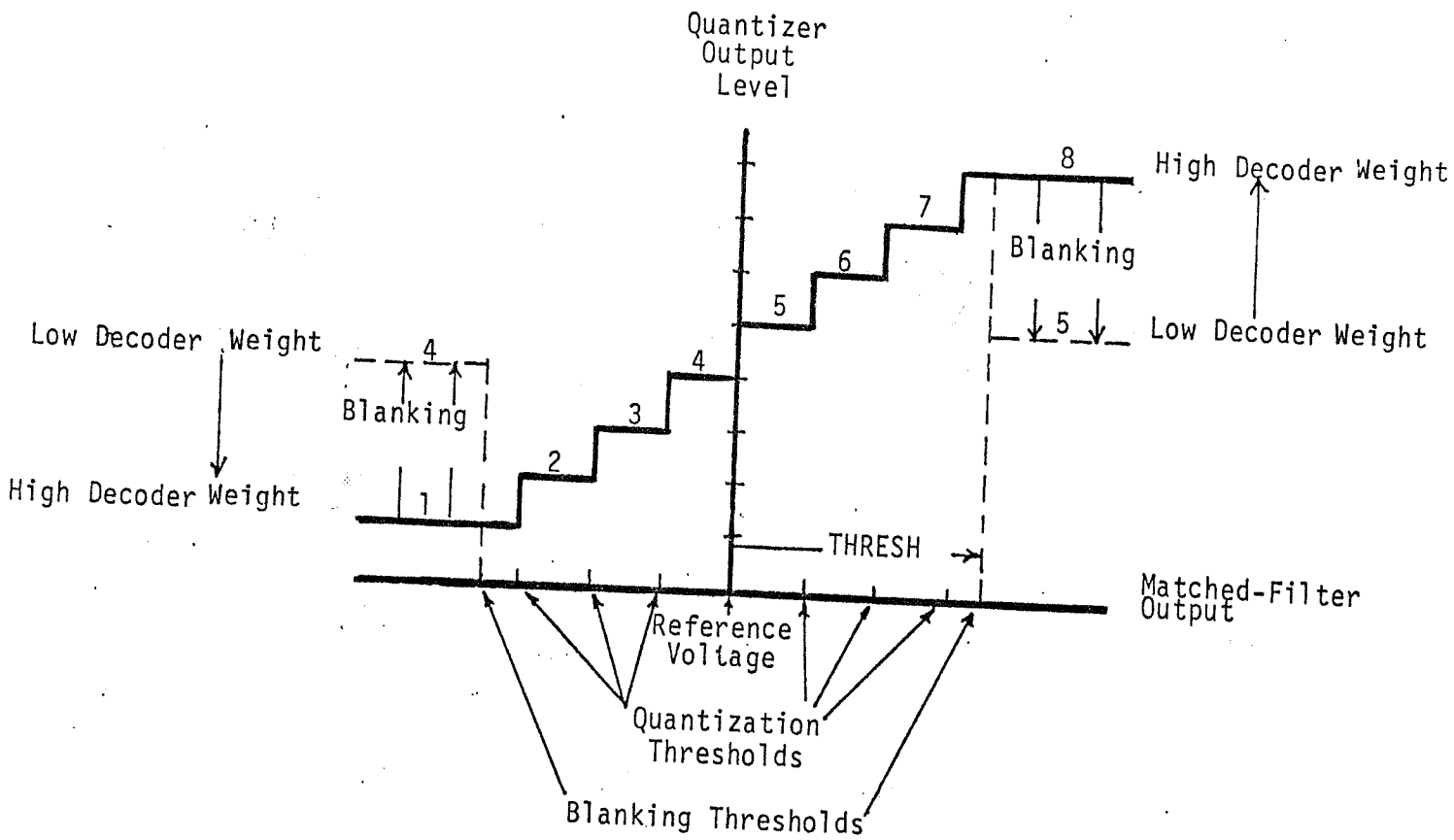

Figure 5: 8-Level Uniform Quantization with Blanking.

Alternative 3: Variable step-size, uniform 8-level quantization with constant blanking

Each of these three techniques is modeled into one software package. The software model is contained in a modified version of a documented LinCsim user program [10]. In the documented program, the reference voltage (Figure 5) of the quantizer is zero. The top three quantization thresholds are computed as k times the quantization step-size variable QSTEP (k=1,2,3); the bottom three thresholds are -k times QSTEP (k=1,2,3) [10].

Alternatives 1, 2, and 3 were programmed by modifying this present quantizer model. QSTEP was converted into an input variable, and a new input variable called THRESH was introduced. THRESH represents the voltage difference between a blanking threshold (Figure 5) and the reference voltage. The probability of a particular quantization level was altered to reflect the action of a constant blanker (Figure 5), which blanks the matched-filter output whenever its amplitude exceeds THRESH. As a result, each of the three alternative quantization methods can now be modeled through appropriate input values of QSTEP and THRESH, as discussed in the remainder of this section.

3.1 Alternative 1: Hard Limiting

A hard limiter quantizes each input into one of two quantization levels, depending on which side of a reference voltage (Figure 5) the input falls. Hard limiting was modeled in the modified version of the CLASS BER program by extremely large values ($> 10^5$) of the quantization step size QSTEP and the blanking threshold amplitude THRESH. When QSTEP is this large, the top and bottom three quantization thresholds are so large and small, respectively, that essentially all matched filter

outputs fall into Level 4 or Level 5 (Figure 5). Thus the eight possible outputs of the quantizer are effectively reduced to two. The high value of THRESH makes the probability of blanking negligible, so hard limiting is simulated.

3.2 Alternative 2: Variable Step-Size, Uniform 8-Level Quantization

Alternative 2 is 8-level quantization in which the step size is variable, although it must be uniform (quantization thresholds evenly spaced). The present quantizer is an example of this alternative, because it is a uniform 8-level quantizer with a step size that varies with the mean matched-filter output amplitude in the absence of RFI. For generality and completeness, however, the step size is arbitrary for Alternative 2. Thus the Alternative 1 step size is permitted in Alternative 2.

As in Alternative 1, an extremely high value of THRESH is entered to effectively eliminate blanking.

3.3 Alternative 3: Variable Step-Size, Uniform 8-Level Quantization with Constant Blanking

The Alternative 3 quantizer repeats the operation of the previous quantizer and then blanks the result (Figure 5). In addition to the reference voltage and six quantization thresholds, the blanking quantizer has two blanking thresholds. Contrary to Alternatives 1 and 2, the blanking threshold amplitude THRESH in this quantizer may be small enough to make the probability of blanking significant. The only restriction on QSTEP and THRESH is that they be positive, so Alternative 1 and Alternative 2 are contained in Alternative 3.

4.0 PERFORMANCE COMPARISON OF ALTERNATIVE METHODS

All three alternative quantization schemes in Section 3 were individually analyzed for the purpose of comparing their performance on

the SSA return link of Table 1. The analyses consist of executions of the LinCsim bit error rate (BER) user program [10] with appropriate modifications of the quantizer (Section 3). Since the decoded BER can be output from the modified version of the program, the BER is the performance measure of the alternative quantization methods.

Before the BER could be computed, the values of all input parameters to the modified program had to be determined. In addition to the quantizer inputs QSTEP and THRESH (Section 3), the modified BER program has two input variables, RXLOSØ and DEIRPØ, which are significant. RXLOSØ represents the multiplicative losses suffered by the signal component of the receiver ALC output as it passes through the demodulator, bit synchronizer, deinterleaver, and Viterbi decoder (Section 2.1). DEIRPØ is the transmitted signal EIRP relative to the baseline signal EIRP as defined in the BER program user manual [10].

RXLOSØ was computed by executing the documented CLASS BER user program, <u>not</u> the modified BER program. The SSA return link parameter values in Section 2.1 and a channel with no RFI were input. The input parameter NRXLOS [10] was set to zero so that the receiver-loss output is the one at which the BER is 10^{-5}. All other input parameters were set to their default values [10] and a receiver loss of 5.2682 decibels (dB) was output. Since the multiplicative losses are assumed to be independent of RFI (Section 2.1), RXLOSØ is 5.2682 dB throughout the performance analyses of the three alternative quantizers.

DEIRPØ, on the other hand, was chosen as an independent variable for the analyses. The transmitted signal EIRP is closely related to the bit-energy-to-thermal-noise-density ratio (E_b/N_0) at the input to the demodulator when the other parameters of the link model are held

constant. This is the case for all plots of BER against DEIRPØ in this report, so the BER depends on DEIRPØ in almost the same way as it depends on E_b/N_0 in these plots.

Except for DEIRPØ and the quantizer variables QSTEP and THRESH, no conditions were allowed to vary on the SSA return link as Alternatives 1-3 were investigated. The TDRS East RFI environment presented in [12] and the return link characteristics described in 2.1 were input. All input parameters which are not mentioned previously in this report, were allowed to default [10].

Each computation of the bit error rate (BER) in the quantization analyses was based on serveral assumptions. Conditioned matched-filter outputs were assumed to be Gaussian random variables and the high data-rate model was used to compute RFI effects on the outputs. In this model, (a) no RFI pulses overlap in time, and (b) all or part of at most one RFI pulse is received during a symbol reception [10]. As in the documented BER program, each matched-filter output was approximated by adding independent time samples of the matched-filter input. The samples were taken at rate B [10], the one-sided bandwidth of the transponder IF filter. After the matched-filter outputs were quantized, the BER was computed as a function of the computational cutoff parameter R_0 [1].

The performance analyses of Alternatives 1-3 are successive executions of the modified BER program, with each result based on different combinations of the inputs QSTEP, THRESH, and DEIRPØ. Transmitted signal EIRP is effectively the only variable in the Alternative 1 analysis, because the quantization step size and blanking threshold are immaterial in a hard limiter. Alternative 2 also has no

blanking, so QSTEP and DEIRPØ are the two variables for this quantizer.

The BER is plotted as a function of DEIRPØ for Alternatives 1 and 2 in Fig. 6. $QSTEP_0$ is the quantization step size for the existing quantizer, so the curve for $\Delta = 1$ gives link performance with the present quantizer. As expected, performance improves in the hard and soft limiters as DEIRPØ, hence E_b/N_0, increases. The benefit of soft decisions is also clear. In the soft limiter, however, performance is quite insensitive to the quantization step size for step-size ratios Δ between 0.5 and 2. The present quantizer is nearly optimal at all signal EIRPs shown in Fig. 6.

Unlike the quantizers of Alternatives 1 and 2, the blanker of Alternative 3 varies as the blanking threshold amplitude THRESH changes. Constant blanking does lower the decoder weight assigned to high RFI amplitudes, but it also lowers quantization accuracy in the absence of RFI. Accuracy is almost always lost when a matched-filter output is blanked and no RFI is received. The curves in Figs. 7-8 depict Alternative 3 performance as a function of THRESH/RMEAN for DEIRPØ = 4 dBW at several different quantization step sizes. RMEAN is the mean amplitude at the matched-filter output when no RFI is received. Again the step-size variation has very little effect and the step size of the present quantizer, shown by the thick curve in Figs. 7-8, is nearly optimal for all values of THRESH.

The optimal threshold amplitude is difficult to detect, because each curve in the figures has more than one relative minimum. Performance is nearly optimal at THRESH/RMEAN = 1.78 for all the curves (Fig. 8). When THRESH is less than QSTEP, Alternative 3 is a hard limiter (Fig. 5) and the performance is constant. Performance improves

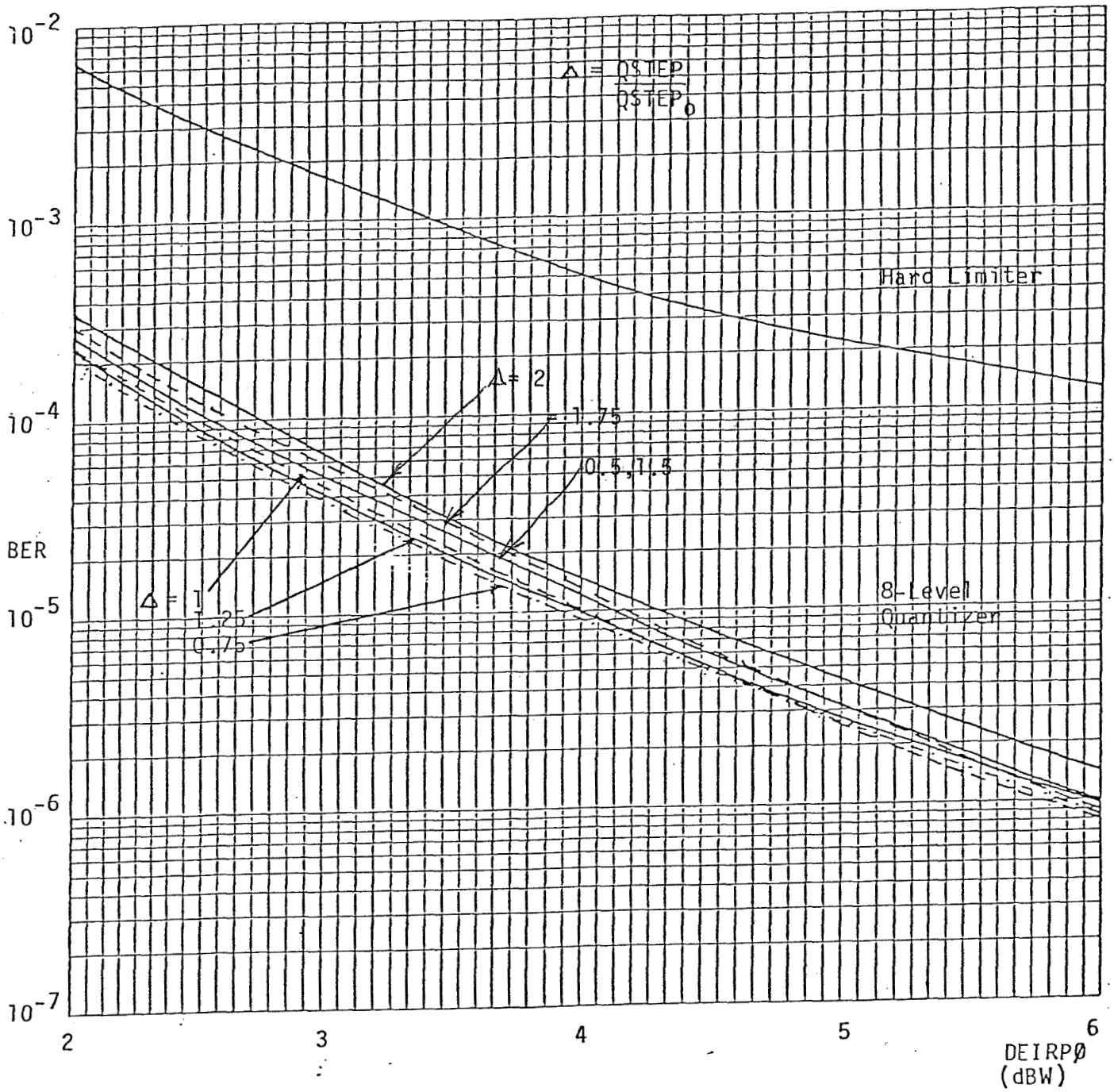

Figure 6: BER as a Function of Additional Signal EIRP for Hard Limiter and 8-Level Quantizer.

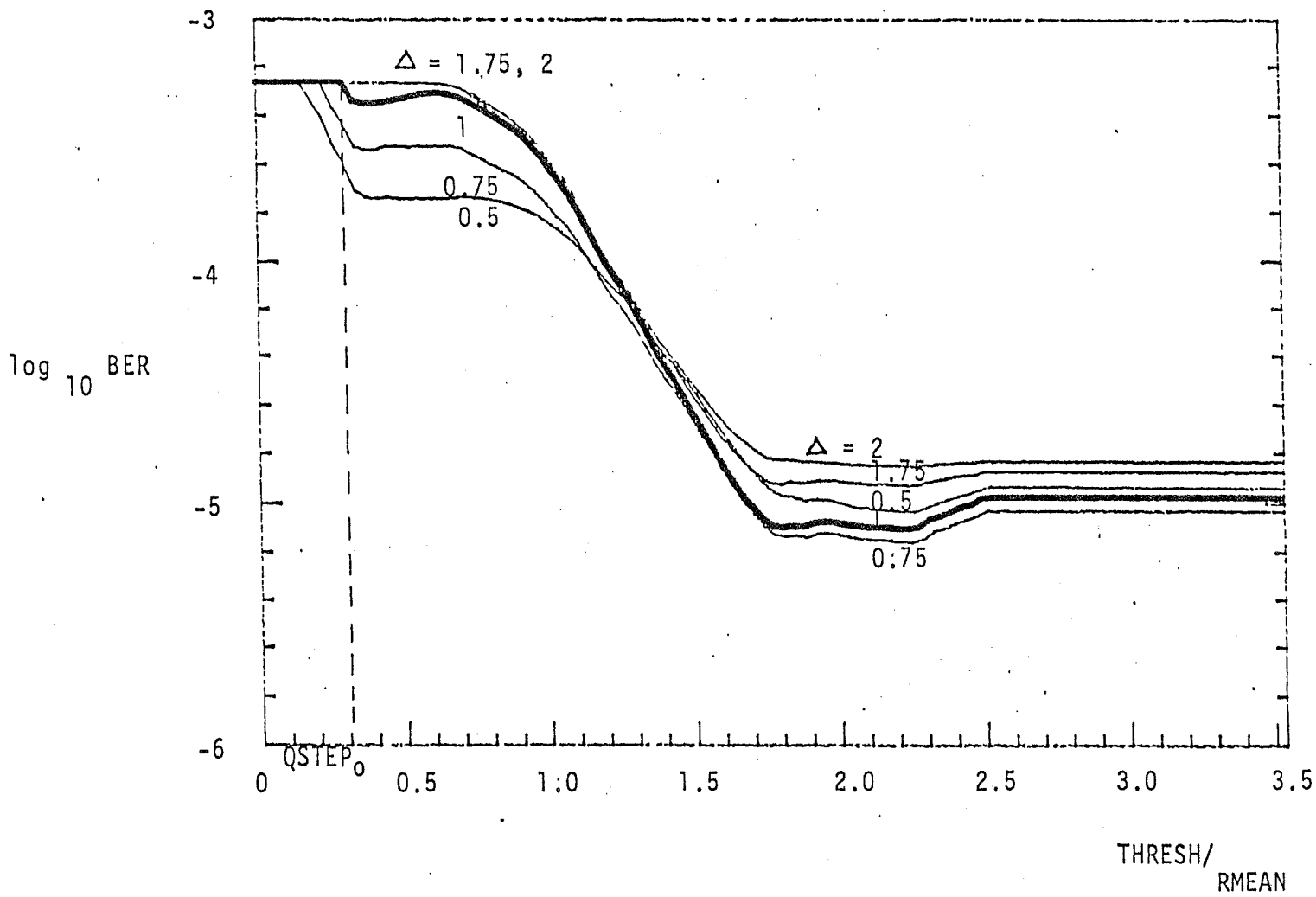

Figure 7: Performance of Constant Blanker as a Function of Blanking Threshold Amplitude THRESH for 28.04 dBW of Signal EIRP (DEIRPØ = 4 dBW).

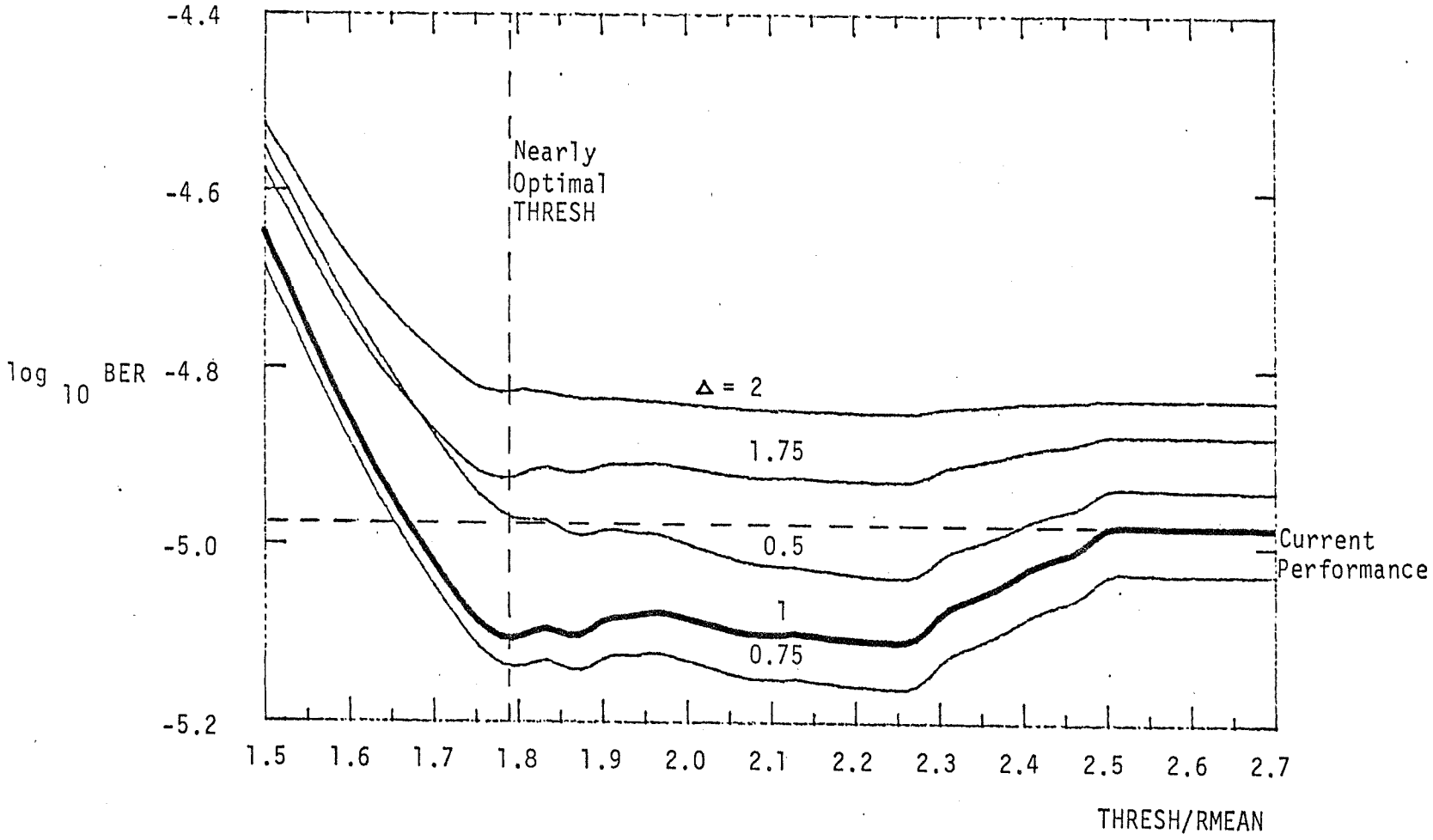

Figure 8: Performance of Constant Blanker as a Function of Blanking Threshold Amplitude THRESH for 28.04 dBW of Signal EIRP.

as the threshold amplitude increases, especially after it surpasses RMEAN (Fig. 7). Quantization errors in the absence of RFI are much less likely when THRESH exceeds RMEAN than they are when THRESH is smaller than this amplitude. The BER becomes constant again (Figs. 7-8) when THRESH is set so high as to eliminate blanking, thereby yielding Alternative 2 quantization.

It is clear from Fig. 8 that the potential improvement from blanking is small. There is very little difference between the minimum BER and the BER without blanking. This fact is also illustrated in Fig. 9, in which performance is plotted as a function of QSTEP/RMEAN for three different blanking threshold amplitudes. The thick curve illustrates this function in the absence of blanking. Since the three curves are so close as to be indistinguishable at some step sizes, the performance improvement due to constant blanking is small, even when THRESH/RMEAN is set at the almost optimal value of 1.78.

All three curves of Fig. 9 show that the BER increases significantly when the quantization step-size ratio Δ is raised above 2 or dropped below 0.5. Whenever the Alternative 3 step size and that of the present quantizer ($QSTEP_0$) differ by more than a factor of 2 ($\Delta < 0.5$ or $\Delta > 2$), performance is worse than when $QSTEP_0$ is used ($\Delta=1$). Therefore step size ratios between 0.5 and 2 (Figs. 6-8) are the best for link performance in Alternatives 2 and 3.

Present link performance cannot be significantly improved by Alternatives 2 or 3, even when blanking and quantization step-size variation are combined. In Fig. 10, the performance of a almost optimal Alternative 3 quantizer is plotted against the approximate BER of the present quantizer. The thick curve is not an exact representation of

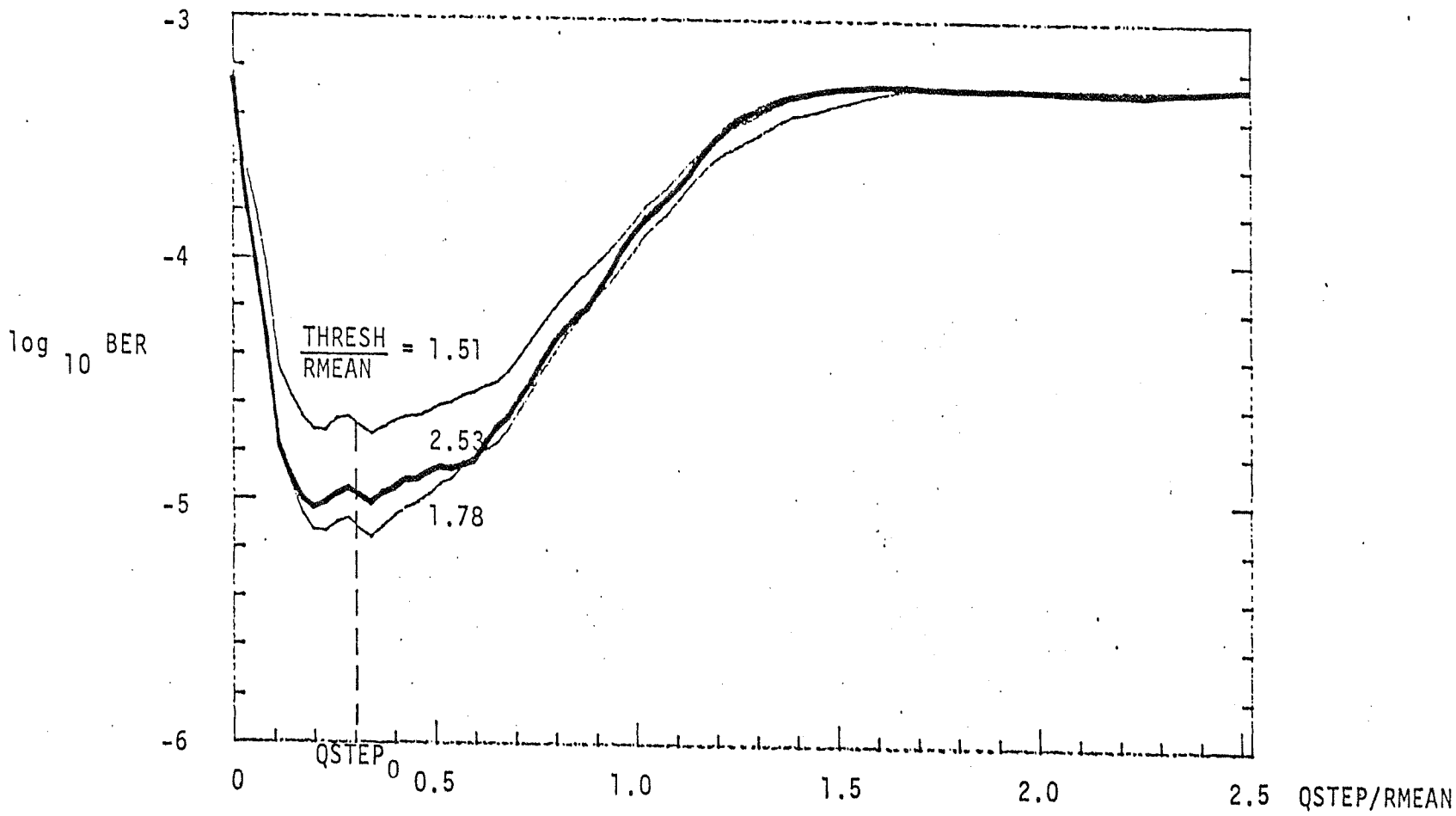

Figure 9: Performance of Constant Blanker as a Function of Step Size for 28.04 dBW of Signal EIRP.

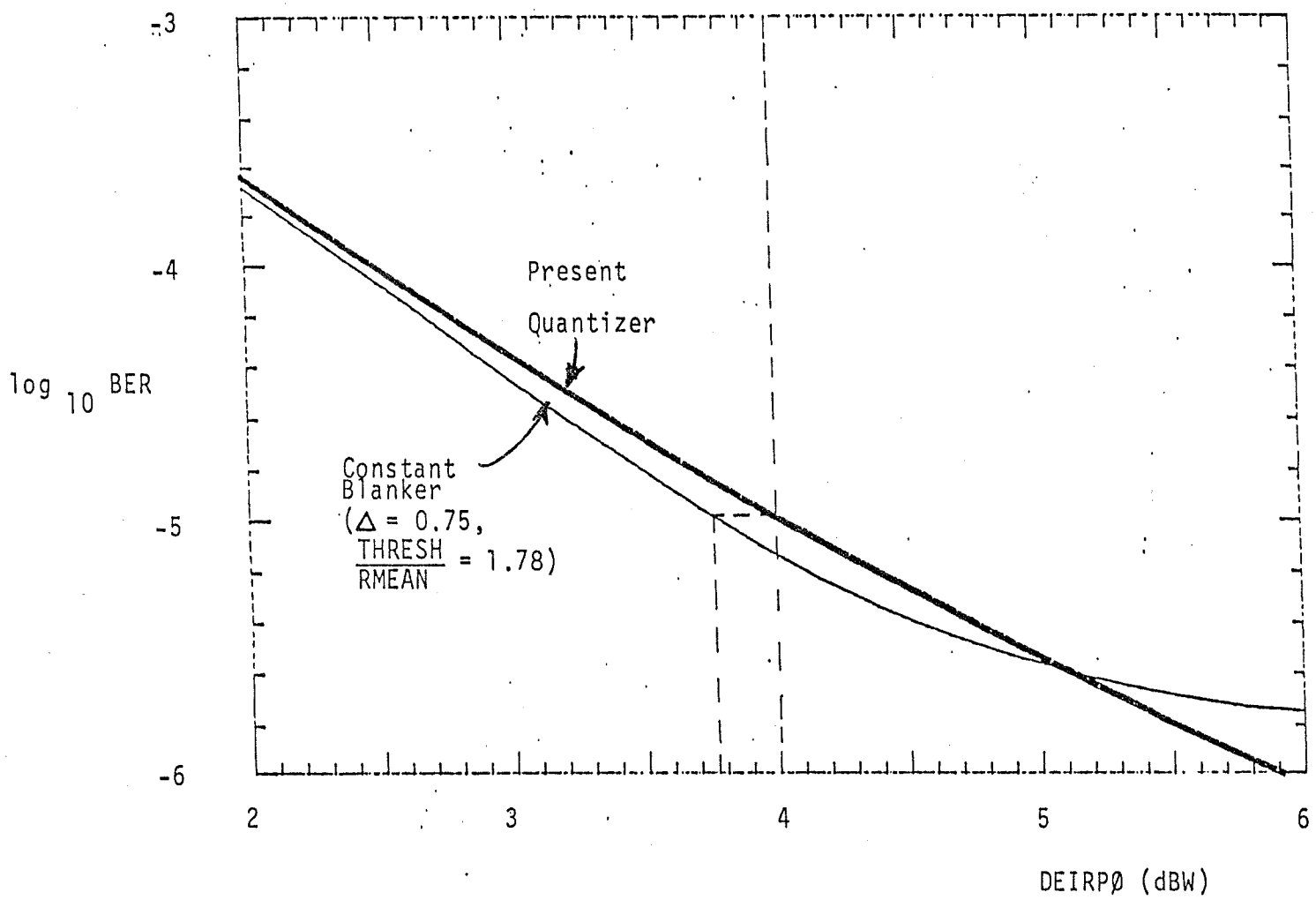

Figure 10: Performance Comparison of Nearly Optimal Constant Blanker with Present Quantizer

the current 8-level quantization performance, because the present quantization step size at 4 dBW of additional EIRP over the baseline EIRP is used throughout the plot. Hence the curve is most accurate in the region around DEIRPØ=4 dBW.

The thin curve, on the other hand, results from a constant blanker with a step-size ratio Δ of 0.75 and a blanking threshold amplitude THRESH that is 1.78 times larger than RMEAN. These two values yield a bit error rate (BER) that is very close to the minimum for DEIRPØ=4 dBW (Figs. 7-9). For a BER of 10^{-5}, the quantization improvement of the almost optimal Alternative 3 quantizer over the present quantizer is approximately 0.2 dBW (Fig. 10). Since Alternative 3 contains Alternatives 1 and 2 as limiting cases (Section 3.3), none of the three alternative quantization methods can mitigate RFI significantly better at a BER of 10^{-5} than the present 8-level quantization scheme does.

5.0 RECOMMENDATIONS

The alternative quantization methods will not offset the degradation due to RFI on the SSA return link of Table 1 with the TDRS East RFI environment given in [12]. As Fig. 10 shows, even a nearly optimal choice of quantization step size and blanking threshold amplitude offers little improvement over the present quantization model. At least 3.7 dBW (Fig. 10) of transmitter EIRP must be added to the baseline EIRP to maintain 10^{-5} BER performance when the TDRS East RFI environment is encountered. This degradation is only slightly smaller than that of the present link model (Fig. 10). Two past efforts [8,9], which produced larger reductions in RFI degradation, restricted in-band CW RFI to coincide with the center frequency of the signal.

Although quantization step-size variation and non-ideal blanking do

not improve its peformance significantly, the present quantization model can be upgraded. Any superior quantizer must assign Viterbi decoder weights in a manner that de-emphasizes RFI pulses more explicitly than the non-ideal blanker of Alternative 3.

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APPENDIX B

ADEQUACY OF UNIFORM 8-LEVEL QUANTIZATION WITHOUT BLANKING IN TDRSS PULSED RFI ENVIORNMENTS

1. Introduction

Significant effort has been focused on improving the coded performance of the Tracking and Data Relay Satellite System (TDRSS) in pulsed radio frequency interference (RFI) environments. Blanking [1] and nonlinear quantization [2,3] are two proposed modifications to the present uniform 8-level quantizer in the TDRSS ground receiver. Both of these changes have recently been presented as methods of mitigating RFI in TDRSS return links.

A study of 8-level uniform quantization with blanking was recently completed by LinCom [13]. The blanker is a uniform 8-level quantizer with an amplitude threshold (Figure 1). Any input voltage to the quantizer that differs from the reference voltage by more than the threshold is assigned to quantization level 4 or level 5, which are given the lowest weight in the Viterbi decoder. Some of the symbols that are corrupted with RFI yield large input amplitudes of the quantizer and contain less information about the transmitted signal than uncorrupted symbols. The blanker shields the decoder from at least some of these corrupted symbols.

The results of this recent study were discouraging, however. They showed that even a nearly optimal quantizer with blanking mitigates less than 0.5 decibels (dB) of the 4.4-dB RFI degradation in the received bit-energy-to-thermal-noise-density ratio (E_b/N_0) at a 10^{-5} bit error rate (BER) for a typical S-band single-access (SSA) return link (Table 1) with the TDRS East RFI environment given in [6]. The link model is shown in Figure 2. 0.5 dB is much smaller than the quantization improvement of a similar ORI study [3], so LinCom initiated a follow-up study of the qualitative reasons for the small improvement.

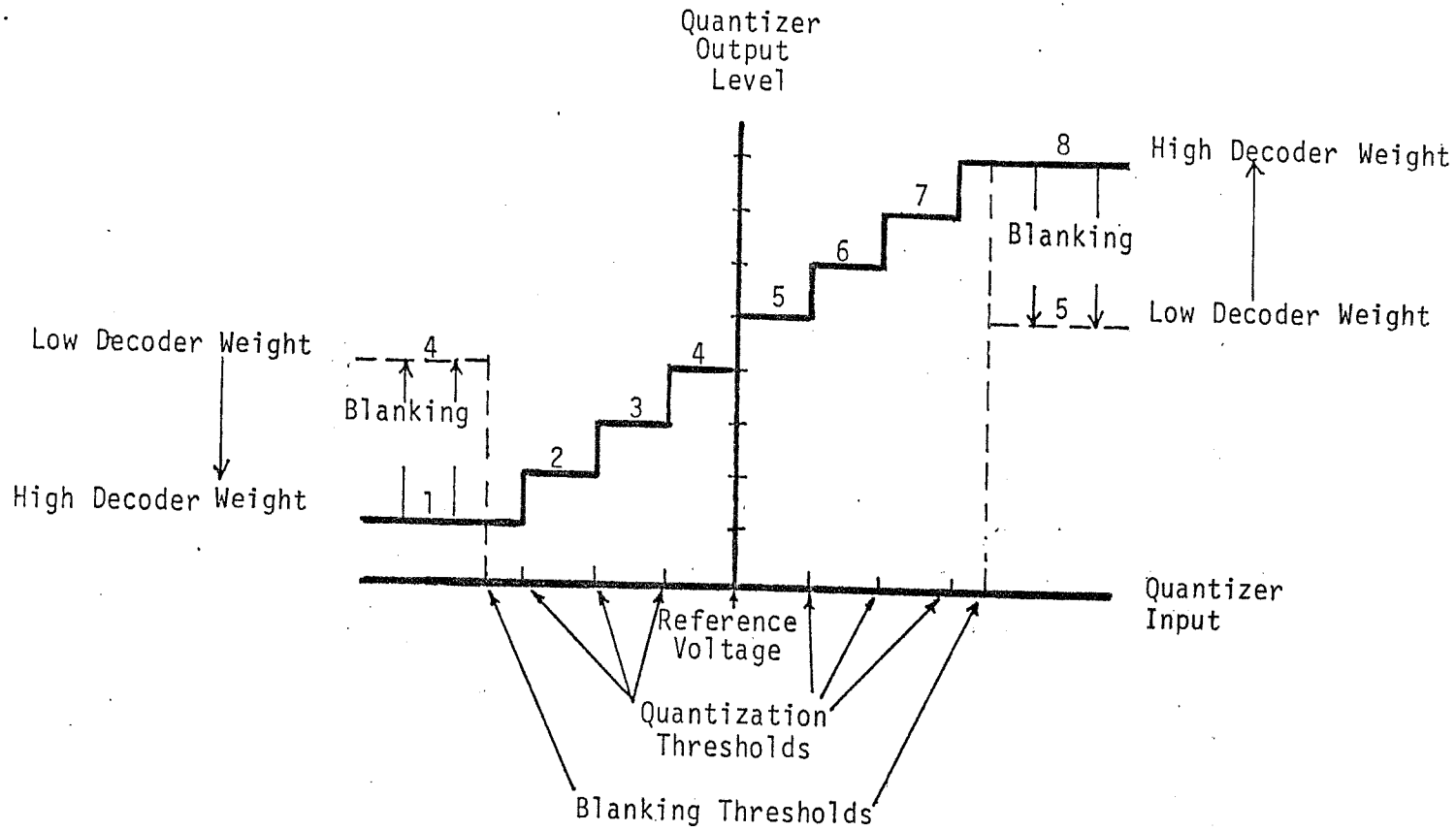

Figure 1. 8-Level Uniform Quantization with Blanking.

Table 1. Characteristics of SSA Return Link Signal Used in This Study.

1. No pseudorandom-noise (PN) coding.

2. Binary phase-shift-keying (BPSK) modulation.

3. 1 megabit per second (Mb/s) data rate.

4. Rate-1/2 convolutional code.

5. No loss of RFI power due to transponder antenna offpointing.

6. Baseline bit-energy-to-thermal-noise-density ratio (E_b/N_0) of -0.680 dB at input to TDRS transponder nonlinearity.

7. Bandwidth of 20 megahertz in intermediate frequency (IF) filter of TDRS transponder.

8. Link nonlinearity consisting of 9-dB clipper and traveling-wave-tube amplifier (TWTA) with 18.5-dB input backoff in TDRS transponder and 3-dB clipper in ground receiver [5].

9. Ground station receiver loss of 5.27 dB is that necessary for a BER of 10^{-5} with baseline E_b/N_0 and no RFI.

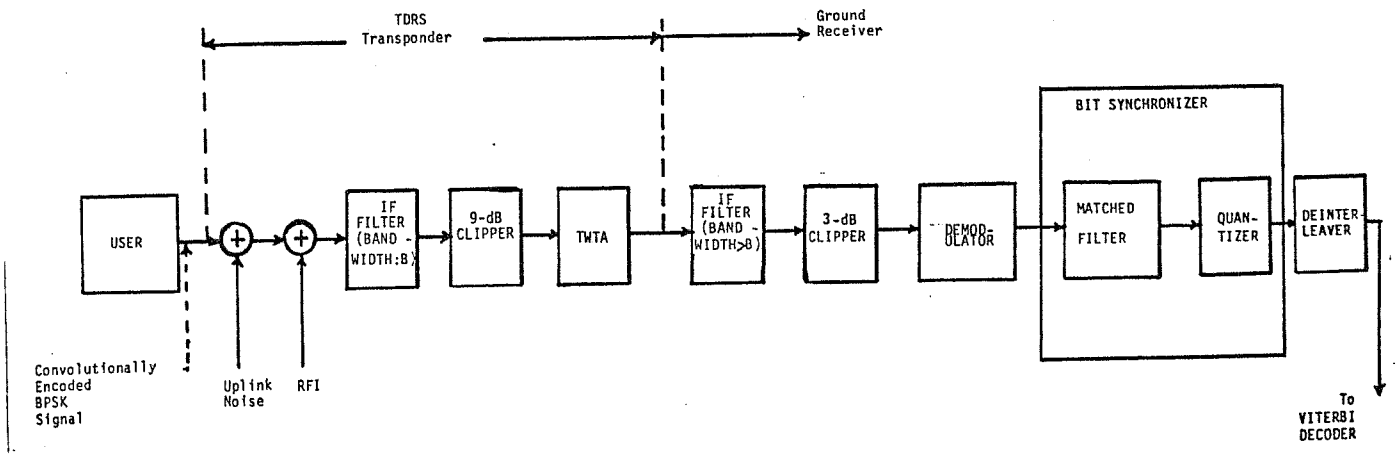

Figure 2. SSA Return Link Model.

This document presents the findings of the follow-up study, which show that no significant improvement of the existing quantizer is possible with the specified RFI environment. This conclusion conflicts with that of [3], primarily because it is based on a different continuous-wave (CW) RFI model. The LinCom model is compared with previous CW RFI models [3,7,8] in Section 2. In Section 3, the reasons for no significant improvement of the present quantizer on the TDRS East SSA return link are detailed. Conclusions and recommendations are given in Section 4.

2. Comparison of CW RFI Models

The bit error rate performance of the SSA return link is very sensitive to the RFI environment on the link. For this study, we assume the RFI consists of three Gaussian noise processes and three CW processes. Each of the six RFI processes has a different duty cycle and power level, but every CW process has a smaller duty cycle and more power than any of the Gaussian noise processes.

The LinCsim software package developed by LinCom was used to compare alternative quantization methods in the recent LinCom study mentioned in Section 1. This software package is described in [9].

TDRSS performance in a TDRS East pulsed RFI environment has also been analyzed by STI [7,8] and ORI [3]. In each of these past studies, however, the CW RFI is modeled differently than it is in LinCsim. The two most important discrepancies lie in:

1. Number of CW frequencies taken in numerical averaging to represent frequency distribution.
2. Time dependence of the phase of CW pulses.

The CW RFI frequencies are confined to the bandwidth B of the

intermediate frequency (IF) filter in the transponder (Figure 2) with a uniform distribution. In LinCsim and the three previous studies, the uniform distribution is approximated by a discrete frequency distribution. A number of RFI frequencies are chosen and the effect of each frequency is numerically averaged.

In LinCsim about eleven frequencies are chosen. The number, values, and probabilities of the frequencies depend on the RFI pulse duration, symbol rate, and symbol format, either biphase or non-return-to-zero (NRZ).

Only two CW frequencies are used in the ORI and STI models. The two frequencies correspond to "in-band" and "out-of-band" CW pulses [7], respectively, and the probabilities attached to them are 2/BT and 1-2/BT, respectively, where T is a symbol duration. Out-of-band CW pulses are separated in frequency from the carrier frequency by more than 1/T, although they still lie within the transponder IF bandwidth B. The actual frequency of an out-of-band pulse is insignificant, as explained later in this section. The frequency of an in-band pulse is assumed to coincide with the carrier frequency [3,7].

This assumption is pessimistic, because the amplitude output by the matched filter (M.F.) is very sensitive to the frequency of an incoming CW RFI pulse. In all the TDRSS RFI environments that LinCom is aware of, almost all the CW RFI is much more powerful than the signal plus thermal noise at the input to the link nonlinearity.

During a CW RFI pulse, the output of the nonlinearity is approximately the sum of much suppressed signal, noise, and RFI phasors. It is nearly just a tone with amplitude fixed by the nonlinearity and independent of the CW RFI power. This limited

amplitude may then be attenuated by the matched filter. The amount of attenuation depends on the frequency offset of the CW pulse from the center frequency of the signal. NRZ (Figure 3) and biphase (Figure 4) matched filters have highly attenuated outputs when this offset is greater than roughly 1/T, corresponding to out-of-band CW RFI.

In the ORI and STI models, the frequency of the in-band CW RFI coincides with the carrier frequency, so there is no attenuation by the NRZ M.F. (Figure 3). Large amplitudes are usually input to the uniform 8-level quantizer during in-band CW pulse receptions. These amplitudes receive high decoding weight because the Viterbi decoder assigns the highest decoding weight to the highest and lowest quantization levels (Figure 1). The quantizer should ideally assign the lowest weight to CW RFI receptions [3] because they contain almost no information about the transmitted signal. Therefore the assumption that the CW frequency coincides with the center frequency of the signal with probability 2/BT is a pessimistic assumption.

The second important discrepancy between the LinCom and STI CW RFI models is that the frequencies of the out-of-band pulses are not significant in the STI model, which assumes that the phases of these pulses are purely random at the input to the matched filter. In both the LinCom and STI models, the M.F. output of a received symbol is approximated by the sum of independent samples of the M.F. input, taken at the Nyquist rate [7,9]. The initial phase of the CW RFI is assumed purely random in LinCsim, but the phases of all succeeding time samples are determined from the frequency of the RFI and its random initial phase [9]. In the STI model, however, the phase of each out-of-band CW pulse is assumed to be purely random at each time sample of the pulse

M.F. INPUT: $\cos(2\pi ft+\alpha)$, $0 \leq t \leq T$, where $\begin{cases} f = \text{frequency offset from NRZ signal frequency} \\ T = \text{symbol duration} \\ \alpha = \text{arbitrary phase} \end{cases}$

M.F. OUTPUT: $\dfrac{\sin(\pi fT)}{\pi fT} \cos(\pi fT+\alpha)$

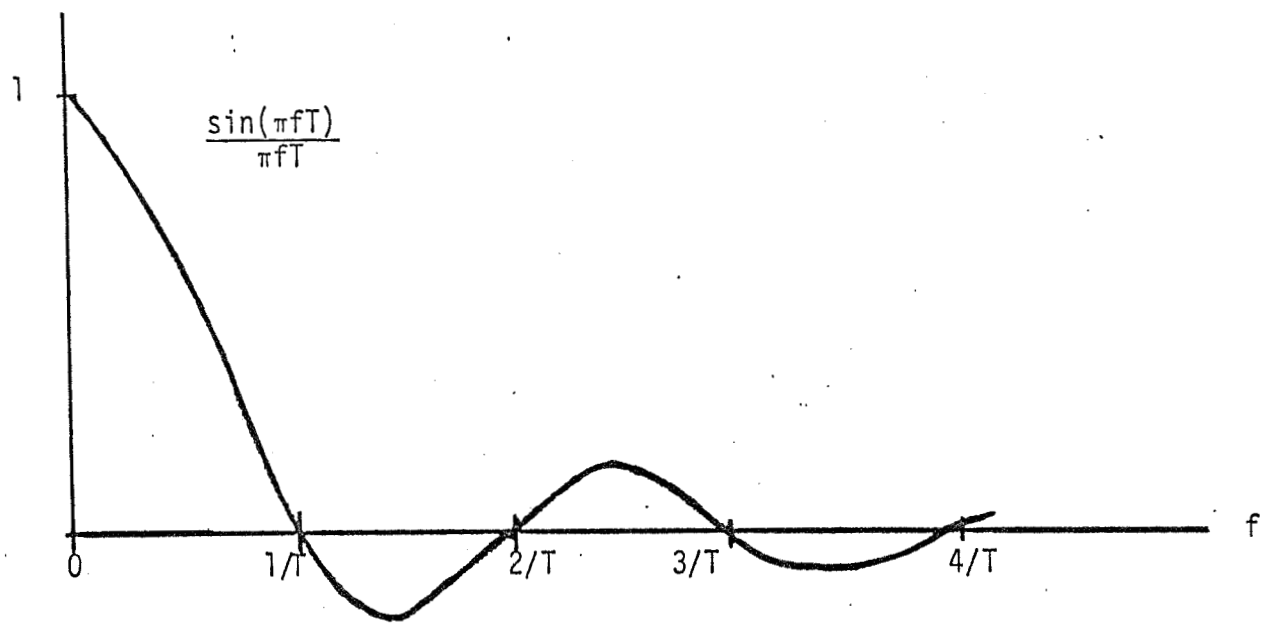

Figure 3. NRZ Matched-Filter Output When Input Is CW for Symbol Duration.

LinCom
LinCom

M.F. INPUT: $\cos(2\pi ft+\alpha)$, $0 \leq t \leq T$, where T = symbol duration

M.F. OUTPUT: $\dfrac{\sin^2(\pi fT/2)}{\pi fT/2} \sin(\pi fT+\theta)$

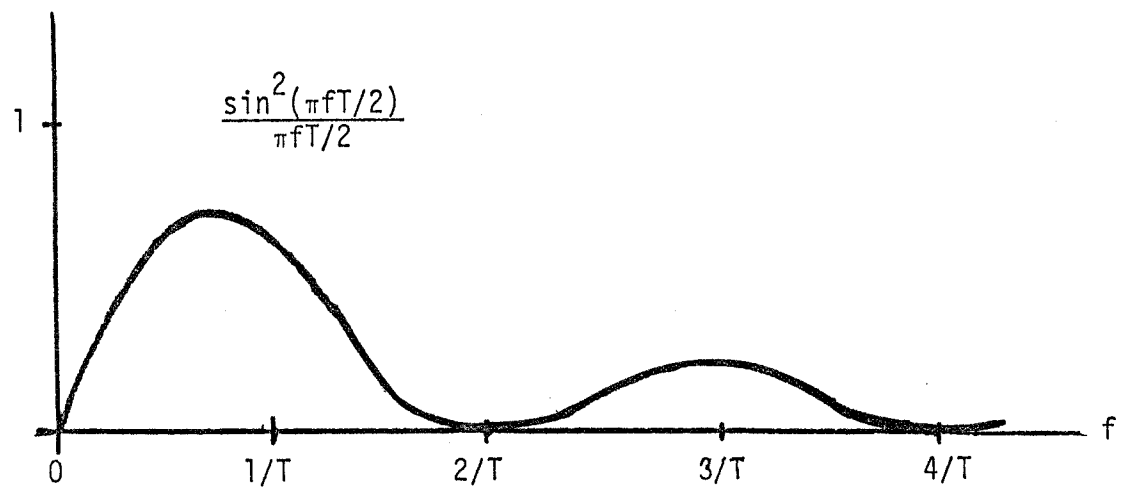

Figure 4. Biphase Matched-Filter Output When Input Is CW for Symbol Duration.

LinCom
LinCom

[7]. This yields a matched-filter output with a larger variance than was derived by the LinCom model, because the STI model neglects the frequency dependence of the filter attenuation of the out-of-band pulses. Therefore the assumption that the phase of an out-of-band CW pulse is independent of time is another pessimistic assumption.

The ORI link model yields a higher BER (dashed curve of Figure 5) [3] than does LinCsim (Figure 6) at the same bit-energy-to-thermal-noise-density ratio E_b/N_0, possibly because ORI used the STI model of CW RFI. ORI did not detail their CW RFI model [3], so no complete explanation of the difference is attempted here.

3. Explanation of Insignificant Improvement

Because the BER performance of the existing quantizer in the TDRS East RFI environment is better in the LinCom model than in the ORI model, the LinCom performance prediction is harder to improve upon. In this section we present the difference between the quantization step sizes that were modeled by ORI and LinCom, respectively. We then explain why no significant improvement of the quantizer modeled by LinCom can be achieved through blanking or non-uniform quantization on the link described in Table 1.

The LinCom and ORI quantization step sizes are different, and this accounts for a small part of the discrepancy between the ORI performance results (Figure 5) and the LinCom performance results (Figure 6). The ORI step size is based on the variance σ^2 of the matched-filter output in the absence of RFI. The LinCom step size is a fraction of the mean amplitude of the filter output in the absence of RFI. In additive white Gaussian noise channels, the two step sizes are equal [9]. LinCom has analyzed both step sizes and has settled on the current approach because

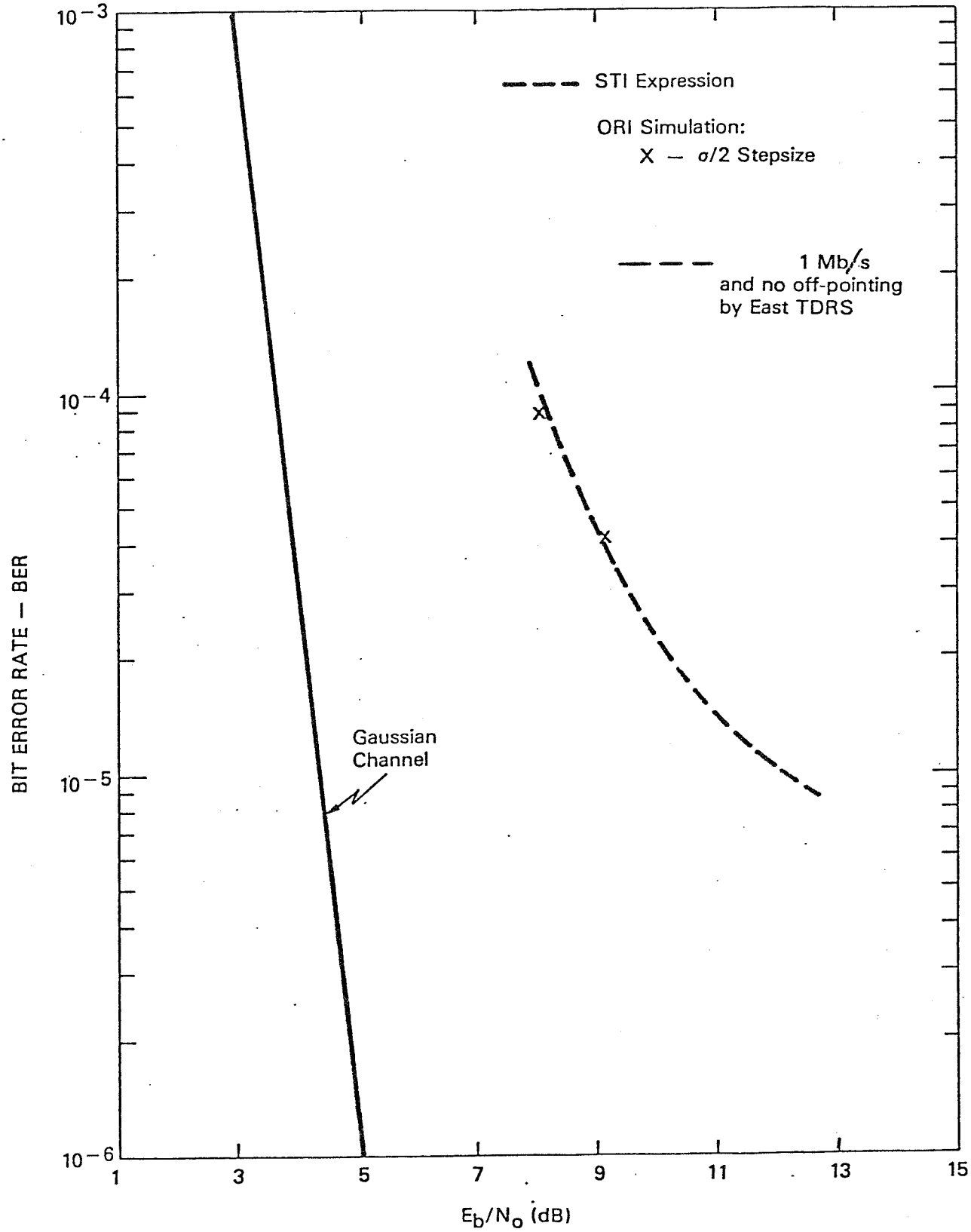

Figure 5. BER Using ORI Model.

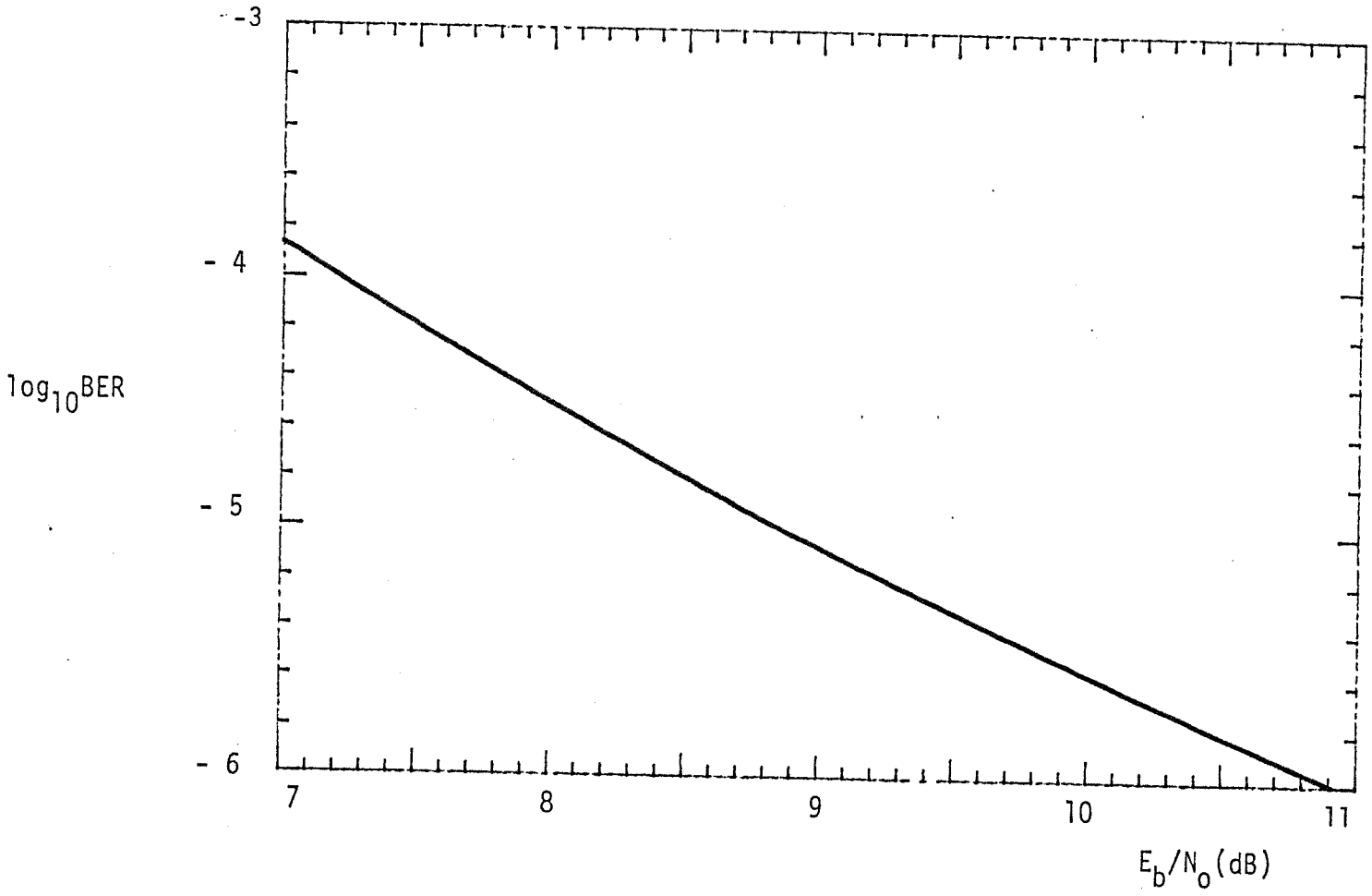

Figure 6. BER for SSA Return Link (Table 1) with Present Quantizer Using LinCsim.

it yields somewhat smaller BERs than the ORI step size does.

The fundamental reasons why no significant improvement of this current quantizer is possible, on the SSA return link described in Table 1 with the TDRS East RFI environment presented in [6], are:

1. The probability density function (PDF) of the matched-filter (M.F) output voltage is nearly Gaussian, even in the presence of RFI, so uniform quantization without blanking is almost optimal [9].
2. The symbol error rate is high relative to the duty cycle of the continuous-wave (CW) RFI processes, so CW RFI alone is not responsible for most of the performance degradation.

In this RFI environment the PDF of the M.F. output voltage is approximated by a weighted sum of seven conditional PDFs. The conditional PDFs include one when no RFI is received and six when RFI is received, along with the signal and uplink thermal noise. Each PDF that is based on received RFI is determined by assuming that only one of the six RFI processes is active. Hence each RFI process has a corresponding PDF. The weights of the PDFs are derived from the duty cycles of the RFI processes. Although the PDFs of the RFI processes differ from the no-RFI PDF, the no-RFI PDF has the largest weight, because the RFI duty cycles are small [6]. We now consider the effects of the noise RFI processes and then the CW RFI processes on the average PDF.

In the TDRS East RFI environment of [6] (and all the other TDRSS environments we have seen), almost all the noise RFI is no more than a few dB more powerful than the signal plus uplink thermal noise. Therefore the mean of the M.F. output voltage in the noise RFI is only slightly lower (due to some clipping of the more powerful noise RFI)

than it is when no RFI is present. Although the variance of the M.F. output increases as the power in a noise RFI process increases, the PDF of the output voltage in the absence of CW RFI (obtained by averaging the PDF in the absence of RFI and the PDF in noise RFI) has a nearly Gaussian shape. Since the LinCom quantization step size is not based on the variance due to thermal noise alone, the uniform quantizer modeled by LinCsim is almost optimal on the SSA return link of Table 1 in the absence of CW RFI.

In spite of the fact that the CW RFI processes are the three most powerful RFI components, we now explain why the shape of the M.F. output average PDF is not significantly affected by these processes. It is true that the time-varying voltage of a CW RFI tone is quite likely to be nearly as large as its maximum voltage (Figure 7) [10], but this maximum voltage is limited by the link nonlinearity (Section 2). The M.F. output voltage is much smaller than even the limited maximum input voltage whenever the CW frequency offset is greater than roughly 1/T (Section 2). Since the symbol rate is 1/T, the PDF of the M.F. output voltage in the presence of CW RFI (averaged over CW frequency and initial phase) becomes more concentrated around zero as the data rate (equal to half the symbol rate) decreases (Figures 8 and 9), provided it is larger than the inverse of the RFI pulse duration [9]. When the data rate is no larger than 1 Mb/s, as in Figs. 5 and 6, the M.F. output voltage, averaged over CW frequency and initial phase, is likely to be small during a CW RFI pulse (Figs. 8 and 9). After accounting for the small duty cycles of the CW processes [6], the LinCsim software yields average PDFs of the biphase and NRZ matched-filter output voltages, respectively, that are nearly Gaussian even in the presence of CW RFI.

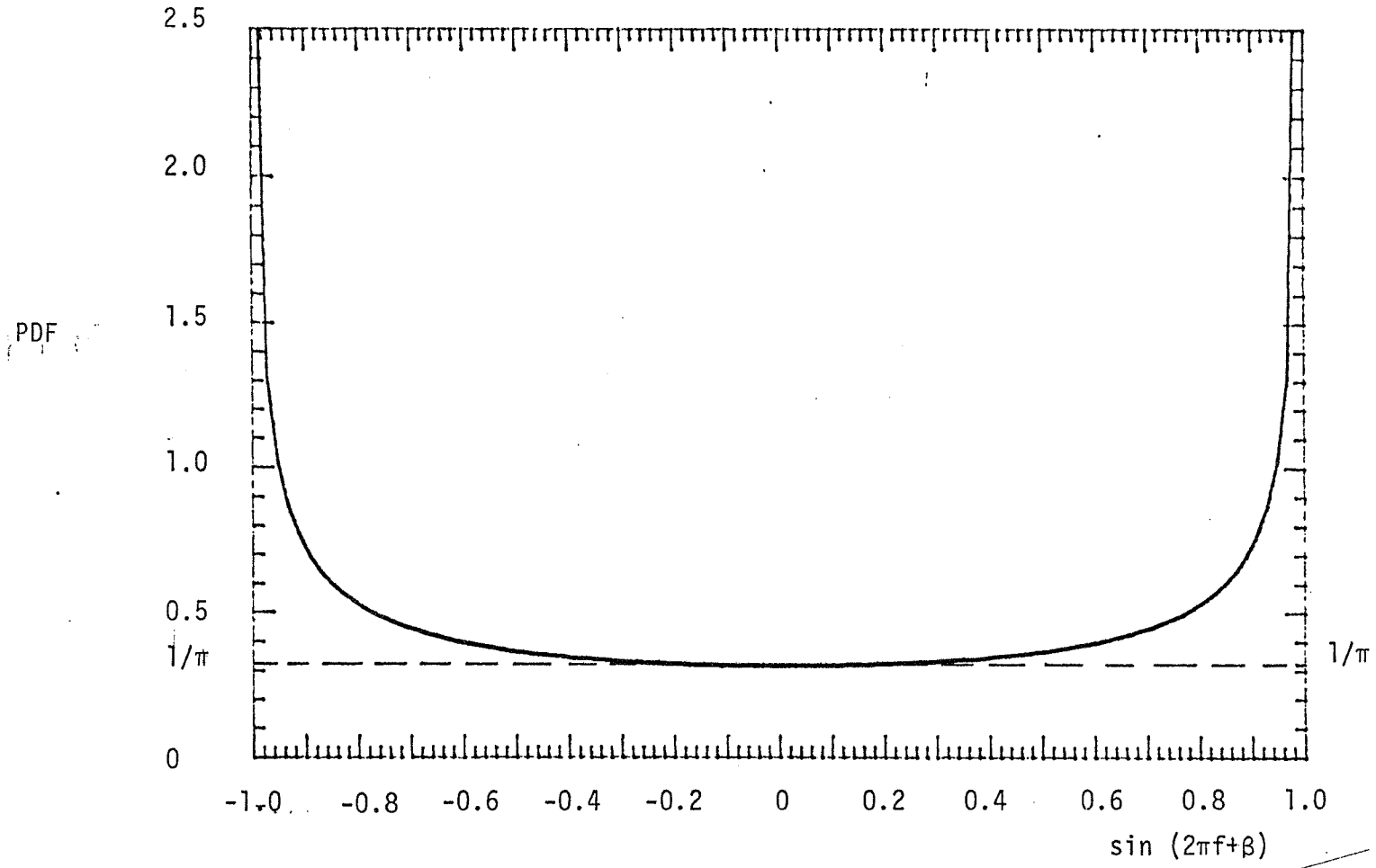

Figure 7. Probability Density Function of Unit Amplitude Sinusoidal Wave at M.F. Input with Completely Random Phase β and Arbitary Frequency f.

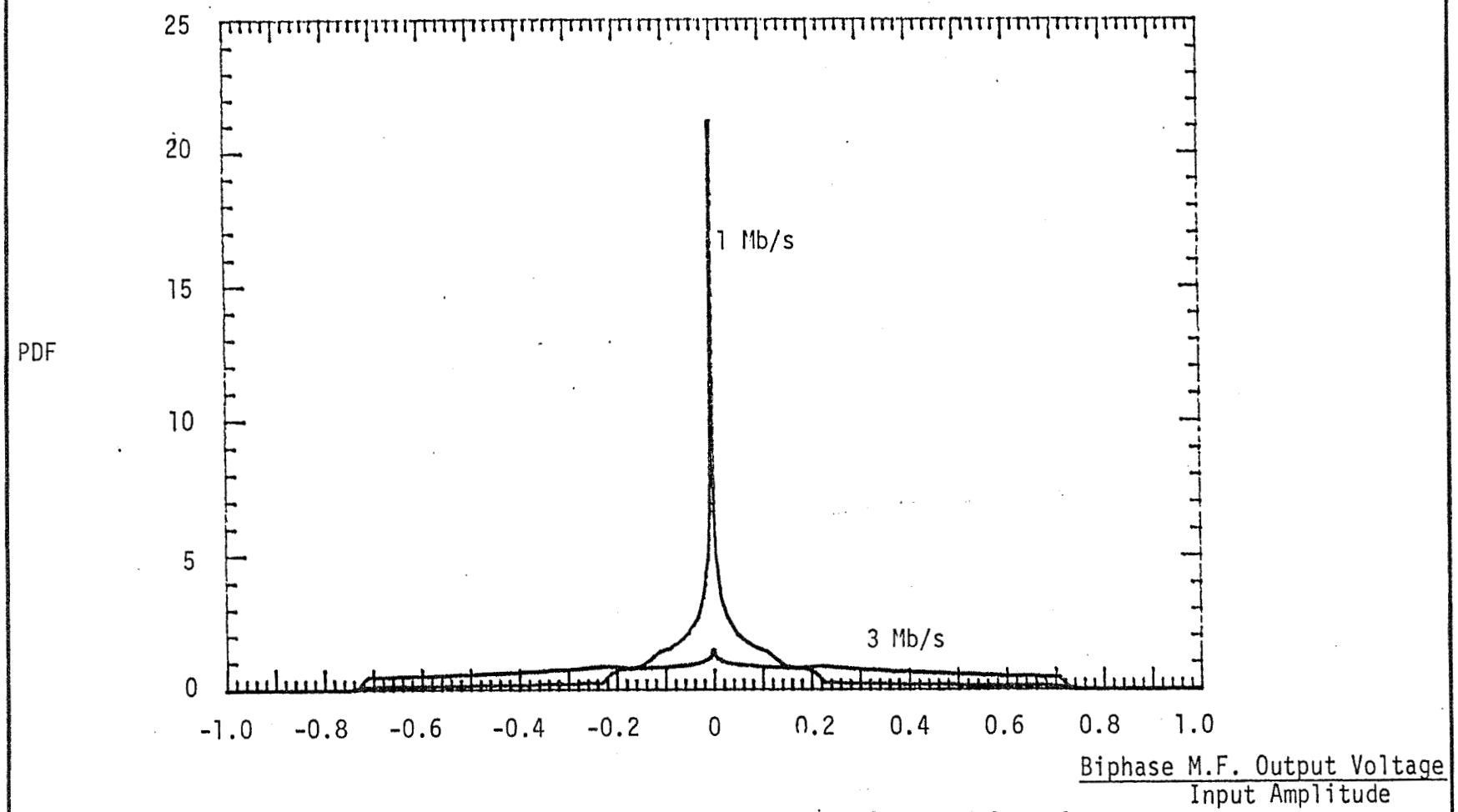

Figure 8. PDF of Biphase M.F. Output Voltage Averaged Over Frequency and Initial Phase, When Input Is CW for Symbol Duration and Channel Bandwidth Is 20 Megahertz.

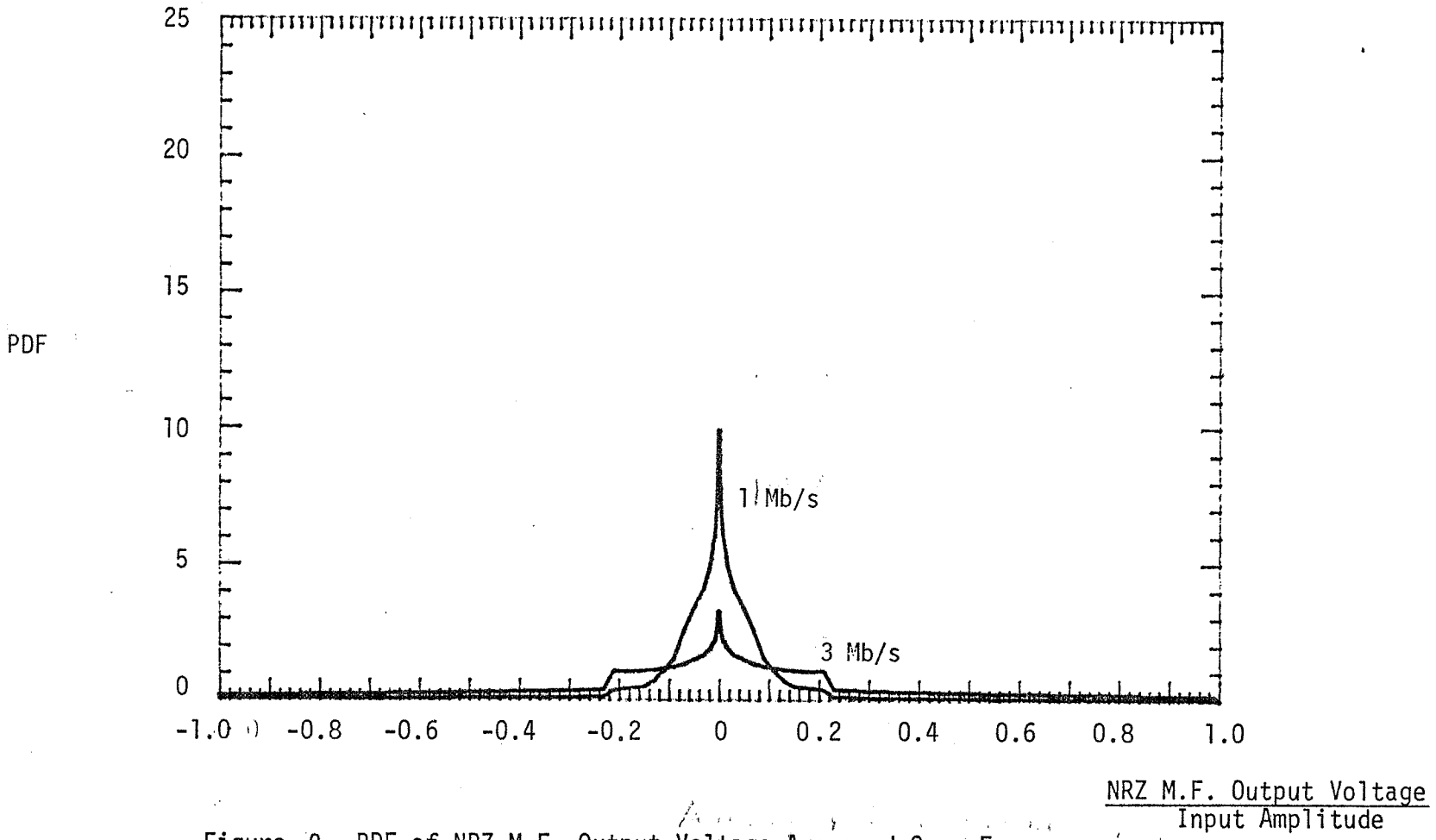

Figure 9. PDF of NRZ M.F. Output Voltage Averaged Over Frequency and Initial Phase, When Input CW is CW for Symbol Duration and Channel Bandwidth is 20 Megahertz.

It is useful to derive the second fundamental reason for insignificant quantization improvement by focusing on completely Gaussian PDFs at the matched-filter output. The probability P_u that a symbol is demodulated incorrectly in a Gaussian channel is equal to the BER when there is no coding (solid curve of Fig. 10 [11]), namely [12]

$$P_u = \frac{1}{\sqrt{2\pi}} \int_{\sqrt{2E_b/N_0}}^{\infty} e^{-x^2/2}\, dx \qquad (1)$$

When rate-1/2 convolutional coding and Viterbi decoding are included, however, the probability P_c of a symbol error becomes much larger than the BER (broken curve of Fig. 10). The coded symbol error probability P_c is [12]

$$P_c = \frac{1}{\sqrt{2\pi}} \int_{\sqrt{2E_s/N_0}}^{\infty} e^{-x^2/2}\, dx \qquad (2)$$

where E_s/N_0 is the symbol-energy-to-thermal-noise-density ratio. Since

$$E_s/N_0 = \frac{1}{2} E_b/N_0 \qquad (3)$$

for a rate-1/2 code, the plot of P_c versus E_b/N_0 is the solid curve of Figure 10 shifted to the right by 3 dB. Thus the superiority of coded BER performance over uncoded performance at low error rates (Fig. 10) leads to a situation where the coded BER is much smaller than the coded symbol error probability, or rate, P_c.

On the particular SSA return link described in Table 1 <u>without</u> RFI, the LinCsim software approximates the broken curve of Fig. 10; a BER of 10^{-5} occurs when E_b/N_0 equals 4.45 dB. From (2), the symbol error rate

Coded Performance

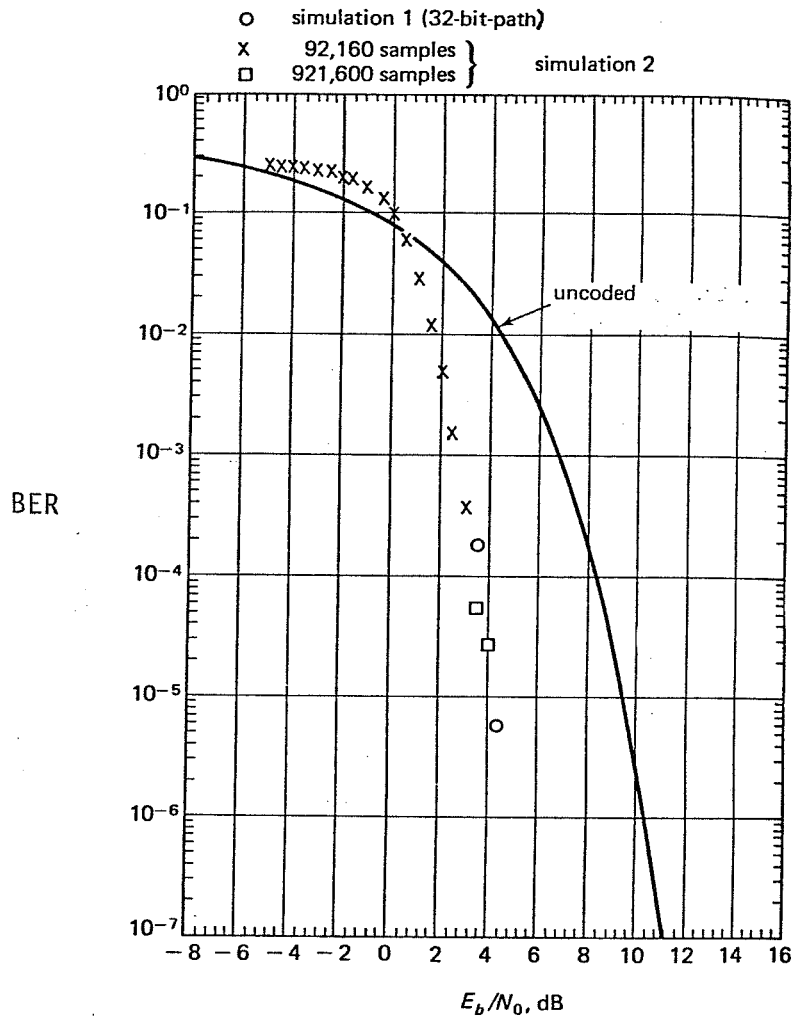

Figure 10. Gaussian-Channel BER Performance for Rate-1/2, Contraint-Length-7, Viterbi-Decoded BPSK Signal and Uncoded BPSK Signal.

P_c is .048 in this case. Therefore P_c is actually larger than the duty cycles of all three CW RFI processes [6]!

To illustrate why the existing quantizer cannot be significantly improved on the SSA return link with RFI (Table 1), we analyze the worst performance degradation due to the CW RFI processes. The worst possible symbol error probability during an RFI pulse is 0.5. Accounting for their duty cycles, an upper bound on the symbol error rate P_{cw} due to these three processes [6] is

$$P_{cw} \leq 0.5(2.0+1.8+0.2)\% = 2.0\% = .020 \qquad (4)$$

If we assume the nearly Gaussian average PDF of the matched-filter output voltage to be completely Gaussian, the average symbol error rate P_s for thermal noise, noise RFI, and CW RFI can be determined. The symbol error rate is a function only of the BER performance in a Gaussian channel, so P_s must equal the no-RFI symbol error rate .048. Therefore most of the symbol errors are caused by thermal noise and the Gaussian noise RFI processes [6] for which the existing quantizer is nearly optimal.

4. Recommendations

Although we have only shown the existing quantizer to be nearly optimal for one set of SSA return link conditions (Table 1), its performance will not be worse for most other scenarios. As the data rate decreases below 1 Mb/s, the average PDF of the matched-filter output voltage at a BER of 10^{-5} becomes more nearly Gaussian. We expect the existing quantizer to be nearly optimal for all data rates on the SSA return links.

In particular, non-uniform quantization and blanking can offer little improvement at best. ORI [3] predicted that almost 3 dB of quantization improvement is possible at a 10^{-5} BER with a pessimistic continuous-wave (CW) RFI frequency distribution (Section 2). This distribution does not reflect those of the real RFI environments. We do not anticipate more than 1 dB of improvement through nonlinear quantization. Blanking has also been analyzed on the SSA return link at a BER of 10^{-5} and it was found to yield less than 0.5 dB improvement by the LinCom model.

No significant amount of RFI can be mitigated after it enters the quantizer, so no RFI mitigation approach should be based solely on modification of the matched-filter output probability density function (PDF). It is possible, however, to mitigate the interference before it enters the quantizer. The clippers in the TDRS transponder and ground receiver already limit the received RFI power. STI has recently investigated the automatic gain control (AGC) circuits in the ground receiver for the purpose of mitigating more RFI [8]. The performance improvement yielded by their proposed modifications is based on pessimistic CW RFI frequency and phase distributions (Section 2), but further study may be worthwhile.

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APPENDIX C

INCREASED CHANNEL THROUGHPUT BY ADPATIVE EQUALIZATION

SUMMARY

This report investigates the performance improvement in terms of higher channel data throughput made possible by including an adaptive equalizer in the AIRS design. The present data rate limit is 6 Mbps (per S-805) per quadrature channel for NRZ data and 3 Mbps for biphase data. Since the measured 3 dB channel bandwidth of the spacecraft filter that sets the bandwidth of the SSA channel is approximately 16 MHz, one would expect it to be capable of supporting a higher data rate by employing equalization techniques.

To find out what is achievable, the SSA channel is modeled as shown in Figure 4 of the report reproduced on the next page. The performance of the tapped delay line equalizer is then simulated. The results are shown in Figure 15 and 19, also reproduced here.

For a designed bit error rate of 10^{-5}, the performance degradation due to the channel bandwidth limitation is shown for NRZ data in Figure 15. The S-805 highest data rate of 6 Mbps gives a $(BT)^{-1}$ of 0.38 for a 16 MHz RF channel. Without equalization, the signal loss due to filtering is approximately 1 dB. However, with a 3-tap tapped delay line (TDL) equalizer, one can more than double the data rate, specifically, achieving 13.6 Mbps with the same 1 dB loss. For biphase data, 3 Mbps ($(BT)^{-1}$=0.19) operation yields a loss of approximately 0.6 dB. With the same loss, a 3-tap TDL improves the data rate to approximately 5.2 Mbps.

It therefore appears that an adaptive equalizer improves the SSA channel throughput by a factor of approximately 2. However, other factors of the link such as signal distortions and channel nonlinearities must be incorporated into the link simulation to obtain a more refined performance assessment.

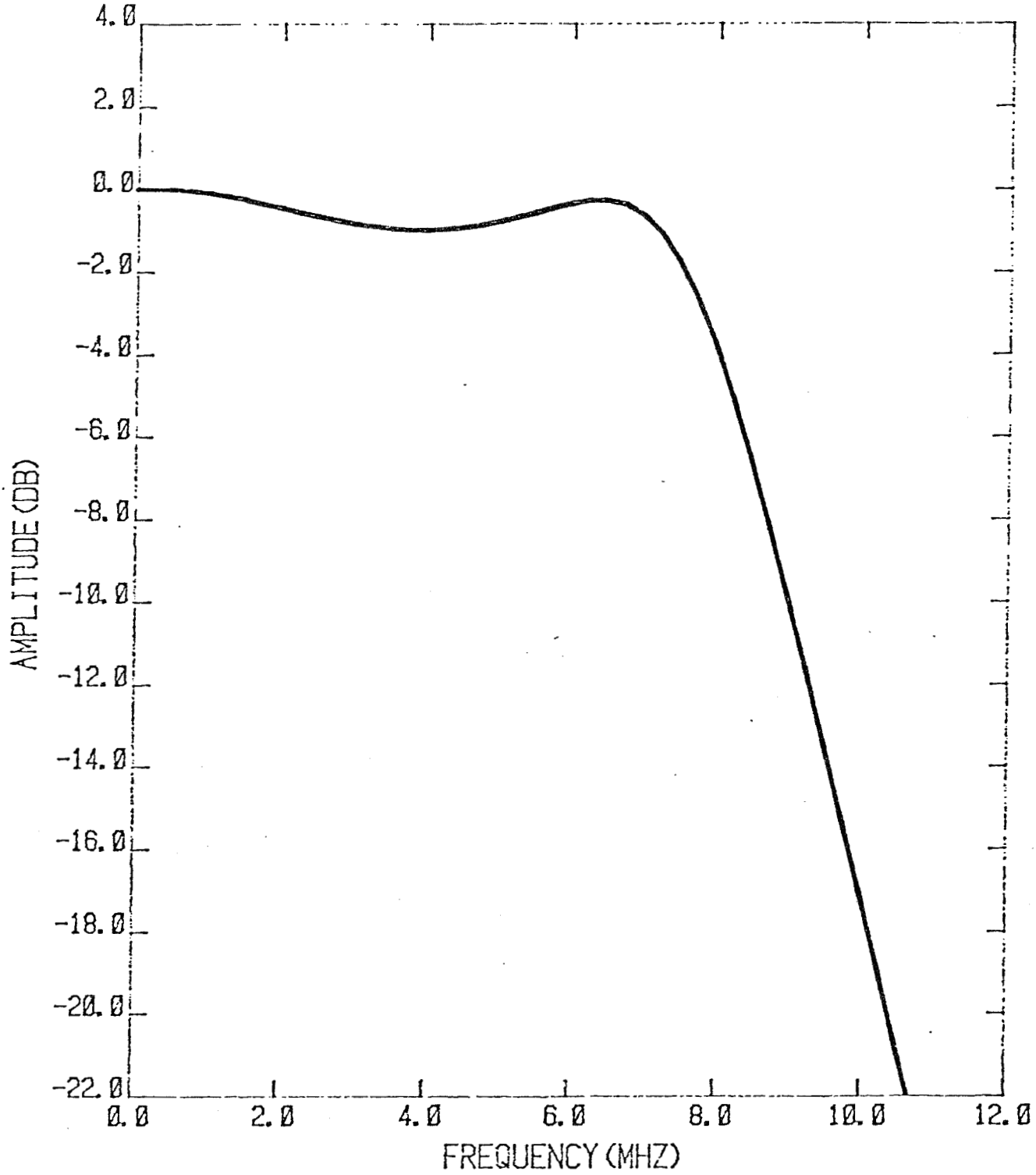

Figure 4. Simulated Channel: Cascade of a 5-Pole Butterworth and a 3-Pole Chebyshev with One dB Ripple, Both 16.5 MHz.

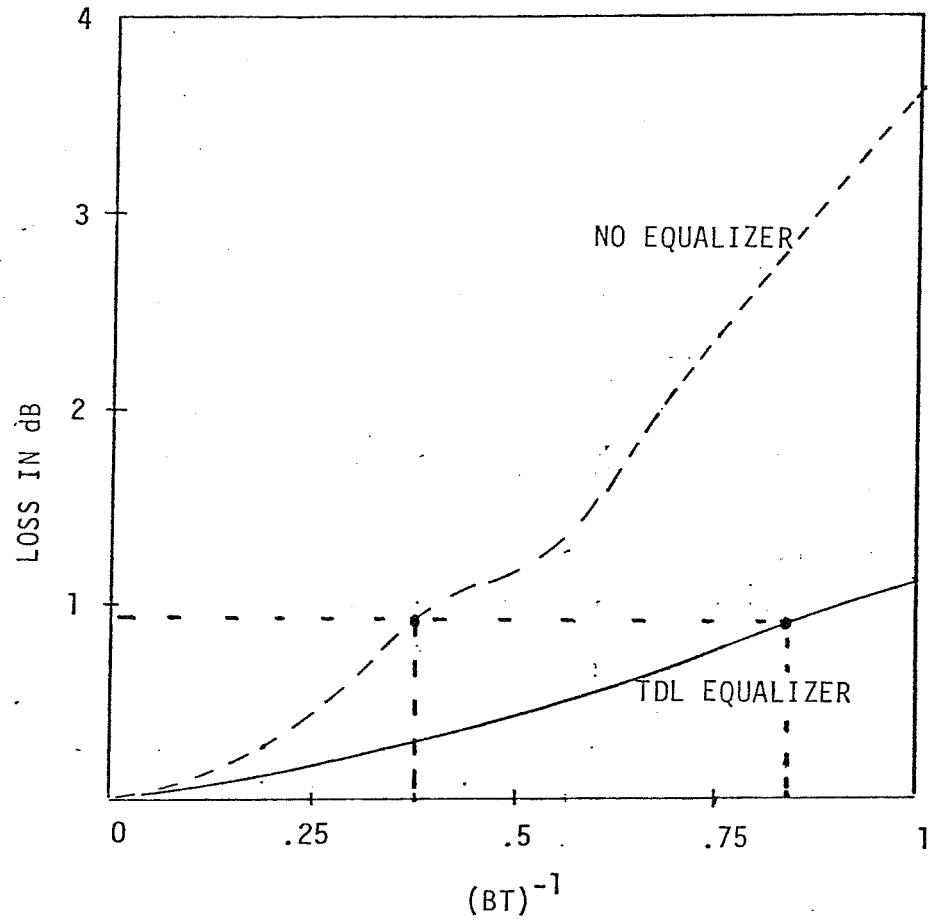

Figure 15. Performance Loss Due to Band Limited Channel.

- BPSK
- NRZ
- K=1 (3 TAPS)
- $P_E=10^{-5}$
- B=RF BANDWIDTH

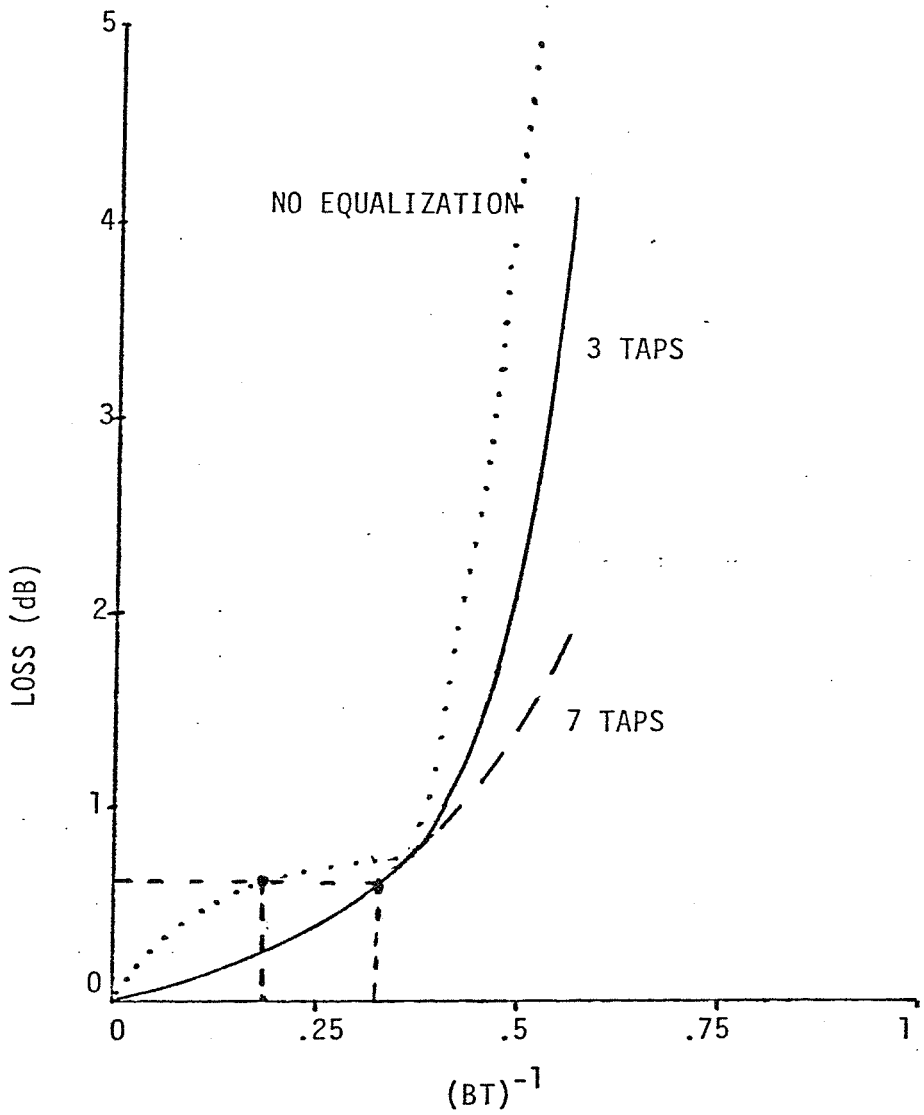

Figure 19. Performance Loss Due to Band Limited Channel

- BPSK
- BIPHASE
- $P_E=10^{-5}$
- B=RF BANDWIDTH

1. INTRODUCTION

A digital communication link maximum data rate is determined by the available channel bandwidth. The intersymbol interference (ISI) caused by a bandlimited channel restricts the link throughput. A band limited channel can be modeled by a lowpass linear filter; therefore, such distortion is mathematically equivalent to a convolution operation. Theoretically, the channel distortion may totally be removed by a deconvolution operation if the channel characteristic is known and the thermal noise is absent. In practice neither of these two assumptions hold and therefore only a portion of information degraded by the scarcity of spectrum can be recovered by deconvolution. In the communications discipline, deconvolution of a nonideal channel is performed by a class of techniques known as equalization. In the communication terminology, equalizers are devices that are utilized by bandlimited receivers in order to mitigate the adverse effect of ISI. Since the channel characteristic may change over time, most equalizers are required to adapt themselves to the varying transmission environment.

One simple and popular form of equalizers for band-limited channels is the tapped delay line (TDL) filter. In this kind of equalization, the demodulated signal is first matched filtered and then samples of the matched-filter output taken with rate 1/T are stored for (2K+1)T seconds, where T and (2K+1) denote the transmission symbol period and the number of taps, respectively. The weighted sum of the stored samples are used for symbol estimation. Mathematically speaking, TDL filtering is equivalent to inverting a matrix of size (2K+1)x(2K+1) corresponding to the channel impulse response. Since the channel

characteristic is not usually known, the TDL filter is desired to operate in a recursive fashion trying to minimize some error criterion. The recursive nature of the equalizer gives rise to the problem of convergence time of the equalizer gains or the equalizer speed. Naturally, equalizers with fast convergence property are desired.

In this report, we are interested in a TDL equalizer for increasing information throughput of a specific channel. Although the channel characteristic is known to us, it is assumed that the equalizer will have no prior knowledge of the channel. In the following a general description of TDL equalizers along with some simulation results are presented.

The link model is shown in Figure 1 where x(t) is the baseband equivalent of the RF signal. Three modulation techniques BPSK, QPSK, and SQPSK are considered. Pulse shape is either NRZ or biphase. The baseband version of the BPSK signal is represented by a real function, whereas, the baseband version of the QPSK (or SQPSK) signal is represented by a complex function. The next section describes an adaptive TDL equalizer similar to the one found in Reference [1].

2. ADAPTIVE EQUALIZER

Let s(t) denote the NRZ or biphase pulse and $\{I_n\}$ denote the statistically independent data sequence with

$$EI_n I_m^* = \begin{cases} \sigma_0^2 & n=m \\ 0 & n \neq m \end{cases}$$

The transmitted signal can be written as[1]

[1] This model represents BPSK (I_n real) or QPSK (I_n complex).

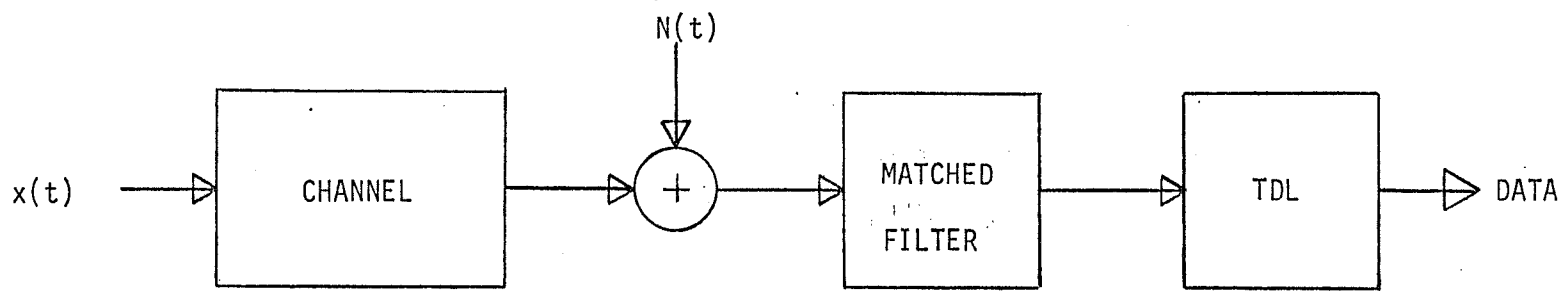

Figure 1. Link Model.

$$x(t) = \sum_{n=-\infty}^{\infty} I_n s(t-nT) \qquad (1)$$

The channel output is expressed by

$$y(t) = N(t) + \sum_{n=-\infty}^{\infty} I_n R(t-nT) \qquad (2)$$

where N(t) is the white Gaussian noise with one-sided spectral density N_0 and R(t) denotes the channel response to s(t).

The matched-filter of Figure 1 is matched to the transmitted pulse with impulse response $s^*(t-\tau)$. The output of the matched filter is

$$m(t) = \sum_{n=-\infty}^{\infty} I_n z(t-nT) + n(t) \qquad (3)$$

where z(t) and n(t) are responses of the matched-filter to R(t) and N(t), respectively.

The output m(t) of the matched-filter is sampled every T seconds. The optimum sampling time is provided by a bit synchronizer. The bit synchronizer operation is beyond the scope of this report and will not be discussed here. Each observed sample is fed into a TDL filter with 2k+1 taps. Clearly the delay line spans (2k+1)T seconds, where T is the NRZ or biphase pulse duration. The delay line stores the most recent 2k+1 samples denoted by m(kT), k = -K,...,0,...,K. A tap delay line with seven taps is shown in Figure 2. The sample stored at each tap is multiplied by a gain corresponding to that tap, and the sum of products

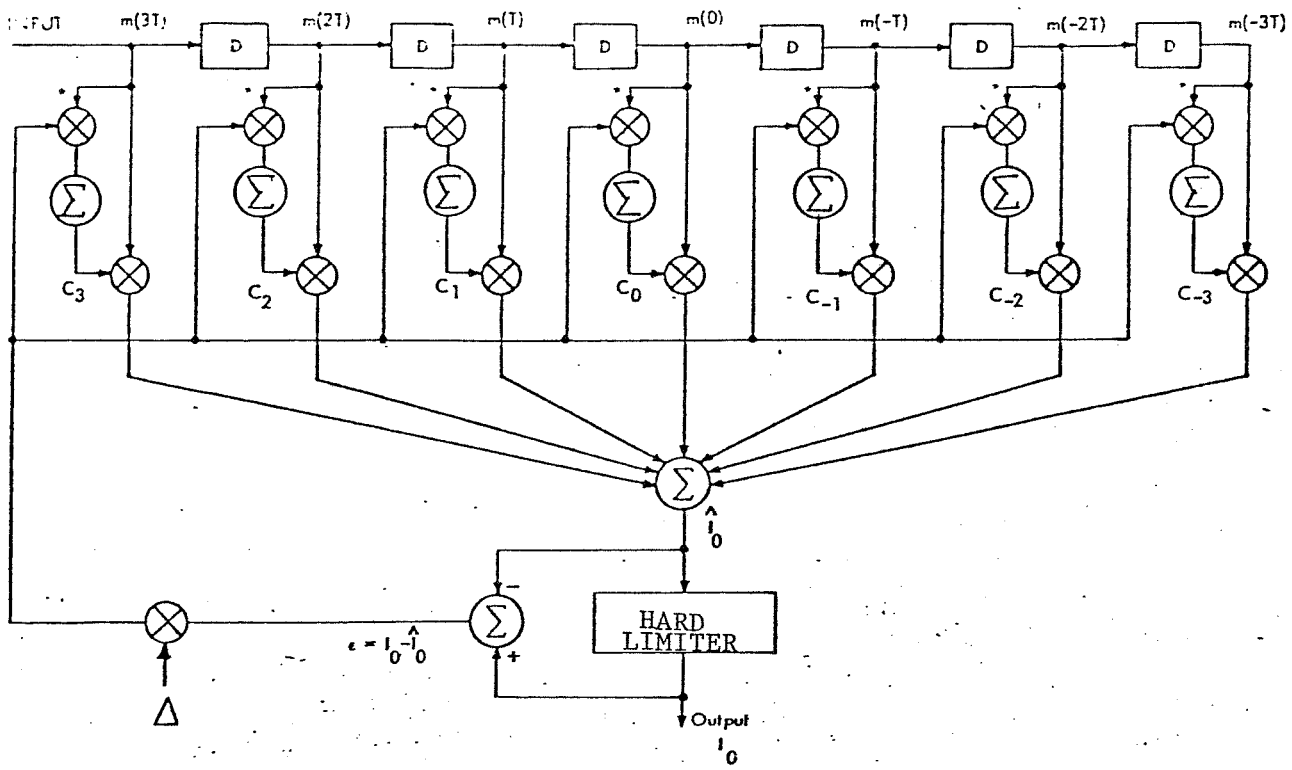

Figure 2. The Adaptive Tapped-Delay-Line Filter.

from all taps is formed to give an estimate of the desired symbol. Let's suppose the desired symbol is I_0 and denote the tap gains as c_k. The estimate of the desired symbol is

$$\hat{I}_0 = \sum_{k=-K}^{K} c_k m(kT) \tag{4}$$

The tap gains $\{c_k\}$ can be evaluated via optimizing some error criterion. The error criterion used here is the mean-square-error (MSE).

Let us focus our attention on I_0. The MSE between I_0 and the estimate $\hat{I}_0$ is

$$\begin{aligned}
\varepsilon &= E|e|^2 = E|I_0-\hat{I}_0|^2 \\
&= E|I_0 - \sum_{k=-K}^{K} c_k m(kt)|^2 \\
&= \sigma_0^2 - 2\mathrm{Re} \sum_{k=-K}^{K} c_k^* \alpha_k + \sum_{k=-K}^{K} \sum_{j=-K}^{K} c_k c_j^* (\psi_{kj}+\phi_{kj})
\end{aligned} \tag{5}$$

where by definition,

$$\begin{aligned}
\psi_{kj} &= \sigma_0^2 \sum_{n=-\infty}^{\infty} z(kT-nT)z^*(jT-nT) \\
\phi_{kj} &= (N_0/T)\Delta(k-j) \\
\alpha_k &= \sigma_0^2 z^*(kT)
\end{aligned} \tag{6}$$

and

$$\Delta(k-j) = \begin{cases} 1 & k=j \\ 0 & \text{otherwise} \end{cases}$$

The tap gains that minimize the MSE are obtained by setting to zero the

gradient components $\partial\varepsilon/\partial c_k$ for $k = -K,\ldots,0,\ldots,K$. The result is a set of (2k+1) simultaneous linear equations:

$$\sum_{k=-K}^{K} c_k(\psi_{ki}+\phi_{ki}) = \alpha_i, \quad i = -K,\ldots,0,\ldots,K \qquad (7)$$

In vector space notation the above equations become

$$AC = \alpha \qquad (8)$$

where A is the (2k+1)x(2k+1) covariance matrix of input samples m(kT), k = -K,...,0,...,K with elements

$$a_{ki} = Em^*(kT)m(iT) = \psi^*_{ki} + \phi^*_{ki}$$

and C is a column vector of the (2k+1) tap gains and α is a column vector whose elements are the (2k+1) cross correlations

$$\alpha_i = EI_0 m^*(iT)$$

The solution of these equations in matrix form is

$$C_{opt} = A^{-1}\alpha$$

where C_{opt} is the vector of optimum tap gains. The minimum MSE is

$$\varepsilon_{min} = \sigma_0^2 - Re(\alpha_t^* C_{opt})$$

where α_t denotes the transpose of α.

Example: Let the channel be ideal with impulse response $\delta(t)$. In this case

$$z(k) = \begin{cases} 1 & k=0 \\ 0 & k\neq 0 \end{cases}$$

$$\psi_{kj} = \begin{cases} \sigma_0^2 & k=j \\ 0 & k\neq j \end{cases}$$

$$\phi_{kj} = \begin{cases} N_0 \frac{1}{T} & k=j \\ 0 & k\neq j \end{cases}$$

$$\alpha_k = \begin{cases} \sigma_0^2 & k=0 \\ 0 & k\neq 0 \end{cases}$$

Hence, A is a diagonal matrix with elements $\sigma_0^2+\frac{1}{T} N_0$ and C is a vector with elements equal to zero except the middle one which equals σ_0^2. The tap gains can easily be computed:

$$c_k = \begin{cases} \sigma_0^2/(\sigma_0^2+ \frac{1}{T} N_0) & k=0 \\ 0 & k\neq 0 \end{cases}$$

If $r = (\sigma_0^2)/(N_0/T)$, then $c_0 = 1/(1+r^{-1})$. The minimum MSE is

$$\varepsilon_{min} = \sigma_0^2 - \frac{\sigma_0^2}{1+r^{-1}} = \frac{\sigma_0^2}{1+r}$$

For large SNR:

$$\lim_{r\to\infty} \varepsilon_{min} = 0$$

A recursive method for inverting matrix A or determining the tap gains c_k is presented in [1]. This method employs the steepest descent technique. Initially a set of tap gains $\{c_k\}$ are chosen and then each tap gain is changed in the direction opposite to its corresponding gradient component. The change in the k-th tap gain is proportional to the size of the k-th gradient component. Let $\{c_k^{(0)}\}$ denote the initial values of the tap gains. Thus, succeeding values are obtained according to the relation:

$$c_k^{(\nu+1)} = c_k^{(\nu)} - \left(\frac{\Delta}{2}\right) \frac{\partial \varepsilon^{(\nu)}}{\partial c_k}$$

$$= c_k^{(\nu)} \pm \Delta E e^{(\nu)} m^*(kT), \quad k = -K,\ldots,0,\ldots,K \tag{9}$$

where $c_k^{(\nu)}$ is the value of the k-th tap gain at the ν-th iteration, $\partial\varepsilon^{(\nu)}/\partial c_k$ is the k-th gradient component at the ν-th iteration, $e^{(\nu)}$ is the error at the ν-th iteration, m(kT) is the sample of the matched filter output in the k-th tap of the TDL filter, and Δ is a positive number chosen small enough to insure convergence of the iterative procedure. If the minimum MSE is reached for some $\nu = \nu_0$, then $E\, e^{(\nu)} m^*(kT) = 0$ for all k and for all $\nu \geq \nu_0$ so that no further changes occurs in the tap gains.

The recursive equation (9) requires the exact knowledge of the error signal e. To overcome this difficulty,it is suggested in [1] to use the following equation instead

$$c_k^{(\nu+1)} = c_k^{(\nu)} + \Delta[e^{(\nu)} m^*(kT)] \tag{10}$$

where $e^{(\nu)}m^*(kT)$ is the product between the error $e^{(\nu)}$ at the ν-th iteration and the complex conjugate of the data sample m(kT) in the k-th tap at the ν-th iteration. The equalizer as formulated by (10) is illustrated in Figure 2.

It can be shown that the iterative technique of equation (10) will converge if the iteration step size Δ satisfies the following inequality [1]

$$\Delta < 2/\lambda$$

where λ is the largest eigenvalue of matrix A. A simpler bound for Δ is derived in [1] and is stated below

$$\Delta < \frac{1}{(2K+1)(\phi_{00}+\psi_{00})} \tag{11}$$

where

$$\psi_{00} = \sigma_0^2 \sum_{n=-\infty}^{\infty} |z(nT)|^2$$

$$\phi_{00} = N_0/T$$

A practical value of Δ is also suggested

$$\Delta = \frac{.2}{(2K+1)(\phi_{00}+\psi_{00})} \tag{12}$$

It can be shown that the convergence time of the tap gains is a linear function of Δ and simulation has revealed that with Δ selected from equation (12) the convergence times are usually close to 500T [1], where T is the symbol duration.

3. TDL FILTER SIMULATION

We have yet to describe the way in which the steady state tap gains of the TDL filter are obtained in the simulation program. Two modeling simplifications, described below, are made that allow a costly Monte Carlo simulation to be avoided. These specifications lead to somewhat different filter operation than that shown in Figure 2. A 63 bit maximal-length PN sequence noise-free signal is repeatedly processed until the TDL filter is no longer changing its state, i.e., its tap weights.

The first modeling simplification is that the filter acts to minimize the expected value, over the noise, of the averages of the squared error in the received bits. The other simplification is to assume that the transmitted bit I_0 is given by

$$I_0 = \text{sign}(E\hat{I}_0)$$

where $\hat{I}_0$ is the corresponding output of the TDL filter, instead of by

$$I_0 = \text{sign}(\hat{I}_0)$$

as in the actual TDL filter. In the case of high SNR the two definitions are very close. The latter simplification is equivalent to replacing m(kT) of equation (4) by noise free samples.

With the above two simplifications, the term $\partial\varepsilon/\partial c_k$ of equation (9) is given by

$$\frac{\partial\varepsilon}{\partial c_k} = -\frac{2}{63}\sum_{n=1}^{63}(I_n - E\hat{I}_n)r^*[(n+k)T] \;, \qquad k = -K,\ldots,0,\ldots,K \tag{13}$$

where $r^*[(n+k)T]$ is the noise free part of $m^*((n+k)T)$. Notice that if $N_0 = 0$, equation (13) is the same as $\partial\varepsilon/\partial c_k$ used in equation (9).

Since equation (13) does not represent a true Monte Carlo simulation, the convergence rate of the simulation program does not correspond to a realistic case. In the program the tap gains are obtained with a few iterations, whereas, in practice perhaps a few hundred iterations will be required.

4. NUMERICAL RESULTS

The channel under consideration is shown in Figure 3. The channel model used in the simulation program, however, is shown in Figure 4. It is desirable to explore the performance of a TDL equalizer as applied to the channel under consideration. The problem here is the scarcity of bandwidth and a TDL equalizer is used to increase channel throughput. Since perfect carrier phase recovery is assumed, the QPSK and SQPSK results are the same as BPSK. In the following, first the simulation results for NRZ pulses are presented and then the biphase case is also shown.

Figures 5-9 show the improvement in BER made possible by equalization for different data rates with K=1 (3 taps). BER is given as a function of E_b/N_0. The dashed curve shows the theoretical (ideal infinite bandwidth channel) case, the dotted curve shows the imperfect channel and the solid curve shows the equalized channel. The next 5 figures (10-14) show BER when K=3 (7 taps). Apparently the improvement due to the increased number of taps is negligible. Figure 15 shows the performance loss for the equalized and the degraded links. At BT = 1 a gain of close to 3 dB is achieved by equalization where B denotes the RF channel bandwidth.

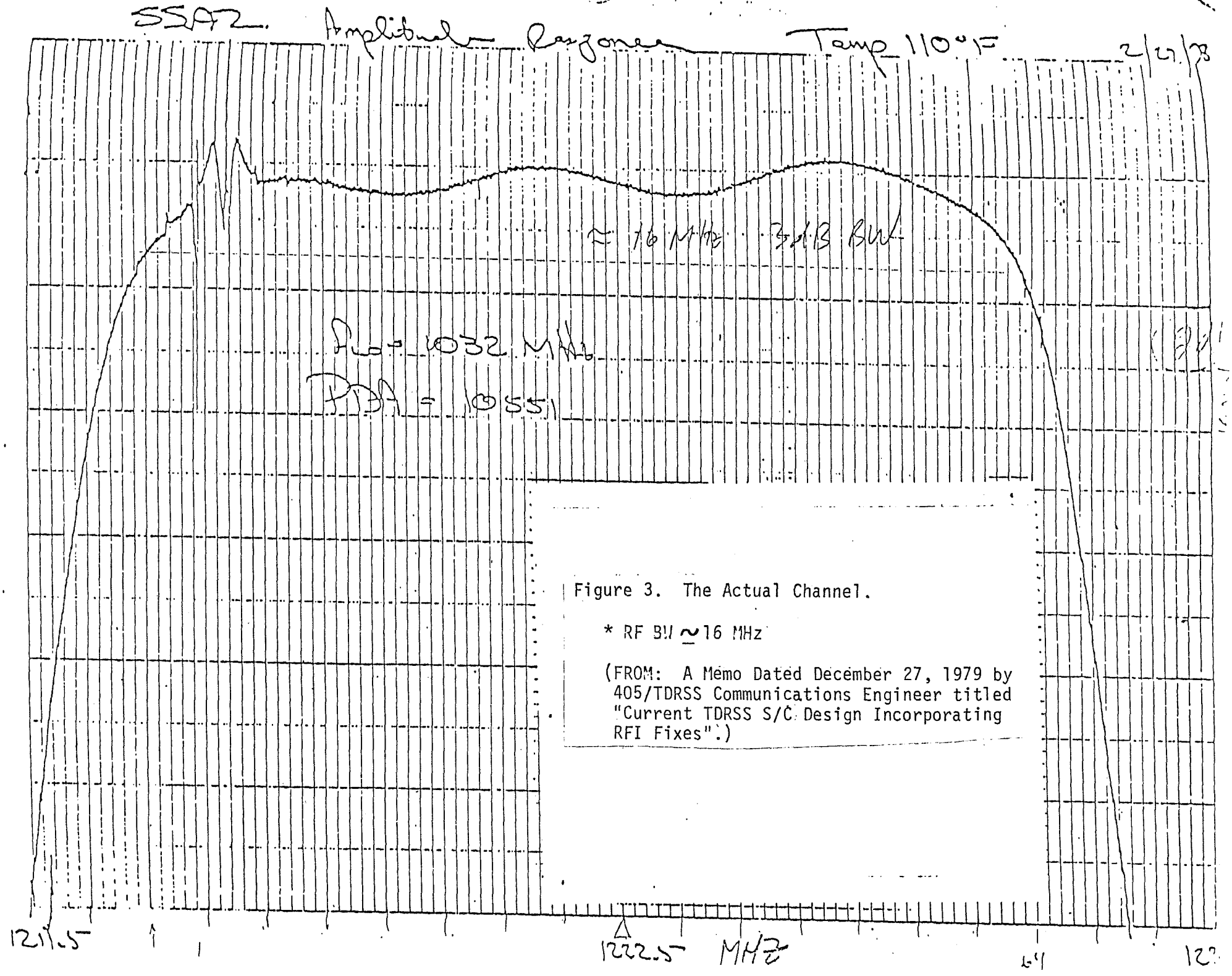

Figure 3. The Actual Channel.

* RF BW ~16 MHz

(FROM: A Memo Dated December 27, 1979 by 405/TDRSS Communications Engineer titled "Current TDRSS S/C Design Incorporating RFI Fixes".)

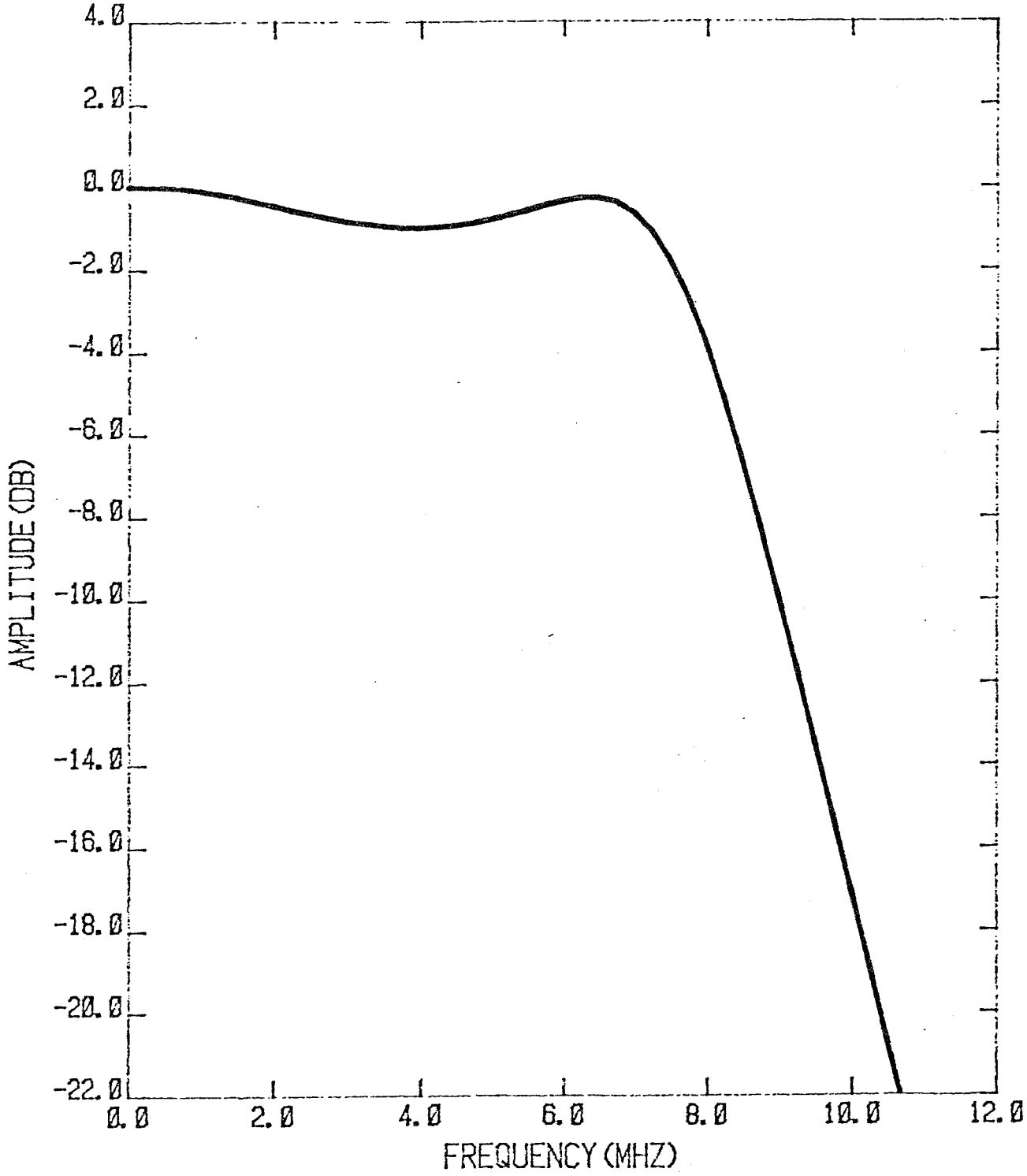

Figure 4. Simulated Channel: Cascade of a 5-Pole Butterworth and a 3-Pole Chebyshev with One dB Ripple, Both 16.5 MHz.

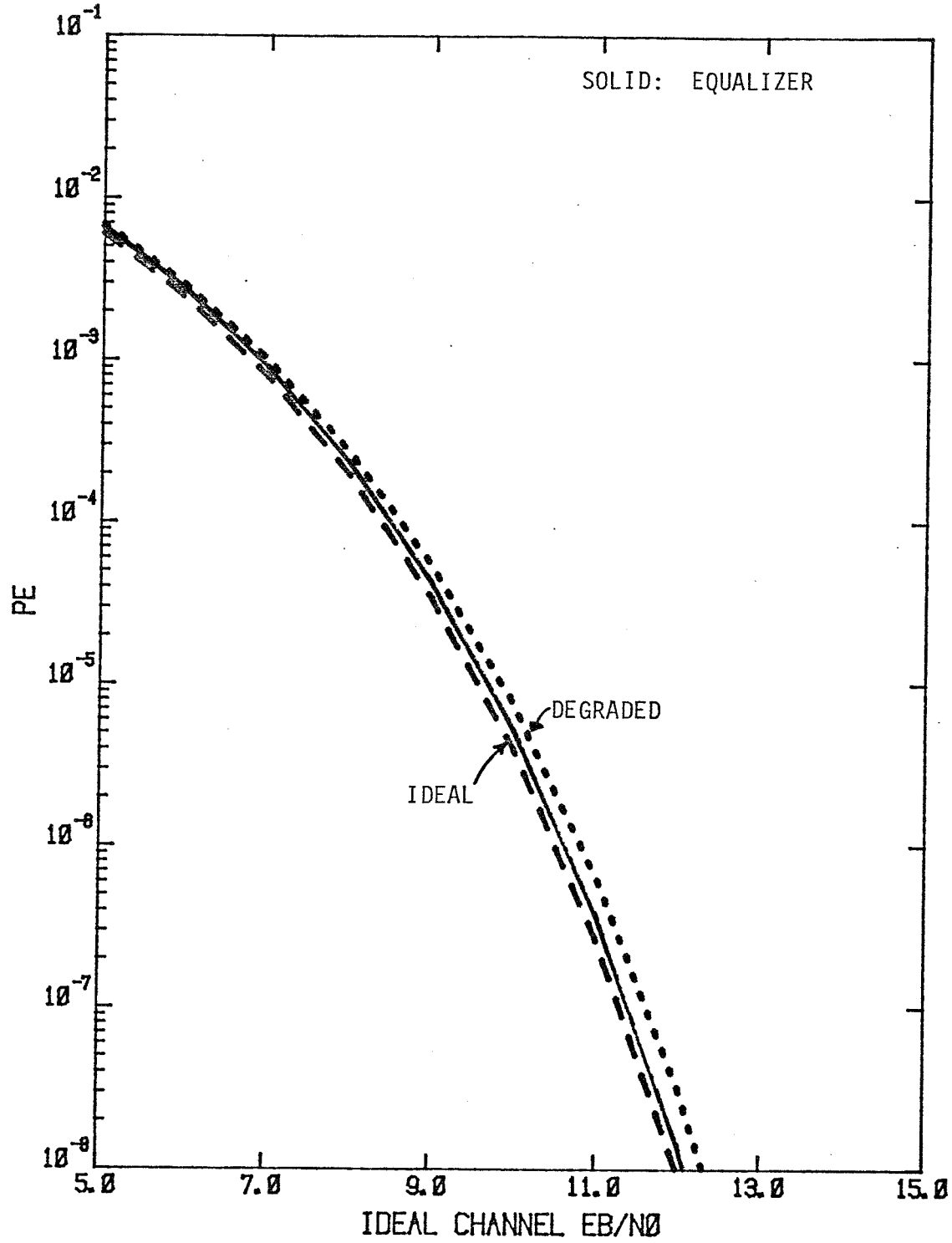

Figure 5. BER Versus E_b/N_0.

- DATA RATE = 3 Mbps
- K = 1 (3 TAPS)
- NRZ
- BPSK

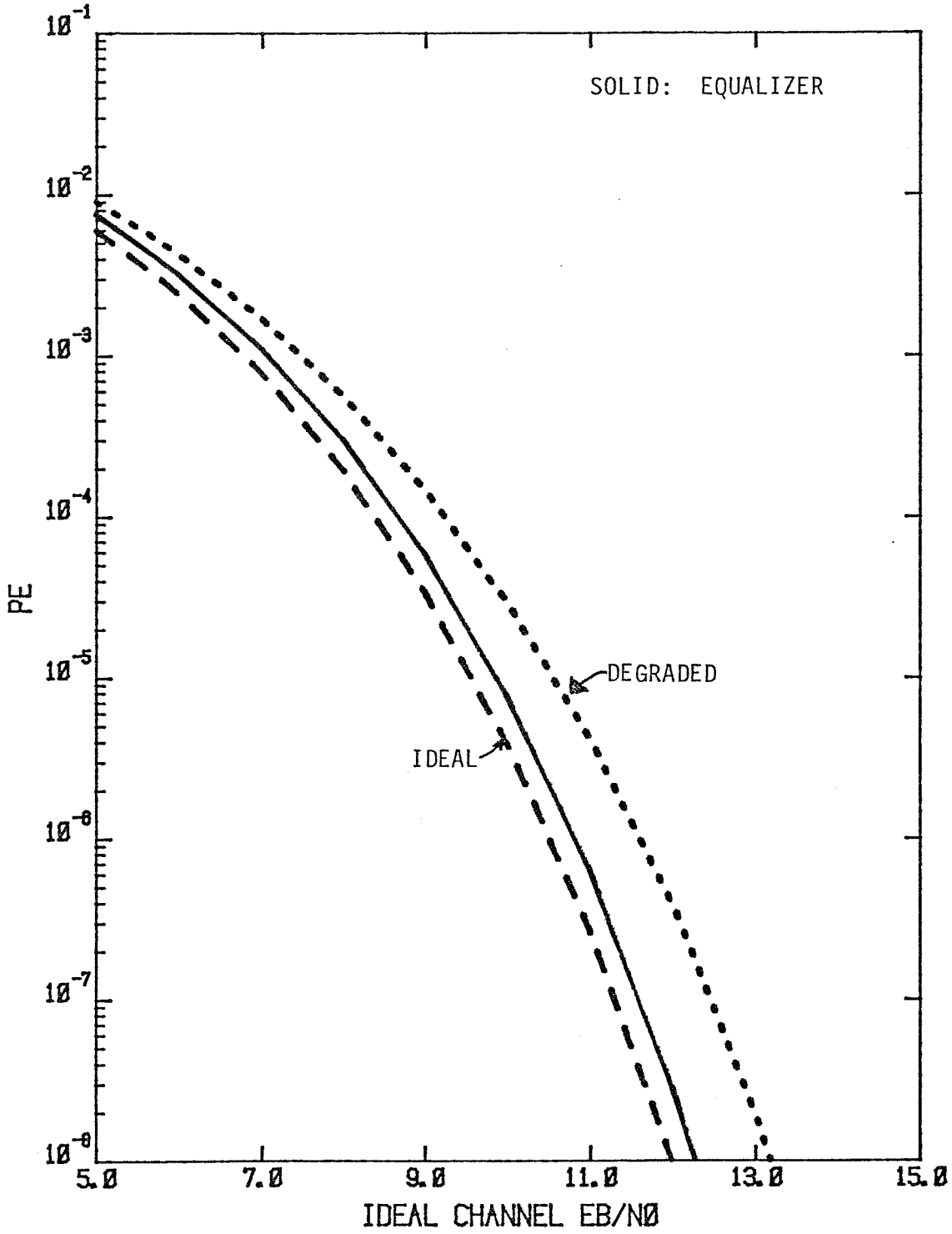

Figure 6. BER Versus E_b/N_0.

- DATA RATE = 6 Mbps
- K = 1 (3 TAPS)
- NRZ
- BPSK

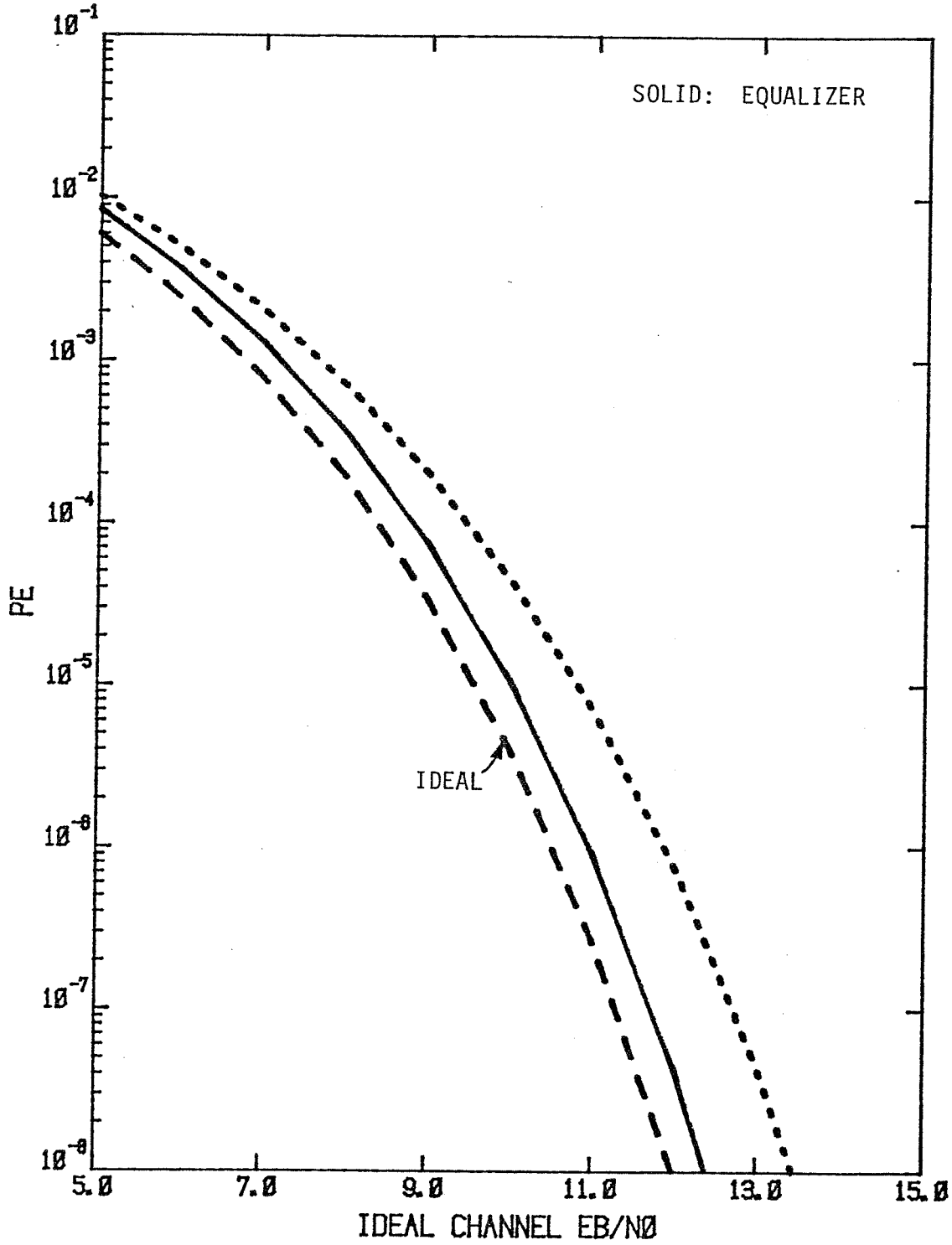

Figure 7. BER Versus E_b/N_0

- DATA RATE = 9 Mbps
- K = 1 (3 TAPS)
- NRZ
- BPSK

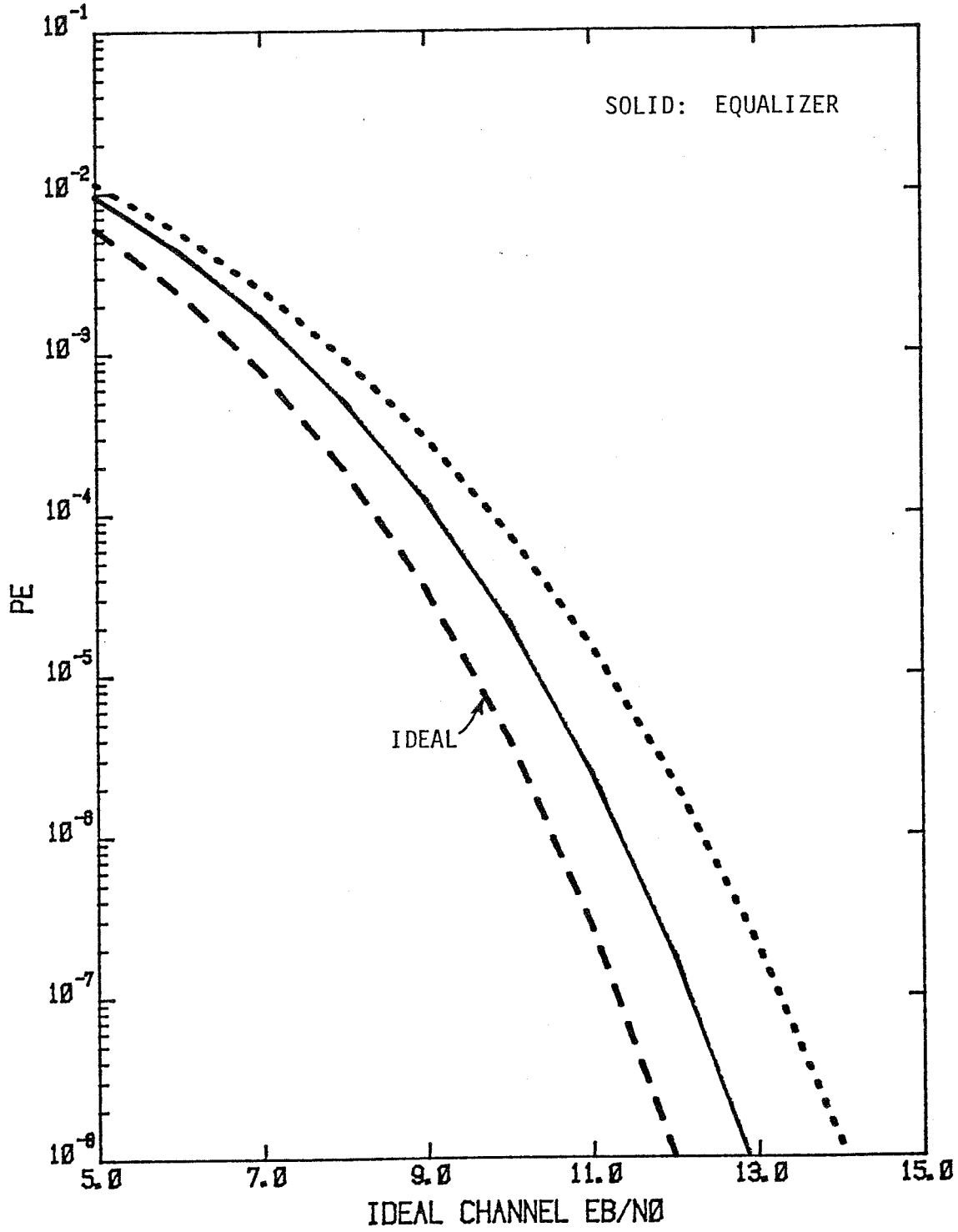

Figure 8. BER Versus E_b/N_0.

- DATA RATE = 12 Mbps
- K = 1 (3 TAPS)
- NRZ
- BPSK

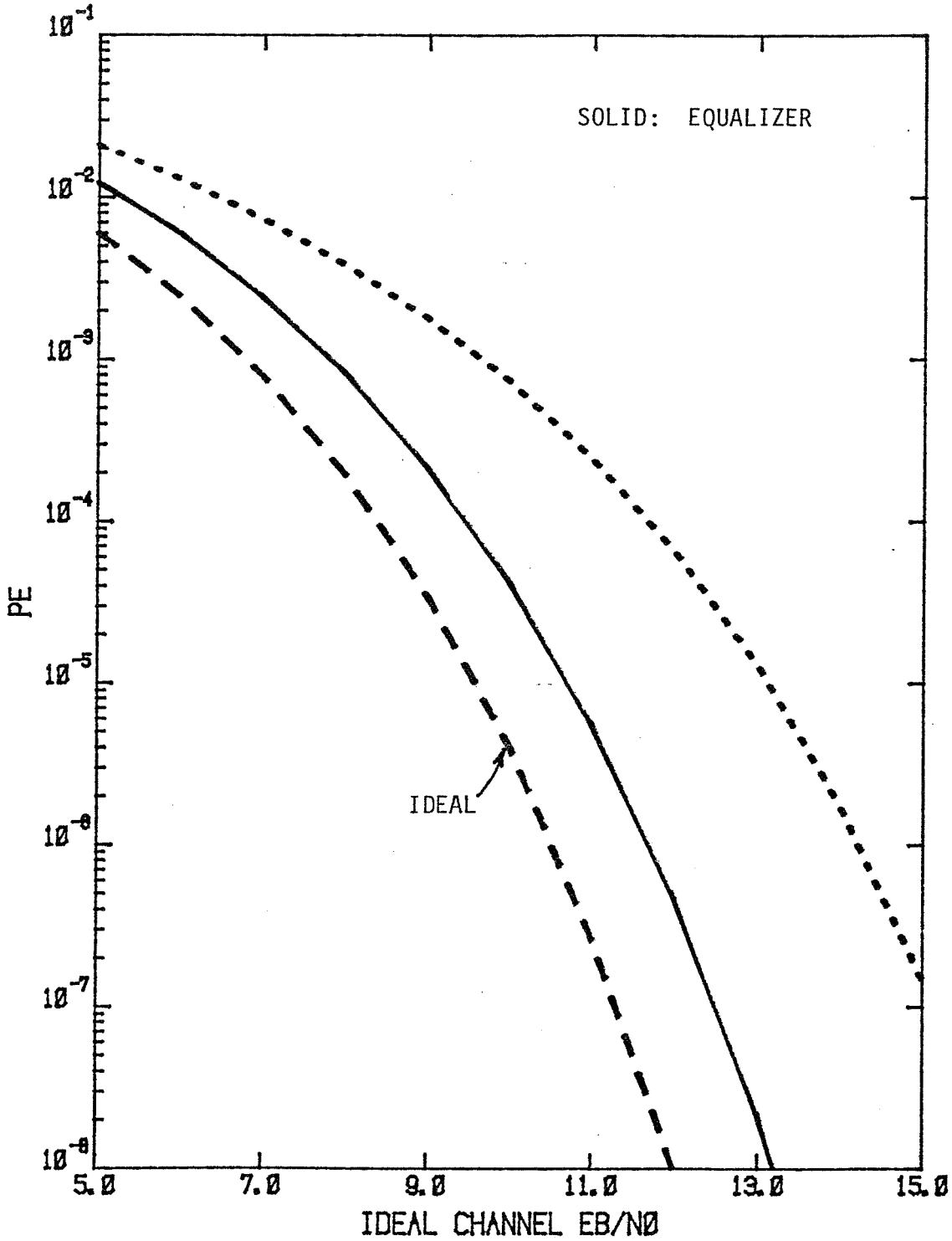

Figure 9. BER Versus E_b/N_0.

- DATA RATE = 16 Mbps
- K = 1 (3 TAPS)
- NRZ
- BPSK

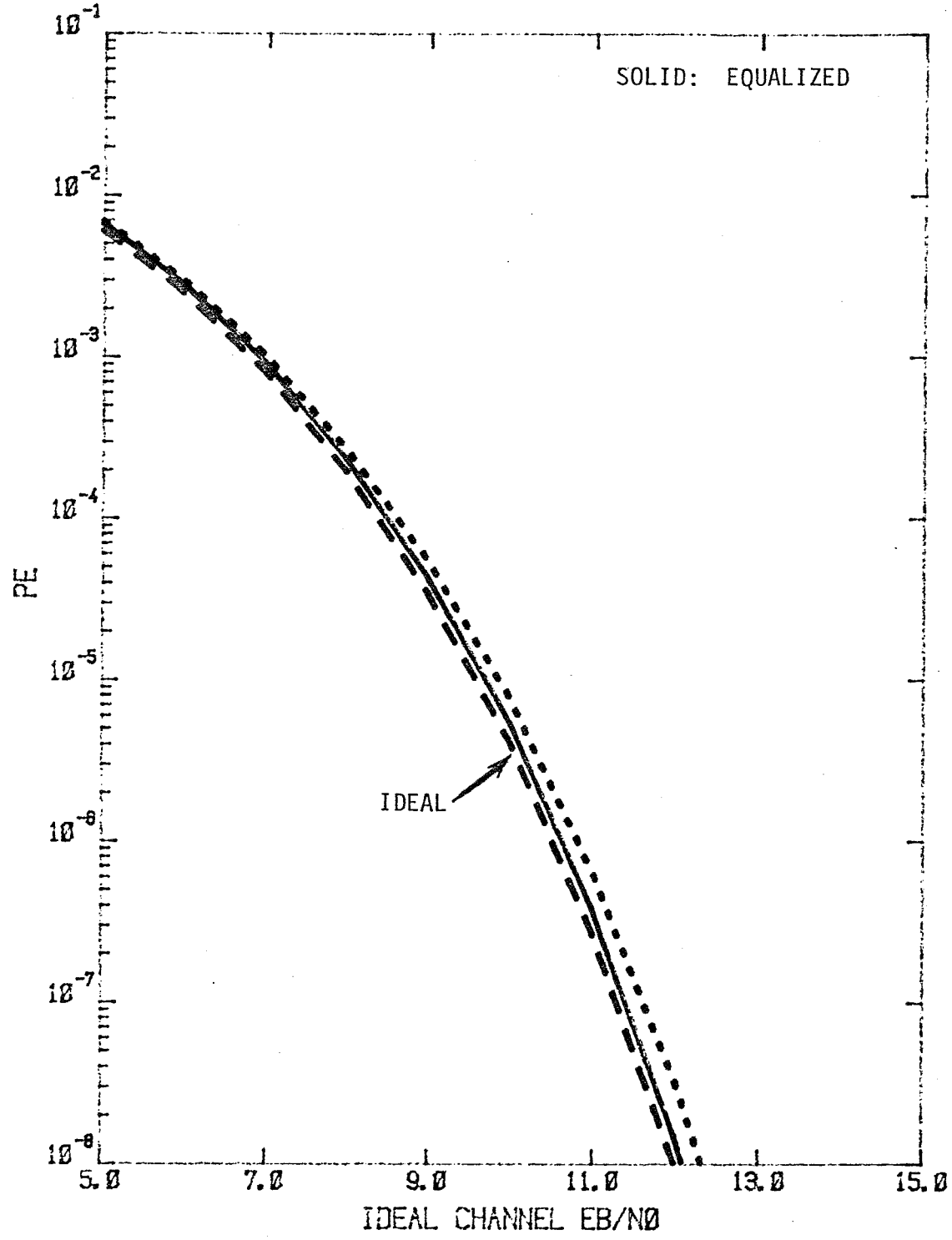

Figure 10. BER versus E_b/N_0.

- DATA RATE = 3 Mbps
- K = 3 (7 TAPS)
- NRZ

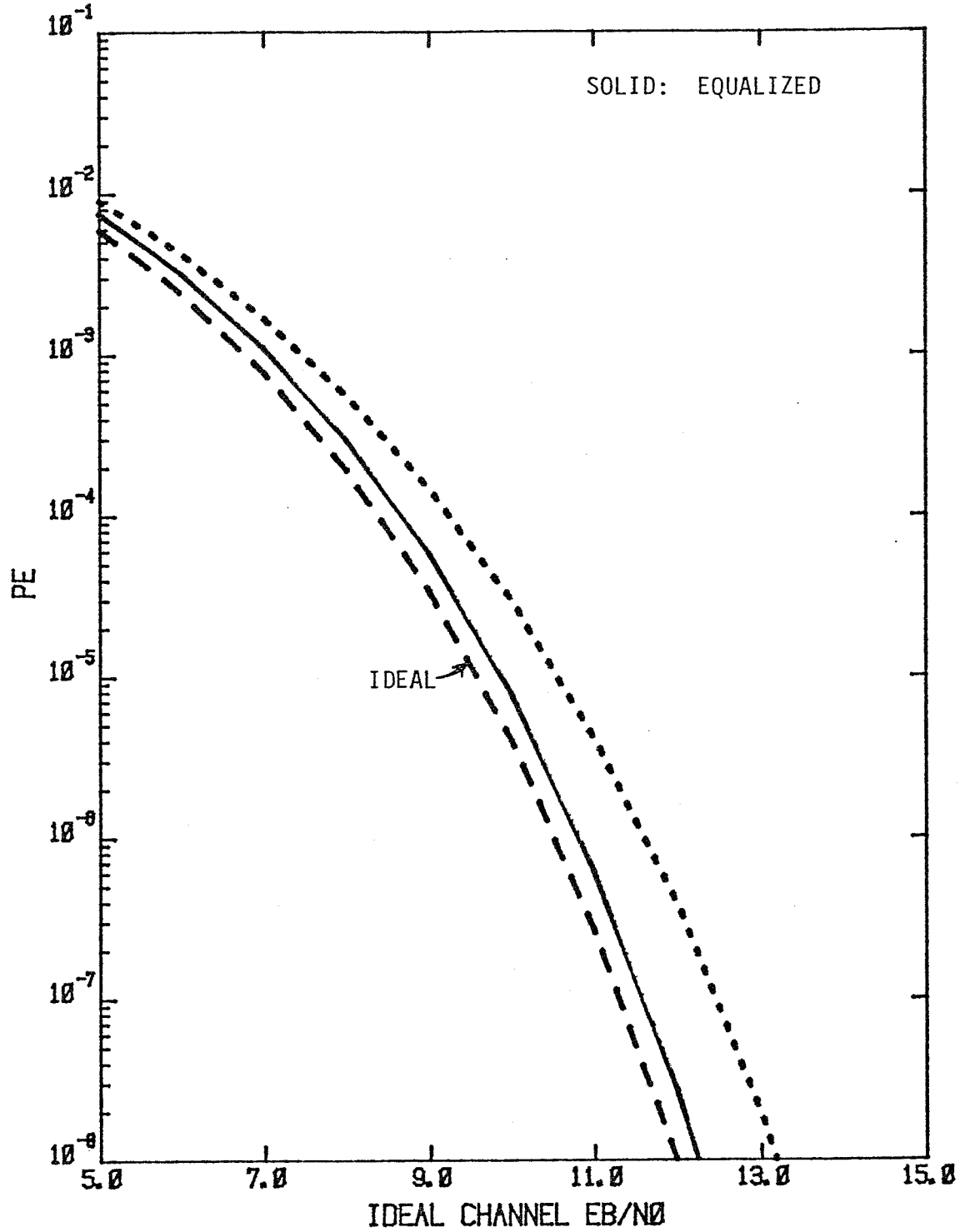

Figure 11. BER versus E_b/N_0.

- DATA RATE = 6 Mbps
- K = 3 (7 TAPS)
- NRZ

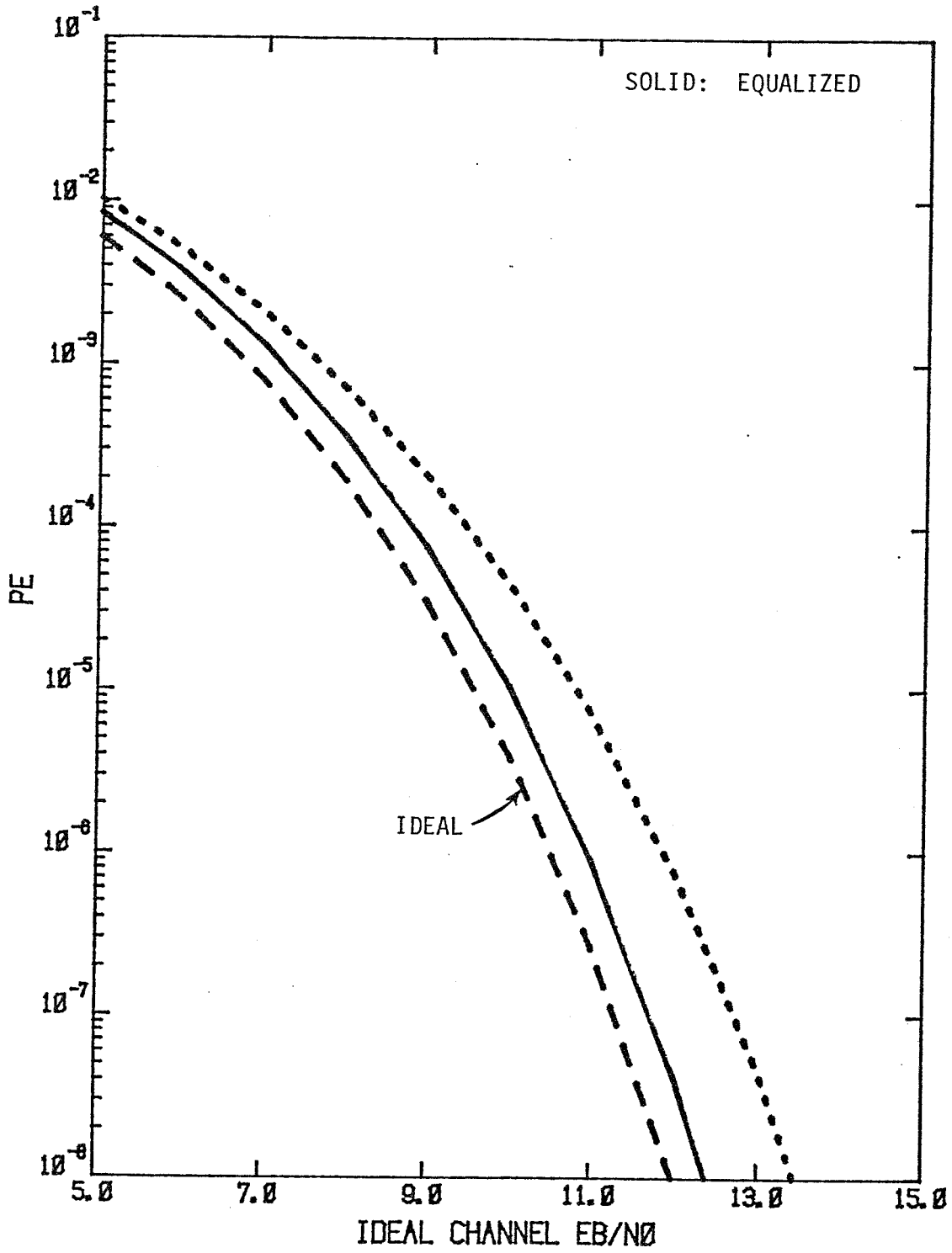

Figure 12. BER Versus E_b/N_0.

- DATA RATE = 9 Mbps
- K = 3 (7 TAPS)
- NRZ

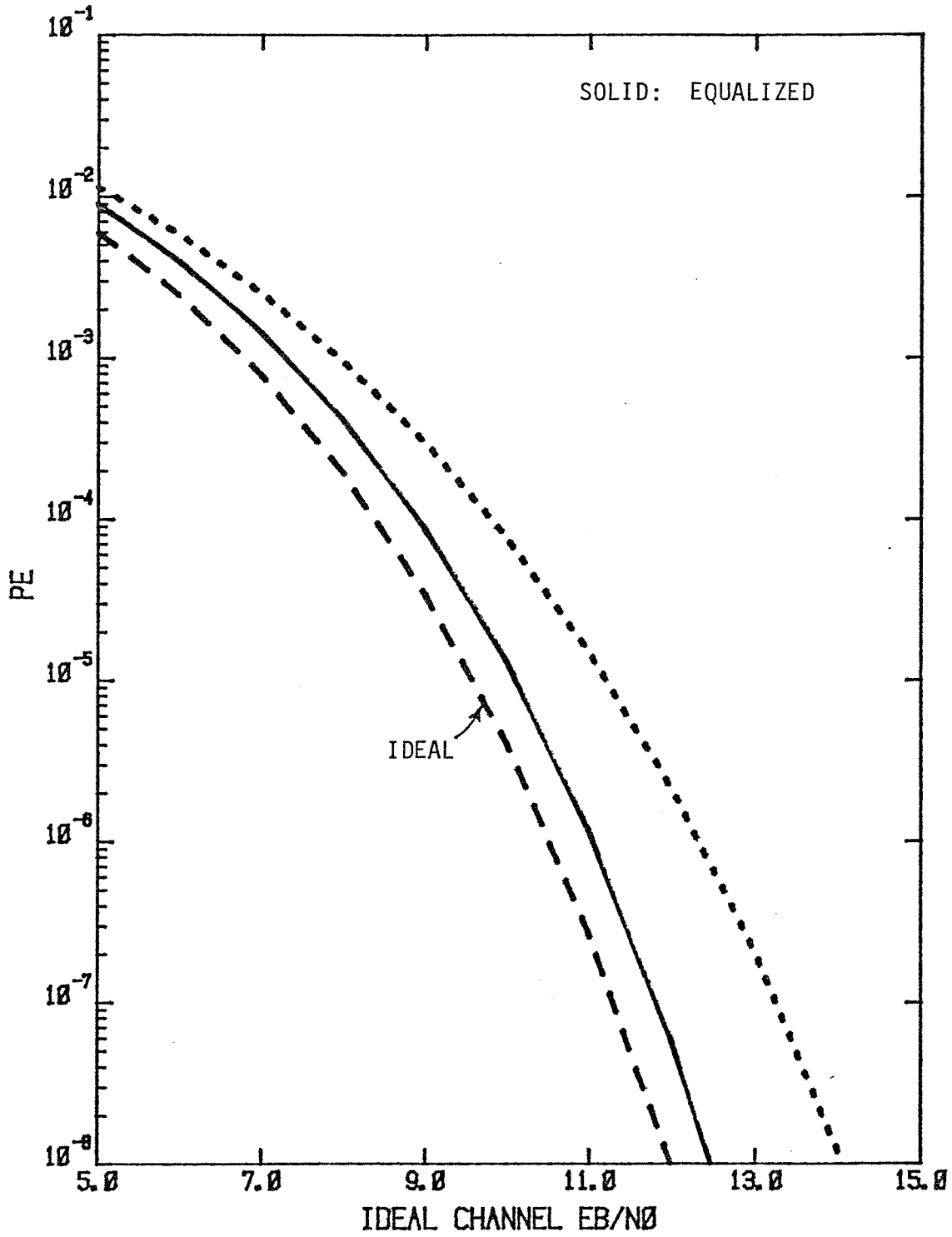

Figure 13. BER versus E_b/N_0.

- DATA RATE = 12 Mbps
- K = 3 (7 TAPS)
- NRZ

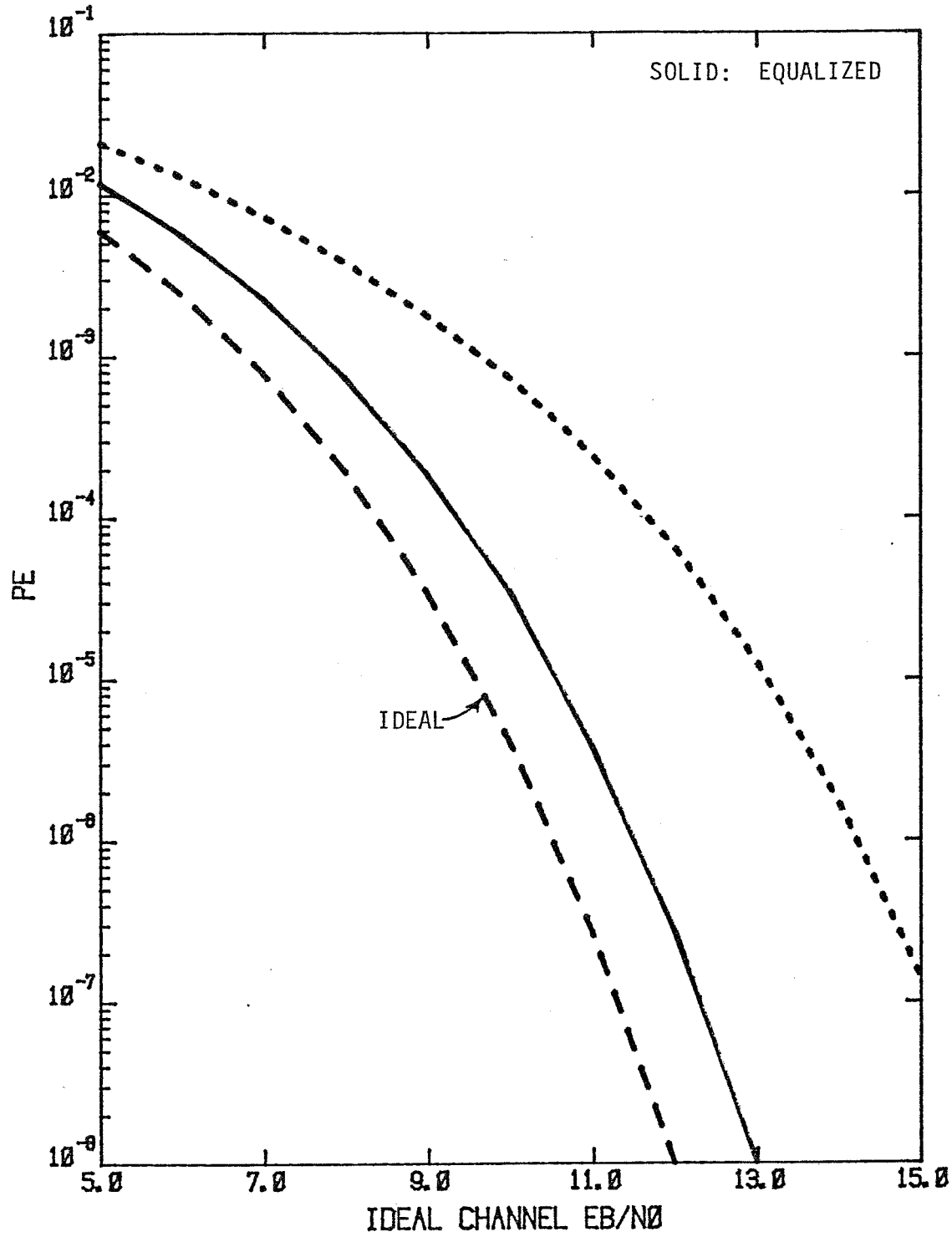

Figure 14. BER versus E_b/N_0.

- DATA RATE = 16 Mbps
- K = 3 (7 TAPS)
- NRZ

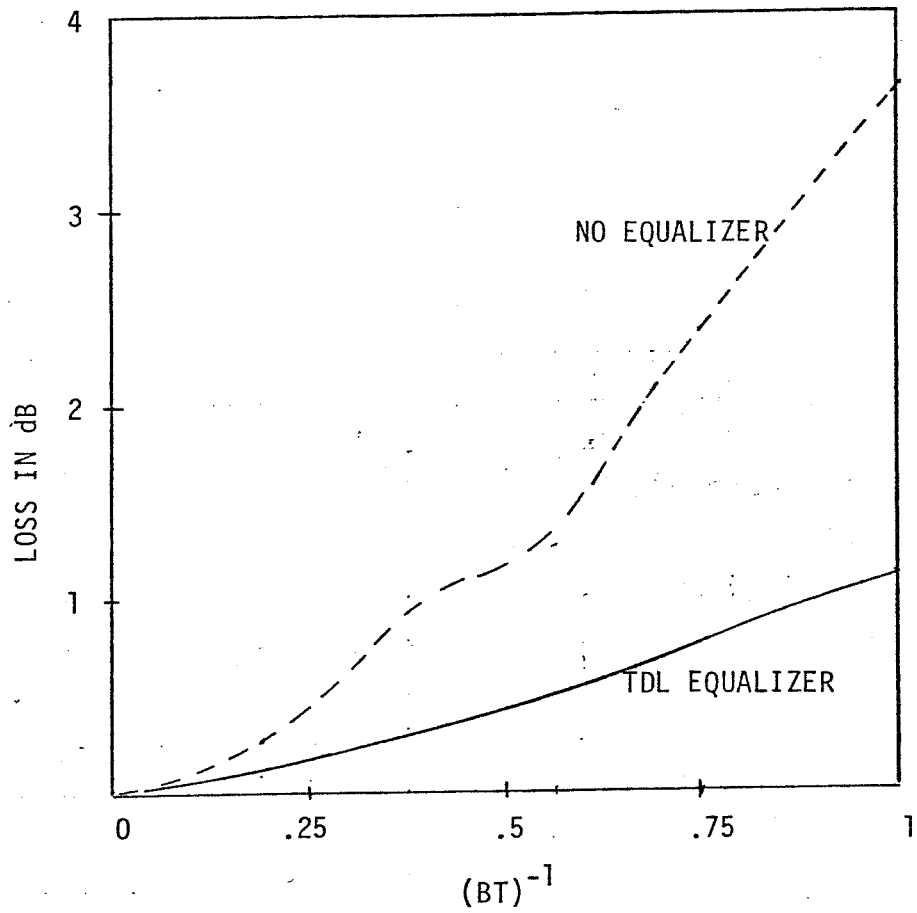

Figure 15. Performance Loss Due to Band Limited Channel.

- BPSK
- NRZ
- K=1 (3 TAPS)
- $P_E=10^{-5}$
- B=RF BANDWIDTH

The simulation results for biphase signal are illustrated in Figures 16, 17, and 18 for data rates 3, 6 and 9 Mbps, respectively. Note that for 3 and 6 Mbps data rates the equalizer is insensitive to the number of taps. However, with 9 Mbps data rate the 7-tap equalizer performs better than the 3-tap equalizer. Figure 19 shows the loss in dB due to insufficient bandwidth. The dotted line illustrated the link loss due to bandlimited channel as a function of the reciprocal of the BT product. The solid and the dashed lines correspond to the same link with 3-tap and 7-tap equalizers, respectively.

4. CONCLUSIONS

In this report an overall review of a TDL filter which minimizes the link MSE is presented. It has been shown that the TDL filter is mathematically equivalent to the inversion of a matrix whose entries depend on the impulse response of the channel and the noise statistics. Since the data is received in a sequence, a recursive solution is considered where the convergence rate of the tap gains depends on the step size of the recursive equation.

A simulation program is utilized to obtain the performance of the TDL filter for a specific channel. The channel model used in the program is only an approximation of the practical medium. The channel is modeled by a cascade of two filters, viz., a 5-pole Butterworth and a 3-pole Chebyshev. Under the assumptions of symmetric channel and perfect carrier phase recovery, the BPSK and QPSK modulations produce similar results. The minimum number of taps is 3. A 3-tap TDL filter appears sufficient for equalizing NRZ signals but a higher number of taps may be required for biphase signals. At BT=1, a 3 dB improvement is achieved due to the equalizer when the signal format is NRZ.

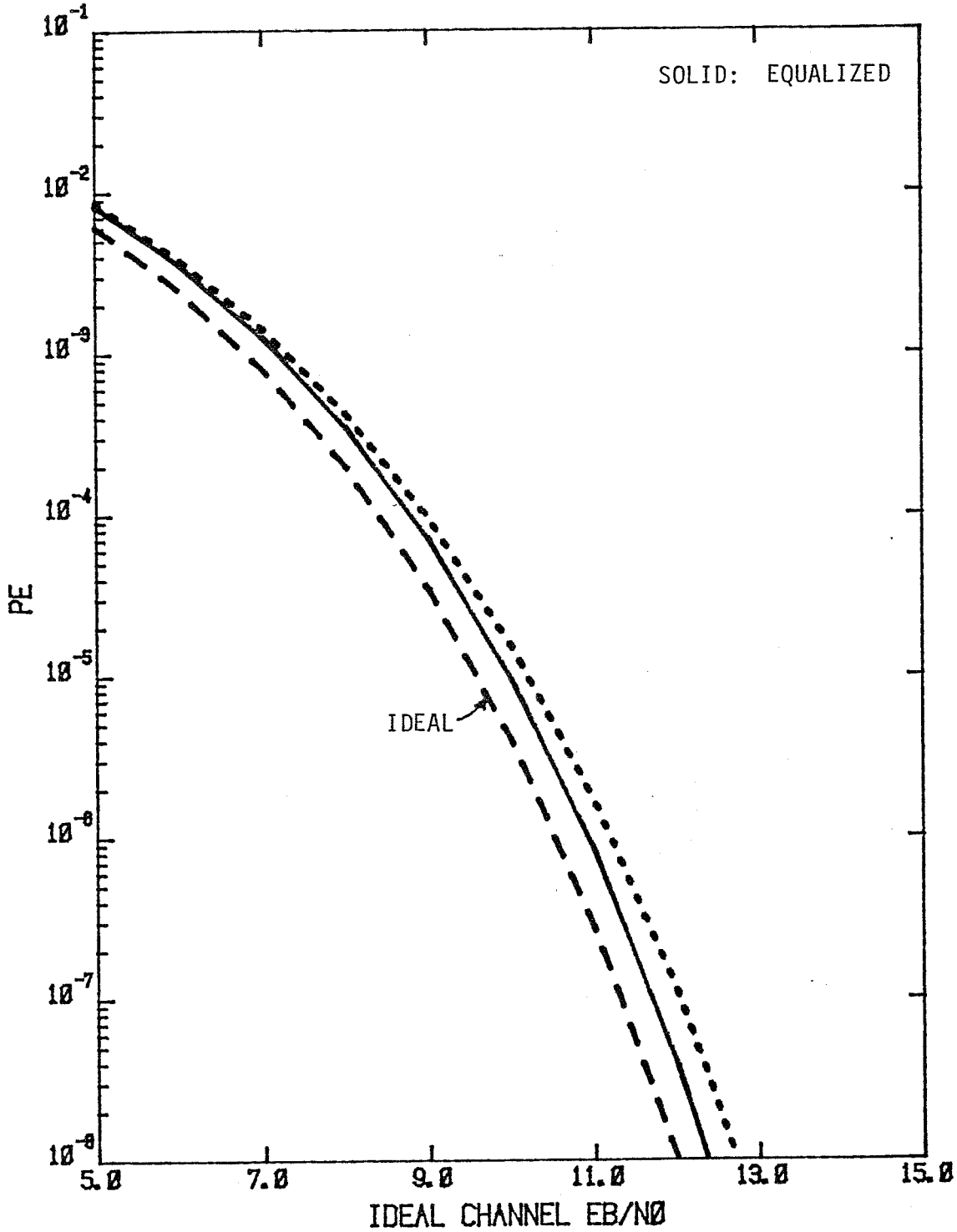

Figure 16. BER Versus E_b/N_0.

- DATA RATE = 3 Mbps
- K = 1,3
- BIPHASE
- BPSK

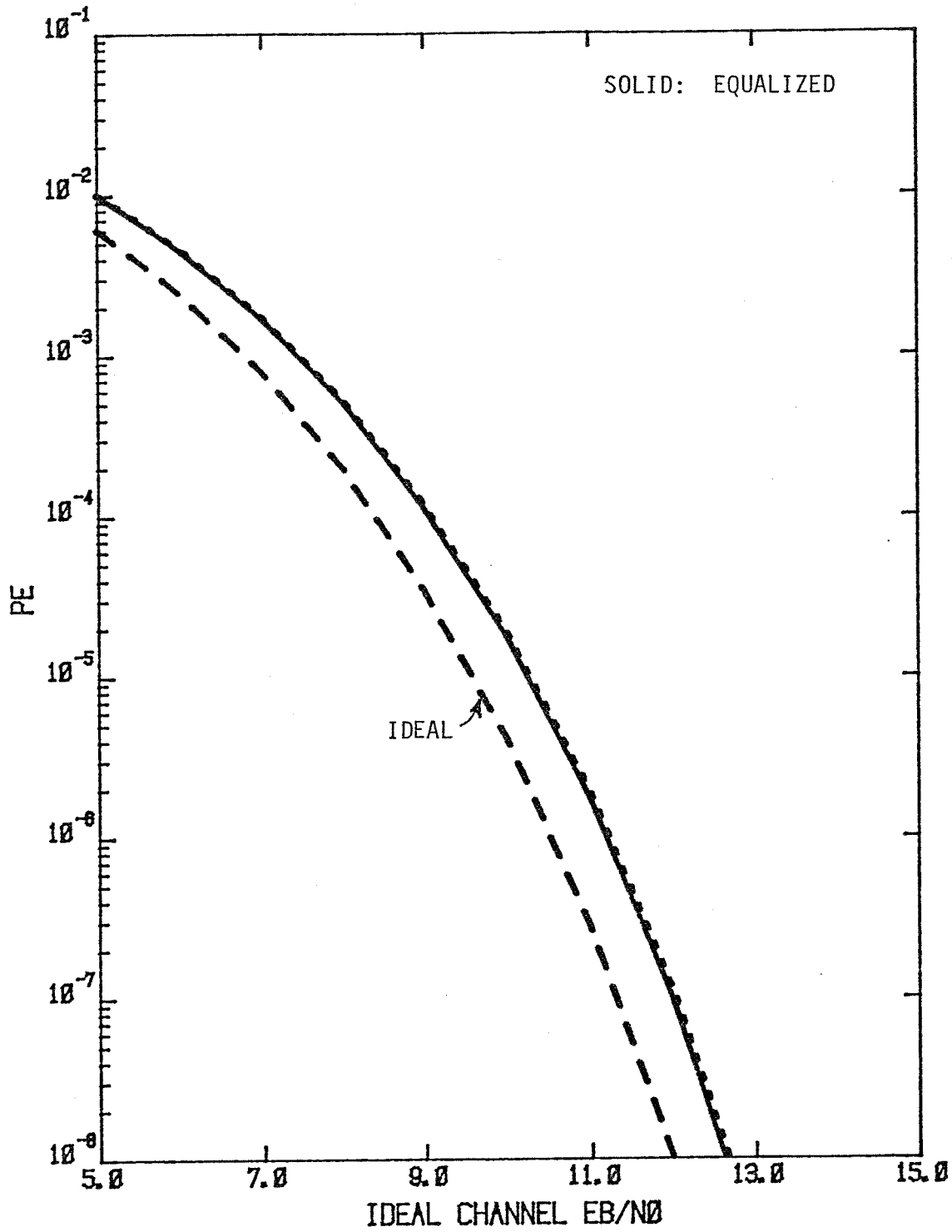

Figure 17. BER Versus E_b/N_0.

- DATA RATE = 6 Mbps
- K = 1,3
- BIPHASE
- BPSK

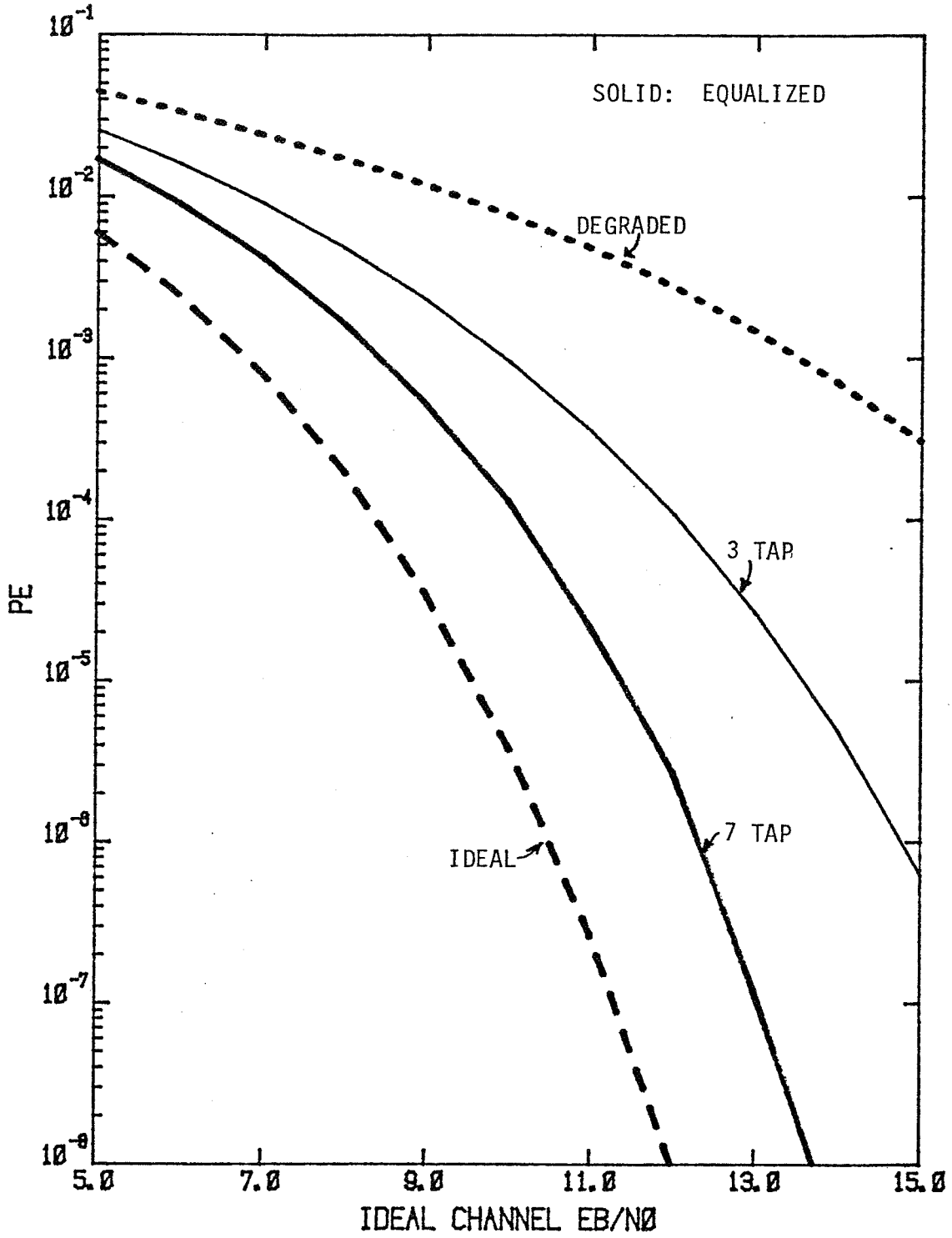

Figure 18. BER Versus E_b/N_0.

- DATA RATE = 9 Mbps
- K = 1,3
- BIPHASE
- BPSK

More work on dispersive channel equalization can be recommended as follows:

(1) Asymmetric Channel: In this case the channel characteristic has to be sampled and passed to the simulation program. Asymmetric channels are known to produce the crosstalk effect between the inphase and the quadrature signals. In this case the tap gains can become complex.

(2) Equalizer Speed: To determine the equalizer speed a true Monte Carlo simulation is necessary. If the speed of the present equalizer is found not satisfactory, faster techniques [2]-[4] have to be considered.

(3) Figure 19 shows that no reasonable system operation is feasible for BT less than 2 when the data is biphase formatted. To extend the equalizer power, nonlinear or feedback techniques have to be considered [5], [6].

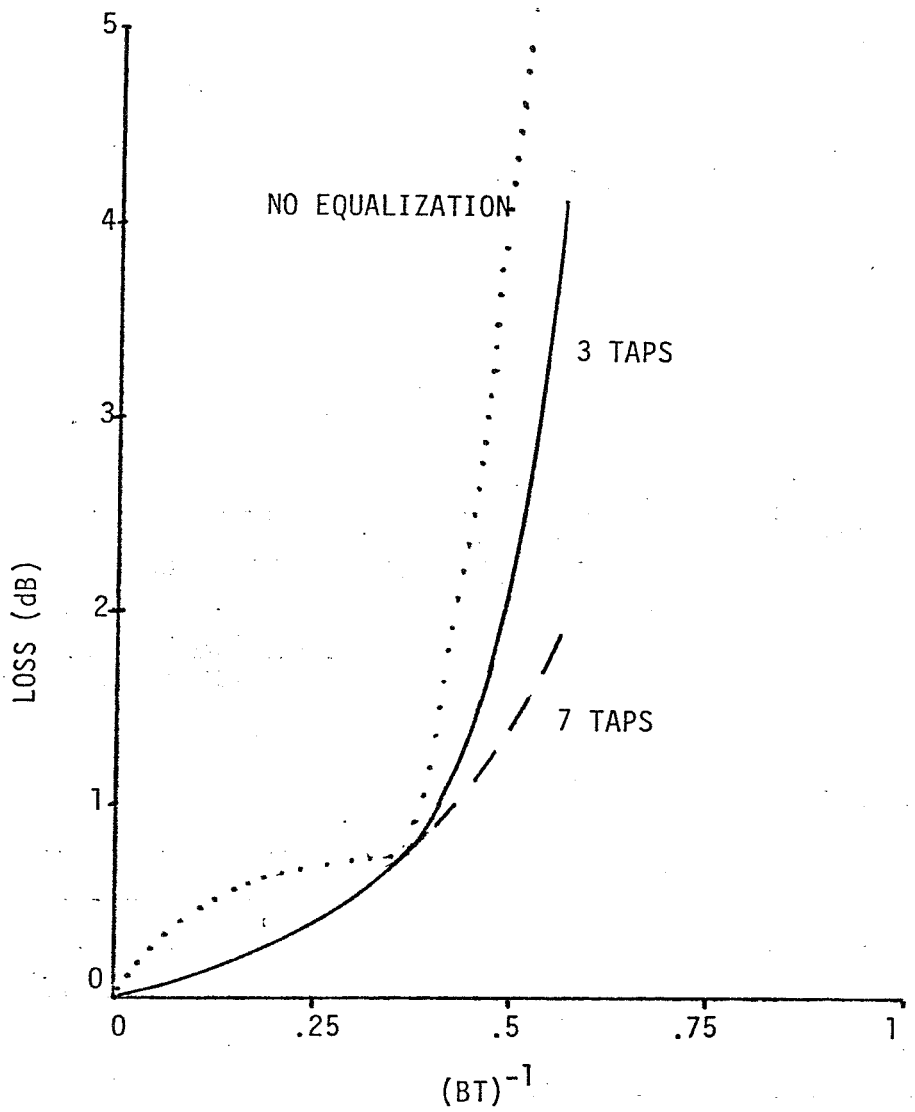

Figure 19. Performance Loss Due to Band Limited Channel

- BPSK
- BIPHASE
- $P_E=10^{-5}$
- B=RF BANDWIDTH

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APPENDIX D

NEW TECHNIQUE FOR MEASURING PHASE-LOCKED LOOP PERFORMANCE

NEW TECHNIQUE FOR MEASURING PHASE-LOCKED LOOP PERFORMANCE

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Until now the acquisition, tracking threshold and frequency stability characteristics of transponders, coherent communication and navigation systems have been extremely difficult to measure. In fact, it was not uncommon to take weeks to set up special test equipments and days of manpower to run a variety of ill-defined tests. Often, because of calibration problems, manpower and cost limitations, the test accuracy was poor, unrepeatable, and probability in the tests was not conserved. In order to statistically characterize the performance measures which predict loop performance a new instrumentation and measurement system, called the Statistical Loop Analyzer, has been developed.

The Statistical Loop Analyzer (SLA) defines and performs probability conserving acquisition, tracking, phase and frequency stability tests. These tests eliminate certain calibration and test accuracy problems, reduce manpower requirements, and, hence, testing cost. Figure 1 illustrates a functional diagram of a typical test set up. Basically, SLA is a new, intelligent test instrumentation system capable of automatically measuring and recording the acquisition, tracking, and frequency stability performance characteristics of synchronization systems, e.g., phase-locked loops, transponders, symbol (bit) synchronizers, code loop synchronizers and carrier tracking loops. The SLA measurement system is designed to characterize the performance of breadboards, engineering prototype models and systems independent of the application. Additionally, the SLA is designed to accomodate a variety of baseband, carrier and spread spectrum modulation techniques, see Figure 2. The SLA can be used to perform system level tests by connecting it to the appropriate system test points. Many of these detailed applications and test set-ups are provided in Ref. 1.

The SLA offers the unique advantage of automatically performing (to the desired accuracy) several sets of statistical measurements thereby minimizing the operator's time required to measure performance. The test data is automatically processed and output in a form suitable for a final report. The test categories conducted by the SLA are carefully defined probability experiments; they have been individually and collectively defined using sound system engineering judgements motivated by modern telecommunication system theory and performance requirements.

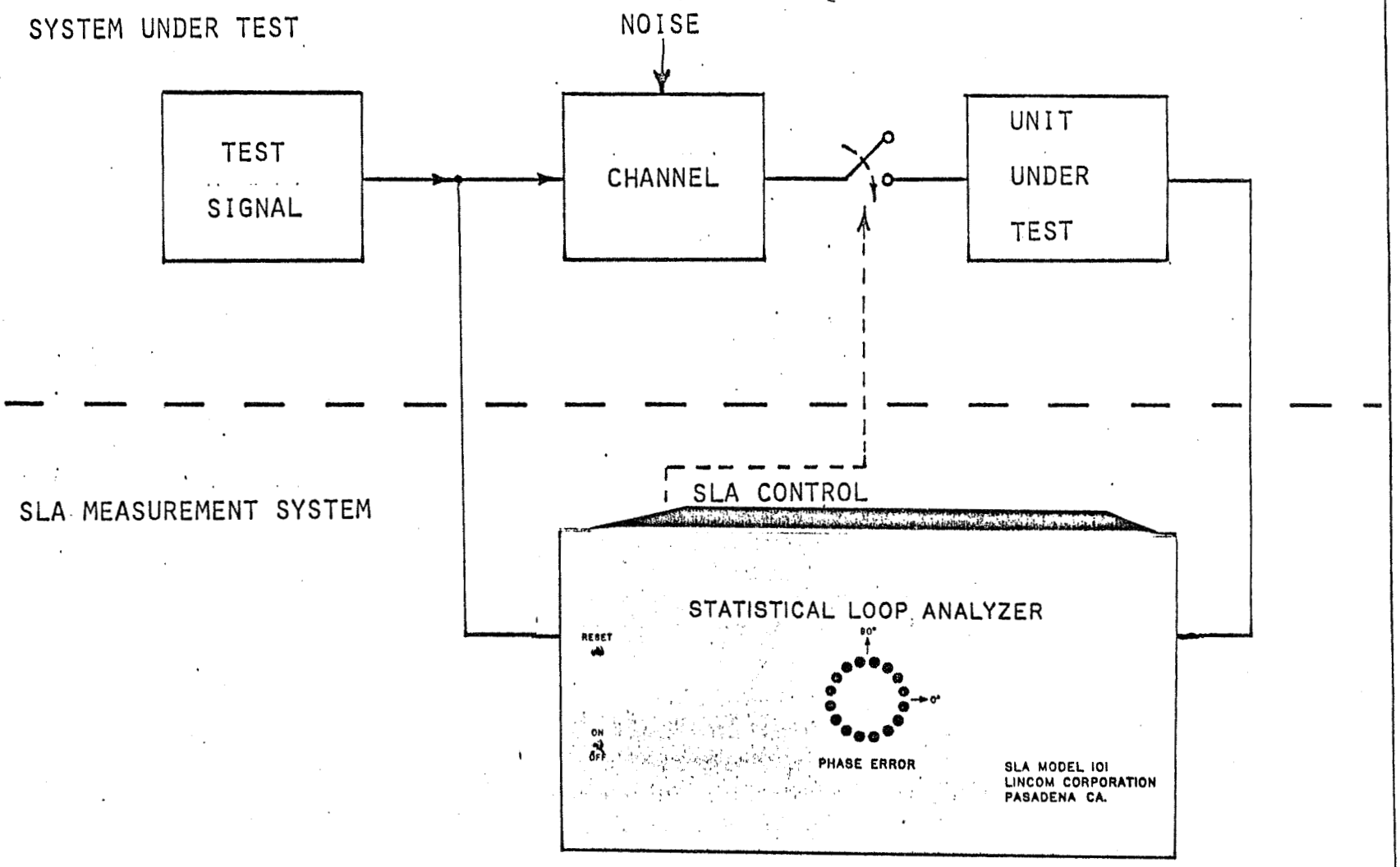
The test menu selectable by the test engineer is summarized below.

STATISTICAL LOOP ANALYZER TEST MENU

A - SELF TEST
B - MAINTENANCE
C - CALIBRATION
D - ACQUISITION TESTS
E - TRACKING TESTS
F - PHASE AND FREQUENCY STABILITY TESTS

The SELF TEST represents a test in which an internal test signal is generated and applied to the SLA to verify the correct operation of all the internal circuitry and certain aspects

Figure 1. Measurement Set Up.



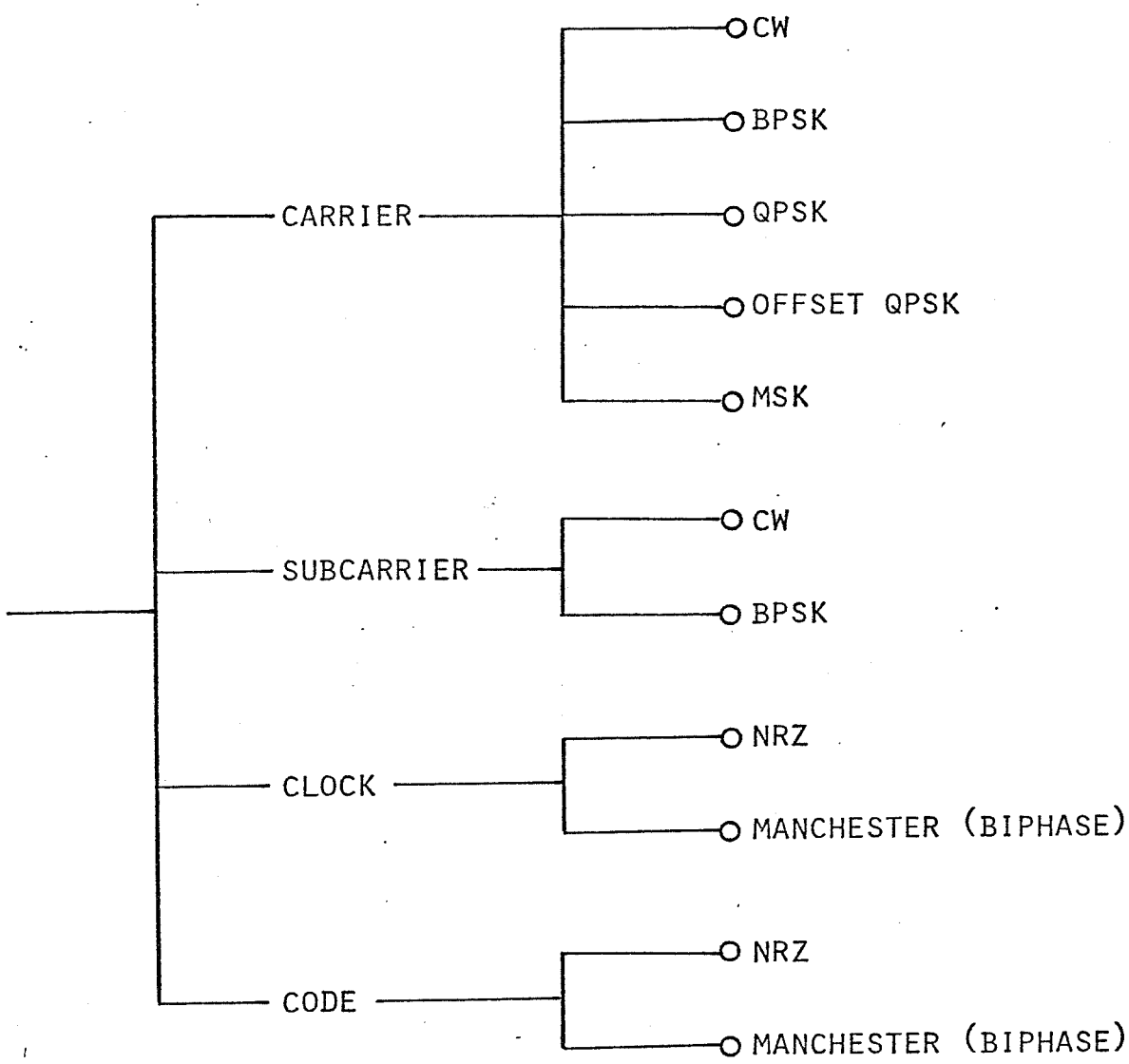


Figure 2. Signal Modulation Techniques Accepted by SLA.

of the SLA software. The Maintenance mode is used to perform diagnostic testing on the SLA and its peripherals.

Prior to conducting any test CALIBRATION of the SLA must be accomplished. Figure 2 summarizes the SLA test capability as a function of the signal modulation techniques.

ACQUISITION TESTS which the operator can select are:

A - PROBABILITY DISTRIBUTION OF ACQUISITION TIME
B - PROBABILITY OF ACQUISITION FOR A FIXED TIME

Acquisition Test A is designed to be a complete acquisition test fully characterizing acquisition performance while Acquisition Test B is designed to be a "quick look" acquisition test.

The TRACKING tests are broken into two main categories. They include:

PHASE ERROR JITTER - SLIP RATE TESTS

A - PHASE NOISE JITTER
B - PHASE ERROR JITTER AND SLIP RATE
C - RANGE JITTER

THRESHOLD TESTS

D - TRACKING THRESHOLD
E - SLIP RATE

The PHASE AND FREQUENCY STABILITY tests which the operator can select and perform are:

A - DOPPLER ACCURACY
B - RMS PHASE DEVIATION
C - FRACTIONAL FREQUENCY DEVIATION
D - ALLAN VARIANCE

With the introduction of the SLA, fast accurate statistical measurements of phase locked loop performance can be routinely made. From these measurements, the fundamental performance limitations can be identified and used at the system engineering level. For further information write LinCom Corporation, P.O. Box 2793D, Pasadena, CA, 91105 or call W. C. Lindsey, (213) 381-3701.

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*Vol. IV of this Final Report.