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New High-Efficiency Silicon Solar Cells

Final Report
August 11, 1983 - February 28, 1985

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Gerald T. Crotty
New High-Efficiency Silicon Solar Cells
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March 1, 1985

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The Solar Energy Research Institute
Through an Agreement with
National Aeronautics and Space Administration
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Pasadena, California
ABSTRACT

A new design for silicon solar cells was investigated as an approach to increasing the cell open-circuit voltage and efficiency for flat-plate terrestrial photovoltaic applications. This deviates from past designs for such applications, where either the entire front surface of the cell is covered by a planar junction or the surface is textured before junction formation, which results in an even greater (up to 70%) junction area. The heavily doped front region and the junction space charge region are potential areas of high recombination for generated and injected minority carriers.

The new design reduces junction area by spreading equidiameter dot junctions across the surface of the cell, spaced about a diffusion length or less from each other. Various dot diameters and spacings allowed variations in total junction area.

A simplified analysis was done to obtain a first-order design optimization. Efficiencies of up to 19% can be obtained.

Cell fabrication involved extra masking steps for selective junction diffusion, and made surface passivation a key element in obtaining good collection. It also involved photolithography, with line widths down to 5 μm.

A method is demonstrated for achieving potentially high open-circuit voltages and solar-cell efficiencies.
The objective of this program was to investigate a new design for silicon solar cells for flat-plate photovoltaic applications that features reduced junction area on the surface of the cell to reduce minority-carrier recombination and increase cell efficiency.

The innovative design consists of equidiameter dot junctions uniformly distributed over the cell surface, spaced about one diffusion length or less apart. In this design, therefore, the junctions cover only a small fraction of the total cell area. Studies of this design are motivated by prospects of reduction of reverse saturation current and increase of short-wavelength radiation absorption within the lightly-doped p-type base silicon rather than within the more heavily doped n⁺ region at the device surface.

The reduced saturation current helps to improve the open circuit voltage; effective surface passivation between the junction dots and proper design of junction configuration allows good collection efficiency. To understand the effects of reduced junction areas and to improve future solar-cell designs, the program was divided into the following tasks:

(1) Design of junction dot patterns
(2) Cell fabrication
(3) Cell characterization
(4) Modeling and correlation of results
ACKNOWLEDGMENTS

The authors acknowledge helpful discussions with O. von Roos. Assistance in spectral response measurements by B. Anspaugh is also acknowledged. The authors also thank K.M. Koliwad and A.D. Morrison for helpful suggestions and encouragement, and are grateful to J. Milstein of SERI for his advice. Secretarial help by M.J. Koop is also appreciated.

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SECTION I

INTRODUCTION

Since the advent of solar cells in 1954 (Reference 1), efforts to increase the efficiency of p-n junction silicon solar cells have continued. Research in materials and device technology (References 2, 3 and 4) has been responsible for better understanding of device physics and improvement in the performance of silicon solar cells.

Development in silicon growth technology has resulted in wafers with reduced dislocation densities and chemical impurities, and thus increased minority-carrier diffusion lengths (References 5 and 6). Research in p-n junction formation, surface preparation with multilayer antireflective (AR) coatings and back-surface reflection has helped in attaining more efficient light absorption. These have contributed to better short-circuit current.

Incorporation of a back-surface field (References 3 and 7) was one very successful design feature that effectively decreased dark current and thereby improved the open-circuit voltage, in addition to increasing the short-circuit current.

In parallel with this, metal-insulator semiconductor (MIS) solar cells (References 8 and 9) have been optimized for improved $V_{oc}$, but current collection has suffered considerably. In addition, long-term stability problems related to metallization, oxide charges and semiconductor surfaces have not been solved. Other approaches such as tandem cells (References 10, 11 and 12), etc., suffer from larger dark currents because of increased junction areas for the same cell area.

This program was directed toward reduction of junction area to reduce dark current and improve open-circuit voltage. It was divided into the following four tasks for understanding of the effects of junction-area reduction and for evaluation of more optimal cell design:

1. design of junction dot patterns
2. modeling
3. cell fabrication
4. cell characterization

These tasks are described following a brief description of theory. Discussions and conclusions are presented. A computer program written in BASIC, which was used in the modeling, is provided in Appendix A.

A similar effort with devices called point-contact solar cells has been made with thermal-photovoltaic cells (Reference 13) and concentrator cells (Reference 14).
A. OPEN-CIRCUIT VOLTAGE

A p-n junction silicon solar cell can be represented by a constant current generator in parallel with a diode. Ideally, a diode with only diffusion current, $I_d$, can be represented by the diode equation

\[ I_d = I_o[\exp(qV/nkT) - 1] \]  

or

\[ I_d = J_o \cdot A_j[\exp(qV/nkT - 1)] \]

where $I_d$ = reverse saturation current  
$J_o$ = reverse saturation current density  
$A_j$ = area of the p-n junction  
$q$ = electronic charge  
$V$ = applied voltage  
$n$ = diode ideality  
$k$ = Boltzmann constant  
$T$ = diode temperature, K

This ignores any series and shunt resistances and the space charge carrier recombination. The photogenerated current, $I_{sc}$, can be added algebraically to the diode current (Equation 1) to obtain the solar-cell output current as

\[ I = I_{sc} - J_o \cdot A_j \cdot [\exp(qV/nkT) - 1] \]  

If the total area of incident radiation on the solar cell is $A_T$, i.e., $I_{sc} = J_{sc} \cdot A_T$, then Equation 2 becomes

\[ I = J_{sc} \cdot A_T - J_o \cdot A_j[\exp(qV/nkT) - 1] \]

Under open-circuit conditions, $I = 0$ and $V = V_{oc}$ and hence, from Equation 3, the open-circuit voltage is given by
\[ V_{OC} = (nkT/q) \ln [(J_{sc} \cdot A_T/J_0 \cdot A_j) + 1] \] 

or

\[ V_{OC} = (nkT/q) \ln [J_{sc}/J_0(A_j/A_T)] + 1 \]

Thus, the ratio \( A_j/A_T \) can be changed to alter \( V_{OC} \). A plot of \( V_{OC} \) vs \( A_j/A_T \) is shown in Figure 2-1 for \( n = 1 \), where \( J_{sc} \) and \( J_0 \) are used as parameters with \( J_{sc} \) of 30 and 40 mA/cm\(^2\) and \( J_0 \) of 10\(^{-10}\), 10\(^{-11}\), and 10\(^{-12}\) A/cm\(^2\). It is seen that an order-of-magnitude reduction in the area ratio \( A_j/A_T \) results in a theoretical increase of about 60 mV in \( V_{OC} \). This may translate into an 8% to 10% increase in efficiency.

Figure 2-1. Open-Circuit Voltage vs Percentage Area Ratio
B. SHORT-CIRCUIT CURRENT

In a conventional p-n junction solar cell, most of the charge carriers generated in the bulk are shielded from front-surface effects by the shallow junction spread across the area of the cell. Also, the charge carriers generated within the heavily doped front region can be prevented from combining at the front surface if the surface is passivated. A recent study (Reference 15) shows that the blue response can be improved considerably by thermally grown thin oxide at the front surface.

In the design presented here, the junction covers only part of the front surface; the less junction area covered (as a fraction of the total area), the less separation of the bulk from the surface by the junction. Thus, most of the photogenerated carriers may not be prevented from reaching the surface. In this case, the surface must be well passivated to enable all the generated carriers to reach the junction. Similarly, the small area junctions must be judiciously spread to within at least a diffusion length of the minority carriers in the base.

Small-area junctions afford another advantage in terms of the current-flow pattern. In conventional cells, the current flow in the diffused region is lateral within the depth of the junction, which is only a fraction of a μm, whereas in dot junctions the flow is nearly perpendicular to junction surface; this is likely to result in lower series resistance.

The value of the short-circuit current will depend on minority-carrier diffusion length, junction spacing, cell thickness, and design of junctions on the cell surface. A variety of junction designs were considered, and are described in Section III.
SECTION III
DESIGN OF MASKS

For thermal diffusion on selective areas of the cell, an etched-out pattern on oxide was thought to be the easiest and most conventional way. For this, a photolithography step was necessary. Three patterns were considered.

A. CONCENTRIC RINGS

This pattern consists of concentric rings spreading out from the center of the cell with increasing radii, such that the radial distance between two consecutive ring edges is of the order of two diffusion lengths or less. The metal grid and annular diffusion patterns are shown in Figure 3-1. It was clear from this design that the metal grid must run along both the base and the diffused areas of the cell and another mask with an intricate pattern will be needed to open up windows in the oxide for metal contact in areas where the grid pattern crosses the rings. With increasing ring diameter, a slight misalignment in the mask would result in either no contact with the diffused region or a shorting of a p-n junction. Further, for larger-diameter rings, a short at one place would short out a fairly large area of the junction. Because of these complications, this design was discarded.

B. PARALLEL-JUNCTION PATTERN

Figure 3-2 shows a design in which a junction is formed with all grid lines and the bus bar on the diffused area, and most of the uncovered area of the cell having no junction. The distance between two consecutive grids would be 200 to 300 µm, which is of the order of two diffusion lengths. In general, the junction area $A_j$ would be about 3% to 8%. No metal would run over a non-diffused area, thus avoiding any chance of junction shorting. This approach has been tried (Reference 16) using aluminum as a dopant for a p'n device. The results were not encouraging. In this design, the junction-area distribution is not uniform; hence, for the same area, the collection of current is less efficient. However, grid pattern alignment is easier, with less chance of junction shorting in case of a processing error.

C. DOT COLLECTORS

A very efficient scheme is to form equidiameter current-collecting dot junctions spaced 100 to 200 µm apart on the cell surface, staggered in alternate columns with grid lines connecting the dots along each column. Different dot diameters give different ratios of junction area to total area $A_j/A_T$ (Figure 3-3). As an example, 25-µm-dia (d) junctions spaced such that the vertical and horizontal spacings $S = 100$ µm will give an area coverage in percentage: $(A_j/A_T) = (\pi/8) \times (d/S)^2 = 2.5\%$.

As in the ring design, the metal grid will run on areas both with and without diffusion. However, because of their symmetrical nature, similar dot
Figure 3-1. Concentric Ring Pattern
Figure 3-2. Parallel Junction Pattern

Figure 3-3. Dot-Collector Pattern
patterns with smaller dot sizes can be used to open windows in oxide for metal-grid contacts on the diffused region only. The remaining oxide acts as a barrier between the silicon surface and the metal grid.

This pattern has the advantage of easily enabling variation in area coverage and offers very efficient current collection for a given area coverage. This pattern was selected for experimentation.

A set of junction mask designs were worked out for \( S = 200 \, \mu\text{m} \) and \( 100 \, \mu\text{m} \) with \( d \) varying from \( 15 \, \mu\text{m} \) to \( 100 \, \mu\text{m} \), to obtain area coverage varying from 1% to 20%. A suitable set of designs for metal grids was also chosen. Parameters of these sets are shown in Table 3-1, with the percentages of area coverage.

The metal grid mask design along with percentage of area shadowing is given, with \( W \) as the width of each grid finger. A line width of \( 5 \, \mu\text{m} \) was considered difficult to obtain at the time; it was thought that it might be necessary to accept higher shadowing losses until the photolithography for finer line widths was in place.

<table>
<thead>
<tr>
<th>Set No.</th>
<th>( S, \mu\text{m} )</th>
<th>( d, \mu\text{m} )</th>
<th>( A_j/A_T, % )</th>
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<td>15</td>
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<td>100</td>
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<table>
<thead>
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<th>( W, \mu\text{m} )</th>
<th>Shadow, %</th>
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<tr>
<td>4</td>
<td>200</td>
<td>20</td>
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</table>
The solar-cell design calls for a three-dimensional code to solve for the cell parameters. This is a time-intensive and costly process. Therefore, it was decided to seek a simpler, two-dimensional solution.

As an initial attempt, the cell was divided into a number of unit subcells (see Figure 4-1a), each with a square collecting junction at its center. It was then modeled as a semi-infinite surface with surface recombination velocity of either infinity or zero. After analysis it was concluded that this was not workable, because of the divergence of the dark current when assuming abruptly changing boundary conditions at the edges of the square collecting junctions. This led to an independent investigation of the origin of this divergence (Reference 17). However, this approach was abandoned for solar-cell modeling.

Another approach was to assume a zero surface recombination velocity and an exponential bulk recombination decrease. This model is described below:

Consider a square unit subcell with a dot junction of diameter d in the center of its surface, with each side of the subcell equal to S. The height, Zt, is the thickness of the cell (Figure 4-1b). This unit subcell is divided into two volumes, I and II; I is the cylinder of diameter d with the junction at the front surface, and II is the remaining volume of the unit subcell (Figure 4-1c).

The number of photons, Nph, incident on the surface will generate electron-hole pairs, in accordance with Lambert's law, throughout the volume of the unit subcell. The number of electron-hole pairs collected by the junction will depend exponentially on the distance of the generation point from the junction.

For volume I, this distance equals the depth of the generation point; for volume II, the distance is the square root of the sum of squares of the horizontal (r) and vertical (z) distances. For volume II, up to a diameter S, the differential surface area consists of a ring of width dr with r varying from d/2 to S/2. For r from S/2 to S\sqrt{2}, the differential surface area consists of a truncated annular ring of width dr and circular arc of length 2r - 8r arc cos (S/(2r)).

For bulk diffusion length of Lb, the current collection in volume I will be proportional to exp(-z/Lb) and in volume II it will be proportional to exp(-SQRT(r^2 + z^2)/Lb). The short-circuit current density is therefore written as:
Figure 4-1a. Unit Subcells With Square Junctions

Figure 4-1b. One Unit Subcell With a Dot Collector Junction
Figure 4-1c. Two Volumes, I and II, of the Unit Subcell With Carrier Collection Distances and Calculations for the Truncated Rings
$$J_{sc} = \frac{1}{S^2} \left\{ q \int_0^{\alpha N_{ph}} e^{-\alpha z} \, dz \left[ \frac{md^2}{4} e^{-z/L_b} + \int_{d/2}^{S/2} 2\pi r dr e^{-\left[(r-d/2)^2 + z^2\right]^{1/2}/L_b} \right] \right\}$$

$$+ \int_{S/2}^{S/\sqrt{2}} \left[ 2\pi r - 8\cos^{-1}(S/2r) \right] e^{-\sqrt{(r^2 + z^2)/L_b}} dr \right\}$$

(5)

where \( \alpha = \) optical absorption coefficient in silicon

\( N_{ph} = \) number of photons incident per cm\(^2\)-sec-\(\mu\)m

\( Z_t = \) thickness of the cell

The I-V curve is obtained from the equation

$$J = J_{sc} - J_o \left( e^{qV/kT} - 1 \right)$$

(6)

where \( V = \) output voltage

\( J_o = \) reverse saturation current density

\[ = \left( \frac{q n_i^2}{N_A} \right) \cdot \left( \frac{D_n/L_b}{\pi d^2/4S^2} \right) \]

and \( J = \) output current density.

A plot of \( J_{sc} \) vs junction diameter \( d \) for \( S = 50, 100, 150 \) and 200 \( \mu \)m and for \( L_b = 100 \) and 300 m is given in Figure 4-2.

Cell parameters of \( V_{oc}, J_{sc}, FF \) and efficiency at 100 mW/cm\(^2\) for \( L_b = 100, 200, \) and 300 \( \mu \)m and with \( N_A = 1 \times 10^{17} \) per cm\(^3\), and \( D_n = 15 \) cm\(^2\)/sec are shown in Table 4-1. It is interesting to note that for 100 \( \mu \)m and 200 \( \mu \)m diffusion lengths, a \( d/S \) of 25/50 offers highest efficiency; for 300 \( \mu \)m diffusion-length material, a \( d/S \) of 25/100 is best. Thus for good material, lesser junction-area coverage is beneficial.
Figure 4-2. Calculated Short-Circuit Current Density for Different Dot Collector Designs and Bulk Diffusion Lengths
## Table 4-1. Calculated Solar-Cell Parameters for Different Dot-Collector Designs

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<th>Lb, µm</th>
<th>S, µm</th>
<th>d, µm</th>
<th>V&lt;sub&gt;oc&lt;/sub&gt;, mV</th>
<th>J&lt;sub&gt;sc&lt;/sub&gt;, mA/cm&lt;sup&gt;2&lt;/sup&gt;</th>
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<td>d, µm</td>
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SECTION V
EXPERIMENTS AND TESTING

Solar-cell fabrication was done on 3-in.-dia, (100) orientation, 1 to 2 Ohm-cm, 0.3 to 0.4 mm (12 to 16 mils)-thick Czochralski (Cz) or float-zone (FZ) wafers using masks to obtain four 2 x 2-cm cells per wafer. The general processing steps needed (see Figure 5-1) were:

(a) Oxidation of front and back surface, 3000 to 4000 Å thick, to act as a diffusion mask.

(b) Etching windows on front surface with photolithography, followed by phosphorus diffusion at 850°C for 20 min. with PH3.

(c) Etching of oxide and phosphosilicate glass using 10% to 20% HF solution.

(d) Thermal oxidation, 100 to 150 Å thick, on the front surface to passivate the cell surface and form an insulation layer on the p substrate to avoid shorting by metallization, and yet etch windows for contact with the diffused regions.

(e) Back metallization by evaporation of Al-Ti-Pd-Ag (600-600-400-25K Å) and sintering at 600°C in H2; front metallization and lift-off by evaporation of Ti-Pd-Ag (600-400-40K Å).

(f) Single or multilayer AR coating for good photon absorption. Single layer is 725 Å SiO2 and multilayer consists of TiO2 and Al2O3 sputtered and sintered at 400°C for 20 min.

A number of runs of cells were made with minor changes in the processing steps as described.

Before receipt of the masks, a preliminary run with a larger-area dot mask was done. A batch of p-type Cz wafers were thermally diffused and mesa-etched to form a dot pattern. A 50% reduction in area reduced the cell efficiency (with no AR coating) from 8.9% to 3.6% (100 mW/cm²). A slight improvement was noticed after growth of a thin oxide at 200°C (Table 5-1). Junction area after etching was reduced from 4 cm² to 2.14 cm².

After receipt of the masks, the first two runs could not be completed because of problems with photo-resists and mask aligner. Proper delineation of dot junctions and grid metal could not be achieved, resulting in aborted cells.

The next run was made to study the fabrication and testing of 100-μm-dia and 50-μm-dia junctions only. Wet oxidation for diffusion masking was done at 1100°C for 1 h.

Dark I-V measurements were made on representative junctions over an area of 4 x 4 cm. It was found that, in general, the diode factor degraded with smaller junctions: about 1:35 to 1:40 for 100-μm-dia junctions and about 1:38 to 1:44 for 50-μm-dia junctions. A typical dark I-V curve is shown in Figure 5-2.
Figure 5-1. Schematic of Solar-Cell Fabrication

(a) Si SUBSTRATE (P) with SiO$_2$
(b) n$^+$ DIFFUSION
(c) n$^+$ DIFFUSION
(d) SiO$_2$
(e) METAL GRID
(f) AR COATING
Table 5-1. Mesa-Etched Solar Cells

<table>
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<tr>
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<th>Before Etch</th>
<th>After Etch</th>
<th>After Oxidation</th>
</tr>
</thead>
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<td>$V_{oc}$</td>
<td>564 mV</td>
<td>527 mV</td>
<td>557 mV</td>
</tr>
<tr>
<td>$I_{sc}$</td>
<td>86.2 mA</td>
<td>38 mA</td>
<td>40 mA</td>
</tr>
<tr>
<td>FF</td>
<td>73%</td>
<td>71%</td>
<td>73%</td>
</tr>
<tr>
<td>$\eta \text{ (No AR Coat)}$</td>
<td>8.9%</td>
<td>3.6%</td>
<td>4.1%</td>
</tr>
</tbody>
</table>

Junction area after etch: 2.14 cm$^2$
Junction area before etch: 4 cm$^2$
Oxide: $\approx$20 Å SiO$_2$ at 200°C

for a 100-μm-dia junction. This fabrication run involved a high-temperature (1100°C, 1 h) oxidation step, which may have not only caused degradation of bulk lifetime but also a depletion of boron at the front-surface p region. A discussion of this effect is presented in Section VI.

To avoid high-temperature oxidation and yet provide a diffusion mask, experiments with different evaporated films of oxides (SiO$_x$, InO, Ta$_2$O$_5$) were tried. Indium oxide and tantalum pentoxide films were strongly adherent and did not etch out properly after the photolithography step. Silicon oxide evaporation with substrate heated at about 200°C in the presence of oxygen resulted in the formation of (probably) Si$_2$O$_3$, which was found to be conducive to subsequent etching and thermal diffusion.

A run with evaporated silicon oxide was made on 1 to 2 Ω-cm, (100), 0.375 mm (15 mils)-thick, 76 mm (3 in.)-dia FZ wafers, using masks with 200-μm dot spacings (S) and dot diameter of 100 μm (referred to hereinafter as 200-100) and with spacing of 100 μm and dot diameters of 75 and 50 μm (100-75 and 100-50), respectively.

After cleaning of the wafers, evaporation of silicon oxide and opening of windows through the oxide, thermal diffusion of phosphorus was done at 850°C to obtain a sheet resistivity of 100 Ω/□. A passivating oxide (40 to 46 Å) was grown at 800°C for 30 min. followed by 15 min. annealing in nitrogen. Alignment for the front metallization on thin oxide, as well as after Ta$_2$O$_5$ AR coating, did not succeed. A third try to align, by indexing on two side edges, was finally successful. Ten 2 x 2-cm cells with dot collectors were fabricated. Figure 5-3 shows photomicrographs of two cells. The cell in Figure 5-3a is 200-50 configuration with 20-μm-wide metal grids, and the cell in Figure 5-3b is a 100-75 configuration with 10-μm-wide grids. Following this experience, a revision of the mask design for smaller-cell geometry with better registration marks and finer grid-line geometry. In addition, four 2 x 2-cm control cells were fabricated with conventional junctions and with the finer grid pattern used for dot-collector cells.

These cells were tested for light and dark I-V characteristics. It was found that the reverse saturation current density was very high ($\approx$1 to 2 x 10$^{-8}$

5-3
$n = 1.38$

$J_0 = 4 \times 10^{-8} \text{ A/cm}^2$

Figure 5-2. Dark I-V Characteristics of 100-$\mu$m-Dia Dot Junction
A/cm²) and the light-generated current collection was very low (Table 5-2). The last column shows a calculated $V_{oc}$ for cell-current collection of the order of 120 mA. Part of the current-collection degradation can be accounted for by greater grid widths due to undercutting during the etching of the oxide. It is estimated that the metal coverage was of the order of 12.5% on these cells. Figure 5-4 shows dark I-V characteristics of typical cells from each set. Spectral response measurement (Figure 5-5) with and without bias show the presence of trap levels. Surface photovoltage (SPV) measurement showed a degradation minority carrier diffusion length from 150 to 200 µm in untreated wafers to less than 40 µm in the cells. This degradation is attributed traced to the $SiO_x$ evaporation step and, therefore, to the $SiO_x$ purity. High-temperature diffusion following the $SiO_x$ evaporation may have incorporated those impurities within the Si.

The next run was done on 1 Ω-cm FZ wafers with a deposited oxide (using a low-temperature CVD system, by courtesy of Applied Solar Energy Corp.) as a diffusion barrier. Similar process steps were followed with a passivating oxide of 150 Å thickness, 10 and 15 µm-wide metal fingers (Ti-Pd-Ag), and a double AR coating. Light and dark I-V tests were performed. Table 5-3 gives the solar-cell parameters. The best efficiency obtained was 14.3% for a 75-µm-dia dot collector and 100-µm junction spacing configuration. It was interesting to note that the 200-100 cells gave approximately the same current collection as did the 100-75 cells. A retest after two days of storage showed considerable degradation in cell parameters, as shown in Table 5-3 by figures in parenthesis. Spectral response measurement showed light bias effect similar to that shown in Figure 5-5. Higher quantum efficiency at longer wavelengths with bias cannot be explained by oxide traps alone. Capacitance-voltage (C-V) measurements of oxide showed a flat-band shift of -1.45 volts (see Figure 5-6).
Table 5-2. Summary of Dot-Collector Cell Results

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<th>Set No.</th>
<th>Cell No.</th>
<th>$V_{OC}$, mV</th>
<th>$I_{SC}$, mA</th>
<th>FF</th>
<th>$\eta%$</th>
<th>$I_0$, A</th>
<th>$V_{OC}$, mV, for $I_{SC} = 120$ mA</th>
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<td>105</td>
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<td>11.9</td>
<td>2.6 x 10^{-8}</td>
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with an oxide interface state density of $10^{12}$/cm$^2$, as against values of -1.1 volts and $\approx10^{11}$/cm$^2$, respectively, for good oxide.

The degradation in the cell performance is presumed to be due to changes in the oxide properties. Further work in understanding of thin oxides for surface passivation must be done to explore the full potential of this cell design.
Figure 5-4. Dark I-V Curves for Dot Collector and Control (C-1) Cells
Figure 5-5. Spectral Response of Cell 100-75 With and Without Bias Light
Table 5-3. Summary of Solar-Cell Results
(1.5 Ω-cm FZ Substrates)

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Figure 5-6. Capacitance-Voltage Measurements for Passivating Oxide
The modeling calculations show that smaller spacing with proper dot-junction areas give improved cell performance. Thus, a potential has been demonstrated for achieving high efficiency with these cells.

Fabrication experiments during the later part of this program were fruitful in demonstrating the feasibility of this approach and also in pointing out some of the design and fabrication pitfalls.

One of the problems faced during fabrication was that the registration marks on the masks were too far apart, leading to difficulties in alignment.

High-temperature wet-oxide growth on p-type substrates introduces an extra high-temperature step that reduces the diffusion length. In addition, with the p-type silicon/SiO₂ interface, it is known that due to redistribution, boron tends to escape into SiO₂ at high temperature (References 18 and 19), leading to a depleted region along the surface surrounding the junction. This tends to increase surface leakage along the p-type surface and to space-charge recombination in the depleted subsurface regions surrounding the dot junctions. Low-temperature-CVD-deposited oxide has solved this problem.

Dark I-V data (Figure 5-4) shows that a conventional junction gives a much better diode ideality factor than is obtained by the dot collectors. A comparison of dark I-V data from the last run is shown in Figure 6-1. The improvement in the characteristics with reduction in junction area is clear. However, the diode ideality factor was found to be 1.2 to 1.25, which is high. In addition, the cell results show considerable shorting, probably due to metal grids running over p regions with a thin (150 Å) oxide. A high series resistance was also noted. These problems led to the degradation of cell performance shown in Table 5-3. A closer look at the metal grid design or suitable alteration in the fabrication procedure may be needed.

More work is needed in theoretical analysis to further optimize the design and determine limits to cell performance. Passivation of front surfaces is important; more research in thin-oxide growth and characterization is needed to arrive at optimum thickness and fabrication procedure. More cell fabrication runs with design variations are also needed to improve performance and to understand the limiting loss mechanisms.

In summary, this work has shown that the dot-junction design has good potential for improving cell efficiency and also that work in key areas of theoretical analysis, oxide passivation and cell fabrication is required.
Figure 6-1. Dark I-V Characteristics of Dot Collector Solar Cells
REFERENCES


APPENDIX A

COMPUTER PROGRAM FOR SOLAR-CELL MODELING

100 REM ********************
110 REM *  DOT COLLECTOR Solar Cell Modeling  *
120 REM *  DATE 12-26-84  *
130 REM *  *
140 REM *
150 REM ********************
160 REM PRINT @37,26:0
180 NEXT I
190 INIT
200 N=124
210 Y=150
220 DIM W1(N),Eph(N),A1(N),A(2),C(2),E0(3),E1(3),F9(N),M1(N),P(2)
230 DIM Nph(N),W2(N),Vo(Y),Io(Y),Po(Y)
240 T=300
250 Zt=0.03
260 READ Q,Qi,H1,C0,Vt
270 REM -----------------------------------
280 REM READ AM 1.5 GLOBAL DATA FROM FILE i
290 REM *******************
300 FIND i
310 FOR I=1 TO N
320 INPUT @33:W1(I),Eph(I)
330 NEXT I
340 REM ---------------------------------------
350 REM CALCULATE ABSORPTION COEFFICIENT, ALPHA
360 REM *******************
370 READ B2,G1,C(i),A(2),A(2),A4,K0,E0(i),E0(2),E0(3)
380 READ F(i),P(2),H2
390 FOR I=1 TO 3
400 E1(I)=E0(I)-B2*T^2/(T+G1)
410 NEXT I
420 FOR K=1 TO N
430 F9(K)=1.239644/W1(K)
440 A1(K)=0
450 FOR I=1 TO 2
460 FOR J=1 TO 2
470 M1(K)=0
480 IF F9(K)<E1(J)+P(I) THEN 530
490 M1(K)=C(I)*A(J)*(F9(K)-E1(J)+P(I))^2/(EXP(P(I)/(K0*T))-1)
500 IF F9(K)<E1(J)+P(I) THEN 530
510 ZI=C(I)*A(J)*(F9(K)-E1(J)+P(I))^2/(1-EXP(-P(I)/(K0*T)))
520 M1(K)=M1(K)+ZI
530 A1(K)=A1(K)+M1(K)
540 NEXT J
550 NEXT I
560 IF F9(K)>E1(3) THEN 580

A-1
570  GO TO 600
580  M1(K)=A4*(F9(K)-E1(3))^0.5
590  A1(K)=A1(K)+M1(K)
600  NEXT K
610  DATA 32,1.601864E-17,6.623773E-34,2.979022E+10,0.02586
620  DATA 7.021E-4,1108,5.5,4,323.1,7237,1052000,8.616E-5,1.1557,2.5
630  DATA 3.2,0.01827,0.05773,6.582E-16
640  REM  --------------------------------------
650  REM  --------------------------------------
660  REM  --------------------------------------
670  IF Q=32 THEN 690
680  PRINT #37,26:1
690  DR=2.5E-4
700  N1=100
710  N2=60
720  N3=74
730  Lb=0.01
740  PRINT " Lb  S  D  Voc  Jsc  FF  Eff1"
750  FOR N4=1 TO 3
760   S=0.005
770   FOR Li=1 TO 4
780     Si=8*10000
790     PRINT " USING 2280: Lb=10000, S1"
800   R1=0.00025
810   FOR M2=1 TO 8
820     D=2*R1*10000
830     C6=0
840     C3=0
850     FOR I=1 TO N3
860       Z2=0
870       U=0
880       IF A1(I)>1000000 THEN 980
890       IF A1(I)>400000 THEN 1000
900       IF A1(I)>100000 THEN 1020
910       IF A1(I)>40000 THEN 1040
920       IF A1(I)>10000 THEN 1060
930       IF A1(I)>4000 THEN 1080
940       IF A1(I)>1000 THEN 1100
950       IF A1(I)>100 THEN 1120
960       Dz=0.005
970       GO TO 1130
980       Dz=5.0E-8
990       GO TO 1130
1000      Dz=1.0E-7
1010      GO TO 1130
1020      Dz=5.0E-7
1030      GO TO 1130
1040      Dz=1.0E-6
1050      GO TO 1130
1060      Dz=5.0E-6
1070      GO TO 1130
1080      Dz=1.0E-5
1090      GO TO 1130
1100      Dz=0.0E-5

A-2
GO TO 1130

Dz=1.0E-4

IF I>1 THEN 1160

W2(I)=0.0032

GO TO 1170

W2(I)=W1(I)-W1(I-1)

Nph(I)=W1(I)*1.0E-8*A1(I)*Eph(I)*W2(I)/(H1*C0)

FOR J=1 TO N1

R=R1

Az=A1(I)*Z2+Dz/2)

C8=0

IF Az>100 THEN 1680

FOR K=1 TO N2

IF R=(S/2 THEN 1270

C2=B*(R+Dr/2)*ACS(S/(2*(R+Dr/2)))

GO TO 1280

C2=0

C9=(2*PI*(R+Dr/2)-C2)*Dr*EXP(-SQRT((R+Dr/2-R1)^2+(Z2+Dz/2)^2)/Lb)

C8=C8+C9

R=R+Dr

IF R=(S/2^0.5 THEN 1330

NEXT K

Dt=PI*R1^2*EXP(-(Z2+Dz/2)/Lb)

Ex=EXP(-Az)

C7=Nph(I)*Ex*Dr

C6=C6+C7*(Dt+C8)

IF U=1 THEN 1410

IF Az<0.5 THEN 1650

U=1

Dz=Dz*2

IF U=2 THEN 1450

IF Az=1 THEN 1650

U=2

Dz=Dz*2

IF U=3 THEN 1490

IF Az=2 THEN 1650

U=3

Dz=Dz*2

IF U=4 THEN 1530

IF Az=4 THEN 1650

U=4

Dz=Dz*4

IF U=5 THEN 1570

IF Az=10 THEN 1650

U=5

Dz=Dz*4

IF U=6 THEN 1610

IF Az=20 THEN 1650

U=6

Dz=Dz*10

IF U=7 THEN 1650

IF Az=40 THEN 1650

U=7
Dz=10*Dz
Z2=Z2+Dz
IF Z2>=Zt THEN 1680
    NEXT J
   NEXT I
C1=Q1*C6*1000/S^2
GOSUB 1010
R1=R1+0.00125
IF S<2*R1 THEN 1740
NEXT M2
S=S+0.005
NEXT L1
Lb=Lb+0.01
NEXT N4
PRINT @37,26:0
PRINT """"""""ALL DONEGGGGG"
1800 END
1810 REM ----------------------------------------
1820 REM CALCULATIONS FOR Voc, FF, AND EFFICIENCY
1830 REM """"""""#####*################################*#
1840 Z=0
1850 Isc=C1/1000
1860 Num=PI*1.6E-19*1.45E+10^2*15
1870 Den=4*1.5E+16*Lb
1880 Rev1=Num/Den*(D/S1)^2
1890 FOR IO=1 TO 20
1900    Vo(IO)=IO*0.05
1910    Io(IO)=Isc-Revi*(EXP(Vo(IO)/Vt)-1)
1920    IF Z=1 THEN 2080
1930    Po(IO)=Vo(IO)*Io(IO)
1940    IF 10=i THEN 2080
1950    IF Po(IO)>Po(IO-1) THEN 2080
1960    FOR L=1 TO 12
1970        M=IO+L-1
1980        Vo(M)=Vo(M-1)+0.005
1990        Io(M)=Isc-Revi*(EXP(Vo(M)/Vt)-1)
2000        Po(M)=Vo(M)*Io(M)
2010        IF Po(M)>Po(M-1) THEN 2060
2020        Zm=Po(M-1)
2030        Z=1
2040        REM
2050        GO TO 2080
2060        REM
2070    NEXT L
2080    IF Io(IO)<0 THEN 2120
2090    REM
2100    NEXT IO
2110 END
2120 FOR K=1 TO 100
2130   J=IO+K-2
2140   Vo(J)=Vo(IO-1)+(K-1)*.0E-3
2150   Io(J)=Isc-Revi*(EXP(Vo(J)/Vt)-1)
2160   IF Io(J)<0 THEN 2210
2170   REM
2180 NEXT K
2190 END
2200 REM FUZZ S,9.0E-4
2210 FOR K=1 TO 100
2220   J=IO+K-2
2230   Vo(J)=Vo(IO-1)+(K-1)*.0E-3
2240   Io(J)=Isc-Revi*(EXP(Vo(J)/Vt)-1)
2250   IF Io(J)<0 THEN 2210
2260   REM
2270 NEXT K
2280 END
2160 NEXT K
2170 PRINT "J
Voc NOT FOUND"
2180 RETURN
2190 Voc=Vo(J)
2200 Ff=Pm/(Voc*Isc)
2210 Eff=Pm*1000
2220 Jsc=Isc*1000
2230 PRINT @Q: USING D,Voc,Jsc,Ff,Eff
2240 RETURN
2250 IMAGE 12X,3D,2X,3D,2X,3D,2X,3D,2X,2D,2D
2260 IMAGE 2X,3D,2X,3D