OVERVIEW OF PROCESSING ACTIVITIES AIMED AT HIGHER EFFICIENCIES AND ECONOMICAL PRODUCTION

JET PROPULSION LABORATORY

D.B. Bickler

Outline

• Background
• Process development concerns
• High efficiency elements
• Sensitivities
• A proposed design
• Process development for proposed design

Background

• Historically, JPL process development dealt with minimizing $/watt
• Current focus on achieving cell efficiencies greater than 18%

Process Development Concerns

• Less than optimum Si sheet
• Control of yield
• Large area cells
High-Efficiency Elements Requiring Process Development

- Bulk material perfection
- Very shallow junction
- Front surface passivation
- Finely detailed metallization

Bulk Material Perfection

- Maintain minority carrier lifetime
- High doping levels add concern
- Large area

Very Shallow Junction

- Sensitive to metallization punch-through
- Series resistance problems
- Control dopant leaching during passivation

Front-Surface Passivation

- Mechanical integrity
- Optical characteristics
- Electrical requirements
- Process selection
  - Thermal oxidation
  - Thermal CVD
  - Plasma CVD
  - Sputtering
  - Evaporation
PLENARY SESSIONS

Finely Detailed Metalization

- Aspect ratio (thickness/width)
- Laser processing
- Electrochemical deposition

Determining Sensitivity to Processing

- Use of mathematical modeling
  - Cell model SPCOLAY from University of Pennsylvania
  - Metal pattern optimization CELCAL from JPL
  - Processing models in SUPREM from Stanford University

- Experimental lab work
  - Individual process steps
  - Combine into process sequences
Power Loss vs Cell Size

Plot showing the relationship between POWER LOSS (mW/cm²) and CELL SIZE (cm). The graph compares the power loss for NOT STRAPPED and STRAPPED conditions.
Low-Resistivity Cell Behavior

A Proposed High-Efficiency Design
PLenary sessions

Process Development Required for Proposed Design

- Thinning process
- BSR optics
- Patterned doped silicon
- Metal grid alignment