AMORPHOUS-SILICON MODULE HOT-SPOT TESTING

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Background

- Hot-spot heating occurs when cell short-circuit current is lower than string operating current
  - Cell goes into reverse bias and absorbs power
    \( = \text{reverse-bias voltage} \times \text{cell current} \)
  - Reverse-bias voltage is proportional to the number of cells in series with the affected cell
  - It is necessary to limit reverse-bias voltage by means of bypass diodes

- Nonuniform heating over cell area leads to increased temperature for same power dissipation

Visualization of Hot-Spot Cell Heating with High-Shunt Resistance Cell
Visualization of Hot-Spot Cell Heating with Low-Shunt Resistance Cell

Key Lessons from Crystalline Silicon

- Maximum allowable temperature for encapsulants: 120°C to 140°C
- Temperature very dependent on cell-to-cell shunt-resistance differences
- Lateral heat transfer from hot spot is important
- Common failure at high heat levels is cell shorting
- Typical crystalline-silicon module requires bypass diodes around every 12 to 18 cells
- Heating is highly non-linear function of applied current and voltage
  - Non-linear reverse I-V characteristic
  - Changing shunt-resistance with temperature
  - Changing hot-spot area with temperature
Amorphous-Cell Hot-Spot Testing Objectives

- To develop the techniques required for performing reverse-bias testing of amorphous cells
- To quantify the response of amorphous cells to reverse biasing
- To develop guidelines for reducing hot-spot susceptibility of amorphous modules
- To develop a qualification test for hot-spot testing of amorphous modules

Approach

- Amorphous cells tested using two techniques
  - First is equivalent to that used in hot-spot testing of crystalline cells
    - Hot-spot temperature monitored using IR camera
    - Reverse-bias I-V curve plotted as test is conducted
  - Second consists of pulsed reverse-bias voltage ranging in duration from 0.01 to 100 milliseconds
    - I-V curve plotted after each pulse

Amorphous-Cell Second-Quadrant I-V Curves
Amorphous-Module Cell-Reverse Quadrant I-V Curves
Illuminated Cells

Amorphous-Module Cell-Reverse Quadrant I-V Curves
Unilluminated Cells
Fraction of Cells Reaching a Given Temperature as a Function of Power Dissipated

(Modules)

Fraction of Cells Reaching a Given Temperature as a Function of Power Dissipated

(Submodules)
Hot-Spot Temperature Versus Power for Cells in Encapsulated Module
(Test Current Equal to 1, 2, and 2 + Cell $I_{SC}$)

Hot-Spot Temperature Versus Power
(Unencapsulated Amorphous-Silicon Submodules, No Illumination)
Hot-Spot Qualification Test

- Hot-spot qualification test performed on one module type
- Same procedure and equipment as for crystalline cells
  - 100-hour cyclic test
  - Treated as low-shunt-resistance cell (Type B)
    - Test performed in absence of illumination
    - Test current is module short-circuit current
  - Module temperature raised to field environment (45°C to 50°C)

Results and Conclusions

- Amorphous cells undergo hot-spot heating similarly to crystalline cells
  - Shunt resistance levels similar
  - Tolerance to heating level similar
- Comparison of results obtained with submodules versus actual module indicate heating level lower in latter
  - Module structure contains thick (relative to front surface) glass substrate not present in submodules
- Module design must address hot-spot heating
  - Heat-sinking cells
  - Use of bypass diodes
  - Use of smaller solar cells (lower maximum current)
- Hot-spot qualification test conducted on module
  - Module passed test with no instabilities
  - Minor cell erosion occurred that is characteristic of amorphous cells
Hot-Spot Test Set-Up

Test Set-Up for Submodule Using Conductive Elastomeric Material
Results of Hot-Spot Testing of Four Submodules

Close-up View of Hot-Spot Area
Module Development and Engineering Sciences

Front Side of Arco Test Module

Back Side of Arco Test Module Showing Added Conductive Ribbon Attached with Conductive Epoxy
Close-up of Arco Test Module Showing Results of Hot-Spot Testing

Hot-Spot Recorded on IR Monitor Using Time-Lapse Photography
Ocilloscope Trace of Pulse-Reverse Bias Testing

>5V

-500µs

+500mV

50V

1V/div. #18

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