Supercomputing on Massively Parallel Bit-Serial Architectures

Consider the idea that supercomputing is a synergy of generic algorithms, languages and architectures and that real breakthroughs in parallel computing will be achieved by considering all three together in a simulated software environment. Engineering tradeoffs could be made between performance, machine transparency, standardization and program portability before any new machines are actually built. Standardized languages could be developed for generic subclasses of parallel machines; languages that really give high performance and encourage free parallel expression and "thinking in parallel".

My own research on the Goodyear MPP (Massively Parallel Processor), suggests that high-level parallel languages are practical and can be designed with powerful new semantics that allow algorithms to be efficiently mapped to the real machines. For the MPP these semantics include parallel/associative array selection for both dense and sparse matrices, variable precision arithmetic to trade accuracy for speed, micro-pipelined "train" broadcast, and conditional branching at the PE control unit level.

The preliminary design of a FORTRAN-like parallel language for the MPP has been completed and is being used to write programs to perform sparse matrix array selection, min/max search, matrix multiplication, Gaussian elimination on single bit arrays and other generic algorithms. The MPP timing estimate for Gaussian elimination of a 4K by 4K single bit matrix is under one second -- the equivalent of approximately 64 billion scalar operations. Parallel Gauss-Jordan matrix inversion is also being investigated. The estimated time to invert a 128 x 128, 32 bit real matrix using full pivoting on the MPP is 50 msec. This is roughly equivalent to a 100 MFLOP scalar rate.

The MPP is a SIMD machine of 16384 single bit processors arranged in a 128 x 128 array. Individual PE's are interconnected with their four nearest neighbors. Each PE can address 1024 bits of its own local memory. A 32 bit shift register in each PE allows for micro-pipelining of long words and faster partial sum accumulation for multiplication. The machine can execute 160 billion micro-instructions per second which translates to 800 GOPS for some instructions. Operations include single bit logical, shift, and add as well as column I/O and one or two dimensional routing in a spiral, cylinder, or torus. All operations can be directly or indirectly masked. The logical "or" of one bit per PE (SUMOR) can be used to pass array information back to the PE control unit for broadcast to other PE's, scalar I/O or conditional branching. If a second MPP were ever built, it might look considerably different than the current MPP. For example, it would certainly have greater memory depth -- at least 64K bits per PE. It might also have a reconfigurable bit/byte serial ALU, staged PE's for table lookup arithmetic, and pipelined SUMOR logic.

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4/15/85
SUPERCOMPUTING ON MASSIVELY PARALLEL BIT-Serial ARCHITECTURES

- Supercomputing Domain
- New Dimensions in Parallel Computing
- Some Generic Algorithms
- The Goodyear MPP
- Some MPP Specific Algorithms Coded in a Fortran-Like Bit-Serial Programming Language
- What Might a Second Generation MPP Look Like?
SUPERCOMPUTING DOMAIN

PARALLEL PROGRAMS

ALGORITHMS

PARALLELISM

CREATIVE THOUGHT

OLD LESSONS?

NEW IDEAS

ARCHITECTURES

STANDARDIZATION

HARDWARE CAPABILITIES

TRANSPARENCY

SYNTAXICS

GRANULARITY

INTERCONNECTIONS

ENGINEERING

LIMITATIONS

PARALLEL GRAMMARS

FOR NEW COMPILERS

DESIGN SPEC'S

FOR NEW MACHINES

SIMULATED SOFTWARE ENVIRONMENT

1-147
NEW DIMENSIONS IN PARALLEL COMPUTING

BIT-Serial

Division by $2^{2^k} + 1$

Min/Max Search
Matrix Multiplication
Column Broadcast
Gaussian Elimination

Parallel

Pipeline/Sequential

Linear Recurrence
PERFORMANCE WITH INTEGER OPERANDS

128 x 128 ARRAY
10 MHz CLOCK RATE

ADD ARRAY TO ARRAY
SUBTRACT ARRAY FROM ARRAY
MULTIPLY ARRAY BY ARRAY

MILLIONS OF OPERATIONS PER SECOND

OPERAND WORDLENGTHS, BITS

1-150
DIVISION BY $2^n \pm 1$ EXAMPLE

FROM THE BINOMIAL THEOREM,

$$\frac{1}{1 \pm x} = 1 \mp x + x^2 \mp x^3 + \cdots \quad (x^2 < 1)$$

BY A CHANGE OF VARIABLE $y = \frac{1}{x}$ THEN

$$\frac{1}{y \pm 1} = \frac{1}{y} \mp \frac{1}{y^2} + \frac{1}{y^3} \mp \cdots \quad (y^2 > 1)$$

NOW LET $y = 2^n$ AND DIVISION BY $2^n \pm 1$
REDUCES TO A SHORT SEQUENCE OF BINARY
SHIFTS AND ADDS (AND/OR SUBTRACTS),

$$\frac{\nu}{2^n \pm 1} = \frac{\nu}{2^n} + \frac{\nu}{2^{2n}} + \frac{\nu}{2^{3n}} + \cdots$$

FOR EXAMPLE, LET $\nu = 237658$ AND $n = 10$
THEN

$$\frac{\nu}{2^n - 1} = \frac{\nu}{1024} = \frac{237658}{1024} = 232.315$$

AFTER 3 SHIFTS AND 2 ADDS.
THE GOODYEAR MPP

- SIMD MACHINE OF 16384 SINGLE BIT PROCESSORS ARRANGED IN A 128 X 128 ARRAY
- NEAREST NEIGHBOR INTERCONNECTIVITY
- 1024 BITS OF MEMORY PER PE
- 32 BIT SHIFT REGISTER ALLOWS FOR MICRO-P IPELINING AND FASTER MULTIPLICATION
- EXECUTION SPEED OF 160 BILLION MICRO-INSTRUCTIONS PER SECOND WHICH TRANSLATES TO 800 GOPS FOR SOME INSTRUCTIONS
- OPERATIONS INCLUDE SINGLE BIT LOGICAL, SHIFT, AND ADD AS WELL AS COLUMN I/O AND ONE OR TWO DIMENSIONAL ROUTING IN A SPIRAL, CYLINDER, OR TORUS
- ALL OPERATIONS CAN BE DIRECTLY OR INDIRECTLY MASKED
- THE LOGICAL "OR" OF ONE BIT PER PE (SUMOR) CAN BE USED TO PASS ARRAY INFORMATION BACK TO THE PE CONTROL UNIT FOR BROADCAST, SCALAR I/O, OR CONDITIONAL BRANCHING
ONE OF 16384 MPP PROCESSING ELEMENTS (PE'S)

DATA BUS (D)

FROM WEST PE

TO SUM-OR TREE

TO EAST PE

RANDOM-ACCESS MEMORY

ADDRESS

SUM CARRY
FULL ADDER

C

MASKS

NBR. PE'S

LOGIC

P

N-BIT SHIFT REG.

B

A

(N=2, 6, 10, 14
18, 22, 26 OR 30)
PARALLEL/ASSOCIATIVE ARRAY SELECTION

MPP

REAL S(8:24), A[64,256](8:24)

S = SUMOR(A[64,256])
MAXIMUM OF 32 BIT INTEGER ARRAY
(OF UNIQUE VALUES)

BIT MAX
INTEGER A[128,128](0:32)
MAX=1
DO 1 I=1,32
   IF (SUMOR(A[MAX](I))) MAX=A[MAX](I)
1 CONTINUE

1-155
REAL A[8,16,128](8:32), B[8,16,128](8:32),
  & C[8,16,128](8:32), T[8,16,128](8:32)

READ A[,,1], B[1,,]
T=A[,,1...]*B[1...,]
C=T[,,+]
PRINT C[,,1]
COLUMN BROADCAST EXAMPLE

\[ A_{i,j} = \]

A\(_{i,j}\) = \( A_{\cdot,j} \)

REAL A[128,128](8:32)
A = A[,J...]

OR

REAL A[128,128](8:32)
BIT M[]
M = [128,128;,,J]
A = A[.NOT.M][,128 \rightarrow]
COLUMN BROADCAST EXAMPLE

PROBLEM: TO BROADCAST A COLUMN OF FLOATING POINT NUMBERS ACROSS THE MPP ARRAY

SOLUTION #1: WITH PE’S INTERCONNECTED IN AN E/W CYLINDER; LOAD, SHIFT AND STORE THE 32 BIT VALUES ACROSS THE ARRAY. THIS TAKES APPROXIMATELY 3 \times 32 \times 128 = 12288 CYCLES.

SOLUTION #2: WITH PE’S INTERCONNECTED IN AN E/W CYLINDER; "TRAIN" BROADCAST THE 32 BIT VALUES ACROSS THE ARRAY. THIS CAN BE VIEWED AS A MICRO-PIPELINING OPERATION AND TAKES ONLY 207 CYCLES. THE ALGORITHM IS AS FOLLOWS:

1. GET "TRAIN" OF 1 STOP BIT + 32 BIT VALUES OUT ONTO THE E/W PE CHANNEL (\approx 33 CYCLES)

2. CIRCULATE "TRAIN" ONCE AROUND (\approx 128 CYCLES). DURING THIS PROCESS INDIVIDUAL PE’S WILL STORE THE "TRAIN" IN THEIR SHIFT REGISTERS. SHIFTING STOPS WHEN THE STOP BIT ENTERS THE CONDITIONAL MASK REGISTER OF EACH PE.

3. STORE ALL SHIFT REGISTERS (\approx 32 CYCLES).
GAUSSIAN ELIMINATION EXAMPLE

SINGLE BIT MATRIX

1 2

40 1 1 1 1 3

%0 0 1 0 1 0 3

10 11 12 13

40 1 1 1 1 3

%0 0 1 0 1 0 3

4000 X 4000

1 OF 1000 BIT PLANES

MPP ARRAY

128 X 128

1-159
GAUSSIAN ELIMINATION EXAMPLE

BIT A[4000,4](1000), M[4000,4], USED(4000)
INTEGER PIVOT(4000,0:14), J1(0:2), J2(0:12), J(0:14)
EQUIVALENCE (J1,J(1)), (J2,J(3))

READ A
DO 1 I=1,4000
    USED(I)=0
1 CONTINUE

DO 7 I=1,4000
    DO 2 J2=1,1000
        IF (SUMOR(A[I,J2])) GO TO 3
    2 CONTINUE
    GO TO 8
3 CONTINUE
4 CONTINUE
    J1=1,4
    IF (SUMOR(A[I,J1](J2))) GO TO 5
4 CONTINUE
5 CONTINUE
    PIVOT(I)=J
    USED(J)=1
    M=A[ ](J2).AND..NOT.(4000,4;I,J1); SAVE PIVOT COLUMN IN NEW MATRIX M, ZEROING THE PIVOT ROW VALUE

    DO 6 J2=1,1000
6 CONTINUE
7 CONTINUE
8 CONTINUE
GAUSS-JORDAN MATRIX INVERSION

WITH FULL PIVOTING
PARALLEL DATA STRUCTURES

REAL ARRAYS

\[ U = [ A : I ] \] \text{ AUGMENTED MATRIX} \\
\[ V = [ : ] \] \text{ WORKING ARRAY} \\
\[ W = \_ : ] \] \text{ WORKING ARRAY} \\

BIT MASKS

\[ X = [ \bar{I} : \bar{0} ] \] \text{ PIVOTED ROW/COLUMNS} \\
\[ Y = [ \bar{I} : \bar{I} ] \] \text{ PIVOT ROW} \\

WHERE \( I \) IS THE IDENTITY MATRIX, \( \bar{I} \) IS THE UNITY MATRIX, \( \bar{0} \) IS THE ZERO MATRIX.
OTHER DATA STRUCTURES

SCALARS

DET = 1        PIVOT
PARALLEL APPROACH TO MATRIX INVERSION

REPEAT FOLLOWING STEPS N TIMES

- FIND NEXT PIVOT
- UPDATE DETERMINE (OPTIONAL)
- ZERO PIVOT ROW AND COLUMN IN X
- ZERO PIVOT ROW IN Y
- NORMALIZE PIVOT ROW IN U
- BROADCAST PIVOT ROW N TIMES INTO V
- BROADCAST PIVOT COLUMN 2N TIMES INTO W
- PERFORM PARALLEL ROW OPERATIONS FOR A SINGLE PIVOT
- RESET PIVOT ROW IN Y

THEN REORDER ROWS IN U TO FORM

\[ U = [ I : A^{-1} ] \]
PARALLEL MATRIX INVERSION ALGORITHM

FOR I = 1 TO N
   PIVOT = MAX |U| PER X
   DET = DET * PIVOT
       [X] = 0
       [Y] = 0
       [U] = [U] / PIVOT
       [V] = [U]
       [W] = [U]
       [U] = U - V * W PER Y
       [Y] = 1

END I
FOR J = 1 TO N
   FOR I = 1 TO N
      IF U[I,J] = 1 THEN V[J,•] = U[I,•]
   END I
END J
U = V
MPP II:
WHAT MIGHT IT LOOK LIKE?

- MUCH GREATER MEMORY DEPTH: AT LEAST 64K BITS PER PE, WITH AT LEAST ONE LEVEL OF INDIRECT ADDRESSING.
- RECONFIGURABLE BIT/NIBBLE/BYTE SERIAL ALU
- STAGED PE'S FOR TABLE LOOKUP ARITHMETIC.
  HOW MANY TABLES? WHAT SIZE? RAM OR ROM?
- PIPELINED SUMOR LOGIC