A VLSI CHIP SET FOR REAL TIME VECTOR QUANTIZATION OF IMAGE SEQUENCES

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ABSTRACT

This paper describes the architecture and implementation of a VLSI chip set that vector quantizes (VQ) image sequences in real time. The chip set forms a programmable Single-Instruction, Multiple-Data (SIMD) machine which can implement various vector quantization encoding structures. Its VQ codebook may contain unlimited number of codevectors, N, having dimension up to \( K = 64 \).

Under a weighted least squared error criterion, the engine locates at video rates the best code vector in full-searched or large tree searched VQ codebooks. The ability to manipulate tree structured codebooks, coupled with parallelism and pipelining, permits searches in as short as \( O(\log N) \) cycles. A full codebook search results in \( O(N) \) performance, compared to \( O(KN) \) for a Single-Instruction, Single-Data (SISD) machine. With this VLSI chip set, an entire video code can be built on a single board that permits realtime experimentation with very large codebooks.
OVERVIEW

- MULTISPECTRAL COMPRESSION PROBLEM
- PHILOSOPHY <--- A NEED
- VX IMPLEMENTATION CHALLENGES
- VQ CHIP SET
COMPRESSION RESEARCH AT UCLA

ALGORITHMS

- LOW RATE VIDEO
- SINGLE FRAME
- MULTISPECTRAL

HARDWARE

- APPLICATION SPECIFIC INTEGRATED CIRCUITS
MULTISPECTRAL COMPRESSION PROJECT (JPL)

\[ 192 \lambda \cdot s \]

\[ 768 - 1000 \text{ PIXELS} \]

\[ 50 \text{ MEGAPIXELS/SEC} \]
\[ \frac{3 \times 10^4}{17 \text{ CHANNELS}} \]

\[ \text{DESIRE OVER 50:1} \]
\[ \longrightarrow \text{ UNDER 1/4 BITS/PIXEL} \]
DESIGNER’S PERCEPTIONS
VS.
USER’S NEEDS

CONFERENCE LEVEL  9TH FLOOR
WHAT IS RELEVANT?

WHAT IS REAL?

DEPENDS ON USER

- MEAN SQUARE ERROR
- HAUSDORFF MEASURE
- HUMAN VISION SYSTEM MODELS
- MISSION SCIENTIST MODELS
Basic VQ

ENCODER

minimize \( d(X, \hat{X}_l) \)

Table Lookup

Channel

DECODER

\( \hat{X} \)

Codebook \( \hat{X}_l, l=1, ..., N_c \)

\( \hat{X}_l \)
Mean-Residual VQ Encoder (MRVQ)

original spectrum

mean

residual

Mean

Scalar Quantizer

MR Preprocessor

Vector Quantizer

MR Postprocessor

reconstructed spectrum
DISTORTION COMPUTATION

Minimize squared error:

\[ x = \text{Source vector,} \quad \hat{x}^i = \text{i}th \text{ Code vector,} \]

\[
  i = \min_{i=1, \ldots, N} \left\{ \sum_{k=1}^{K} w_k | x_k - \hat{x}_k^i |^2 \right\},
\]

\[
  = \min_{i=1, \ldots, N} \left\{ \sum_{k=1}^{K} \frac{w_k(x_k)^2}{2} - \sum_{k=1}^{K} w_k \hat{x}_k^i x_k + \frac{\sum_{k=1}^{K} w_k(\hat{x}_k^i)^2}{2} \right\},
\]

\[
  = \min_{i=1, \ldots, N} \left\{ \sum_{k=1}^{K} z_k^i x_k + c^i \right\},
\]

where

\[
  z_k^i \triangleq -w_k \hat{x}_k^i, \quad c^i \triangleq \frac{\sum_{k=1}^{K} w_k(\hat{x}_k^i)^2}{2}.
\]

\[
\begin{array}{c}
  x_1 \\
  z_1^i \\
  c^i
\end{array}
\]

\[
\begin{array}{c}
  x_2 \\
  z_2^i
\end{array}
\]

\[
\begin{array}{c}
  x_3 \\
  z_3^i
\end{array}
\]

\[
\begin{array}{c}
  x_K \\
  z_K^i
\end{array}
\]

\[
\begin{array}{c}
  K-1 \text{ delays} \\
  \overline{i}
\end{array}
\]

\[
\begin{array}{c}
  \min_{i=1, \ldots, N} \rightarrow i
\end{array}
\]

- = Unit delay element
Basic Finite-State Vector Quantization Block Diagram.
PROBLEM: LIMITED SEARCH TIME

- Given:
  - 256x256 resolution image
  - 15 frames per second
  - 4x4 block size.
  \[ \rightarrow 983,040 \text{ pixels/sec} \]
  \[ \rightarrow 61440 \text{ 4x4 blocks/sec} \]
  or 16.3 microseconds/block

- Assume:
  - Pipeline, 10 MHz clock, 1 distortion/clock
  \[ \rightarrow 163 \text{ distortion computations / block} \]
  \[ \rightarrow 163 \text{ codevectors searched / block} \]

THESE #'S VARY AT RESOLUTION, BLOCKSIZE, RATE, ETC. - BUT:

- Problem:
  \[ \rightarrow \text{Prefer 4000+ codevectors in codebook} \]
  \[ \rightarrow \text{Must limit search through codebook} \]
ONE SOLUTION: TREES

N search \quad O(\log N) \text{ search}
N memory \quad O(N) \text{ memory}

- Example

\begin{align*}
N & = 4096 = 2^{12} = 2^5 \times 2^7 \\
\text{Search} & = 2^5 + 2^7 = 160 \\
\text{Memory} & = 2^5 + 2^5 \times 2^7 = 32 + 4096 = 4128
\end{align*}

- Problem: data dependency
  - Minimize pipeline latency
  - Buffer to process several source vectors
OVERALL SYSTEM

![Diagram of OVERALL SYSTEM](image-url)
FEATURES

- SEARCH TREE STRUCTURED CODEBOOKS
  - VECTOR DIMENSION UP TO 64 PIXELS
  - CODEBOOK SIZE LIMITED BY MEMORY
  - ONE DISTORTION COMPUTATION PER CLOCK
  - 6 BITS + SIGN

- ARCHITECTURE
  - SYSTOLIC ARRAY
  - ON CHIP BUFFERING
    --> FULL PROCESSOR UTILIZATION
  - CARRY SAVE ADDER AND DYNAMIC MANCHESTER CARRY CHAIN
  - PIPELINED COMPARATOR

- MMAC IMPLEMENTATION
  - 3 MICRON CMOS (MOSIS)
  - 7900 x 9200
  - ABOUT 30000 TRANSISTORS
  - 10 MHz PROJECTED => 10^7 VECTOR DISTORTIONS PER SECOND
  - 132 PINS

- NAI IMPLEMENTATION
  - 3400 x 4600
  - 1376 TRANSISTORS
  - 28 PIN
  - 12 MHz
SUMMARY

- MULTISPECTRAL COMPRESSION ALGORITHMS UNDER STUDY

- WHAT IS RELEVANT?

- HIGH SPEED VX CHIP SET
  - 10 MEGADISTORTIONS/SEC
  - TREE CODEBOOKS (LARGE)
  - INEXPENSIVE TECHNOLOGY