ANALYSIS AND DESIGN OF A HIGH POWER, DIGITALLY-CONTROLLED SPACECRAFT POWER SYSTEM

SIX MONTH REPORT

PREPARED FOR NASA/GODDARD SPACE FLIGHT CENTER GREENBELT, MD 20771 NAG5-1232

PREPARED BY F.C. LEE AND B.H. CHO

May 16, 1990
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I. SUMMARY

This midterm report describes the progress to date on the Analysis and Design of a High Power, Digitally Controlled Spacecraft Power System. Two quarterly presentations have already been made to NASA Goddard. This report contains the presentation material as well as a summary of the accomplishments to date.

The Statement of Work is divided into two phases.

1. Phase I:
   - Task 1. Battery Discharger Topology Trade-off

2. Phase II:
   - Task 1. ORU Level Modeling and Control
   - Task 2. DC Bus Regulation and Mode Control
   - Task 3. Example Design of Digitally Controlled Spacecraft
   - Task 4. Bus Performance Verification With Model

This report describes the progress on Phase 1, Task 1 and Phase 2 Tasks 1 and 2. The remaining two tasks have just been started.
II. Phase 1, Task 1: Battery Discharger Topology Trade-off

Several battery discharger topologies have been compared for use in the space platform application. The task originally called for a comparison of the following candidate topologies:

1. Boost Converter
2. Tapped-Boost Converter
3. Voltage-Fed Push-Pull with Auto-transformer

Updated information has since been provided on the battery voltage specification. Initially it was thought to be in the 30 to 40 V range. It is now specified to be 53 V to 84 V. This eliminated the tapped-boost and the current-fed auto-transformer converters from consideration. After consultations with NASA, it was decided to trade-off the following topologies:

1. Boost Converter
2. Multi-Module, Multi-Phase Boost Converter
3. Voltage-Fed Push-Pull with Auto-transformer
A non-linear design optimization software tool developed by VPEC was employed to facilitate an objective comparison. Non-linear design optimization insures that the best design of each topology is compared.

The results indicate that a four-module, boost converter with each module operating 90 degrees out of phase is the optimum converter for the space platform.

**Phase 2, Task 1: ORU Level Modeling and Control**

Large-signal and small-signal models have been generated for the shunt, charger, discharger, battery, and the mode controller. The models were first tested individually according to the space platform power system specifications supplied by NASA. The battery ORU model consists of the battery, charger, and discharger models integrated together. This model was used to investigate issues such as interfacing, control, and paralleling of ORU's.

The effect of battery voltage imbalance on parallel dischargers was investigated with respect to dc and small-signal responses. Similarly, the effects of paralleling dischargers and chargers were also investigated. A solar array and shunt model was included in these simulations. A model for the bus mode controller (power control unit) was also developed to interface the ORU model to the platform power system.
Phase 2, Task 2: DC Bus Regulation and Mode Control

The small signal models were used to generate the bus impedance plots in the various operating modes. The large signal models were integrated into a system model, and time domain simulations were performed to verify bus regulation during mode transitions. Some changes have subsequently been incorporated into the models. The changes include the use of a four module boost discharger, and a new model for the mode controller, which includes the effects of saturation. The new simulations for the boost discharger show the improvement in bus ripple that can be achieved by phase-shifted operation of each of the boost modules.
ANALYSIS AND DESIGN OF A HIGH POWER, DIGITALLY CONTROLLED SPACECRAFT POWER SYSTEM

Quarterly Progress Review

for

NASA Goddard Space Flight Center
Greenbelt, MD

January 31, 1990

Prepared by

Virginia Power Electronics Center
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BATTERY DISCHARGER TOPOLOGY TRADEOFF STUDY
COMPARISON APPROACH

DESIGN SPECIFICATIONS

SPREADSHEET PROGRAM

COMPONENT STRESSES

SELECTION OF POWER COMPONENTS

COMPONENT PARAMETERS

SPREADSHEET PROGRAM

INITIAL DESIGN VALUES
INITIAL EFFICIENCY CALCULATION
INITIAL WEIGHT CALCULATION

MINIMUM EFFICIENCY

OPTIMIZATION PROGRAM

BEST DESIGN UNDER GIVEN CONSTRAINTS
BOOST CONVERTER CHARACTERISTICS

SIMPLEST STEP-UP TOPOLOGY
1 SWITCH, 1 DIODE
NO TRANSFORMER

CONTINUOUS INPUT CURRENT

HIGH RMS CURRENT STRESS IN C_o

DIFFICULT CONTROL CHARACTERISTICS
MOVING POLES
RIGHT-HALF-PLANE ZERO
CIC NECESSARY TO OBTAIN GOOD PERFORMANCE
VFPPAT CONVERTER CHARACTERISTICS

Vo/Vi = 1 + ND

BUCK-TYPE STEP-UP TOPOLOGY
   2 SWITCHES, 2 DIODES

CONTINUOUS OUTPUT CURRENT

SEMI-CONTINUOUS INPUT CURRENT

HIGHER SWITCH AND DIODE VOLTAGE STRESS

SIMPLER CONTROL CHARACTERISTICS
   CIC NECESSARY TO FLUX-BALANCE TRANSFORMER

LOW SWITCHING LOSS

POTENTIALLY HIGH LEAKAGE INDUCTANCE LOSS
VOLTAGE-FED, PUSH-PULL WITH TAPPED AUTOTRANSFORMER (VFPPAT) CONVERTER
MULTI-MODULE/MULTI-PHASE CONCEPT

DRAMATIC REDUCTION OF OUTPUT CAP: STRESS BENEFICIAL FOR THE BOOST CONVERTER MUCH FASTER TRANSIENT RESPONSE POSSIBLE CAN BE MORE RELIABLE CLOSED-LOOP CURRENT SHARING N+1 REDUNDENCY
OUTPUT FILTER DESIGN

SECOND STAGE CAPACITOR IS BUS CAPACITANCE
DESIGN FOR 1V P-P RIPPLE ON FIRST STAGE
SECONDARY RESONANCE DESIGNED FOR Fs/5
95% EFFICIENT BOOST DESIGN

Fs: 110 KHZ
L: 30 uH
C: 70 uF
INDUCTOR TURNS: 11
INDUCTOR CORE WIDTH: 9.5E-3 M
INDUCTOR WINDOW WIDTH: 4.3E-3 M
INDUCTOR AIR GAP: 13 MILS
INDUCTOR WIRE SIZE: 1.03E-6 M^2

LOSS BREAKDOWN
FET CONDUCTION LOSS: 9.5 W
FET SWITCHING LOSSES: 50.0W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 9.4
INDUCTOR COPPER LOSS: 11.4 W
INDUCTOR CORE LOSS: .9 W

WEIGHT BREAKDOWN
INDUCTOR WEIGHT: .02 KG
CAPACITOR WEIGHT .32 KG
TOTAL: .34 KG
97% EFFICIENT BOOST DESIGN

Fs: 45 KHZ
L: 72 uH
C: 180 uF
INDUCTOR Turns: 22
INDUCTOR CORE WIDTH: 1.1E-2 M
INDUCTOR WINDOW WIDTH: 1.1E-2 M
INDUCTOR AIR GAP: 28 MILS
INDUCTOR WIRE SIZE: 3.2E-6 M^2

LOSS BREAKDOWN
FET CONDUCTION LOSS: 9.1 W
FET SWITCHING LOSSES: 20.3 W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 3.8 W
INDUCTOR COPPER LOSS: 8.1 W
INDUCTOR CORE LOSS: 0.4 W

WEIGHT BREAKDOWN
INDUCTOR WEIGHT: .08 KG
CAPACITOR WEIGHT: .74 KG
TOTAL: .82 KG
95% EFFICIENT VFPPAT DESIGN

Fs: 75 KHZ
L: 63 uH
Co: 3 uF
Ci: 25 uF
IND. TURNS: 56
IND. CORE WIDTH: 4.1E-3 M
IND. WINDOW WIDTH: 9.3E-3 M
IND. AIR GAP: 32 MILS
IND. WIRE SIZE: 9.3E-7 M^2

XFORMER TURNS: 9
XFORMER CORE WIDTH: 1.3E-2 M
XFORMER WINDOW WIDTH 4.0E-3 M
XFORMER LEAKAGE L: 1.3 uH

LOSS BREAKDOWN
FET CONDUCTION LOSSES: 32.8 W
FET SWITCHING LOSSES: 17.2 W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 7.2
INDUCTOR COPPER LOSS: 7.4 W
INDUCTOR CORE LOSS: 0.0 W
XFORMER COPPER LOSS: 11.0 W
XFORMER CORE LOSS: 1.6 W
XFORMER LEAKAGE LOSS: 5.9 W

WEIGHT BREAKDOWN
INDUCTOR WEIGHT: .01 KG
CAPACITOR WEIGHT: .13 KG
XFORMER WEIGHT: .13 KG
TOTAL: 0.27 KG
95% EFFICIENT FOUR MODULE BOOST DESIGN

$\text{Loss Breakdown}$

- **FET Conduction Loss:** 9.6 W
- **FET Switching Losses:** 50.0 W
- **Diode Conduction Loss:** 13.5 W
- **Diode Switching Losses:** 9.4 W
- **Inductor Copper Loss:** 8.7 W
- **Inductor Core Loss:** 2.7 W

$\text{Weight Breakdown}$

- **Inductor Weight:** .04 KG
- **Capacitor Weight:** .11 KG
- **Total Weight:** .15 KG
97% EFFICIENT FOUR MODULE BOOST DESIGN

Fs: 40 KHz
L: 319 uH
C: 50 uF
INDUCTOR TURNS: 5
INDUCTOR CORE WIDTH: 2.2E-2 M
INDUCTOR WINDOW WIDTH: 1.7E-3 M
INDUCTOR AIR GAP: 2 MILS
INDUCTOR WIRE SIZE: 3.3E-7 M^2

LOSS BREAKDOWN
FET CONDUCTION LOSS: 9.1 W
FET SWITCHING LOSSES: 17.7 W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 3.3 W
INDUCTOR COPPER LOSS: 9.8 W
INDUCTOR CORE LOSS: 5.3 W

WEIGHT BREAKDOWN
INDUCTOR WEIGHT: .23 KG
CAPACITOR WEIGHT: .23 KG
TOTAL: .46 KG
CONCLUSIONS

A MULTI-MODULE BOOST CONVERTER OFFERS THE LOWEST WEIGHT BATTERY DISCHARGER

97% EFFICIENCY IS OBTAINABLE AND PRACTICAL

FLIGHT QUALIFIED PARTS CAN BE USED

BOTH THE VFPPAT AND THE BOOST DESIGNS REQUIRE CIC. VFPPAT FOR FLUX BALANCING, AND THE BOOST FOR DYNAMIC PERFORMANCE AND STABILITY

THE STABILITY MARGIN OF THE BOOST DESIGN CAN BE MADE EQUAL TO THE VFPPAT DESIGN

OUTPUT IMPEDANCE AND LOAD TRANSIENT RESPONSE OF THE BOOST DESIGN CAN BE MADE EQUAL TO OR BETTER THAN THE VFPPAT DESIGN
SPACE PLATFORM ORU-LEVEL MODELING AND CONTROL
SPACE PLATFORM
ORU LEVEL MODELLING AND CONTROL

PHASE II, TASK 1

* BATTERY ORU = BATTERY, CHARGER, & DISCHARGER
  - MODULARITY AND REPLACEMENT
  - REDUNDANCY

* EASY5 MODEL GENERATION FOR BATTERY ORU
  - USE OF EXISTING COMPONENT MODELS
  - EASE OF PARALLELING

* PARALLELING OF BATTERY ORUs
  - EASY5 SIMULATION
  - ANALYSIS

* BATTERY DISCHARGER PARALLELING

* BATTERY CHARGER PARALLELING
  - CHARGE CURRENT REGULATION
  - BUS VOLTAGE REGULATION
PARALLEL BATTERY ORU MODULES

120V BUS
(+/- 4%)

CHARGER

BATTERY
64-84V
ORU # 1

SOLAR ARRAY
SHUNTS
LOADS

CHARGER

BATTERY
64-84V
ORU # 4
BATTERY DISCHARGE POWER CONVERTER

**BOOST CONVERTER DESIGN FROM SPREADSHEET**

**CONVERTER CHARACTERISTICS**
- \( V_{in} = 64 - 84 \text{ V} \)
- \( V_{out} = 120 \text{ V} \)
- DUTY RATIO = .30 TO .47
- EFFICIENCY = 96 \%
- 75 KHz SWITCHING FREQUENCY
- VOLTAGE RIPPLE < 200mV Pk-Pk
- OUTPUT POWER = 1500W CONTINUOUS / 1800W PEAK

**TWO LOOP CONTROL METHOD**
- SINGLE COMMON VOLTAGE LOOP
- ONE CURRENT LOOP PER DISCHARGER
- PRELIMINARY LOOP COMPENSATION

**TWO STAGE FILTERING**
- LOW OUTPUT VOLTAGE RIPPLE
- LOW OUTPUT IMPEDANCE
EASY5 DISCHARGE CONVERTER MODEL

* LARGE SIGNAL CHARACTERISTICS

* DISCRETE CIRCUIT EQUATIONS
  - CONTINUOUS CONDUCTION MODE
  - DISCONTINUOUS CONDUCTION MODE

[Diagram of the circuit components, including Boost Power Stage, Current Sense, Error Amp and Compensator, PWM Stage, with labels IL, IQ, VO, VE, VI.]
DC ANALYSIS FOR PARALLEL DISCHARGERS

* BATTERY VOLTAGE IMBALANCE
  - CHARGE IMBALANCE
  - SHORTED CELL

* CURRENT MODE CONTROL: CURRENT SHARING
  - BATTERY CURRENT = INDUCTOR CURRENT
  - PEAK CURRENT DETECTION

\[ \frac{dl}{dt} = \frac{dV}{L} \]

BATTERY "A" VOLTAGE > BATTERY "B" VOLTAGE

RESULT: BATTERY "A" AVERAGE CHARGE CURRENT IS HIGHER
PARALLEL DISCHARGER CURRENTS
BATTERY "A" = 64V, BATTERY "B" = 84V

Free Running
Freq. Mismatch

"A" I_{i1}

4.5 A p-p

AVE = 23.5A

"B" I_{i1}

L6A p-p

AVE = 25.2A

"A" I_{i2}

AVE = 12.5A

"B" I_{i2}

AVE = 17.6A

Check peak value
SINGLE DISCHARGER TRANSIENT RESPONSE #

Vbus

lload

PARALLEL DISCHARGER TRANSIENT RESPONSE #

Vbus

lload

# SAME COMPENSATION
SMALL SIGNAL ANALYSIS OF PARALLEL DISCHARGERS

* STABILITY MODIFIED BY ADDING PARALLEL MODULES

* MODIFICATION OF FILTER CORNER FREQUENCIES
  - FIRST CORNER FREQUENCY = VARIABLE
  - SECOND CORNER FREQUENCY = FIXED

* WORST CASE IS FOUR PARALLEL DISCHARGERS

* LOOP RECOMPENSATION NECESSARY

* SPICE MODEL FOR FEEDBACK LOOP ANALYSIS
Parallel Boost Converters

Vin1 = Vin2 = 6.4V, Re = 4Ω

Original Compensation

Gain vs Deg.
LOOP RECOMPENSATION FOR PARALLEL DISCHARGERS

* TWO POLE & ONE ZERO COMPENSATOR

\[
\frac{V_o}{V_{bus}} = \frac{W_m(1 + S/W_z)}{S(1 + S/W_p)}
\]

* RECOMPENSATION STRATEGY
- SHIFT ZERO TO HIGHER FREQUENCY
- REDUCE DC GAIN

* TRADE-OFF MODULARITY FOR LOOP GAIN & BANDWIDTH

* LOOP GAIN AND PHASE NOT AFFECTED BY BATTERY VOLTAGE IMBALANCE
Parallel Boost Converters

\[ V_{in1} = V_{in2} = 6uv, \quad R_L = 4 \Omega \]

New Compensation

\[ \phi_M = 59^\circ \]

\[ f_c = 17 \text{kHz} \]
RECOMPENSATED PARALLEL DISCHARGER TRANSIENTS

Vbus

Ibus

IL1
BAT "A"

IL2
BAT "B"

Vbat "A" = 64V, Vbat "B" = 84V
EASY5 BATTERY CHARGER MODEL

* BUCK CONVERTER EXAMPLE DESIGN FROM FAIRCHILD REPORT

* CHARGE CURRENT REGULATION
  - INDUCTOR CURRENT SENSING & REGULATION
  - CHARGE RATE LIMITING

* BUS VOLTAGE REGULATION
  - CHARGE CURRENT VARIED TO CONTROL BUS VOLTAGE
  - BUCK CONVERTER WITH FEEDFORWARD OF Vbus
  OR
  BOOST CONVERTER WITH FEEDBACK OF Vbus
Battery Charger Circuit
PARALLEL CHARGER MODEL

Redraw the block diagram.

Vbus

Vref

Verr

OR

AMP

Iref

COMP

RAMP

ORU #1

OR

AMP

Iref

COMP

RAMP

ORU #2
--- CHARGE CURRENT REGULATION MODE ---

SINGLE CHARGER TRANSIENT RESPONSE *

PARALLEL CHARGER TRANSIENT RESPONSE *

* SAME COMPENSATION FOR EACH CASE
-- BUS VOLTAGE REGULATION MODE --

SINGLE CHARGER TRANSIENT RESPONSE *

Vbus

115.2
115.16
115.12
115.08
115.04
115
114.96
0.001
0.002
0.003
0.004
0.005
0.006
0.007
Vbus FROM BUS

Ichg

25
22.5
20
17.5
15
12.5
10
7.5
0.001
0.002
0.003
0.004
0.005
0.006
0.007
PARALLEL CHARGER TRANSIENT RESPONSE *

Vbus

115.2
115.16
115.12
115.08
115.04
115
114.96
0.001
0.002
0.003
0.004
0.005
0.006
0.007
Vbus FROM BUS

Ichg

14
12
10
8
6
4
2
0.001
0.002
0.003
0.004
0.005
0.006
0.007
* BOTH BATTERIES = 64V
SUMMARY OF BATTERY ORU MODELLING

* EASY5 MODELS DEVELOPED FOR BATTERY ORU

* PARALLEL DISCHARGER MODELLING
  - DC CURRENT SHARING
  - RECOMPENSATION FOR PARALLEL MODULES
  - BATTERY VOLTAGE IMBALANCE & LOOP GAIN

* PARALLEL CHARGER MODELLING
  - CHARGE CURRENT REGULATION MODE
  - BUS VOLTAGE REGULATION MODE
REVIEW OF SPACE PLATFORM POWER SYSTEM MODELING
INTRODUCTION

Modeling and simulation:

Large and small signal component models have been developed for the following, using the EASY5 analysis program:

- Solar cells/solar array
- Solar array shunt switching units
- DC-DC converters (buck, boost, flyback, forward)
- Error amplifiers, PWM controllers
- Battery dischargers (boost, tapped-boost) and output filter
- Battery charger (buck) and input filter
- Battery
- Loads
- Mapham inverter
- Spacecraft power system models (for both AC and DC bus)

These models have been used to study:

- Transient response to step change of load
- Mode transitions with changes of illumination level
- Paralleling of chargers and dischargers
- Stability study using frequency response plots (small signal models)

Design and analysis:

- Battery charger design
- Battery discharger topology trade-off study
- Battery discharger design
- Analysis of bus impedance, stability and ripple in the shunt regulation mode
- Analysis of bus impedance in charger and discharger regulated modes

Proposed future work:

- Modeling, analysis, design
- Hardware system testbed
Fig. 2.1-5 Compensators for [SR] model
Fig. 4 Loop gain and bus impedance plots
Salient design features for shunt unit and bus capacitor

- For a properly designed system, the peak bus impedance is the ESR of the bus filter capacitor (this determines the overshoot for a step load change).

- A proportional controller has fast transient response but has a load dependant bus voltage error (a voltage "band" requirement).

- An integrator type compensator can decrease the voltage band requirement, but the zero required to reduce phase lag results in a low frequency pole in the bus impedance. This may make the transient response slower.

- The bus ripple depends on the following factors:
  
  Switching frequency
  Bus capacitor ESR
  Bus capacitance
  Current per parallel switch

\[ V_{pp} = I_p R_c + D(1 - D) \frac{T_s I_p}{C} \]

where

\[ D = \text{duty ratio modulation} \]
\[ R_c = \text{bus capacitor ESR} \]
\[ I_p = \text{current from one set of NPS strings} \]
\[ T_s = \text{switching period} \]
\[ C = \text{bus capacitor} \]
Fig. 5a  Simulation for proportional compensator
Fig. 5b  Simulation for PI compensator
Battery charger circuit (Buck) with input filter

- An input filter is added to smooth the pulsating current drawn by the buck converter.
- The circuit can be made to function in two modes.
- In the bus voltage regulation mode, the current is less than the maximum battery charge current and the charger regulates the bus.
- When the array has sufficient illumination to provide the maximum charge current, the charger current is limited to this maximum value. The bus voltage rises and the array shunt switching unit regulates the bus.
Salient design features for the charger

- Input filter corner frequency is one decade below the switching frequency to lower the ripple to 1% of output side ripple
- An integrator type compensator (2 poles, 2 zeroes) is used.

\[ H_v = \frac{w_m}{s} \frac{(1 + s/w_{z1})(1 + s/w_{z2})}{(1 + s/w_p)} \]

- The low frequency compensator zero is the dominant pole for bus impedance and determines transient response. It is kept as large as possible. However, placing it beyond the low frequency pole of the power stage can cause conditional instability
- The peak overshoot is determined by the ESR of the bus filter capacitor
- The second zero approximately determines the settling speed of the system
- These transient response features have been verified from the step load simulation
Simulation for transient response of charger

illuminaton level

[A]

currents

[A]

input filter current

[V]

bus voltage
**Discharger topology comparison**

Topologies considered for discharger

**Boost**

**Tapped boost**

Voltage fed push pull with tapped auto transformer (VFPPTAT)

Current fed push pull with tapped auto transformer (CFPPTAT)
<table>
<thead>
<tr>
<th></th>
<th>Boost</th>
<th>T-Boost</th>
<th>VFPPTAT</th>
<th>CFPPPTAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor Tap Ratio</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>X-former Tap Ratio</td>
<td>n/a</td>
<td>n/a</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Conversion Frequency</td>
<td>25kHz</td>
<td>25kHz</td>
<td>50kHz</td>
<td>50kHz</td>
</tr>
<tr>
<td>Inductance (15% Ripple)</td>
<td>59µH</td>
<td>140µH</td>
<td>65µH</td>
<td>5.5µH</td>
</tr>
<tr>
<td>Peak Inductor Current</td>
<td>66 A</td>
<td>42.5 A</td>
<td>19.2 A</td>
<td>66 A</td>
</tr>
<tr>
<td>Inductor Energy ($\frac{1}{2} LI_\delta^2$)</td>
<td>.13 W-S</td>
<td>.13 W-S</td>
<td>.010 W-S</td>
<td>.012 W-S</td>
</tr>
<tr>
<td>Max. Duty Cycle</td>
<td>73%</td>
<td>56%</td>
<td>41% *</td>
<td>47% *</td>
</tr>
<tr>
<td>Peak Q current</td>
<td>66 A</td>
<td>85 A</td>
<td>57.6 A</td>
<td>49.5 A</td>
</tr>
<tr>
<td>RMS Q current</td>
<td>49 A</td>
<td>55 A</td>
<td>37 A</td>
<td>30 A</td>
</tr>
<tr>
<td>Peak Q Voltage</td>
<td>120 V</td>
<td>82.5 V</td>
<td>90 V</td>
<td>120 V</td>
</tr>
<tr>
<td>Peak Diode Current</td>
<td>66 A</td>
<td>42.5 A</td>
<td>19.2 A</td>
<td>33 A</td>
</tr>
<tr>
<td>Peak Diode Voltage</td>
<td>120 V</td>
<td>16.5 V</td>
<td>210 V</td>
<td>180 V</td>
</tr>
<tr>
<td>Input Cap RMS Current</td>
<td>0</td>
<td>18.4 A</td>
<td>19.7 A</td>
<td>0</td>
</tr>
<tr>
<td>Output Cap RMS Current</td>
<td>26 A</td>
<td>19 A</td>
<td>0</td>
<td>10.3 A</td>
</tr>
<tr>
<td>Pri. Leakage L delta I</td>
<td>0</td>
<td>42.5 A</td>
<td>38.4 A</td>
<td>16.5 A</td>
</tr>
</tbody>
</table>

+ This is the whole inductance. The primary inductance is $35\mu H$.

* This is the duty cycle per switch. The duty cycle seen by the inductor is twice.
Results of comparison: choice of discharger topology

- the boost converter is simple, has only one switch, one diode and no transformer, and continuous input current
- it however has disadvantages (specially if the step up ratio is high). These are the RHP zero in the control/output voltage transfer function, high output current stress in the output capacitor, and difficulty in control loop design at high transformation ratios (i.e., high duty ratio)
- the tapped boost allows a lower duty ratio for a given voltage step up, the RHP zero is at a higher frequency and more manageable
- the VFPPTAT is buck derived so it provides continuous output current, well behaved control characteristics, and a lower current stress than the boost or tapped boost
- the VFPPTAT however needs two diodes and two switches, and the circuit is sensitive to transformer saturation
- CFPPTAT has many desirable features such as lowest switch current stress.
- the CFPPTAT however needs two switches, and it is expected that that it may not compare favorably with 2 tapped boost converters operating in parallel and out of phase by 180 degrees
- the tapped boost topology was therefore selected for modeling as discharger
Simulation waveforms for tapped boost discharger model

a) First Stage Capacitor Bank Voltage

b) Bus Voltage

c) Input Current
Transient response of discharger to a 1 A step load current change

(a) First Stage Capacitor Bank Voltage

(b) Bus Voltage

(c) Input Current
Bus Impedance in Shunt Mode

Bus Impedance in Charge Mode

Bus Impedance in Discharge Mode

Comparison of bus impedances in different modes
Fig. 4.1-5  Sunlight to eclipse transition
Fig. 4.1-6  Eclipse to sunlight transition
Proposed future work: Hardware system testbed

Objectives:

- To enable verification and improvement of existing EASY5 computer models
- To provide experimental confirmation of analytical design procedures

Proposed hardware work:

The following are to be designed, built and tested. The designs will be optimized by VPEC’s power converter optimization (CADO) software.

- battery charger
- battery discharger (boost, and an alternate topology)
- mode controller

These are to be tested with:

- a simple solar array simulator
- battery simulator
- load bank

These will allow verification of simulations for many of the system modes. Future work could incorporate a solar array shunt switching unit for verification of the shunt mode.
References:


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QUARTERLY PROGRESS REVIEW

for

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VIRGINIA POLYTECHNIC INSTITUTE AND STATE UNIVERSITY
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PRESENTATION OUTLINES

1. Space Platform Power System Modeling
   1.1 Battery discharger analysis & design  
   1.2 EASY5 modeling for battery ORU
      Battery charger/discharger mode control

2. Space Platform Power System Testbed
   2.1 Battery discharger design
      2.1.1 Four-module boost
      2.1.2 Voltage-fed push-pull autotransformer
   2.2 Battery charger design

3. Discussion
1. SPACE PLATFORM

POWER SYSTEM MODELING
### NASA/GSFC Space Platform Modeling

#### Project Schedule

**Phase II (Ending 8/31/90)**

<table>
<thead>
<tr>
<th>NO</th>
<th>TASK DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><strong>ORU Level Modeling and Control</strong></td>
</tr>
<tr>
<td></td>
<td>• Parallel battery ORU subsystem modeling</td>
</tr>
<tr>
<td></td>
<td>• ORU control and analysis</td>
</tr>
<tr>
<td></td>
<td>- Issues related to paralleling</td>
</tr>
<tr>
<td>2</td>
<td><strong>DC Bus Regulation and Mode Control</strong></td>
</tr>
<tr>
<td></td>
<td>• PV subsystem w/the parallel ORU modeling</td>
</tr>
<tr>
<td></td>
<td>• Design</td>
</tr>
<tr>
<td></td>
<td>• Analysis and Simulation of PV Subsystem</td>
</tr>
<tr>
<td></td>
<td>- Controller Design</td>
</tr>
<tr>
<td></td>
<td>- Band Tolerance and bus regulation</td>
</tr>
<tr>
<td></td>
<td>- Charger, SASU</td>
</tr>
</tbody>
</table>

4/26
<table>
<thead>
<tr>
<th>NO</th>
<th>TASK DESCRIPTION</th>
<th>11</th>
<th>12</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.</td>
<td>Example Design of Integrated System</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>System Level Simulation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Verifications</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.</td>
<td>Report</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Quality</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Final Report</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Final Presentation
BATTERY DISCHARGER ANALYSIS

PROGRESS SINCE LAST MEETING

1) TRADEOFF STUDY HAS BEEN FURTHER REFINED
   USE OF POLYPROPYLENE INSTEAD OF POLYCARBONATE CAPS
   INDUCTOR CORE LOSS DATA HAS BEEN UPDATED
   TWO DIODES IN SERIES EMPLOYED FOR REDUNDENCY

2) MULTI-MODULE BOOST CONVERTER CONTROL LOOP HAS BEEN REFINED
   DAMPING PROVIDED FOR SECONDARY OUTPUT FILTER
   HIGHER GAIN MARGIN PROVIDED

3) DESIGNS HAVE BEEN SELECTED FOR HARDWARE BUILD
   45 KHZ, 97% EFFICIENT MULTI-MODULE BOOST CONVERTER
   40 KHZ, 96% EFFICIENT VOLTAGE-FED AUTOTRANSFORMER CONVERTER
BATTERY DISCHARGER TRADEOFF STUDY

BOOST CONVERTER

VOLTAGE-FED, PUSH-PULL WITH TAPPED AUTOTRANSFORMER (VFPPAT) CONVERTER
MULTI-MODULE/MULTI-PHASE CONCEPT

OUTPUT CAPACITOR RIPPLE CURRENT

![Graph showing output capacitor ripple current vs. battery voltage. The graph compares single phase and four phase systems. The single phase system shows a linear decrease, while the four phase system shows a more complex, non-linear pattern.](image)

**Single Phase**

**Four Phase**
SINGLE-MODULE BOOST DESIGNS

![Graph showing weight (kgs) vs. switching frequency (kHz) for different efficiencies. The graph indicates that as the switching frequency increases, the weight decreases for 97% efficient designs, remains constant for 96% efficient designs, and increases slightly for 95% efficient designs.](image-url)
VOLTAGE-FED AUTOTRANSFORMER DESIGNS

96% EFFICIENT

95% EFFICIENT

WEIGHT (KGS)

SWITCHING FREQUENCY (KHZ)
FOUR MODULE BOOST DESIGNS

![Graph showing weight (kgs) versus switching frequency (kHz) for different efficiency levels: 97%, 96%, and 95% efficient. The graph illustrates the trade-off between weight and efficiency at various switching frequencies.](image-url)
FOUR MODULE BOOST CONTROL CIRCUIT

PWM
70KHZ
183uH
183uH
183uH
183uH

10uH
.3 3uH
2000uF

40uF

Vbus

1.3M
37pF

12.8 V
Vref
6.65K

1000pF
20.5K

1.6M

V_sense
83.8K

10K

MODE CONTROL

BATTERY CHARGE

SHUNT
BOOST CONVERTER

Date/Time run: 04/28/90 11:53:36
Temperature: 27.0

1 amp step load transient Response

119.85V

119.80V

119.75V

9.0ms 10.0ms 12.0ms 14.0ms 16.0ms 18.0ms 20.0ms
ORU MODELLING WITH EASY5

SUMMARY AND REVIEW

- PARALLEL DISCHARGER CONTROL
  * BATTERY VOLTAGE IMBALANCE & CURRENT SHARING
  * 2'nd STAGE LC FILTER
  * EFFECT OF PARALLELING ON STABILITY

- PARALLEL Charger CONTROL

NEW EASY5 MODELS

- MODE CONTROLLER (PCU)
- FOUR PHASE MODULATOR

ORU POWER SYSTEM CONTROL
SPACE PLATFORM POWER SYSTEM

BATTERY ORU #1

DISCHARGER

PHASE 1

PHASE 2

PHASE 3

PHASE 4

CHARGER

64-84V

BATTERY

SOLAR ARRAY AND SSU

LOADS

COMMON FILTER

120V BUS

Cbus

BATTERY ORU #2

BATTERY ORU #3

BATTERY ORU #4

MODE CONTROLLER (PCU)

TO DISCHARGER

TO SHUNTS

1.2-2
PARALLEL DISCHARGER CONTROL

120V BUS
Cbus
Load

ERROR AMP & COMPEN.
Vref

Vc

ORU #1
L2
L3
C1
RAMP
COMP
Is

ORU #2
L2
L3
C1
RAMP
COMP
Is

L1
BATTERY1

L1
BATTERY2

1.2-3
DC ANALYSIS FOR PARALLEL DISCHARGERS

* BATTERY VOLTAGE IMBALANCE
  - CHARGE IMBALANCE
  - SHORTED CELL

* CURRENT MODE CONTROL: CURRENT SHARING
  - BATTERY CURRENT = INDUCTOR CURRENT
  - PEAK CURRENT DETECTION

Battery "B" voltage > Battery "A" voltage

Result: Battery "B" average discharge current is higher, voltage imbalance corrected.
TWO STAGE LC FILTER

\[ L1 \quad -- \quad C1 \quad -- \quad L2 \quad \quad \quad L1 \gg L2 \]
\[ CBUS \quad >> \quad C1 \]

\[ \text{CHARACTERISTIC EQUATION} \]

(Note: \( C2 = CBUS \))

\[ S^4 + S^2 \left( \frac{1}{L2 C1} + \frac{1}{L2 C2} \right) + \frac{1}{L1 L2 C1 C2} = 0 \]

\[ \left[ S^2 + \frac{1}{L1 (C1 + C2)} \right] \left[ S^2 + \frac{1}{L2 C1} + \frac{1}{L2 C2} \right] = 0 \]

\[ \text{RESONANT FREQUENCIES} \]

\[ W_{o1} = \frac{1}{\sqrt{L1 (C1 + C2)}} \approx \frac{1}{\sqrt{L1 C2}} \]

\[ W_{o2} = \frac{1}{\sqrt{L2 \left( \frac{C1 C2}{C1 + C2} \right)}} \approx \frac{1}{\sqrt{L2 C1}} \]
PARALLEL CONVERTERS WITH TWO STAGE FILTERS

(BUCK OR BOOST EQUIVALENT)

\[ W_{o1} = \frac{1}{\sqrt{\frac{L1}{n} (n C1 + Cbus)}} \approx \frac{\sqrt{n}}{\sqrt{L1 Cbus}} \]

\[ W_{o2} = \frac{1}{\sqrt{\frac{L2}{n} \left[ \frac{n C1 Cbus}{n C1 + Cbus} \right]}} \approx \frac{1}{\sqrt{L2 C1}} \]
PARALLEL CHARGER MODEL

Vbus

Cbus

Vref

amp

Verr

+ AMP

Iref

COMP

RAMP

ORU #1

ORU #2

1.2-7
EASY5 FOUR PHASE MODULATOR MODEL

VOLTAGE ERROR

CURRENT ERRORS

VI1, VI2
VI3, VI4

FM

DUTY CYCLE

IQ1, IQ2
IQ3, IQ4

THE FOUR MODULATOR RAMPS ARE ALL SHIFTED BY 90 DEG:

VR1

VR2

VR3

VR4

90 DEG
EASY5 MODE CONTROLLER MODEL

NOTE: ALL OP-AMPS HAVE ONE COMMON 12.8V REFERENCE
MODELING AND SIMULATION OF POWER SYSTEM

- System block diagram
- Operation of solar array
- Operation of 4-module discharger
- Operation of charger
- Mode transition from array to discharger
• New models are controlled by a central mode controller
• New discharger is a 4-module boost converter
• Models are set up as per the proposed hardware design
• Details are shown in the subsequent simulations
• Each mode is tested with a step load change
• Mode transition is induced by changing the illumination level
SOLAR ARRAY SWITCHING UNIT OPERATION

- The solar array is controlled by a central mode controller
- The bus is regulated by the array
- The simulation shows a change in parallel strings with load
SOLAR ARRAY OPERATION FOR LOAD STEP CHANGE

Bus Voltage

Number of parallel strings

Control voltage

Load current
• The voltage error is common to all modules
• Each module has its own phase shifted PW modulator
• Current feedback is applied separately to each module
PHASE-SHIFTED RAMPS FOR MULTIMODULE BOOST DISCHARGER

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>20</th>
<th>40</th>
<th>60</th>
<th>80</th>
<th>µ sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1.2-15
DISCHARGER OPERATION FOR A LOAD STEP CHANGE

0.4 0.6 0.8 1.0 1.2 1.4 1.6 m sec

Bus Voltage

Filter primary cap. volt.

Control voltage

Load current

Filter Inductor Current

Damping Inductor Current

1.2-16
EQUAL SHARING OF CURRENT BY THE FOUR MODULES

0.4  0.6  0.8  1.0  1.2  1.4  1.6 m sec

[Graphs showing current sharing over time]
DISCHARGER OPERATION WITHOUT PHASE SHIFTED RAMPS

Bus Voltage

Filter primary cap. vc

Control voltage

Load current

Filter Inductor Current

Damping Inductor Current
In the voltage regulation mode, the charger regulates the bus.

The bus is regulated by changing the charging current.
- In the current regulation mode, the array regulates the bus
- The charger regulates the charging current at the limiting value
CHARGER IN CURRENT REGULATION MODE

Battery charging current

Filter Cap. voltage

Charger Input current

1.2 - 20 A

C.2
CHARGER IN VOLTAGE REGULATION MODE

Bus Voltage

Filter Cap. voltage

Control voltage

1.2 -20B
- Mode transitions are induced by changing the illumination level.
- With sufficient illumination, the array regulates the bus.
- At low illumination level, the discharger regulates the bus.
SIMULATION FOR TRANSITION FROM SUNLIGHT TO ECLIPSE

Bus Voltage

Illumination level

Shunt Control voltage

Discharger Control voltage

Parallel strings (shunt)

Discharger Current
2. SPACE PLATFORM

POWER SYSTEM TEST BED
NASA/GSFC Space Platform Testbed

Year 1 Tasks

1. Design Multi-Module Boost Converter  
2. Design VFPPAT Converter  
3. Build Multi-Module Boost Converter  
4. Build VFPPAT Converter  
5. Design Battery Charger  
6. Build Battery Charger  
7. Test Multi-Module Boost Converter (Open-Loop)  
8. Test VFPPAT Converter  
9. Select Optimum Discharger & Design Control Loop  
10. Build Discharger Controller, Integrate & Tester  
11. Test Battery Charger  
12. Design Charger Controller  
13. Build Charger Controller & Integrate  
14. Integrate Charger & Discharger (W/Mode Controller)  
15. Test ORU System  
16. Investigate Bi-directional Converter
97% EFFICIENT FOUR MODULE BOOST DESIGN

INDUCTOR DESIGN
- Inductor Turns: 31
- Inductor Core Width: 8.6E-3 M
- Inductor Window Width: 8.9E-3 M
- Inductor Air Gap: 9 MILS
- Inductor Wire Size: 1.54E-6 M^2

WEIGHT BREAKDOWN
- Inductor Weight: 0.16 KG
- Capacitor Weight: 0.16 KG
- Total: 0.32 KG

LOSS BREAKDOWN
- FET Conduction Loss: 9.1 W
- FET Switching Losses: 11.8 W
- Diode Conduction Loss: 22.5 W
- Diode Switching Losses: 3.7 W
- Inductor Copper Loss: 5.9 W
- Inductor Core Loss: 4.8 W
MULTI-MODULE BOOST HARDWARE DEVELOPMENT

UC3825

UC3825

UC3825

UC3825

284u 1N5816

IRF250

UC3706

284u

IRF250

UC3706

284u

IRF250

UC3706

1N5816

Vbus

20u

20u

20u

Vbatt

45KHZ φ1-φ4

CD4017

CD4047

JOHNSON COUNTER

180KHZ OSC
FOUR MODULE BOOST INDUCTOR

CORE: MC1200-1B (METGLAS)
40 TURNS 4 MIL X 1 INCH COPPER FOIL
13 MIL AIRGAP
<table>
<thead>
<tr>
<th>COMPONENT PARAMETER</th>
<th>APPLIED VALUE</th>
<th>RATED VALUE</th>
<th>STRESS RATIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET CONTINUOUS DRAIN CURRENT</td>
<td>9 Amps</td>
<td>33 Amps</td>
<td>27%</td>
</tr>
<tr>
<td>PEAK TRANSISTOR DRAIN-TO-SOURCE VOLTAGE</td>
<td>120 Volts</td>
<td>200 Volts</td>
<td>62%</td>
</tr>
<tr>
<td>PEAK TRANSISTOR GATE VOLTAGE</td>
<td>10 Volts</td>
<td>±20 Volts</td>
<td>50%</td>
</tr>
<tr>
<td>PEAK DIODE CURRENT</td>
<td>9 Amps</td>
<td>20 Amps</td>
<td>45%</td>
</tr>
<tr>
<td>PEAK DIODE REVERSE VOLTAGE</td>
<td>60 Volts</td>
<td>150 Volts</td>
<td>40%</td>
</tr>
<tr>
<td>OUTPUT CAPACITOR VOLTAGE</td>
<td>120 Volts</td>
<td>200 Volts</td>
<td>60%</td>
</tr>
<tr>
<td>OUTPUT CAPACITOR RMS CURRENT</td>
<td>1.1 Amps</td>
<td>22 Amps</td>
<td>5%</td>
</tr>
</tbody>
</table>
VOLTAGE-FED, PUSH-PULL, AUTOTRANSFORMER, (VFPPAT) BATTERY DISCHARGER

HARDWARE DESIGN TOPIC LIST

DESIGN SPECIFICATIONS .............................................. 2.1.2.2
BASIC SCHEMATIC AND RESULTING WAVEFORMS ............. 2.1.2.3
SCHEMATIC WITH ACTUAL COMPONENTS ....................... 2.1.2.4
PRELIMINARY PARTS LIST ........................................ 2.1.2.5
COMPONENT STRESS EVALUATION ............................ 2.1.2.6
AUTOTRANSFORMER DESIGN ...................................... 2.1.2.7
INDUCTOR DESIGN ................................................... 2.1.2.8
VFPPAT
BATTERY DISCHARGER DESIGN SPECIFICATIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>64 VDC to 84 VDC</td>
</tr>
<tr>
<td>OUTPUT VOLTAGE RANGE</td>
<td>120 VDC + 4%</td>
</tr>
<tr>
<td>OUTPUT VOLTAGE RIPPLE</td>
<td>200 mV peak to peak</td>
</tr>
<tr>
<td>OUTPUT POWER RANGE</td>
<td>0 Watts to 1800 Watts</td>
</tr>
<tr>
<td>SWITCHING FREQUENCY</td>
<td>40 kHz</td>
</tr>
<tr>
<td>EFFICIENCY GOAL</td>
<td>96%</td>
</tr>
<tr>
<td>TRANSIENT PERFORMANCE</td>
<td></td>
</tr>
<tr>
<td>OUTPUT VOLTAGE PEAKING RANGE</td>
<td>115.2 VDC - 124.8 VDC</td>
</tr>
<tr>
<td>OUTPUT SETTLING TIME</td>
<td>10 msec</td>
</tr>
</tbody>
</table>
VOLTAGE-FED, PUSH-PULL WITH TAPPED AUTOTRANSFORMER (VFPPAT) CONVERTER

\[ V_{in} \]

\[ I_{S2} \]

\[ I_{L2} \]

\[ T \]

\[ C_{O} \]

\[ V_{S1} \]

\[ V_{S2} \]

\[ V_{ds1} \]

\[ V_{ds2} \]

\[ I_{L} \]

\[ I_{S1} \]

\[ I_{S2} \]

\[ I_{L1} \]

\[ I_{L2} \]

\[ 2.1.2.3 \]
VFPPAT SCHEMATIC WITH ACTUAL COMPONENTS

- **Vin**
- **±**
- **UC3706**
- **S1**
- **S2**
- **IRF350**
- **10 uF**
- **1N5816**
- **L 94uH**
- **5 uF**
- **Co 5 uF**
DISCHARGER POWER STAGE COMPONENTS

POWER SWITCH
- IRF350, INTERNATIONAL RECTIFIER
- TWO IN PARALLEL FOR HIGH EFFICIENCY
- \( R_{dson} = 250 \, \text{mOHM} \)

POWER DIODE
- 1N5816, UNITRODE
- \( T_{rr} = 35 \, \text{nS} \)

INDUCTOR
- MC0007 METGLAS CUT C-CORE, MAGNETICS, INC.
- \( L = 94 \, \text{uH} \)

INPUT AND OUTPUT CAPACITORS
- POLYPROPYLENE, ELECTRONIC CONCEPTS, INC.
- LOW ESR
- LIGHTWEIGHT

DRIVER IC
- UC3706, DUAL OUTPUT DRIVER, UNITRODE
- PEAK OUTPUT CURRENT = 1.5 A
VFPPAT MAXIMUM COMPONENT STRESS EVALUATION

<table>
<thead>
<tr>
<th>STRESS PARAMETER</th>
<th>APPLIED VALUE</th>
<th>RATED VALUE</th>
<th>PERCENT USAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEAK TRANSISTOR DRAIN CURRENT*</td>
<td>8.3 Amps</td>
<td>60 Amps</td>
<td>14%</td>
</tr>
<tr>
<td>PEAK TRANSISTOR DRAIN-TO-SOURCE VOLTAGE</td>
<td>168 Volts</td>
<td>400 Volts</td>
<td>42%</td>
</tr>
<tr>
<td>PEAK TRANSISTOR GATE VOLTAGE</td>
<td>10 Volts</td>
<td>±20 Volts</td>
<td>50%</td>
</tr>
<tr>
<td>PEAK DIODE CURRENT*</td>
<td>8.15 Amps</td>
<td>20 Amps</td>
<td>41%</td>
</tr>
<tr>
<td>PEAK DIODE REVERSE VOLTAGE*</td>
<td>82 Volts</td>
<td>150 Volts</td>
<td>55%</td>
</tr>
<tr>
<td>OUTPUT CAPACITOR VOLTAGE</td>
<td>120 Volts</td>
<td>200 Volts</td>
<td>60%</td>
</tr>
<tr>
<td>OUTPUT RMS CURRENT*</td>
<td>0.4 Amps</td>
<td>22.5 Amps</td>
<td>2%</td>
</tr>
<tr>
<td>INPUT CAPACITOR VOLTAGE</td>
<td>84 Volts</td>
<td>200 Volts</td>
<td>42%</td>
</tr>
<tr>
<td>INPUT CAPACITOR RMS CURRENT*</td>
<td>3.25 Amps</td>
<td>15 Amps</td>
<td>25%</td>
</tr>
</tbody>
</table>

* 50% DIVISION OF PARAMETER ASSUMED
** APPLIED VALUES PREDICTED USING A SPREAD SHEET PROGRAM
AUTOTRANSFORMER DESIGN

Lower Winding

Upper Winding

Bobbin

CORE: EE4242/15 TDK H7C1
20 TURNS 3 MIL X 1.1 INCH COPPER FOIL
VFPPAT INDUCTOR DESIGN

CORE: MC0007-1B (METGLAS)
32 TURNS 4 MIL X 1 INCH COPPER FOIL
24 MIL AIRGAP
## Battery Charger Design Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>120 Volts +/- 4%</td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>53 - 84 Volts</td>
</tr>
<tr>
<td>Duty Ratio</td>
<td>44% to 70%</td>
</tr>
<tr>
<td>Topology</td>
<td>Single Phase Buck</td>
</tr>
<tr>
<td>Charge Current Range</td>
<td>1 to 20 Amps</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>80 KHz</td>
</tr>
<tr>
<td>Estimated Efficiency</td>
<td>95%</td>
</tr>
<tr>
<td>Control</td>
<td>Bus Voltage / Charge Current</td>
</tr>
</tbody>
</table>
BATTERY CHARGER SCHEMATIC

IRFP250
X 4

IN5816
.025

Fsw = 80Khz

UC3706
DRIVER
ICs

+15V

+12V

BUS VOLTAGE
ERROR SIGNAL
FROM
MODE CONTROLLER

I REF
FOR CHARGE
CURRENT
REGULATION

UC1825
PWM
IC

out A
out B

DRIVE
CIRCUIT
X 4

DRIVE
TRANSFORMER
X 4

Ki
CHARGER POWER STAGE COMPONENTS

POWER SWITCH
- IRFP250 MOSFET, INTERNATIONAL RECTIFIER
- FOUR IN PARALLEL FOR HIGH EFFICIENCY
- $R_{\text{dson}} = 85 \text{ mOHM}$

POWER DIODE
- 1N5816, UNITRODE
- TWO IN PARALLEL
- $T_{rr} = 35 \text{ nS}$

INDUCTOR
- METGLAS CUT C-CORE, MAGNETICS, INC.
- $L = 46 \mu\text{H}$

INPUT CAPACITOR
- POLYPROPYLENE, ELECTRONIC CONCEPTS, INC.
- LOW ESR
- LIGHTWEIGHT

INPUT FILTER
- COMMON TO DISCHARGER
# BATTERY CHARGER STRESS ANALYSIS

<table>
<thead>
<tr>
<th>COMPONENT PARAMETER</th>
<th>APPLIED VALUE</th>
<th>RATED VALUE</th>
<th>STRESS RATIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET CONTINUOUS DRAIN CURRENT</td>
<td>5 Amps</td>
<td>33 Amps</td>
<td>15%</td>
</tr>
<tr>
<td>PEAK TRANSISTOR DRAIN-TO-SOURCE VOLTAGE</td>
<td>120 Volts</td>
<td>200 Volts</td>
<td>60%</td>
</tr>
<tr>
<td>PEAK TRANSISTOR GATE VOLTAGE</td>
<td>+10 Volts</td>
<td>+20 Volts</td>
<td>50%</td>
</tr>
<tr>
<td>RMS DIODE CURRENT</td>
<td>7.5 Amps</td>
<td>20 Amps</td>
<td>38%</td>
</tr>
<tr>
<td>PEAK DIODE REVERSE VOLTAGE</td>
<td>120 Volts</td>
<td>150 Volts</td>
<td>80%</td>
</tr>
<tr>
<td>INPUT CAPACITOR VOLTAGE</td>
<td>120 Volts</td>
<td>200 Volts</td>
<td>60%</td>
</tr>
<tr>
<td>INPUT CAPACITOR RMS CURRENT</td>
<td>4.2 Amps</td>
<td>15 Amps</td>
<td>28%</td>
</tr>
</tbody>
</table>
CHARGER POWER INDUCTOR DESIGN

MATERIAL : METGLAS
- HIGH Bsat ALLOWS SMALL INDUCTOR SIZE
- LOW LOSS
- 1 MIL LAMINATION : HIGH RESISTIVITY & LOW EDDY CURRENT LOSS
- HIGH PERMEABILITY
- LOW Bsat DRIFT OVER TEMPERATURE

CONDUCTOR AND INSULATION
- COPPER FOIL : 5 MIL THICKNESS
  * HIGH WINDOW UTILIZATION
  * LOW SKIN EFFECT LOSS
  * LOW PROXIMITY LOSS
- INSULATION : 2 MIL KAPTON TAPE

CORE
- MAGNETICS, INC. MC1603 CUT C-CORE
- 14 MIL GAP FOR L = 46 uH
- DISADVANTAGE : GAP LOSS AND PROXIMITY LOSSES

DESIGN
- SPREAD SHEET PROGRAM
- AREA PRODUCT APPROACH
- TRADE-OFFS : LOSSES AND WEIGHT
- CONSIDERATIONS : STANDARD FOIL AND TAPE DIMENSIONS
CHARGER POWER INDUCTOR DESIGN

CORE: MC1603-1B (METGLAS)
21 TURNS COPPER FOIL (5 MIL X 1 INCH)
14 MIL AIR GAP (PER LEG)
CHARGER PWM AND DRIVE CIRCUITS

ISOLATED GATE DRIVE

DRIVE TRANSFORMER
- CORE RESET
- FERRITE TOROID
- 1:1 TURNS RATIO FOR HIGH COUPLING

FOUR SEPARATE DRIVE CIRCUITS
- MOSFET TURN-ON CURRENT SHARING
- ELIMINATING PARASITIC OSCILLATIONS

UNITRODE UC3706 DRIVER CHIPS
- I_{peak} = 1.5 AMPS
- SWITCHING SPEED

UNITRODE UC1825 PWM IC
CHARGER REGULATION CIRCUITS

CHARGE CURRENT REGULATION

- RESISTIVE CURRENT SENSING
  * 25 mΩHM IN SERIES WITH THE BATTERY
  * ADVANTAGE : SIMPLICITY
  * DISADVANTAGE : LOSSES
    10 A CHARGE = 2.5W LOSS
    20 A CHARGE = 10W LOSS
- ADJUSTABLE CHARGE CURRENT REFERENCE

BUS VOLTAGE REGULATION

- IMMEDIATELY AFTER ECLIPSE
- DURATION
- ERROR SIGNAL FROM MODE CONTROLLER (PCU)

CURRENT/VOLTAGE MODE SELECTION

- DIODE OR-ING CIRCUIT
- CHARGE CURRENT REFERENCE LEVEL
- MODE CONTROLLER THRESHOLDS
3. DISCUSSION
DISCUSSION

1) BATTERY CHARGING CURRENT
2) SOLAR ARRAY CHARACTERISTICS
3) BATTERY RIPPLE CURRENT SPEC
4) MINIMUM BATTERY VOLTAGE
5) BIDIRECTIONAL CONVERTER ??
6) APPROVED PARTS
7) SOLAR ARRAY SIMULATOR
8) MULTI-MODULE CHARGER ??
9) SERIES DIODES
10) V/T LIMIT