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# Interim Service ISDN Satellite (ISIS) Hardware Experiment Design

for  
Advanced ISDN Satellite Design  
and Experiments

28 February 1992

(NASA-CR-186943) INTERIM SERVICE ISDN  
SATELLITE (ISIS) HARDWARE EXPERIMENT DESIGN  
FOR ADVANCED ISDN SATELLITE DESIGN AND  
EXPERIMENTS Report, 1 May 1991 - 28 Feb.  
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Task Completion Report  
NASA SCAR Contract NASW-4520, 13 Sep 1990

Prepared by  
Gerard R. Pepin  
GTE/Government Systems  
15000 Conference Center Drive  
Chantilly, Virginia 22021-3808

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# SECTION 1

## INTRODUCTION

### 1.1 Background

The objectives of this element of the NASA Satellite Communications Applications Research (SCAR) Program are to develop new advanced on-board satellite capabilities that will enable the provision of new services, namely interim and full Integrated Services Digital Network (ISDN) services via satellite and to provide a system analysis of futuristic satellite communications concepts, namely broadband services via satellite.

This aspect of the NASA SCAR Program provides a research and development effort to:

- 1) develop basic technologies and concepts to use the on-board processing and switching capabilities of advanced satellites that will enable the provision of interim and full ISDN services and
- 2) provide a systems and requirements analysis of future satellite communications concepts based on a new generation of broadband switching and processing satellites.

These objectives will be achieved in part by designing and implementing hardware to interface between terrestrial ISDN networks and a communications satellite, possibly with the Advanced Communications Technology Satellite (ACTS).

### 1.2 Scope

This task completion report documents the ISDN Satellite Terminal Adapter (ISTA) design associated with the Interim Services ISDN Satellite (ISIS) architecture. The process and methodology is applicable to the ISIS system as described in Figure 1.2-1, "NASA/SCAR Approaches for Advanced ISDN Satellites". The ISIS Network design represents satellite systems like the Advanced Communications Technology Satellite (ACTS) orbiting switch.

The ACTS will be controlled by a Master Ground Station (MGS) shown in Figure 1.2-2, "Closed User-Oriented Scenario". A user of the ACTS satellite orbiting switch requests services from the MGS, a combination of the NASA Ground Station (NGS) and the Master Control Station (MCS). The MGS, in turn, commands the satellite to switch the appropriate communications channel.

The ultimate aim of this element of the SCAR Program is to move these MGS functions on-board the next generation ISDN communications satellite as shown in Figure 1.2-3, "Advanced ISDN Satellite". The technical and operational parameters for the advanced ISDN communications satellite design will be obtained from an engineering software model of the major subsystems of the ISDN communications satellite architecture. Discrete event simulation experiments will be performed with the model using various traffic scenarios, design parameters, and operational procedures. The data from these simulations will be analyzed using the NASA SCAR performance measures discussed in previous reports. Data from hardware experiments will be used to verify the model results.

In order to associate modeling and simulation results with real-world data, some ISDN hardware design and implementation were undertaken. Hardware development was limited to the ISIS approach. Figure 1.2-4, "ISIS System Configuration for Remote Access",



### ISIS

Interim Service  
ISDN Satellite

### FSIS

Full Service  
ISDN Satellite

### BSIS

Broadband Service  
ISDN Satellite

- ACTS-like Satellite Design and Transponder
- Provide Narrowband ISDN Services (Basic Rate Access)
- Provide remote access ISDN Satellite Terminals using ISDN Satellite Terminal Adapter
- Will use D channel signaling but NOT SS7
- Will use ACTS call control and Baseband Switching Architecture

- New ISDN Satellite Design with onboard Class 5 Switch and SS7 Network Interface
- Provide Narrowband ISDN Services (Basic/Primary Rate Access)
- Provide nationwide single hop single CONUS earth coverage antenna satellite link connectivity to an interexchange node for ISDN Satellite Terminals (up to 10,000 ISAT)
- Will use D channel signaling with SS7
- Will use SS7 call control with minimum call set-up time and efficient satellite BW utilization

- Advanced ISDN Satellite Design with onboard Class 5 Switch and SS7 Network Interface and layered protocol
- Provide Broadband ISDN Services (Primary Rate Access)
- Provide nationwide single hop, multiple high gain hopping beams, forward error control, optical processing, and "zero delay" satellite link interexchange node connectivity
- Will use D channel signaling with SS7
- Will center design around ATM fast packet switching techniques

Figure 1.2-1 NASA/SCAR Approaches for Advanced ISDN Satellites

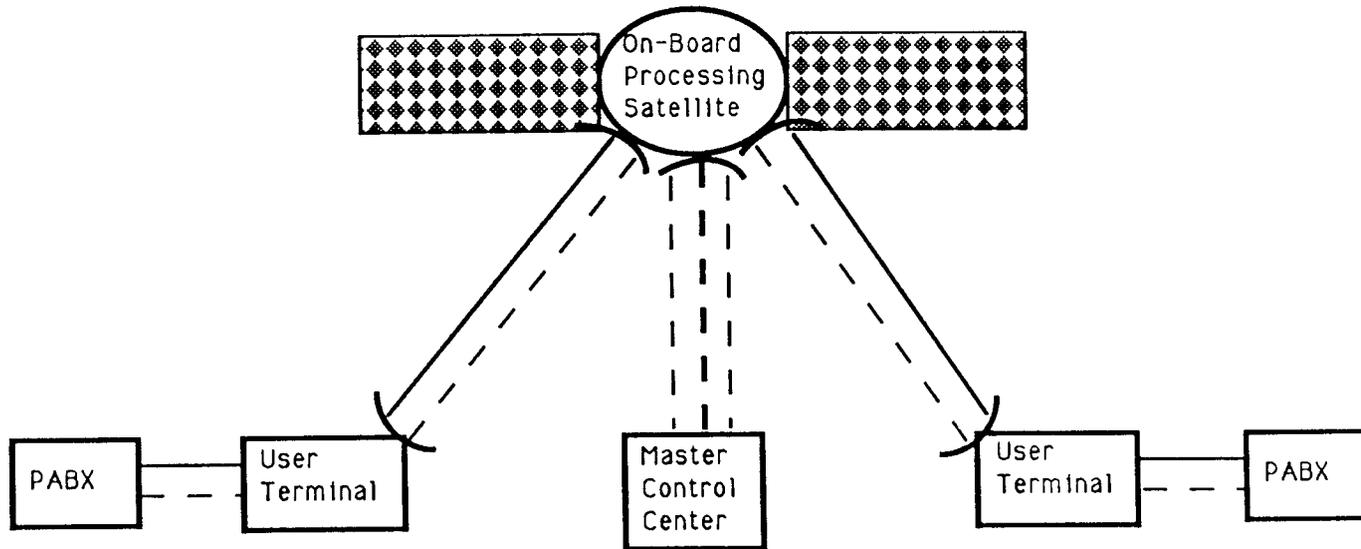


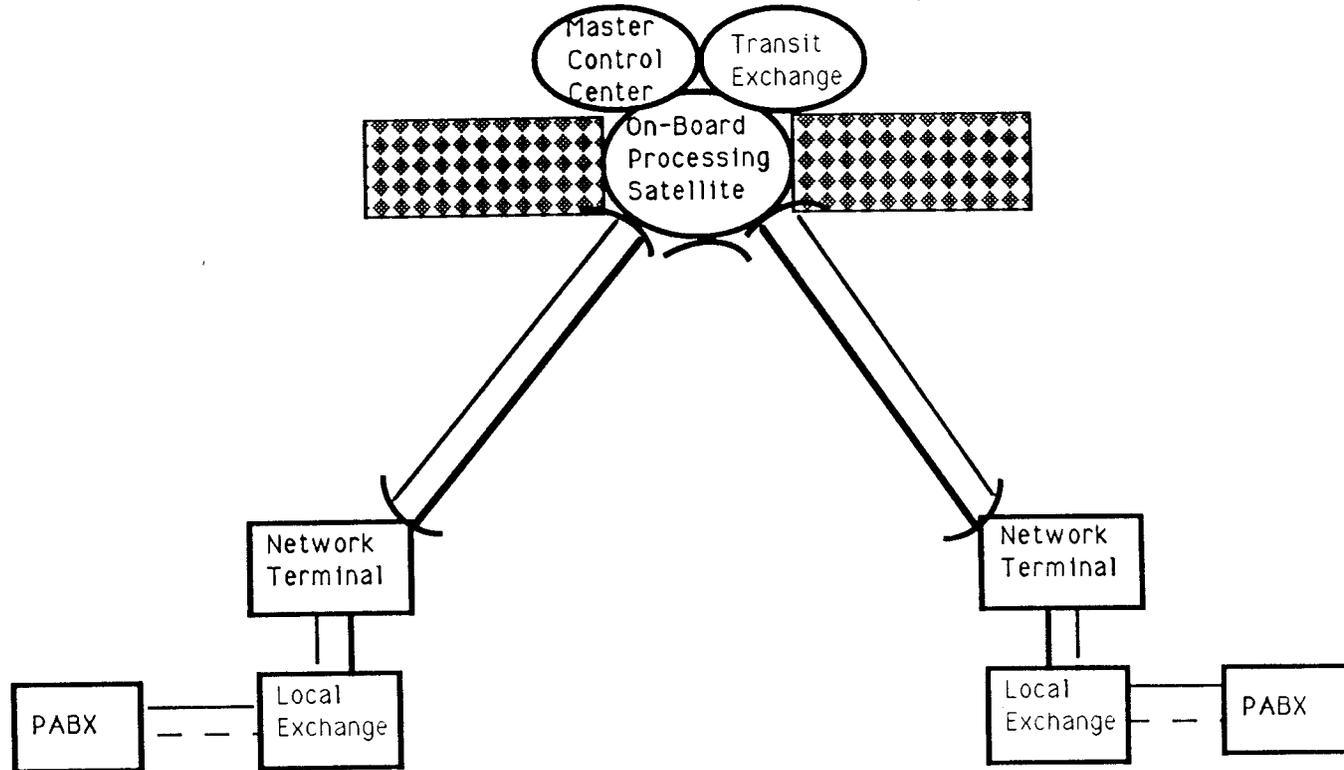
Figure 1.2 -2 Closed User-Oriented Scenario

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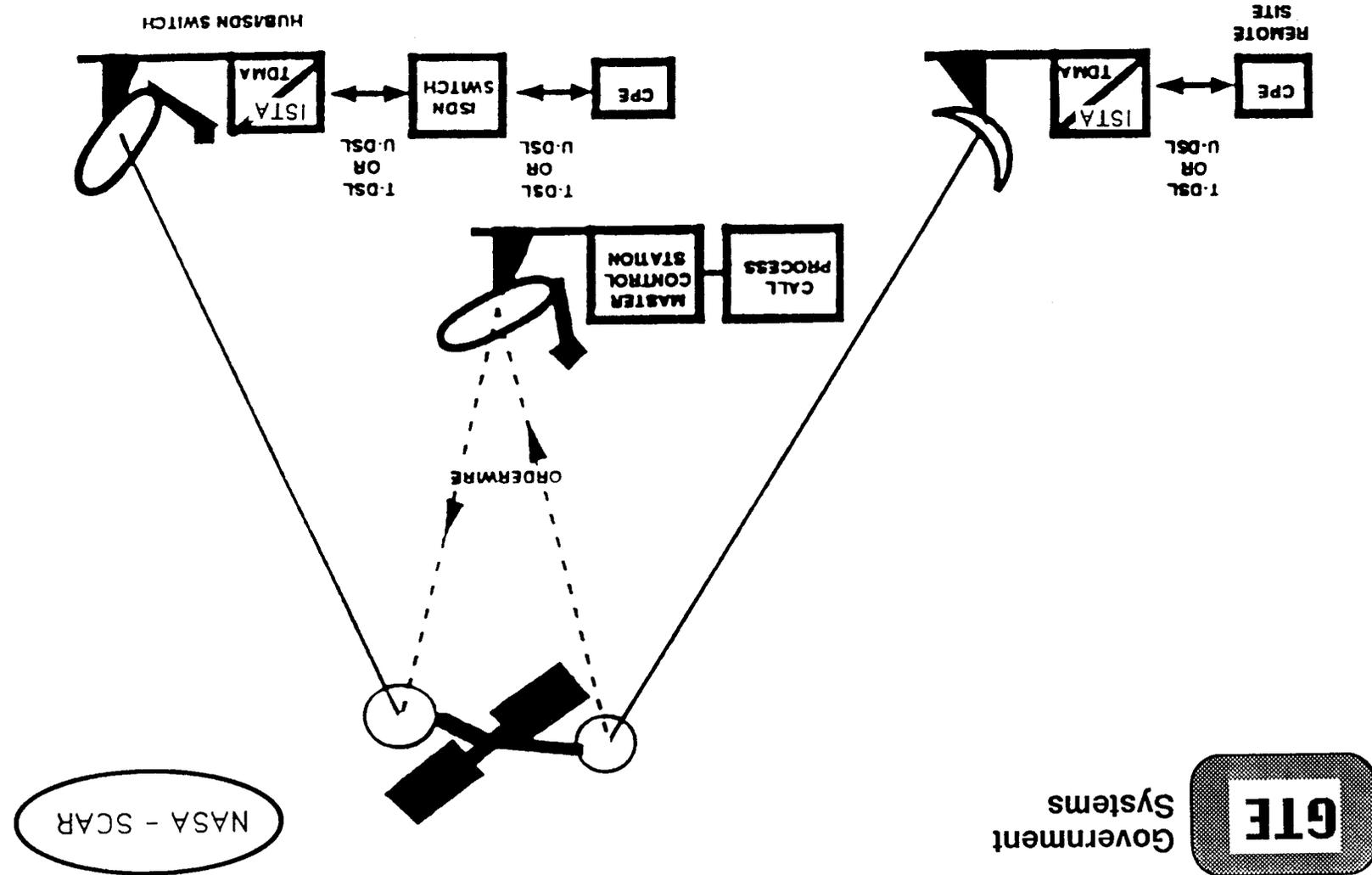


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Figure 1.2-3 Advanced ISDN Satellite

Figure 1.2-4 ISIS System Configuration for Remote Access

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illustrates the ISIS system configuration. The ISDN Satellite Terminal Adapter (ISTA) was designed to interface with the Type 1 network termination (NT1) at the user site via the ISDN U-interface and the line termination (LT) unit of the ISDN switch.

### **1.3 Document Overview**

This task completion report begins by describing the objectives of the ISIS hardware experiment in terms related to a communications satellite connected to an ISDN terrestrial link. A specific application of sending compressed video from NASA Lewis in Cleveland, Ohio to the GTE #5ESS switch in Chantilly, Virginia is postulated as a context for discussions for the design of the ISTA.

The ISTA design is decomposed into several detailed views identifying the design refinements along the way. These design views are described in terms of their associated hardware, the chip set, and the software design. The ISDN basic access superframe structure and the satellite link access HLDC Frame Structure are described down to the bit level.

The ISTA activation and deactivation protocols for both the exchange and terminal equipment are presented in the context of end-to-end Z-diagrams. The relationship between the 68000 Development System and the ISTA is shown and a detail circuit design down to the chip pin connections is provided.

## SECTION 2

### POTENTIAL ISDN HARDWARE EXPERIMENTS

#### 2.1 ISDN Hardware Experiment Objective

The objective of the ISDN Hardware Experiment is to demonstrate the feasibility of using typical communications satellites to connect ISDN users to ISDN exchanges via a non-ISDN Communications Satellite Link. Figure 2.1-1, "ISIS Hardware Development" shows the top view of a User Terminal connected to a #5ESS Switch via line termination and network termination. The ISTA converts the ISDN Basic Access Superframe Structure into Satellite Link Access HDLC Frame Structure suitable for transmission via satellite. The ISTA design must also be capable of reversing the process on the network side of the satellite connection.

#### 2.2 ISDN Typical Basic Access - Terrestrial/Satellite Links

Figure 2.2-1, "ISDN Typical Terrestrial/Satellite Links", shows customer premises connected to an ISDN switch at a local telephone exchange by a U-interface with 3.5 miles of twisted pair copper wire. This connection between the NT1 unit and the line termination (LT) provides the user with all the access for basic rate ISDN services.

Replacing this copper wire with a satellite link requires matching both the NT1 and the LT termination in terms of bit transfer, protocol timing and data rate adaption related to CCITT time-out values. Both the satellite and the corresponding ground system must be capable of supporting the typical ISDN 160Kbps basic access rate. The ISTA ensures that the protocol and user data conversions permit the timely support of the ISDN protocol and data.

#### 2.3 Potential Application of ISTA

One of the postulated demonstrations of the ISTAs is to provide ISDN connectivity between the NASA Lewis Complex and the GTE #5ESS at Dulles International Airport. Figure 2.3-1, "Potential ISDN Satellite Connectivity", shows a compressed video image at NASA Lewis, Cleveland, Ohio being transmitted to GTE Chantilly, Virginia via ISTA equipped ground terminals. From GTE-Chantilly the ISDN frames pass through a U-interface in the Brite Channel Bank across 10 miles of fiber optic link to a Brite channel bank in the GTE Dulles #5ESS ISDN Switch. Tests of throughput and response-time can be made using this configuration or other similar configuration. The principal message for this report is that the ISTA provides the necessary conversion between the ISDN world and the satellite world.

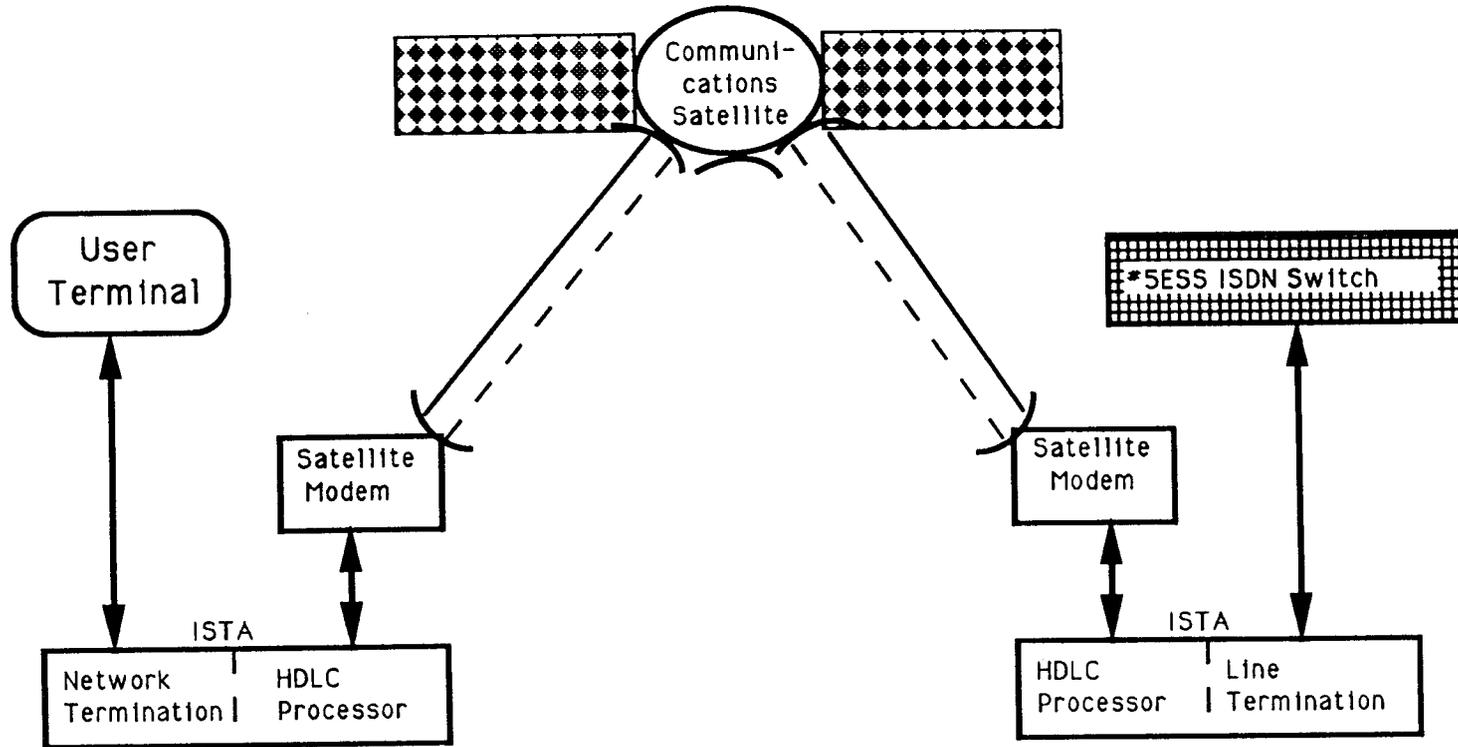


Figure 2.1-1 ISIS Hardware Development

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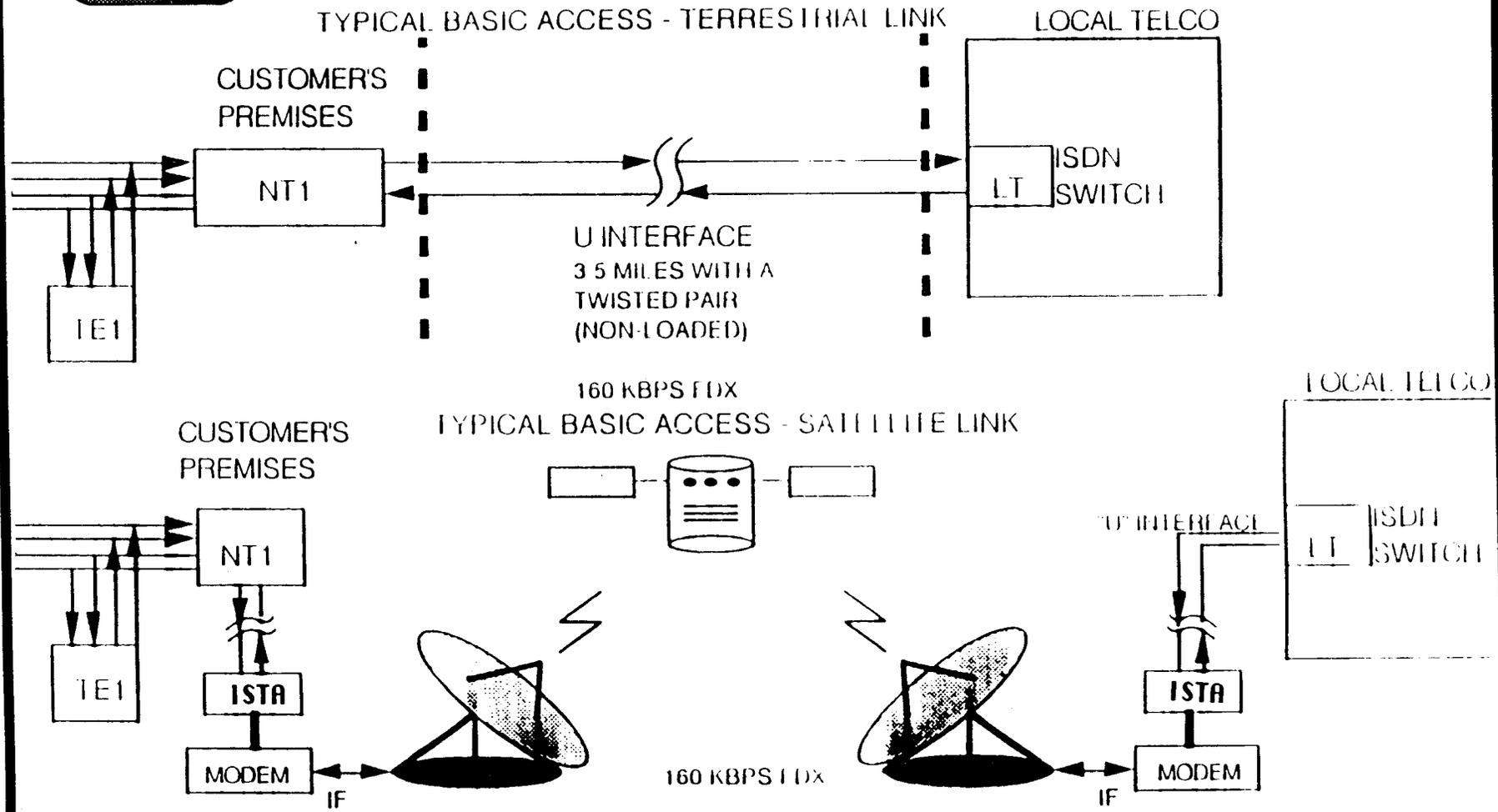


Figure 2.2-1 ISDN Typical Terrestrial/Satellite Links

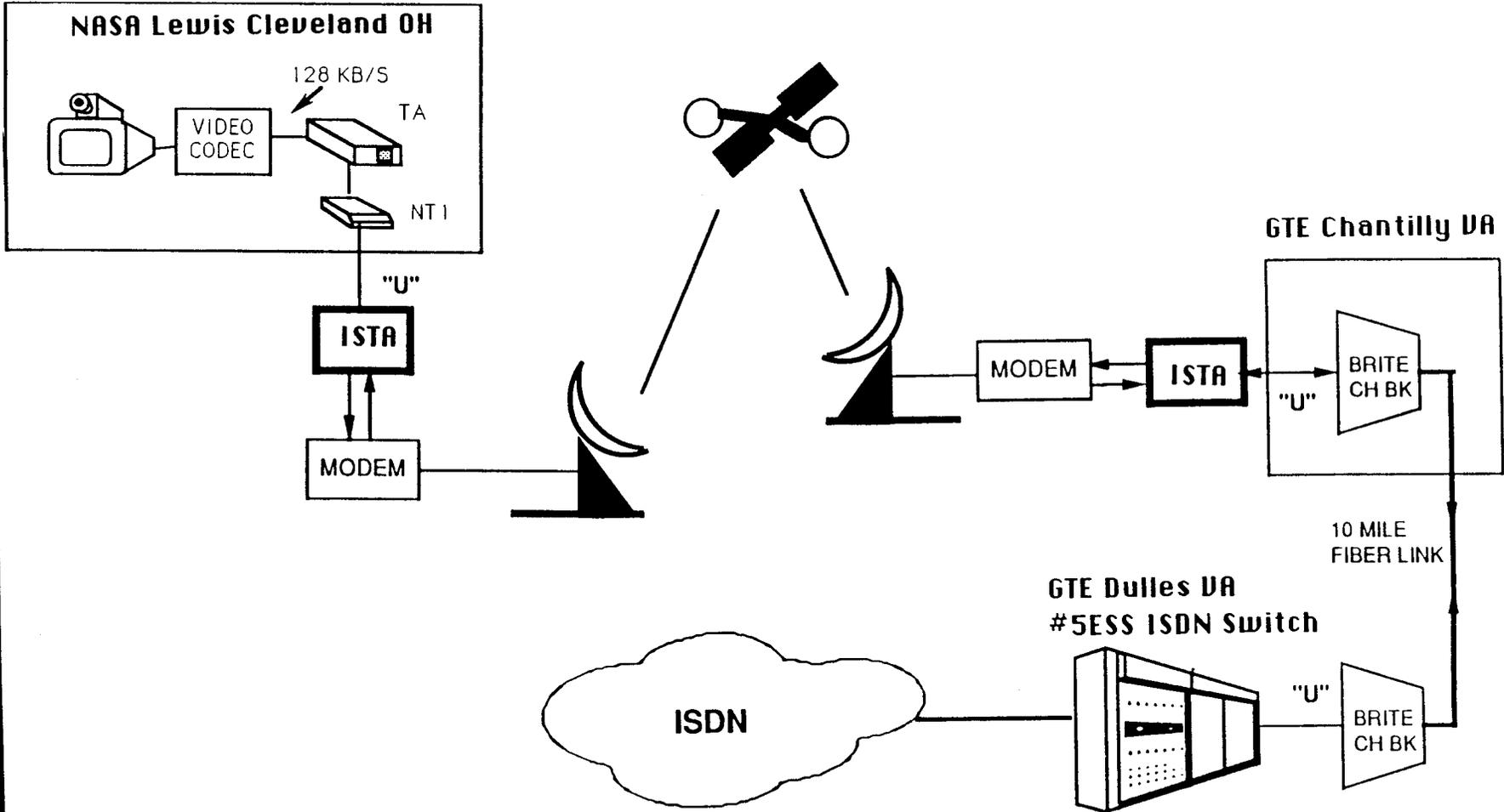
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Figure 2.3-1 Potential ISDN Satellite Connectivity

## SECTION 3

### ISTA HARDWARE DESIGN

#### 3.1 ISTA Top View

At the top level, the ISTA interfaces the U-interface with the V.35 interface at the 160Kbps rate. Figure 3.1-1, "ISDN Satellite Terminal Adapter (ISTA)", shows the ISTA between the user terminal and the Low Bit Rate Terminal (LBR-2). The expanded view at the LT and HDLC level, and implementation view using the MC145472 and the MC68302 chip set are discussed in subsequent sections.

#### 3.2 ISTA Functional Block Diagram

Figure 3.2-1, "ISTA Functional Block Diagram", shows both the CPE side and the switch side of the ISTA. For the CPE side the U-interface connects the user NT1 to a line terminal that is connected to a HDLC processor that converts the basic access frames to the V.35 frames for the communications satellite. On the switch side of the ISTA the V.35 frames are converted by the HDLC processor to provide ISDN basic access frames between the NT unit and the LT unit of the #5ESS ISDN Switch.

#### 3.3 ISTA Frame Structures

Each side of the ISTA has its unique frame structure to accommodate their respective protocols. Figure 3.3-1, "ISDN Frame Structures", shows both frame structures. The ISDN Basic Access Superframe Structure uses a format of 1920 bits. The transmission across the U-interface is organized into groups of eight 2B1Q frames, called superframes. A frame consists of three fields:

*Synchronization word (SW)*: Used for physical layer synchronization and frame alignment. It consists of a pattern of 18 bits.

*User Data (12(2B+D))*: 12 groups of 2B and D information. Each group contains 8 B1 bits, 8 B2 bits, and 2 D bits resulting in 216 bits of user data.

*Overhead Data*: These bits are used for physical channel maintenance, error detection and power status. A total of 6 bits are used per frame.

As shown in Fig 3.3-1 the inverted synchronization word (ISW) identifies the first frame in the superframe; it is a pattern of 18 bits that is merely the inverse of the normal synchronization word. The superframe organizes the 6 overhead bits of each frame into a block of 48 bits

The satellite link access HDLC frame structure consists of the same 1920 bits apportioned in a different manner. The eight frames of user information are combined into a single frame of 1728 bits for the 96(2B+D). The overhead bits are collected into Flag, Control, CRC, M-bits and Fill. The fill is used to perform rate adaption between the terrestrial and satellite protocols.

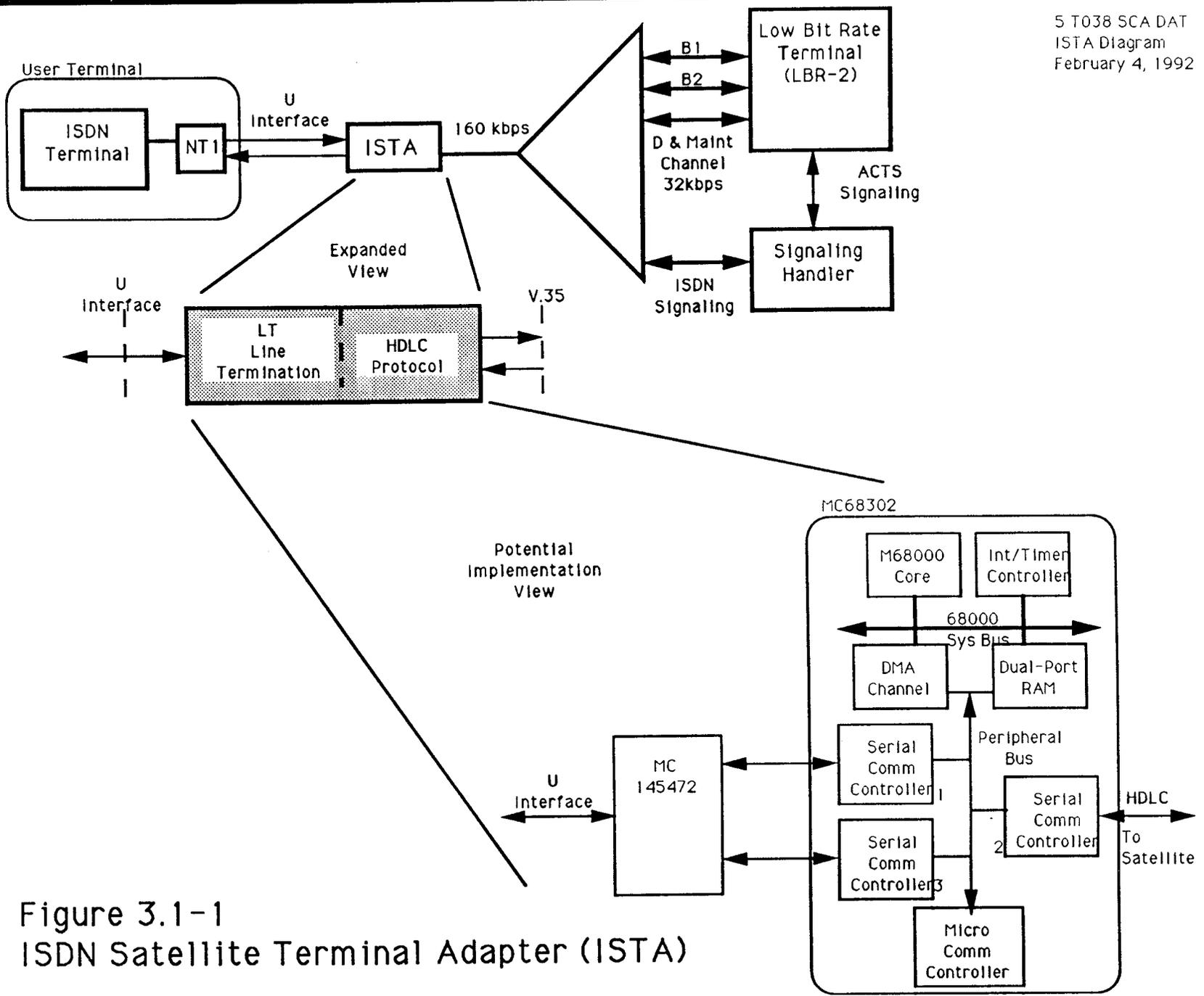


Figure 3.1-1  
ISDN Satellite Terminal Adapter (ISTA)

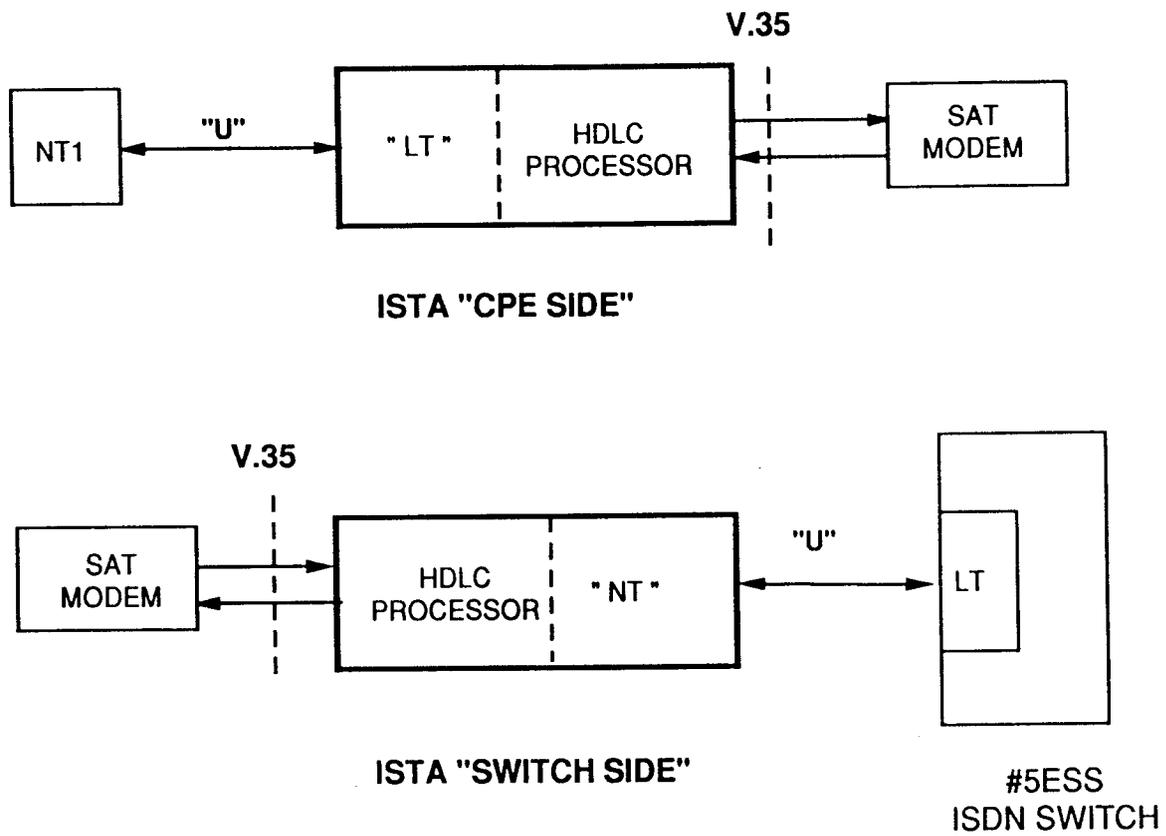
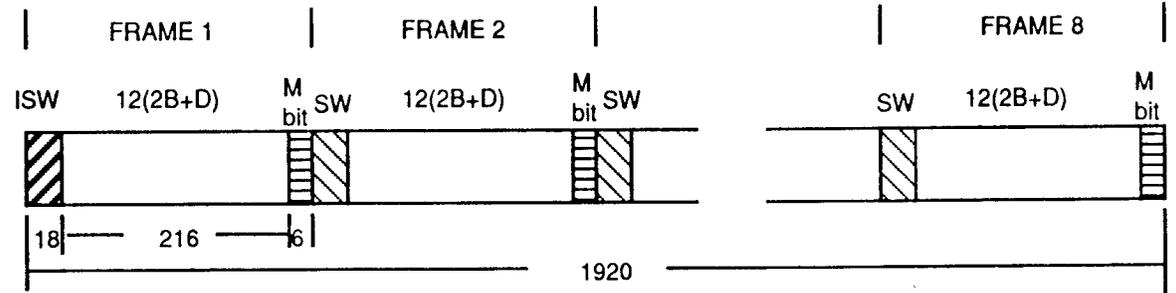


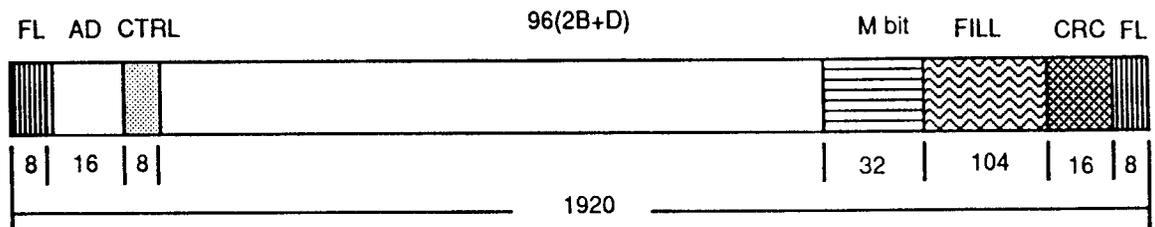
Figure 3.2-1 ISTA Functional Block Diagram

3-3



B = 8 bits  
D = 2 bits

**ISDN Basic Access Superframe Structure**



Data rate = 1920 bit/frame x frames/sec  
 = 1920 x 1/0.012 sec  
 = 160,000 bits/sec

**Satellite Link Access HDLC Frame Structure**

Figure 3.3-1 ISDN Frame Structures

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### 3.4 ISTA Chip Set

The ISTA design shown in Figure 3.4-1, "ISTA Hardware Block Diagram", includes using the MC145472 ISDN U-Interface Transceiver, the MC68302 Multi-Protocol Processor and added RAM/ROM for suitable memory. The serial communication controllers on the MC68302 are used to drive the ISDB U-interface transceiver. The third serial communications controller connected to the same MC68302 peripheral bus as the other two communications controllers provides HDLC frames to the V.35 line Tx/Rx function.

This same ISTA design is capable of supporting the CPE side and the switch side of the interface. To synchronize with satellite timing the the satellite clock pulses are used in a phase lock loop to control the ISDN U-interface transceiver when the ISTA is used on the switch side - Switch to Satellite interface. The same loop timing switch is open when the ISTA is used on the CPE side - NT1 to Satellite interface.

### 3.5 ISTA Software

The ISTA design uses off-the-shelf chip sets that require principally pin to pin circuit connectivity. These chips, however, rely on digital instructions to perform their transmission, reception, and protocol frame conversion processes. Figure 3.5-1, "ISTA Software Flow Diagram", depicts the top level flow diagram for the ISTA software. After the sequential initialization of the MC68302, the HDLC Comm, the 2B+D Comm and the SCP the software selects the the U interface initialization depending on the ISTA switch setting. After all these initialization on both ISTAs the respective software starts the appropriate activation procedure and waits for an interrupt.

These interrupt service routines include:

- \* M4 Bits Processing
- \* Activation/Deactivation
- \* Embedded Operation Channel Processing
- \* IDL "2B+D" Tx and Rx Buffer Processing
- \* HDLC Tx and Rx Buffer Processing

The ISTA software will be developed on a system like the 68000 Development System using the MC145494 Evaluation Kit and ADS302 Development System shown in Figure 3.5-2, "ISDN Satellite Terminal Adapter Development System".



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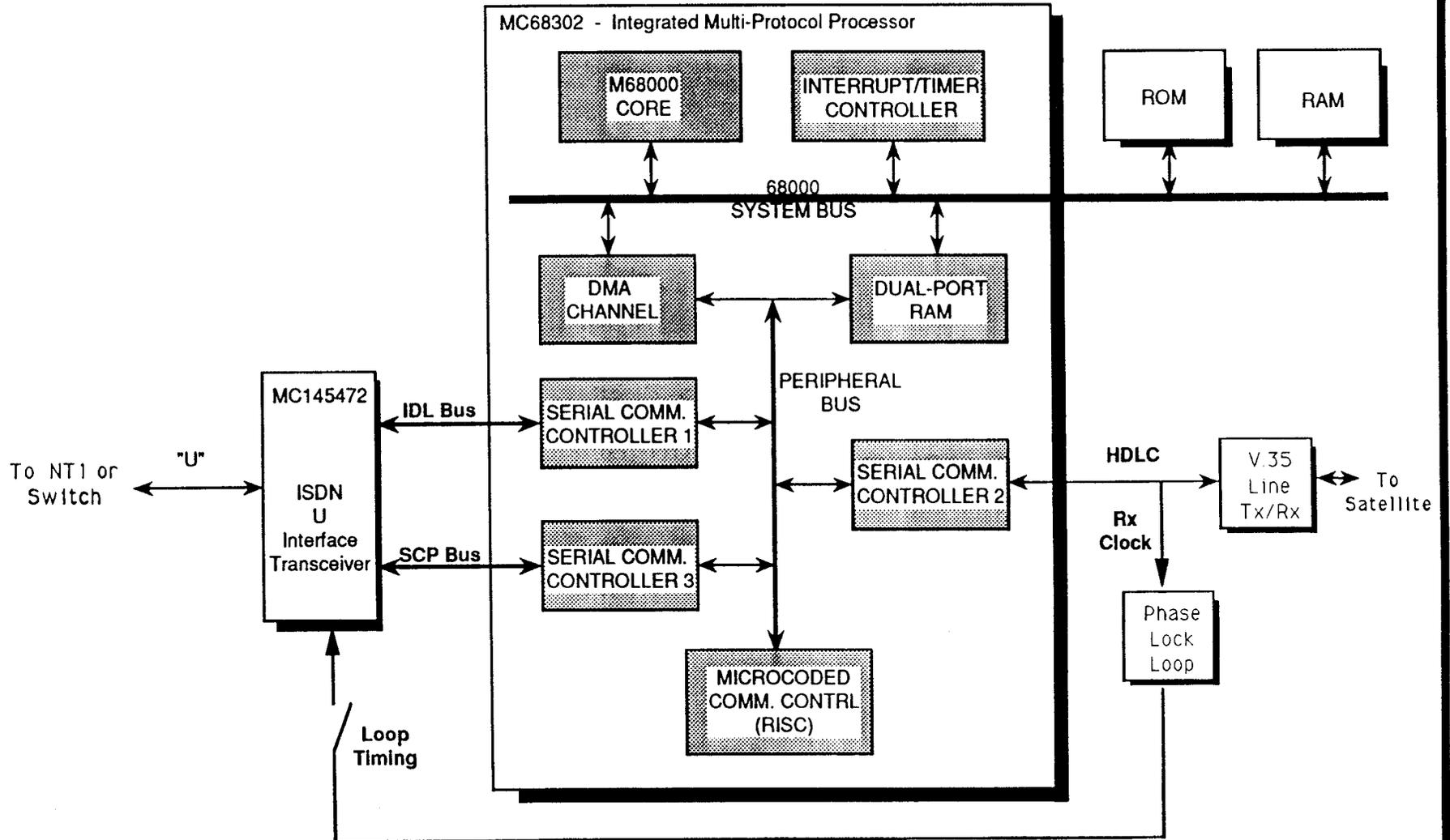


Figure 3.4-1 ISTA Hardware Block Diagram

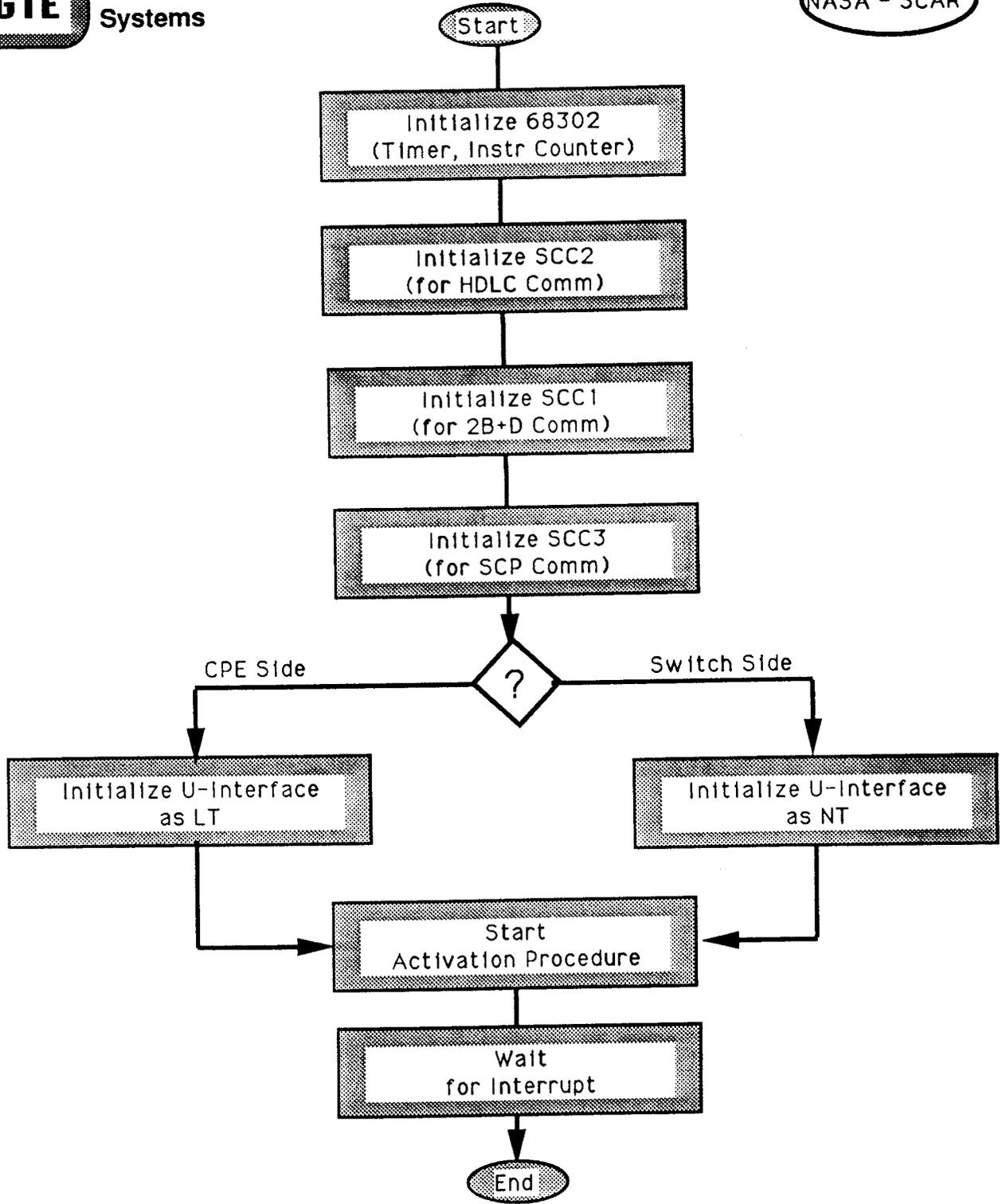
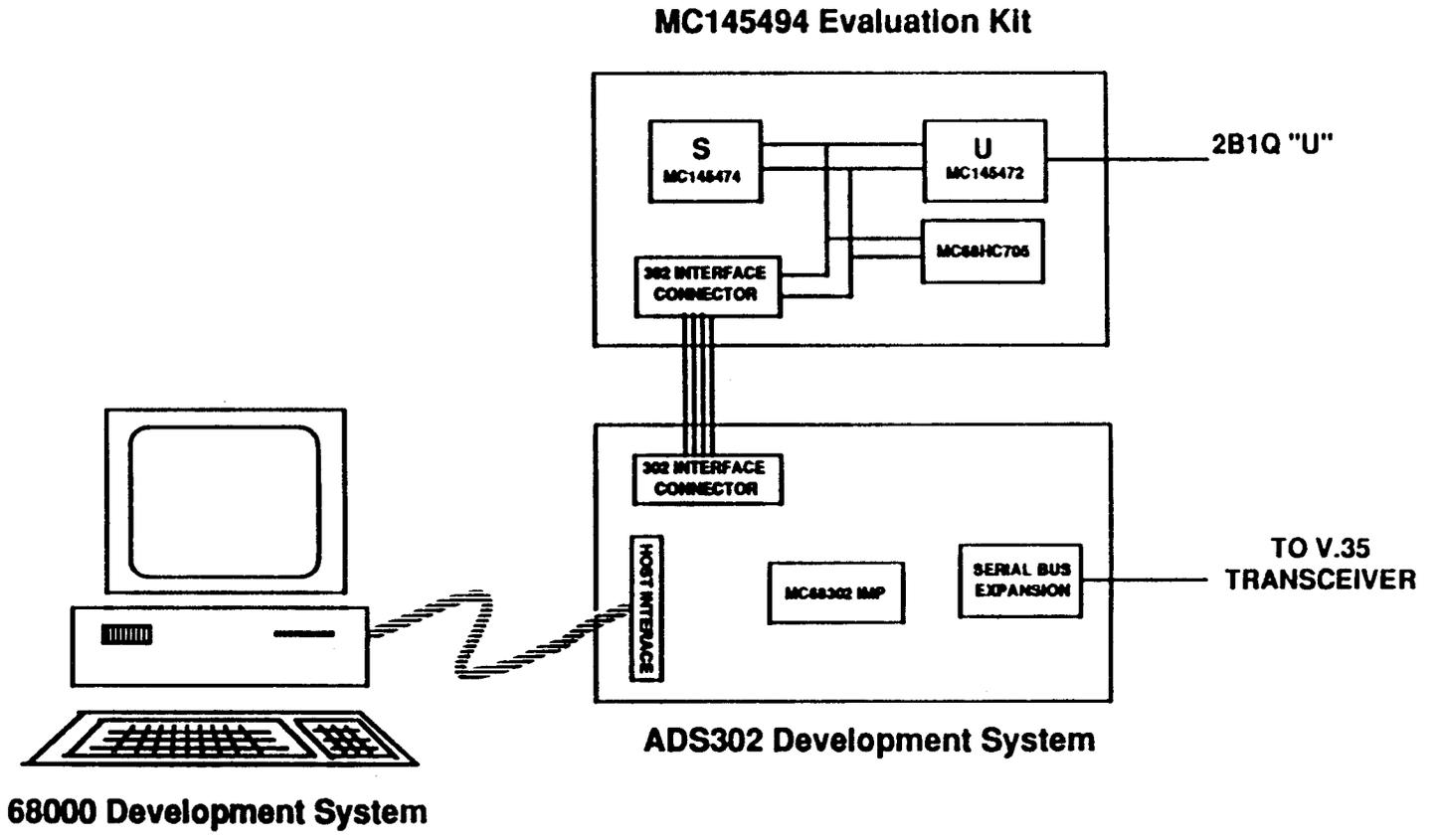


Figure 3.5-1 ISTA Software Flow Diagram



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## SECTION 4

### ISTA Activation Diagrams

#### 4.1 Introduction

Before meaningful ISDN communication services can be provided through the satellite, each ISTA must be activated with the proper protocol sequence in conjunction with its counter part ISTA at the other end. In that context, activations can be viewed as being initiated by either the exchange or initiated by the equipment.

#### 4.2 ISTA Activation Initiated by the Exchange

Figure 4.2-1, "Total Activation Initiated by the Exchange", shows the sequence of protocols initiated by the exchange and the responses that will permit the ultimate communication of ISDN user traffic. The Z-chart of these protocol sequences is aligned with a top level block diagram of the satellite connectivity between the ISDN switch and the terminal equipment (TE). The exchange begins the activation process from its null state when it receives an activation request (AR) protocol message. The switch LT changes its state to activation proceeding (AP) and sends an activation request to its local ISTA, NT>ISTA, which immediately sets its state to the AP state. The AR protocol message received by the NT section of the ISTA converts the digital AR message into control bits in the HDLC frames that are continually being sent through the communications satellite to the other ISTA, SAT>LT, and sets its state to AP. The NT>SAT ISTA begins the exchange of synchronizing information with the LT at the Exchange.

Meanwhile the HDLC protocols with the set control bits are received by the SAT>LT ISTA which sets its state to AP and begin exchanging synchronizing information with the user terminal's NT. That NT also sets its state to AP. The superframe synchronization (SS) on the each side of the satellite results in both the exchange-LT and the equipment -NT being set to the SS along with their corresponding ISTAs. The user-NT sends an Info2 message indicating it is ready to receive user data as Info3. The proper reception of Info3 sets the states of all the interfaces to activated (act=1) along the way and an activation indication (AI) state is entered. The timely response to an Info3 message by an Info4 message keeps all the interfaces synchronized for continuous information flow.

#### 4.3 ISTA Activation Initiated by the Terminal Equipment

Figure 4.3-1, "Total Activation Initiated by Terminal Equipment", shows the sequence of protocols initiated by the exchange and the responses that will permit the ultimate communication of ISDN user traffic. The Z-chart of these protocol sequences is aligned with a top level block diagram of the satellite connectivity between the ISDN switch and the terminal equipment (TE). The terminal equipment begins the activation process from its null state by receiving an activation request (AR) protocol message in the form of Info1 from the terminal equipment. The protocol exchange process continues in the same fashion as described above until all interface states are in the activated state (act=1), signaling activation indication (AI), and a superframe synchronized flow of information is flowing in terms of Info3 and Info4.

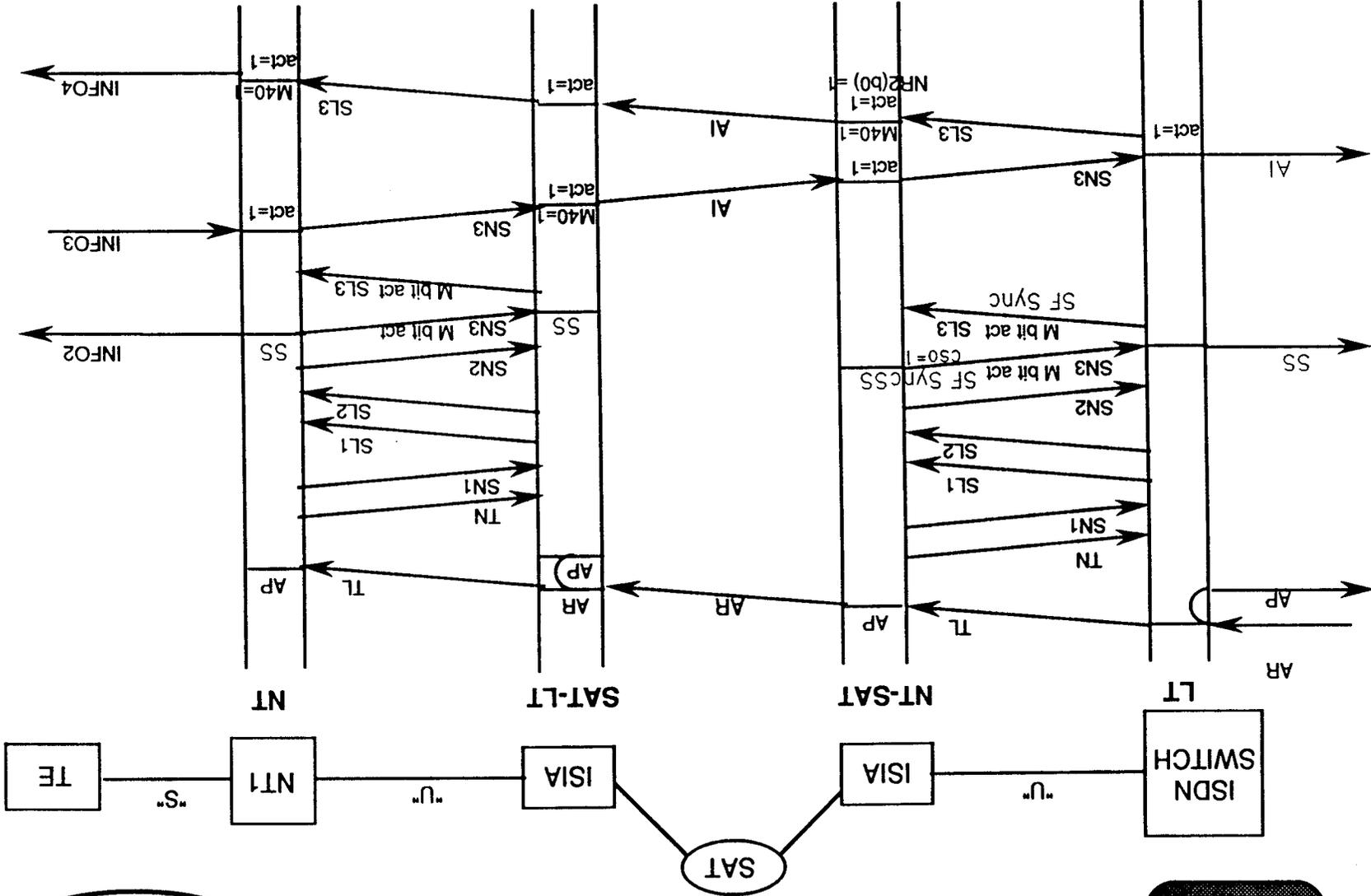


Figure 4-2-1 Total Activation Initiated by the Exchange

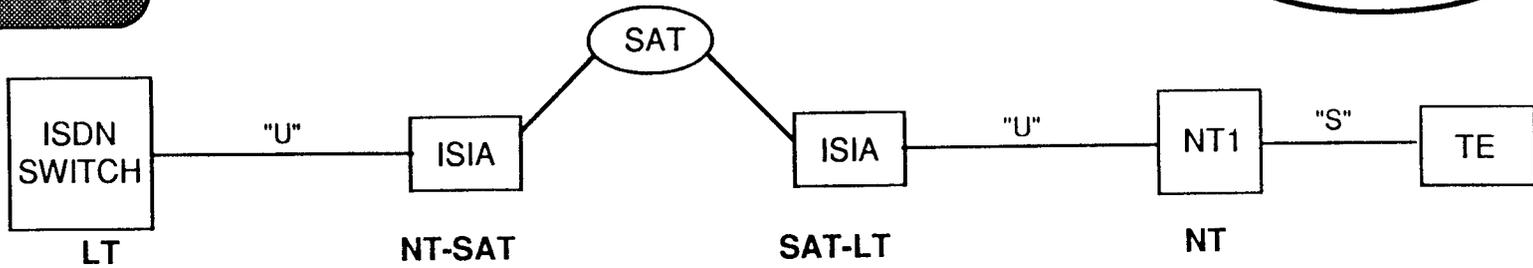
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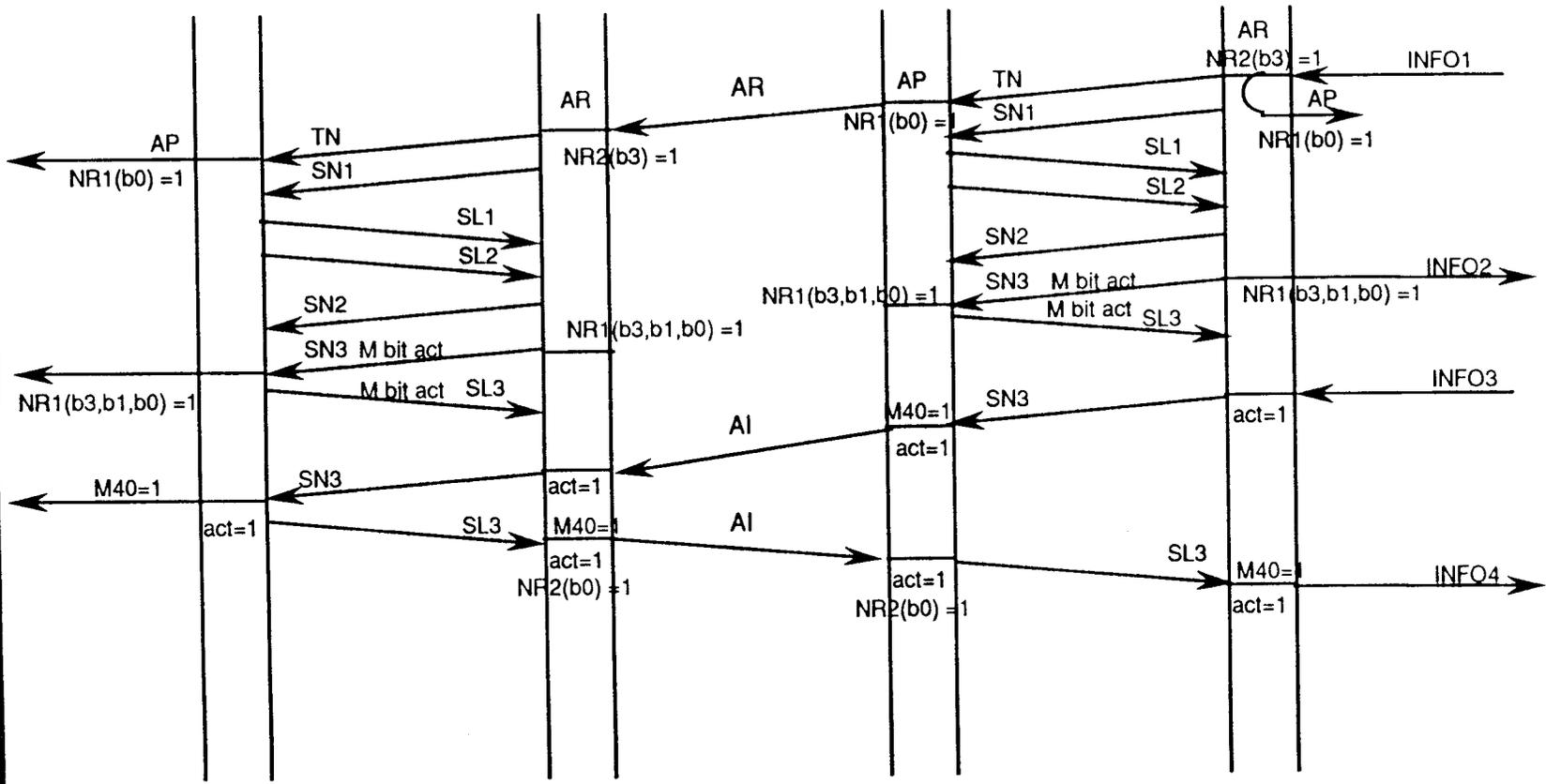


Figure 4.3-1 Total Activation Initiated by Terminal Equipment

#### **4.4 ISTA Deactivation Process**

Figure 4.4-1, "Total Deactivation Process", shows the sequence of protocols initiated by the exchange and the responses that will permit the deactivation of all the interfaces. The Z-chart of these protocol sequences is aligned with a top level block diagram of the satellite connectivity between the ISDN switch and the terminal equipment (TE). The LT on the exchange side receives a deactivation request (DR) that is passed along in term of state changes, protocol messages, and reset at the interfaces. Then at the terminal user end the NT1 and TE continue to exchange Info0 protocol messages.

#### **4.5 ISTA Circuit Diagram**

The circuit diagram shown in Figure 4.5-1a,b,c, "ISTA Circuit Diagram" shows the pin to pin connections of the ISDN U-Interface Transceiver (MC145472), the Integrated Multi-Protocol Processor (MC68302), and the ancillary circuitry identified in the Figure 3.4-1. The specific component values will be addressed in the design reviews that will be part of the implementation of these ISTAs.



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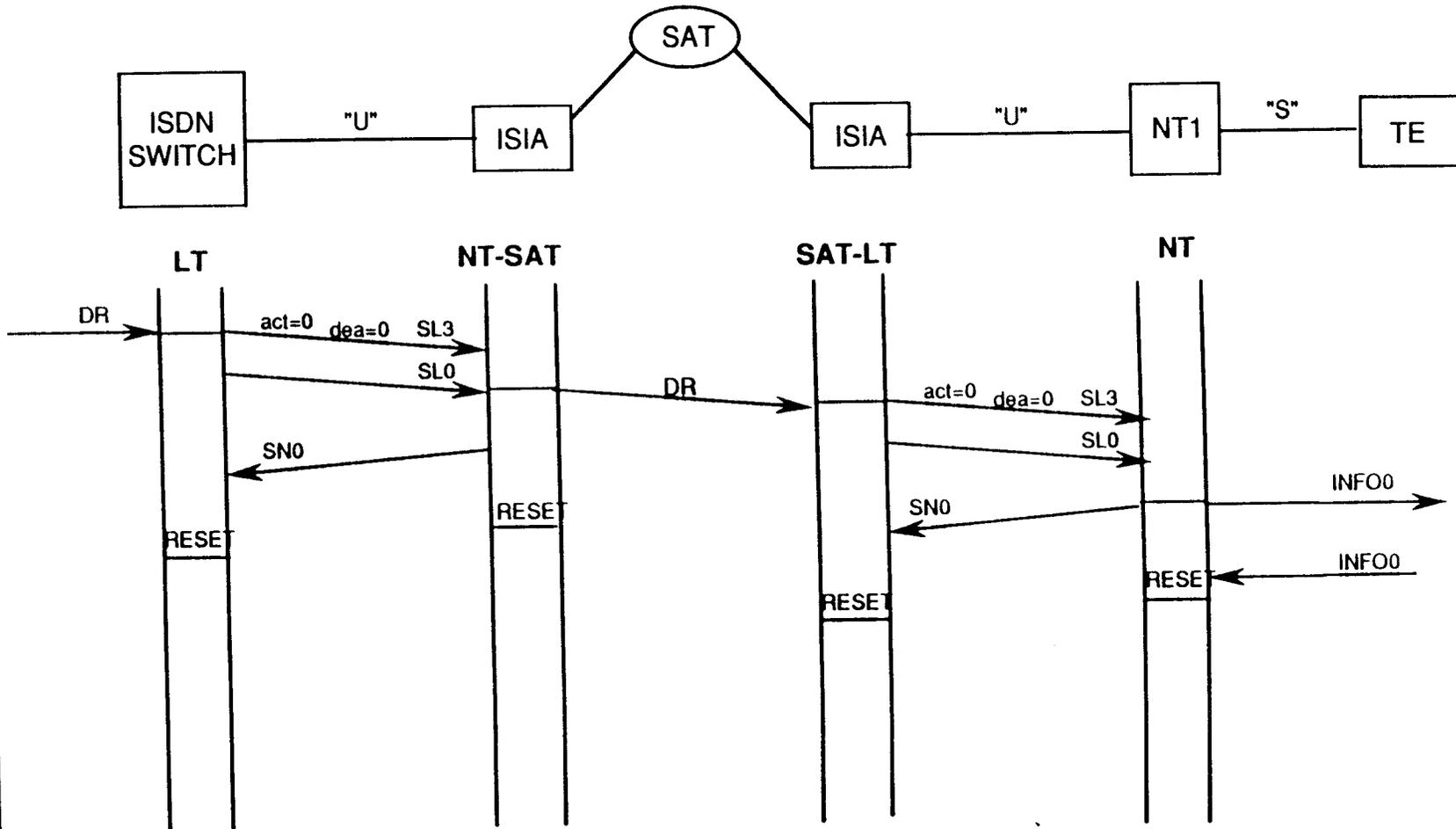
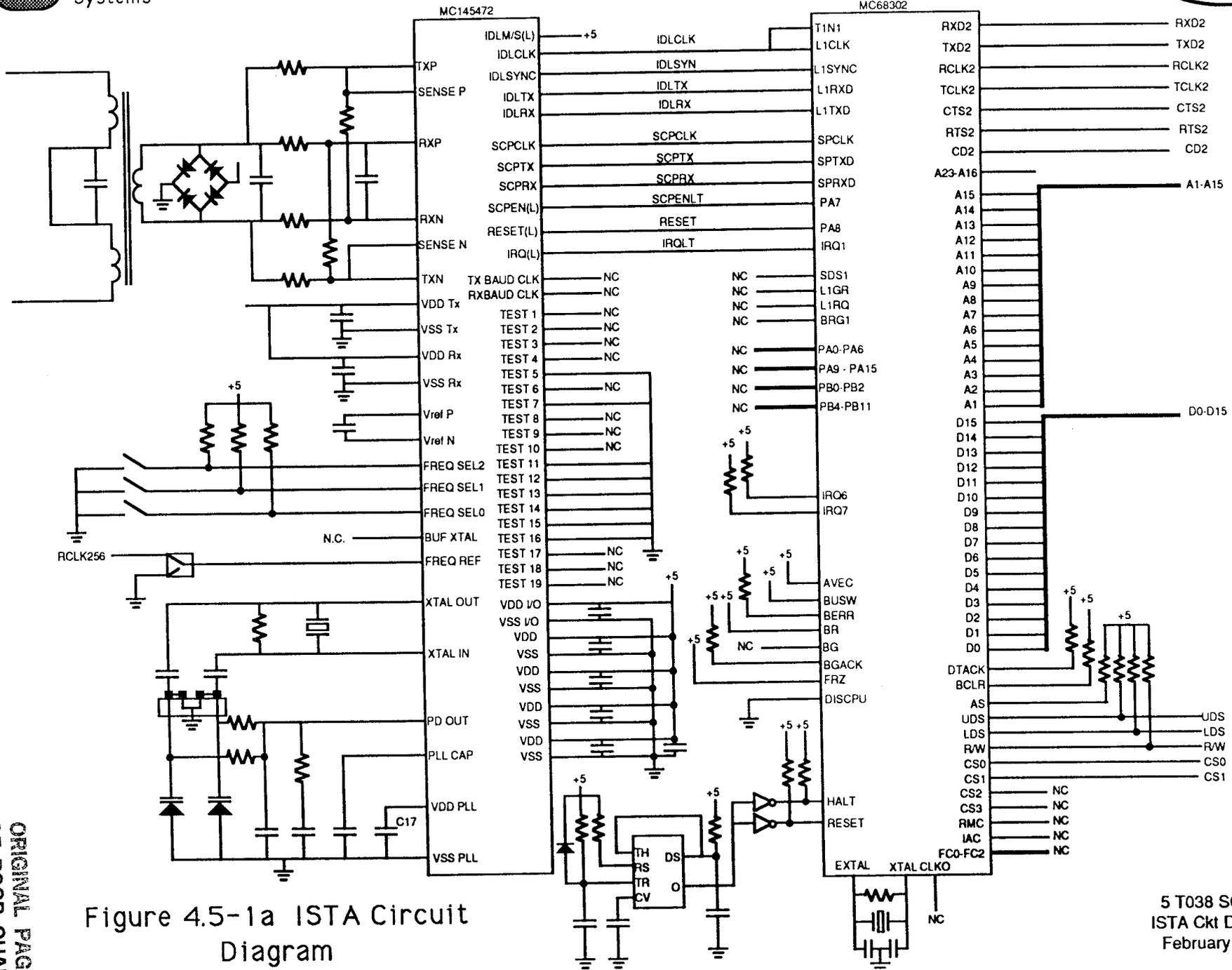


Figure 4.4-1 Total Deactivation Process



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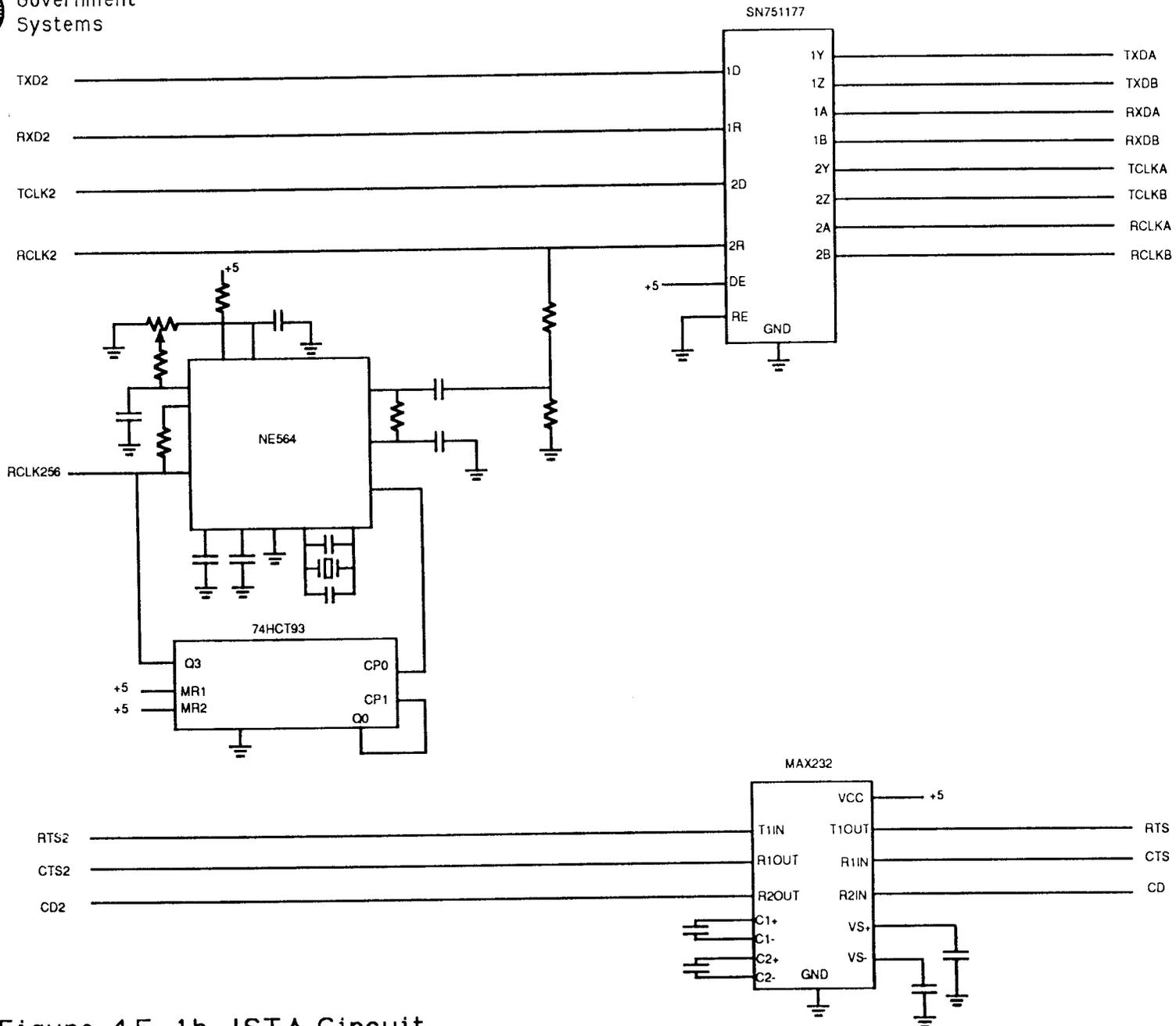
Figure 4.5-1a ISTA Circuit Diagram

5 T038 SCA DAT ISTA Ckt Diagram a February 4, 1992



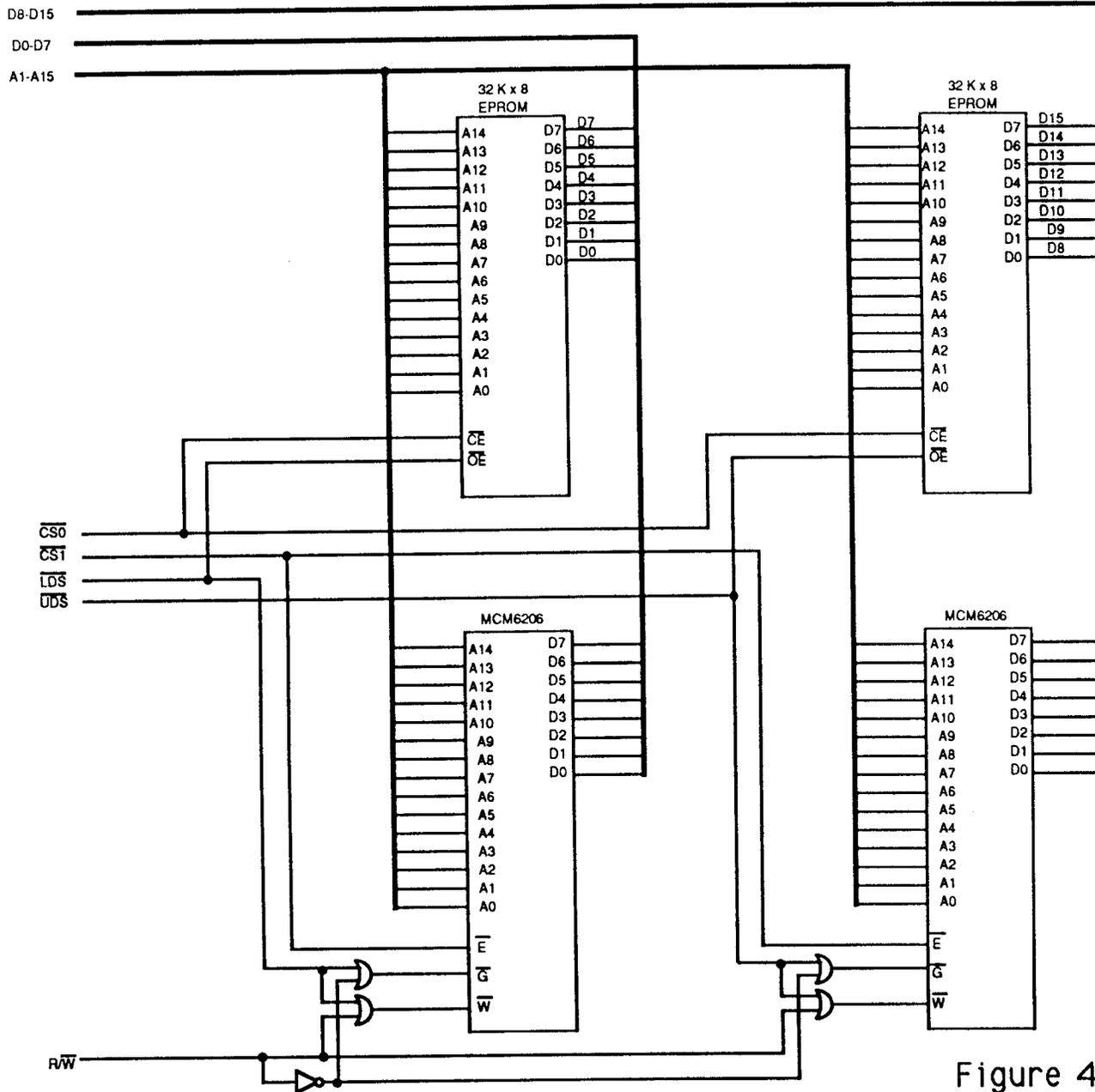
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Figure 4.5-1b ISTA Circuit Diagram



4 - 8

Figure 4.5-1c ISTA Circuit Diagram

## SECTION 5

### SUMMARY

#### 5.1 General

This task completion report for the ISIS Hardware experiment design presented the complete end-to-end view from the basic objectives to the ISTA circuit design. The ISTA hardware design is applicable to the the Interim Service ISDN Satellite (ISIS) and can be used with any HDLC interfaced communications satellite. The ultimate aim of this aspect of the SCAR Program is to demonstrate that ISDN communications via satellite is possible and to corroborate the engineering design values for new advanced ISDN communications satellite. The technical and operational parameters for this ISDN advanced communications satellite design will be obtained from an engineering software model of the major subsystems of the ISDN communications satellite architecture. Discrete event simulation experiments will be performed with these ISIS models using various traffic scenarios, technical parameters, and operational procedures. The data from those simulations will be analyzed using the performance measures discussed in previous NASA SCAR reports. These same data will be compared from data gathered from hardware experiments using ISTAs cited in this report.

#### 5.2 Review

This task completion report begins by describing the objectives of the ISIS hardware experiment in terms related a communications satellite connected to an ISDN terrestrial link. A specific application of sending compressed video from NASA Lewis in Ohio to the GTE #5ESS switch in Virginia was postulated for discussions about the design of the ISTA.

The ISTA design was decomposed into several detailed views identifying the design refinements along the way. Each of these design views was described in terms of their associated hardware, the chip set, and the software design. The ISDN basic access superframe structure and the satellite link access HLDC Frame Structure were described down to the bit level.

The ISTA activation and deactivation for both the exchange and terminal equipment was discussed in the context of end-to-end Z-diagrams. The relationship between the 68000 Development System and the ISTA was shown and a detail circuit design down to the chip pin connections was provided.

#### 5.3 Continuing Efforts

The design of the ISTA is completed. A subcontractor with prior expertizes with this SCAR program has contracted to build three ISTAs suitable for experiments with ACTS or other communications satellites. Experiments will be conducted to verify the performance of the ISTA and to demonstrate the proof of concept. The experiment configuration will include ISDN terminals, ISTAs, the ISDN hub switch and, optionally, the ACTS/TDMA simulator. An ISDN protocol emulator/analyzer will be used to verify protocol conformance of the ISTA interfaces. The ACTS/TDMA hardware simulator could be used to augment ISTA testing. The ACTS/TDMA simulator would provide a hardware simulation of ACTS call processing procedure, processing delays, and switching delays and would help the team to undertake more advanced ISDN communications tests. Experiments are expected to include ISDN call applications such as voice call management, video conference, and Group IV facsimile transmission in addition to various passive bus configurations.