

NASA Conference Publication 10053

Advanced Modulation And Coding Technology

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CODING TECHNOLOGY CONFERENCE (NASA) 324 0
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*Proceedings of a conference sponsored by
NASA Lewis Research Center
Cleveland, Ohio
June 21-22, 1989*

NASA

NASA Conference Publication 10053

Advanced Modulation And Coding Technology

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June 21 and 22, 1989*

NASA
National Aeronautics and
Space Administration
**Scientific and Technical
Information Program**

1992



PREFACE

The Space Electronics Division, under the auspices of NASA's Office of Space Science and Applications and the Lewis Research Center, was pleased to sponsor this conference on Advanced Modulation and Coding Technology. Participants from government agencies, industry, and academia exchanged information on a variety of modulation and coding technology development programs, characterized civil applications, and defined future mission needs for these technologies.

The conference included 23 papers in five sessions, a poster session, and a panel discussion. The conference was organized as follows:

- I. NASA/Lewis Program Review
- II. Lewis Bandwidth Efficient Modulation - Advanced Modulation Technology Development (AMTD)
- III. Other Lewis Modulation and Coding Work
- IV. Poster Displays and Technology Reviews
- V. Other Advanced Modulation and Coding Problems
- VI. Technology Needs/Opportunities for Future Missions
- VII. Panel Response and Discussion

The first four sessions addressed Lewis-sponsored development programs and consisted of presentations, hardware demonstrations, and poster displays. Sessions V and VII dealt with other applications. Although 23 papers were presented, only 22 were available at the time of this publication. Papers and authors are grouped by session in the Table of Contents. The transcript of Session VII, the panel response and discussion, which focussed on the issues and challenges of future technology development, was too lengthy to be included in this publication.



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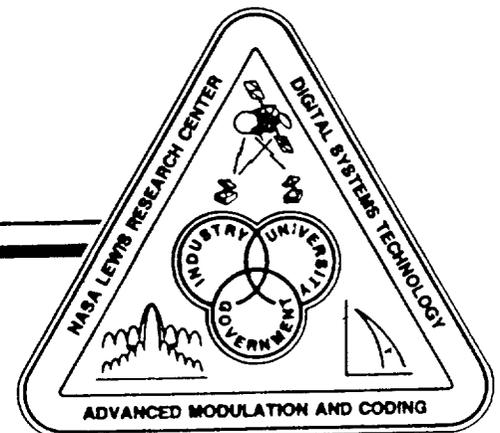


SESSION I

NASA AND LEWIS PROGRAM REVIEW
CHAIR: J.R. RAMLER

LEWIS COMMUNICATIONS PROGRAM OVERVIEW
J.R. RAMLER

LEWIS ADVANCED MODULATION AND CODING PROJECT:
INTRODUCTION AND OVERVIEW
J.M. BUDINGER

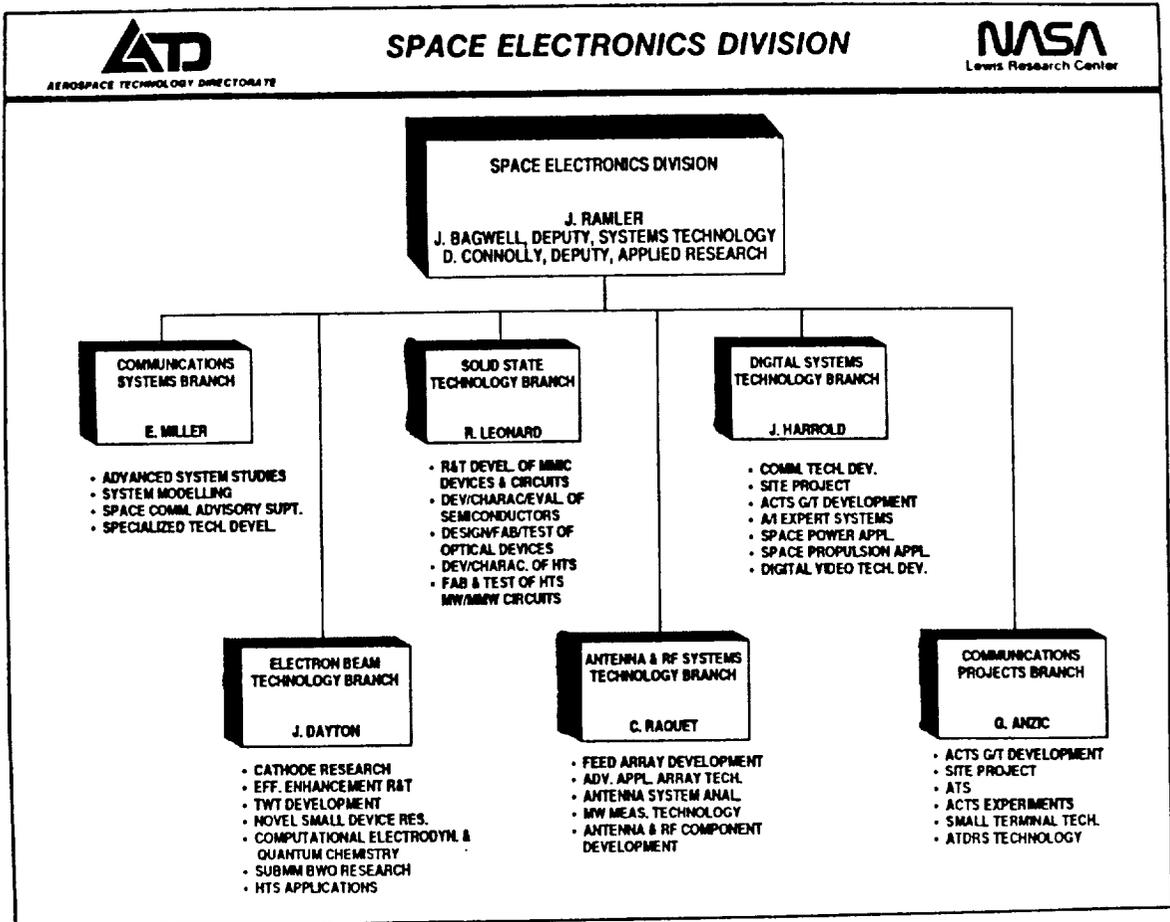




LEWIS COMMUNICATIONS PROGRAM OVERVIEW

James R. Ramler
 National Aeronautics and Space Administration
 Lewis Research Center
 Cleveland, Ohio 44135

The Space Electronics Division conducts a program of research and technology development related to space communications, power and propulsion to meet the needs of NASA, other government agencies and U.S. industry. Division activities include the development of electron beam and solid state technologies, antennas, radio frequency (RF) systems ranging from microwave to submillimeter wavelengths, digital systems, and the development and application of intelligent systems, and applications of high temperature superconductivity. The level of technology development ranges from applied research through space flight experimentation. Division activities also include the conduct of systems studies to help define and guide the technology programs. The Division also participates in, and provides technical consultation to international meetings and conferences on the use of frequency spectrum and geostationary orbital arc. The Division's programs are carried out through a combination of in-house, contract and grant activities.



The majority of research and technology development conducted by the Space Electronics Division is aimed at space communications applications. In fiscal year 1989, the Lewis Research Center will devote approximately 120 workyears to this area. This includes about 100 Civil Servants (CS) and about 20 on-site Support Service Contractors (SSC) and University Grantees. Funding is provided principally by NASA's Office of Aeronautics and Space Technology (OAST) and Office of Space Science and Applications (OSSA). About 50% of the Division's funding is directed to contracts with U.S. Industry, 10% to Grants with universities and 40% to the Division's in-house research and technology development.

**LEWIS COMMUNICATIONS TECHNOLOGY PROGRAM
RESOURCES (FY89)**

• **WORKYEARS**

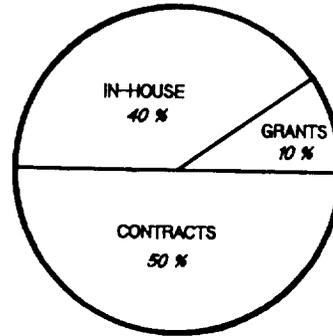
102 CS (64 S & E, 38 SPT)

19 ON-SITE SSC / UNIV

• **FUNDING (\$M)**

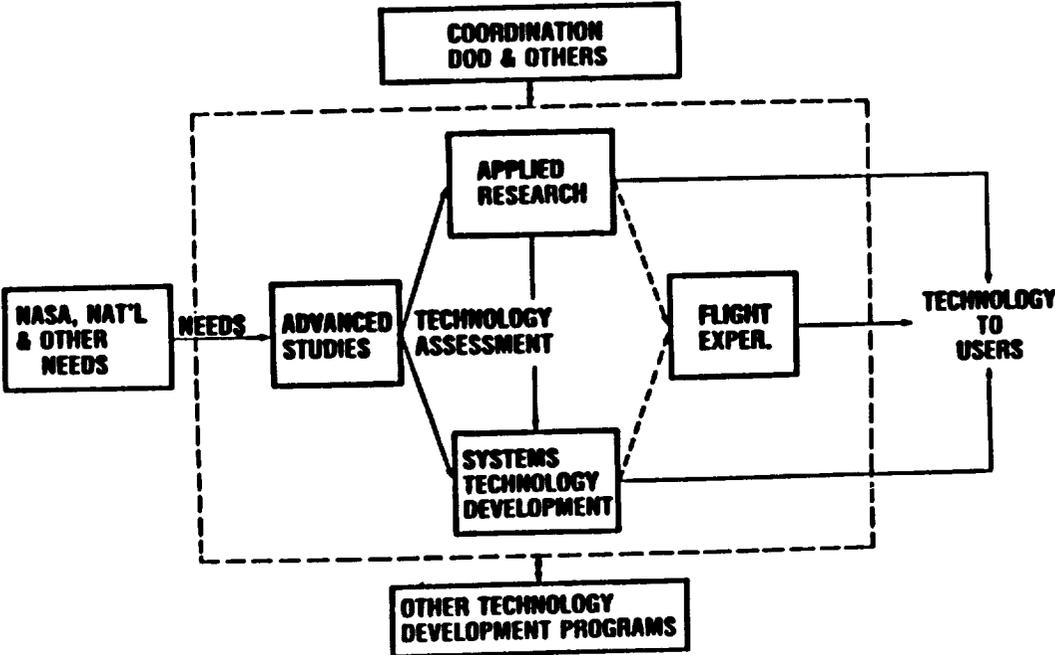
OAST	4.4
OSSA	6.6
OTHER	<u>2.5</u>
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• **DISTRIBUTION**

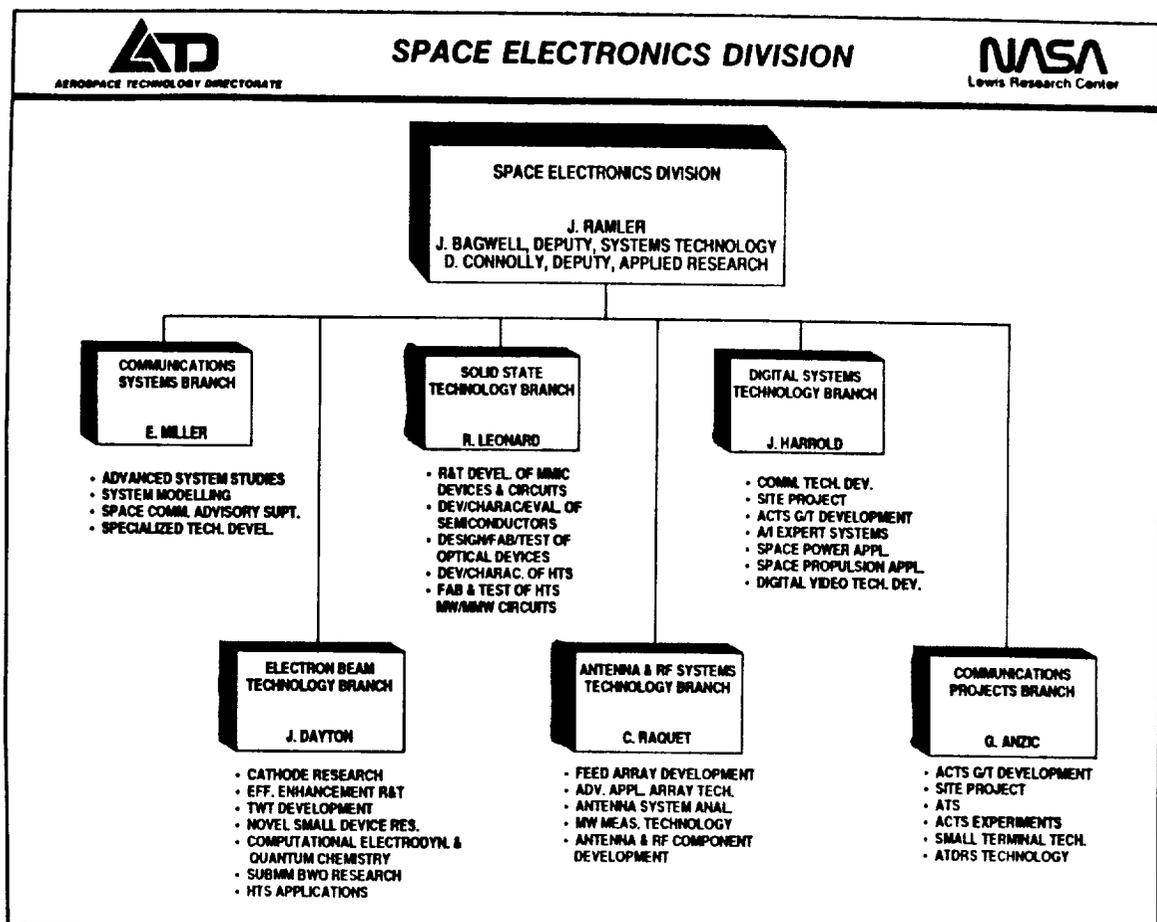


The Division's program is primarily need driven but opportunities afforded by the advancement of technology also help to determine program direction. System studies of advanced space communications concepts, architectures and spacecraft configurations are conducted to determine technical and economic requirements and to identify technology needs. Applied research is conducted to demonstrate technical feasibility usually at the device or component level. Systems technology development is undertaken to carry promising technologies to at least a proof-of-concept level of maturity, typically at the subsystem or system level. Flight experiments are conducted to test and demonstrate technologies in an operational space environment. The Advanced Communications Technology Satellite (ACTS) being developed by OSSA and LeRC for launch in 1992 will demonstrate multi-beam communications at Ka-band with on-board processing and switching - technologies pioneered by LeRC.

PROGRAM METHODOLOGY



The Space Electronics Division conducts a program of research and technology development related to space communications, power and propulsion to meet the needs of NASA, other government agencies and U.S. industry. Division activities include the development of electron beam and solid state technologies, antennas, radio frequency (RF) systems ranging from microwave to submillimeter wavelengths, digital systems, and the development and application of intelligent systems, and applications of high temperature superconductivity. The level of technology development ranges from applied research through space flight experimentation. Division activities also include the conduct of systems studies to help define and guide the technology programs. The Division also participates in, and provides technical consultation to international meetings and conferences on the use of frequency spectrum and geostationary orbital arc. The Division's programs are carried out through a combination of in-house, contract and grant activities.



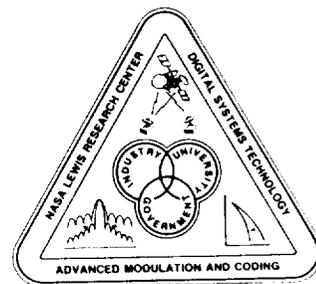
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LEWIS ADVANCED MODULATION AND CODING PROJECT:
INTRODUCTION AND OVERVIEW

James M. Budinger
National Aeronautics and Space Administration
Lewis Research Center
Cleveland, Ohio 44135

ABSTRACT

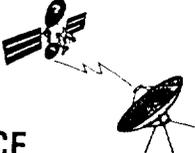
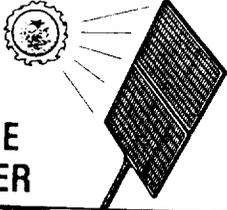
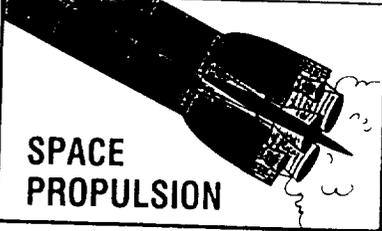
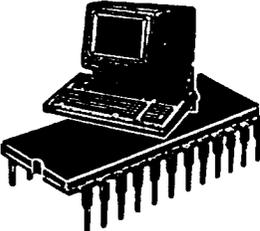
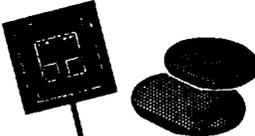
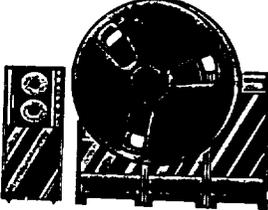
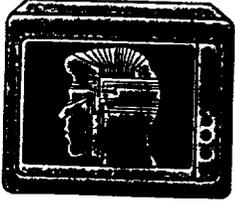
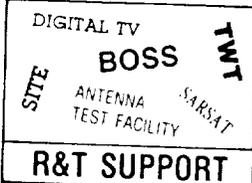
The Advanced Modulation and Coding Project at NASA Lewis Research Center is sponsored by the Office of Space Science and Applications, Communications Division, Code EC, at NASA Headquarters and conducted by the Digital Systems Technology Branch of the Space Electronics Division. Advanced Modulation and Coding is one of three focused technology development projects within the branch's overall Processing and Switching Program. The program consists of industry contracts for developing proof-of-concept (POC) and demonstration model hardware, university grants for analyzing advanced techniques, and in-house integration and testing for performance verification and systems evaluation. The Advanced Modulation and Coding Project is broken into five elements: (1) bandwidth- and power-efficient modems; (2) high-speed codecs; (3) digital modems; (4) multichannel demodulators; and (5) very high-data-rate modems. At least one contract and one grant have been awarded for each element.



DIGITAL SYSTEMS TECHNOLOGY MISSIONS

The Space Electronics Division has maintained prime responsibility for space communications research and technology development at Lewis and has recently expanded its charter to provide electronics technology support to space power and propulsion missions. The Digital Systems Technology Branch provides expertise in advanced digital systems development disciplines including design of custom, computer-based, digital equipment, mini- and microcomputer software and control, application-specific integrated circuits (ASIC), and most recently, expert systems. To date, the branch's activities have been predominantly directed toward space communications.

In-house facilities and hardware and software expertise have been applied to the development of ground terminal digital subsystems, link effects simulation, and experiment control for evaluating microwave components and time-division-multiple-access (TDMA) networks. The branch also provides custom hardware and computer support to division research facilities for traveling wave tube amplifiers, near-field antenna pattern measurements, and digital video signal compression.

<div style="background-color: black; color: white; padding: 5px; text-align: center; font-weight: bold;">ADVANCED DIGITAL SYSTEMS</div> <div style="text-align: center; margin-top: 10px;">  <p>SPACE COMMUNICATIONS</p> </div> <div style="text-align: center; margin-top: 10px;">  <p>SPACE POWER</p> </div> <div style="text-align: center; margin-top: 10px;">  <p>SPACE PROPULSION</p> </div>	<div style="text-align: center; margin-bottom: 10px;">  <p>MICROCOMPUTERS</p> </div> <div style="text-align: center; margin-bottom: 10px;">  <p>DIGITAL DESIGN & TEST</p> </div> <div style="text-align: center;">  <p>ASIC DESIGN</p> </div>	<div style="text-align: center; margin-bottom: 10px;">  <p>MINICOMPUTERS</p> </div> <div style="text-align: center; margin-bottom: 10px;">  <p>EXPERT SYSTEMS</p> </div> <div style="text-align: center;">  <p>R&T SUPPORT</p> </div>
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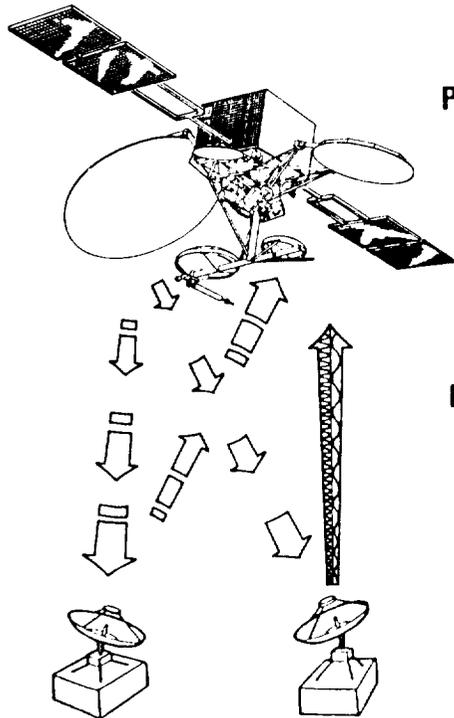
PROGRAM GOALS AND FOCUS

The main goals of the Processing and Switching Program are shown below. The intention of the program is to identify and develop critical digital components and technologies that either enable new commercial and civil missions or significantly enhance the performance, cost efficiency, or reliability of existing and planned space communications systems. The sketch is intended to indicate that both frequency- and time-division multiple access (FDMA and TDMA), with onboard information processing and switching, and multiple-beam, time-division-multiplexed (TDM) downlink systems are investigated. Space and ground segment component designs are addressed concurrently to ensure cost efficiency and realistic operational constraints. Advanced theoretical concepts are implemented in hardware suitable for demonstrating risk reduction and commercial potential. Eventually the application of fault-tolerant design techniques and real-time expert system controls will address fully autonomous operation of onboard systems.

To date, the program has been focused on developing of advanced modulation and coding technologies through contracts and grants and on ground-based processing and control through in-house design, fabrication, and evaluation. The Digital Systems Technology Branch plans to significantly increase the attention paid to space-based processing and control through design and development of fault-tolerant, autonomous, onboard processors for information processing and switching.

DIGITAL SYSTEMS TECHNOLOGY PROCESSING AND SWITCHING PROGRAM

NASA
Lewis Research Center



PROGRAM GOALS:

- MISSION-ENABLING TECHNOLOGIES
- APPLICATION-FOCUSED MODELS
- DEVICES, COMPONENTS, AND SUBSYSTEMS
- CONCURRENT SPACE AND GROUND SEGMENTS
- ONBOARD FAULT TOLERANCE AND AUTONOMY
- RISK REDUCTION AND TECHNOLOGY TRANSFER

PROGRAM FOCUS:

- ADVANCED MODULATION AND CODING
- SPACE-BASED PROCESSING AND CONTROL
- GROUND-BASED PROCESSING AND CONTROL

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DEVELOPMENT PLAN

The Digital Systems Technology Branch has successfully implemented the technology development plan shown below. Depending on program priorities, multiple contract awards and multiple phased developments can be accommodated to increase the probability of achieving viable solutions. Fully digital solutions are sought to exploit inherent advantages of reduced size, power consumption, and production cost; increased reliability; and avoidance of alignment, drift, and aging problems associated with analog techniques. Most contract developments address flexible, programmable, or extendable designs to reduce nonrecurring engineering costs and to ease the development of mission-focused hardware. Proposers are encouraged to identify preliminary designs, plans for transferring technology development into commercial products, and cost-sharing approaches in their proposals.

DIGITAL SYSTEMS TECHNOLOGY TECHNOLOGY DEVELOPMENT PLAN

NASA
Lewis Research Center

- **CONTRACTS FOR ADVANCED IMPLEMENTATIONS OF THEORETICAL CONCEPTS**
- **MULTIPLE CONTRACTS; MULTIPLE DEVELOPMENT LEVELS**
- **GRANTS TO EXPLORE PROMISING TECHNIQUES THROUGH DESIGN AND BREADBOARD**
- **IN-HOUSE VERIFICATION AND SYSTEMS EVALUATION**
- **ADVANCED, DIGITAL SOLUTION—RECOGNIZED BENEFITS**
- **STUDY TASK AND TECHNOLOGY ASSESSMENT ADDRESSED IN PROPOSAL**
- **TECHNOLOGY TRANSFER AND COMMERCIALIZATION PLANS**
- **COST SHARING**

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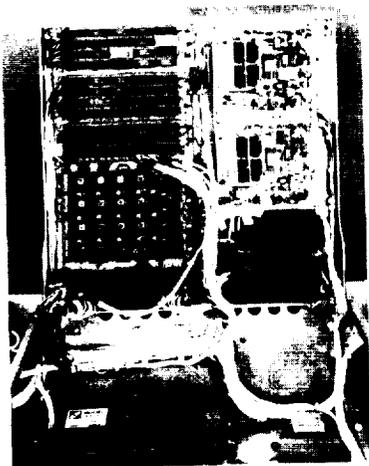
PROGRAM APPROACH

Advanced techniques investigated under university grants, small business innovative research (SBIR) contracts, and aerospace industry study contracts help to establish the requirements for developing critical components and subsystems. Both universities and industry fabricate hardware models and special test equipment (STE) appropriate for demonstrating the advanced techniques on a stand-alone basis. The photograph on the left shows a portion of Ford Aerospace's 8-PSK POC demodulator.

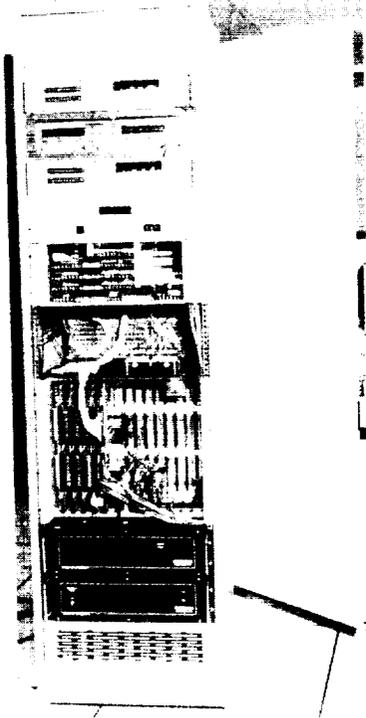
Digital subsystems for communications network and transponder test facility experiments, as well as some necessary STE and experiment controllers, are designed and developed in-house. The center photograph shows the 220 Mbps digital range delay simulator designed and fabricated in-house to simulate coarse and fine satellite motion. The simulator is used to evaluate network timing acquisition and synchronization techniques.

Under Lewis' Systems Integration, Test, and Evaluation (SITE) Project, POC and demonstration models are integrated with in-house and commercial hardware and software to create an end-to-end simulation facility of a satellite-switched, time-division-multiple-access (SS-TDMA) satellite network. The photograph on the right shows one of the TDMA ground terminals that incorporate 220/110-Mbps serial minimum shift keying (SMSK) modems developed under contract by Motorola, commercial 6809- and 68000-based microcomputer chassis, and in-house designed and fabricated TDMA controllers and multiple terrestrial user simulators.

**UNIVERSITY AND
INDUSTRY
DEVELOPMENT**



**IN-HOUSE
DEVELOPMENT**



**IN-HOUSE
EXPERIMENTAL SYSTEMS
INTEGRATION, TEST
AND EVALUATION**



READINESS LEVELS

The Office of Aeronautics and Space Technology (OAST) at NASA Headquarters defines seven levels of technology readiness shown in the left two columns below. The Space Electronics Division at Lewis has used the terms in the right column for several years in its requests for proposals and technical reports. The Processing and Switching Program addresses technology development from level 2 through level 5. In general, a POC model development (level 3) is selected when the first conversion of an advanced theoretical concept into hardware is required. A study and refinement of proposed design phase (level 2) is usually conducted by the contractor in an early POC contract task. For those technologies that currently exist in some hardware form, and where a significant increase in performance or packaging efficiency is necessary, the demonstration model approach (level 4) will be pursued. Finally, a flight-qualifiable model (level 5) may be fabricated for those technologies that require demonstration in a relevant environment to ensure mission readiness. Typically, the flight-qualified model and the flight model itself will be developed by a flight mission project office.

DIGITAL SYSTEMS TECHNOLOGY TECHNOLOGY READINESS LEVELS



<u>LEVEL</u>	<u>NASA DEFINITION</u>	<u>LEWIS NOMENCLATURE</u>
1	BASIC PRINCIPLES OBSERVED	BASIC RESEARCH AND TECHNOLOGY DEVELOPMENT
2	TECHNOLOGY CONCEPT AND/OR APPLICATION FORMULATED	PROOF-OF-CONCEPT STUDY PHASE
3	ANALYTICAL OR EXPERIMENTAL CRITICAL FUNCTION OR CHARACTERISTIC PROVED	PROOF-OF-CONCEPT MODEL DEVELOPMENT
4	COMPONENT AND/OR BREADBOARD VALIDATION IN THE LABORATORY	DEMONSTRATION MODEL DEVELOPMENT
5	COMPONENT AND/OR BREADBOARD DEMONSTRATION IN A RELEVANT ENVIRONMENT	FLIGHT-QUALIFIABLE MODEL
6	SYSTEM VALIDATION MODEL DEMONSTRATION IN A SIMULATED ENVIRONMENT	FLIGHT-QUALIFIED MODEL
7	SYSTEM VALIDATION MODEL DEMONSTRATION IN SPACE	FLIGHT MODEL

ADVANCED MODULATION AND CODING PROJECT OBJECTIVES

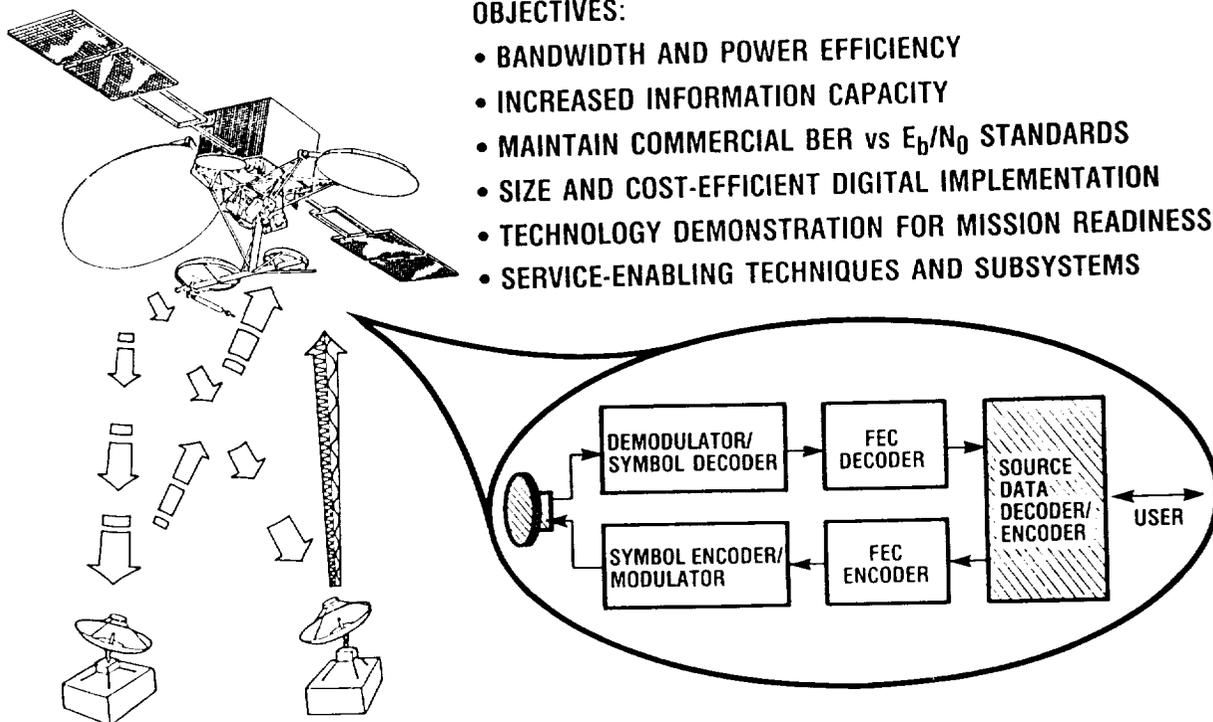
The objectives of the Advanced Modulation and Coding Project are shown below. The primary goal of this project is to develop bandwidth-efficient digital modulation schemes that are suited to the power, cost, and complexity constraints of an operational system. These schemes should provide bit-error-rate performance comparable to commercial quadrature phase shift keying (QPSK) standards. As is true of all three projects within the Processing and Switching Program, an underlying objective is to reduce the development risk and cost and thereby increase the potential for technology transfer to the commercial industry.

The highlighted blocks in the diagram indicate a concentration of effort on combined modulation and coding techniques and on forward-error-correction (FEC) coding. Techniques and components are under development for both space and ground segment applications.

An overview of the recent and current contracts and grants under the Advanced Modulation and Coding Project is presented later in this paper.

DIGITAL SYSTEMS TECHNOLOGY ADVANCED MODULATION & CODING

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Lewis Research Center



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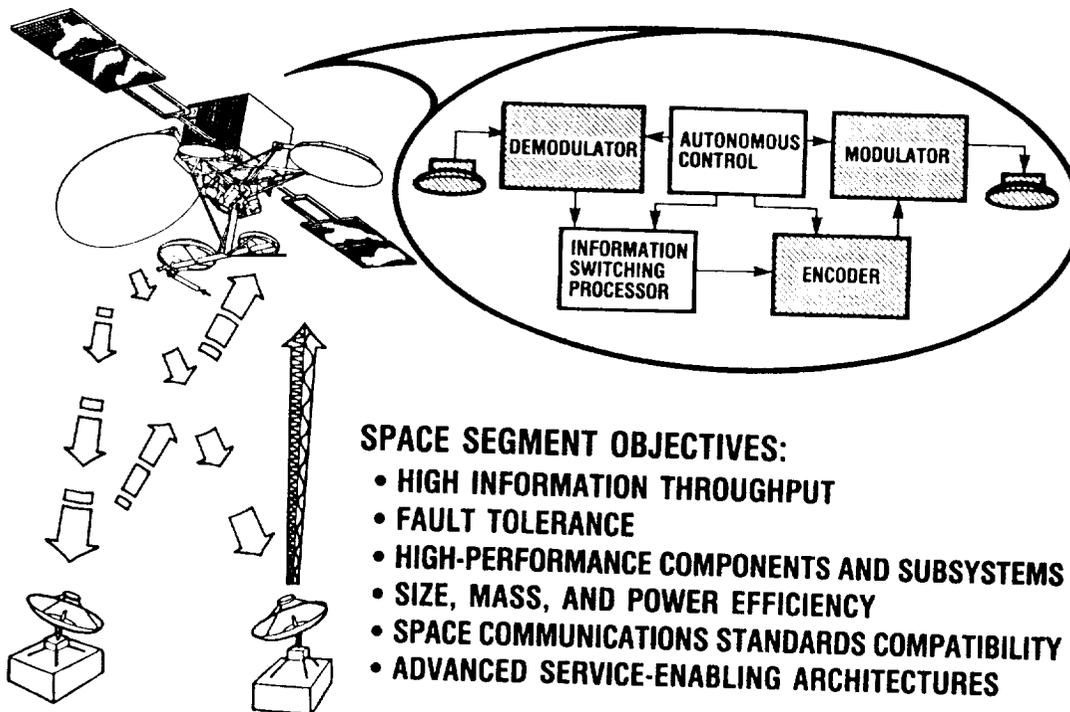
SPACE-BASED PROCESSING AND CONTROL PROJECT OBJECTIVES

The objectives of the Space-based Processing and Control Project are shown below. The project has two primary goals associated with the two highlighted blocks in the diagram. The first goal is to develop a high-throughput, fault-tolerant, information-switching processor with circuit and packet switching capabilities compatible with emerging commercial and international space communications standards. The second goal is to incorporate into the onboard electronics package selected network control and data-processing functions traditionally performed in various locations within a terrestrial network.

Both the information-switching processor and the autonomous controller will require radiation-tolerant components with built-in testability and some level of real-time artificial intelligence for fault detection and isolation and real-time reconfiguration of onboard resources. When combined with advanced modulation techniques such as multichannel demultiplexing and programmable digital modems, fault-tolerant onboard processing and autonomous control can enable new commercial and civil satellite services.

DIGITAL SYSTEMS TECHNOLOGY SPACE-BASED PROCESSING AND CONTROL

NASA
Lewis Research Center



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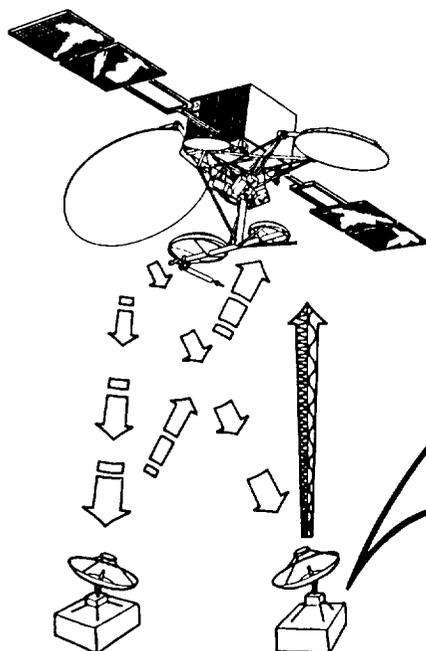
GROUND-BASED PROCESSING AND CONTROL PROJECT OBJECTIVES

The objectives of the Ground-based Processing and Control Project are shown below. The primary goal of this project is to develop flexible FDMA and TDMA controllers and terrestrial user interfaces for cost-efficient ground terminals. The controllers and interfaces must be compatible with the evolving processing satellite network architectures envisioned by NASA.

To date, only in-house activities have been pursued under this project. In support of the Systems, Integration, Test, and Evaluation (SITE) Project, multiple TDMA ground terminal digital subsystems have been designed and developed. Modems and codecs developed under the Advanced Modulation and Coding Project will be integrated with the digital, ground-based processing and control hardware for performance evaluation in the SITE satellite network simulation facility.

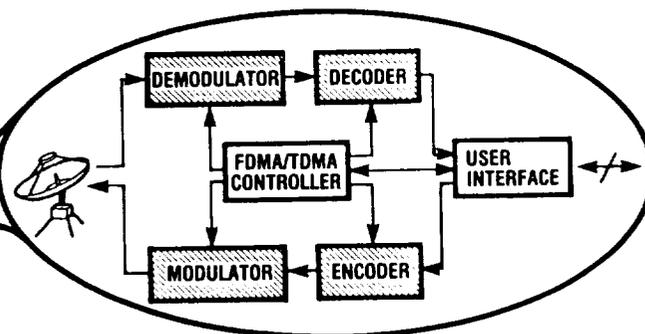
DIGITAL SYSTEMS TECHNOLOGY GROUND-BASED PROCESSING AND CONTROL

NASA
Lewis Research Center



GROUND SEGMENT OBJECTIVES:

- COST-EFFICIENT IMPLEMENTATION
- HIGH-PERFORMANCE COMPONENTS
- FLEXIBILITY AND PROGRAMMABILITY
- INDUSTRY STANDARDS COMPATIBILITY
- INTELLIGENT SYSTEMS APPLICATIONS
- NETWORK SERVICE ENABLING



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PROGRAM FUNDING DISTRIBUTION

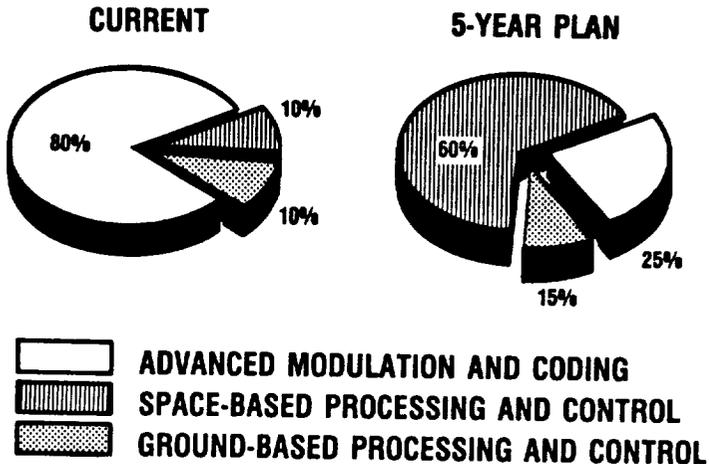
Currently, about 80 percent of the Processing and Switching Program funding is expended on the Advanced Modulation and Coding Project. The Space- and Ground-based Processing and Control Projects each consume about 10 percent of the remaining funds. Within 5 years the Digital Systems Technology Branch plans for the Space-based Processing and Control Project funding level to grow to about 60 percent of available funds and Ground-based Processing and Control funding to grow to about 15 percent. Since the total Processing and Switching Program funding projections vary yearly according to NASA priorities, funds available for the Advanced Modulation and Coding Project will vary as well.

The distribution of funds among industry contracts, university grants and in-house projects over the next 5 years is expected to remain nearly constant. The percentage distribution is shown below.

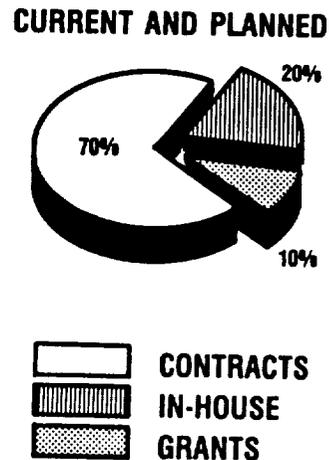
DIGITAL SYSTEMS TECHNOLOGY PROCESSING AND SWITCHING PROGRAM



FUNDING DISTRIBUTION BY PROGRAM ELEMENT



FUNDING DISTRIBUTION BY PROGRAM APPROACH



CD-88-40918

ADVANCED MODULATION AND CODING PROJECT CONTRACTS AND GRANTS

The Advanced Modulation and Coding Project consists of five elements: (1) bandwidth- and power-efficient modems; (2) high-speed codecs; (3) digital modems; (4) multichannel demodulators; and (5) very high-data-rate modems. Contracts and grants are in place for each of the first four elements. Nearly all current and planned contracts are the cost-plus-fixed-fee type. Work under the fifth element is planned to begin in fiscal year 1990. Whenever possible, the Digital Systems Technology Branch has attempted to pursue each element by awarding a mix of openly competed hardware development contracts, SBIR contracts, and university grants. The unifying goal of this approach is the implementation and demonstration of advanced concepts and techniques.

DIGITAL SYSTEMS TECHNOLOGY ADVANCED MODULATION & CODING CONTRACTS & GRANTS



BANDWIDTH- AND POWER-EFFICIENT MODEMS:

- ADVANCED MODULATION TECHNOLOGY DEVELOPMENT
FORD AEROSPACE, TRW, COMSAT LABS, HARRIS
- AMTD FOLLOW-ON
CONTRACT(S) TO BE DETERMINED
- MODULATION TECHNIQUES FOR POWER- AND SPECTRALLY EFFICIENT SATCOM SYSTEMS
UNIVERSITY OF CALIFORNIA, DAVIS

HIGH-SPEED CODECS:

- FLEXIBLE HIGH-SPEED CODEC
HARRIS
- IMPLEMENTATION OF ADVANCED CODING CONCEPTS
UNIVERSITY OF SOUTHERN CALIFORNIA

DIGITAL MODEMS:

- PROGRAMMABLE RATE MODEM USING DIGITAL SIGNAL PROCESSING TECHNOLOGY
MULTIPOINT (T.I.W. SYSTEMS)
- DIGITAL MODEM DEVELOPMENT
UNIVERSITY OF TOLEDO
- PROGRAMMABLE DIGITAL MODEM
COMSAT LABS

CD-89-40920

ADVANCED MODULATION AND CODING PROJECT
CONTRACTS AND GRANTS (CONTINUED)

DIGITAL SYSTEMS TECHNOLOGY
ADVANCED MODULATION & CODING CONTRACTS & GRANTS



MULTICHANNEL DEMODULATORS:

- | | |
|---|--------------------------------|
| • ADVANCED TECHNOLOGY FOR A MULTI-CHANNEL DEMULTIPLEXER/DEMODULATOR | CONTRACTS (2) TO BE DETERMINED |
| • FDMA/TDM CONVERSION FOR NONCONTIGUOUS CARRIERS | UNIVERSITY OF TOLEDO |
| • INNOVATIVE PULSE COMPRESSORS FOR SATELLITE COMMUNICATIONS | AMERASIA |
| • DIGITAL SIGNAL PROCESSING FOR MULTI-CHANNEL DEMODULATION | LEWIS IN-HOUSE |

VERY HIGH-DATA-RATE MODEMS:

- | | |
|--|---------------------------|
| • VERY HIGH-DATA-RATE MODEM | CONTRACT TO BE DETERMINED |
| • MODEMS FOR COMPRESSED VIDEO TRANSMISSION | GRANT TO BE DETERMINED |

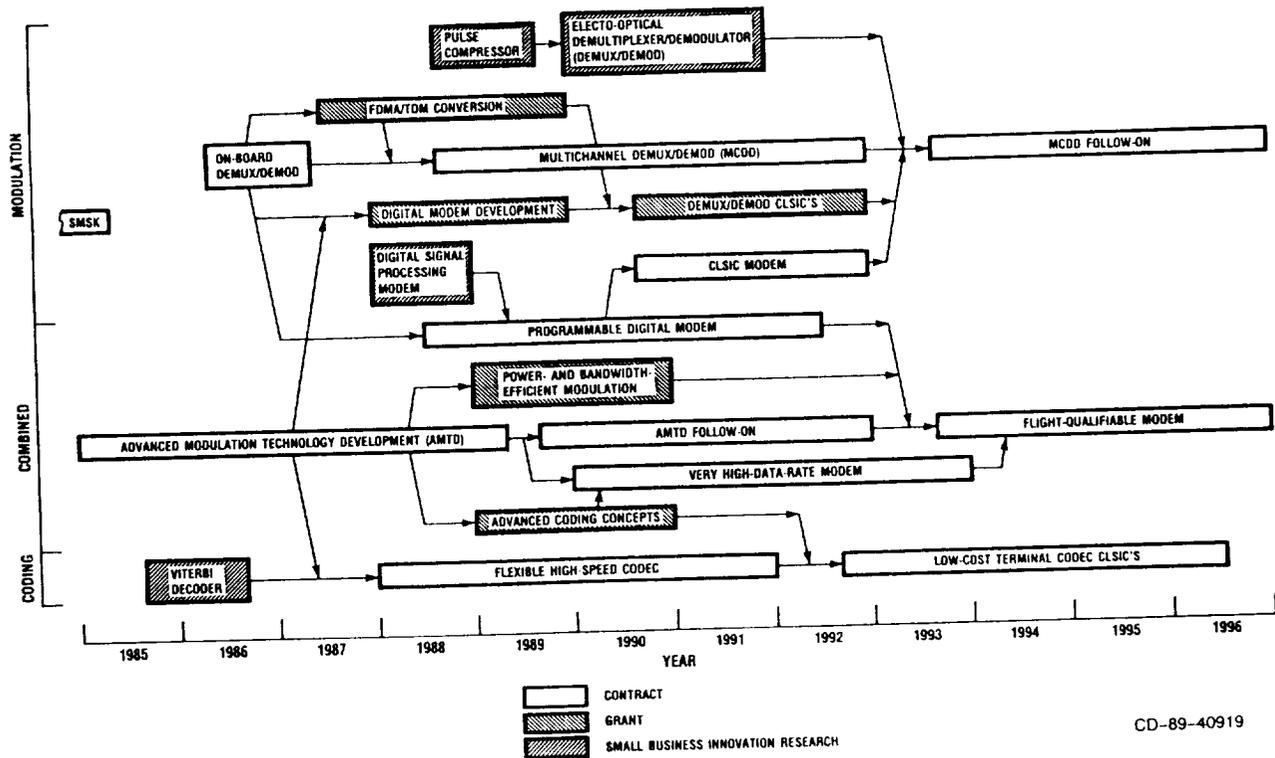
CD-89-40921

ADVANCED MODULATION AND CODING PROJECT CONTRACTS AND GRANTS (CONCLUDED)

The schedule below shows the Digital Systems Technology Branch's past, present, and planned contracts and grants in advanced modulation and coding and their phased relationship to each other. Contracts and grants are located from top to bottom by the level of attention paid to modulation techniques, coding techniques, and the combination of the two. All but the following two contracts are described further in this paper and in papers by the responsible contractors and universities.

The branch's responsibility for advanced modulation hardware development contracts began in mid-1983 with a modification to the baseband processor POC contract with Motorola Government Electronics Group (NAS3-22502). Under the modification, Motorola fabricated four sets of 220/110-Mbps SMSK modem pairs and six 27.5-Mbps SMSK modulators. The modems are similar to those being designed for the Advanced Communications Technology Satellite (ACTS) and have been used extensively in the SITE Project. They have also been included in the in-house link evaluation terminal (LET) designed to characterize the on-orbit performance of the ACTS high-burst-rate (HBR) subsystem.

Under a study contract funded by another branch within the Space Electronics Division, COMSAT Laboratories developed the conceptual design for an "onboard multichannel demultiplexer demodulator" (NAS3-24885). Several digital approaches were investigated and compared by computational complexity. The selected design featured a single, large, forward fast Fourier transform (FFT) processor followed by an inverse FFT for individual channel demultiplexing and a fully digital demodulator. The study served as the basis for a grant in FDMA/TDM conversion and both the multichannel demultiplexer demodulator (MCDD) and programmable digital modem (PDM) statements of work.



CD-89-40919

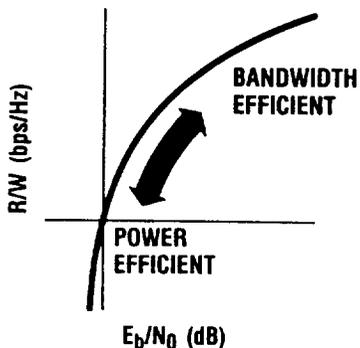
BANDWIDTH- AND POWER-EFFICIENT MODEMS

The curve shown below is based on the Shannon-Hartley capacity theorem, with the information bit rate equal to the capacity of the ideal channel. It illustrates the tradeoff between bandwidth and power efficiency for a given probability of bit error in a practical system. When both bandwidth and power are constrained, combined modulation and coding techniques such as trellis-coded modulation offer improved bandwidth efficiency with BER performance nearly identical to that of practical QPSK systems. The drawback of this approach is increased computational complexity.

The purpose of this project element is to develop practical implementations of bandwidth- and power-efficient modems that are suitable for application in space and ground environments. For spacecraft demodulators, rapid, independent acquisition and small size, mass and power consumption are desirable. For ground terminal demodulators, high data rates and low-cost implementations are the primary goals. The techniques demonstrated under this project element are scalable in information rate, largely independent of the frequency band of operation, and applicable to a variety of spacecraft communications links.

DIGITAL SYSTEMS TECHNOLOGY BANDWIDTH- AND POWER-EFFICIENT MODEMS

NASA
Lewis Research Center



OBJECTIVES:

- TRIPLE ACTS SMSK BANDWIDTH EFFICIENCY
- MAINTAIN QPSK BER vs E_b/N_0
- ACQUIRE BURSTS INDEPENDENTLY
- RAISE INFORMATION RATE TO 200 Mbps OR HIGHER
- COMBINE MODULATION AND CHANNEL SYMBOL ENCODING

BENEFITS:

- CAPACITY DOUBLE THAT OF EXISTING LINKS
- IDENTICAL OR REDUCED TRANSMITTER POWER
- OPERATION AT OR NEAR SATURATION
- REDUCED RISK AND COST

APPLICATIONS:

- PROCESSING SATELLITES:
TDMA UPLINKS
WIDEBAND CROSSLINKS
MULTIPLE-BEAM TDM DOWNLINKS
- SATELLITE-SWITCHED TDMA:
LOW-COST GROUND TERMINALS

CD-89-40922

BANDWIDTH AND POWER EFFICIENT MODEM APPROACH

The four advanced modulation technology development (AMTD) contracts have addressed the implementation of bandwidth-efficient, combined modulation and coding techniques in high-data-rate, TDMA environments with varying degrees of success. All have selected some form of channel symbol encoding to overcome the effects of the bandlimited channels. Although each was required to implement independent burst acquisition, the satellite demodulators were designed to a more difficult adjacent-channel interference requirement. The power efficiency of the modem was a secondary constraint.

The University of California will bring an increased emphasis on power efficiency to this project element. The investigators intend to design modulation systems that are suitable for use with nonlinear high-power amplifiers and to implement and test a slow-speed version of the modems.

If program priorities permit, the Digital Systems Technology Branch intends to pursue a "follow-on" to the AMTD contracts. An openly competed demonstration model contract would address the packaging issues uncovered during the POC developments, while further increasing data rate and bandwidth and power efficiency in a design optimized for application in TDM downlinks. A statement of bidder qualifications will ensure that high-data-rate, bandwidth-efficient modem hardware comparable to the AMTD POC models has already been developed by potential contractors.

DIGITAL SYSTEMS TECHNOLOGY

BANDWIDTH- AND POWER-EFFICIENT MODEMS—APPROACH

NASA

Lewis Research Center

MULTIPLE PROOF-OF-CONCEPT MODEL CONTRACTS "ADVANCED MODULATION TECHNOLOGY DEVELOPMENT" (AMTD)

- ≥ 2 bps/Hz; 200 Mbps; ≤ 500 -ns ACQUISITION
- SATELLITE DEMODULATORS:
 - FORD (NAS3-24678), RATE-5/6-CODED 8-PSK
 - TRW (NAS3-24679), RATE-3/4-CODED 16-QAM
- GROUND TERMINAL DEMODULATORS:
 - COMSAT (NAS3-24680) RATE-8/9-CODED 8-PSK
 - HARRIS (NAS3-24681) RATE-1/2-CODED 16-CPFSK

GRANT—UNIVERSITY OF CALIFORNIA, DAVIS (NAG3-1007) "MODULATION TECHNIQUES FOR POWER- AND SPECTRALLY EFFICIENT SATCOM SYSTEMS"

- SUPERPOSED QAM AND BANDLIMITED SQAM AND QPSK
- OPTIMIZED FOR NONLINEAR HIGH-POWER AMPLIFIERS
- 1.5 bps/Hz
- 64- TO 300-kbps ENGINEERING PROTOTYPE

DEMONSTRATION MODEL CONTRACT—TO BE DETERMINED "AMTD FOLLOW-ON"

- ADVANCED PACKAGING FOR SIZE, MASS, AND POWER REDUCTIONS BY FACTOR OF 3 TO 5 EACH
- 25% IMPROVEMENT IN BANDWIDTH OR POWER EFFICIENCY OVER AMTD
- ANALOG/DIGITAL CHIP SET ON BOARD-LEVEL PRODUCT

CD-89-40923

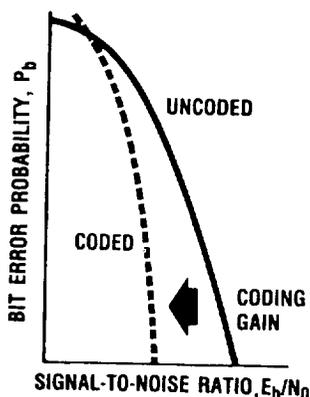
HIGH-SPEED CODECS

The curve shown below illustrates the primary goal of forward-error-correction (FEC) encoding - to reduce the received E_b/N_0 required to yield a specific probability of decoded bit error. Codecs that meet the combination of objectives shown below will provide an alternative to convolutional and block decoding approaches while preserving the best features of each. Such codecs will be well suited to onboard and ground-based processing of a variety of TDMA and FDMA signal formats in both dedicated and shared hardware applications.

DIGITAL SYSTEMS TECHNOLOGY HIGH-SPEED CODECS

NASA

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OBJECTIVES:

- RAISE UNCODED DATA RATES TO 300 Mbps
- ACHIEVE HIGH CODE RATES AND CODING GAIN
- SUPPORT SOFT DECISION DECODING AND MULTIPLE MODULATION SCHEMES
- OPERATE ON SHORT, INDEPENDENT BURSTS AND CONTINUOUS DATA
- IMPLEMENT CLSIC CHIP SETS

BENEFITS:

- REDUCED ANTENNA SIZE AND TRANSMITTER POWER
- BANDWIDTH EXPANSION LIMITED BY EFFICIENT CODES
- SUITABLE FOR TDMA AND CONTINUOUS LINKS
- IMPROVED DATA QUALITY FOR GIVEN POWER

APPLICATIONS:

- PROCESSING SATELLITES:
 - TDMA UPLINKS
 - WIDEBAND CROSSLINKS
 - SHARED DECODER AFTER BULK DEMODULATOR
 - MULTIPLE-BEAM TDM DOWNLINKS
- SATELLITE-SWITCHED TDMA TERMINALS

CD-89-40924

HIGH-SPEED CODEC APPROACH

The SBIR Phase 1 contract with Stanford Telecommunications, Inc. (STI) provided a design approach for increasing the throughput of convolutional decoders by interconnecting an array of commercially available decoders. When the contract was completed in late 1986, single-chip decoders with data rates to 10-Mbps were the state of the art. Although a Phase 2 contract was not awarded (STI was no longer a small business), their design defined a fundamental approach to high-speed decoding with high coding gain but low code rates.

Key features of the flexible, high-speed codec from Harris include its ability to utilize soft decision information, to independently decode short bursts or packets, and to yield high coding gain with high code rates. The hardware will be configurable for operation with multiple phase- and frequency-shift keying (PSK and FSK) modulation schemes. Under this demonstration model contract, Harris will implement two, independent, hard decision, 300-Mbps BCH codecs on each 50,000 gate CMOS gate array.

Under a recently awarded grant, the University of Southern California (USC) has begun investigating jointly designed decoders and equalizers to yield performance superior to that obtained from independent designs. USC will also investigate methods of exploiting soft decision information with RS decoding. In the future both techniques will be demonstrated in commercial digital signal processing hardware.

DIGITAL SYSTEMS TECHNOLOGY HIGH-SPEED CODES—APPROACH



SBIR PHASE 1 CONTRACT—STANFORD TELECOMMUNICATIONS, INC. (NAS3-24742)

“A NOVEL HIGH-SPEED VITERBI DECODER DESIGN WITH ROBUST ATTRIBUTES”

- MASSIVE PARALLEL BLOCK DECODING HARDWARE DESIGN
- ARRAY OF TWELVE 256-kbps TO 10-Mbps VITERBI DECODERS FOR 2- TO 100-Mbps THROUGHPUT

DEMONSTRATION MODEL CONTRACT—HARRIS (NAS3-25087)

“FLEXIBLE HIGH-SPEED CODEC”

- DUAL 300-Mbps BCH CODECS PER CLSIC FOR HARD DECISION
- CHASE ALGORITHM APPLIQUE FOR SOFT DECISION
- INDEPENDENT DECODING OF 256- TO 512-BIT BURSTS
- VARIABLE CODE RATES FROM 7/8 TO 15/16
- CODING GAIN > 5 dB TOTAL
- TWO 10-in. BY 10-in. BOARDS; 60-W TOTAL POWER

GRANT—UNIVERSITY OF SOUTHERN CALIFORNIA (NAG3-982)

“IMPLEMENTATION OF ADVANCED CODING CONCEPTS”

- CODESIGNED DECODER AND EQUALIZER
- REED-SOLOMON DECODING WITH FULL SOFT DECISION
- MOTOROLA DIGITAL SIGNAL PROCESSOR IMPLEMENTATION OF BOTH

DIGITAL MODEMS

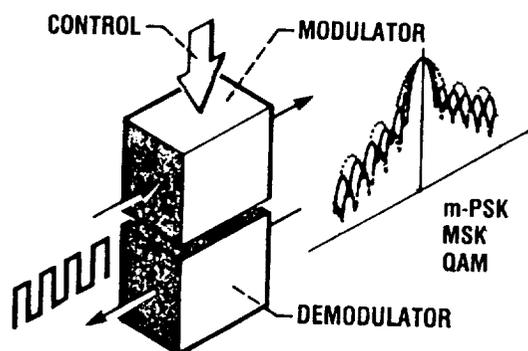
Digitally implemented modems offer significant advantages over analog modems: potential for reduced size, mass, and power consumption in very large-scale integrated (VLSI) versions; elimination of alignment, drift, and aging problems; improved reliability; reconfigurability for data rates, modulation schemes, and operational modes; and reduced production costs. A programmable digital modem has the additional advantage of being remotely reconfigurable to increase the fault tolerance of processing satellites and to enable new services over the life of the satellite. For low-cost ground terminal applications the digital modem offers the potential for implementation as a custom chip set.

Because of its digital architecture much of the nonrecurring engineering effort expended in the initial design of a digital modem can be applied to a mission-focused version. The digital approach will also benefit directly from advances in high-performance, radiation-tolerant VLSI technology.

DIGITAL SYSTEMS TECHNOLOGY DIGITAL MODEMS

NASA

Lewis Research Center



OBJECTIVES:

- MINIMIZE ANALOG COMPONENTS
- ACHIEVE RECONFIGURABLE OR PROGRAMMABLE INFORMATION BIT RATES MODULATION SCHEMES OPERATIONAL MODES
- IMPLEMENT IN DSP OR CLSIC

BENEFITS:

- SIGNIFICANTLY REDUCED COST AND RISK
- REDUCED SIZE, MASS, AND POWER OVER ANALOG
- ELIMINATION OF ALIGNMENT, DRIFT, AND AGING
- LONGER SERVICE LIFE DUE TO RELIABILITY AND RECONFIGURABILITY
- GREATER COMMERCIALIZATION POTENTIAL

APPLICATIONS:

- PROCESSING SATELLITES:
 - UPLINKS
 - CROSSLINKS
 - SHARED DEMODULATOR AFTER MULTICHANNEL DEMULTIPLEXER
 - MULTIPLE-BEAM DOWNLINKS
- COST-EFFICIENT GROUND TERMINALS

CD-89-40926

DIGITAL MODEM APPROACH

Under a Phase 1 SBIR contract TIW Systems Incorporated (formerly Multipoint Communications Corporation) outlined tradeoffs for nine critical digital modem design issues: (1) modulator data filtering; (2) clock generation; (3) carrier synthesizer; (4) demodulator automatic gain control; (5) data filtering; (6) radiofrequency oscillator phase noise; (7) carrier selectivity; (8) carrier recovery; and (9) timing recovery. For each issue Multipoint investigated multiple implementation techniques and provided specific recommendations on realizable circuit designs with special attention to utilizing digital signal processing (DSP).

The University of Toledo has also been investigating the implementation of digital QPSK burst modems. A digital demodulator design algorithm was implemented on a commercial Motorola DSP56001 evaluation board to identify limitations on information bit rate due to both the algorithm and the DSP hardware. Modifications to the software and hardware algorithms will be addressed in the parallel and pipelined version being designed to substantially increase the speed of a VLSI version.

NASA is currently negotiating a contract with COMSAT Laboratories for fabrication of a demonstration model, programmable digital modem (PDM) with the features shown below. The PDM will be programmable over six modulation schemes, the full range of data rates from 1.92 to 300 Mbps and three satellite operational modes. The proposed design offers excellent potential for a full custom VLSI chip set implementation.

DIGITAL SYSTEMS TECHNOLOGY DIGITAL MODEMS—APPROACH



SBIR PHASE 1 CONTRACT—MULTIPOINT (T.I.W. SYSTEMS) (NAS3-25336) “PROGRAMMABLE RATE MODEM USING DIGITAL SIGNAL PROCESSING TECHNOLOGY”

- BPSK AND QPSK BURST AND CONTINUOUS MODES
- ALL DIGITAL, COMMERCIAL DSP-BASED DESIGNS
- REALIZABLE CIRCUIT DESIGN TRADEOFFS ADDRESSED NINE MAJOR ISSUES

GRANT—UNIVERSITY OF TOLEDO (NAG3-865) “DIGITAL MODEM DEVELOPMENT”

- MOTOROLA DSP56001-BASED QPSK DEMODULATOR
- PARALLEL/PIPELINED VLSI TO INCREASE SPEED

DEMONSTRATION MODEL CONTRACT—(COMSAT, UNDER NEGOTIATION) “PROGRAMMABLE DIGITAL MODEM”

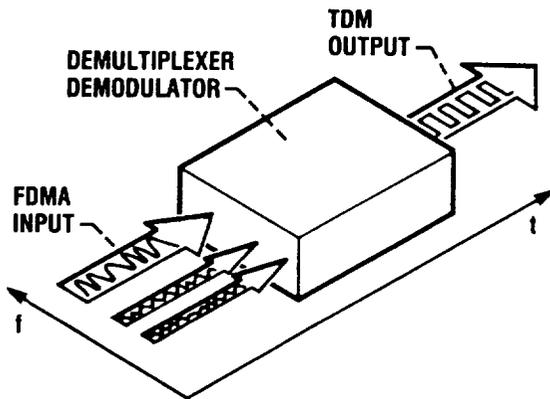
- QPSK, OPSK, 16-PSK, OQPSK, MSK, AND 16-QAM
- 1.92- TO 75-Mbps (1.92- TO 300-Mbps) CHANNEL SYMBOL RATES
- CONTINUOUS, DEPENDENT, AND INDEPENDENT BURST MODES
- FULLY PROGRAMMABLE
- MULTIPLE USE OF ECL GATE ARRAY
- UNDER 150 in.² AND 100 W TOTAL

MULTICHANNEL DEMODULATORS

The multichannel demodulator has been identified in advanced architecture studies as an enabling technology for a cost-efficient network with FDMA on the uplinks, onboard processing and switching, and TDM downlinks. The goal of this project element is to demonstrate digital and optical techniques that can be extended to enable simultaneous demultiplexing and demodulation of hundreds to thousands of channels. In an operational system the channel mix may consist of several channel bandwidths and multiple modulation techniques.

DIGITAL SYSTEMS TECHNOLOGY MULTICHANNEL DEMODULATORS

NASA
Lewis Research Center



OBJECTIVES:

- ACHIEVE SIMULTANEOUS DEMULTIPLEXING AND DEMODULATION OF HUNDREDS OF FDMA CHANNELS
- ACCOMMODATE MULTIPLE-CHANNEL BANDWIDTHS
- IMPLEMENT IN ADVANCED DIGITAL AND OPTICAL TECHNOLOGIES
- MINIMIZE GROUND SEGMENT IMPACT

BENEFITS:

- ENABLING TECHNOLOGY FOR FDMA NETWORK WITH ONBOARD PROCESSING
- REDUCED GROUND TERMINAL COSTS COMPARED WITH TDMA: LOWER EIRP AND SIMPLIFIED SYNCHRONIZATION

APPLICATIONS:

- PROCESSING AND SWITCHING SATELLITES WITH FDMA UPLINKS
- COST-EFFICIENT GROUND TERMINAL PROCESSING OF FDM DOWNLINKS

CD-89-40928

MULTICHANNEL DEMODULATOR APPROACH

Because of the importance of the multichannel demodulator to the success of future missions, a multifaceted approach is being pursued. Since the study contract by COMSAT Laboratories (see page 11), the Digital Systems Technology Branch has awarded a grant and a Phase 1 SBIR contract to investigate viable digital and optical techniques for multichannel demultiplexing and demodulation. The University of Toledo is investigating FFT techniques, and Amerasia Technology, Incorporated is applying innovative transducers and a single reflective array compressor (RAC) approach to the problem.

NASA intends to award multiple contracts for the development of multichannel demultiplexer/demodulators. A demonstration with two channel bandwidths and a total of six channels is required for proof of the proposed concept and its implementation technique.

The branch has begun an in-house activity to augment the university and industry investigations and to better understand their approaches. The short-term objective is to implement a multichannel demodulator with 144-kbps information rate channels. The microcoded implementation of a high-performance FFT processor is being pursued for the long-term solution.

DIGITAL SYSTEMS TECHNOLOGY MULTICHANNEL DEMODULATORS—APPROACH



GRANT—UNIVERSITY OF TOLEDO (NAG3-799) “FDMA/TDM CONVERSION FOR NONCONTIGUOUS CARRIERS”

- GWHT FOR LIGHTLY POPULATED SYSTEM
- PIPELINED VLSI ARCHITECTURE FOR FFT-BASED TRANSMULTIPLEXER

SBIR PHASE 1 CONTRACT—AMERASIA (NAS3-25617) “INNOVATIVE PULSE COMPRESSORS FOR SATELLITE COMMUNICATIONS”

- SAW CHIRP FOURIER TRANSFORM TECHNIQUE
- HYPERBOLIC RAC TRANSDUCER FOR FSK DEMULTIPLEXING

MULTIPLE PROOF-OF-CONCEPT MODEL CONTRACTS—TO BE ANNOUNCED “ADVANCED TECHNOLOGY FOR A MULTICHANNEL DEMULTIPLEXER/ DEMODULATOR”

- PROOF-OF-CONCEPT APPROACH EXTENDABLE TO SYSTEM WITH HUNDREDS OF CHANNELS
- FOUR NARROWBAND, TWO WIDEBAND CHANNELS
- DIGITAL AND/OR OPTICAL SOLUTIONS

LEWIS IN-HOUSE “DIGITAL SIGNAL PROCESSING FOR MULTICHANNEL DEMODULATION”

- MOTOROLA DSP56000-BASED DEMULTIPLEXER/DEMODULATOR
- SYSTOLIC ARRAY FFT PROCESSOR

CD-89-40929

VERY HIGH-DATA-RATE MODEMS

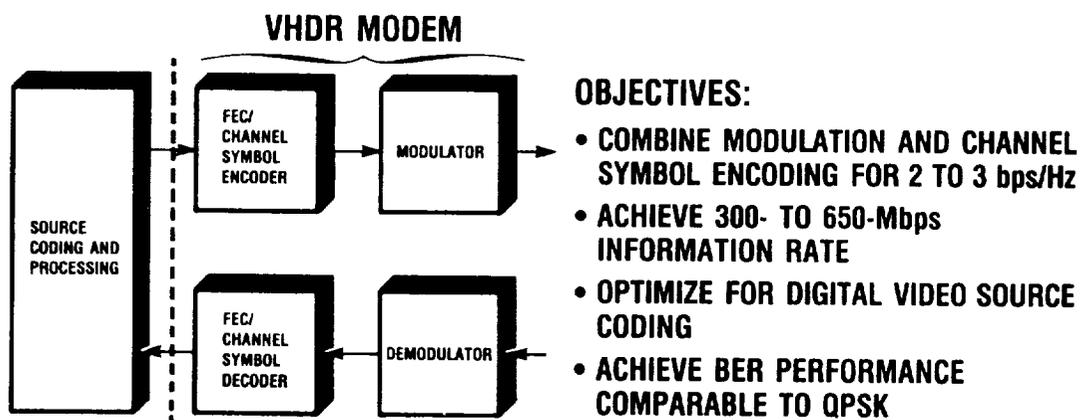
For real-time transmission of very high information rate signals (from 300 to 650 Mbps), modems with 2 to 3-bps/Hz bandwidth efficiency are required for transmitting the signals via existing and planned satellite links. Both FEC and channel symbol coding must be employed in a very high-data-rate (VHDR) modem to ensure a specific BER performance level under specific constraints imposed by the link budget.

In applications where the information present in the source signal can be compressed into a lower data rate signal, as in most digital video applications, tradeoffs among source coding, FEC coding, and channel symbol coding must be addressed in order to maximize the quality of the transmission and minimize the hardware complexity. It is anticipated that such a real-time transmission capability can enable "telescience" - ground-based control of space experiments.

The Digital Systems Technology Branch plans to discuss potential applications of the VHDR modem technology within NASA in order to establish a priority for its development. The branch will pursue its development if sufficient rationale and interest exist.

DIGITAL SYSTEMS TECHNOLOGY VERY HIGH-DATA-RATE MODEMS

NASA
Lewis Research Center



BENEFITS:

- CAPACITY DOUBLE THAT OF EXISTING WIDEBAND LINKS
- REAL-TIME TRANSMISSION OF VERY HIGH INFORMATION RATES

APPLICATIONS:

- WIDEBAND CROSSLINKS AND DOWN-LINKS FOR PROCESSING SATELLITES
- HIGH-RESOLUTION, HIGH-FRAME-RATE VIDEO TRANSMISSION (HHVT) AND TELESCIENCE

CD-89-40930

VERY HIGH-DATA-RATE MODEM APPROACH

Depending on program priorities a potential development approach would include a university grant and a demonstration model contract. The university would address modem design issues for "broadcast quality" transmission of moderate-information-rate digitized video such as the existing National Television Standards Committee (NTSC) and emerging high-definition television (HDTV) signals. A contractor would develop advanced bandwidth efficient modulation and coding techniques and VHDR modem hardware to demonstrate real-time transmission of very high-data-rate signals such as the high-resolution, high-frame-rate video technology (HHVT) signal format envisioned for microgravity science experiments.

DIGITAL SYSTEMS TECHNOLOGY VERY HIGH-DATA-RATE MODEMS—APPROACH



GRANT—TO BE DETERMINED “MODEMS FOR COMPRESSED VIDEO TRANSMISSION”

- 2- TO 3-bps/Hz BANDWIDTH EFFICIENCY
- OPTIMIZED FOR COMPRESSED NTSC AND HDTV SIGNAL FORMATS

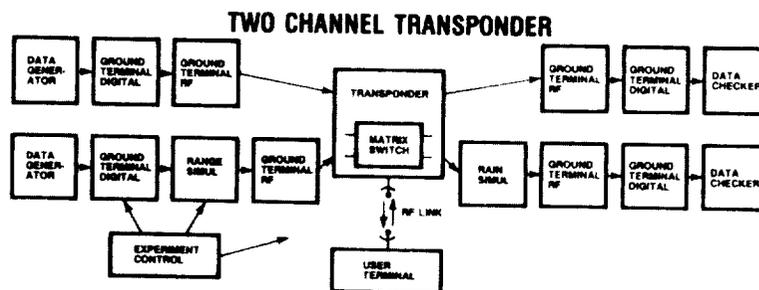
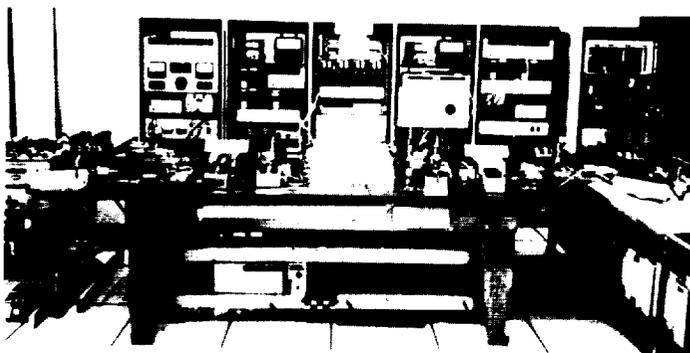
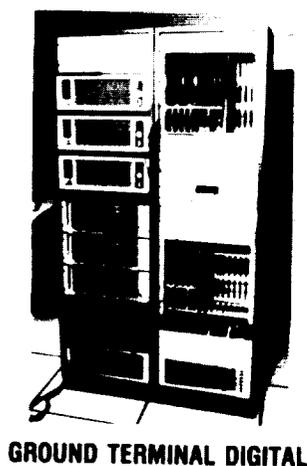
DEMONSTRATION MODEL CONTRACT—TO BE DETERMINED “VERY HIGH-DATA-RATE MODEM”

- 650-Mbps INFORMATION RATE
- NEARLY 3-bps/Hz BANDWIDTH EFFICIENCY
- RAPID SIGNAL ACQUISITION
- OPTIMIZED FOR HHVT SIGNAL FORMAT
- SUITABLE FOR DEMONSTRATION VIA ACTS HBR

POC AND DEMONSTRATION MODEL EVALUATION

A multiple-ground-terminal satellite network simulation facility has been developed under the Space Electronics Division's System Integration, Test, and Evaluation (SITE) Project. The facility integrates POC model modems, low-noise receivers, intermediate frequency matrix switches, and traveling-wave tube amplifiers with in-house-developed rain fade and range delay hardware simulators and TDMA ground terminal digital subsystems. The SITE facility has been used to characterize the performance of a variety of microwave components. In addition to repeating the acceptance testing performed by the contractors, the Digital Systems Technology Branch intends to incorporate the hardware models developed under the Advanced Modulation and Coding Project into the SITE facility for further testing and evaluation.

SITE MULTI TERMINAL NETWORK SIMULATION



- FEATURES**
- TWO CHANNEL OPERATION
 - NETWORK CONTROL
 - DYNAMIC SWITCHING
 - BURSTED DATA (229 Mb/s)
 - SIMULATED RANGE DELAY
 - REMOTE RF LINK (26.15)
 - SIMULATED RAIN FADE
 - EXPERIMENT CONTROL

CD-88-34583

SESSION II

**LEWIS BANDWIDTH EFFICIENT MODULATION
—ADVANCED MODULATION
TECHNOLOGY DEVELOPMENT (AMTD)
CHAIR: M.J. SHALKHAUSER**

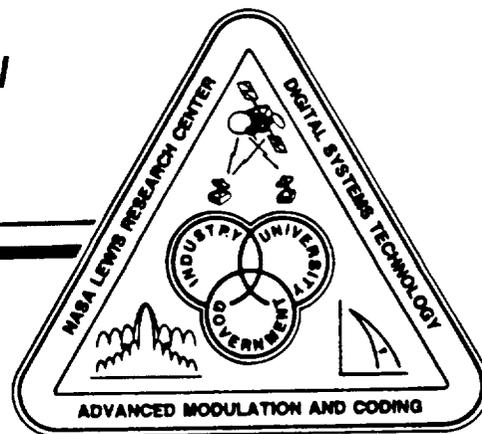
**8-PSK CODED TDMA SATELLITE DEMODULATOR
S.A. AMES
FORD AEROSPACE CORPORATION**

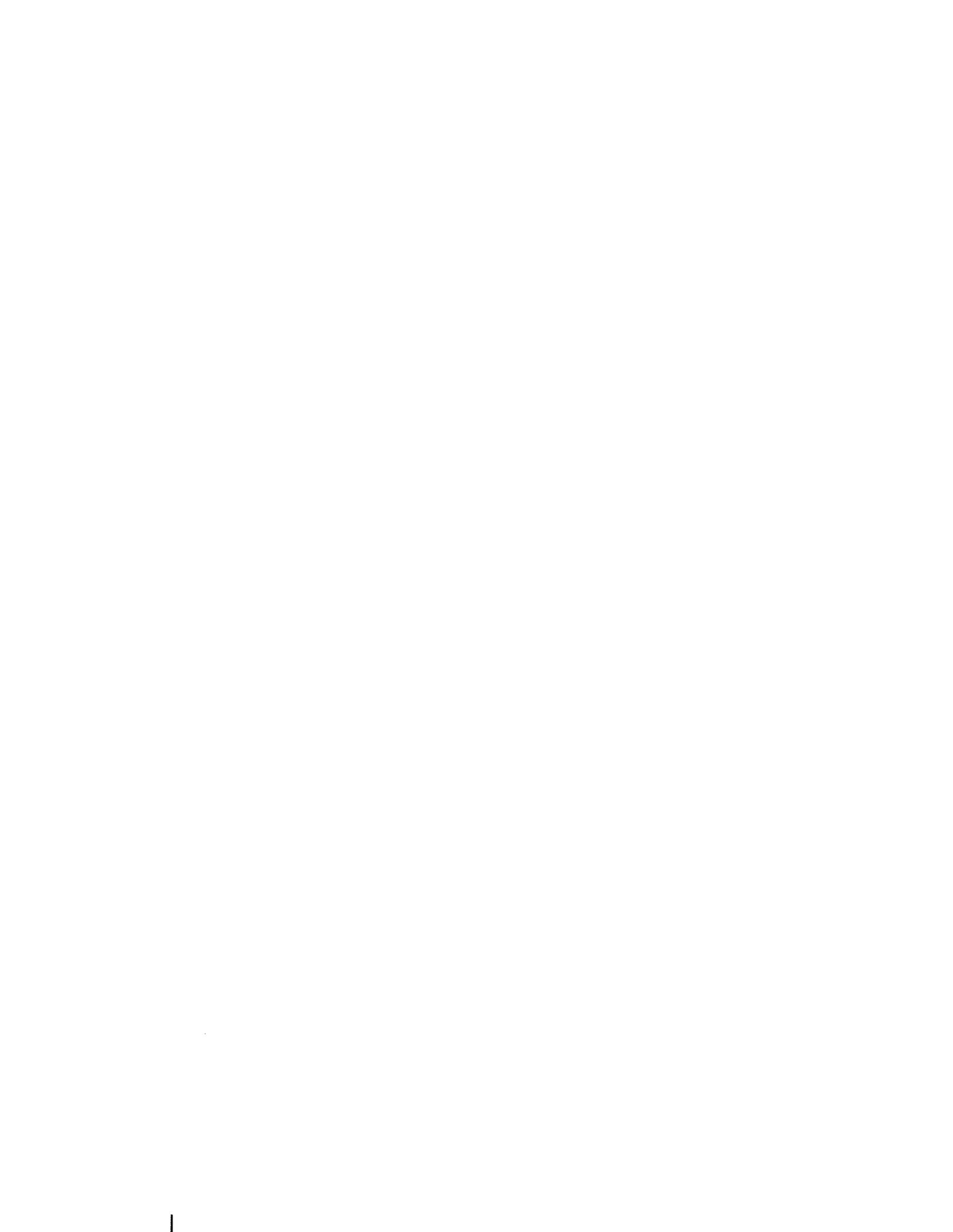
**RATE 3/4 CODED 16-QAM FOR UPLINK APPLICATIONS
E.M. MROZEK AND J.K.N. WONG
TRW, INCORPORATED**

**AN 8-PSK TDMA UPLINK MODULATION AND CODING SYSTEM
S.A. AMES
FORD AEROSPACE CORPORATION**

**RATE 8/9 CODED 8-PSK SYSTEM FOR DOWNLINK APPLICATIONS
R. FANG, M. KAPPES, AND S. MILLER
COMSAT LABORATORIES**

**CODED 16-CPFSK FOR DOWNLINK APPLICATIONS
R. DAVIS
HARRIS CORPORATION**





8-PSK CODED TDMA SATELLITE DEMODULATOR

S.A. Ames
Ford Aerospace Corporation
Space Systems Division
Palo Alto, California 94303

FINAL BRIEFING

**ADVANCED TECHNOLOGY SATELLITE DEMODULATOR
DEVELOPMENT**

NAS3-24678

**PRESENTED AT
NASA LEWIS RESEARCH CENTER
JUNE 8, 1989**

ABBREVIATIONS USED IN BRIEFING

• ACI	adjacent channel Interference
• AMTD	Advanced Modulation Technology Development
• ASIC	application specific Integrated circuit
• AWGN	additive white Gaussian noise
• BER	bit error rate
• CCI	co-channel Interference
• codec	coder/decoder
• ECL	emitter coupled logic
• MCD	multi-channel demultiplexer and demodulator
• MMIC	monolithic microwave integrated circuit
• modem	modulator/demodulator
• SAW	surface acoustic wave
• TDMA	time division multiple access

EXECUTIVE SUMMARY

- OBJECTIVES
- REQUIREMENTS
- PHASES
- COSTS AND DURATION
- PROOF-OF-CONCEPT MODEL BLOCK DIAGRAM
- PROOF-OF-CONCEPT MODEL PHYSICAL CONFIG.
- PERFORMANCE OF POC MODEL
- CONCLUSIONS OF PROGRAM
- RECOMMENDATIONS FOR FUTURE

OBJECTIVES:

- Develop a proof-of-concept uplink modulation system which will significantly increase the bandwidth efficiency of a TDMA uplink system
- Maintain present performance levels
- POC model should exhibit potential for low weight and power consumption

SALIENT REQUIREMENTS FROM RFP:

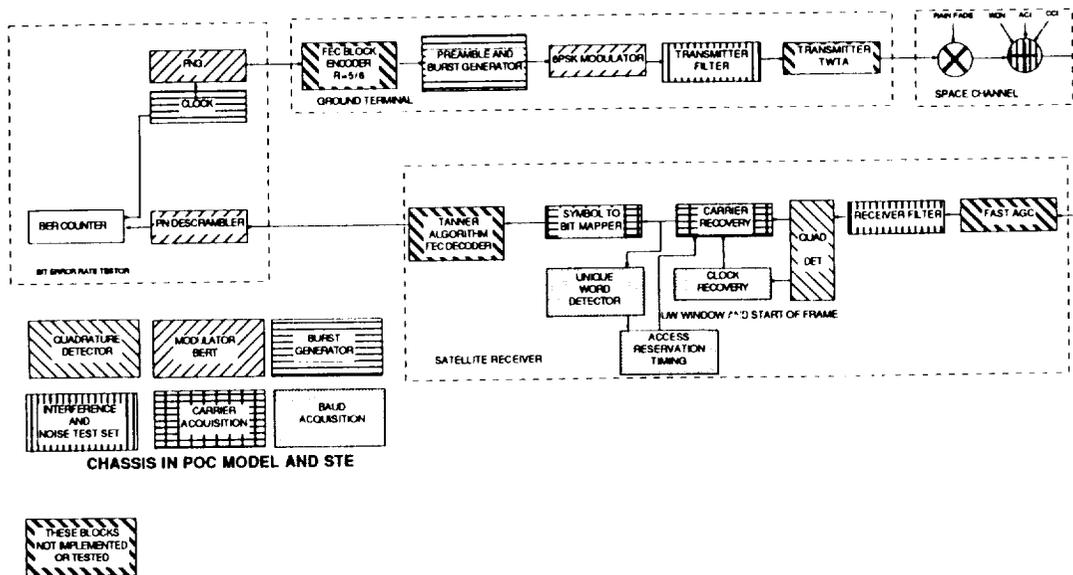
- Bandwidth Efficiency > 2 bits/ sec/ Hz
- Implementation loss < 2 dB
- 1 dB degradation in 20 db ACI or CCI
- TDMA burst mode with preamble < 100 bit periods
- Throughput > 200 Mbps

DERIVED REQUIREMENTS:

- 8PSK modulation
- Nyquist filter with rolloff factor of 0.2
- CCI spec requires forward error correction coding
- Mostly digital mechanization for eventual ASIC design

PHASES:

- Refine preliminary design
- Develop preliminary design
- Build and test breadboard
- Plan, specify, and fab POC model
- Test POC model and establish POC
- Product assurance



BLOCK DIAGRAM OF GROUND AND SATELLITE TDMA TEST SYSTEM

CONCLUSIONS OF PROGRAM

- CONCEPT OF THE POWER AND BANDWIDTH EFFICIENT SATELLITE DEMODULATOR HAS BEEN PROVEN WITHIN THE BUDGETARY CONSTRAINTS OF THE PROGRAM
- BANDWIDTH EFFICIENCY COULD BE DEMONSTRATED (I.E., ACI SPEC MET) THROUGH FILTER IMPROVEMENTS
- POWER EFFICIENCY COULD BE DEMONSTRATED (I.E., BER SPEC MET IN AWGN) THROUGH IMPROVEMENTS IN CLOCK RECOVERY LOOP AND FILTERS
- DIGITAL PORTION OF THE SATELLITE DEMODULATOR COULD BE REALIZED IN TWO GATE ARRAYS PLUS SOME MEMORY CHIPS, ANALOG PORTION COULD BE GREATLY REDUCED IN SIZE AND WEIGHT BY UTILIZING SAW FILTERS AND AN MMIC QUADRATURE DETECTOR
- CODEC PERFORMANCE WITH DEMOD IN CCI PROVEN BY SIMULATION

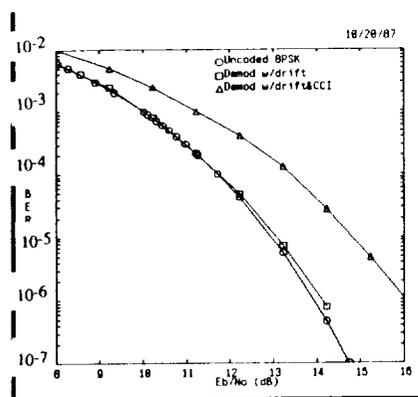
RECOMMENDATIONS FOR FUTURE

- CONTINUE SATELLITE MODEM DEVELOPMENT IN COMPACT FORM
 - (A) ASIC REALIZATION OF DIGITAL PORTION (TWO ECL GATE ARRAYS)
 - (B) DEVELOPMENT OF STEEP SKIRTED NYQUIST FILTERS IN SAW TECHNOLOGY AT ABOUT 300 MHz
 - (C) MMIC OR HYBRID QUADRATURE DETECTOR AND LO
- CONTINUE DEVELOPMENT OF SATELLITE CODEC IN ASIC
- CONTINUE DEVELOPMENT OF LOW BIT RATE MCD IN ASIC AND/OR DSP

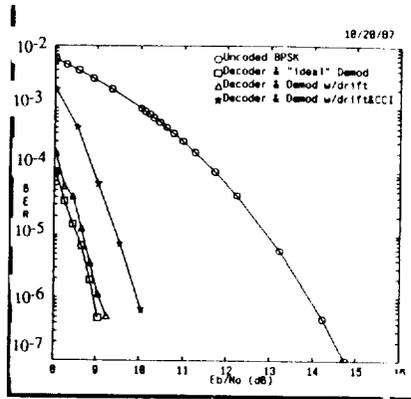
SPECIFICATIONS OF POC MODEL

PARAMETER	VALUE	TEST SPEC. NO. OR METHOD OF DETERMINING COMPLIANCE
Bandwidth Efficiency	> 2 Bits/sec/Hz	1
Bit Rate	240 Mbps	by design
Channel Spacing	96 MHz	by design
Transmission Mode	TDMA	by design
Frame Length	1 ms	by design
Preamble (CW portion) (UW portion)	32 symbols 8 symbols	by design
Receive Frequency	3.373056 GHz±1.5KHz	by design
Input level at receiver filter	-30 dBm±0.5 dB	by design
BER at Es/No=21 dB	$< 5 \times 10^{-7}$	2
Degradation Due to +20 dB ACI	< 1 dB	3
Degradation Due to -20 dB CCI	< 1 dB	3
Probability of bit error due to missing unique word	$< 1 \times 10^{-7}$ at Es/No =13 dB	by computation (4)
Probability of Carrier Cycle Slip	< TBD at Es/No= TBD dB	5
Bit-timing Jitter	< 125 ps RMS	6
Probability of Clock Cycle Slip	< TBD at Es/No=TBD dB	7
Minimum Guard Time Between Bursts	25 ns	by design of STE

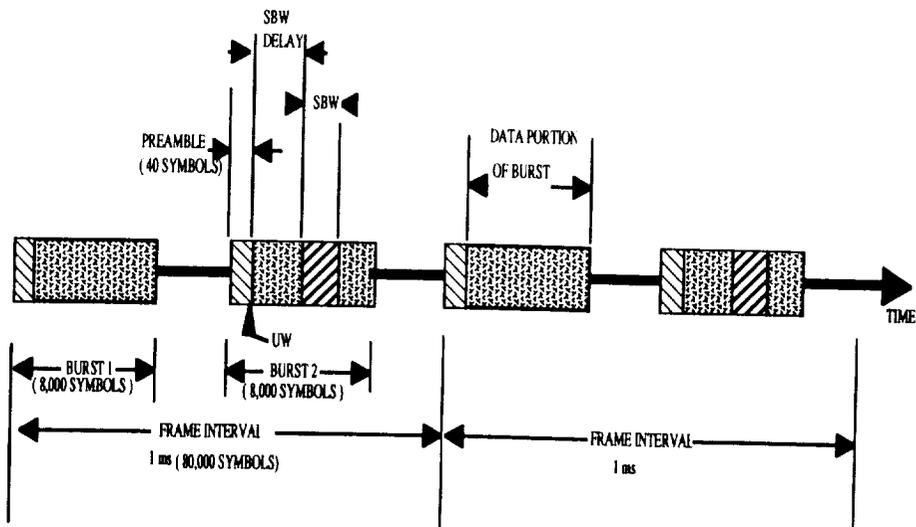
SIMULATIONS OF DEMOD PERFORMANCE WITH DRIFT AND CCI

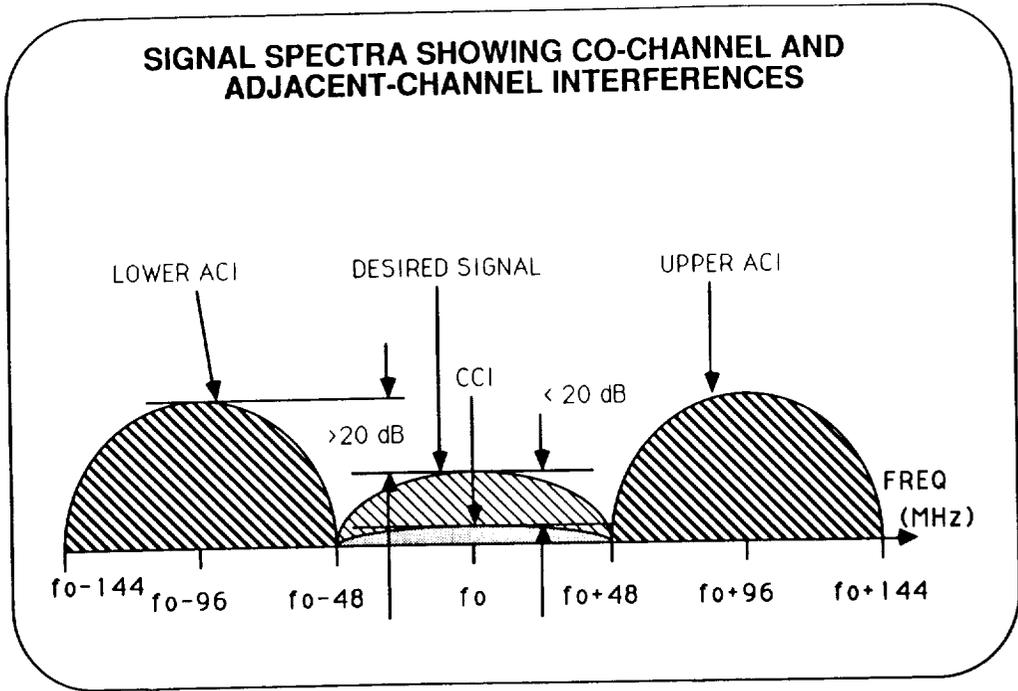


SIMULATIONS OF DEMOD AND DECODER PERFORMANCE WITH DRIFT AND CCI



PREAMBLE AND BURST STRUCTURE





AMTD INTERFERENCE AND NOISE TEST SET CHASSIS

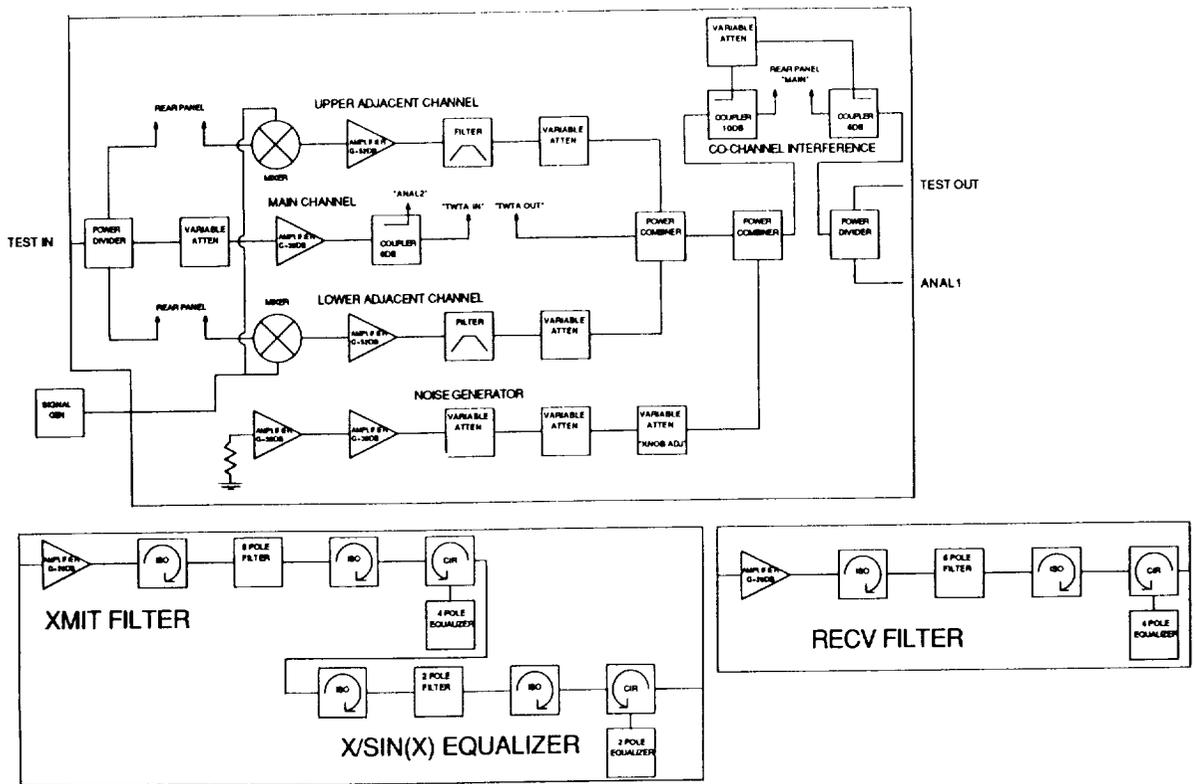
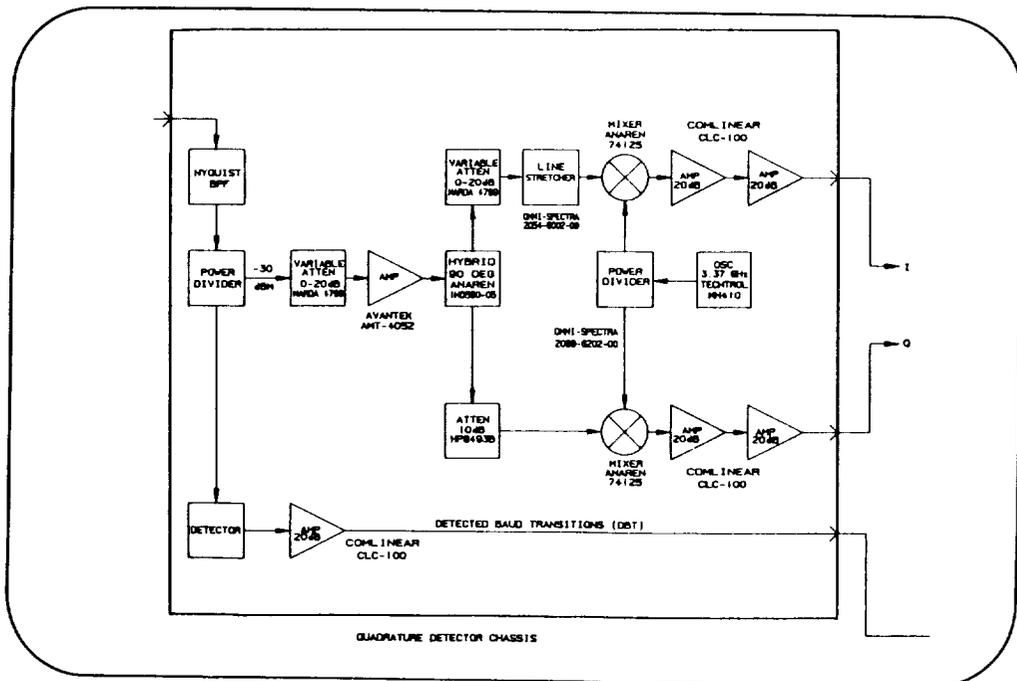
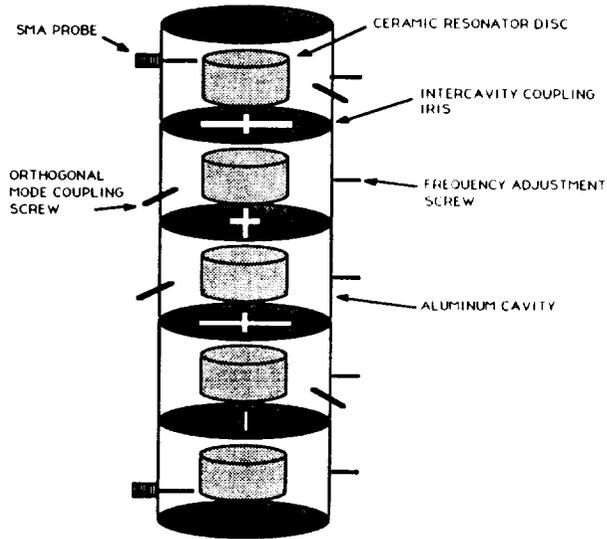
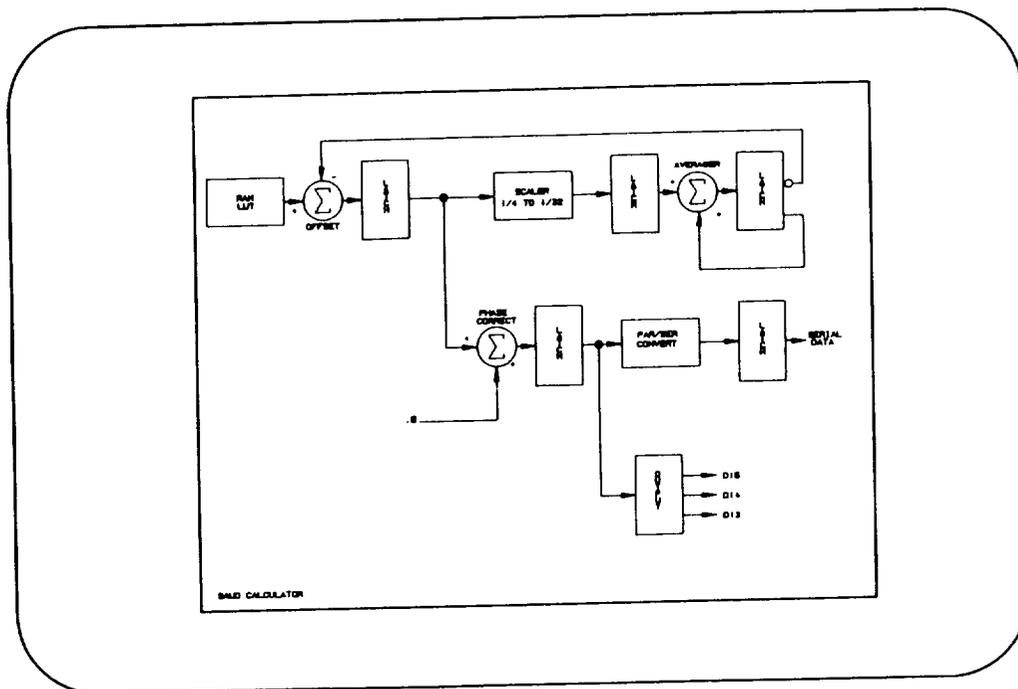
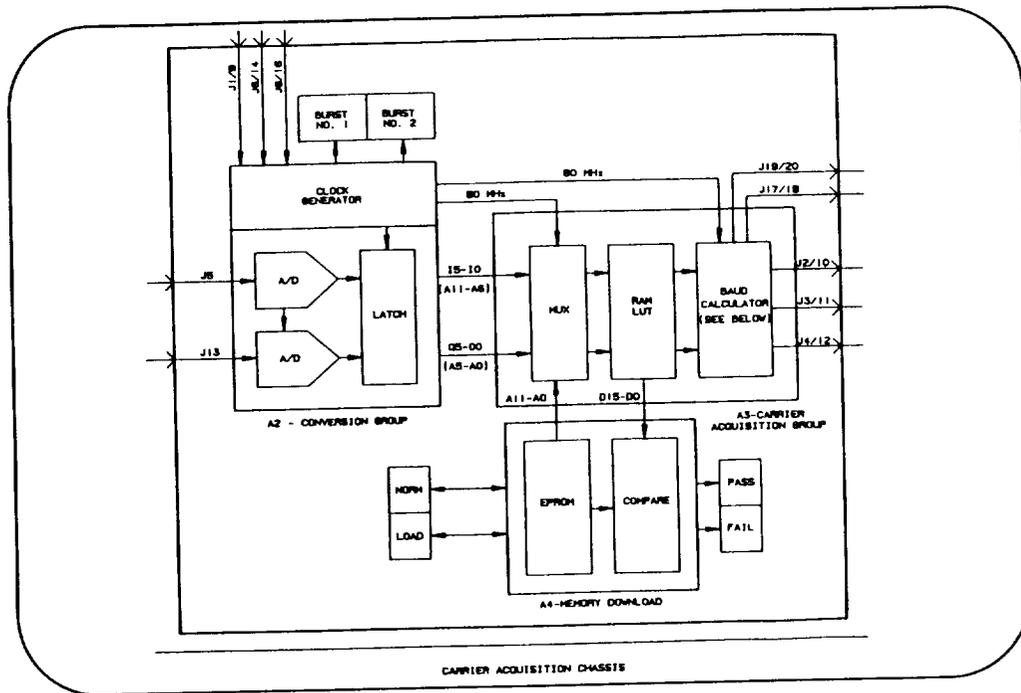


Figure 1 Interference/Noise Generator Block Diagram

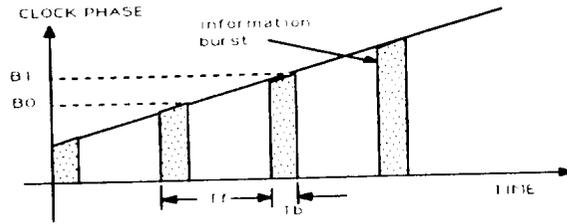
MECHANICAL CONFIGURATION OF NYQUIST FILTERS

9 Pole Dielectric Resonator Filter



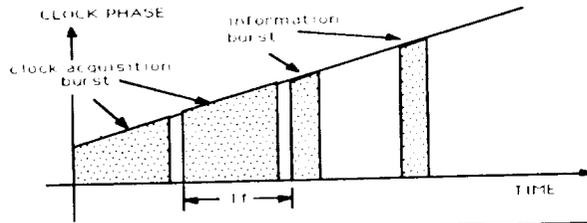


SYMBOL CLOCK ACQUISITION

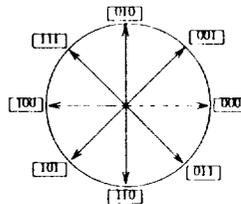


$$\text{phase slope} = (B1 - B0) / T_f$$

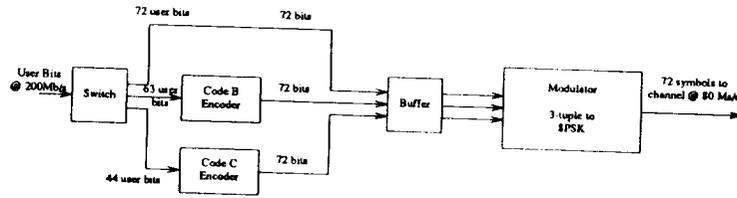
$$\text{phase correction} = \text{phase slope} \cdot (T_f - T_b) = (B1 - B0) \cdot (T_f - T_b) / T_f$$



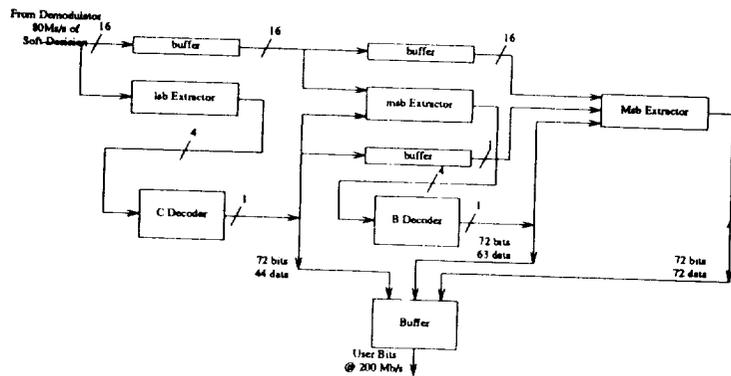
SIGNIFICANT BIT 8PSK TO 3-TUPLE MAPPING



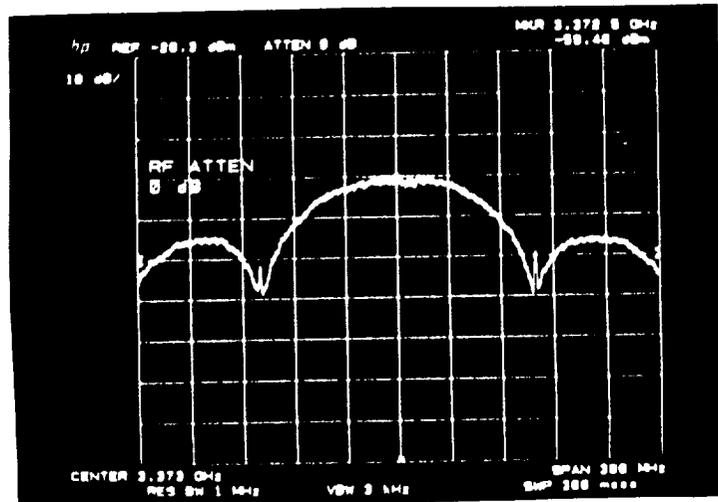
ENCODER SYSTEM



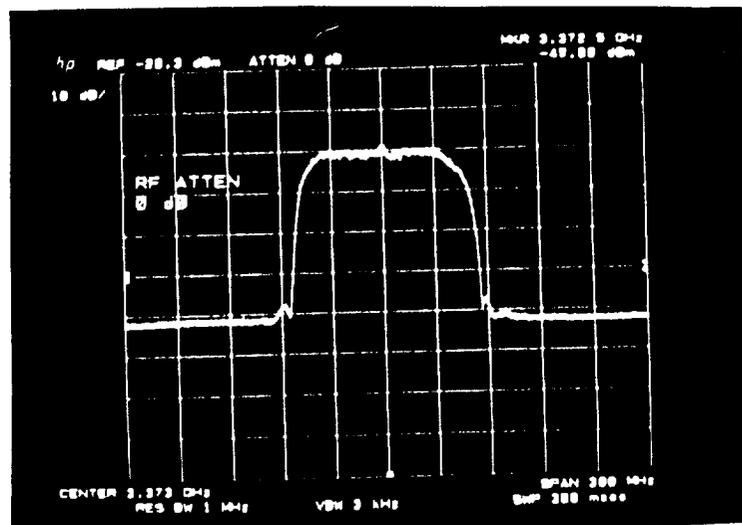
DECODER SYSTEM



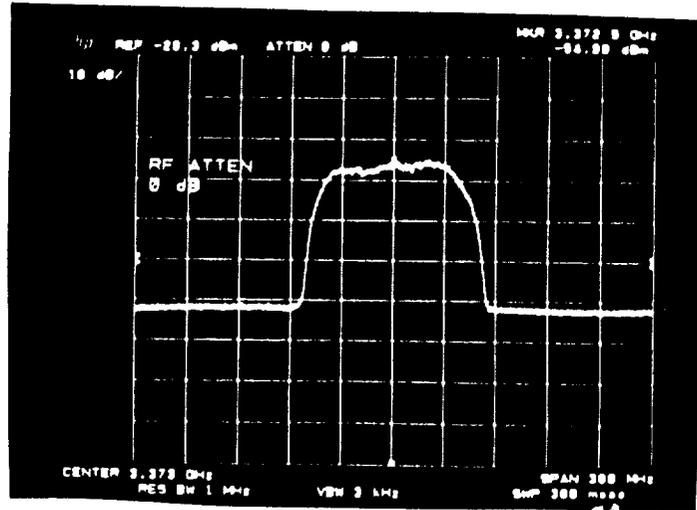
MODULATOR OUTPUT SPECTRUM



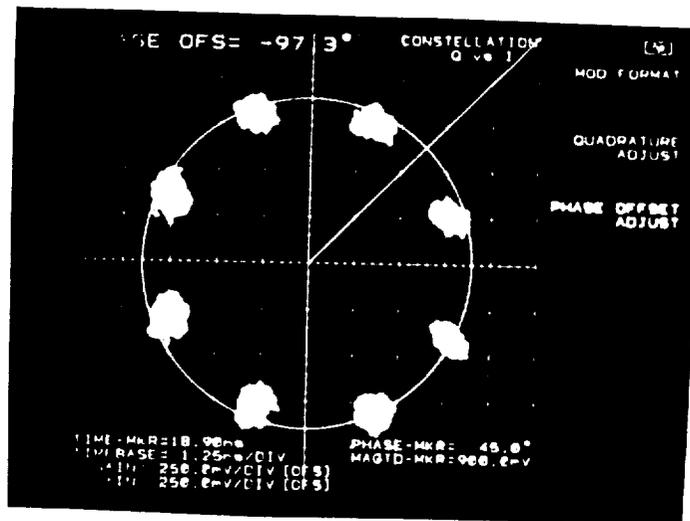
TRANSMITTER FILTER OUTPUT SPECTRUM



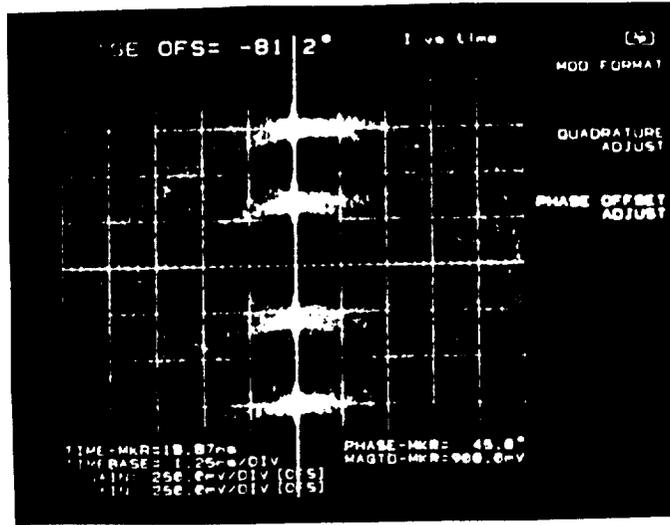
RECEIVER FILTER OUTPUT SPECTRUM



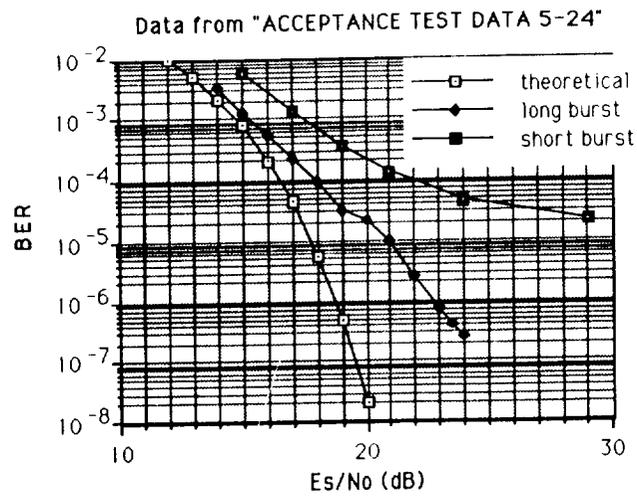
CONSTELLATION OUTPUT AT RECEIVER QUADRATURE DETECTOR



EYE PATTERN AT "I" SIDE OF QUADRATURE DETECTOR

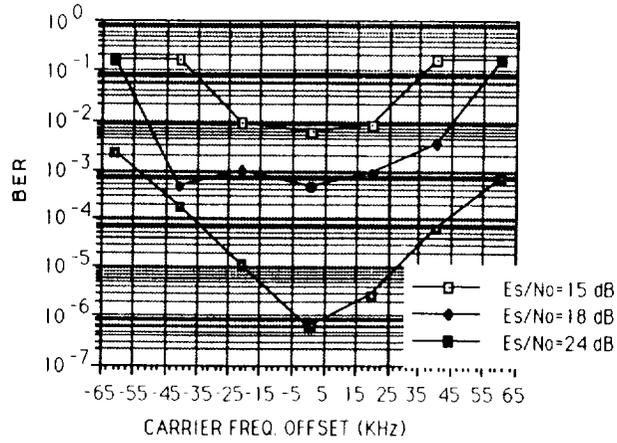


BIT ERROR RATE VERSUS E_s/N_0 IN AWGN FOR LONG AND SHORT BURSTS



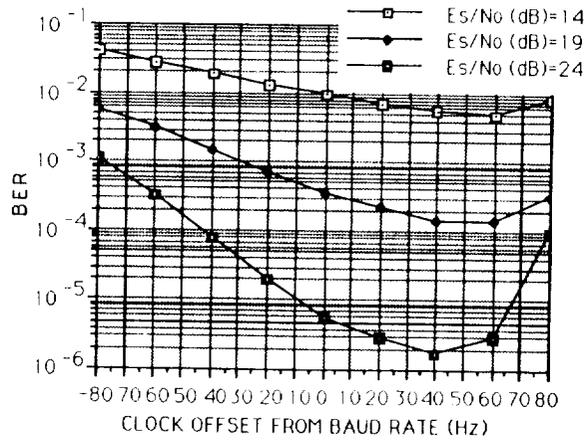
BER VERSUS CARRIER FREQUENCY OFFSET

NOTE: CLOCK OFFSET < 2 HZ

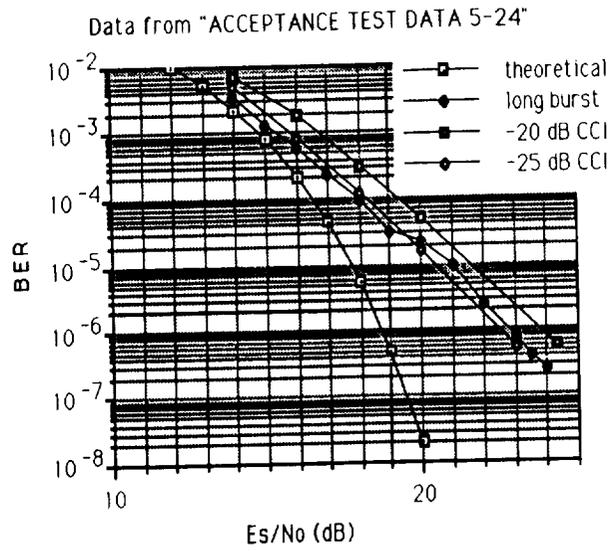


BER VERSUS CLOCK OFFSET FREQUENCY

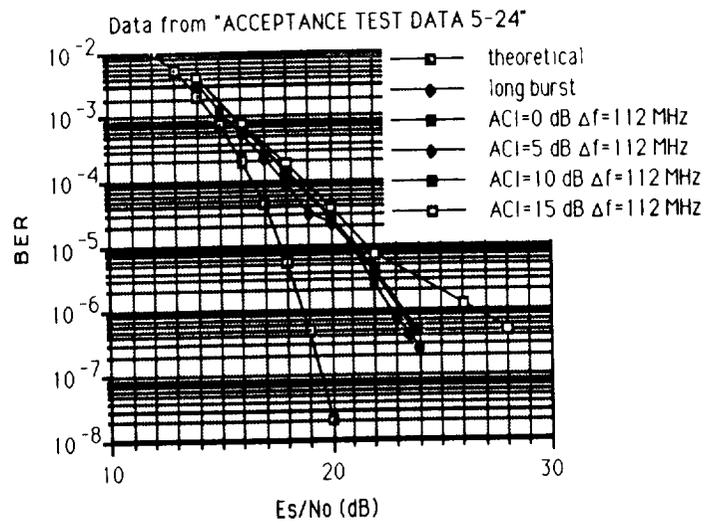
DATA SHEET 10 1 5/10/89



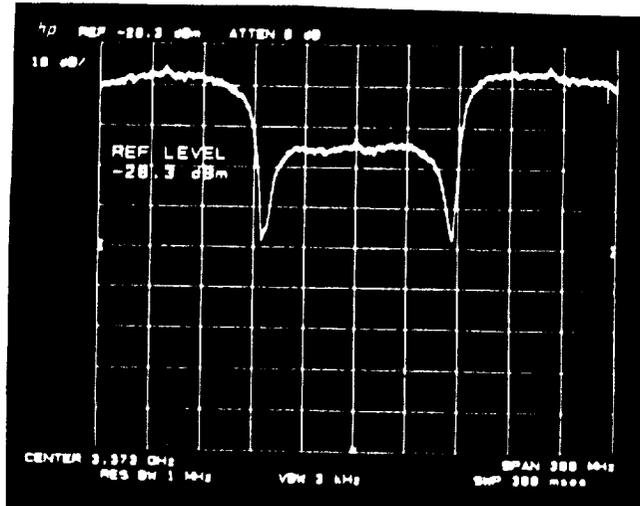
BER VERSUS ES/NO IN CCI



BER VERSUS Es/No IN ACI FOR 112 MHz SPACING



INPUT SPECTRUM TO RECEIVER WITH +20 dB ACI AT ± 112 MHz



N 9 2 - 2 2 0 0 4

RATE 3/4 CODED 16-QAM FOR
UPLINK APPLICATIONS

Eric M. Mrozek and Jerry K.N. Wong
TRW - Electronic Systems Group
Redondo Beach, California 90278

ABSTRACT

First phase development of an advanced modulation technology which synergistically combines coding and modulation to achieve 2 bits per second per Hertz bandwidth efficiency in satellite demodulators is nearing completion. A proof-of-concept model is being developed to demonstrate technology feasibility, establish practical bandwidth efficiency limitations, and provide a data base for the design and development of engineering model satellite demodulators. The basic considerations leading to the choice of 4x4 Quadrature Amplitude Modulation (16-QAM) and its associated coding format are discussed, along with the basic implementation of the carrier and clock recovery, automatic gain control, and decoding process. Preliminary performance results are presented. Spectra for the modulated signal and its interferers show the effect of the nonlinear channel. The envelope of the modulated signal shows the effects of the square root Nyquist filters in the modulator. BER results for the Encoder/Decoder subsystem show near ideal results, although power consumption is high and baseband BER performance of the Nyquist filter set is poor. Recommendations regarding the present system to improve BER performance and acquisition speed are given.

SYSTEM DESIGN

Objective (Statement of Work 0.1)

- Develop POC model of a satellite demodulator with associated special test equipment
- Significantly increase BW efficiency
- Maintain present system performance levels
- Exhibit potential for low weight and power consumption

Modulation System Requirements (SOW 3.1)

- FDM/TDMA uplink
- Single modulator & transmitter per channel
- Channel nonlinearity = TWTA (provided by NASA)
- Fixed burst rate = 200 Mbps
- Variable length of data portion of burst (range = same as preamble length to length for 1 ms burst)
- IF demodulation at 3.373 GHz. (assumes linear low noise receiver)
- 2 adjacent channels identical to desired channel but 20 dB higher in level
- 1 co-channel interferer identical to desired signal but uncorrelated and 20 dB lower in level

Performance Requirements (SOW 3.2.2)

Parameter	Specification	Performance/Operation
Bandwidth Efficiency	≥ 2 bits/s/Hz	1.998 bits/s/Hz
E_s/N_0 degradation at 5×10^{-7} BER	≤ 2 dB	TBM
Dynamic Range for BER Spec.	20 dB (maximum)	20 dB
Time to Acquire Synchronization	≤ 100 information bit times	192 info bits times
Probability of Acquisition Failure	$\leq 10^{-8}$	TBM
Unique Word Length	≤ 20 bit times	12 bit times
BER Degradation for ACI	≤ 1 dB	TBM
BER Degradation for CCI	≤ 1 dB	TBM
Guard Time	10 nsec (minimum)	30 nsec
Burst Rate Instability	$\pm 5 \times 10^{-7}$ (maximum)	$\pm 5 \times 10^{-7}$
Mean Time to Cycle Slip (at $E_s/N_0 = 3$ dB less than for BER Spec)	$\geq \text{Preamble Length} \times 10^4$	TBM

SYSTEM DESIGN (continued)

Modulation/Coding Scheme Tradeoffs

A given information rate can be communicated in a smaller bandwidth by using a higher order modulation format (larger M , where M = the number of modulation states), but at the expense of bit error rate (BER) performance. To meet the bandwidth efficiency given in the system requirements and provide for protection against adjacent channel interference (ACI), an $M = 16$ modulation is desirable. The other formats investigated couldn't meet the bandwidth efficiency requirements or performed poorly. 16-PSK could theoretically yield excellent performance, but the phase accuracy required for efficient coherent detection is unrealistic. The uplink also does not have as strong of a requirement as the downlink to use the high power amplifier (HPA) optimally by continuously running it in saturation. 4,12 circular quadrature/amplitude modulation (QAM) has the advantage of only two power levels which could allow easier compensation of the high power amplifier (HPA) nonlinearity by the use of predistortion, but 4x4 -QAM is simpler in that each quadrant has independently selected, equally spaced quadrature levels. The ideal performance of coded 4x4 -QAM is also slightly better than coded 4,12 circular QAM. Of the 16-ary modulations, the 4x4 rectangular constellation is the most practical choice for both performance and implementation.

Forward error correction (FEC) coding of rate $p = 3/4$ yields 3 information bits per 16-QAM symbol, so that an information bit rate of $R_b = 201$ Mbit/s is obtained from a modulation speed of only $R_s = 67$ Msymbol/s. Consequently, Nyquist filtering with 30 - percent rolloff can be employed so that the coded 16-QAM power spectrum occupies only about 87 MHz of a 100-MHz channel. This provides frequency guard space for protection against ACI. A simple FEC code of only 8 states provides an asymptotic gain of 5.3 dB for coded 4x4 -QAM relative to uncoded 8-PSK.

CANDIDATE NUMBER	CODE RATE	MODULATION TECHNIQUE	SYMBOL RATE (MSymbol/s)	B/R _s for B = 100 MHz	ASYMPTOTIC CODING GAIN RELATIVE TO 8-PSK.		NUMBER OF STATES IN DECODER
					AVERAGE	PEAK	
1	5/6	8-PSK	80	1.25	5.0	5.0	8
2	5/6	8-PSK	80	1.25	6.3	6.3	16
3	8/9	8-PSK	75	1.33	4.3	4.3	8
4	8/9	8-PSK	75	1.33	4.3	4.3	16
5	3/4	16-PSK	67	1.50	4.0	4.0	8
6	3/4	16-PSK	67	1.50	4.4	4.4	16
7	3/4	16-QAM (4X4)	67	1.50	5.3	2.5	8
8	3/4	16-QAM (4X4)	67	1.50	6.1	3.6	16
9	3/4	16-QAM (4,12)	67	1.50	4.7		8
10	3/4	16-QAM (4,12)	67	1.50	5.1		16
11	1	COHERENT 8-CPFSK H=0.125, N=2	67	1.50	-1.7		16
12	1	COHERENT MULTI-H CPFSK	67	1.50			256

Modulation/Coding Choice

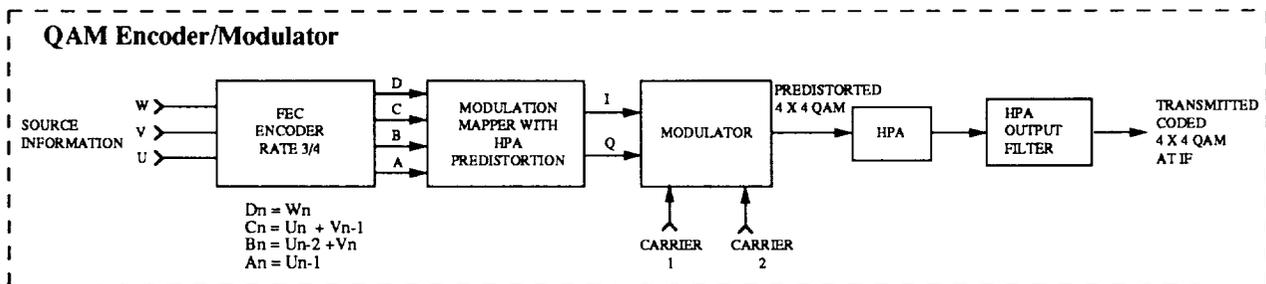
Coded 4x4 16-QAM was selected as the uplink modulation/coding choice for bandwidth efficiency, implementation simplicity, and power efficiency. Bandwidth efficiency is provided by using a large modulation alphabet of $M = 16$. The linear structure of the 4x4 square constellation allows some simplification in implementing the modulation and demodulation. FEC coding, soft detection, and Viterbi decoding provide power efficiency.

SYSTEM DESIGN (continued)

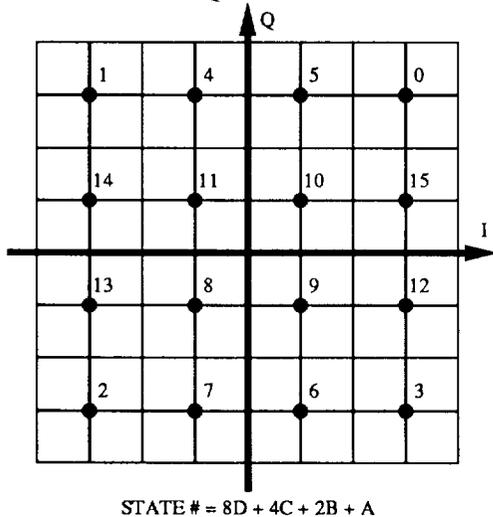
With the use of FEC coding of rate $p = 3/4$, coded 16-QAM conveys three information bits per 16-ary modulation symbol. Thus, an information rate of 201 Mbit/s can be obtained with a modulation rate of only 67 Msym/s, which can be sent in an allocated bandwidth of 100 MHz for a bandwidth efficiency of 2 b/s/Hz. The D bit of the encoded symbol causes modulation state changes with the highest minimum Euclidean distance, so it is left uncoded, allowing maximum coding for the other bits.

The nonlinear uplink channel is a traveling wave tube amplifier (TWTA). It is used at zero backoff and the nonlinearity is partially compensated for by adjusting the modulator to phase and amplitude predistort the constellation. Residual signal scatter however, will still exist due to ISI. The spectral regrowth from the HPA requires some filtering to suppress ACI [Rhodes, 1972], so the simulations also included a four pole elliptical filter at the HPA output with ideal group delay equalization.

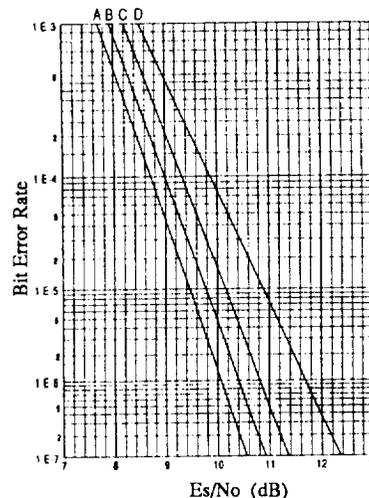
The computer simulated BER performance of the selected modulation/coding system is shown below. It assumes a 64 symbol (192 info bit times) preamble length for carrier and clock recovery with independent operation of the automatic gain control (AGC). The simulations were made down to $BER = 1 \times 10^{-4}$ and extrapolated to extend to 1×10^{-7} . Curve A shows the Average White Gaussian Noise (AWGN) performance in a linear channel. Curve B is the performance in the nonlinear uplink channel. Curve C is the nonlinear channel performance with ACI. Curve D is the nonlinear channel performance with co-channel interface (CCI). These extended curves show that, at $BER = 5 \times 10^{-7}$, the nonlinear channel itself degrades system performance 0.4 dB from the ideal theoretical case, leaving 1.6 dB for degradation due to hardware implementation. ACI degrades nonlinear channel performance by 0.5 dB (specification = 1 dB) and CCI degrades nonlinear channel performance by 1.4 dB (spec= 1 dB).



IDEAL 4X4 QAM PHASE PLANE



CODED 4x4 QAM COMPUTER SIMULATION RESULTS



DEMODULATOR/DECODER IMPLEMENTATION

Ringling Filters

Ringling filters (narrowband low-order bandpass filters) are superior to phase-locked-loops (PLLs) in TDMA communication systems. Although the two approaches have similar noise performance and the PLL is usually less complex, the absence of "hangup effect" in the ringling filter is a great advantage. The tuned filter (assuming it rings up from a "quenched" state) also exhibits an inherently faster phase transient. [Gardner, 1976]. Two sets of ringling filters are used in both the carrier recovery and clock recovery. Because of the extremely short guard time between bursts we "ping-pong" between the two sets of filters and quench one set while the second set is ringling up on the new burst. The carrier frequency is generated from the suppressed carrier QAM by remodulation techniques and separated from spurious products by the ringling filter. The clock frequency is generated from the detected data using a squaring nonlinearity.

Frequency Controlled Loop

Because of the various sources of frequency drift (such as the local oscillator in the transmitter, doppler offsets, and the tuning of the ringling filter) some method of frequency tracking is necessary. It is also desirable to downconvert the modulated signal to a frequency where lower cost components are available, so a frequency controlled loop is used. The carrier frequency is kept in the center of the filter by controlling the downconversion oscillator via detection of the average phase shift (over many bursts) through the ringling filter in the carrier recovery. The system design study showed the sensitivity of the system performance to inaccuracies in clock recovery to be much less than for carrier recovery making frequency control for the clock unnecessary.

Automatic Gain Control

The 20 dB dynamic range of the input signal requires some form of gain control for correct detection and decoding. The AGC was implemented in the demod portion of the Demodulator/Decoder. The carrier recovery and I/Q Detection circuits are slightly sensitive to the signal power, so a "coarse" AGC is used in the front end to reduce the dynamic range to 2 dB as fast as possible. A "fine" AGC is then used immediately before soft detection to further reduce the range to a level acceptable for proper operation of the Viterbi decoder.

Detection Filter

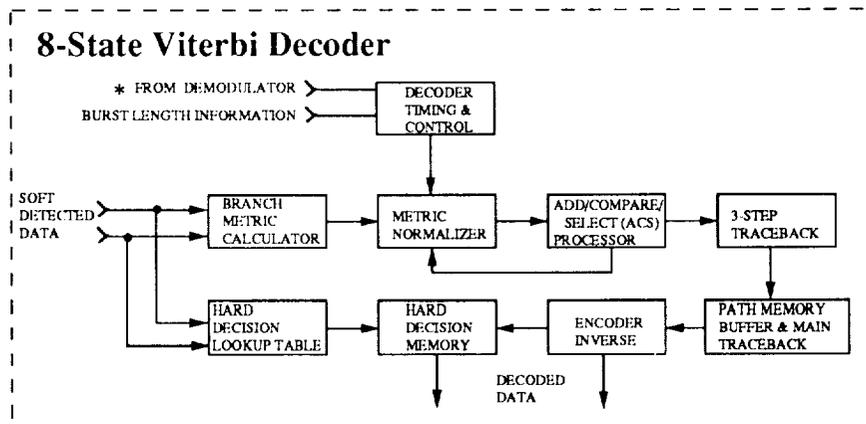
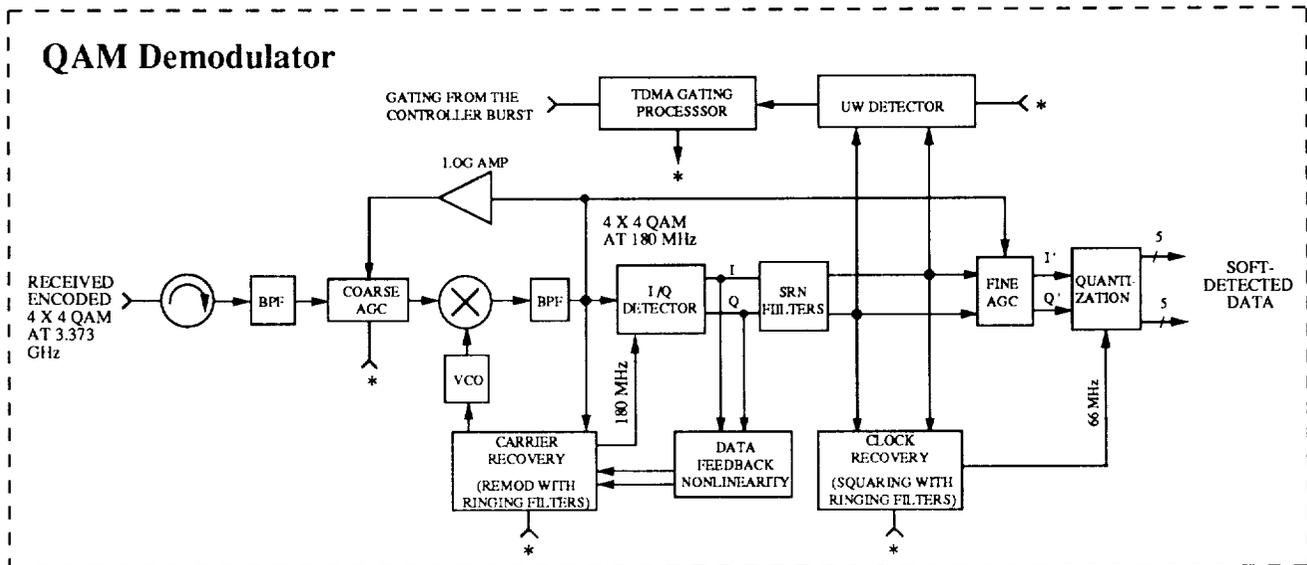
Achieving 2 bits/s/Hz bandwidth efficiency requires a highly bandlimited system. Correct regeneration of an original impulse stream can be obtained in a minimum bandwidth by avoiding intersymbol interference (ISI) through the use of special channel filtering. The basic filter characteristic is an ideal linear-phase "brick wall" filter, having a single-sided cutoff frequency of half the symbol rate ($f_c = f_s/2$), although practical filters are realizable since cutoff symmetry is allowable. [Nyquist, 1928]. For optimal BER performance the Nyquist filter is equally split between the modulator and the demodulator [Feher, 1983]. An inverse sinc amplitude function is also included in the modulator to account for the pulse shape of the nonreturn to zero (NRZ) data stream that is used.

Decoder

The encoder leaves one uncoded information bit in each symbol and has 3-bit memory, implying 8 code states with 4 input branches for each state. The uncoded bits (1 bit for each symbol) are decoded by a hard decision, with the correct axis chosen at the completion of the decoding process. The branch metric calculations are made using a lookup table, and the results are used by the state metric calculator to compute the accumulated path metrics. Selection of the minimum path metric is

DEMODULATOR/DECODER IMPLEMENTATION (continued)

performed in parallel by 6 high speed comparators, and normalization is used to prevent accumulated path metrics from overflowing. The traceback is partitioned into a 3-step traceback (to lower the traceback rate by a factor of three, allowing the use of TTL/CMOS logic) and a main traceback with an 8 symbol path memory length. Finally, the encoder inverse transforms the estimates of the input state sequence into information bits and selects the appropriate axis for the hard decisions.



PERFORMANCE RESULTS

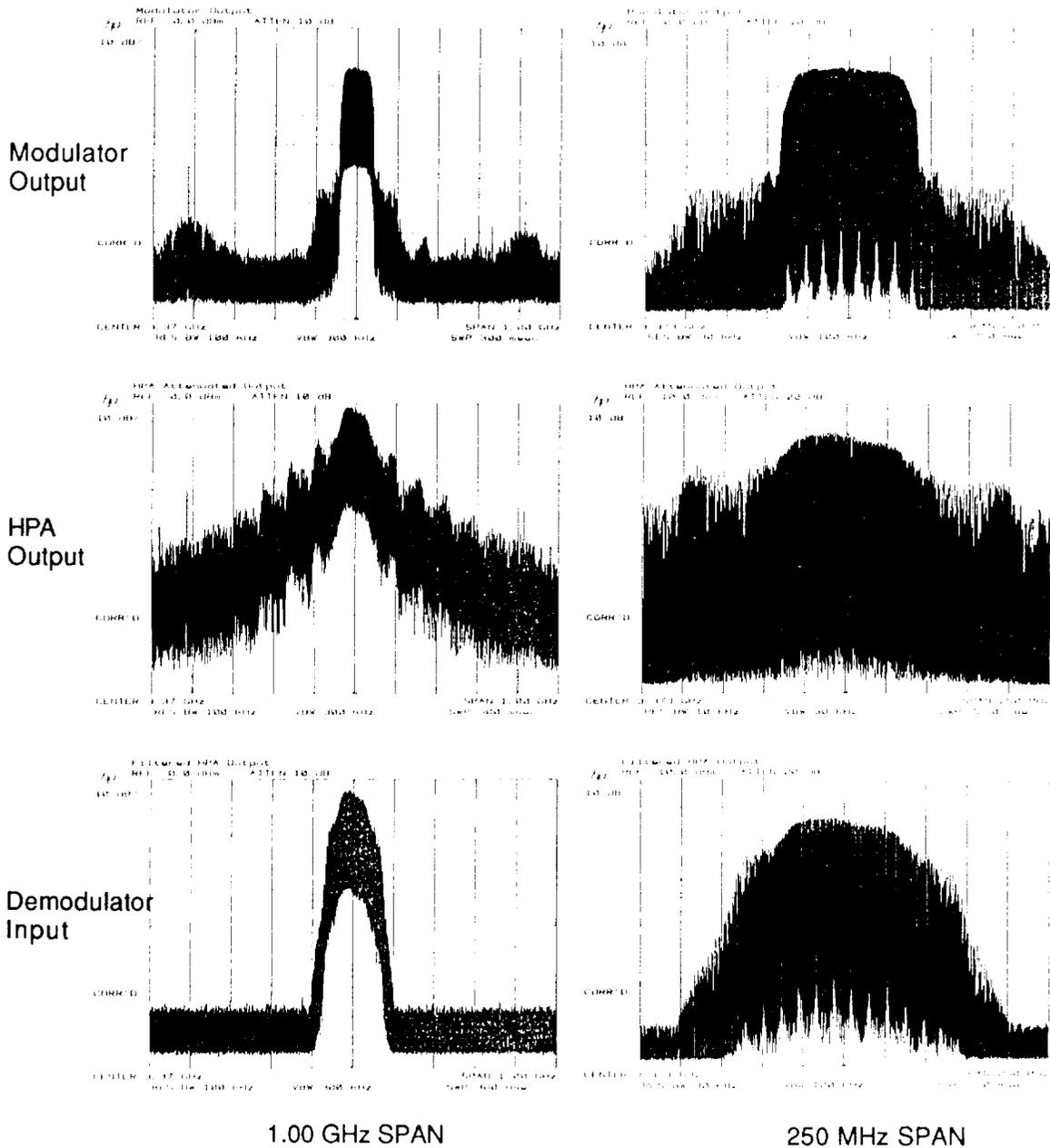
Bandwidth Efficiency

The bandwidth efficiency is a function of several parameters: Channel bandwidth (100 MHz), modulation alphabet size (16 = 4 bits/symbol), symbol burst rate (66.666 MSymbol/sec), coding rate (3/4), guard time (2 Symbols), unique word length (4 Symbols), preamble length, and the length of the data portion of the burst. All of these parameters except the last two have been predetermined by the system design. A preamble length of 64 symbols (192 information bit times) was chosen in the system design phase but the hardware is variable. This length results in a maximum length burst efficiency (burst length = 1ms) of 1.998 bit/s/Hz, and a minimum length burst efficiency (data length = preamble length) of 0.955 bit/s/Hz.

PERFORMANCE RESULTS (continued)

Signal Power Spectrum

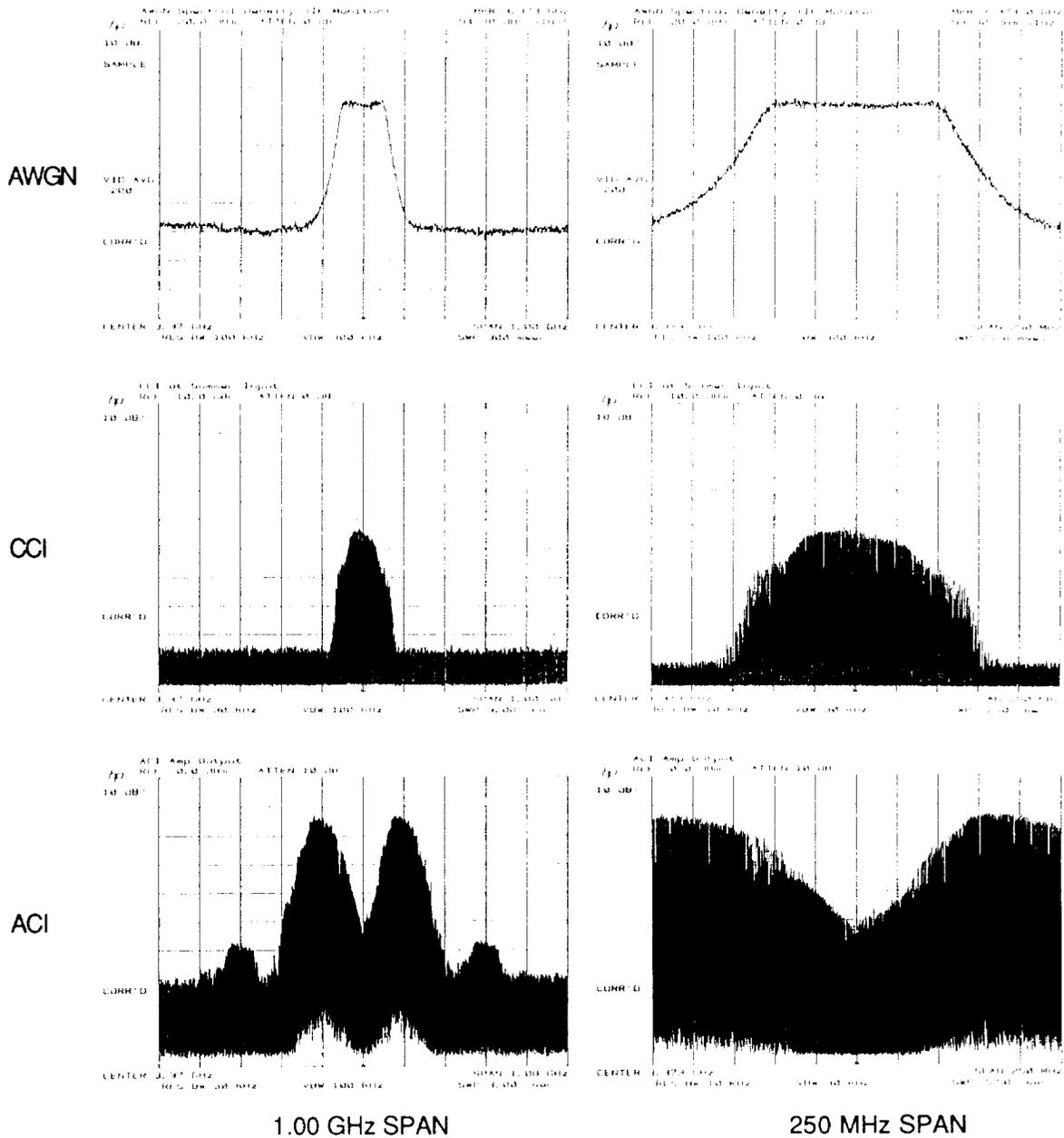
Spectra for the modulated signal, the effects of the nonlinearity (the HPA) on spectral regrowth, and the effect of the HPA output filter on the reduction of ACI are shown below. The simple case of BPSK was used to obtain these plots. The ± 414 MHz spurs at the modulator output are expected to have no impact on BER performance or E_s/N_0 measurement, but will be eliminated before BER testing of the entire system begins. Note that the main lobe of the modulator output is spectrally flat and 67 MHz wide, while all spectral components outside of the 100 MHz channel bandwidth are suppressed by greater than 35 dB.



PERFORMANCE RESULTS (continued)

Interference Spectra

The flatness of the AWGN noise source is shown below. The noise density was measured and a calibration factor of +2.24 dB was computed for E_S/N_0 measurements. The CCI appears spectrally identical to the desired channel and 20 dB lower in power. The ACI displays some third order intermodulation, but it is entirely out of the desired channel and should not affect BER performance. The spectra of the two adjacent channels are spread which will cause more interference than actual adjacent channels. The ACI noise floor has also been amplified significantly by a high gain amplifier, but the it is still low enough that it won't effect the measurement of BER performance.



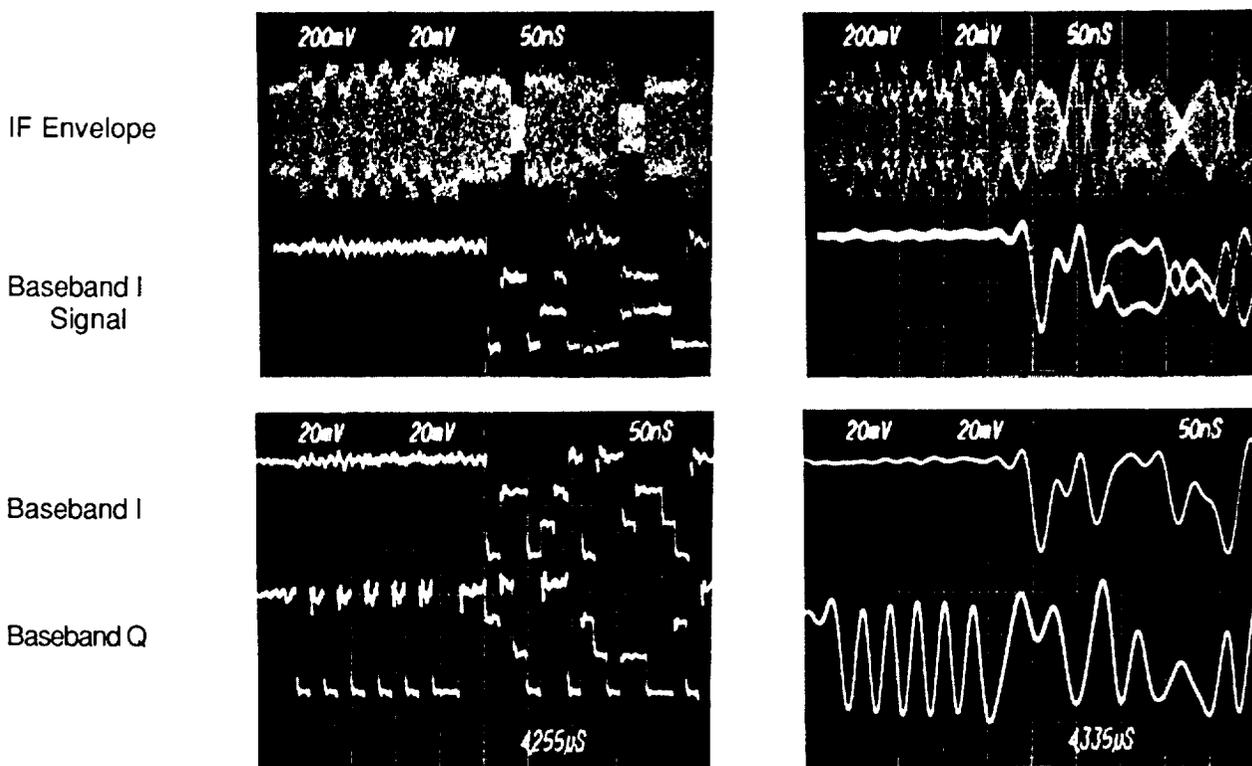
PERFORMANCE RESULTS (continued)

Envelope Deviation

The modulator performance is seen from the IF envelope at the modulator output and the baseband quadrature signals. Predistortion is turned off, so the wideband modulation displays four equally spaced levels for each quadrature signal, and three distinct IF envelope amplitudes. The effect of square root Nyquist filtering is also shown. The first half of each photograph is a short preamble followed by a 4 symbol unique word. The variation in the envelope during this time, which should be constant and at peak amplitude, reflects a misalignment in the RF section of the modulator. The second half of each picture is the beginning of a pseudo-random bit sequence (PRBS). The baseband I signal has multiple traces because we had problems with one of the PRBS generators at the time of the test. All errors will be corrected before final testing of the system.

Wideband 4x4 QAM Modulation

SRN Filtered 4x4 QAM Modulation



Power Consumption

The demodulator consumes about 86 Watts of power; primarily using ± 15 Volts for operating RF amplifiers and high speed opamps, and ± 5 Volts for logic operations. The decoder consumes three times as much power due to the complexity of the digital processing.

Voltage	DEMODULATOR		DECODER	
	Current	Power	Current	Power
+15 V	1.64 A	24.60 W		
-15 V	1.40 A	21.00 W		
+5 V	1.04 A	5.20 W	38.70 A	193.50 W
-2 V			14.17 A	28.34 W
-5 V	6.89 A	34.45 W	10.61 A	53.05 W
	Total Power = 85.25 W		Total Power = 274.89 W	

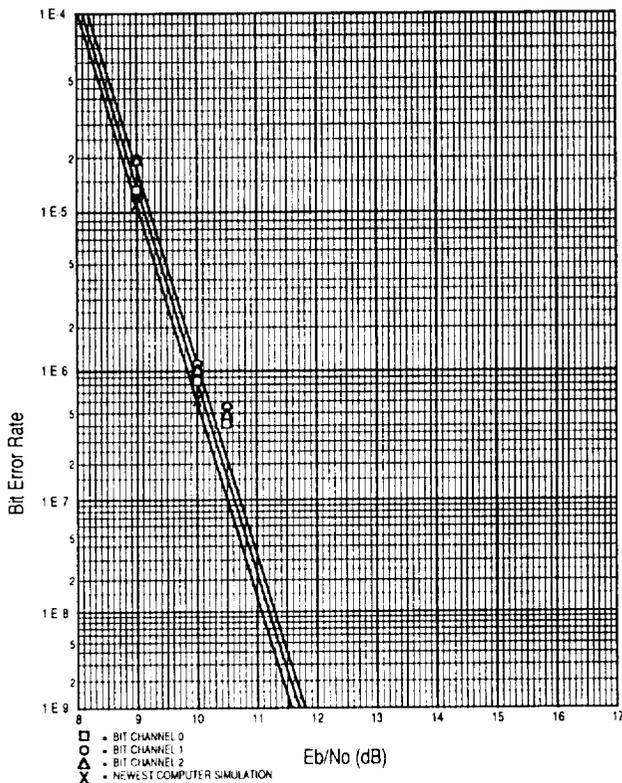
PERFORMANCE RESULTS (continued)

Subsystem BER Performance

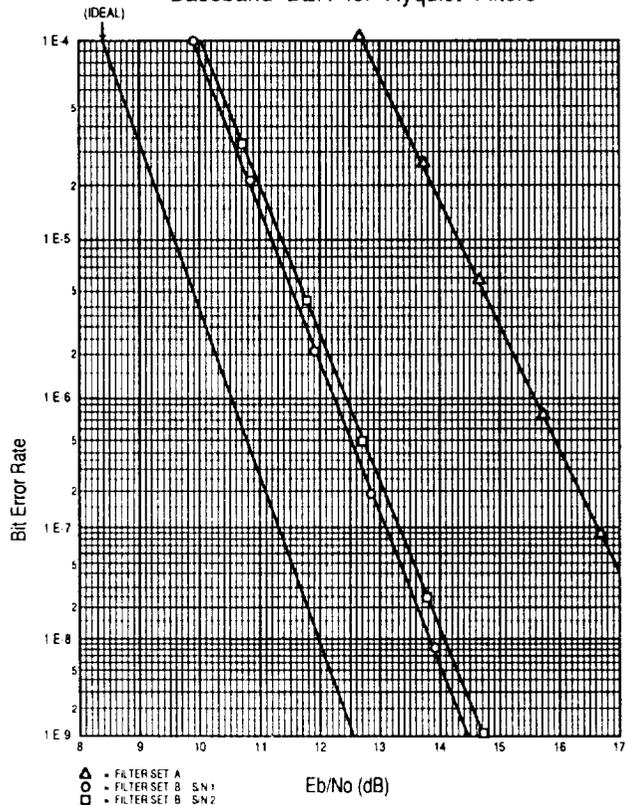
The encoder/decoder portion of the system has been completed and separately tested for BER performance. Worst case degradation from ideal performance was 0.2 dB at BER = 5×10^{-7} . The new ideal performance curve, as predicted by computer simulation, is different from the reference curve in the system performance section. A more accurate model was used and is slightly less optimistic. The results for each of the three information bits per symbol are shown. The decoder actually outputs nine different bit channels, but the remaining six exist because symbols are processed in groups of three after the three-step traceback circuit. The corresponding bit channels from the other two symbols performed identically to the first three. The measured performance degrades at high E_b/N_0 because of limitations of the digital noise simulator used to test the encoder/decoder.

The Nyquist filters were also tested separately from the system. Filter set A was originally built, but performed poorly with 5.1 dB of degradation at BER = 5×10^{-7} . The degradation for the entire system is specified at 2 dB. The filter requirements were refined and two new filter sets were developed, one for each quadrature baseband signal. Both new filters performed much better than the A version, but still with significant degradation at 1.9 dB worst case. The actual filter parameters and their effect on BER performance is discussed on the following page.

Encoder/Decoder BER Performance



Baseband BER for Nyquist Filters



PERFORMANCE RESULTS (continued)

Nyquist Filter Parameters

The pulse response, eye pattern, and group delay of the Nyquist filters give us insight into the BER performance. The pulse response of both filter versions is similar in the square root Nyquist (SRN) case, but there is significant degradation for the full Nyquist response of version A. The eye patterns show the actual amount of intersymbol interference (ISI) at the ideal sampling point more clearly. The eye closure for both filter sets is similar in the SRN case again, but actually gets worse for the full Nyquist response of version A. This suggests that the second half of the version A filter is the main source of its degradation. One of the prime requirements of Nyquist filters is minimal group delay variation in the passband. The version A filter set has about 18 ns of group delay ripple which is significant relative to a 15 ns symbol period. The version B set has 6 ns of ripple, although it's mostly at the bandedge.

Version A Filter Set

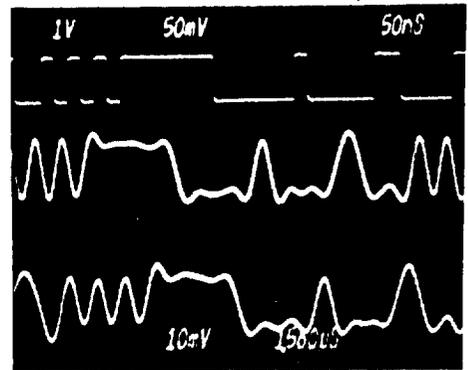
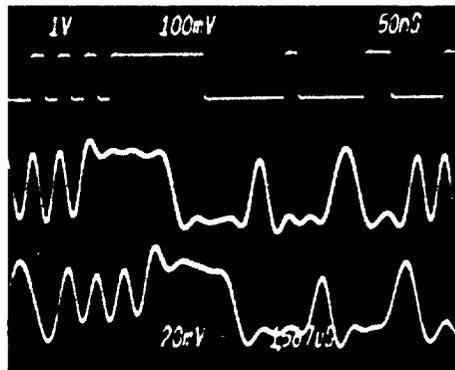
Version B Filter Set (S/N 2)

Pulse Response

NRZ Source

SRN

Full Nyquist

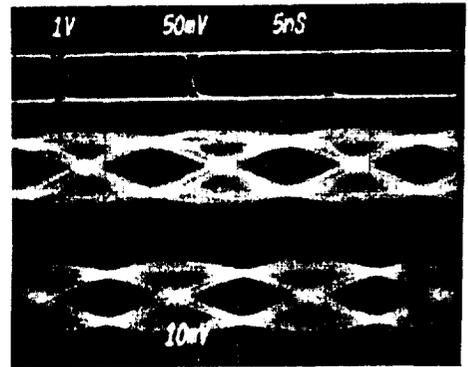
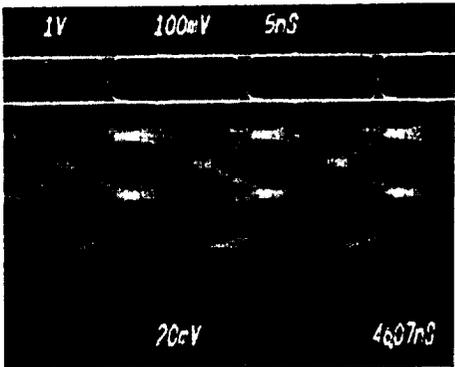


Eye Patterns

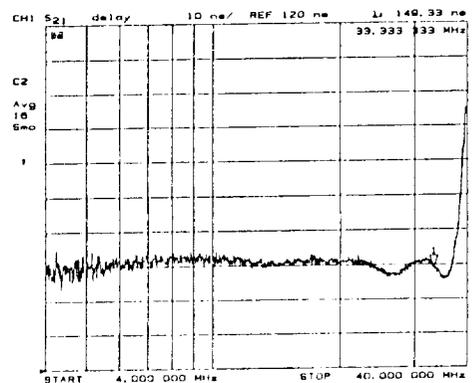
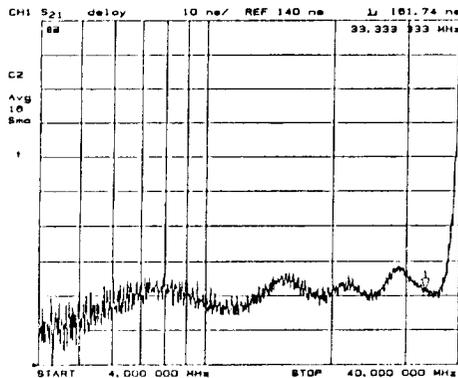
NRZ Source

SRN

Full Nyquist



Full Nyquist Group Delay

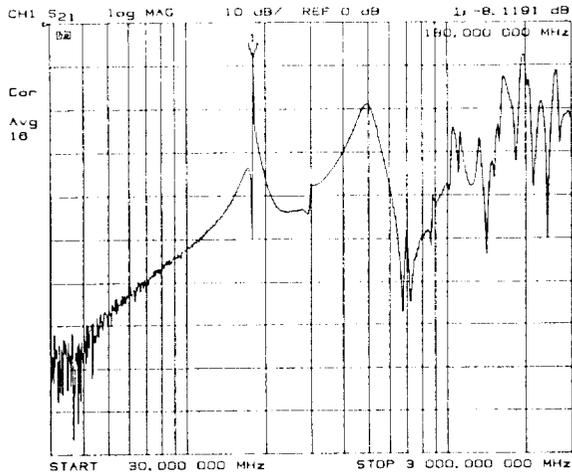


PERFORMANCE RESULTS (continued)

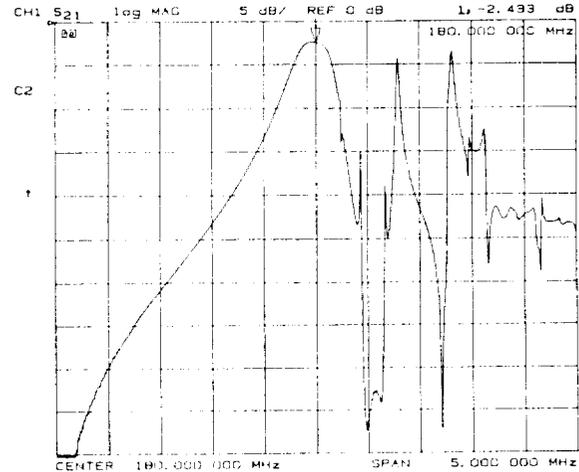
Ringing Filters

The simulations for 4x4 QAM showed the BER to be highly sensitive to the RMS phase error of the recovered carrier which makes the ringing filters in the carrier recovery a critical component. The narrowband spurious response is of greatest concern because some of the spurious products from the remodulation process will significantly add to the phase error of the recovered carrier. The actual BER performance degradation that can be expected is unknown at this time.

Typical 180 MHz Crystal Filter Passband (S/N 3A)



Wideband

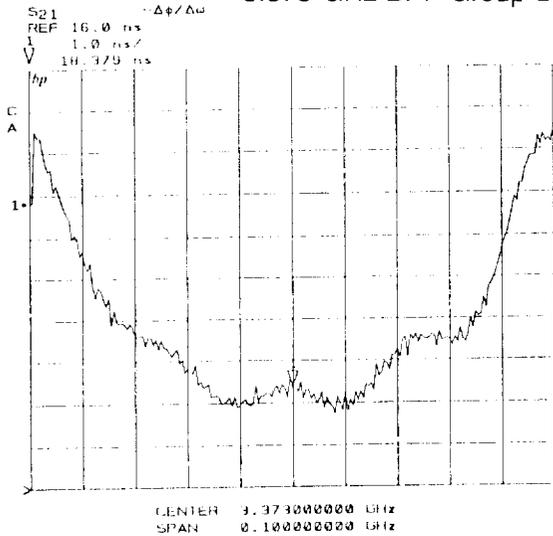


Narrowband

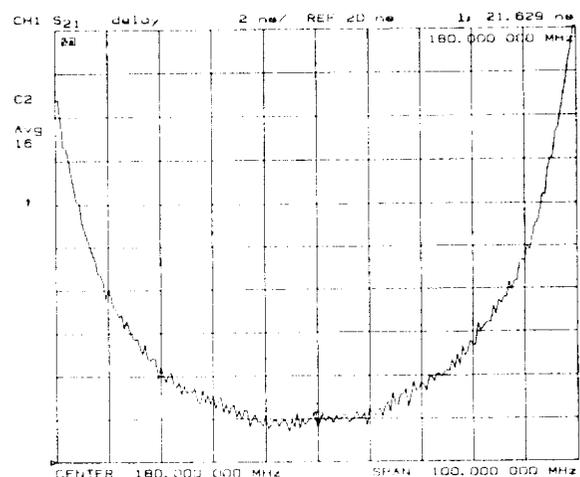
Bandpass Channel Filters

Another source of BER degradation is group delay variations in the bandpass filters used on the QAM signal in the demodulator. The filter centered at 3.373 GHz is at the input to minimize ACI effects, and the filter at 180 MHz is directly after the downconversion. The filter at 180 MHz has less fine grain ripple in the center of the band but degrades more rapidly at the edges. Both filters introduce less group delay distortion than the Nyquist filters so the impact on BER performance will be relatively small.

3.373 GHz BPF Group Delay



180 MHz BPF Group Delay



RECOMMENDATIONS

Degradation Implementation

The ACI spectra, as documented in the previous section, clearly show third order intermodulation between the two adjacent channels. The intermodulation is low enough in level that measurement of the adjacent channel power is still accurate, but the internal spectral spreading of each seems to be significant and the use of amplifiers with higher third order intercept points is recommended.

Another difficulty is the requirement of an HPA Output Filter to compensate for regrowth of the sidelobes. The system design showed good results but was unrealistic because ideal equalization of the filter's group delay was assumed. Reasonable filters of this bandwidth can be built at 3 GHz, but become much more difficult in real world systems which would likely run at 20/30 GHz.

Decoder Implementation

Although the actual power consumption of the decoder is about 60% of the originally predicted worst case, it still is 3/4 of the total power consumption. It could be reduced in the engineering model phase of development by using gate arrays or custom ICs for some portions of the decoder. The add/compare/select function of the state metric calculator has already been hybridized to reduce interconnect delays. Future refinement of the processing algorithms for hardware simplification could also be investigated.

Coarse AGC Design

An improvement to the design of the coarse AGC may be obtained by implementing it entirely after the downconversion instead of at the higher IF. One advantage is that it would use all low frequency components which are more readily available. The phase margin of the closed loop would also be increased because the logamp in the feedback loop would be tied directly to the AGC output instead of after a path delay. The logamp is used to linearize the control loop response of the pin diode attenuator and is much easier to obtain at the lower frequency. Finally, the input bandpass filter could be eliminated, although high level adjacent channels may cause third order intermodulation in the input amplifier and downconverting mixer.

The coarse AGC is presently implemented as an analog, closed-loop control system which impacts the system acquisition time with a settling speed of approximately 360ns (=72 information bit times). The carrier acquisition time is twice the specified preamble length of 100 bit times and the carrier recovery circuitry is somewhat level sensitive, so in the worst case the total acquisition time is $192 + 72 = 264$ information bit times. This could only be marginally improved with state of the art components in the AGC, so alternate topologies are recommended for future design efforts. The carrier recovery circuitry could be designed for insensitivity to the 20dB dynamic range of the QAM signal. The AGC could also be significantly sped up by implementing it as an open loop compensator which could use a fast detector and digitizer to drive a digitally controlled attenuator.

Nyquist Filters

The Nyquist filters significantly degrade BER performance due to ISI. The performance section shows the amount of ISI from the filters in the eye pattern figures, and that a major source of the problem is group delay ripple. The BER degradation of the entire system will be limited by the filters, so the BER degradation specification of 2 dB cannot be met with the present filters. Bandwidth efficiency restrictions on this system require the use of Nyquist filters, so specification and implementation of them will be an important part of any future work.

RECOMMENDATIONS (continued)

Ringing Filters

The spurious response of the present crystal filters can be expected to affect the phase error of the recovered carrier and clock. The frequency plan of the Demodulator could be redone to change the percent bandwidth of the carrier recovery filter, which might allow operation of the crystals without forcing a response which results in spurs. This cannot be done for the clock recovery where the frequency is determined by the symbol rate, so alternate filter implementations should be investigated for both cases.

Signal Path Filters

Several narrowband filters exist in the QAM signal path which are expected to affect the BER performance of the system by introducing intersymbol interference (ISI) distortion through group delay ripple. The BER simulations in the initial system study include the effects of an HPA output filter, but the implemented Demodulator has two additional filters. One is at the input to minimize the effect of the adjacent channels on the coarse AGC and its high-gain RF amplifier. The second is after the downconversion to eliminate the mixing spurs. With the use of "better" Nyquist filters, it may be necessary to more tightly specify these filters. The possibility of removing the second filter from the signal path and only inserting it directly before level detecting circuits should also be investigated.

Component Selection

Wideband track/hold (T/H) amplifiers are presently used three times in the Demodulator. The purpose is to "lock in" various control voltages at UW detection to avoid fluctuations due to envelope variations of the QAM signal during the data portion of the burst. The problem with using T/H Amps is their inherent pedestal offset and droop rate. The sensitivity of the system's BER performance to these parameters has not yet been determined, but is expected to be a minor problem. Future designs may need to use improved T/H amps or use feedforward digital control.

Wideband opamps are used at thirteen spots in the Demodulator. Seven of them dissipate a lot of power (900mW) but were used because of their performance characteristics. New opamps are now available which would improve performance in five locations, require fewer external components, and dissipate less than 150 mW each.

The Gating Processor and the UW Detector in the Demodulator are presently implemented using 100K ECL and dissipate about 6.6 Watts. The power consumption of the system as well as size could be reduced by using ECL (or possibly high speed TTL or CMOS) programmable logic for these two functions.

MIMIC/Commercial Components

Several companies, including TRW, are presently developing millimeter-wave microwave integrated circuit (MIMIC) technology which will provide attractive opportunities to reduce the size of the RF portions of the modem/codec system. As one example, TRW is developing HBT technology which has definite size and unit cost advantages because the transistor structure supports high yields and high integration density. Switches, amplifiers, mixers, and logamps are under current development, and more advanced functions such as digital attenuators, I/Q detectors, and linear mixers could be expected in the future.

RECOMMENDATIONS (continued)

Summary

Object	Change	Improvement
Degradation Implementation Decoder Implementation Coarse AGC Design	Amplifier IP3, HPA filter Use more gate array technology Settling time Topology	Measurement accuracy Power dissipation Acquisition speed (preamble Length) Material cost, complexity
Nyquist Filters Ringing Filters Signal Path Filters Component Selection	Tighter specifications Spur-free Specs and system topology New components Use programmable logic Use MIMIC where possible	BER performance Acquisition speed, BER performance BER performance Performance, space and power Size and power Size and cost

CONCLUSION

In order to achieve 2 bit/s/Hz bandwidth efficiency along with implementation simplicity and power efficiency for the Uplink, a modulation/coding format of 4x4 QAM with rate 3/4 FEC coding was chosen. The special test equipment is very near completion with only a few performance discrepancies that need to be resolved. The demodulator portion is at the beginning of the integration phase so complete performance results are not yet available. The 8-state Viterbi decoder portion of the POC system is completed and performs very well with a worst case BER degradation of 0.2 dB from theory. It is known, however, that several major sources of degradation in BER performance and acquisition time exist and that power consumption for the POC system is high. The actual performance of the system and the individual impact of each portion of the system will be available at the conclusion of the program.

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 Keith K. Yamashiro - Quenching Analysis

REFERENCES

- Feher, K. Digital Communications: Satellite/Earth Station Engineering. Prentice-Hall, Englewood Cliffs, New Jersey, 1983. p. 155.
- Gardner, Floyd M., Carrier and Clock Synchronization for TDMA Digital Communications. European Space Agency, Paris, France. December 1976. pp. 19-28.
- Nyquist, H. "Certain Topics in Telegraph Transmission Theory," Trans. AIEE, Volume 47, 1928.
- Rhodes, S. A. "Effects of Hardlimiting of Bandlimited Transmissions with Conventional and Offset QPSK Modulation," IEEE Telecommunications Conference Record. Houston, Texas, 1972. pp. 20-F-1 to 20-F-7.



AN 8-PSK TDMA UPLINK MODULATION AND CODING SYSTEM

S.A. Ames
Ford Aerospace Corporation
Space Systems Division
Palo Alto, California 94303

ABBREVIATIONS USED IN BRIEFING

• ACI	adjacent channel interference
• ADC	analog to digital converter
• AMTD	Advanced Modulation Technology Development
• ASIC	application specific integrated circuit
• AWGN	additive white Gaussian noise
• BER	bit error rate
• CCI	co-channel interference
• codec	coder/decoder
• DAC also D/A	digital to analog converter
• DBT	detected baud transitions
• ECL	emitter coupled logic
• LUT	lookup table
• MCD	multi-channel demultiplexer and demodulator
• MMIC	monolithic microwave integrated circuit
• modem	modulator/demodulator
• PCB	printed circuit board
• POC	proof-of-concept
• SAW	surface acoustic wave
• SBW	sub-burst window
• TDMA	time division multiple access
• UW	unique word

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OVERVIEW

- OBJECTIVES
- PHASES
- REQUIREMENTS
- PROOF-OF-CONCEPT MODEL BLOCK DIAGRAM
- PROOF-OF-CONCEPT MODEL PHYSICAL CONFIG.
- PERFORMANCE OF POC MODEL
- CONCLUSIONS OF PROGRAM
- RECOMMENDATIONS FOR FUTURE

OBJECTIVES AND PHASES

OBJECTIVES:

- Develop a proof-of-concept uplink modulation system which will significantly increase the bandwidth efficiency of a TDMA uplink system
- Maintain present performance levels (i.e., QPSK power and bandwidth efficiencies)
- POC model should exhibit potential for low weight and power consumption

PHASES:

- Refine preliminary design
- Develop preliminary design
- Build and test breadboard
- Plan, specify, and fab POC model
- Test POC model and establish POC
- Product assurance

REQUIREMENTS

SALIENT REQUIREMENTS FROM RFP:

- Bandwidth Efficiency > 2 bits/ sec/ Hz
- Implementation loss < 2 dB
- 1 dB degradation in 20 db ACI or CCI
- TDMA burst mode with preamble < 100 bit periods
- Throughput > 200 Mbps

DERIVED REQUIREMENTS:

- 8PSK modulation
- Nyquist filter with rolloff factor of 0.2
- CCI spec requires forward error correction coding
- Mostly digital mechanization for eventual ASIC design

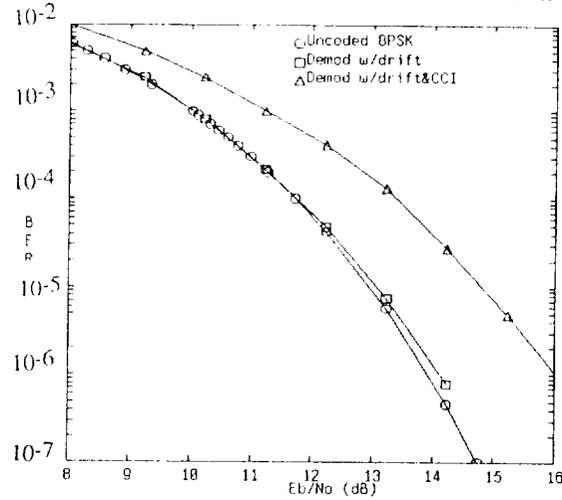
The combination of 8PSK modulation and >2 bits/sec/Hz drove the design of the Nyquist filter to one specified to have a rolloff factor of 0.2. This filter when built and tested was found to produce too much intersymbol interference and was abandoned for a design with rolloff factor of 0.4.

Preamble is limited to 100 bit periods of the uncoded bit period of 5 ns for a maximum preamble length of 500 ns or 40 8PSK symbol times at 12.5 ns per symbol.

For 8PSK modulation, the required maximum degradation of 1 dB in -20 dB CCI drove the requirement for forward error correction coding. In this contract, the funding was not sufficient to develop the proposed codec so the codec was limited to a paper design during the preliminary design phase.

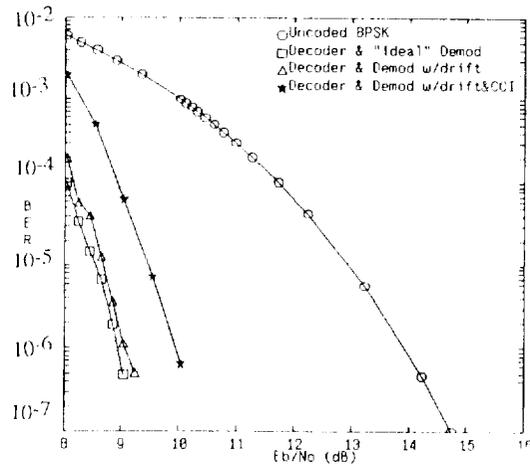
The mechanization of the demodulator is digital starting from the output of the ADCs which quantize the outputs of the quadrature phase detectors. This approach is amenable to an ASIC replacement in the next phase of development.

SIMULATIONS OF DEMOD PERFORMANCE WITH DRIFT AND CCI



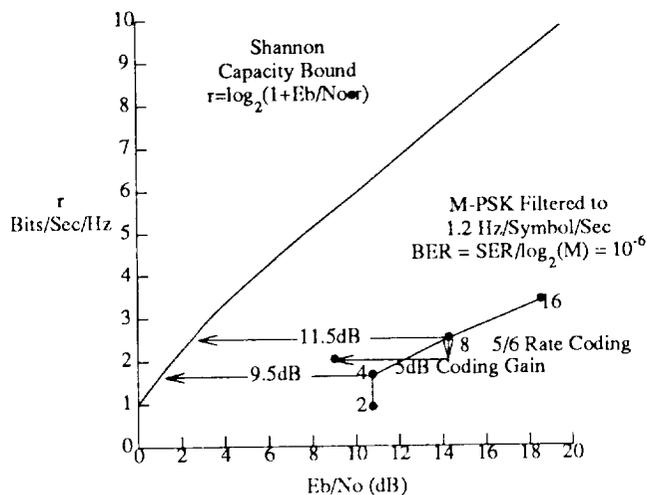
At BER equal to 5×10^{-7} , degradation from theoretical for -20 dB CCI is seen to be about 2 dB. This drove the requirement for forward error correction coding.

SIMULATIONS OF DEMOD AND DECODER PERFORMANCE WITH DRIFT AND CCI



The simulated codec (to be shown in some detail below) produces 5 dB improvement in AWGN and, in the presence of CCI, the degradation is only 1 dB.

BANDWIDTH AND POWER EFFICIENCIES OF MODULATION SYSTEMS



Note that with coding, 8PSK system is both more power and bandwidth efficient than uncoded QPSK which satisfies the requirement for both bandwidth efficiency and to "maintain present performance levels".

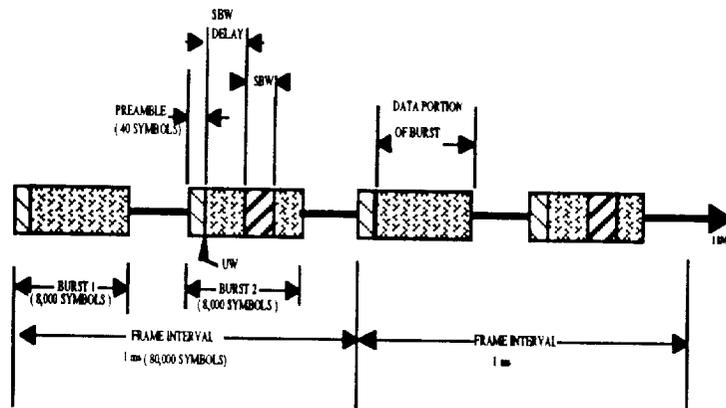
$r = \text{capacity/occupied bandwidth}$

16 QAM and 16PSK were both considered but were rejected as requiring a more complex modem.

SPECIFICATIONS OF POC MODEL

PARAMETER	VALUE	TEST SPEC NO OR METHOD OF DETERMINING COMPLIANCE
Bandwidth Efficiency	> 2 bits/sec/Hz	1
Bit Rate	240 Mbps	by design
Channel Spacing	96 MHz	by design
Transmission Mode	TDMA	by design
Frame Length	1 ms	by design
Preamble (CW portion) (UW portion)	32 symbols 8 symbols	by design
Receive Frequency	3.47056 GHz ± 1 MHz	by design
Input level at receiver filter	-30 dBm to 0.5 dB	by design
BER at Es/No = 21 dB	$< 5 \times 10^{-7}$	2
Degradation Due to +20 dB ACI	-1 dB	3
Degradation Due to -20 dB CCI	-1 dB	4
Probability of bit error due to missing unique word	$< 1 \times 10^{-7}$ at E _s /N ₀ = 21 dB	by computation (3)
Probability of Carrier Cycle Slip	< 100 at E _s /N ₀ = 10 dB	5
Bit Timing Jitter	< 10 ps RMS	6
Probability of Clock Cycle Slip	< 100 at E _s /N ₀ = 10 dB	7
Minimum Guard Time Between Bursts	25 ns	by design of SLE

PREAMBLE AND BURST STRUCTURE

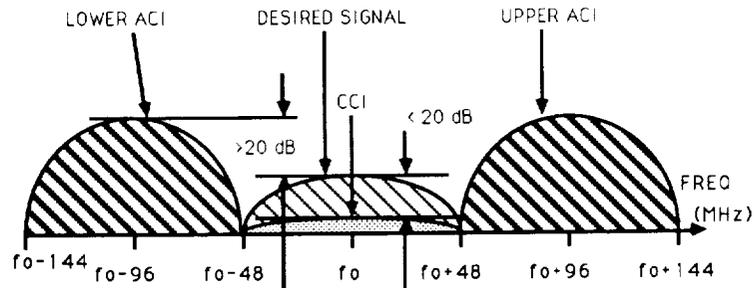


The sub-burst window (SBW) is used to measure the BER in only a selected portion of the burst. Its position within the burst and length are adjustable.

8,000 symbol bursts shown only for example; test equipment can generate any length bursts up to 80,000 symbols

The unique word is eight BPSK symbols for high noise immunity.

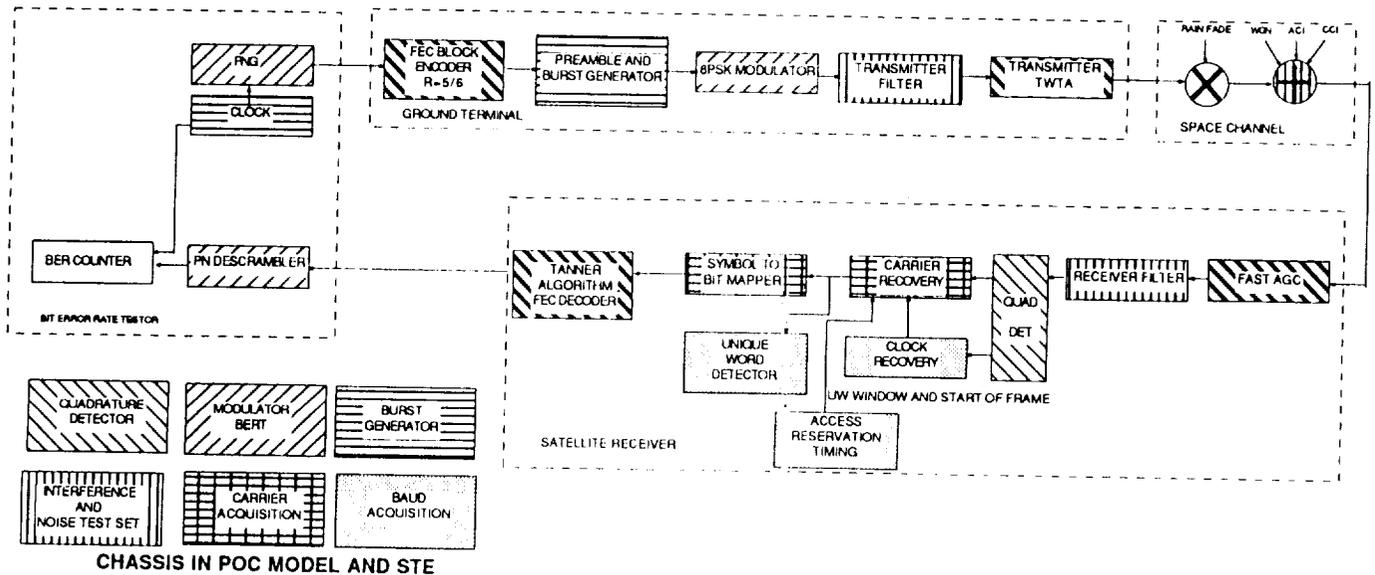
SIGNAL SPECTRA SHOWING CO-CHANNEL AND ADJACENT-CHANNEL INTERFERENCES



Center frequency, f_0 , specified as 3.373056 GHz \pm 1.5 KHz

ACI spacing shown to achieve the design goal of 2 bits/sec/Hz with a rolloff factor of 0.2

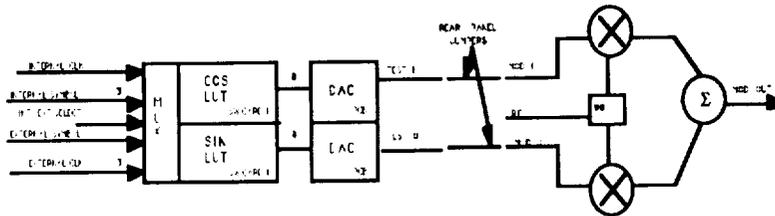
A block diagram of the ground and satellite system is shown on the following page. The seven different shadings are shown to signify the physical chassis in which the functional unit is located within the POC model and STE. The heavy diagonal hatching (plus the rain fade) illustrates those elements which would be in a full system but were not implemented in the POC model stage because of time and/or budget limitations.



THESE BLOCKS
NOT IMPLEMENTED
OR TESTED

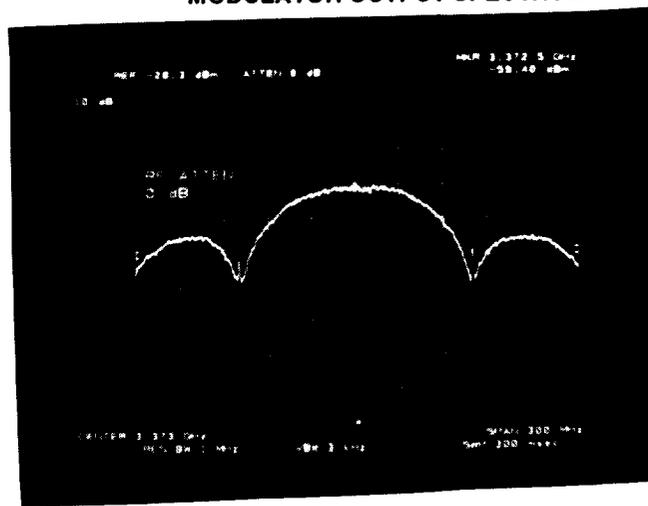
BLOCK DIAGRAM OF GROUND AND SATELLITE TDMA TEST SYSTEM

QUADRATURE MODULATOR

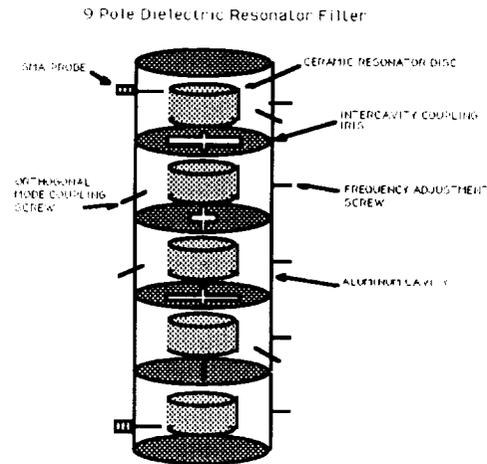


Three bits of Gray coded data are applied as addresses to the sine and cosine LUTs. The LUT contents, which are the projections of the modulation symbol in the I and Q axes, are applied to a pair of DACs and then to the quadrature balanced mixer to produce the spectrum shown on the following page. A highly accurate modulator can be produced since compensation for non-ideal behavior of the balanced mixers can be included in the LUT.

MODULATOR OUTPUT SPECTRUM



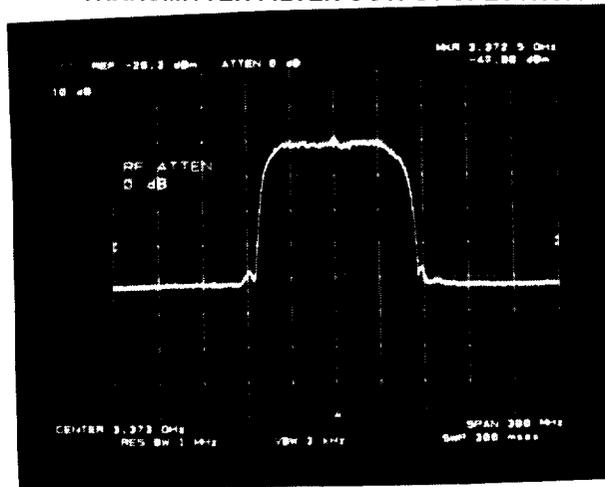
MECHANICAL CONFIGURATION OF NYQUIST FILTERS



The original Nyquist filter design was to produce a rolloff factor of 0.2 (excess bandwidth of 20%) but when tested, too much intersymbol interference resulted. The rolloff factor was increased to 0.4 where a satisfactory eye-pattern was obtained.

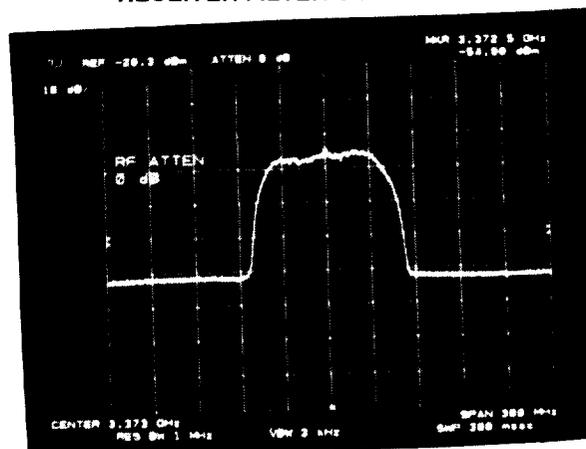
The nine pole filter shown above was comprised of four dual mode and one single mode dielectric resonators to produce the square-root Nyquist response. Identical filters were used in both the modulator and demodulator. In addition, an inverse sinc function equalizer in the transmitter and amplitude and group delay equalizers in both transmitter and receiver utilizing similar resonators were used.

TRANSMITTER FILTER OUTPUT SPECTRUM



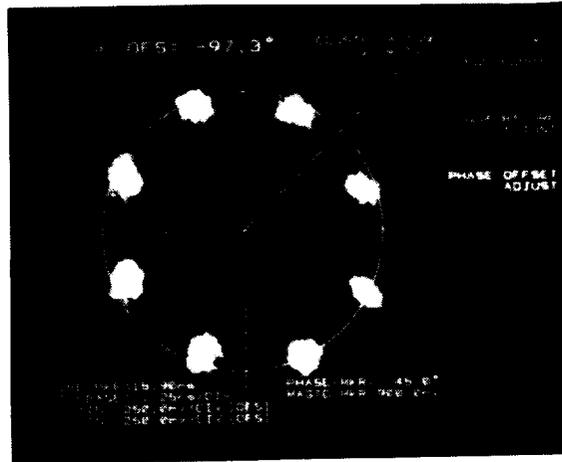
The transmitter spectrum is shown above where the previously displayed modulator spectrum has been equalized by the inverse sinc and then passed through the transmitter square-root Nyquist filter with a 0.4 rolloff factor.

RECEIVER FILTER OUTPUT SPECTRUM

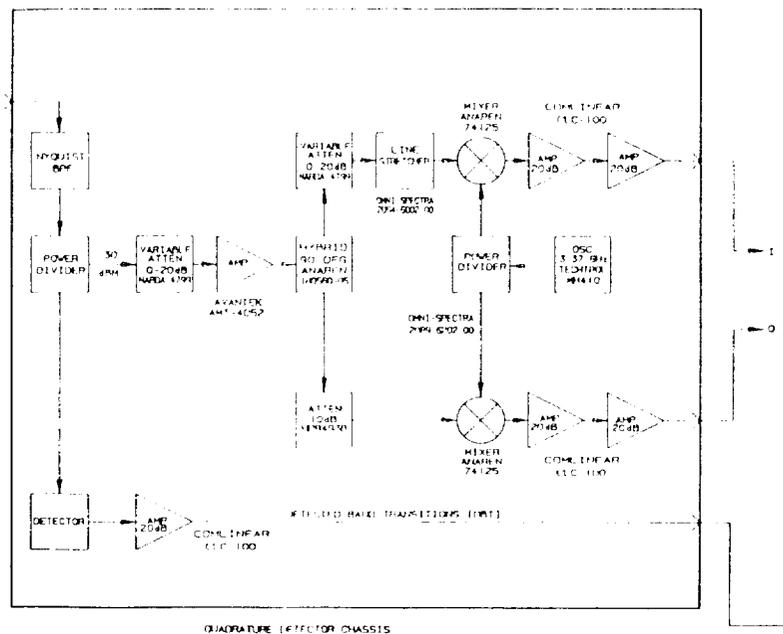


The output of the receiver filter shown above displays the full Nyquist response with 0.4 rolloff factor.

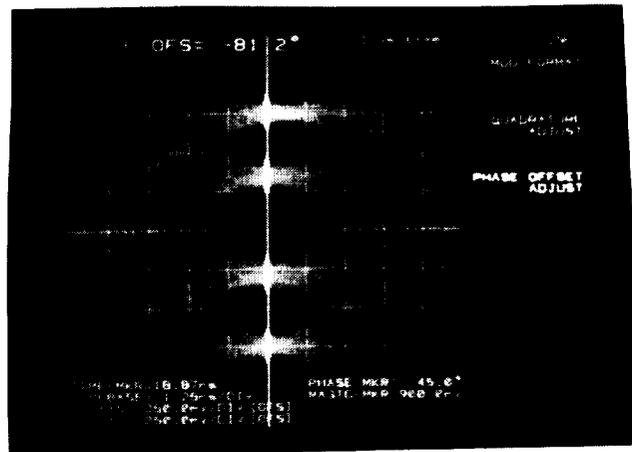
CONSTELLATION OUTPUT AT RECEIVER QUADRATURE DETECTOR



The 8PSK constellation at the output of the receiver quadrature detector as displayed on the HP 8980A vector analyzer. It is at this point that the I and Q signals are digitized and applied to the digital PLL. Note that the constellation at this point is normally still spinning at a rate equal to the difference frequency between the received carrier and the LO. However, for the purposes of producing this constellation display, it has been despun by using a coherent LO.



EYE PATTERN AT "I" SIDE OF QUADRATURE DETECTOR



The eye patterns using the rolloff factor of 0.4 are open at the point of sampling.

EYE PATTERN AT "Q" SIDE OF QUADRATURE DETECTOR



FEATURES OF THE DIGITAL DEMODULATOR

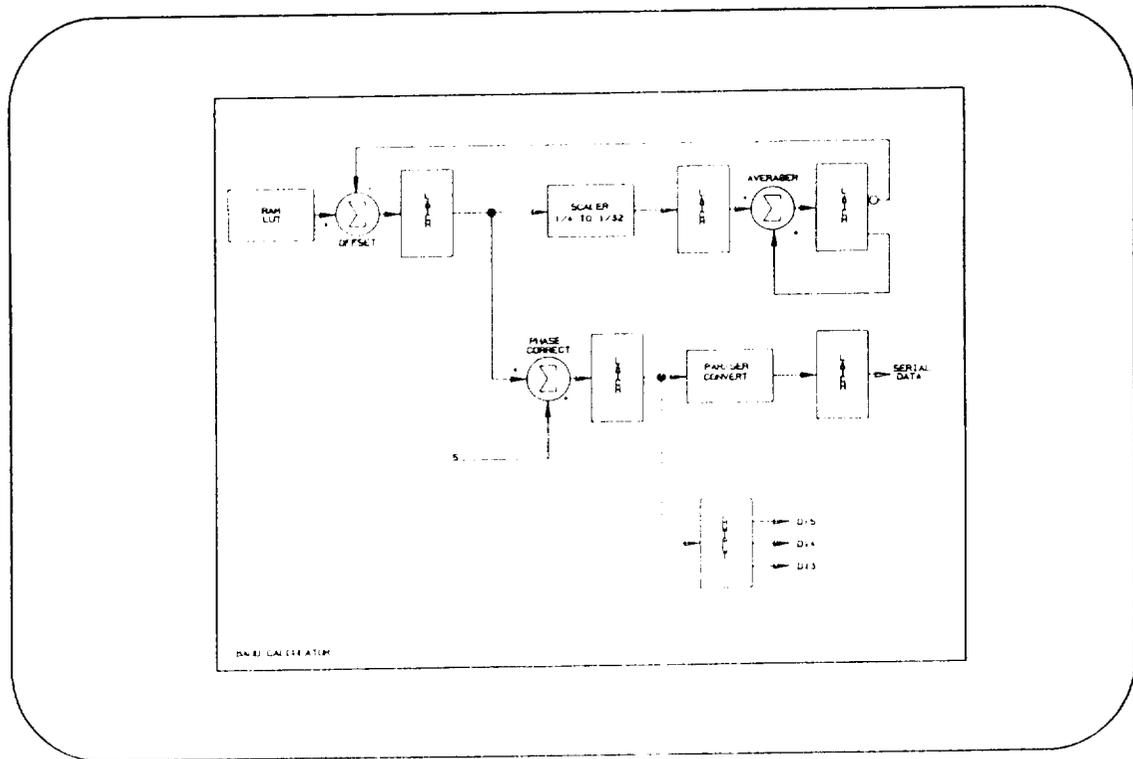
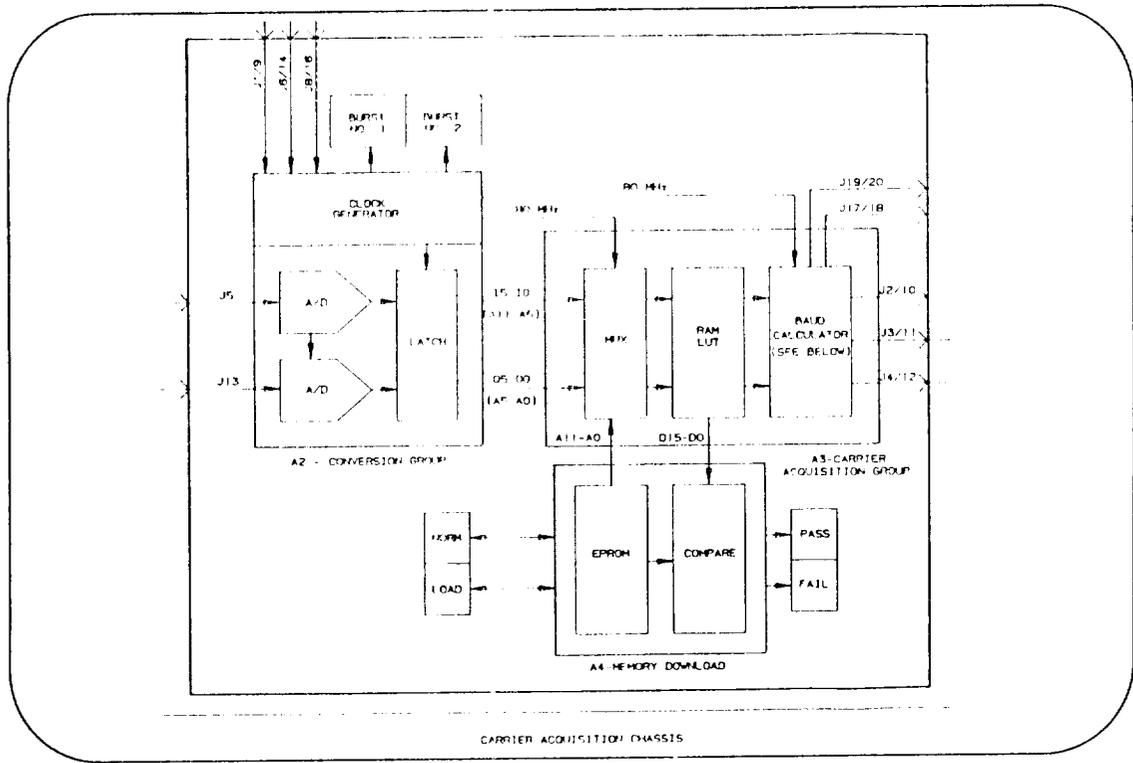
CARRIER ACQUISITION CHASSIS

Clock generator is locked to the recovered symbol clock and drives the sampling of the I and Q ADCs once per symbol.

A RAM LUT was used instead of a ROM since a ROM with the necessary access time (less than 5 ns) was not available when the design was started. The RAM is downloaded from the ROM when the system is started. Its contents are the arctangents of the addresses formed by the I and Q data words.

BAUD CALCULATOR

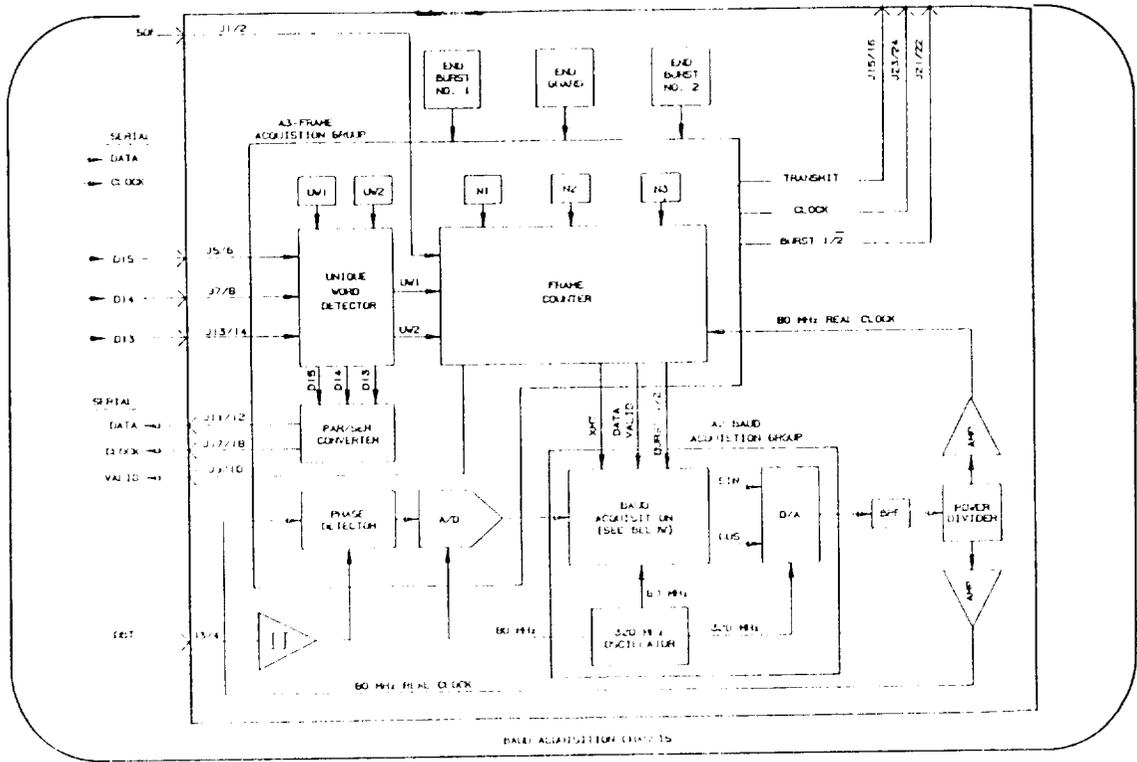
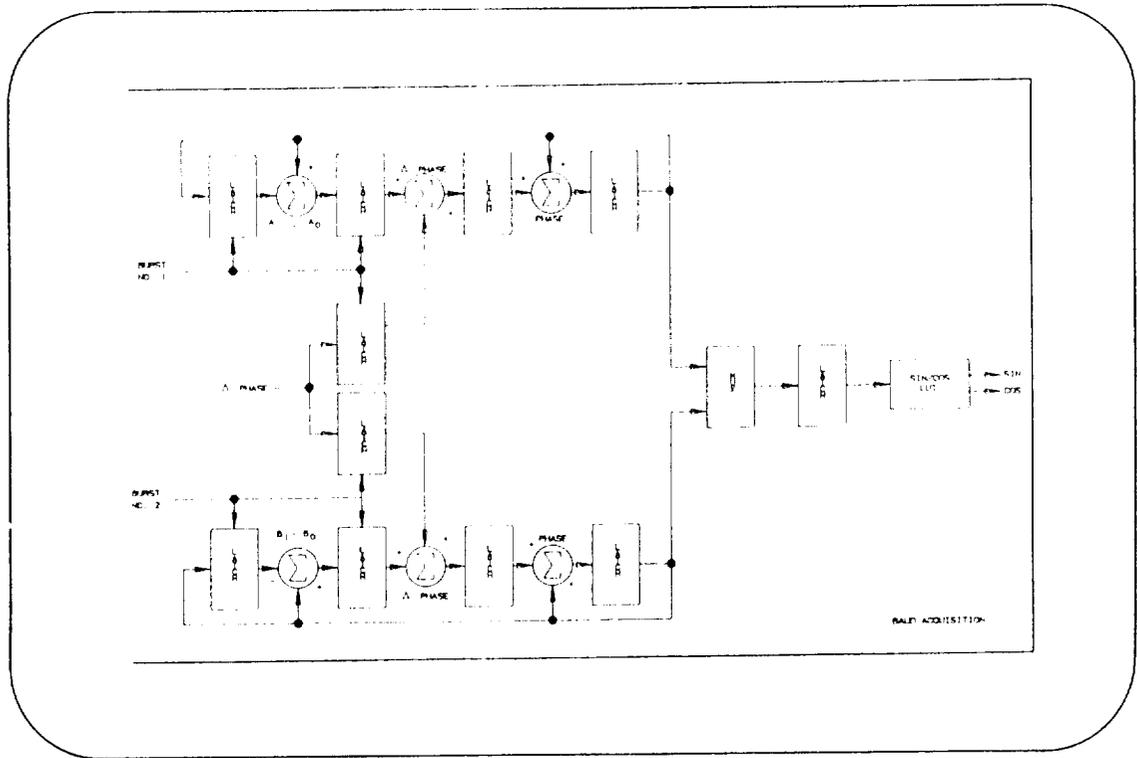
The first order carrier PLL despins the constellation. The PLL gain is $1/8$ during the carrier acquisition portion of the preamble and decreases to $1/32$ during modulation when it tracks the incoming carrier modulo 45 degrees. The value 0.5 is added to the phase error at the phase correction summer to rotate the phase error samples by 22.5 degrees. This numerically adjusts the decision boundaries so that the symbol decision can be made by simply truncating the phase error samples to its three most significant bits.



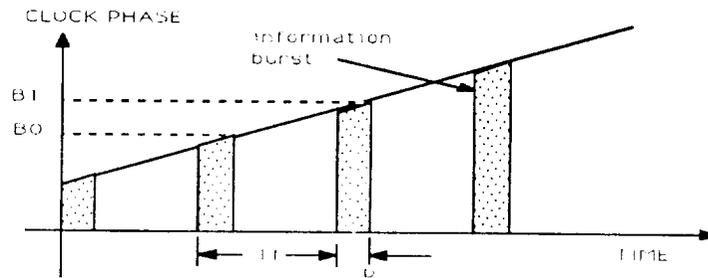
FEATURES OF THE DIGITAL DEMODULATOR (CONT.)

BAUD ACQUISITION CHASSIS

Detected baud transitions are applied to a threshold and phase compared with the output of a numerically controlled oscillator running at a nominal four samples per cycle. A detail of the baud acquisition is shown in the following diagram. It has two independent first order PLLs which track the two test bursts. The baud acquisition exploits the phase continuity of the symbol clock between bursts of the same access to predict the phase change between bursts from the same access. In principle, such a scheme can improve the burst efficiency by eliminating the need for clock transitions to appear in the preamble of each burst. In practice, this scheme needs a "training burst" for each access (probably on a super-frame basis) to correctly initialize the phase predictor. The training burst was not implemented during the POC model phase which probably explains the degraded performance as the bursts were shortened.

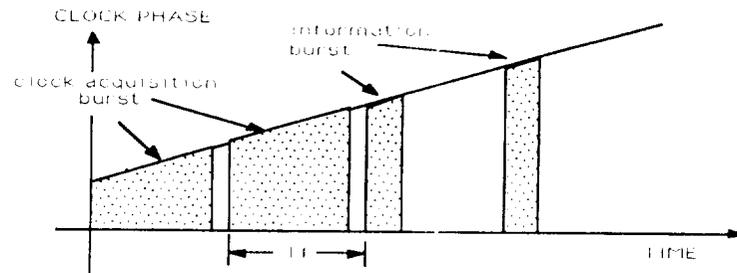


SYMBOL CLOCK ACQUISITION

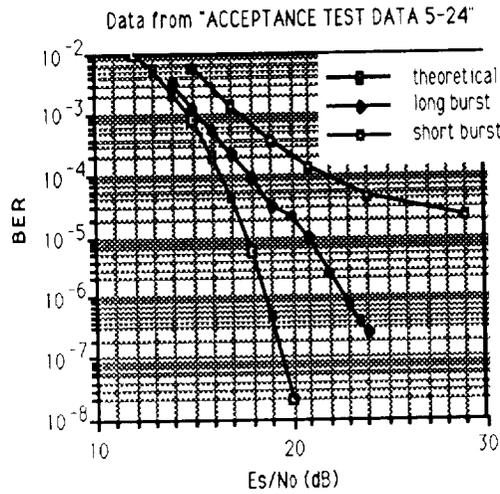


phase slope = $(B1 - B0) / T1$

phase correction = phase slope $\bullet (T1 - Tb) = (B1 - B0) \bullet (T1 - Tb) / T1$

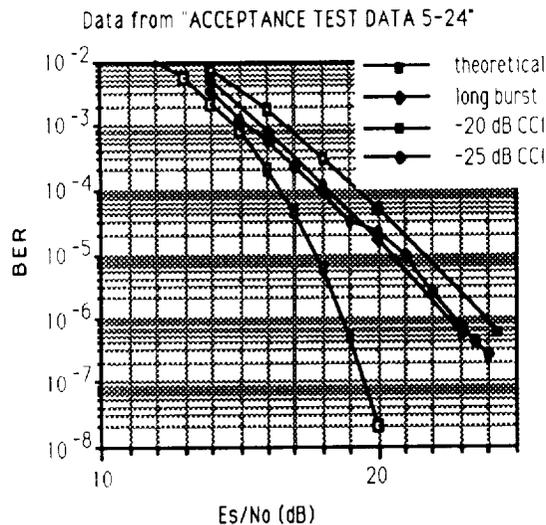


BIT ERROR RATE VERSUS E_s/N_0 IN AWGN FOR LONG AND SHORT BURSTS



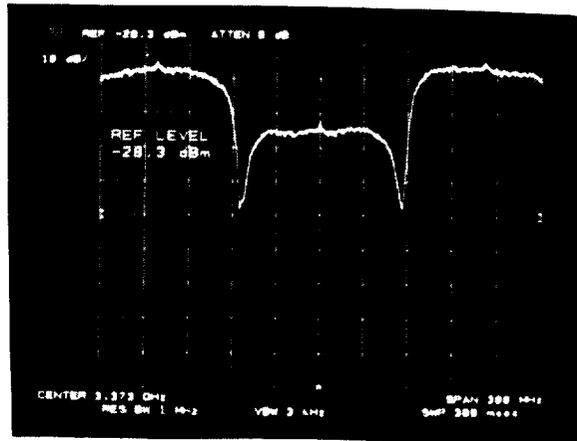
Displayed above is the BER versus the E_s/N_0 . The leftmost curve is the theoretical curve for Gray coded 8PSK. The next curve to the right is the measured curve of the POC model when using long bursts (about 90% of the frame). The rightmost curve is the BER for a burst length of about 46% of the frame. The degradation during shorter bursts is probably due to the poor performance of the phase predictor.

BER VERSUS E_s/N_0 IN CCI



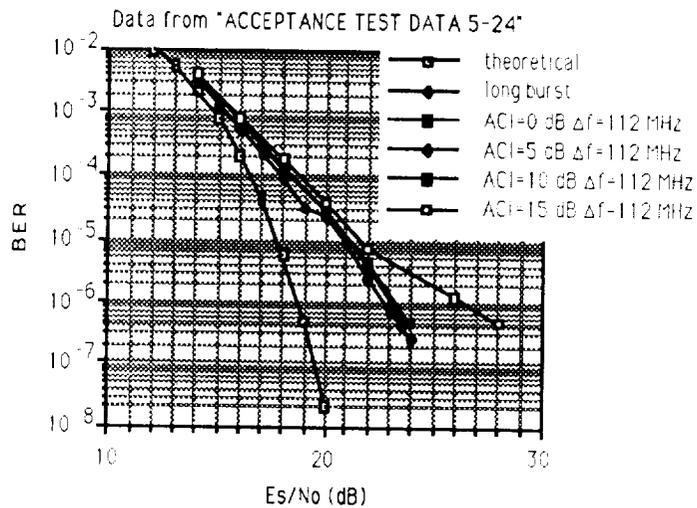
The relatively insensitive behavior of the BER in CCI is probably due to the implementation loss being high enough to mask the effect of CCI. Recall that the CCI degradation predicted from computer simulations at -20 dB CCI was 2 dB at BER equal to $5E-7$ while the measured degradation is only about 1 dB.

INPUT SPECTRUM TO RECEIVER WITH +20 dB ACI AT ± 112 MHz



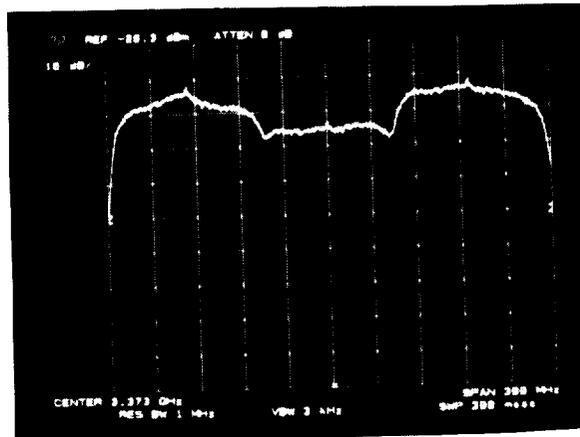
The original spacing between adjacent channels was to be 96 MHz based on the rolloff factor of 0.2. However, since satisfactory filters could not be built with this steepness in the transition band, the correct spacing for the filters with a rolloff factor of 0.4 is 112 MHz. The above spectral display shows two 20 dB ACI signals spaced by 112 MHz. The deep cusps between the spectra indicate little leakage of the ACI power into the desired signal.

BER VERSUS E_s/N_0 IN ACI FOR 112 MHz SPACING



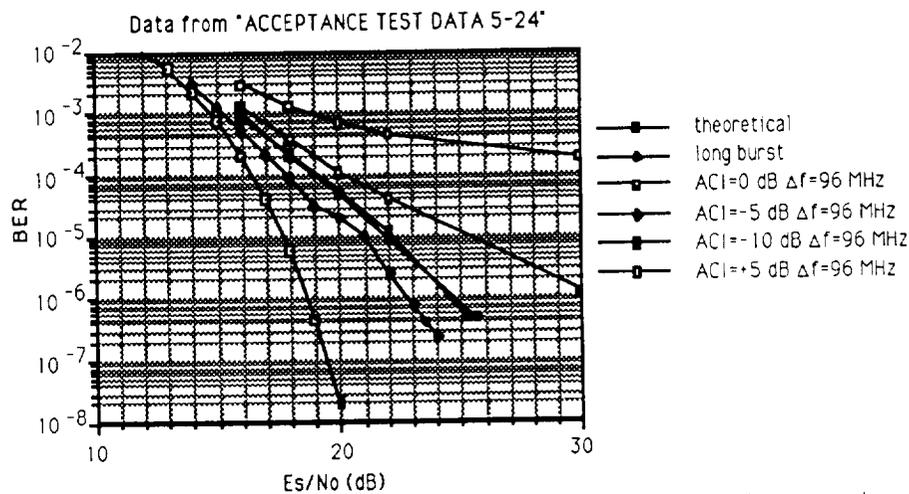
As predicted from the spectral display, until the ACI exceeds 15 dB, small degradation is experienced.

INPUT SPECTRUM TO RECEIVER WITH +10 dB ACI AT ± 96 MHz



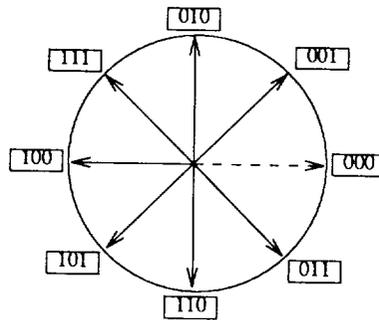
Shown here is the spectral display with the ACI at ± 96 MHz but still using the Nyquist filter with rolloff factor of 0.4. As expected, since the transition band skirts are much less steep, the ACI power leaks into the desired signal to such an extent that the cusps between the spectra are completely filled in even with the ACI at only 10 dB.

BER VERSUS E_s/N_0 FOR ACI SPACING OF 96 MHz



As expected, the degradation in ACI for the 96 MHz spacing is very large. The obvious conclusion is that to realize the target bandwidth efficiency with the coded 8PSK, it is necessary to use a Nyquist filter with a 0.2 rolloff factor. We believe that such a filter can indeed be realized using a properly equalized SAW device at a center frequency of about 280 MHz. Several iterations of the filter mask may be required to achieve the desired response and this contingency should be planned for.

SIGNIFICANT BIT 8PSK TO 3-TUPLE MAPPING

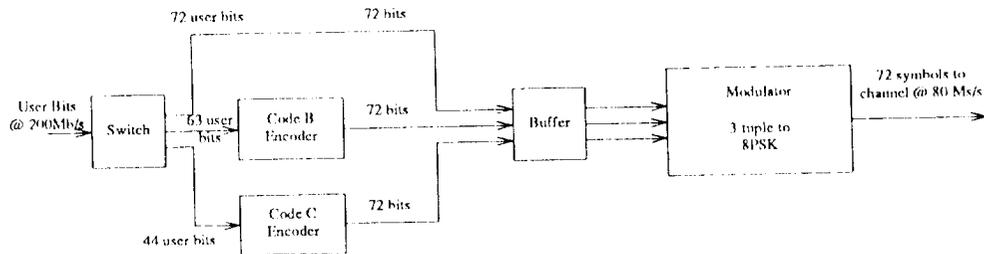


Due to budgetary limitations, the coding portion of the AMTD POC model was only produced as a "paper design". Its features will be outlined in the next few panels.

While the POC model used Gray coding of the symbol constellation for improved noise immunity, the constellation coding shown above would be used with our FEC system. The coding shown is called significant bit 8PSK to 3-tuple mapping and results in a combined modulation and FEC system which can be set partitioned as follows:

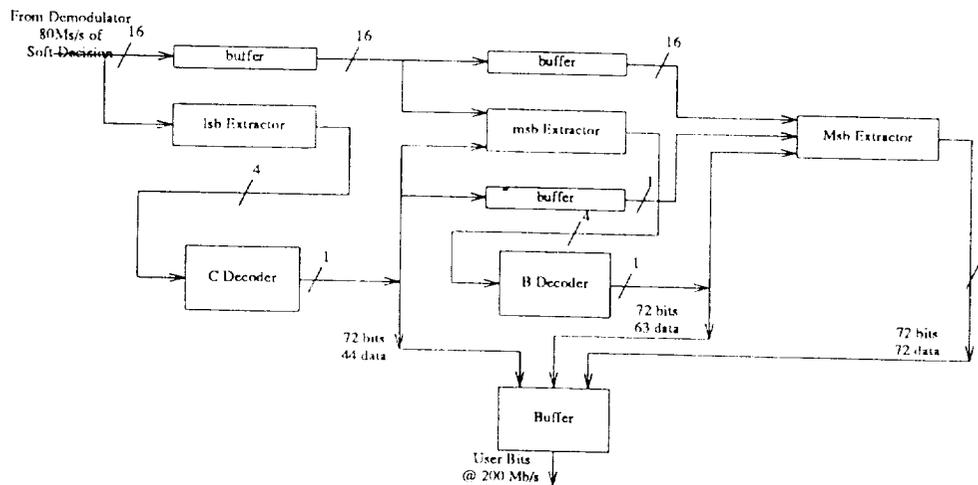
The lsb (the rightmost bit) if it is a 0 signifies one QPSK constellation while if it is a 1, signifies the other QPSK set rotated 45 degrees to the first. Similarly, within each QPSK set, the msb (middle significant bit) signifies one of two BPSK sets. The Msb (Most significant bit) signifies which of the BPSK states is sent. The decoder uses this knowledge of the set partitioning to decode the symbol starting with the lsb and using that information to decode the msb and, finally, uses the lsb and msb information to decode the Msb.

ENCODER SYSTEM



The encoder system shown above takes into account the minimum Euclidean distances (E.D.) between the transmitted phase states. Since the lsb's select between adjacent QPSK constellations which have the smallest E.D., they are encoded with the most powerful code, a shortened 73 bit BCH code of rate 44/72; indicated above as the Code C encoder. The msb's select between alternative BPSK sets within the QPSK sets. Since the BPSK sets have a larger E.D., Code B, which encodes the msb is a lower power Hamming code of rate 63/72. The Msb, since it selects between antipodal states, is uncoded. The overall coding rate is approximately 5/6. The bandwidth expansion is 6/5 which when combined with the 200 MHz uncoded data rate yields 240 Mbps (coded). Using 8PSK with 3 coded bits per symbol and the targeted adjacent channel spacing (using the 0.2 rolloff filter) of 96 MHz, obtains the target bandwidth efficiency of $200/96=2.08$ bits/sec/Hz.

DECODER SYSTEM



A block of 72 8PSK symbols are input from the demodulator to a cascade of buffers each 72 symbols long and 16 bits wide. The input rate is 80 Msps or 240 Mbps (coded). The lsb extractor estimates the lsb sign and soft decision weight from the channel data and passes this information to the C Decoder. The C Decoder performs a soft decision block decoding on the lsb data according to the Tanner Algorithm B (reference 1). The Tanner algorithm has the advantage of a lower computational complexity and is amenable to a highly parallel decoder circuit architecture compared to the traditional BCH hard decision decoders such as those using the Berlekamp-Massey algorithm. The C Decoder will "almost always" correct four errors in a block and can correct up to eight errors.

The channel data along with the lsb decisions are passed to the msb extractor. The lsb decisions are also buffered for use by the msb extractor. The msb extractor estimates the signs of the block of msbs and passes them for decoding in the hard decision B Decoder which is a modified Hamming decoder correcting one error per block. The lsb and msb decisions along with the channel data is passed to the Msb extractor for hard decisions on the block of Msbs. The lsb, msb, and Msb data is serialized and output from the output buffer at 200 Mbps (uncoded). The performance of this decoding system was shown on a previous page. It produces about 5 dB coding gain in AWGN at an output BER of $5e-7$.

Reference 1: R. M. Tanner, "A Recursive Approach to Low Complexity Codes", IEEE Transactions on Information Theory, VOL. IT-27, No. 5, Sept. 1981

SUMMARY

- **CONCEPT OF THE POWER AND BANDWIDTH EFFICIENT SATELLITE DEMODULATOR HAS BEEN PROVEN WITHIN THE BUDGETARY CONSTRAINTS OF THE PROGRAM**
- **BANDWIDTH EFFICIENCY COULD BE DEMONSTRATED (I.E., ACI SPEC MET) THROUGH FILTER IMPROVEMENTS**
- **POWER EFFICIENCY COULD BE DEMONSTRATED (I.E., BER SPEC MET IN AWGN) THROUGH IMPROVEMENTS IN CLOCK RECOVERY LOOP AND FILTERS**
- **DIGITAL PORTION OF THE SATELLITE DEMODULATOR COULD BE REALIZED IN TWO GATE ARRAYS PLUS SOME MEMORY CHIPS, ANALOG PORTION COULD BE GREATLY REDUCED IN SIZE AND WEIGHT BY UTILIZING SAW FILTERS AND AN MMIC QUADRATURE DETECTOR**
- **CODEC PERFORMANCE WITH DEMOD IN CCI PROVEN BY SIMULATION**



N92-22006

RATE 8/9 CODED 8-PSK SYSTEM FOR DOWNLINK APPLICATIONS

Russell Fang, Mark Kappes and Susan Miller
COMSAT Laboratories
Clarksburg, Maryland 20871

ABSTRACT

An advanced Coded Trellis Modulation (CTM) System which achieves a 2 bits/s/Hz bandwidth efficiency at an information rate of 200 Mbit/s while minimizing satellite power requirements, has been developed for downlink earth station applications. This CTM system employs a high-speed rate 8/9 convolutional code with Viterbi decoding and an 8-PSK modem. The minimum Euclidean distance between the modulated waveforms corresponding to the information sequences are maximized in order to maximize the noise immunity of the system. Nyquist filters with square-root 40 percent roll-off are used at the transmit and receive sides of the modem in order to minimize intersymbol interference, adjacent channel interference, and distortion at the nonlinear satellite power amplifier. The use of coded system here also minimizes the effects of co-channel interference. The developed performance of the hardware system has been measured to achieve within 1.5 dB from theory at a bit error rate of 5×10^{-7} over an additive white Gaussian noise channel.

The Viterbi codec subsystem operates at an information rate of 200 Mbit/s and a channel rate of 225 Mbit/s without using parallel processing and is believed to be the highest speed, high code rate Viterbi codec ever built in the world. This codec required the development of 16 special hybrid circuits to realize the 16 add-compare-select (ACS) operations necessary for decoding the 16 state convolutional code with the Viterbi algorithm. These ACS hybrids can operate at a speed as high as 110 MHz. Due to excessive power dissipation, forced air is required for cooling. To minimize power dissipation and the cooling requirements, these ACS hybrid circuits are now being replaced by ECL gate-arrays with lower power dissipation. Each gate-array chip contains two ACS circuits, and hence a total of 8 is needed rather than 16. No forced air will be necessary. These ECL gate-arrays have achieved a clock speed ranging from 120 MHz to 150 MHz. The gate-array upgrade version of the coded 8-PSK system will be completed in the Summer of 1989.

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PROGRAM OBJECTIVES

- To develop an advanced coded trellis modulation system which achieves a 2 Bit/s/Hz bandwidth efficiency at an information rate of 200 Mbit/s while minimizes satellite power requirements for downlink applications.
- Specifically, to develop a rate 8/9 high speed Viterbi FEC codec, a burst-mode 75 MBaud 8-PSK modem, and the associated special test equipment (STE).

PERFORMANCE GOALS

The key performance goals of the coded 8-PSK system are summarized into the table below.

PERFORMANCE GOALS

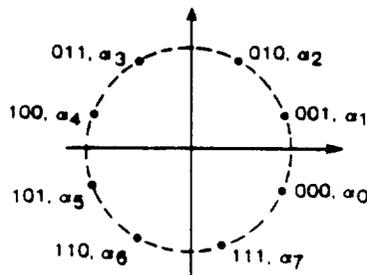
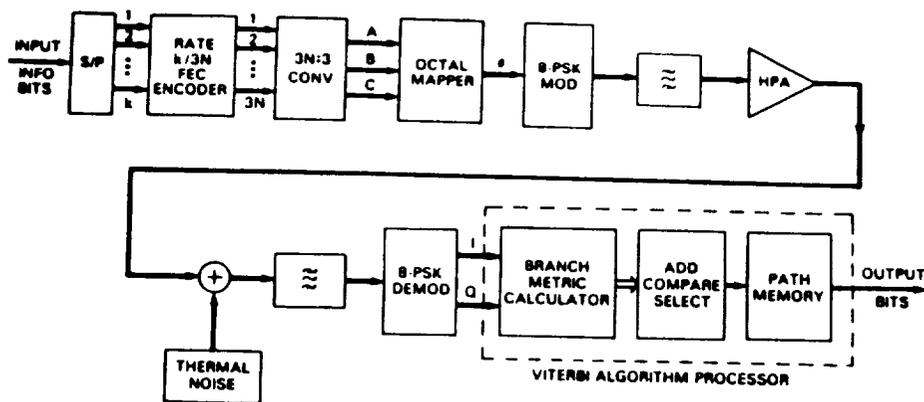
<u>PARAMETER</u>	<u>GOAL</u>
INFORMATION RATE	200 MBPS
8-PSK SYMBOL RATE	75 MSPS
BANDWIDTH EFFICIENCY	2 BIT/S/Hz
CHANNEL BANDWIDTH	100 MHz
FEC CODE RATE & TYPE	8/9, CONVOLUTIONAL
DECODER TYPE	VITERBI @ 75 MHz
GUARD TIME BETWEEN BURSTS	10 usec
PROB. OF MISS AND FALSE UW DETECTION	$<1 \times 10^{-8}$
BURST TO BURST VARIATION	10 dB
BACK-TO-BACK MODEM/CODEC PERFORMANCE	2 dB FROM THEORY @ 5×10^{-7} OVER AWGN CHANNEL
DEGRADATION DUE TO CCI @ C/I=20 dB	$<1 \text{ dB @ } 5 \times 10^{-7}$
DEGRADATION DUE TO ACI @ ACI = 20-dB	$<1 \text{ dB @ } 5 \times 10^{-7}$

SYSTEM OVERVIEW

CODED 8-PSK SYSTEM SYSTEM DESCRIPTION

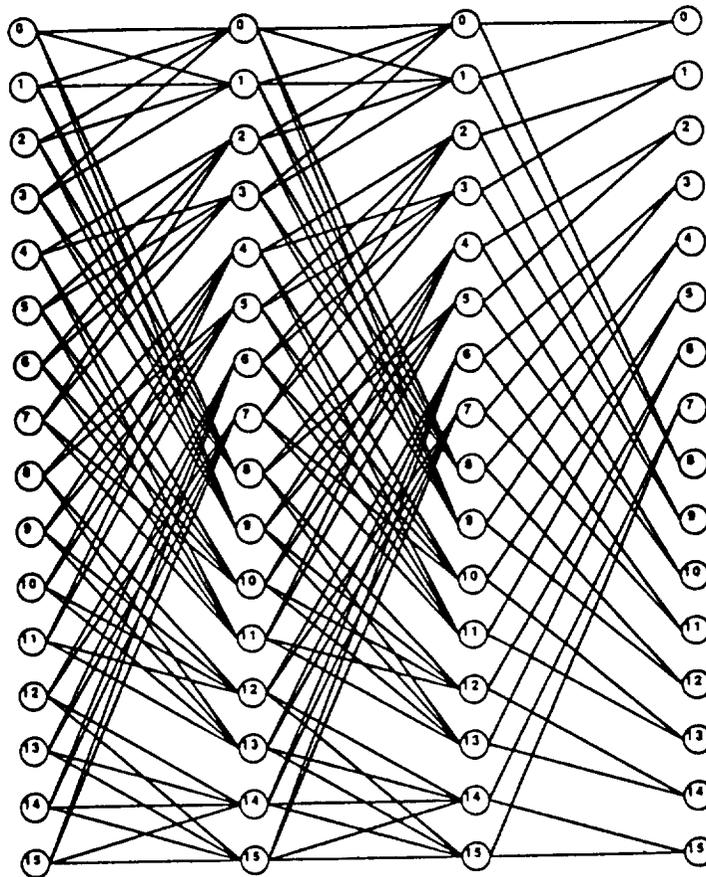
Input information bits at 200 Mbit/s are converted by the serial-to-parallel converter into 8-bit words at 25 MHz. These 8-bit words are encoded by a rate 8/9 convolutional encoder followed by a 3 to 1 parallel-to-serial converter. Thus, these output 3-bit words are at a speed of $25 \times 9 \div 3 = 75$ MHz. Each of these 3-bit word is mapped by an octal mapper into one of the 8 phases for transmission by an 8-PSK modulator at 75 Msps.

CODED 8-PSK SYSTEM



TRELLIS REPRESENTATION

The output of the modulator can be represented by a trellis. To maximize the system noise immunity, the convolutional encoder and the octal mapping function are optimized to maximize the minimum Euclidean distance between the code word sequences at the output of the modulator rather than merely the minimum Hamming distance between the algebraic code words at the input of the octal mapper. To further simplify the codec implementation a time varying code is selected, which is composed of three subcodes of rate $3/3$, $3/3$, and $2/3$ each.

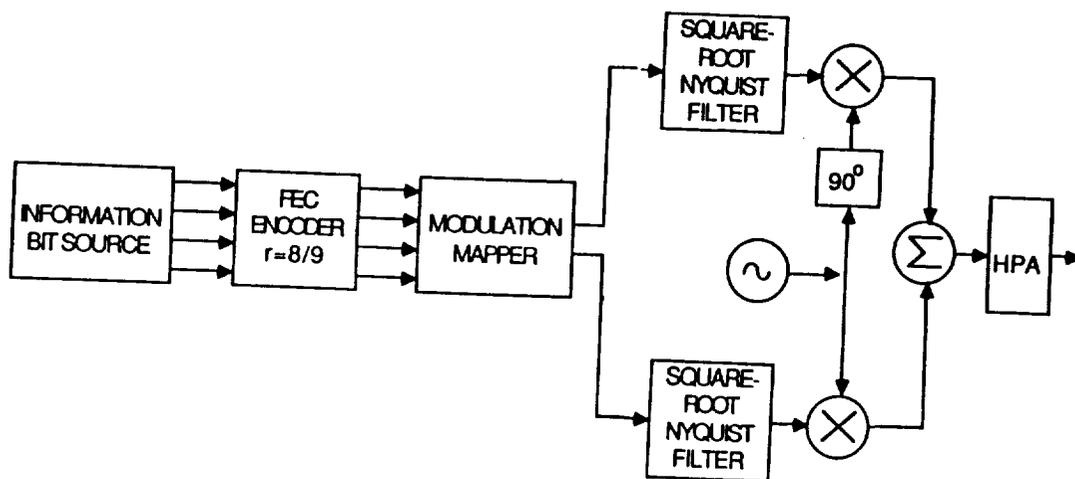


TRELLIS OF RATE 8/9 CODE

8-PSK MODULATOR

The 8-PSK modulator employs a quadrature modulation structure. The shaping filters are realized in the baseband. To minimize intersymbol interference and adjacent channel interference, 40 percent square root Nyquist filters are employed.

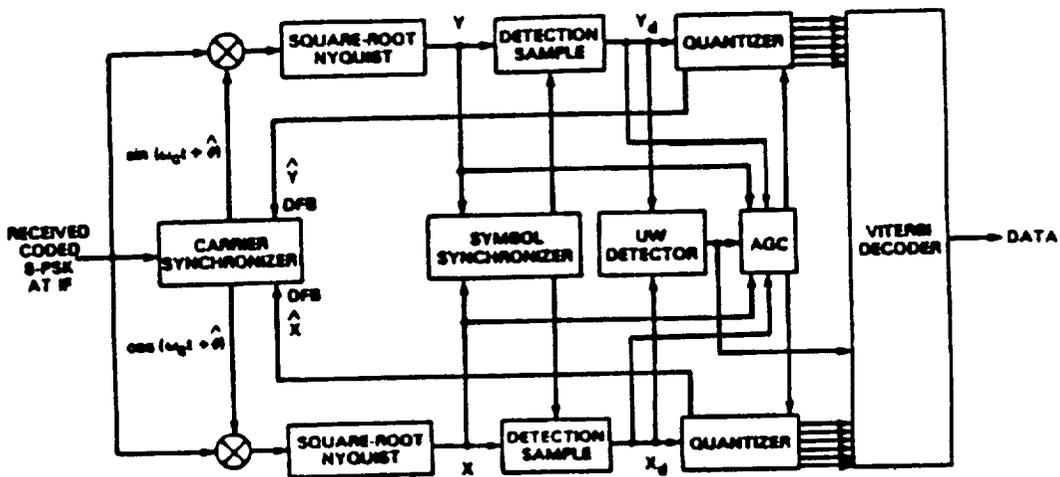
GENERATION OF CODED OPSK BY THE USE OF A QUADRATURE MODULATOR



8-PSK DEMODULATION

The received coded 8-PSK signals are coherently detected into in phase and quadrature components by first recovering the carrier. Nyquist filters with 40 percent roll off are then employed to match filter these two components. After symbol timing, UW and AGC are obtained, these two quadrature components are sampled and quantized into 5-bit words for Viterbi decoding.

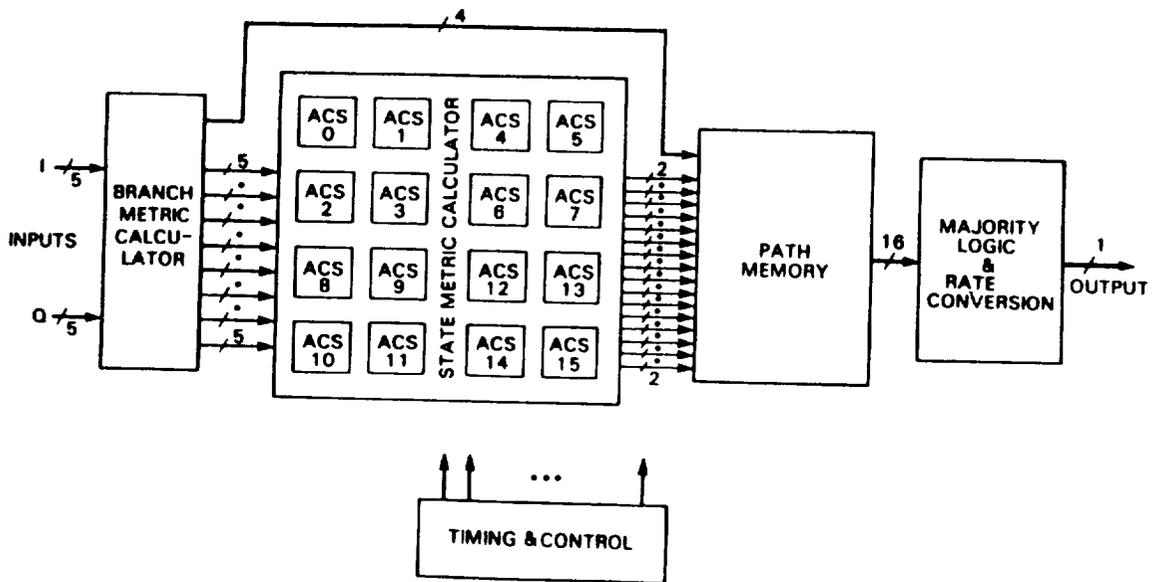
DEMODULATOR



VITERBI DECODER

The Viterbi decoder takes the 5-bit I and Q components from the 8-PSK demodulator and performs the following functions: (i) branch metric calculation for each branch leading into each code state, (ii) adding branch metric to the path metric leading into each code state, comparing them, and selecting the largest cumulative path metric as the new state metric, and (iii) path memory traceback for recovering the corresponding information sequence.

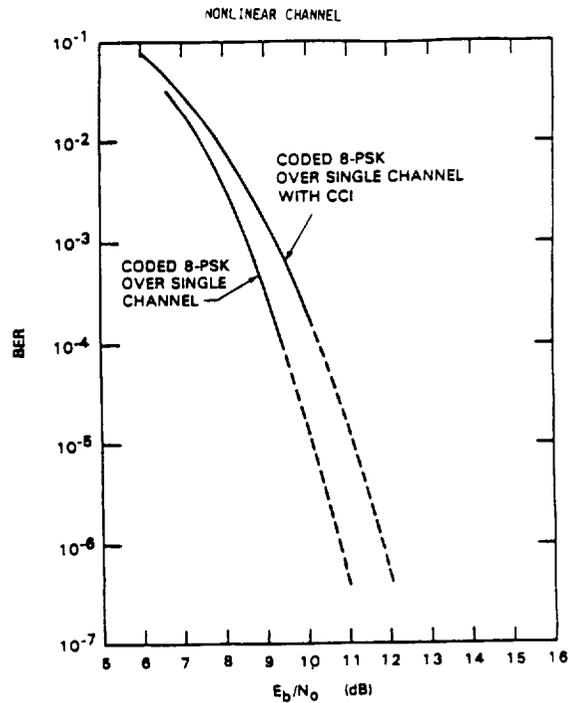
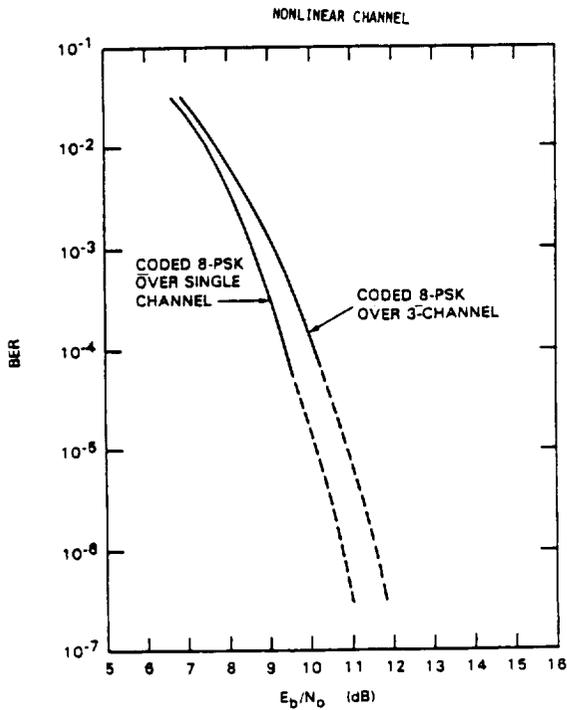
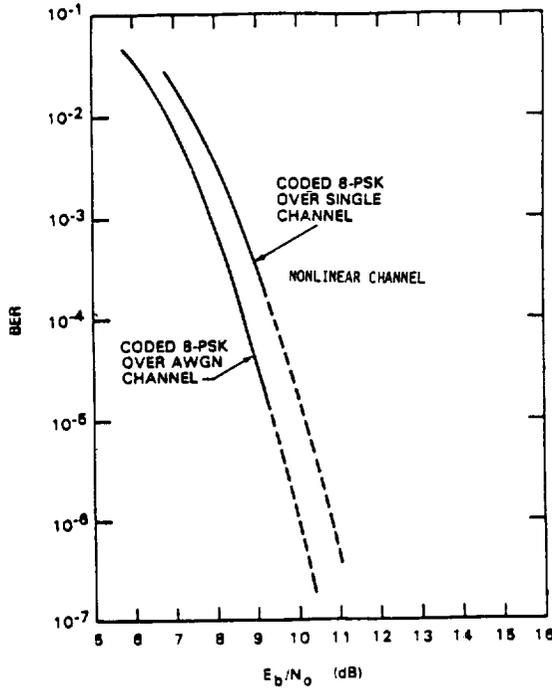
MAXIMUM-LIKELIHOOD VITERBI DECODER



PERFORMANCE SIMULATION

Performance of the rate 8/9 coded 8-PSK system has been simulated for various channel conditions including: (i) AWGN channel, (ii) a single nonlinear satellite channel, (iii) three contiguous nonlinear satellite channels, and (iv) a single nonlinear satellite channel with co-channel interference. In all cases, 40 percent roll off square root Nuquist filters are employed.

COMPARISON OF CODED TRANSMISSION OVER THE LINEAR AND NONLINEAR CHANNEL



Viterbi decoding is an implementation of maximum likelihood decoding for convolutional codes. The output of a maximum likelihood decoding of any sequence of received symbols, \mathbf{y} , is that sequence of transmitted symbols, \mathbf{x}' , which maximizes the conditional probability:

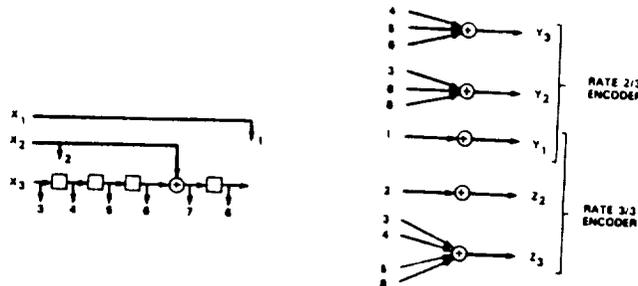
$$\mathbf{x}' = \mathbf{x}_m \text{ if } \Pr(\mathbf{x}_m|\mathbf{y}) > \Pr(\mathbf{x}_{m'}|\mathbf{y}) \text{ for all } m' \neq m \quad (1)$$

This rule will result in minimum probability of error. Equivalently, the logarithm of the probability can be maximized, since the logarithm is a monotonically increasing function. If the symbols are independent, the logarithm of this joint probability can be decomposed into the sum of the logarithms:

$$\ln \Pr(\mathbf{x}|\mathbf{y}) = \sum \ln \Pr(x_i|y_i) \quad (2)$$

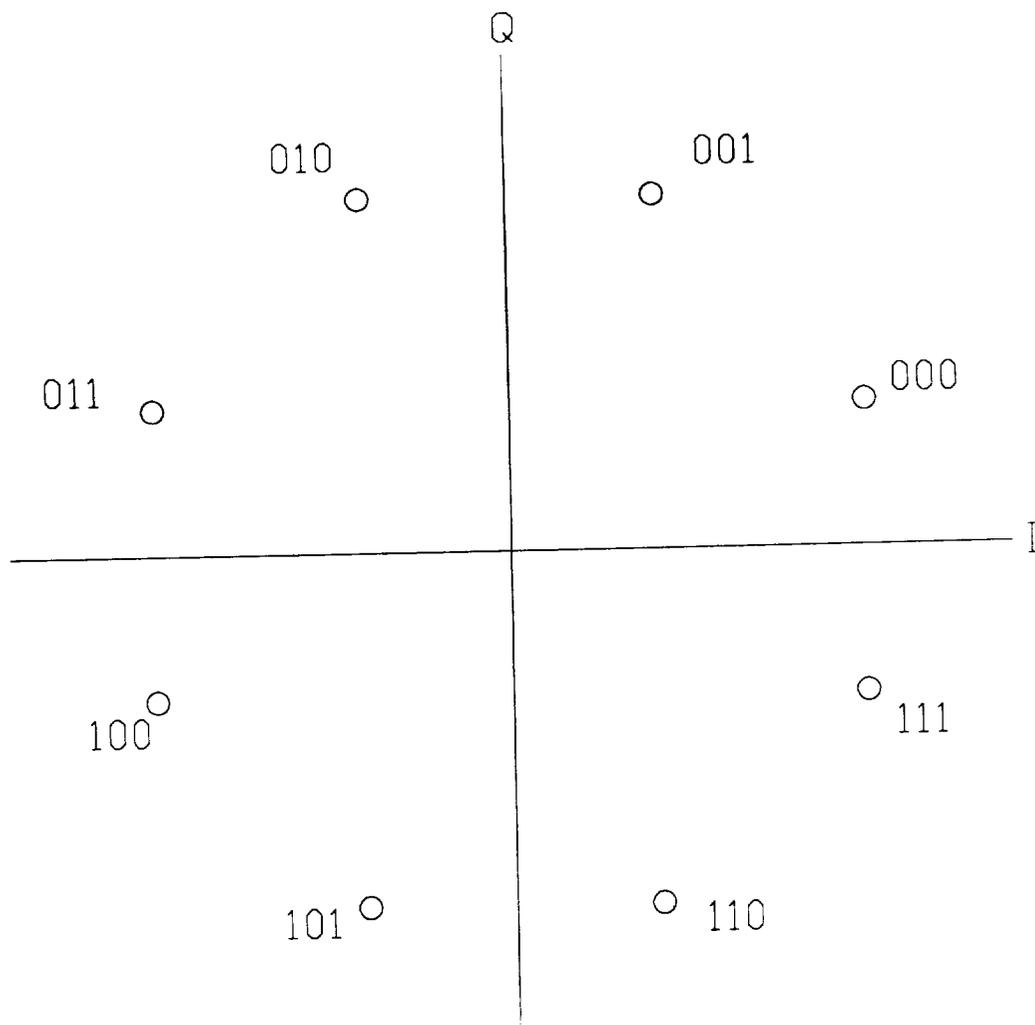
Thus, maximum likelihood decoding of independent symbols is performed by finding the set of symbols, x_i , which maximizes this sum of conditional probabilities. The convolutional coding system used here is based on a finite state machine and can therefore be represented by a trellis diagram. Because the encoder has finite memory, the summations in (2) do not have to be taken over a set of sequences that increases exponentially without bounds over increasing sequence length. Instead, each sequence can be considered as one path through the trellis diagram. Whenever two or more paths merge in the same state, only the best path needs to be followed. Thus, rather than forming an unlimited number of summations over all possible sequences, there need be only a finite number of summations, one for each state.

The convolutional encoder used in this application implements a periodically time-varying code, with a period of three symbols. The first symbol is formed from two information bits, while the second and third symbols are formed from three information bits. This gives a total of 8 information bits forming three octal symbols, for an overall rate of 8/9. The four bit memory of the encoder implies 16 possible code states. Notice, too, that the MSB of each output symbol is identical to one of the information bits; this bit is referred to as uncoded. The introduction of the uncoded bits through the encoder is one of the factors that allows the decoder design to depart from that of a conventional Viterbi decoder.



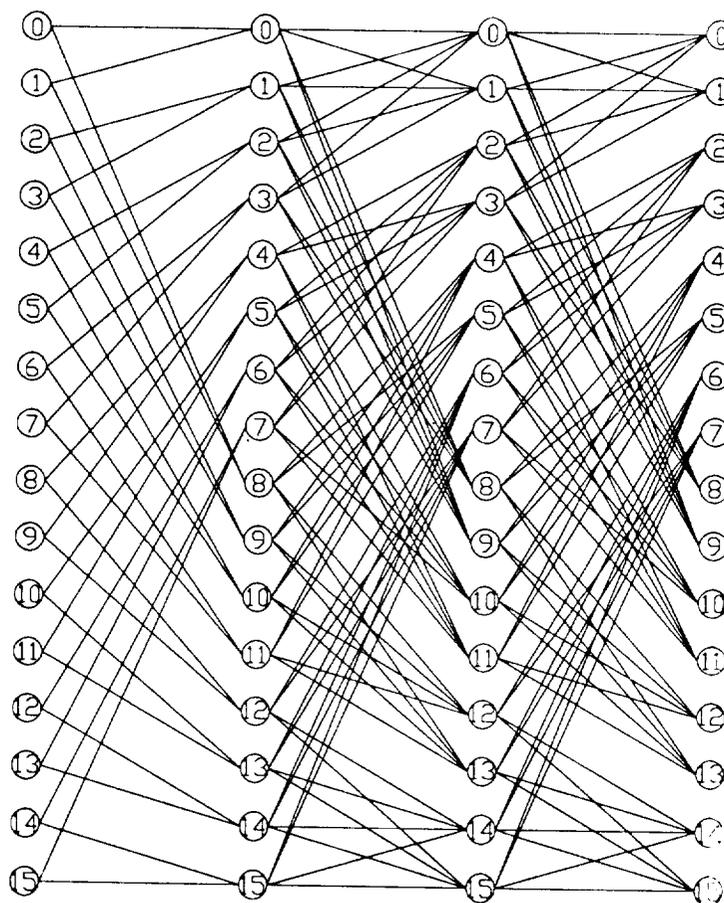
Rate 8/9 Time-varying Convolutional Encoder Block Diagram.

The encoder output symbols are mapped into 8-PSK modulator input symbols in such a way as to maximize the Euclidean distance between them. As mentioned previously, one bit of each symbol is uncoded, in the sense that it does not affect the state of the encoder. Under mapping, this bit selects between antipodal symbols. The large Euclidean distance between the uncoded bits is sufficient to decode the points without additional error protection. However, decoding of the uncoded bits leads to a new design complexity. While these bits are simply decoded by a binary hard decision as in BPSK, the axis on which the decision is made is not known by the decoder a priori. There are four possible decision axes corresponding to the two lower bits of each symbol. The BPSK hard decision must be made after the Viterbi processor determines the two lower bits of each symbol.



8-PSK Mapping of Encoded Symbols.

Considering the four bit convolutional encoder finite state machine operation, the rate 8/9 code can be represented by this 16-state trellis diagram. Any sequence of symbols can be represented as a path through this trellis diagram. One full period of the periodically time-varying code is shown. On two of the code steps, there are four possible paths into each state, while on the third step there are two possible paths into each state. Actually, each of the branches on the trellis is a double branch, since two different information sequences, differing in the uncoded bit, can lead to the same state transition. The maximum likelihood decoding procedure for this code selects the best of the four inputs into each state as each symbol is received and resolves the double branch issue as a BPSK decision using the path information selected from the trellis decoding. During the time-varying steps of the trellis decoding process, the hardware control multiplexes different inputs into the state processors that correspond to the branch metrics for the related encoder transitions.



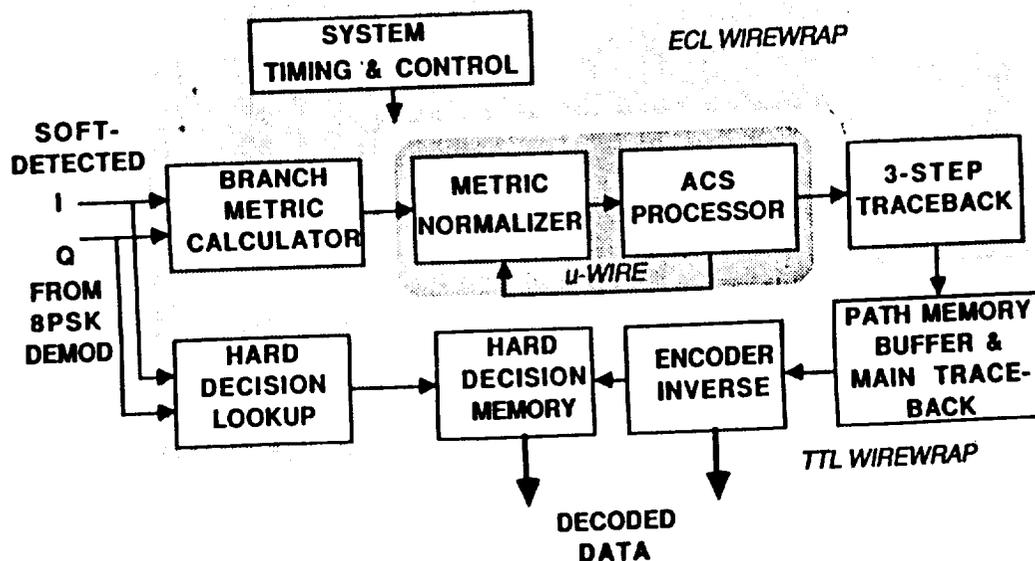
Trellis of Rate 8/9 Code.

The hardware implementation of the Viterbi decoder is divided into 8 major functions. These are:

- branch metric calculator
- hard decision lookup
- metric normalizer
- ACS processor
- 3-step traceback
- main traceback
- hard decision memory
- encoder inverse

The functions are grouped into circuit boards according to the board packaging technology used. The different technologies are :

- ECL wirewrap
- Microwire
- TTL wirewrap



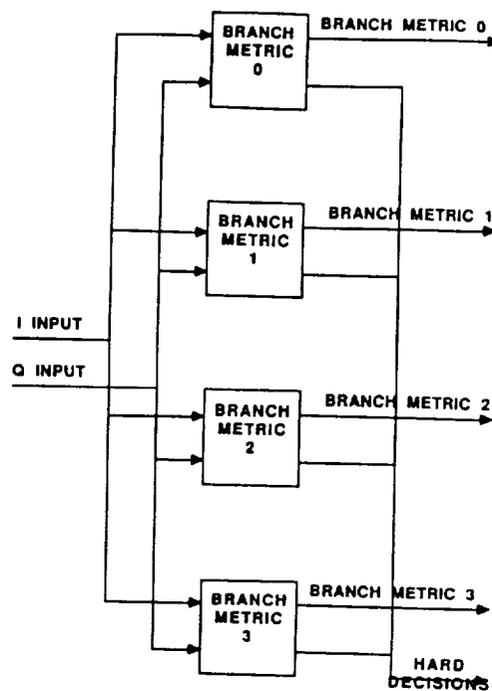
Viterbi Decoder Block Diagram.

For independent symbols over an AWGN channel, the branch metrics are linearly related to the log of the conditional probability :

$$BM(\underline{x}, \underline{y}) \sim \ln[\Pr(\underline{x}|\underline{y})] \sim (\underline{y} - \underline{x})^2$$

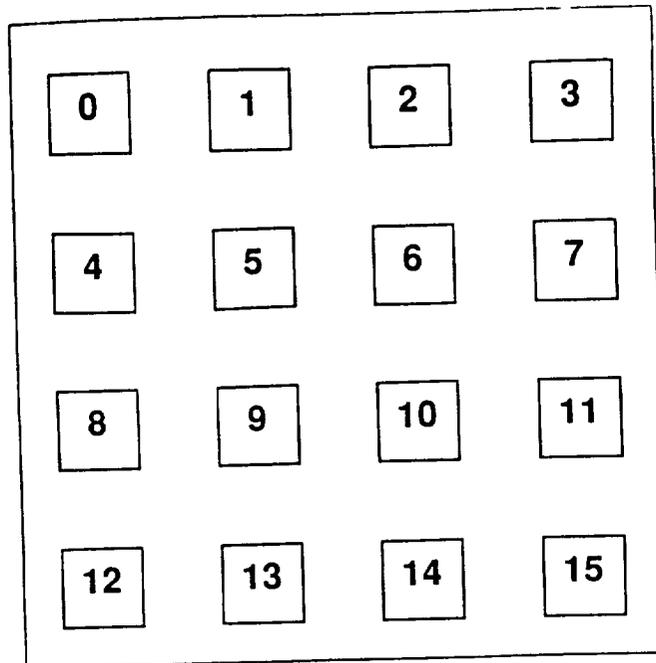
where \underline{y} is the received symbol vector and \underline{x} is the transmitted symbol vector. These branch metrics are the inputs to the ACS processor. The uncoded bits are decoded by a simple binary antipodal decision, called a hard decision, since the uncoded bit is used to select antipodal symbols. The correct axis to use for the binary decision is not known until the other two bits in the symbol are decoded, so all four possible decisions are made on the input vector and these decisions are stored for later use.

The branch metric calculation and hard decision operations are both performed in parallel by a simple table lookup in the decoder. The table is formatted so that it automatically selects the closest of the pairs of symbols. There are four six bit branch metrics and four sets of 1 bit hard decisions for each (I,Q) input vector from the demodulator.



Branch Metric and Hard Decision Lookup Block Diagram.

The state metric calculator is the heart of the Viterbi decoder, and must operate at the received symbol rate. It consists of 16 Add-Compare-Select (ACS) units, one for each code state. Each ACS unit has four branch metric inputs and four corresponding state metric inputs. The state metric output of each ACS unit connects to the state metric inputs of four ACS units, in the same interconnection pattern as shown in the trellis diagram. Because the code is time-varying, during the rate 2/3 code step only two sets of inputs are used, while on the rate 3/3 code steps all four inputs are used. The ACS units have additional inputs which are used to disable the unused branch and state metric inputs during the rate 2/3 step. These ACS units compute the accumulated path metrics (state metrics) by adding the branch metric inputs to the corresponding state metric, and selecting the minimum (most likely) as the new state metric for that state. The ACS units also output a binary code at each symbol interval, indicating which of the input branches was selected. This branch select information is used by the traceback circuits.

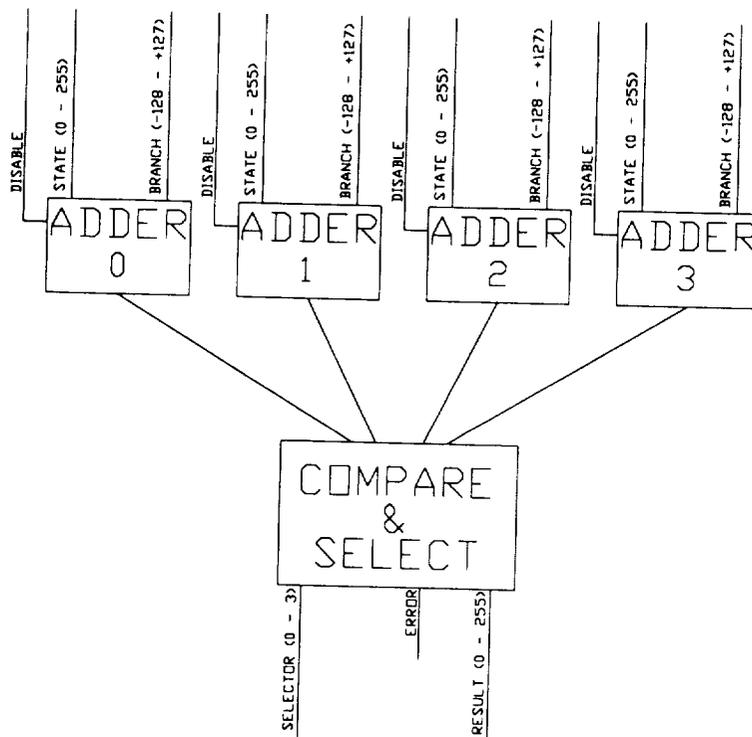


State Metric Calculator Block Diagram.

Each ACS unit has four high speed adders operating in parallel which add the state metric input values to the corresponding branch metric input values. These four path metrics are then compared and the minimum is chosen and sent to the output of the device as the new state metric. The comparison is performed by six comparators, which perform all pairwise comparisons of the four path metrics in parallel. The selection is performed by two levels of basic gates which operate directly from the comparator outputs. The ACS unit also provides a binary output indicating which of the four input branches was chosen. The ACS unit operates at the symbol rate.

The AMTD Rate 8/9 decoder was originally designed with an ACS unit that was fabricated as a high speed ECL hybrid circuit containing 22 100K ECL devices with two-level metal interconnect, controlled impedance lines, and thin film terminations.

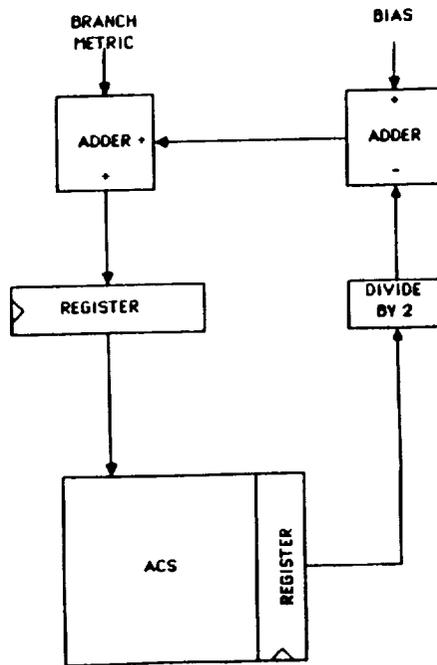
A recent modification to the AMTD Rate 8/9 decoder included the conversion of the ACS unit design into a monolithic high speed ECL gate array. This new ACS unit will be incorporated into the state metric calculator and will improve the overall power consumption of the system, as well as provide greater timing margin to this time critical portion of the system.



ACS Unit Block Diagram.

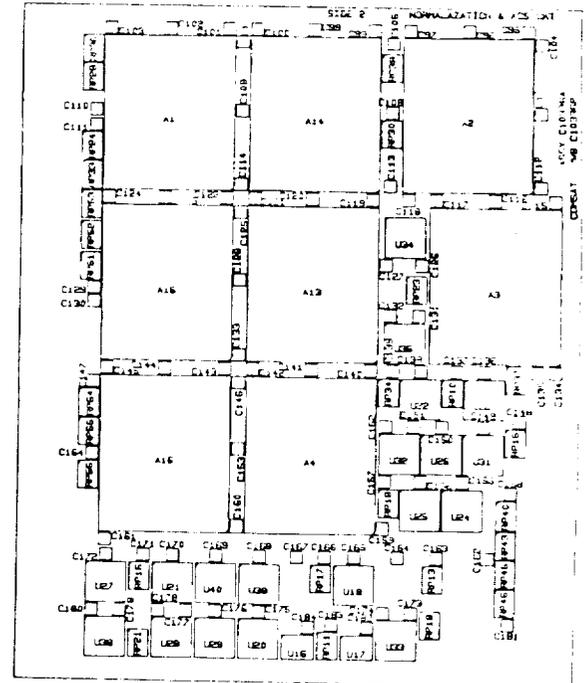
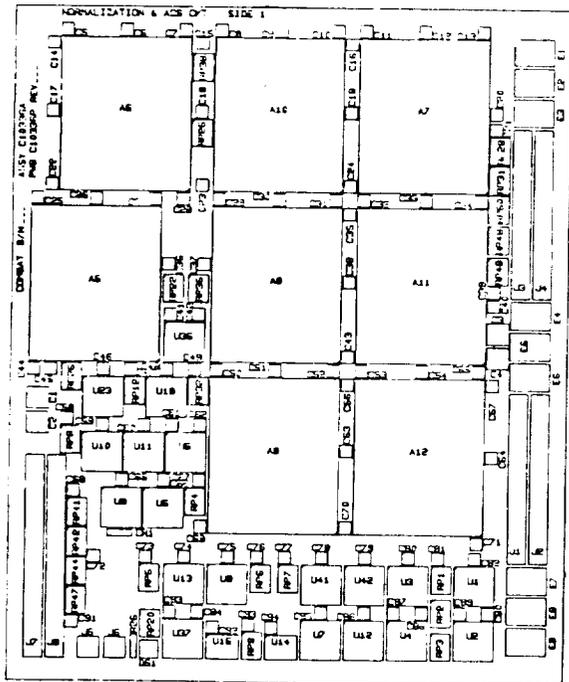
The state metrics accumulated by the ACS units would naturally tend to grow larger in value over time, eventually overflowing the finite arithmetic capacity of these units if some precautions were not taken to prevent it. A commonly used technique to prevent overflow subtracts some value from all of the state metrics periodically. This procedure is called normalization. Ideally, the minimum state metric value is found and subtracted from the others, so that the minimum becomes zero, but this is impractical for high speed implementation since the task of finding the minimum from 16 state metrics is quite difficult at high speeds.

In this design, an arbitrarily selected metric is subtracted from the others, a procedure more suited to high speed implementation. This technique is not optimum, since the dynamic range of the state metrics is doubled, but it involves far less hardware complexity than the traditional method. The subtraction is done to the branch metric inputs, rather than in the ACS operation, thus removing the subtraction from the time critical paths, and reducing the number of subtraction circuits required.



Normalization Block Diagram.

The ACS Processor board is a high speed (75 MHz) design that implements the normalization and state metric calculation functions. It incorporates 16 large ACS ECL units in a highly interconnected network. The circuit requires a large surface area while the high speed operation requirement places severe limitations on the length of the interconnecting signal wires. To overcome this problem, half of the parts were placed on each side of a Microwire board so that the surface area that the wires need to traverse is effectively cut in half, thus reducing the length of the wires to a distance which supports the critical operating speed requirement. Microwire technology supports surface mount technology, and provides a controlled impedance environment and reduced signal crosstalk.

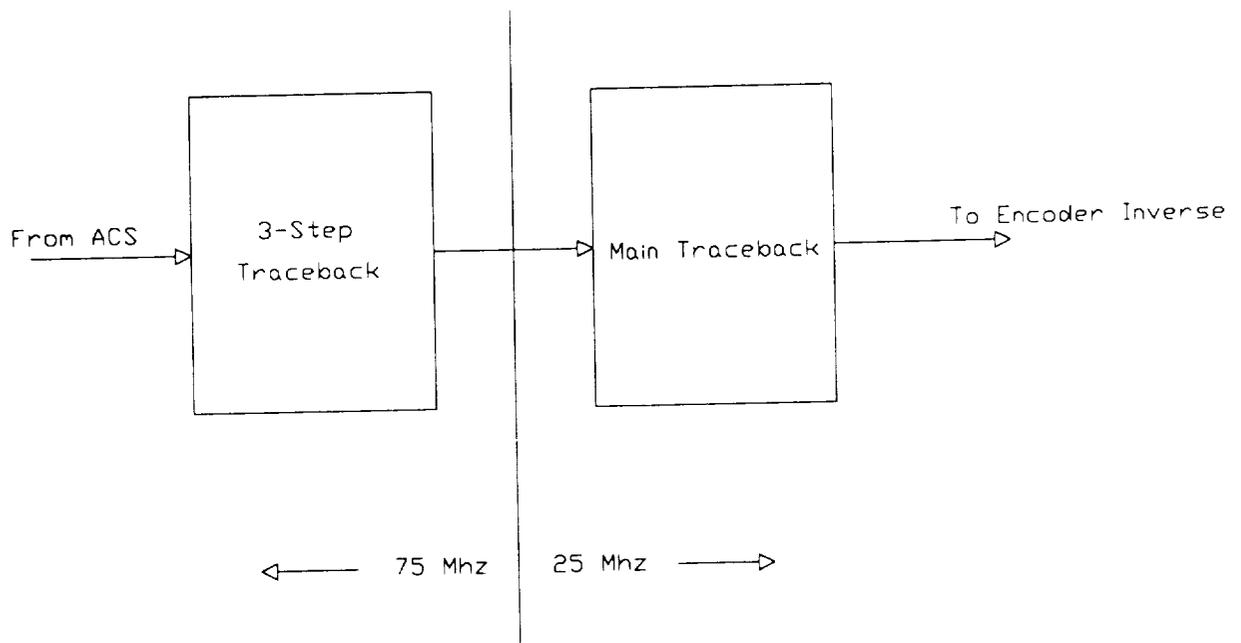


Two-sided ACS Processor Board Layout.

The traceback, or the path memory, is the final step in the decoding process. Starting at an arbitrary state, the most likely path is traced backward in time a finite number of symbols. This gives an estimate of the most likely state sequence, from which the information bits can be derived.

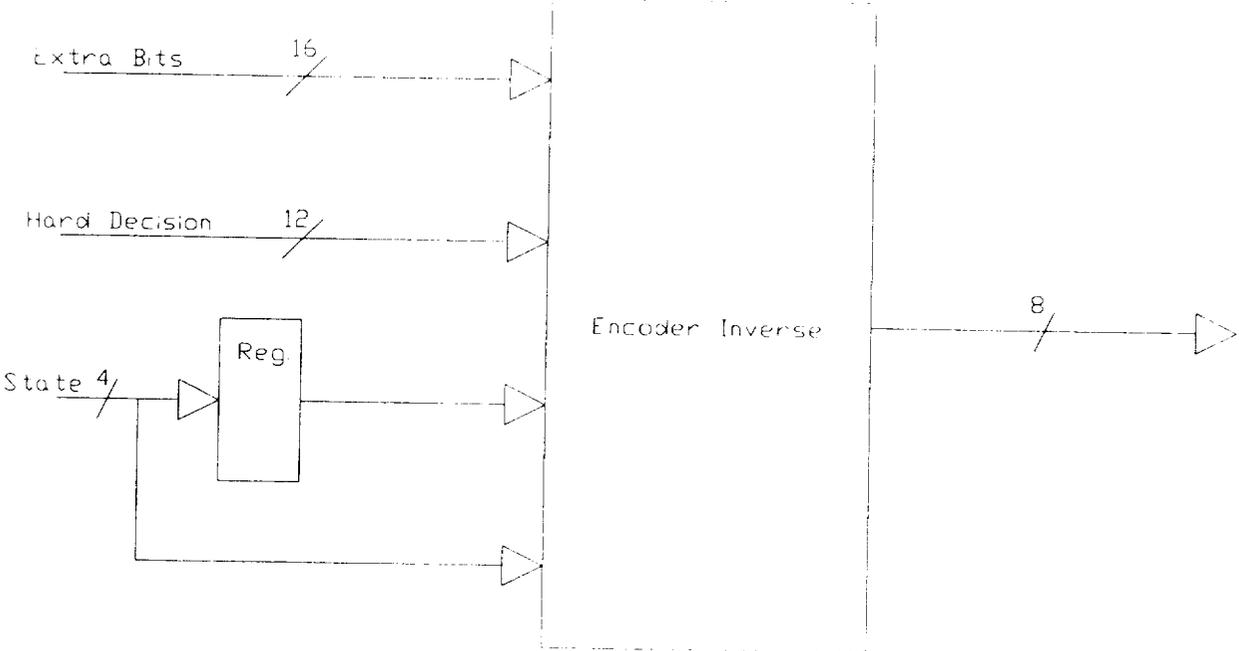
The unique design employed here divides the traceback operation into two stages. The first stage, performed at the symbol rate uses the branch selection outputs from the ACS units. For this process the ACS branch select outputs are transformed into a best predecessor state and processed by the three-step traceback circuits. There are 16 three-step traceback circuits, one for each code state. They have low complexity, and operate easily at the symbol rate. The output of these 16 circuits is the best predecessor to each state over 3 steps. These best predecessor state results are fed to the main traceback, which operates at 1/3 of the symbol rate, allowing the use of TTL and CMOS circuitry.

The main traceback circuit completes the traceback function by finding the best estimate of the sequence of encoder states for some finite path history. This circuit processes three code steps at a time. The unique design not only allows the main traceback to operate at 1/3 of the symbol rate, but it also reduces the number of processing stages by a factor of three. Each stage of the traceback finds the best predecessor state to the state number input to that stage. The main traceback circuit uses a pipelined architecture to perform the traceback in real time.



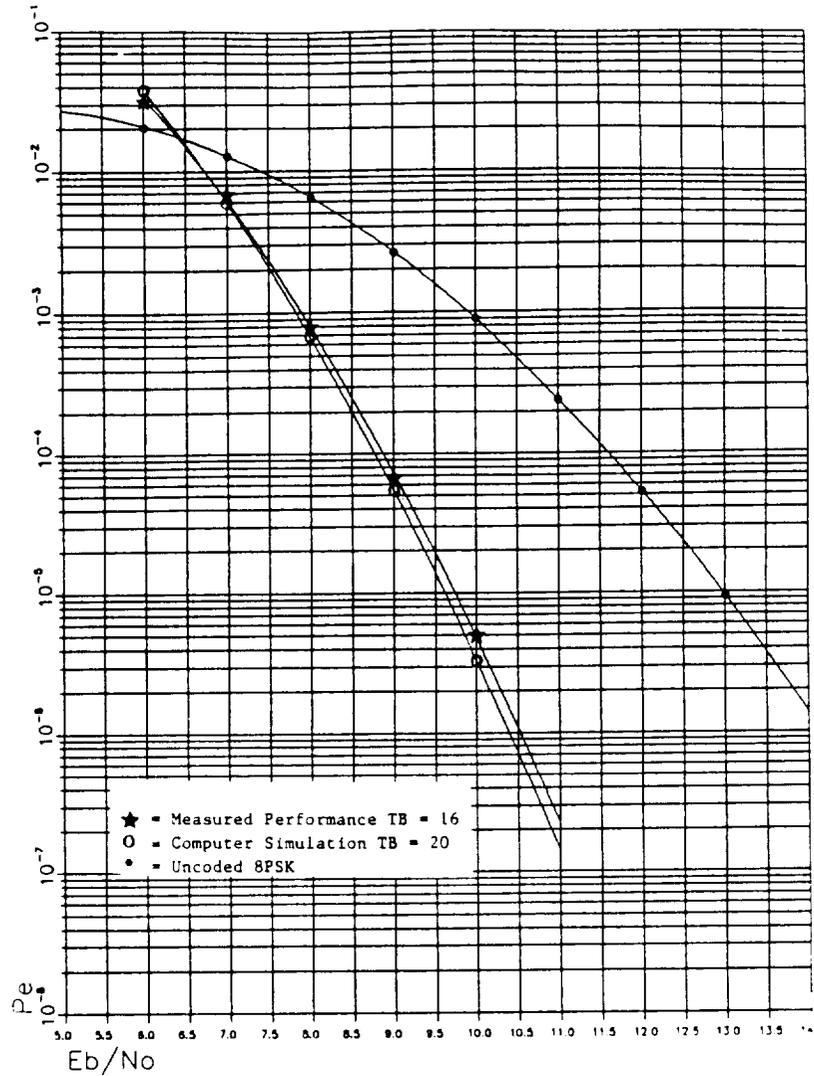
Traceback Partitioning.

The encoder inverse uses the information from the main traceback and the hard decision memory to derive the best estimate of the information bits. The coded bits are obtained from the estimate of the encoder state sequence by combinatorial algebraic processing. The encoder inverse uses the state sequence to select the appropriate bits from the hard decision memory, which gives the estimate of the uncoded information bits.



Encoder Inverse Block Diagram.

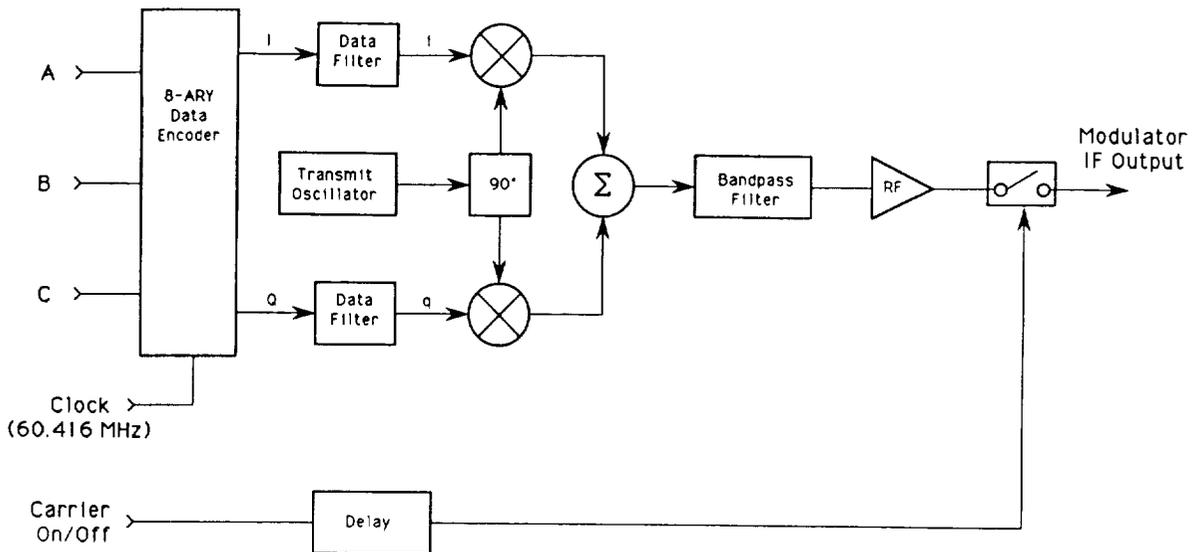
Performance of the rate 8/9 Viterbi decoder was measured at an operating frequency of 75 MSPS using a specially developed digital noise test set which simulated an AWGN channel with an ideal modem. As shown in the performance curve, the rate 8/9 time-varying convolutional decoder is capable of providing a BER of 10^{-6} at an E_b/N_0 of 10.6 dB, assuming a perfect modem. This compares favorably with uncoded 8PSK which requires approximately 14 dB to give the same error rate performance.



BER for Rate 8/9 Codec Over AWGN Channel.

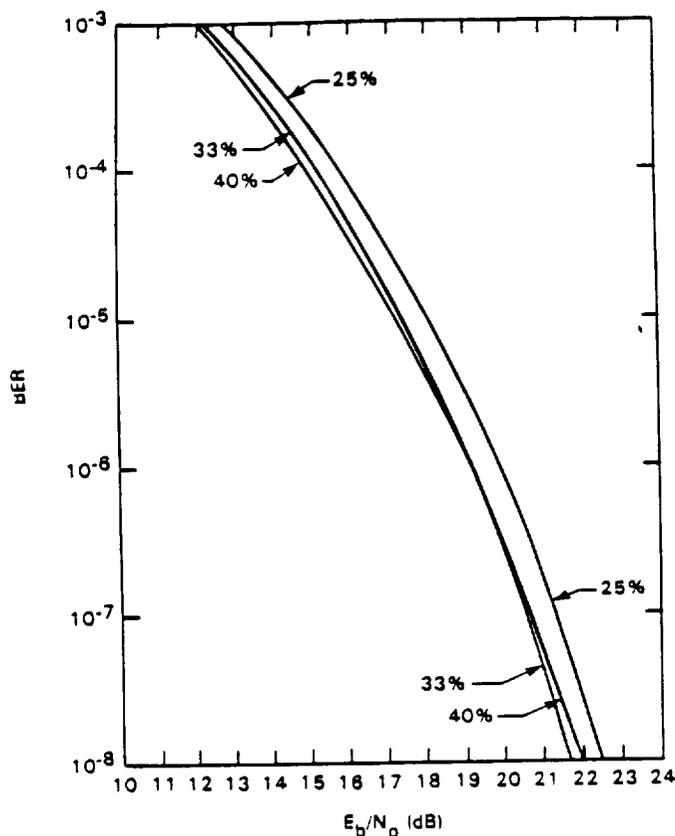
8-PSK MODULATOR

The 8-PSK modulator receives the three bits from the encoder and maps these bits into the proper level to obtain the correct carrier phase. This results in one of four levels which appear at the I and Q channel data filter inputs. These four level signals are filtered with a square root 40% raised cosine filter which also employs $x/\sin x$ equalization. These signals then modulate quadrature components of the IF carrier. The signals are then combined, filtered, amplified and passed through an IF switch used for burst mode operation.



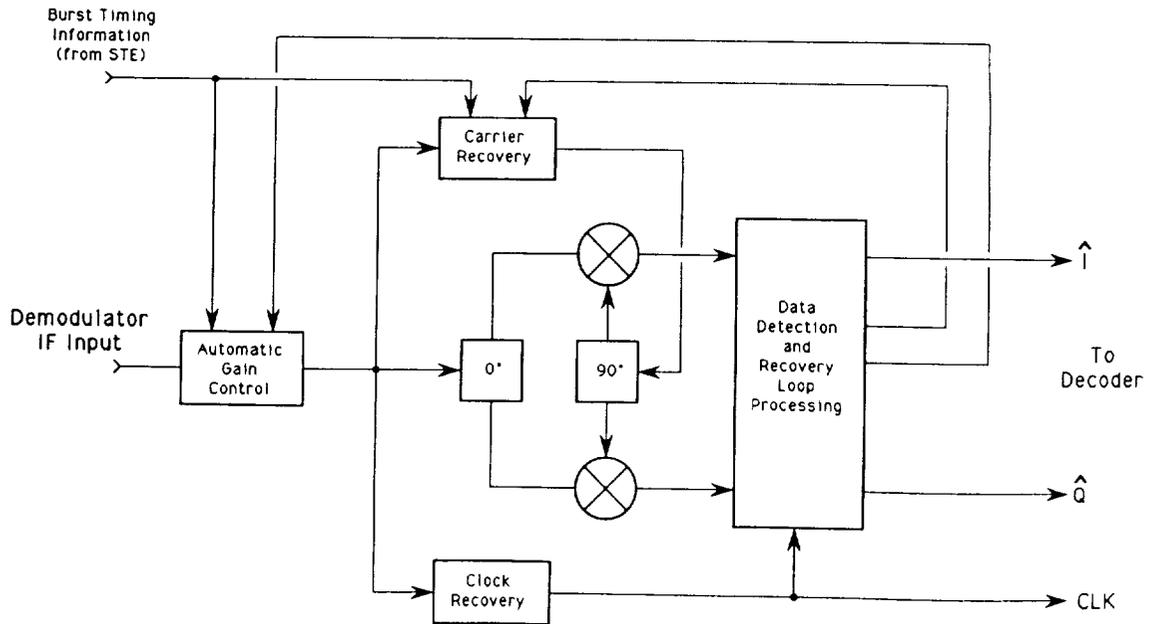
DATA FILTER ROLLOFF SELECTION

Selection of the data filter rolloff characteristics for the coded 8-PSK system was based on computer simulations through a nonlinear channel with adjacent channel interference. Assuming a code rate of 8/9 and an information rate of 200 Mbit/s, the resulting 8-PSK symbol rate is 75 Msymbols/s. The adjacent channels are assumed to be at 100 MHz spacing to give the required 2 bits/s/Hz bandwidth efficiency. Results of BER vs E_b/N_0 performance simulations of the 8-PSK modem under these conditions with raised cosine filters of varying rolloffs is shown below. The choice is between 33% and 40% rolloff, since each performs better in one segment of the E_b/N_0 range. The 40% rolloff filter was selected due to ease of implementation and its slightly better performance in the range of E_b/N_0 where actual operation is anticipated.



OVERALL DEMODULATOR BLOCK DIAGRAM

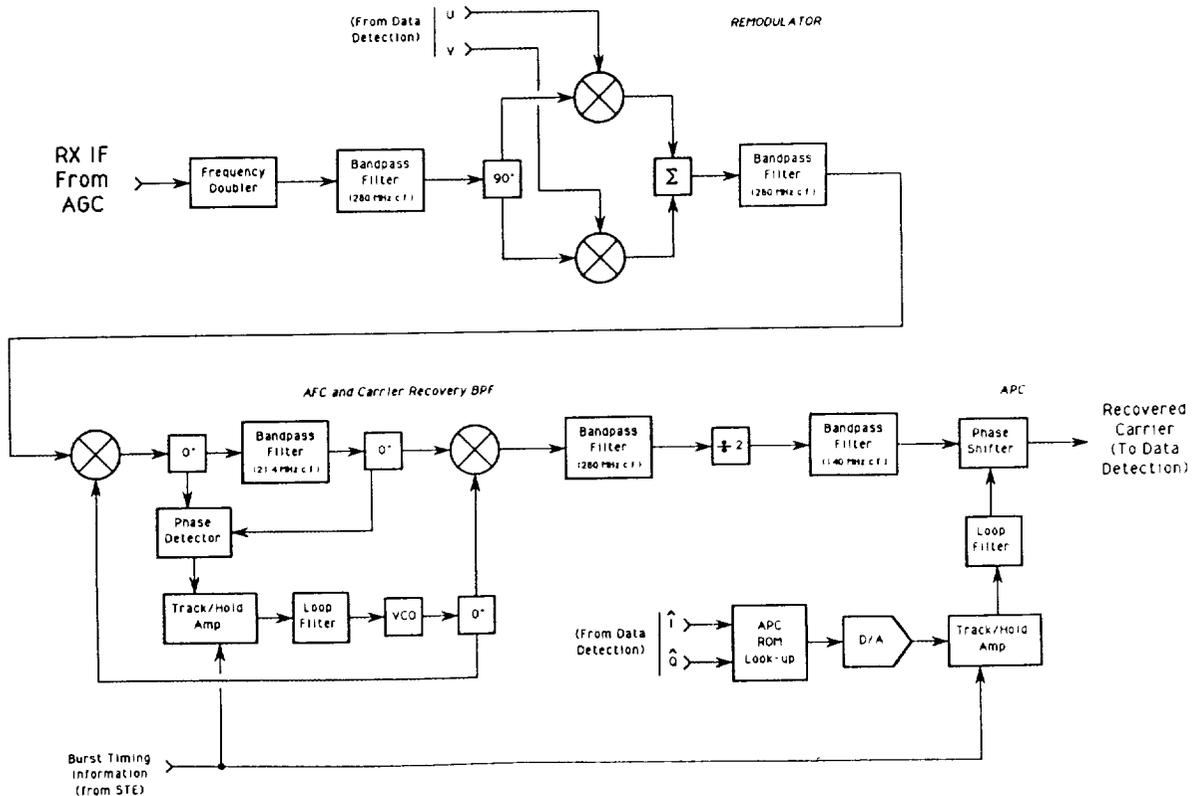
The demodulator receives the incoming IF signal at 140 MHz, removes level variations through the use of automatic gain control (AGC), recovers the carrier and clock references, demodulates the 8-PSK signal into quadrature paths, and provides 5 bit soft detected data to the decoder. Burst timing information for the various demodulator functions is received from the special test equipment. The major components of the demodulator are shown in the block diagram below and will be detailed further in the following charts.



CARRIER RECOVERY FOR 8-PSK

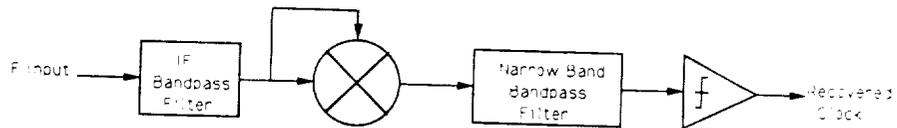
The carrier recovery circuit shown in block diagram form below, must recover a replica of the transmitted unmodulated carrier from the 8-PSK spectrum with low phase jitter. The circuit must be capable of operation in burst mode and handle IF frequency offsets of ± 25 KHz. Additionally, the stability of the absolute phase reference must be maintained to a high degree due to the sensitivity of 8-PSK to phase offsets.

The basic principle of operation for the carrier recovery is a modified decision feedback structure. The incoming IF is first doubled, which maps the eight phase states of the signal into only four phase states. This greatly simplifies the decision feedback implementation, since the multipliers are now ± 1 rather than the 8-PSK values of ± 0.383 and ± 0.924 . Once the modulation is removed, the signal is passed through a narrow band filter embedded in an automatic frequency control (AFC) loop. The AFC is used to keep the recovered carrier signal in the center of the filter passband thereby reducing phase offsets due to frequency variations. The AFC loop functions in a track and hold mode for burst operation. After division by two, the phase of the carrier reference is adjusted by an automatic phase control (APC) circuit which monitors the receive eye patterns and maintains the phase at the correct value. The APC also operates in burst mode via a track and hold circuit.



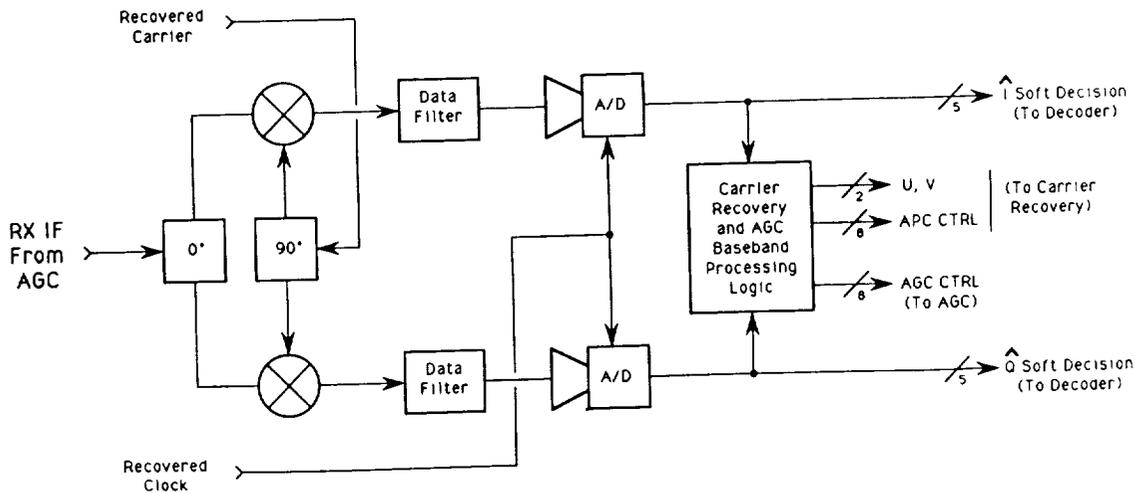
SYMBOL TIMING RECOVERY

Symbol timing recovery is accomplished by taking advantage of the envelope fluctuations introduced by bandlimiting of the 8-PSK signal. After bandpass filtering, the IF is frequency multiplied by two and the clock component extracted by the narrow band filter. An ECL comparator then converts the signal to the proper ECL level for distribution to the data detection circuits.



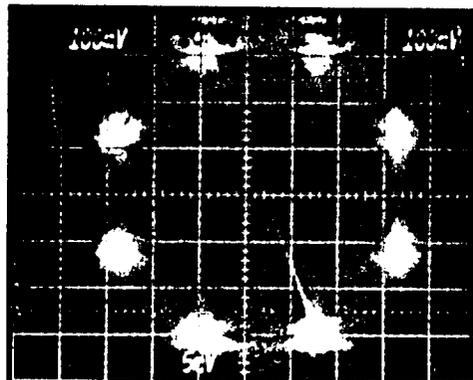
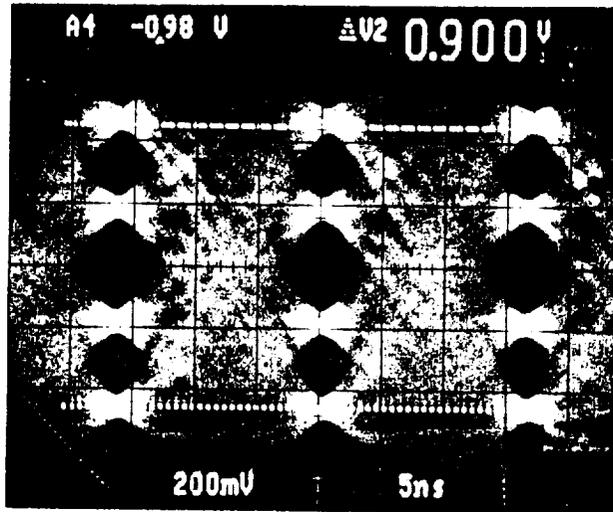
DEMODULATION AND DATA DETECTION

The demodulator shown in the block diagram below first separates the data into two quadrature paths using the recovered carrier. The resulting baseband signals are filtered by square root 40% raised cosine filters to obtain the multilevel eye patterns and then sampled by a 6 bit flash A/D converter. These digitized waveforms are then processed to obtain the U and V decision feedback values as well as the AGC and APC control values. The five most significant bits are passed to the unique word detector for unique word detection and phase ambiguity removal before entering the decoder



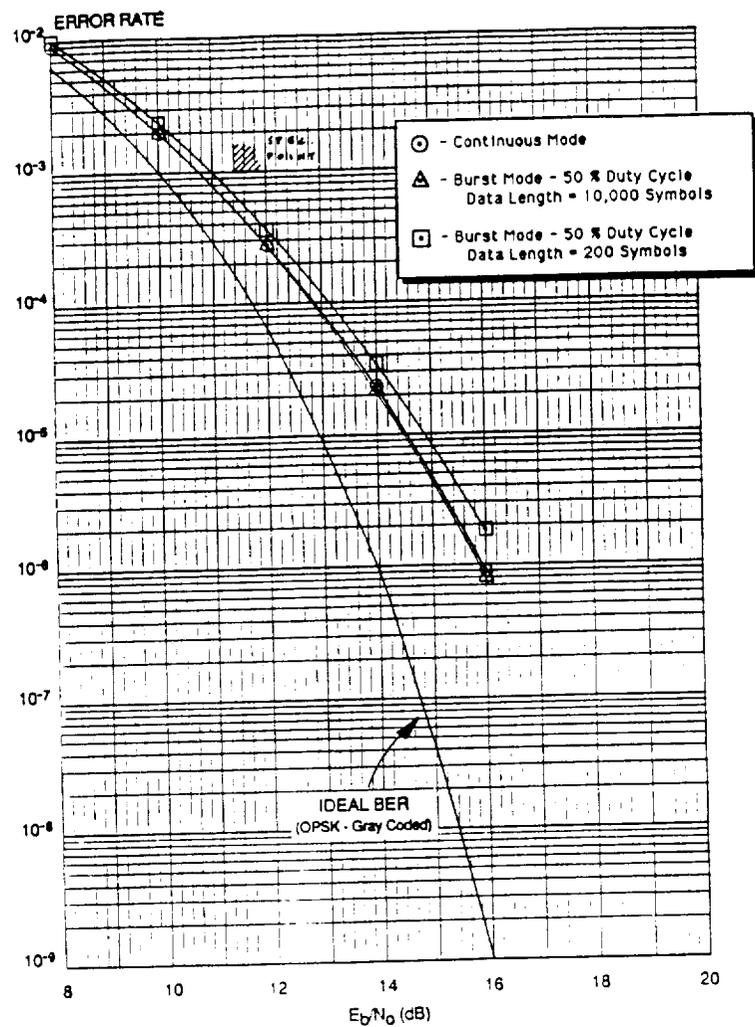
RECEIVE EYE PATTERNS AND PHASE STATE SCATTER DIAGRAM

The top photo below shows one of the two receive eye patterns from the 8-PSK modem. Also shown is the phase state scatter diagram which was obtained using the receive eye pattern test points to drive the horizontal and vertical inputs of a high speed oscilloscope.



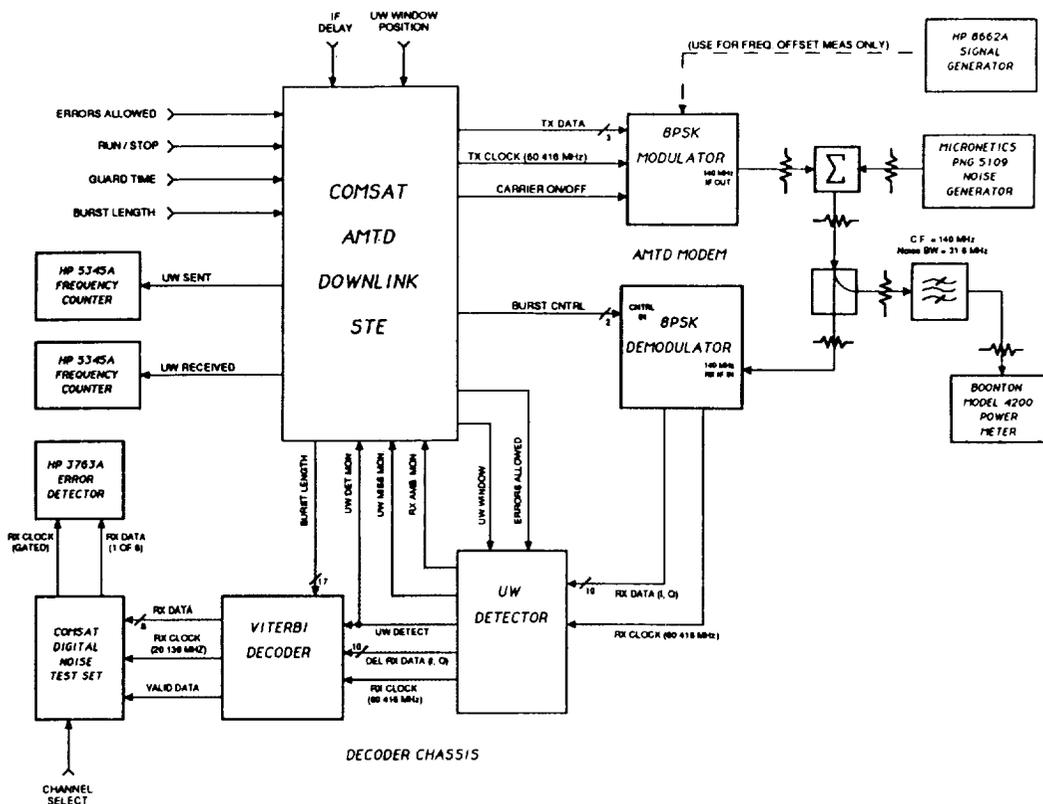
MODEM SELF TEST BER PERFORMANCE

Performance of the modem hard decision BER is shown in the curves plotted below. Data was taken for continuous mode, and burst mode with long and short bursts. Also shown for reference is the 8-PSK ideal performance curve.



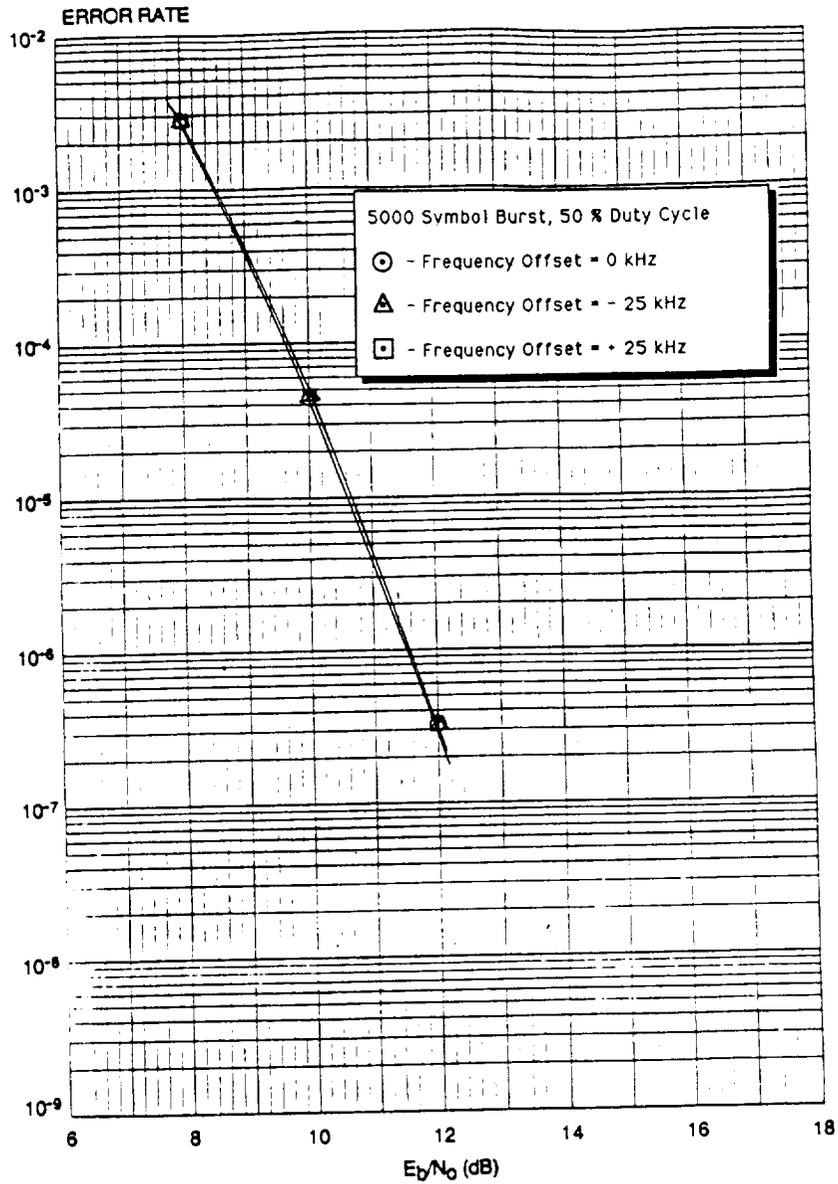
CODED SYSTEM BER AND UW MISS TEST SETUP

Performance of the coded 8-PSK system was measured using the test setup shown below. Data for the eight parallel 20 Mbit/s channels were generated in the STE which also encoded the data. Noise was added at the IF and the C/N was then measured using a separate calibrated filter. BER was measured at the decoder output on one of the eight received channels by the HP BER receiver. The digital noise test set was used for convenience to select which of the channels was to be measured. Unique word misses and bursts transmitted were measured using standard frequency counters for determination of unique word miss rate.



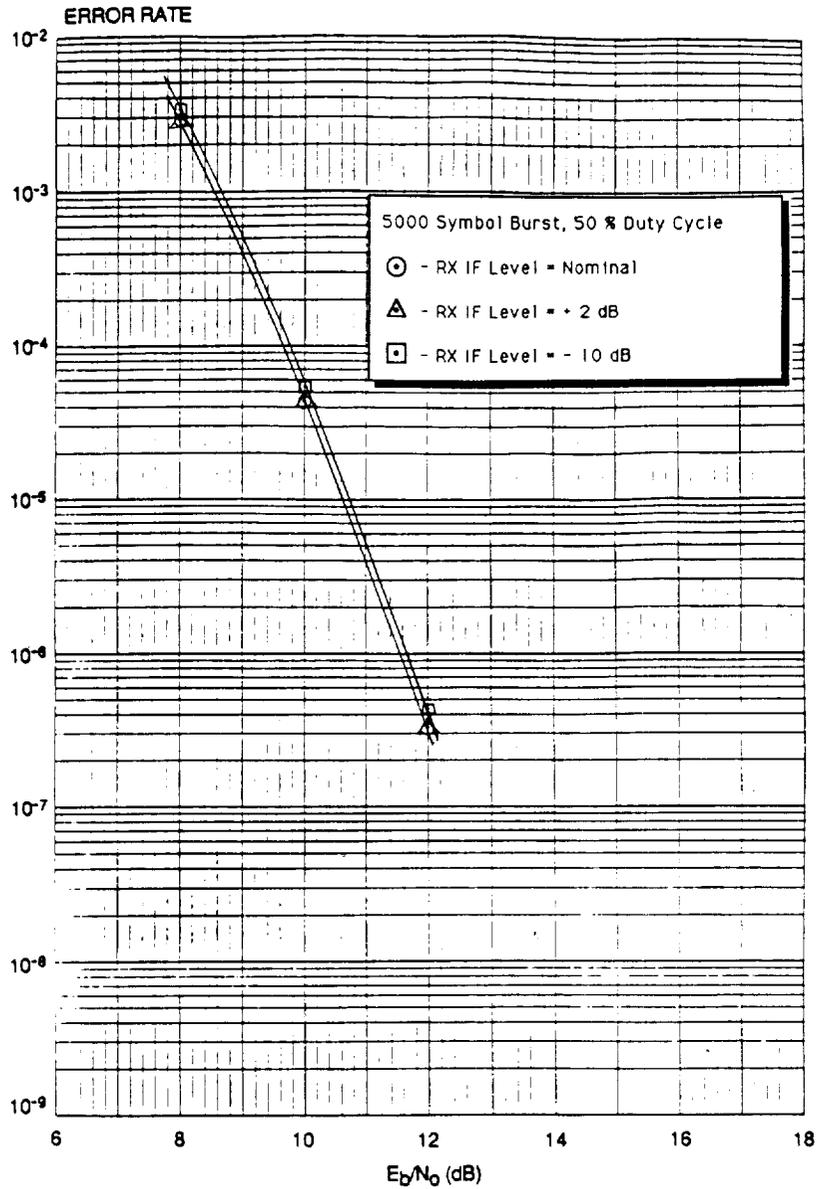
BER vs. E_b/N_0 WITH FREQUENCY OFFSET

BER vs E_b/N_0 Performance of the coded system is shown below for frequency offsets of zero and ± 25 KHz. Frequency offset of the IF signal can result in phase offsets in the carrier recovery loop if left uncorrected.



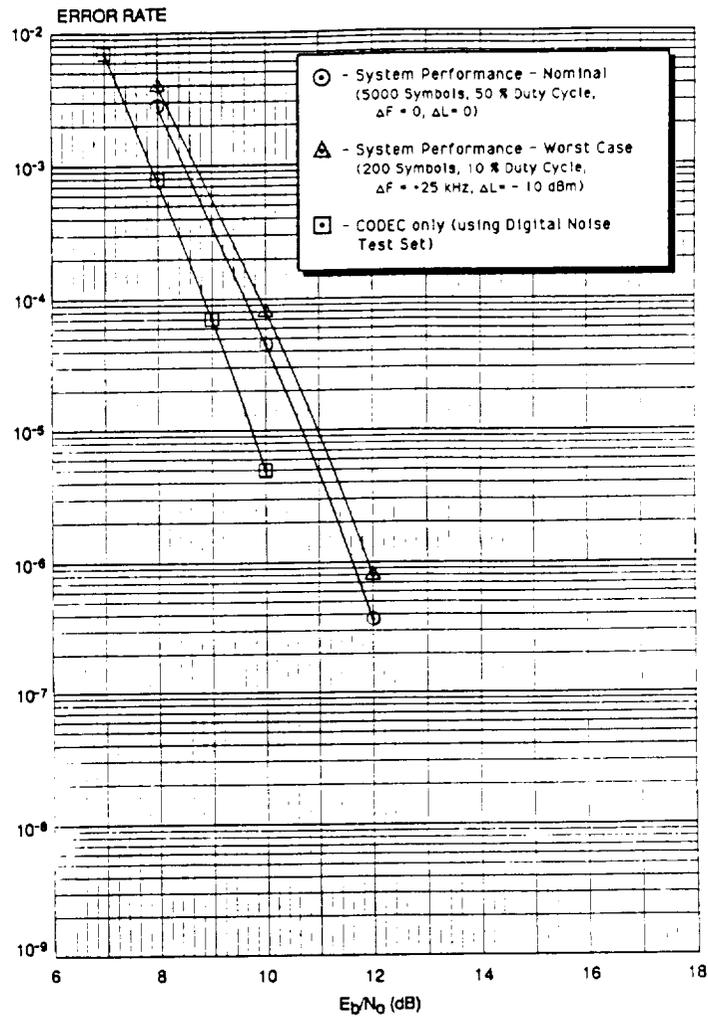
BER vs. E_b/N_0 WITH IF INPUT LEVEL VARIATION

BER vs E_b/N_0 performance of the coded system with input IF level variation over the specification range is shown in the figure below. In general, 8PSK will be more sensitive than QPSK to level variations due to the multilevel nature of the quadrature eye patterns.



CODED SYSTEM BER PERFORMANCE

The curves below illustrate the overall coded system BER vs E_b/N_0 performance in an AWGN channel for nominal and worst case operating conditions. Also shown for comparison is the codec performance data taken using the codec digital noise self test setup. As can be seen from the figure, the modem introduces approximately 1 dB of implementation loss.





N92-22007

CODED 16-CPFSK FOR DOWNLINK APPLICATIONS

Robert Davis
Harris Corporation
Government Systems Sector
Advanced Technology Department
Melbourne, Florida 32901

ABSTRACT

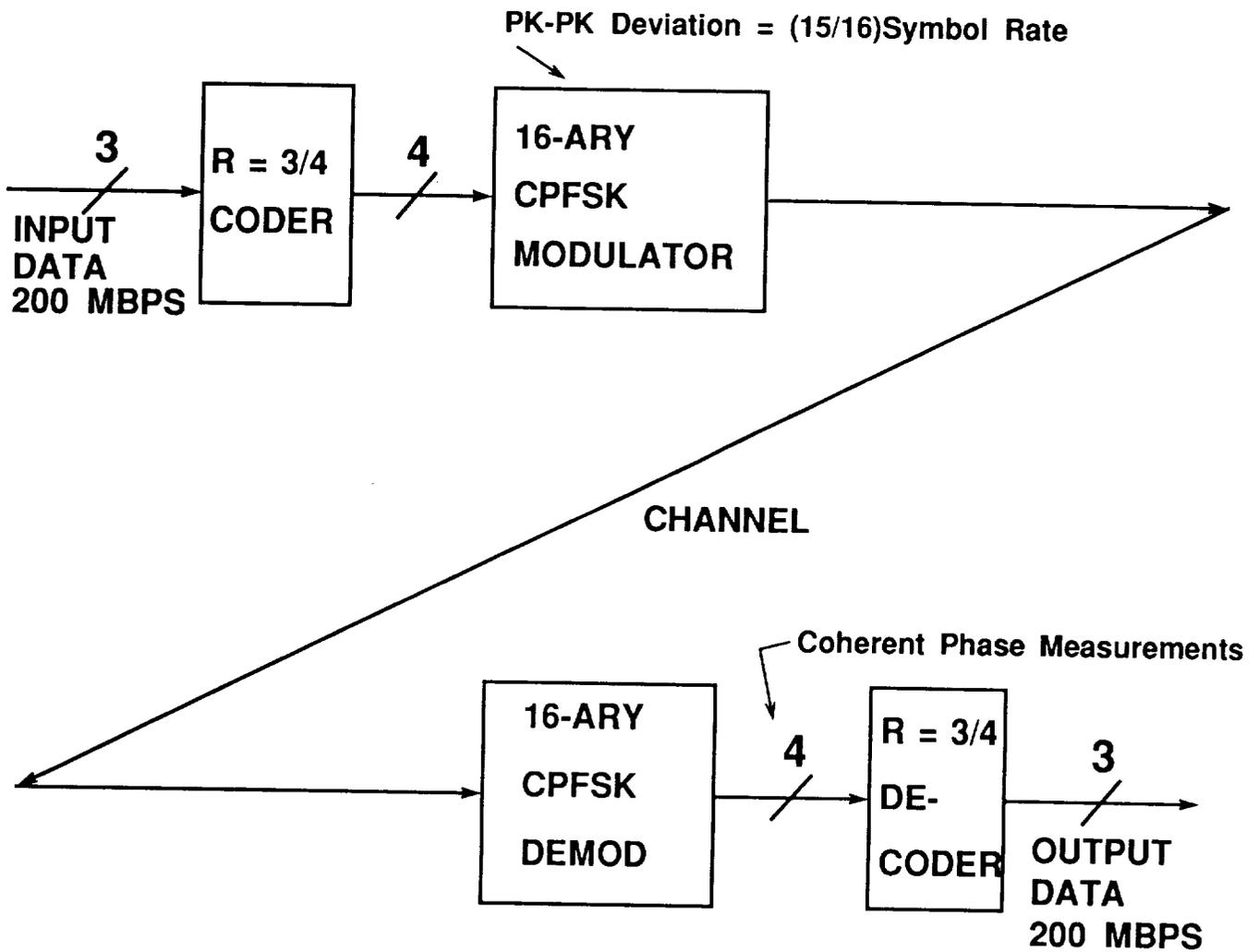
We describe a bandwidth-efficient constant-envelope Proof-of-Concept (POC) modem developed on an Advanced Modulation Techniques Development contract for NASA/Lewis Research Center. The POC modem employs 16-ary Continuous Phase Frequency Shift Keying (16-CPFSK) modulation. The 16 frequencies are spaced every 1/16th baud rate which produces a compact spectrum allowing 2 bits/sec/Hz operation. The modem is designed for 200 mb/s TDMA application with 100 MHz adjacent channel spacing. Overall rate 3/4 convolutional coding is incorporated. The demodulator differs significantly from typical quadrature phase detector approaches in that phase is coherently measured by processing the baseband output of a frequency discriminator. Baud rate phase samples from the baseband processor are subsequently decoded to yield the original data stream. The method of encoding onto the 16-ary symbol-ending phase nodes, together with convolutional coding gain, results in near QPSK theoretical performance. The modulated signal is of constant envelope; thus the power amplifier can be saturated for peak performance. The spectrum is inherently bandlimited and requires no RF filter for sidelobe containment. Two novel theoretical techniques are used in this 16-CPFSK modem: I) Coherent phase measurements are obtained by processing an FM discriminator baseband output; II) Modulation is accomplished via a closed-loop-linearized VCO.

*Work performed for NASA/Lewis Research Center on Contract NAS3-24681

BASIC BLOCK DIAGRAM OF MODEM

This figure shows a very basic level block diagram for the 200 Mbps TDMA modem Proof-of-Concept modem investigated by Harris Corporation on the Advanced Modulation Technology Development contract with NASA/Lewis Research Center.

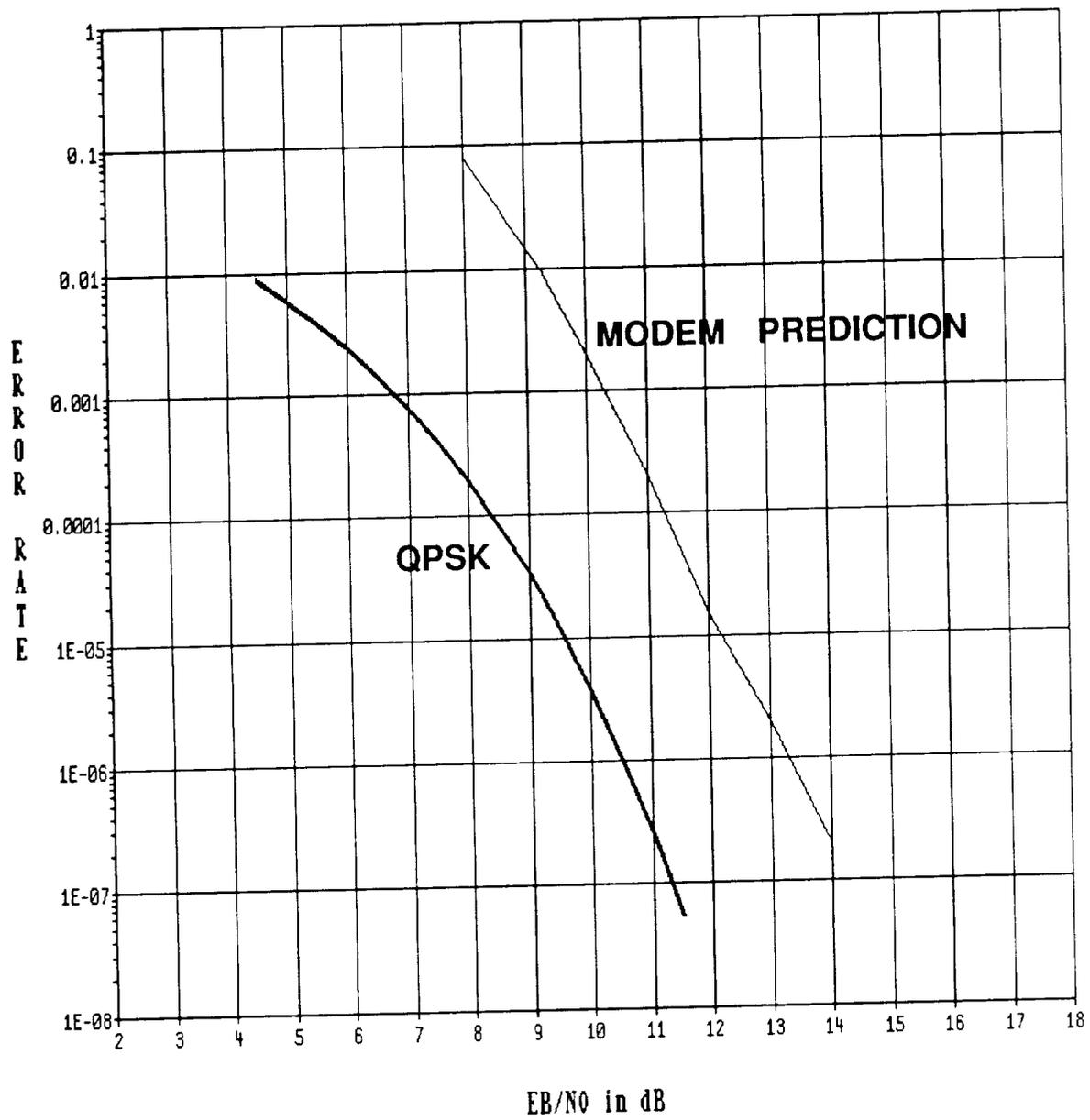
BASIC MODEM BLOCK DIAGRAM



MODEM ERROR RATE PERFORMANCE

The figure shows the Bit Error Rate Performance predicted for the Harris TDMA Modem compared to QPSK performance.

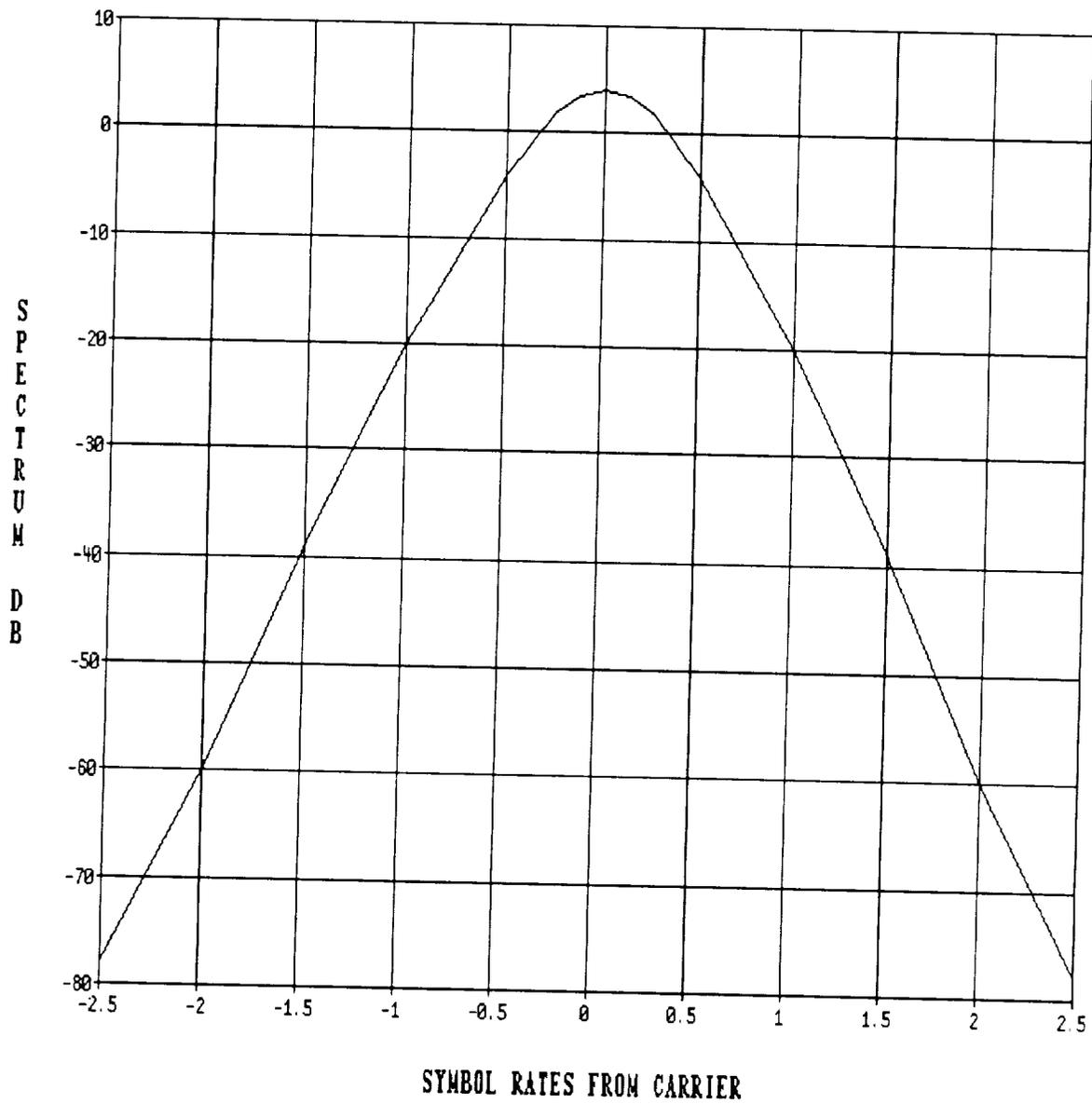
PERFORMANCE OF 16-CPFSK



MODEM SPECTRUM

Here is the spectrum for the Harris 200 Mbps TDMA Modem. The symbol rate is 72.73 MHz.

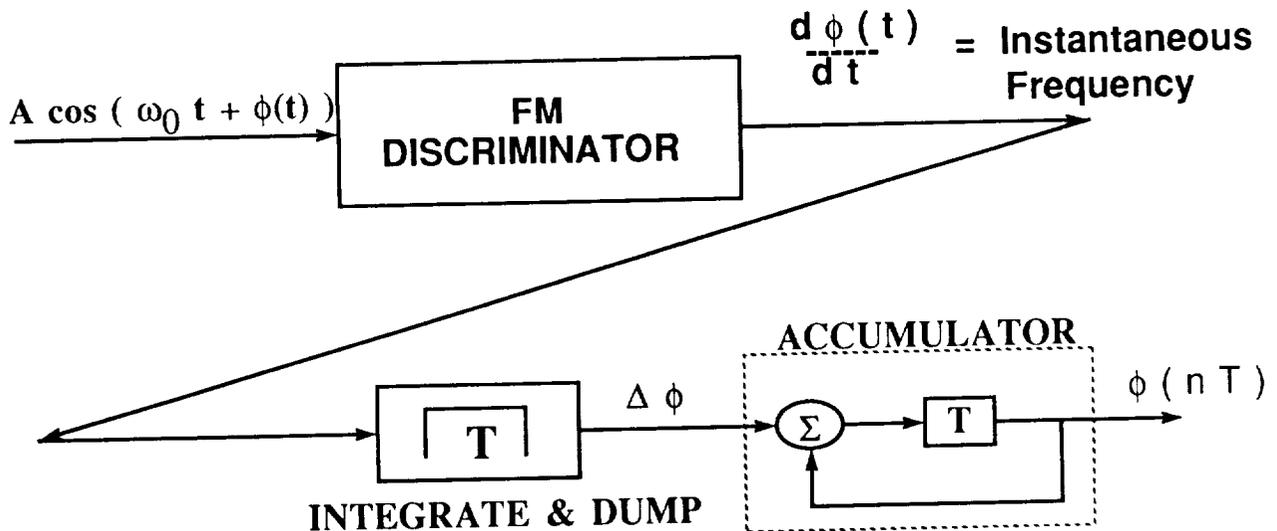
SPECTRUM OF BASEBAND FILTERED 16-CPFSK



OBTAINING COHERENT PHASE FROM A DISCRIMINATOR.

A discriminator outputs $\phi'(t)$ where $\phi(t)$ is the signal's phase modulation. Integration of $\phi'(t)$ recovers the desired signal, $\phi(t)$. Implementation of the integration has several practical problems: 1) Integrator output can grow without bound; 2) Initial phase, $\phi(0)$, must be determined; 3) AGC is needed on the baseband signal. Regarding problem 1), fortunately, we need only know phase Mod- 2π . Thus the growth problem is avoided by integrating Mod- 2π . How can such an integrator be implemented? It is essential only that we obtain $\phi(nT)$, phase at baud time intervals. An integrator yielding $\phi(nT)$ can be implemented as a T-interval Integrate-and-Dump (I&D) sampled by an A/D which feeds a digital accumulator that rolls over Mod- 2π . The I&D is actually a lowpass Half-Nyquist filter in this modem, but the conceptual picture remains useful.

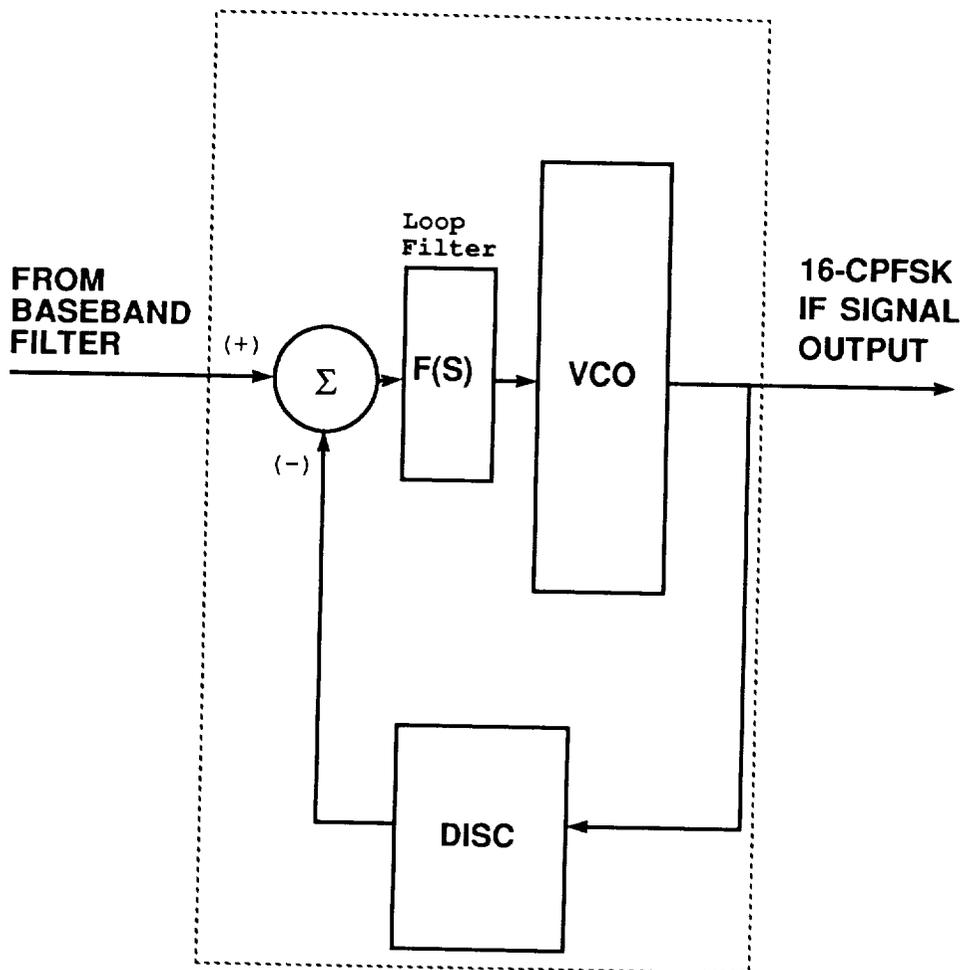
Problem 2)--acquiring initial unknown phase, $\phi(0)$, is handled by first observing for each baud time, the phase error to the closest one of the 16-CPFSK phase nodes (Mod- 2π) equally spaced in the accumulator. This phase error is filtered by a lowpass loop filter whose output is subtracted from the accumulator input. The initial phase error, $\phi(0)$, appears as a DC component of the error and is eliminated by the baseband loop. Frequency offset (DC offset from the discriminator) also is eliminated by this baseband loop, the equations for which are identical to those for a PLL.



LINEARIZED VCO MODULATOR

The figure below shows the closed-loop-linearized VCO modulator. The baseband filter output is applied through a feedback summer to the VCO. $F(s)$ is a wideband loop filter. The output of the VCO is immediately converted back to baseband by the discriminator (DISC) and subtracted from the baseband input modulating signal to generate a correction signal in the closed loop. The VCO is thus modulated with small error between the baseband modulating signal and the output of the DISC. If the modulator DISC is identical to the demod DISC, this modulator linearizes the baseband signal path through the modem's VCO/DISC combination.

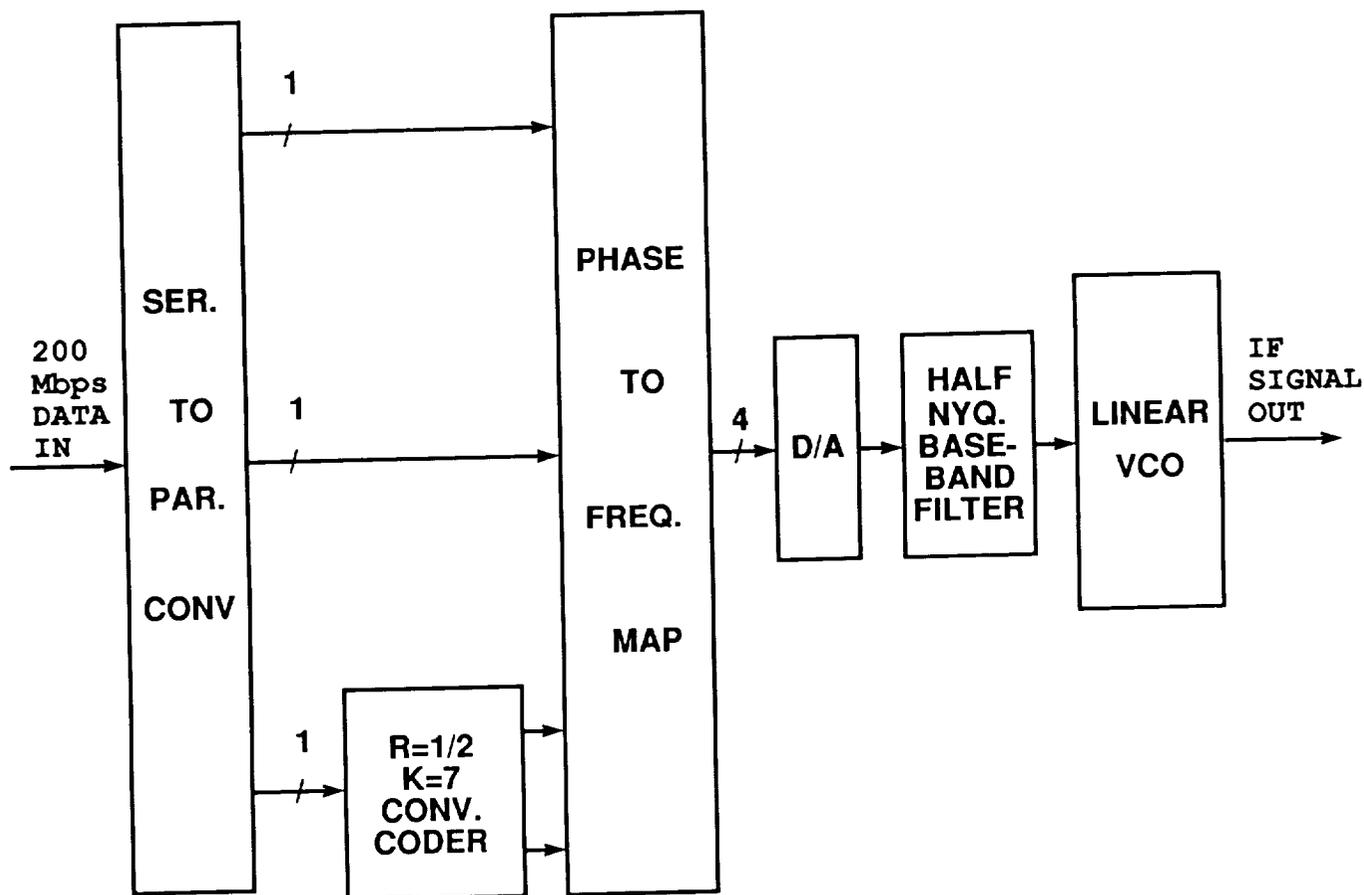
LINEARIZED VCO



BRIEF DESCRIPTION OF MODULATOR OPERATION

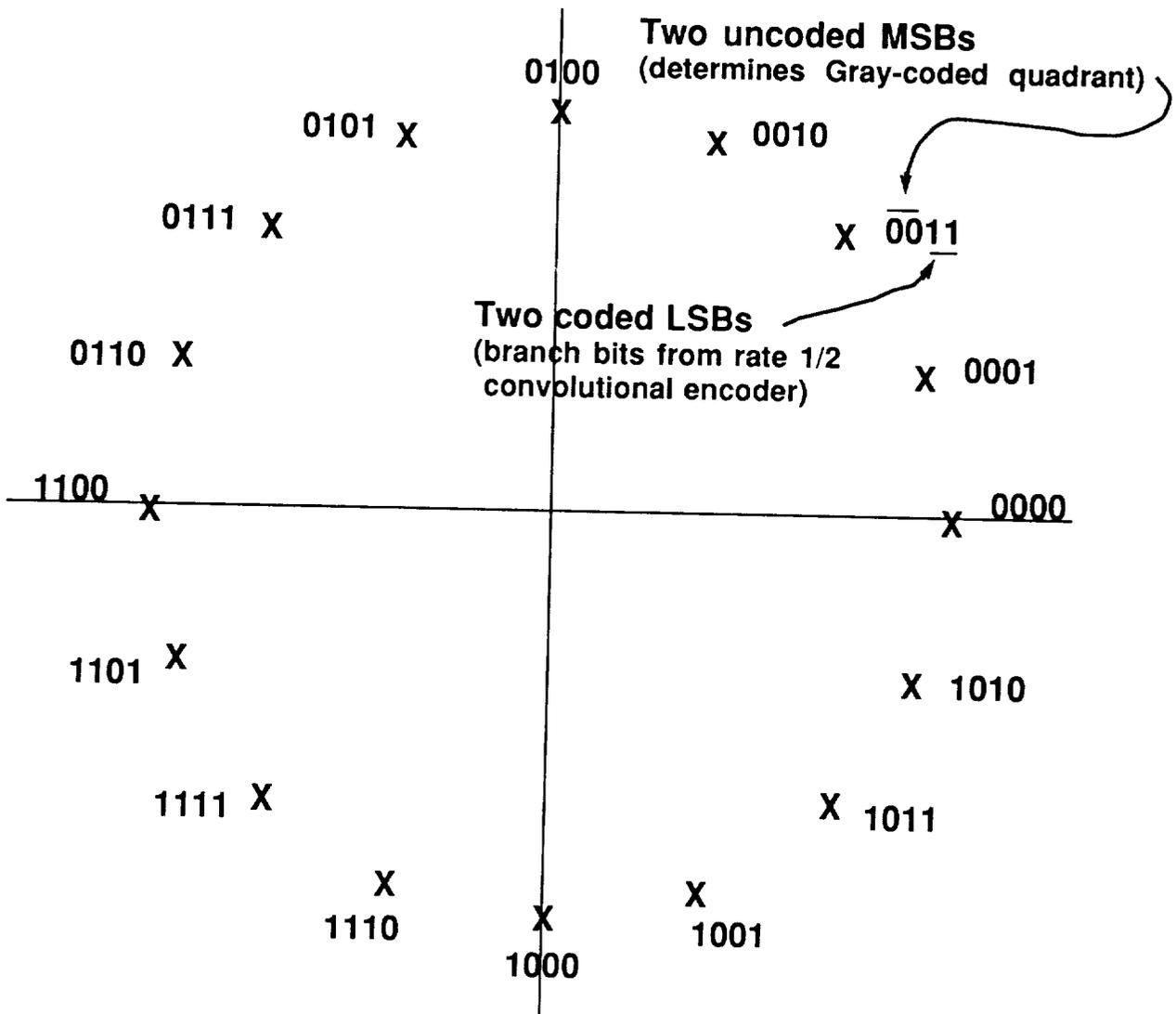
As shown in the figure below, incoming data is split into 3 parallel bit streams. The 2 MSBs are passed unaltered to modulator MSB positions. The LSB bit stream is coded by a rate 1/2, K=7 convolutional encoder. The 2 resulting coded branch bits go to the 2 LSB positions of the modulator. The 4 bits produced by this encoding process specify one of 16 symbol-ending phases ($\text{Mod}-2\pi$) from the 16-CPFSK modulator. Half-Nyquist filtering is employed at the VCO baseband on 16-ary impulses to produce the IF signal at the modulator.

BASIC MODULATOR BLOCK DIAGRAM



16-CPFSK PHASE NODES AND CODING STRATEGY

The figure below shows the 16-CPFSK symbol-ending phase nodes, along with the mapping of coded 4-bit groups onto them. Any set of 4 adjacent phases contains all 4 rate 1/2 code branches and has good distance structure. This fact forms the basis for our decoding strategy, which is: (1) Retain only the 4 phase nodes nearest the received coherent phase measurement; (2) then let the Viterbi decoder determine which of these 4 phases is most likely to have been transmitted; (3) The 2 modulator MSBs (which we call "tagalong bits") associated with the decoder's decision are output as 2 of the decoded bits; (4) The third bit decision is the data bit decision made by the decoder. These 3 bits form the total output data bit stream.

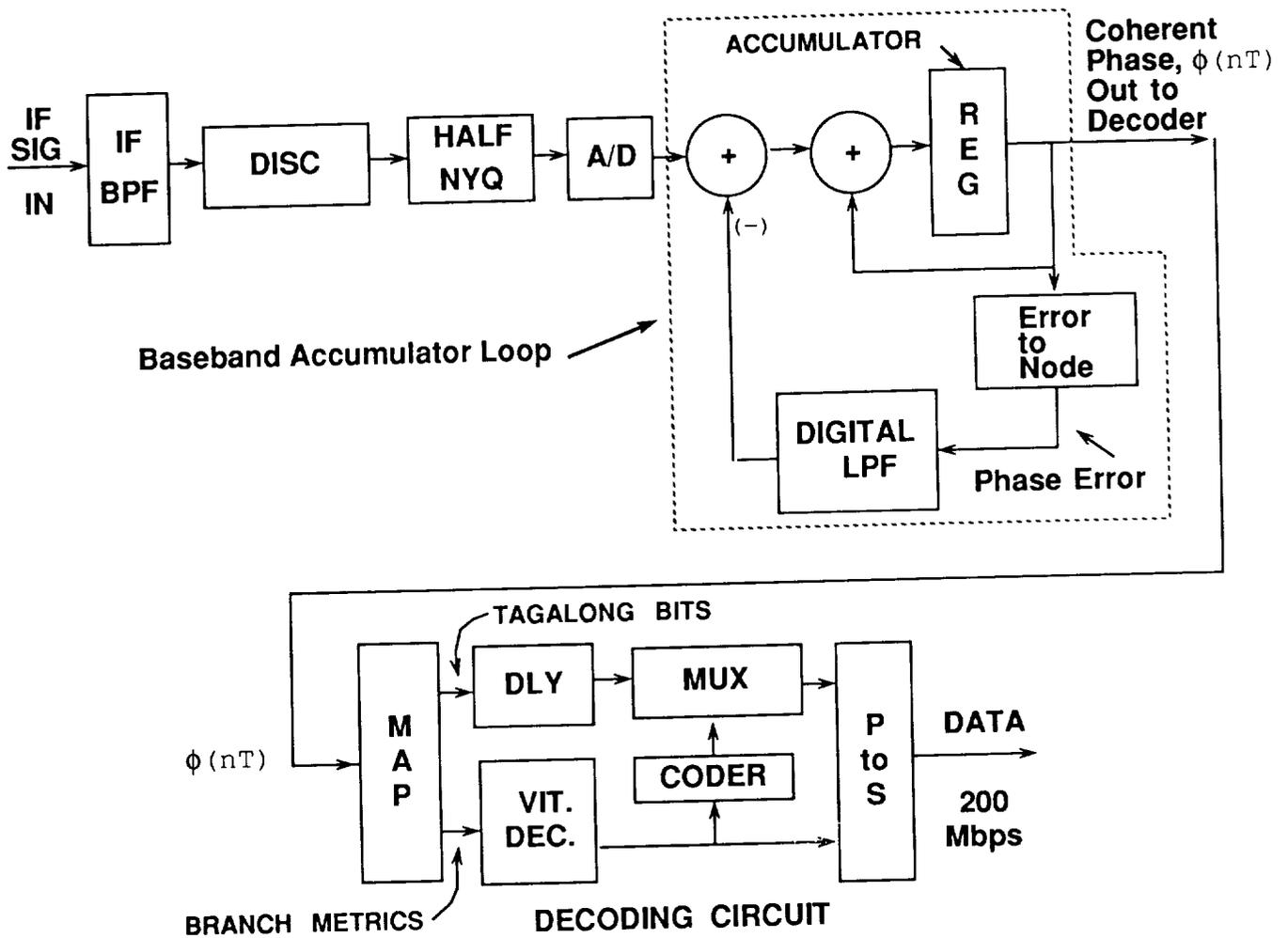


16-CPFSK ENDING PHASES

BRIEF DESCRIPTION OF DEMODULATOR OPERATION

At the demod the IF signal is filtered and passed to the discriminator (DISC). The DISC baseband signal is Half-Nyquist filtered and sampled at symbol rate by an 8-bit A/D. The Half-Nyquist filter completes shaping begun at the VCO, producing an overall Nyquist response to 16-ary impulses from VCO baseband to discriminator baseband. The A/D samples feed the accumulator, whose output is $\phi(nT)$. These coherent measured phase samples feed a Viterbi decoder for demodulation of the original 3 data streams.

BASIC DEMODULATOR BLOCK DIAGRAM



IMPLEMENTATION PROBLEMS

BASEBAND NOISE SOURCES:

Baseband noise sources must be carefully controlled. The A/D Converter's quantizing noise is 42 dB below signal power. To keep other sources of broadband noise small relative to this irreducible quantizing noise, the baseband SNR needs to be 50 dB or greater. At present, our Signal Combiner chassis is a source of unacceptably high levels of broadband noise. We currently are bypassing the Signal Combiner to isolate other problems.

BASEBAND NONLINEAR DISTORTION:

The nonlinearity from VCO baseband input to Discriminator baseband output needs to be 1% or less. For a cubic nonlinearity, this translates to a requirement that Third Order Intermod Distortion (IMD), as measured by a two-tone test, be at least 45 dB down relative to the desired tones. This is difficult to achieve. At one time we had achieved these levels of IMD. After buttoning up some of the equipment into the chassis, the IMD levels rose to 30 to 35 dB down. At this writing we believe we have discovered the source of this problem and we are working to remove it. We believe that this totally unacceptable level of IMD is a major source of our 5×10^{-3} irreducible error rate.

BASEBAND LINEAR DISTORTION:

With the 16-ary modulation used on this modem, the linear amplitude and group delay distortions must be carefully controlled. By careful adjustments of the baseband filters, we believe this source of difficulty has been largely controlled. The amplitude response is flat to within 0.1 to 0.2 dB and group delay distortion is less than 1 nsec out to the Nyquist band edge.

SUMMARY:

We believe that the major problem we currently are fighting in removing our 5×10^{-3} error floor is the baseband nonlinearity problem. At one time we had this parameter under control -- having produced -45 dB IMD. Our currently observed -30 to -35 dB IMD is totally unacceptable and we believe we will reduce this again to acceptable levels shortly.

SESSION III

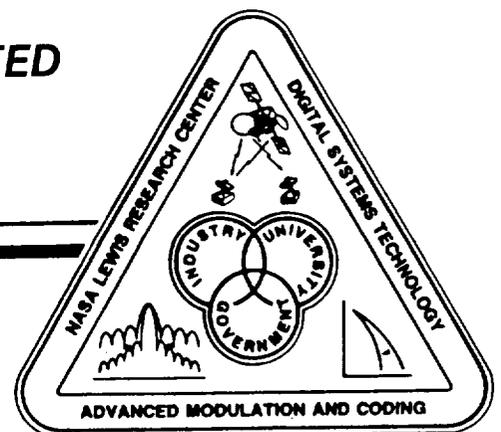
**OTHER LEWIS MODULATION AND
CODING WORK
CHAIR: J.M. BUDINGER**

**HIGH SPEED HARDWARE DEVELOPMENT FOR
FDMA/TDM SYSTEM
S.C. KWATRA, M.M. JAMALI
UNIVERSITY OF TOLEDO**

**A CO-DESIGNED EQUALIZATION, MODULATION
AND CODING SCHEME
R.E. PEILE
UNIVERSITY OF SOUTHERN CALIFORNIA**

**MODULATION TECHNIQUES FOR POWER AND SPECTRALLY
EFFICIENT SATCOM SYSTEMS
K. FEHER
UNIVERSITY OF CALIFORNIA**

**PROGRAMMABLE RATE MODEM UTILIZING DIGITAL
SIGNAL PROCESSING TECHNIQUES
A. NAVEH
TIW SYSTEMS, INCORPORATED**



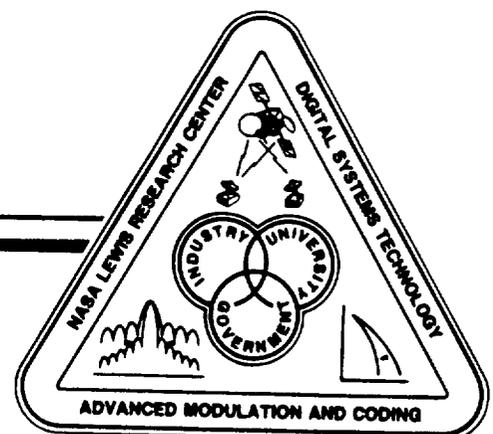
SESSION III CONTINUED

**MULTI-USER SATELLITE COMMUNICATIONS SYSTEM
USING AN INNOVATIVE COMPRESSIVE RECEIVER**

**E.J. STAPLES
AMERASIA TECHNOLOGY, INCORPORATED**

**FLEXIBLE HIGH SPEED CODEC
R.W. BOYD AND W.F. HARTMAN
HARRIS CORPORATION**

**PROGRAMMABLE DIGITAL MODEM
M. KAPPES
COMSAT LABORATORIES**



HIGH SPEED HARDWARE DEVELOPMENT FOR FDMA/TDM SYSTEM

S. C. Kwatra, M. M. Jamali
Department of Electrical Engineering
The University of Toledo
Toledo, Ohio 43606

Abstract

In satellite communications systems incorporating small earth stations, the application of multiple-access techniques of single channel per carrier/frequency division multiple access (SCPC/FDMA) in the uplink, on-board switching and time division multiplexing (TDM) in the downlink is significantly effective in improving satellite transponder utilization and reducing the required effective isotropic radiated power (EIRP) in both the earth stations and the satellite. A conceptual block diagram of the multicarrier demodulator is shown in Figure 1.

For FDMA/TDM conversion, the uniformly spaced FDMA channels have to be separated which can be accomplished with a transmultiplexor. After separating these channels, they are demodulated using a QPSK demodulator. The transmultiplexor is implemented with the aid of a commutator, bank of polyphase filters and discrete Fourier transform (DFT) implemented via FFT.

Development and advances in the area of VLSI and digital systems can be exploited for the development of a transmultiplexor and QPSK demodulator. Goals for designing the architecture for the transmultiplexor and QPSK demodulator are that the system should meet real time signal processing requirements of the future satellite systems and should consume very small amount of power. In this work we design the architecture of this transmultiplexor and the demodulator by pipelining all the modules namely commutator, filter bank FFT and the internal modules of the QPSK. The architecture is designed for the case of 800 channels each having a bandwidth of 45 KHz and a bit rate of 64 Kb/s. In this case each module will have $(1/45 \text{ KHz} = 22.22 \text{ micro seconds})$ 22.22 micro seconds to complete computation.

This research is partly supported by NASA grant NAG3-799 and NAG3-865.

A uniform channel filter bank consists of a polyphase filter bank, phase shifter, DFT block and multiplication by a constant. This uniform filter bank is shown in Figure 2. The polyphase filter bank will require 800 9 tap FIR filters and a 1024 point FFT operation.

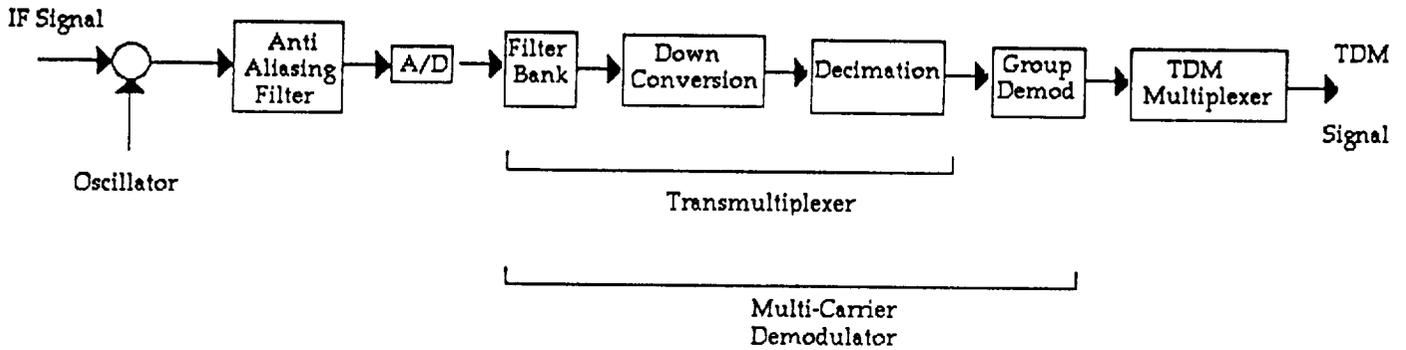


Figure :1 SYSTEM FOR FDMA/TDM CONEVRSION

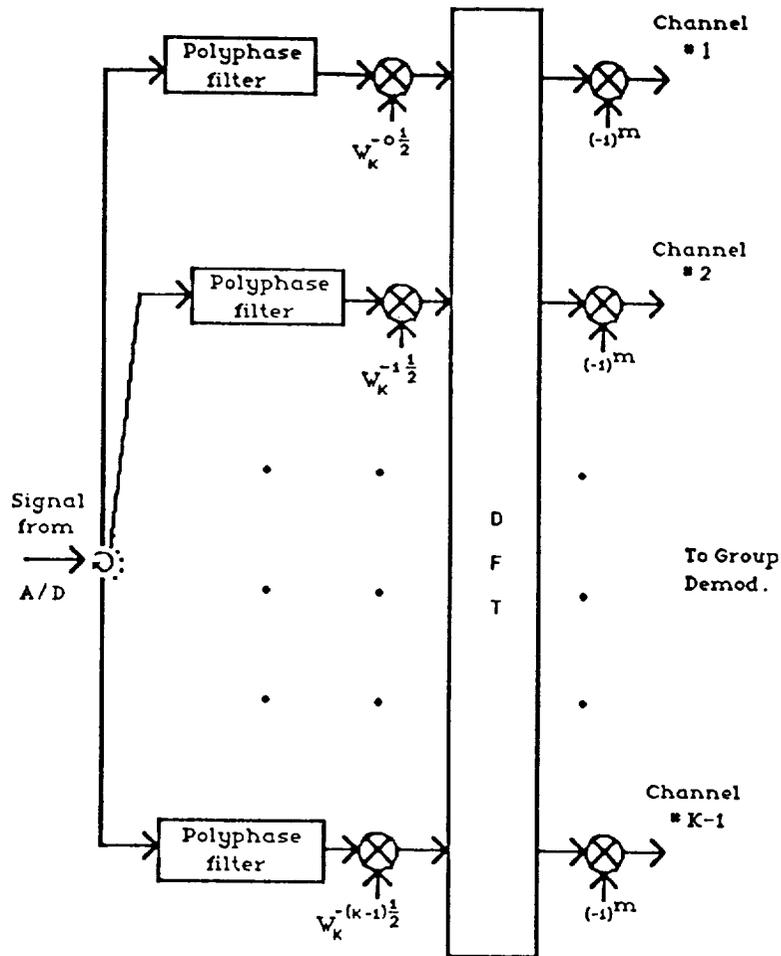


Figure 2: Uniform Channel Filter Bank

Filter banks can be implemented using 800 different 9 tap FIR filters. The amount of required hardware will be prohibitive for our application because of size and power requirements. A multiplexed 9 tap FIR filter architecture has been designed which will meet the speed requirements. This structure utilizes RAM's to store data and tree structure for multiplication and add operations as shown in Figure 3.

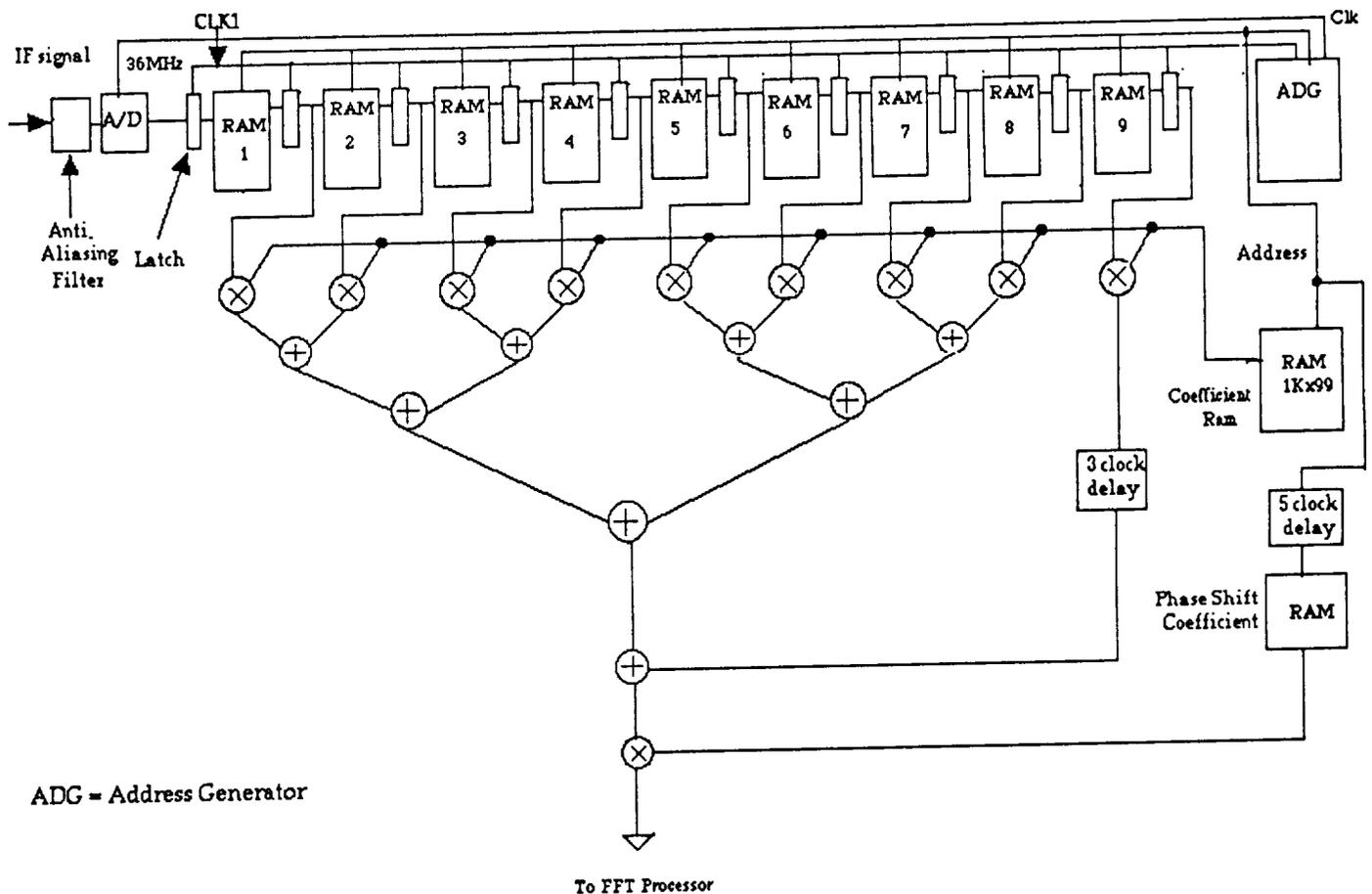


Figure 3: Shared Filter Architecture

In order to meet the speed requirements of this system, a pipelined FFT structure has been designed. This structure has 10 stages with dual memories in between the stages. It is capable of performing 1024 point complex FFT in 22.22 microseconds which is the pipeline speed of this system. The structure is shown in Figure 4.

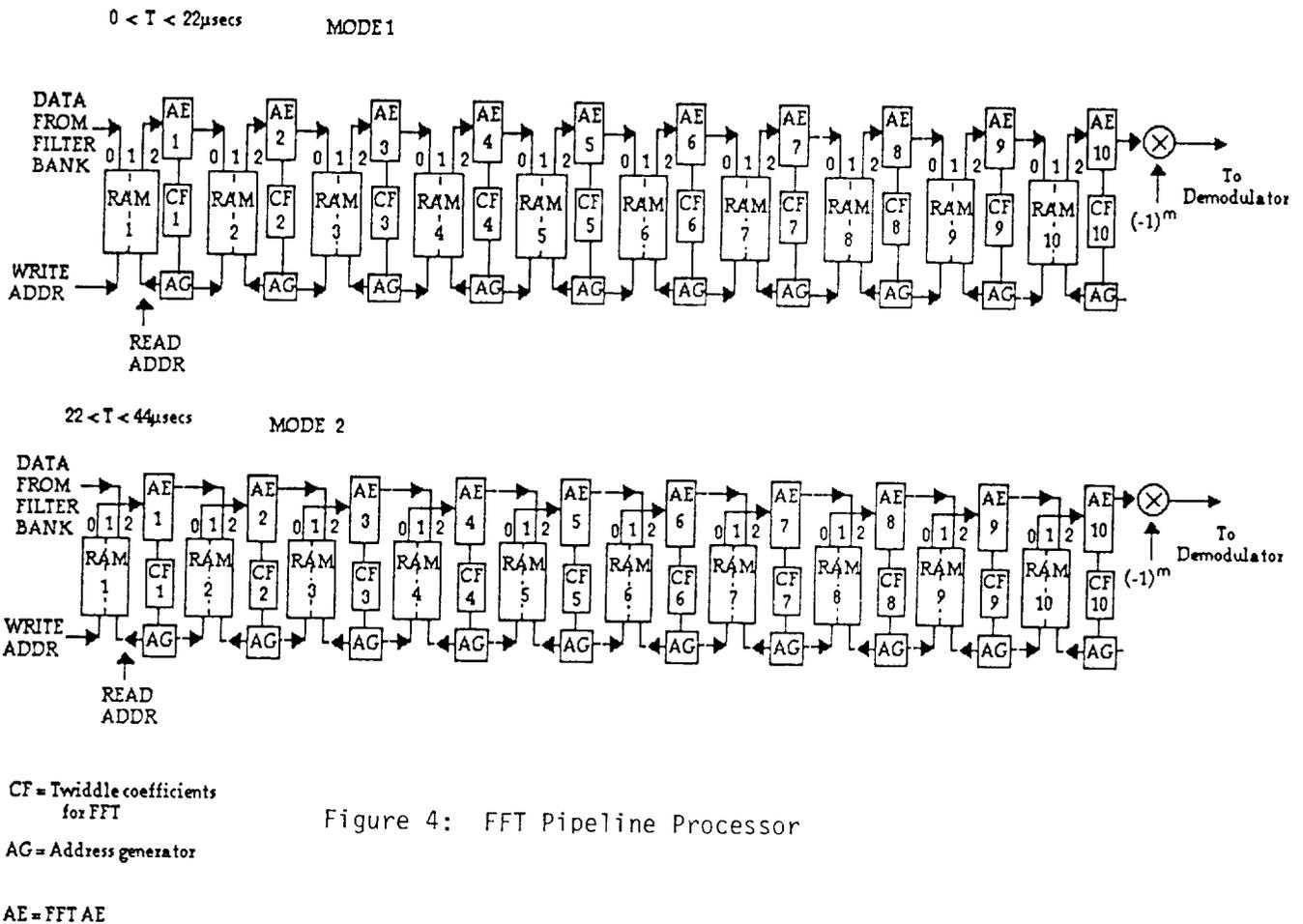
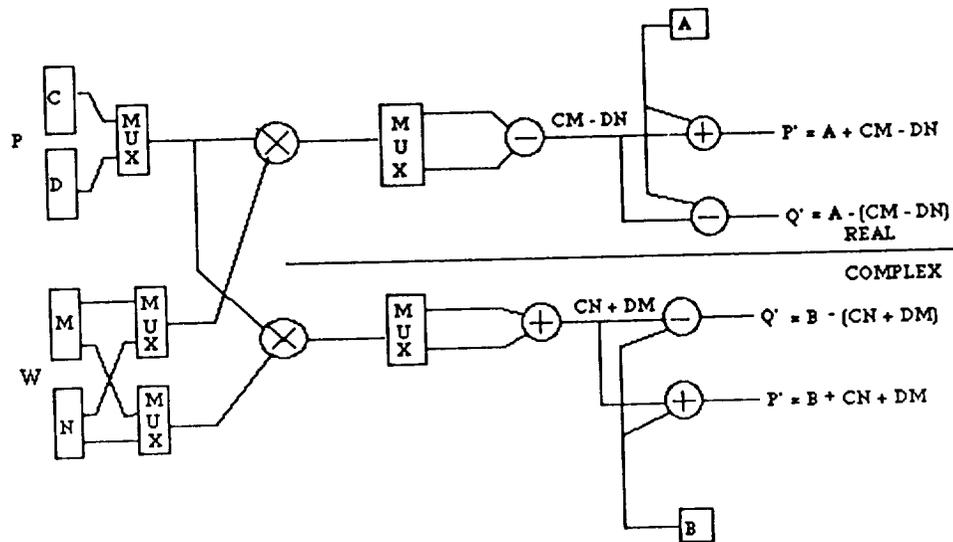


Figure 4: FFT Pipeline Processor

A FFT multiplexed butterfly arithmetic element has also been designed and is shown in Figure 5. The data flow through this arithmetic element moves according to specified pipeline speed. This element also performs parallel arithmetic operations.



In Place Radix 2 butterfly where
 $P = C + jD$
 $Q = A + jB$
 $W = M + jN$

Figure 5: FFT Muxed Butterfly Arithmetic Element (MAE)

A TDMA frame consists of guard bits, preamble, unique word and data bits. The demodulator has to process the preamble, unique word and data bits to recover the message. A block diagram of a QPSK demodulator is shown in Figure 6.

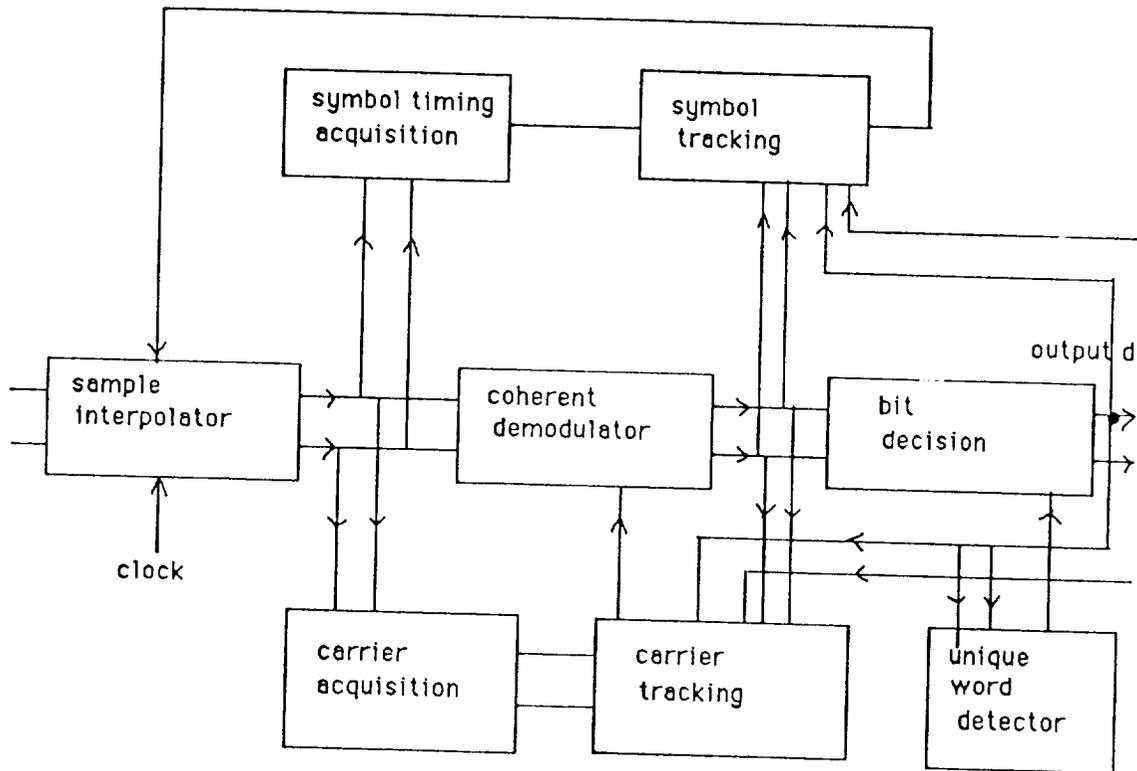
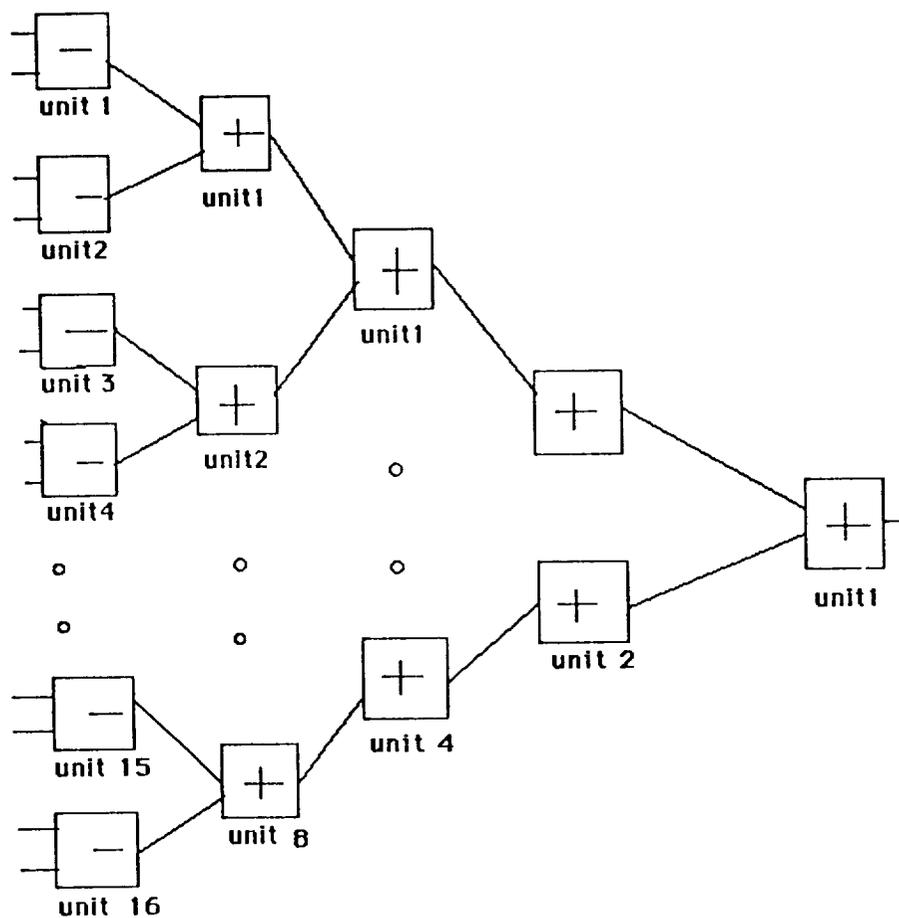


Figure 6: QPSK Demodulator

Preamble processing involves the carrier acquisition and timing acquisition modules. A tree structure based module has been designed for the preamble processing which computes the carrier phase and symbol timing. The hardware structures for various demodulator modules are shown in Figures 7 to 11.



Initial block of the preamble

The input to the subtractor units are the sample values.

Figure 7

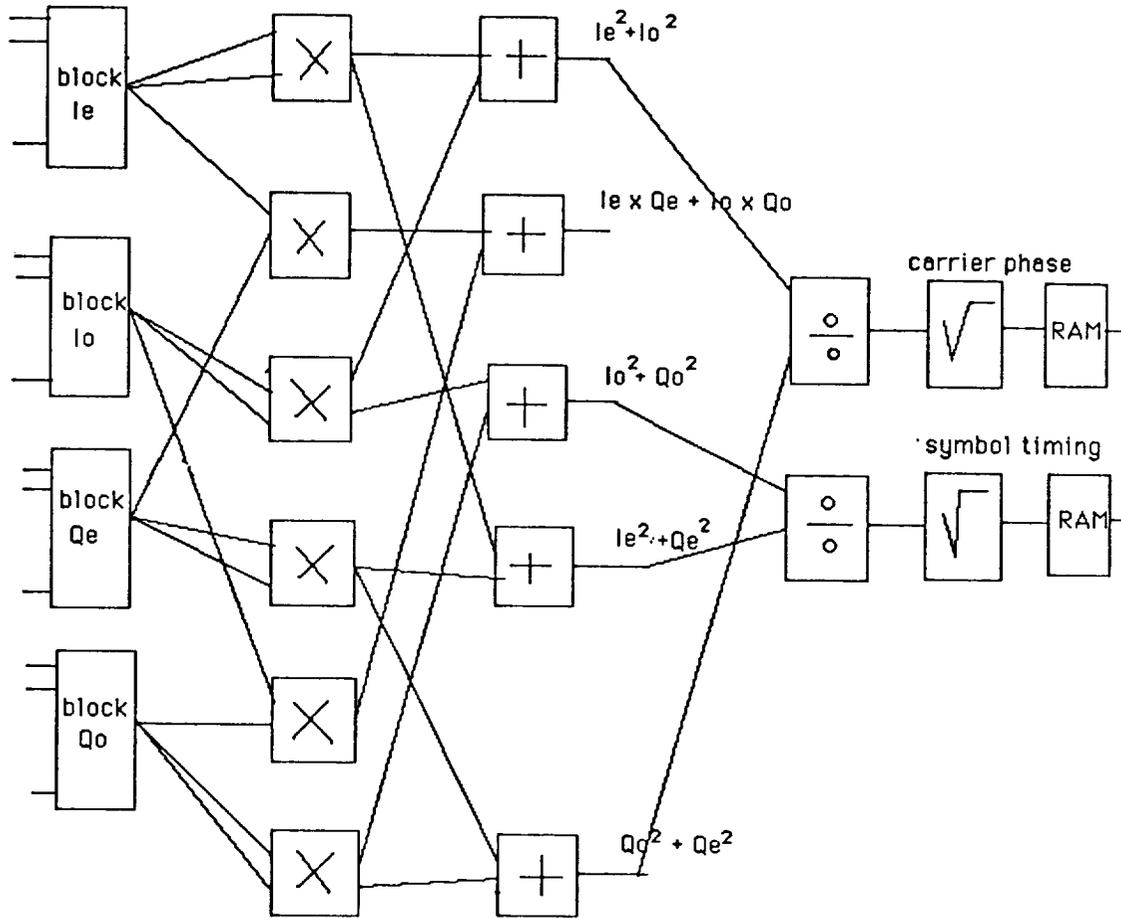
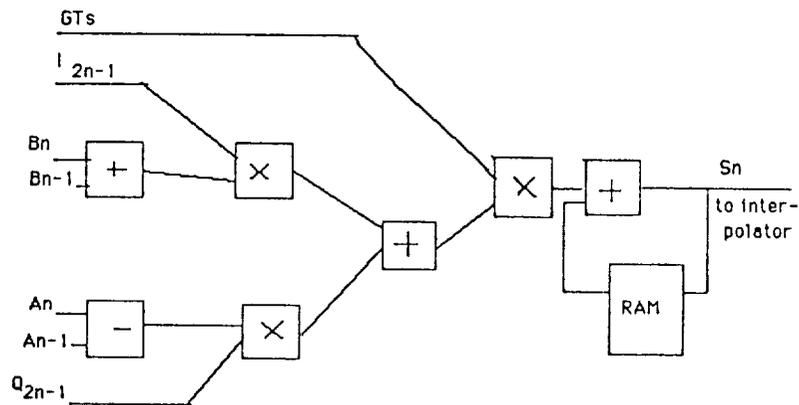
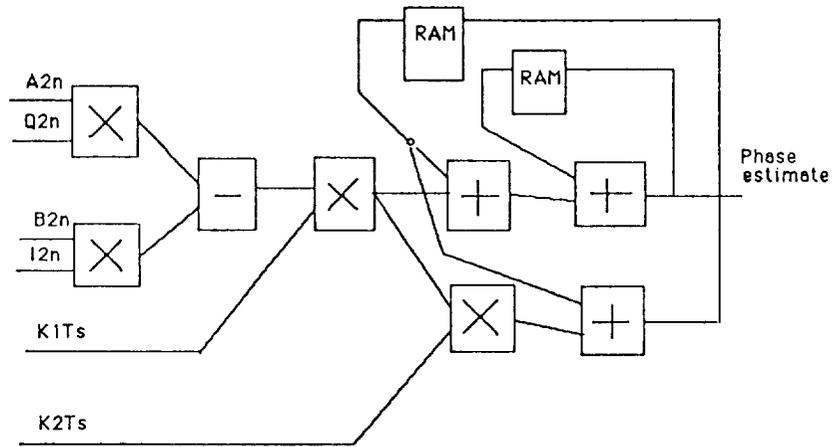


Figure 8: Preamble Module Units



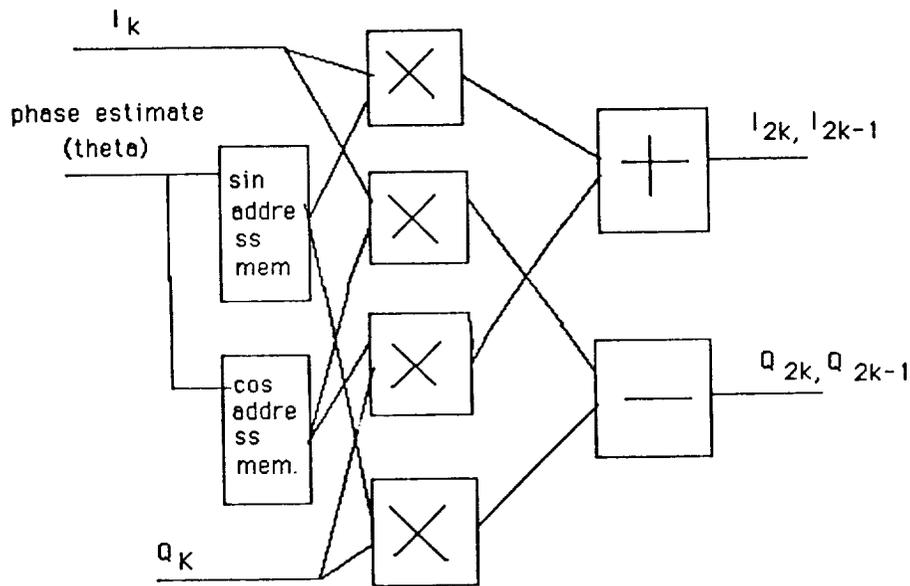
I_{2n-1}, Q_{2n-1} are odd numbered samples from the coherent demodulator
 $A_n, A_{n-1}, B_n, B_{n-1}$ are the bit decision outputs
 S_n is the output from the the module which is used by the sampling clock

Figure 9: Symbol Timing Tracking Module



A_n, B_n are outputs of bit-decision module
 $K1Ts, K2Ts$ are the gain values of the loop
 X_{2n}, Y_{2n} are even samples output from the coherent demodulator

Figure 10. Carrier Tracking Module



I_k, Q_k are the outputs from the interpolator
 Phase estimate is the output from the carrier tracking
 The output samples are used by the bit decision, timing tracking & carrier tracking.
 Even numbered samples are used by the bit-decision & carrier tracking ; odd numbered by the timing tracking.

Figure 11: Coherent Demodulator

REFERENCES

- 1) S.C. Kwatra, R. Bexten, "Analysis and design of a burst mode digital demodulator implemented using a digital signal processor," University of Toledo, Rep DTVI-22, Dec 1988.
- 2) S.J. Campanella, S. Sayegh, "Onboard multichannel demultiplexer/demodulator," NASA contract No. cr1801827, 1987
- 3) M. Morikura, K. Enamoto, S. Kato, "High speed onboard digital signal processing and LSI implementation," GLOBECOM 1988, Section 16, pp493-498.
- 4) B.W. Smith, H.J. Siegel, "Models for use in the design of macro-pipelined parallel processors," IEEE Journal on computer architecture, 1985, pp116-123.
- 5) F. Guibaly, B. McKinney, "A flexible pipeline architecture for digital signal processors," IEEE conference Communications, Computers, Signal processing, 1987, pp370-373.
- 6) S. Kato, K. Ohtani, T. Kohri, M. Morikura, M. Umehira, S. Kubota, "Onboard digital signal processing technologies for present and future SCPC systems," International Journal of Satellite Communications (IJSC), Vol 6, pp 289-300, 1988.
- 7) E.D. Re, R. Fantacci, "Alternatives for onboard digital multicarrier demodulation," IJSC, Vol 6, pp267-281, 1988.
- 8) A. Thanawala, "FDMA/TDM conversion for non contiguous channels," M.S Thesis, University of Toledo, 1989.
- 9) B.G. Evans, F.P. Coakley, "Multi Carrier Demodulators for OBP satellites," IJSC, Vol 6, pp243-251, 1988.
- 10) R. Crochiere, L. Rabiner, "Multirate signal processing," Prentice-Hall, 1983.
- 11) G. Perrota, G. Losquadro, "FDMA/TDM satellite communication systems for domestic/business services," Proceedings of International conference on digital satellite communication (ICDSC) -7, pp155-162, 1986.
- 12) N.R. Powell, "Signal processing with bit serial word parallel architectures," Proceedings SPIE "Real-Time signal processing" Vol 154, pp 98-104, Aug 28-29 1988.
- 13) G. Luikuo, "A 500 MOPS DSP chip set," Electronic Engineering supplement, pp 109-113, June 1988.

A CO-DESIGNED EQUALIZATION, MODULATION AND CODING SCHEME¹

Robert E. Peile
 University of Southern California
 Los Angeles, CA 90089-0272

1) Outline

This article reports on work being performed under a Nasa-Lewis Research grant (No. NAG3-982) into a scheme that attempts to combine the advantages of certain coding, modulation and equalization techniques in order to remedy well-known disadvantages with the individual techniques. The work should be seen in the context of much of the recent research and progress made in the bandlimited channel over the last ten years. The commercial impact and technical success of Trellis Coded Modulation seems to illustrate that, if Shannon's capacity is going to be neared, the modulation and coding of an analogue signal ought to be viewed as an integrated process. More recent work, including this project, has tried to press beyond the gains obtained for Average White Gaussian Noise and combine the coding/modulation in with adaptive equalization. The motive is to gain similar advances on less perfect or idealized channels.

This work has split into several different areas. One important area is for a single point-to-point communications link for which it is assumed that the channel changes slow enough for the transmitter to be aware of the channel response function. Under these conditions, the transmitter can apply "pre-equalization" and pre-filtering to the signal prior to transmission. It seems clear that, under these conditions, the least complexity solution to this problem is not the traditional solution of placing all the processing at the receiver [refs. 1-6]. Another important area, that of this paper, looks at the case of multipoint transmission over variable quality, diverse channels, i.e. when the transmitter can not simultaneously pre-process a signal to be optimal at the input to each and every modem. In fact, both areas are encouraged by results due to Price [ref. 7]. This proved that, under high-power conditions, an "ideal" Decision-Feedback Equalizer followed by a code designed for the AWGN channel could achieve capacity. This result raises two immediate questions:

- i) What is the difference between "ideal" and "non-ideal" Decision-Feedback Equalizers?
- ii) How can the performance of "ideal" Decision-Feedback Equalizers be better approximated?

Section 2 reviews the definition of a DFE and the cost of non-ideal performance. In Section 3, we describe helical interleaving and a property of this scheme that basic to our system. In Section 4, we describe the coding and modulation schemes selected for the system. The target base constellations are 32 point PSK and 256 point QAM and the codes are derived from the Barnes-Wall lattice [refs. 14,18]. In Section 5, we pull the ingredients together and describe the entire system. It must be stressed that that the entire system is seen as more than the sum of the parts; the components reinforce each other. Section 6 discusses the results of simulations for simpler models. Section 7 presents conclusions.

2) Decision-Feedback Equalizers

The system to be described revolves around an improved use of coding in systems using a Decision Feedback Equalizer (DFE). In these equalizers, a channel baud is detected via a two-fold process:

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- i) by applying a transversal filter to channel samples taken at times up to and including the time of the present baud.
- ii) by applying a transversal filter to the *decisions* as to the previously transmitted bauds.

The first process is known as the feedforward section and the latter as the feedback section. Figure 1 shows such an equalizer. For both sections the taps to the transversal filter are adjusted so that the combined effect of the system is to remove the effect of the channel transfer function and to produce decisions as to the transmitted bauds. For reasonably stationary channels the taps are adjusted (or "trained") and then left fixed. For more time-varying channels, various algorithms exist for continuous adjustment, ranging from the low complexity LMS algorithm to the more complex Kalman algorithm. The LMS algorithm is suitable for slowly varying channels (actually channels for which the eigenvalue spread of the covariance matrix is small) and the Kalman algorithm is suited for more adverse channels. Hybrid schemes have also been used. The importance of the feedback section has long been understood in relation to several classes of channels. It is of most value when the channel destroys information as well as distorts the signal, for example when a deep spectral null appears on the channel. The decision feedback section, being non-linear, is capable of re-introducing some amount of this lost information that a linear system, operating on the received signal, can not. Figures 2, 3 and 4 (taken from [ref. 8]) show some performance results of a DFE versus a linear equalizer that employs feedforward alone. Figure 2 shows the channel response of three channels. Figure 3 shows the performance of equalizers without decision feedback ("linear feedback" means that a section contains the unquantized outputs). Figure 4 shows the performance of a DFE on the two worst of the three channels. Clearly there are some channels for which the non-linear decision feedback section is critical for communication.

One recognized drawback with DFEs is that of error propagation; when the DFE does produce an error in the detection of the transmitted baud, this error is fed back through the feedback section, providing an erroneous input to several successive symbols and possibly producing further errors in the detected bauds. This can cause performance to be degraded relative to that of correct symbol feedback. In Figure 4, performance curves show the effect of using detected data rather than correct data can result in degradation of at least 2dBs. This is the issue that the proposed system attempts to address. Other authors have addressed this question [refs. 4,5,9] from different perspectives. One might consider solving this problem by adding error correction between the symbol detection and the feedback register (point A in Figure 1). This transpires, at least in the form suggested, to be impractical and/or disappointing in practice. The reason is simple. The correction either involves excessive delay before corrected data is available for input into the feedback section or the code selection is limited to codes of short length and, consequently, limited performance. Fortunately, helical interleaving can remove this dilemma. It is easier to describe helical interleaving as stand-alone technique prior to adapting it to the equalization problem. This is done in Section 3.

3) Helical Interleaving

In this system the above limitation is removed by using the time scrambling inherent in all interleaving and, in particular, a property of a type of interleaving known as helical interleaving, see Figure 5. This interleaving was invented by Tong and Berlekamp of Cyclotomics. It was used by them for forecasting correlated digital error bursts to a Reed-Solomon decoder [ref. 10]. The salient feature of helical interleaving is that every symbol of a codeword is immediately preceded by a symbol that is either in an earlier codeword or is a synchronization symbol. It remains to describe the interleaving. We will describe it by example.

Consider interleaving a code with a block length of eight symbols. To each codeword we attach another synchronization symbol, giving a total block length of nine symbols. Figure 5a shows several codewords with the attached symbol S . The numbering reflects the time ordering of the symbols leaving the encoder and prior to the action of the interleaver. (Note that the sync. character represents the symbol numbers divisible by nine). At the interleaver, the codewords are written down the columns of an array as shown in Figure 5b. When complete, the rows of the array are read out and transmitted. Figure 5c gives the transmit sequence of a few rows. Note that consecutive symbols of a codeword are separated by precisely 8 symbols. At the receiver the process is reversed, i.e., the rows are filled in with the received data and complete columns ending with 'S' are read out. In fact, the entire interleaver and de-interleaver process can be made symmetric.

A symbol c received from the channel is said to "have a prediction" if the preceding channel symbol is either:

- (i) a symbol from a codeword that is decoded earlier than the codeword to which c belongs;
- (ii) a synchronization symbol.

Inspection of Figures 5b and 5c exposes a major advantage of Helical interleavings; every symbol has a prediction. For channels that have heavily correlated error statistics, this is ideal; if a symbol is in error, the following symbol is highly likely to also be in error. If a symbol is known to be in error, the following symbol can be treated as an erasure (for more detail see [ref. 11].) However, we will be adapting this property for a different purpose in Section 5.

4) The Barnes-Wall Lattice and System Coding

4.1 Introduction, encoding and synchronization

An overview of coding for the bandlimited channel is outside of the scope of this paper. A selective list of references are given [refs. 12-18]. There are, in essence, three basic elements that have to be examined prior to the addition of any coding. These are:

- i) An infinite set of lattice points in the complex plane. We think of these as containing the coded signaling constellation if we were not limited to a peak power constraint.
- ii) A finite set of these lattice points that lay within the region that we can signal. For example, on a non-linear channel, we have m regularly spaced points on a unit circle giving m -ary PSK. On a linear channel, we can select a finite set of m points placed on or within a circle of radius r . For example, Figure 6 shows 64-QAM, a set of 64 points arranged in a grid. The grid is obviously a subset of an infinite grid or checkerboard.
- iii) A labeling of the finite set of points that reflects the squared Euclidean distance between pairs of points.

The exact way in which a finite subset of points is "punched out" of an infinite grid varies from case-to-case and can lead to greater or lesser performance gains. This parameter is often called "the shape gain". Since the principles of the present system do not rely upon the exact number of points or the exact shape, we have not optimized this aspect; this can, to a large extent, be done at a later date. This project is targeting two constellations. The first is 32-ary PSK. The second is 256 point QAM. For the QAM case, we have concentrated upon a *square* grid of 256 points (8 channel bits per modulation symbol). A circle containing 256 points from a square grid would produce additional gain in terms of average SNR. Given a base constellation, the next essential is to give it a labeling that reflects the Euclidean distance between the points. Although there have been many generalizations, Ungerboeck's [ref. 12] labeling by set-partitioning is the simplest to understand. For PSK, the

labeling is relatively intuitive, amounting to a clock order around the circumference. For QAM, the labeling is only slightly harder, [ref. 14]. For example, in Figure 6, 64 QAM points are labeled 0-63. The labeling is constructed so that the least significant bit is the most error prone, the second most least significant bit is the next most etc. To be more precise, if the minimum squared Euclidean distance between any two distinct points in the square is d_{\min}^2 and two points agree in the first k least significant bits, $k \geq 0$, then the minimum distance between the points is $\geq 2^k \cdot d_{\min}^2$. Alternatively, the constellations selected by specifying the least k bits of a modulation baud have superior distance and performance properties as k increases, the gain being at least 3dBs per increment of k .

With the constellation and labeling fixed, we are ready to add coding. We are going to use a particular example derived from the Barnes-Wall lattice of complex dimension 8 and real dimension 16 and written as $BW(16)$, [refs. 14,16,18]. By definition, the Barnes-Wall lattice is an application to a square grid constellation. However, the same coding scheme can be used for PSK, i.e. encoded integers can be used as to select PSK points using mapping by set-partitioning. Data is entered in a n by 8 array, where $n \geq 3$. The first row only has 1 data bit, the second row only has 4 data bits and the third has 7 bits. The remaining $n-3$ rows are fully occupied by data bits. The first row is completed by setting all the row entries equal to the data bit in that row. This is a (8,1;8) codeword. The second row is completed by taking the 4 bits in that row, encoding them into a (8,4;4) Reed-Muller codeword and placing the codeword into the second row. The third row is completed by adding an eighth bit that makes the third row entries add to an even entry, a codeword from a (8,7,2) code. An example is given in Figure 7. The columns of the array are regarded as integers. Hence the digital encoding gives a sequence of eight integers. Each of these integers selects a unique constellation point using a set-partitioning labeling. For a square grid labelled by set-partitioning we get points from $BW(16)$, the Barnes-Wall lattice [refs. 14,18]. For a PSK system, the encoded integers can still be used to select constellation points but the process does not give Barnes-Wall lattice points. In either case, a codeword can be regarded as sequence of 8 complex constellation points and every sequence of eight constellation points is not necessarily a codeword.

A $BW(16)$ lattice using n rows contains $(n-3) \cdot 8 + 12 = 8n-12$ bits of data spread over 8 modulation symbols, e.g. 52 bits for $n=8$. This allows the nominal gain of the lattice (for large n and high SNR) to be estimated and normalized for both the redundancy and dimensionality. Unfortunately, the definition of gain differs from source to source. [ref. 16, p. 74] gives the gain as 5.491dBs while Forney [ref. 14] gives the gain as $10 \log_{10}(2^{1.5}) = 4.5118$ dBs. $BW(16)$ is the best known lattice of complex dimension 8 and there is strong evidence [ref. 16] this is the best possible lattice of this dimension. It was selected for this project as a compromise between ease of decoding and return in gain.

In this system, we add a ninth synchronization symbol to each lattice point, giving a combined block-length of nine modulation symbols per block. The n_s least most significant bits of the synchronization symbol are set to a fixed pattern and the $n - n_s$ most significant bits are used for data communication. The value of n_s is a parameter to be optimized. Obviously, small values are better in terms of throughput. Higher values are better in terms of training and synchronization performance. This symbol is used for block synchronization and equalizer training.

4.2 Decoding/demodulation

The description of the decoding/demodulation for the PSK constellation application is virtually identical to that of the QAM Barnes-Wall lattice and we concentrate the description upon the latter.

There are various methods that can be used for the demodulation/decoding of the Barnes-Wall lattice. The method being implemented is simple but sub-optimal. The process consists of the

sequential soft-decision decoding of the (8,1;8) (8,4;4) and the (8,7;2) codes. In more detail, suppose that we receive eight complex points, $(r_1, r_2, r_3, r_4, r_5, r_6, r_7, r_8)$ and we wish to estimate the point from $BW(16)$ that was transmitted. The following process takes place:

- i) For each received point r_i , $1 \leq i \leq 8$, we form $d(i) = d_{0,i}^2 - d_{1,i}^2$, where $d_{\delta,i}$ is the squared Euclidean distance from r_i to the nearest point ending in a lsb = δ , for $\delta = 0$ or 1 .
- ii) We compute $d = \sum_{i=1}^{i=8} d(i)$. If d is positive, we decode the lsbs to $(0,0,0,0,0,0,0,0)$. If d is negative, we decode the lsbs to $(1,1,1,1,1,1,1,1)$. Suppose that the decoding decision is that $t_{0,i}$ was sent where $t_{0,i}$ is a constant (0 or 1) for all $i : 1 \leq i \leq 8$.
- iii) For each received point r_i , $1 \leq i \leq 8$, we form $c(i) = c_{0,i,t}^2 - c_{1,i,t}^2$, where $c_{\delta,i,t}$ is the squared Euclidean distance from r_i to the nearest point that has its two least significant bits equal to $(\delta, t_{0,i})$, for $\delta = 0$ or 1 . More intuitively, we look for the metrics within the subconstellation of points selected by placing the lsb equal to the decoded value.
- iv) Using the $c(i)$ as metrics, we apply soft-decision decoding to the (8,4;4) code. (This can be accomplished, for example, by the Hadamard transform [ref. 19]). Suppose that the decoder decides the secondmost least significant bits are equal to $(t_{1,i} | 1 \leq i \leq 8)$, where these form a (8,4;4) codeword.
- v) For each received point r_i , $1 \leq i \leq 8$, we form $b(i) = b_{0,i,t}^2 - b_{1,i,t}^2$, where $b_{\delta,i,t}$ is the squared Euclidean distance from r_i to the nearest point that has its three least significant bits equal to $(\delta, t_{1,i}, t_{0,i})$, for $\delta = 0$ or 1 .
- vi) We place $t_{2,i}$ equal to 0 if $b(i)$ is positive and 1 otherwise. If the sum of the $t_{2,i}$ is odd, we locate i_{\min} , the value of i for which $b(i)$ is smallest in absolute value, and invert $t_{2,i_{\min}}$.
- vii) For each received point r_i , $1 \leq i \leq 8$, we find the constellation point $m(i)$ having the least squared Euclidean distance from r_i subject to the point having its three least significant bits equal to $(t_{2,i}, t_{1,i}, t_{0,i})$. The sequence of $m(i)$ is the demodulated signal, or, equivalently, the decoded point of the $BW(16)$ lattice.

5) System Description

From Sections 2, 3 and 4, we are in a position to describe the system and to understand the motivations for the various combinations of techniques. In 5.1 we describe the process at the transmitter. In 5.2 the receiver process is described. The notation as to symbol and sample order is defined in Section 5.1. A system block diagram is shown in Figure 8.

5.1 Transmitter process and channel notation

The data is assumed independent and identically distributed (iid) with a probability = 0.5 of a 0 or 1, i.e. it has been encrypted. Data is encoded using the binary codes described in Section 4. We concentrate the description on the case of 256 QAM. This takes, for a targeted 8 bit per modulation symbol system, 54 bits and encodes them into 8 labels where each label contains 8 points. A ninth label is added to each $BW(16)$ lattice point. This ninth label contains n_s pre-set synchronization bits and $8 - n_s$ data bits. Thus, if $n_s = 2$, a total of 60 bits are encoded into a total of nine labels. When we refer to label number 13, we mean the 13-th label to leave the coding device. Labels are integers. (Conceptually, we could dispense with labels and regard the encoder output as a sequence of complex constellation points. However, it is implementationally easier to interleave integer labels rather than complex numbers.) We now helically interleave the labels in the exact fashion described in Section 3 and Figure 5. The interleaved stream of labels are used to select complex constellation points

and these points are transmitted. Point 13 corresponds to the point that is selected by the 13-th label leaving the encoder. Points are members of the constellation, i.e. they are complex numbers.

5.2 Receiver process

The transmitted points are subject to a convolution with the channel response function and the addition of Gaussian noise. The resulting signal is sampled at the transmitter at the signaling rate (this article does not consider fractionally spaced equalizers). The numbering convention reflects the same numbering of the underlying sequence of constellation points. For example, sample number 13 refers to the sample of the received signal that would, in the absence of any intersymbol interference and additive noise, correspond to the constellation point selected by the 13-th symbol leaving the encoder. Sample numbers are complex numbers that might not belong to the constellation. Note that there is a difference between sample number 13, point number 13 and label number 13. The processing is described assuming that block synchronization (which is a study in its own right) has been achieved. The broad idea is that there a bank of eight slow DFE equalizers and one fast DFE equalizer. The combined complexity, in terms of equalizer operations per bit, is approximately equal to that of two fast equalizers. The fast equalizer does not enjoy any advantage over that of a conventional DFE (it is also not trusted to be as correct as the slow equalizers). This equalizer processes the input signal samples in a conventional process. When a non-synchronization symbol is being processed, the equalizer tap updates use data-directed mode, i.e. the difference between the predicted symbol and the received signal sample is used as the error signal to re-adjust the tap values. The re-adjustment could use any of a wide variety of algorithms but, in fact, we are using the simple LMS gradient algorithm. The Kalman Algorithm and its various derivatives would be a (high complexity) alternative. Upon receiving a synchronization symbol, the fast equalizer still uses data-directed mode but the difference is between the predicted symbol and the closest constellation point that has a label ending with the pre-set synchronization pattern. Since the sub-constellation of possible synchronization points has superior distance properties than the entire constellation, the update on synchronization points is more accurate. The process is seen as two-fold; the synchronization symbols "snaps the equalizer in" and the other updates try to track the changes.

The slow equalizers work in an iterative fashion. Throughout this description we assume that the system is giving correct data. In Figure 9, we show the equalizers at the start of a cycle. We will describe the process for codeword 73-80. The registers to the left are the feedforward part of the equalizers. They hold channel samples. The labels on the feedforward registers refer to the sample times with the above notation. Note that each register contains the samples received immediately prior to and including the symbol that it is attempting to predict. The registers to the right are the decision feedback registers. They hold decisions as to the immediately preceding constellation points. It is important to note that the decision registers hold two types of decisions. The shaded areas of memory refer to the decisions made by the fast equalizer. These are, given the correct decoder assumption, relatively unreliable. The unshaded areas in the decision registers refer to constellation points that have either been decoded prior to this codeword or which are synchronization symbols. These are relatively reliable. Consider the iterative procedure. The slow equalizers predict the constellation points of the codeword. These predictions are corrupted versions of the original sequence and the decoder is called upon to correct the noise (a non-linear process). The output of the decoder is, by assumption, the correct sequence of constellation points. For each register, the decoded constellation point can be compared to the predicted point to get an error signal. Note that this will be more reliable than the normal data-directed error signal (for example, one of the equalizers might diverge completely and still be re-trained with the decoded data-directed error signal; this is unlikely to happen with a single data-directed equalizer). The taps for each slow equalizer are re-trained using

the decoded data-directed error signals. The decoded constellation points are stepped into the decision feedback registers, the entire contents and taps of each register are rotated up and new channel samples are entered into the feedforward sections. This, except for the lowest register, gives the next stage of the iteration, as shown in Figure 10. The taps for the lowest register are obtained from the fast equalizer. After the fast equalizer has processed the synchronization symbol, the taps and contents of the equalizer are transferred to the bottom equalizer. With this transfer, the iteration is closed and we are ready to repeat the process for codeword 82-89, as shown in Figure 10. There are several points to note:

- i) The most important part of the decision feedback cancellation process are the decisions immediately preceding the present sample. These are the most reliable in this scheme. Note that the top registers are more reliable than the low registers as they hold less undecoded decisions and that the undecoded decisions are farther back in time relative to the predicted symbol.
- ii) If the channel is varying in time, the taps values of each equalizer can vary from each other. The decoding process does not imply correlation between register tap values.
- iii) In terms of implementation, the registers and taps are not "rotated up" The registers are arranged as a circular area of memory with a pointer to each area. The "rotation" consists of decrementing each register's pointer modulo 8. The register with the pointer equal to zero has the contents and tap values discarded and replaced by those in the fast equalizer. (Note that, with this approach, the inputs to the decoder have to be cycled before they are in correct order). Similarly, the equalizer that is going to be discarded is not updated.
- iv) There are only seven slow equalizer updates per codeword and only one codeword per nine channel symbols. There is one fast equalizer update per channel symbol.

6) Model Results

Before embarking upon this design the principle of helical interleaving and DFEs was investigated using simpler models. In these experiments, one-dimensional PAM was used for modulation. The channels were assumed stationary and the tap values pre-computed. The channels were taken from a magnetic recording source [ref. 8] and are shown in Figure 11. They are similar except in severity. They are referred to as Channel 1 and 3 (Channel 2 was intermediate in definition and results). The experiments used a (16,5;8) Reed-Muller decoded with soft-decision information via a Hadamard transform. The performance curves show four lines: the matched filter bound (i.e. the performance if no intersymbol interference or coding is present), conventional DFE (no coding and interleaving), co-designed receiver with corrected feedback (i.e. the full scheme with corrected data in the decision feedback registers whenever possible) and a receiver that uses interleaving and decoding but which does not attempt to replace the DFE estimates in the decision registers. The coding results were penalized by $10\log_{10}(17/5) \approx 5.31\text{dBs}$, i.e. for the utilized redundancy. Figure 12 shows the results for Channel 1. The straight addition of coding with no corrected feedback does little more than Conventional DFE once the normalization is added. However, the addition of corrected feedback makes a considerable difference, even after normalization. The improvement to conventional DFE is approaching 2dBs with improving SNR. Figure 13 shows the curves for the much harsher Channel 3. The straight use of coding does not justify the redundancy; the normalized figures are worse than DFE alone. The addition of coding with corrected feedback and helical interleaving is worthwhile; even with normalization, there are significant power gains over conventional DFE. Without the normalization penalty, the scheme is working at much lower SNR. Note that the total gain can be considered as the sum of the coding gain plus the co-designed gain.

In other experiments, it was observed that the co-designed gain depends on the channel; different channels cause greater or lesser degrees of error propagation. At worst you get the coding gain, at best you get considerably more.

7) Conclusions

This is work in progress and present efforts are concentrating upon refining the design and to implement it on a Motorola DSP56000 Digital Signal Processing system. It is a pleasure to acknowledge the support of Comdisco Inc. in this regard.

However, it seems that the technique will provide superior performance when:

- i) The channel has significant non-linearities and/or spectral nulls;
- ii) The throughput delay is not a critical parameter;
- iii) The transmission is broadcast.

In summary, a technique is presented that appears to offer significant benefits over a black-box approach to equalization and modulation. The technique is closest in spirit to a technique introduced by Eyuboglu [ref. 4] and fits into several other attempts to improve upon DFE [refs. 2,4-6,7,9].

References

- [1] Kasturia, S., J. Asalanis and J. Cioffi, "Vector Coding for Partial Response Channels," submitted to *IEEE Trans. Info. Theory*.
- [2] Forney, G.D., Jr. and A.R. Calderbank, "Coset Codes for Partial Response Channels," submitted to *IEEE Trans. Info. Theory*.
- [3] Peile, R.E., "Coding in Correlated Gaussian Noise," pre-print.
- [4] Eyuboglu, M.V., "Detection of Coded Modulation Signals on Linear, Severely Distorted Channels using Decision-Feedback Noise Prediction with Interleaving," *IEEE Trans. Comm. Theory*, Vol. 34, No. 4, April 1988.
- [5] Eyuboglu, M.V. and S.U. Qureshi, "Reduced-State Sequence Estimation for Trellis-Coded Modulation on Intersymbol Interference Channels," submitted to *IEEE SAC*, Special Issue on Band-Limited Channels.
- [6] Eyuboglu, M.V., "Coding and Equalization," CSI/ARO Workshop, May 1989.
- [7] Price, R., "Nonlinearly Feedback Equalized PAM versus Capacity for Noisy Filter Channels," *Proc. of ICC '72*, Philadelphia, PA, June 1972.
- [8] Proakis, J.G., *Digital Communications*, McGraw-Hill, 1983.
- [9] Bergmans, J.W.M., S.A. Rajput and F.A.M. Van De Laar, "On the Use of Decision Feedback for Simplifying the Viterbi Detector," *Philips J. Res.*, Vol. 42, 1987, pp. 399-428.
- [10] Tong, P. and E.R. Berlekamp, "Improved Interleavers for Algebraic Block Codes," US patent 4 559 625, December 17, 1985.
- [11] Peile, R.E., "Error Correction, Interleaving and Differential Pulse Position," *International Journal of Satellite Communication*, Vol. 6, 1988, pp. 173-187.
- [12] Ungerboeck, G., "Channel Coding with Multilevel/Phase Signals," *IEEE Trans. on Info. Theory*, Vol. 28, No. 1, January 1982.
- [13] Calderbank, A.R. and N.J.A. Sloane, "New Trellis Codes Based on Lattice and Cosets," *IEEE Trans. on Info. Theory*, Vol. 33, No. 2, March 1987.

- [14] Forney, G.D., Jr., "Coset Codes I: Introduction and Geometrical Classification," *IEEE Trans. Info. Theory*, 1989.
- [15] Sloane, N.J.A., "Binary Codes, Lattices and Sphere-Packings," in *Combinatorial Surveys: Proceedings of the Sixth British Combinatorial Conference*, Academic Press, 1977 (Ed. P.J. Cameron).
- [16] Conway, J.H. and N.J.A. Sloane, *Sphere Packings, Lattices and Groups*, New York, Springer-Verlag, 1987.
- [17] Forney, G.D., Jr., R.G. Gallager, G.R. Lang, F.M. Longstaff and S.U. Qureshi, "Efficient Modulation for Band-Limited Channels," *IEEE J. Selected Areas Commun.*, Vol. SAC-2, 1984, pp. 632-647.
- [18] Barnes, E.S. and G.E. Wall, "Some Extreme Forms Defined in Terms of Abelian Groups," *J. Australian Soc.*, Vol. 1, 1959, pp. 47-63.
- [19] MacWilliams, F.J. and N.J.A. Sloane, *The Theory of Error-Correcting Codes*, North-Holland, 1977.

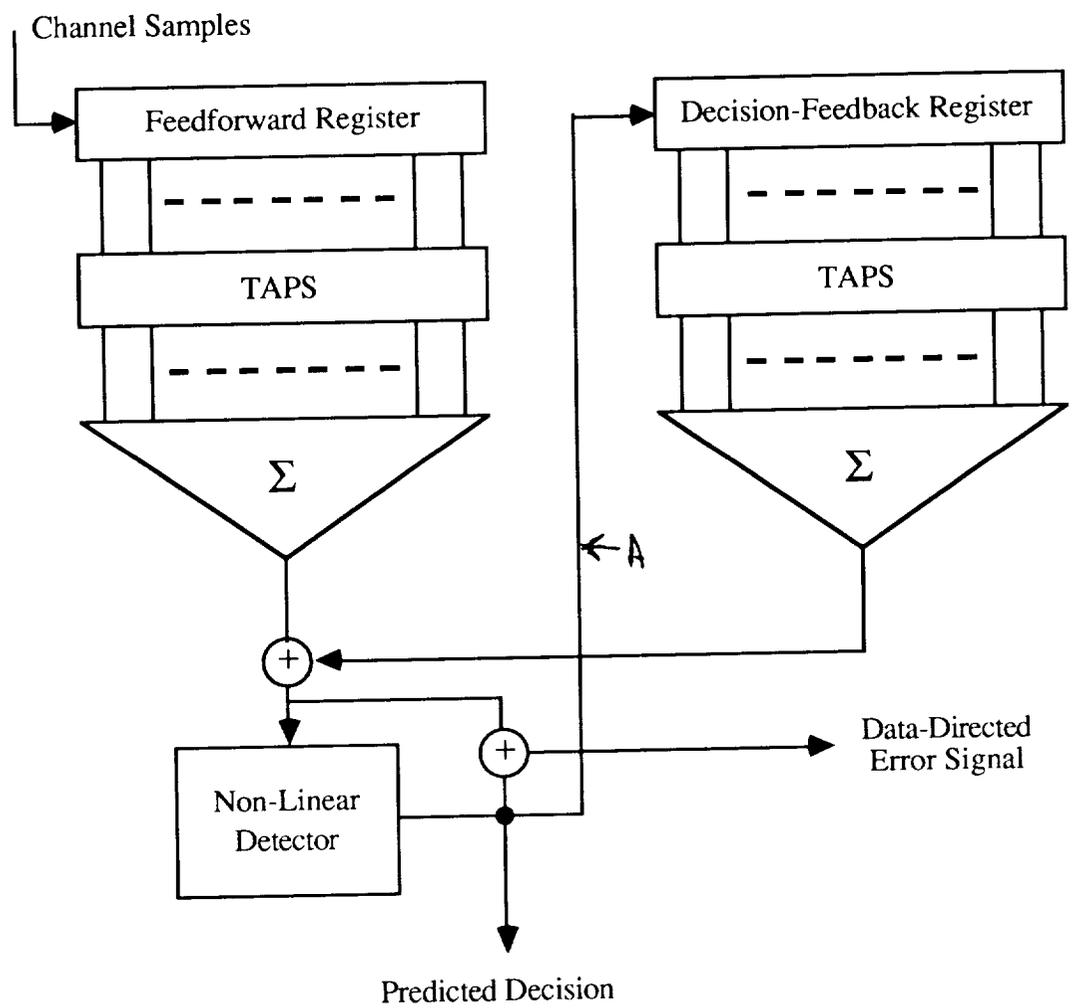
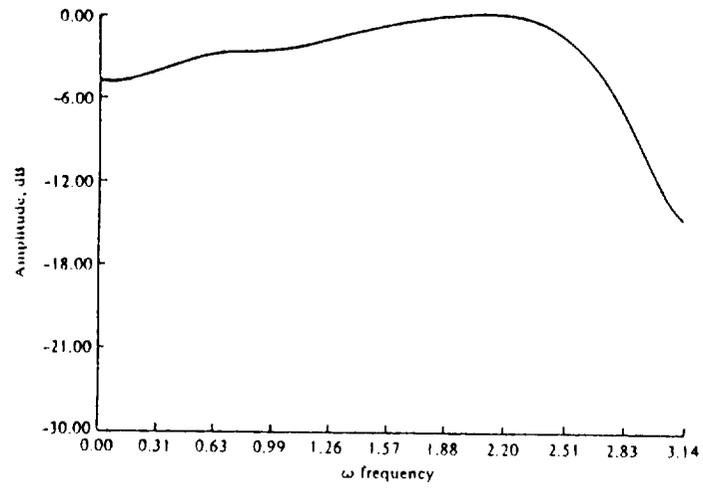
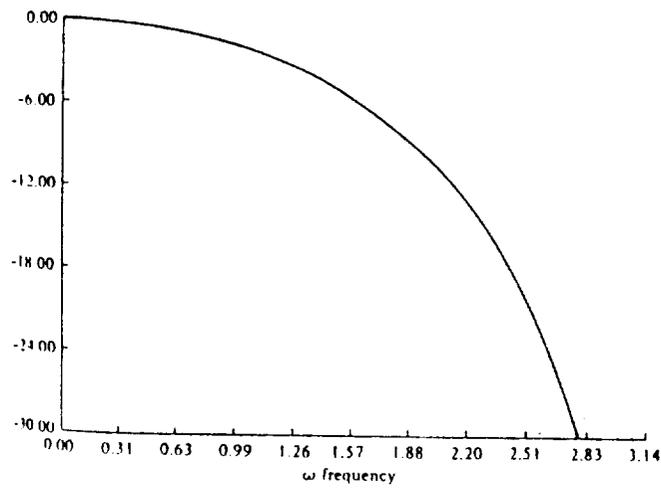


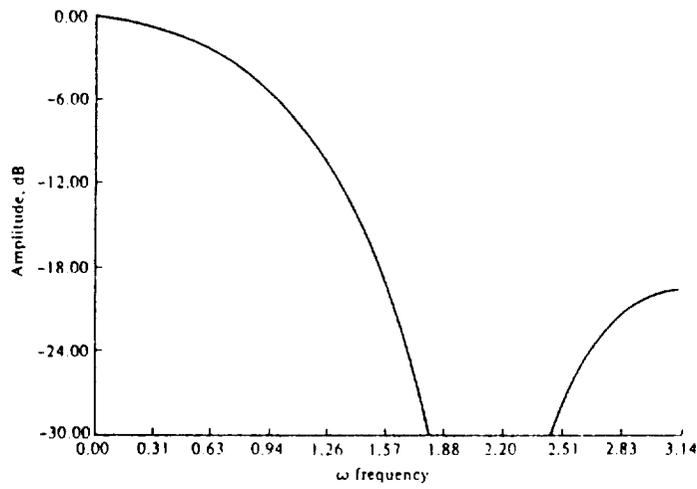
Figure 1: Decision Feedback Equalizer Schematic



a)



b)



c)

Figure 2: Channels

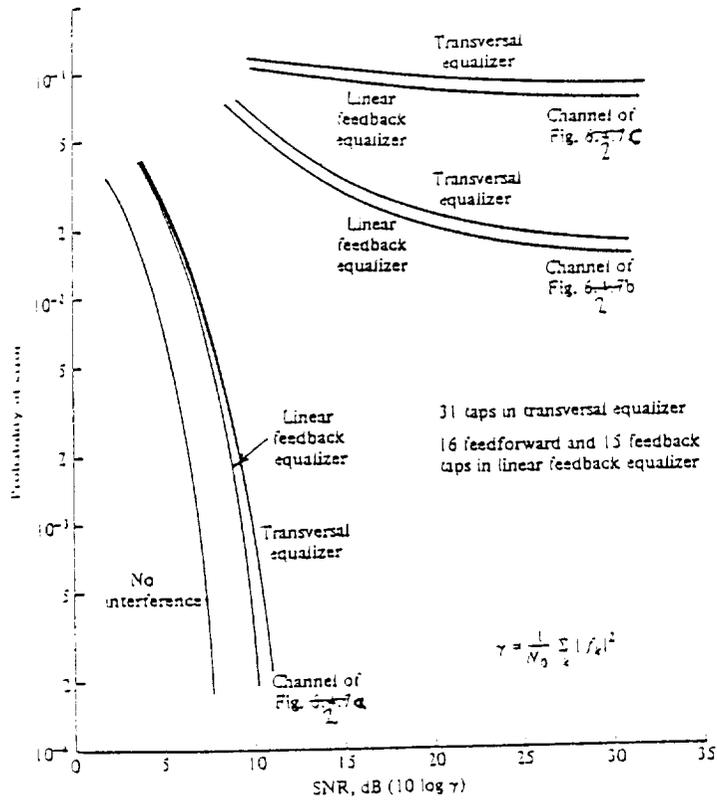


Figure 3: Error Rate Performance of Linear MSE Equalizer

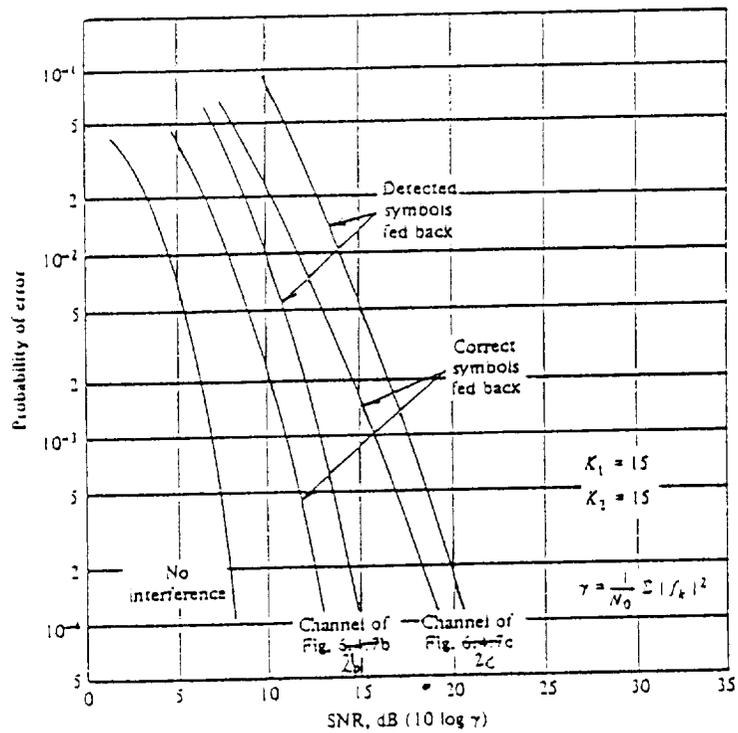


Figure 4: Performance of decision-feedback equalizer with and without error propagation.

5a: Encoded Data plus Sync Stream

1,2,3,4,5,6,7,8,	S
10,11,12,13,14,15,16,17,	S
19,20,21,22,23,24,25,26,	S
28,29,30,31,32,33,34,35,	S
37,38,39,40,41,42,43,44,	S
46,47,48,49,50,51,52,53,	S
55,56,57,58,59,60,61,62,	S
64,65,66,67,68,69,70,71,	S
73,74,75,76,77,78,79,80,	S
82,83,84,85,86,87,88,89,	S
91,92,93,94,95,96,97,98,	S
100,101,102,103,104,105,106,107,	S

5b: Interleaving Array

1,							
2,	10,						
3,	11,	19,					
4,	12,	20,	28,				
5,	13,	21,	29,	37,			
6,	14,	22,	30,	38,	46,		
7,	15,	23,	31,	39,	47,	55,	
8,	16,	24,	32,	40,	48,	56,	64,
S,	17,	25,	33,	41,	49,	57,	65,
73,	S,	26,	34,	42,	50,	58,	66,
74,	82,	S,	35,	43,	51,	59,	67,
75,	83,	91,	S,	44,	52,	60,	68,
76,	84,	92,	100,	S,	53,	61,	69,
77,	85,	93,	101,	109,	S,	62,	70,
78,	86,	94,	102,	110,	118,	S,	71,
79,	87,	95,	103,	111,	119,	127,	S,
80,	88,	96,	104,	112,	120,	128,	136,
S,	89,	97,	105,	113,	121,	129,	137,

5c: Transmitted Stream (Partial)

8,16,24,32,40,48,56,64,S,17,25,33,41,49,57,65,73,S,26,34,42,50,58,66,
 74,82,S,35,43,51,59,67,75,83,91,S,44,52,60,68,76,84,92,100,S,53,61,
 69,77,85,93,101,109,S,62,70,78,86,94,102,110,118,S,71,79,87,95,103,
 111,119,127,S,80,88,96,104,112,120,128,136,

Figure 5: Helical example

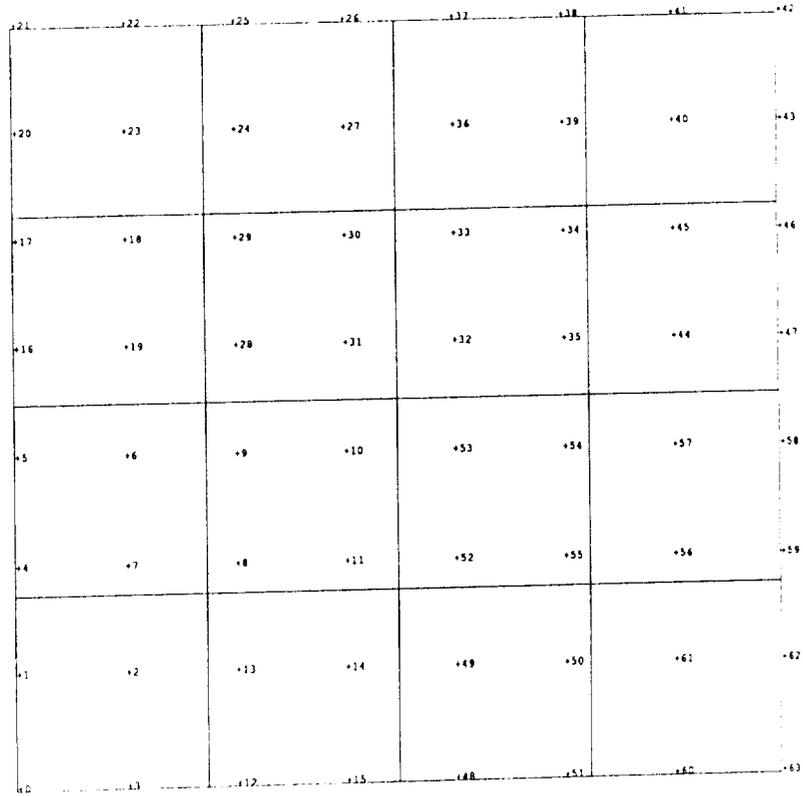


Figure 6

1	1	1	1	0	1	1	1
0	0	1	0	0	0	1	1
0	0	0	1	0	1	1	1
1	0	1	1	1	1	0	
1	0	1	1				
1							

Data-block

↓ Encoding

1	1	1	1	0	1	1	1
0	0	1	0	0	0	1	1
0	0	0	1	0	1	1	1
1	0	1	1	1	1	0	1
1	1	0	0	0	0	1	1
1	1	1	1	1	1	1	1

(8,7,2) codeword
 (8,4,4) codeword
 (8,1,8) codeword

Integer: 37 35 53 45 5 45 49 63

Figure 7: Encoding Example

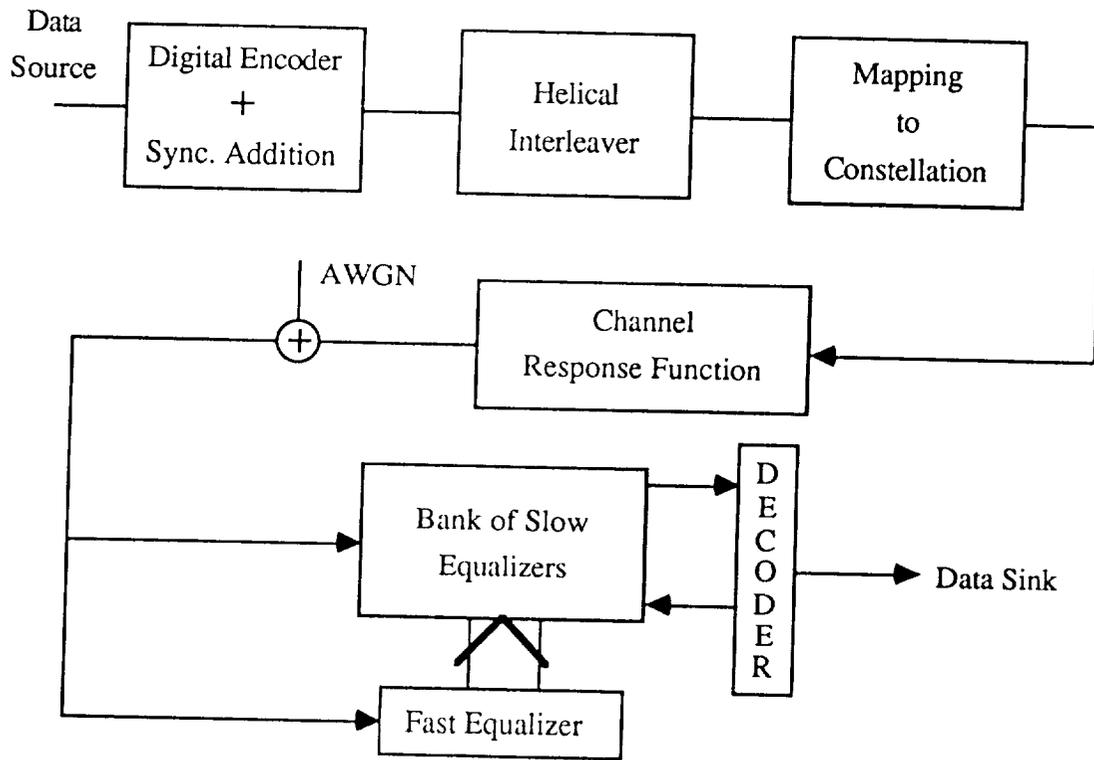
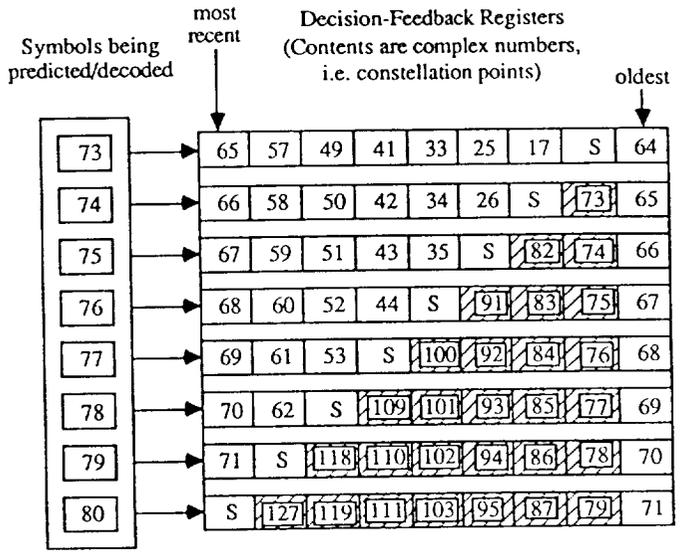
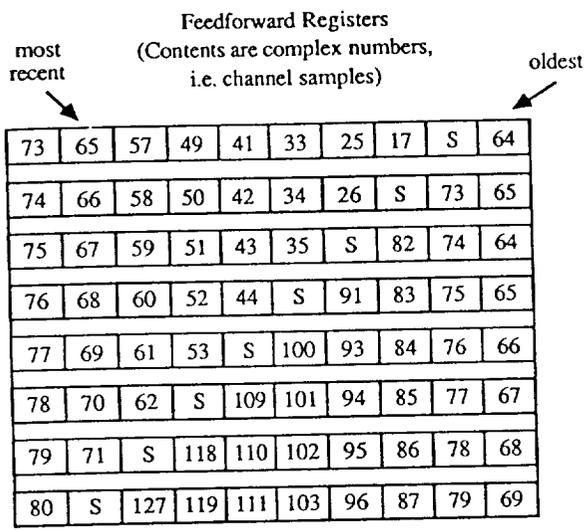
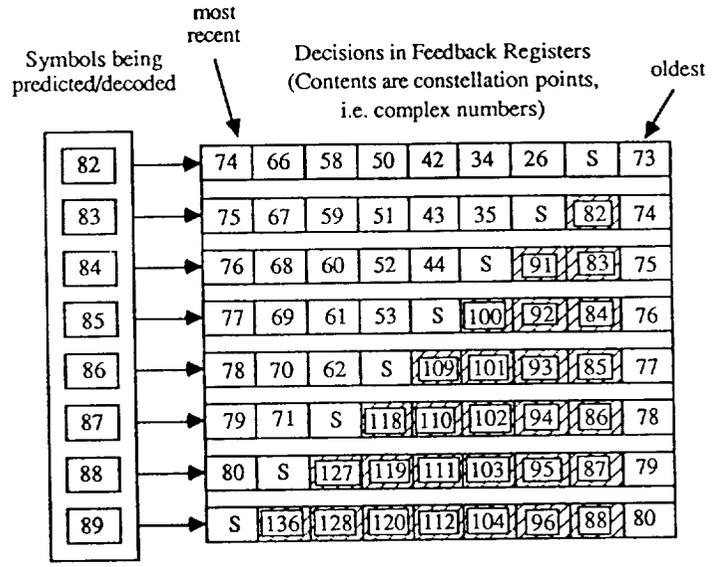
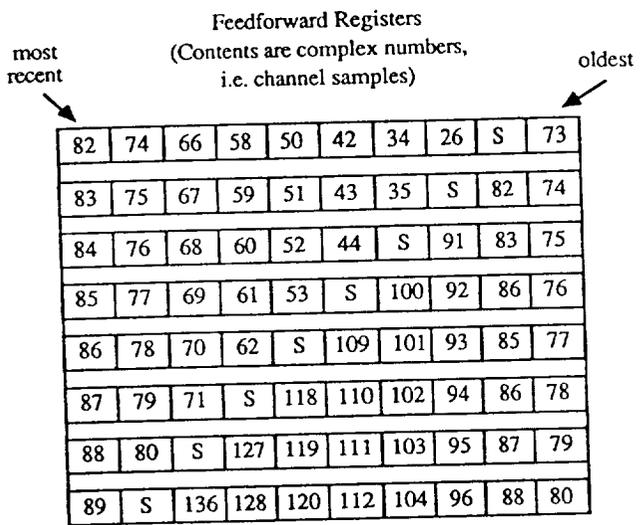


Figure 8: System Description



 Relatively unreliable decision,
i.e. fast equalizer output

Figure 9: Contents of Slow Registers at Initial Prediction



 Relatively unreliable decision,
i.e. fast equalizer output

Figure 10: Contents of Slow Registers at Next Codeword

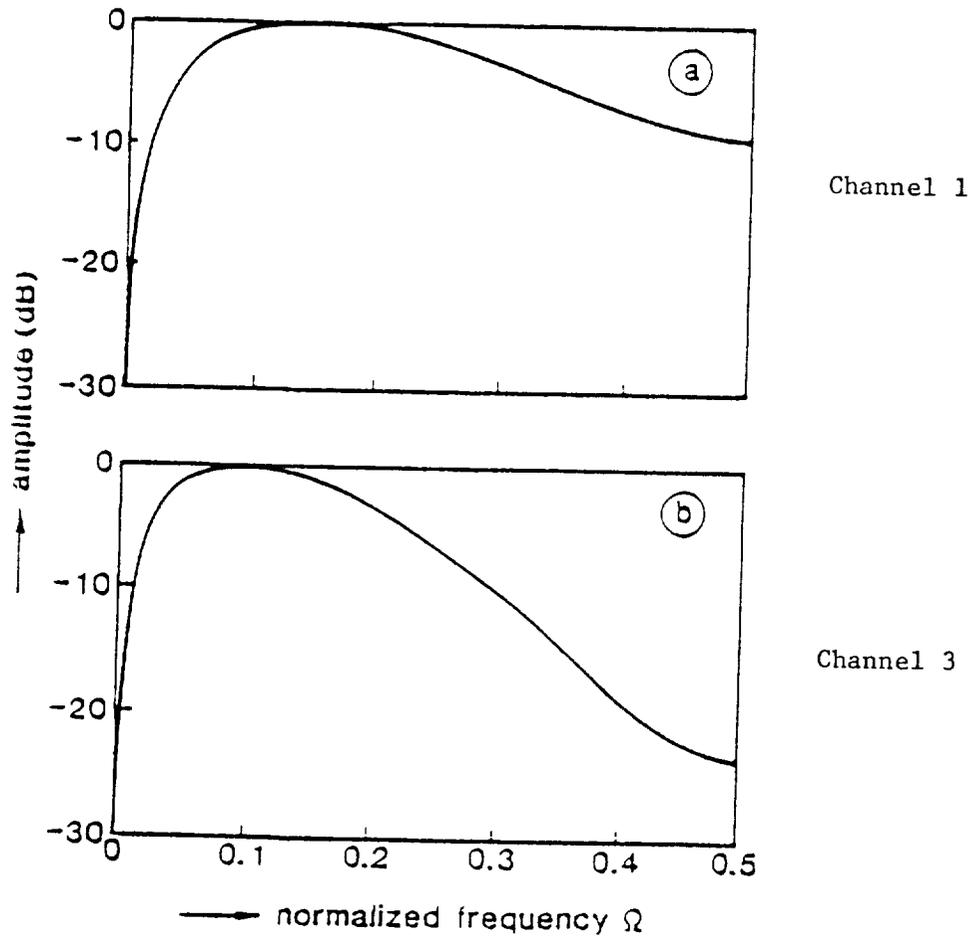


Figure 11

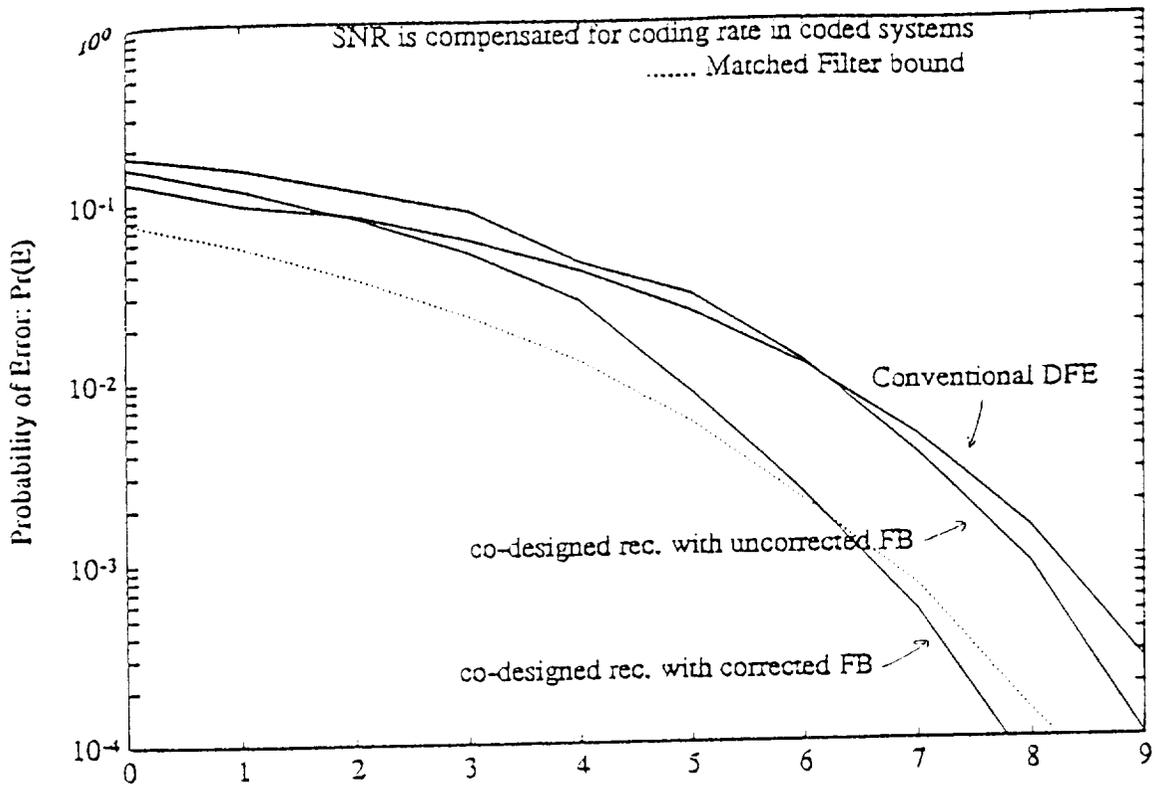


Figure 12: SNR vs Pr(E) plot for Channel 1

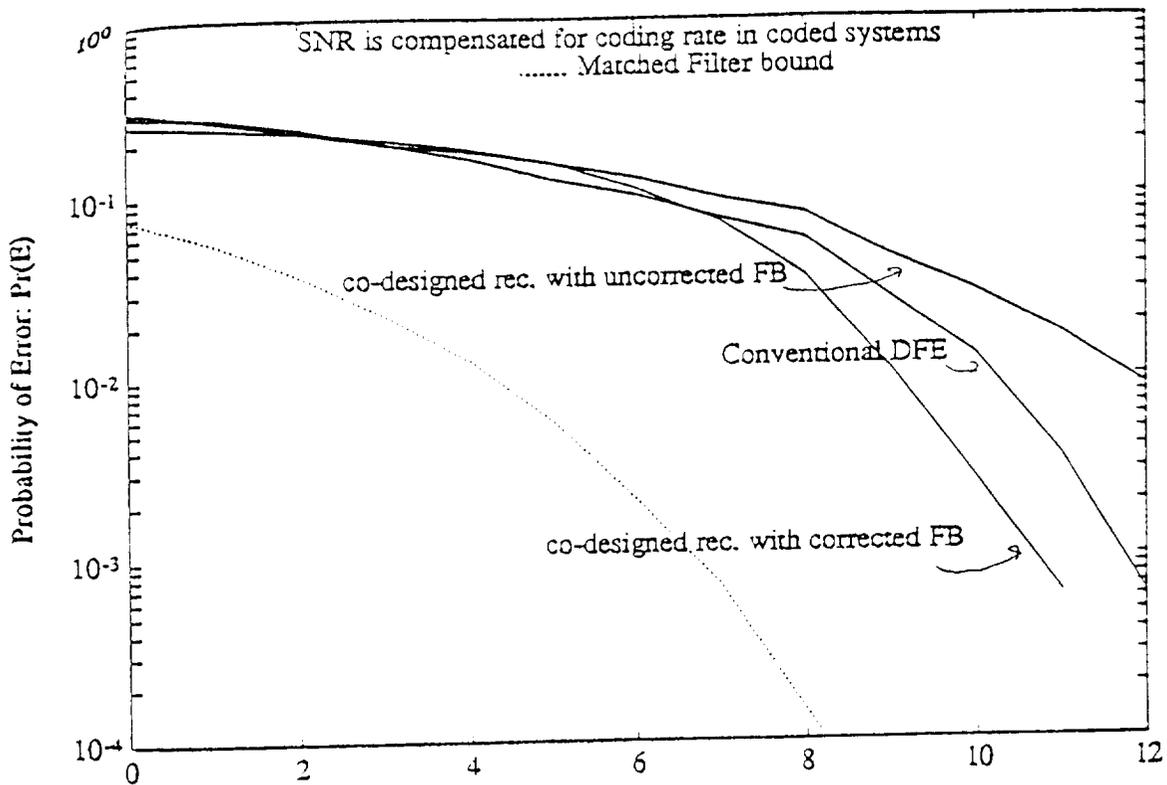


Figure 13: SNR vs Pr(E) plot for Channel 3

N 9 2 - 2 2 0 1 0

MODULATION TECHNIQUES FOR POWER AND SPECTRALLY EFFICIENT SATCOM SYSTEMS

KAMILO FEHER

Department of Electrical Engineering and Computer Science
University of California, Davis; Davis, CA 95616 (*)

ABSTRACT

Research on modulation/demodulation (modem) techniques which leads to improved power and spectral efficient digital satellite communications systems is proposed. A new family of digital modems, which enable satellite earth station and satellite transponder operation with fully saturated high power amplifiers (HPA) in an adjacent channel environment, having an optimized $P(e) = f(E_b/N_o)$ performance will be introduced and analyzed.

We propose the study of Superposed-Quadrature-Amplitude-Modulated (SQAM) systems which have offset and/or coincident transition crosscorrelated and pulse overlapped baseband signal processors. We will introduce and optimize the performance of a new generation of $\pi/4$ -shift SQAM linear modulation techniques for fully saturated power amplifier and spectrally efficient SATCOM system applications. It is expected that $\pi/4$ -shift SQAM and $\pi/4$ -shift bandlimited QPSK systems will have reduced envelope fluctuations and lead to reduced spectral spreading. A new class of linear and nonlinear phase transmit and receive intersymbol-interference (ISI) free filters combined with reduced overshoot power baseband signal processors is also expected to lead to improved efficiency SQAM digital satellite transmission systems.

The proposed new generation of SQAM modulated signals is suitable for coherent as well as for differential demodulation. Differential demodulators have a faster synchronization time than their coherent counterparts. The performance of our proposed modems will be compared with the performance of continuous phase modulation (CPM) and trellis coded satellite modems.

Following the proposed theoretical investigations and computer simulations, hardware prototypes will be built and tested.

(*) Work funded under Grant No. NAG 3 1007; NASA Technical Officer: J. M. Budinger

OBJECTIVES OF PROPOSED RESEARCH

Our goal is to improve the power and spectral efficiency and the network flexibility of new generations of digital satellite and other digital transmission systems. To achieve this goal we propose to undertake the development and analysis of the following closely related research tasks:

- (a) Introduce and study the performance of a new generation of **Superposed-Quadrature-Amplitude-Modulated (SQAM)** digital satellite communications systems. Research of our crosscorrelated nonlinear-phase ISI free premodulation filters with reduced overshoot power [1] is expected to lead to an increased spectral efficiency of about 50% and to a 2 to 4 dB improved power efficiency in a nonlinearly amplified system. The proposed modem techniques will be optimized in a complex interference environment, including Additive White Gaussian Noise (AWGN), Adjacent Channel Interference (ACI) and Co-Channel Interference (CCI).
- (b) Introduce and optimize $\pi/4$ -shifted **SQAM** and $\pi/4$ -shifted QPSK satellite modems operated in nonlinear satellite systems. These bandlimited linearly modulated systems have a reduced envelope fluctuation and reduced spectral spreading. $\pi/4$ -shift SQAM modulated signals may be **coherently and differentially demodulated** [2].

In order to reduce the size of the antenna and or to enable operation with smaller, lower cost earth station high power amplifiers (HPA), new modulation/demodulation system models will have to take into account high power efficiency requirements. The objective of our research is to develop a new family of digital modems which will enable satellite earth station transmitter operation with fully saturated HPA in a closer spaced adjacent channel environment. Our proposed new system models as well as hardware prototypes are expected to achieve a good performance **without** the requirement of complex (and with present technology frequently impossible) **post HPA filters**. We propose to have a low-power-hard-limiting-amplifier (LPHA) before the final HPA amplifier. LPHA devices can be designed to have a much lower AM to PM conversion than their HPA counterparts.

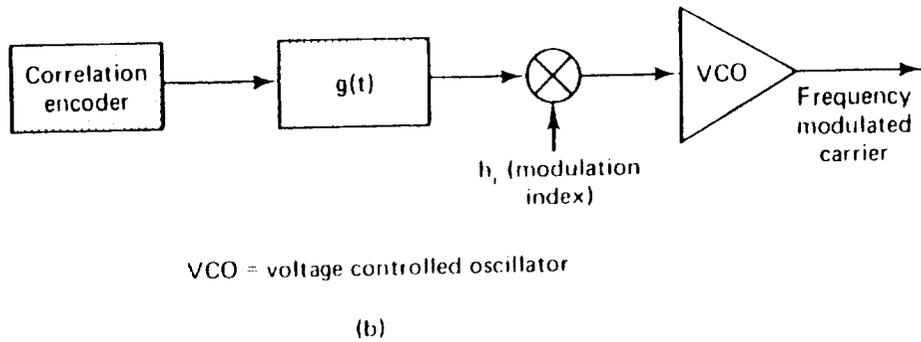
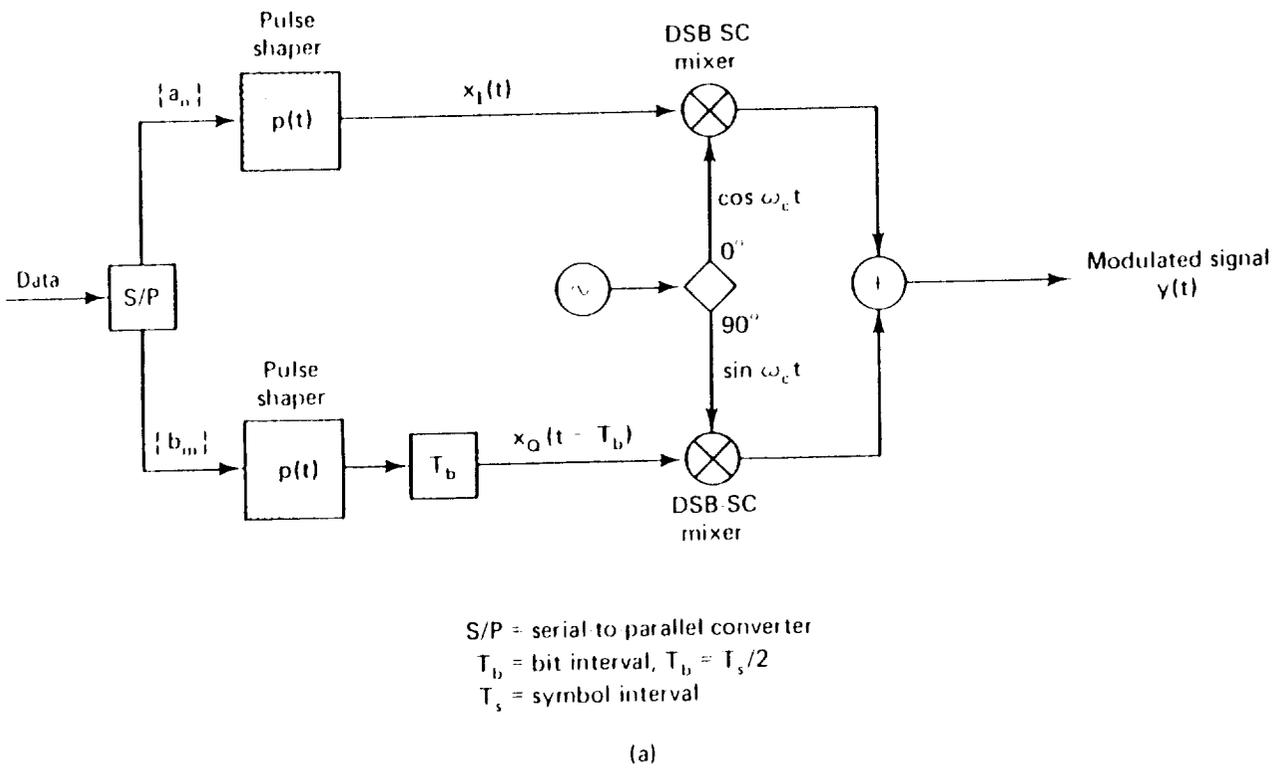
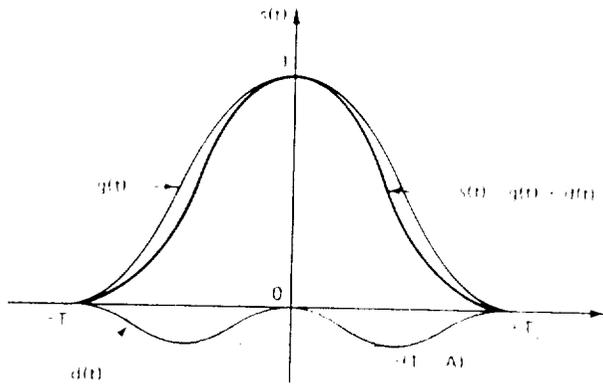
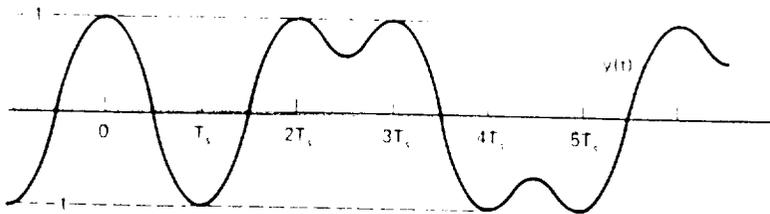
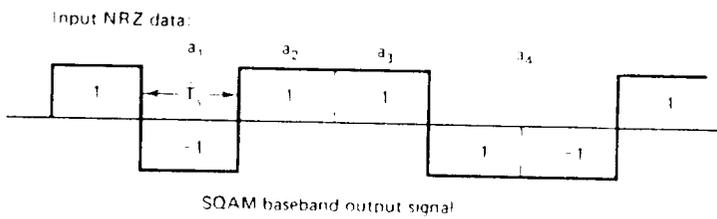


Figure 1 (a) Block diagram of a quadrature amplitude modulator
 (b) Block diagram of CPFSK modulator



(a) An example of an SQAM double interval pulse $s(t)$, which is a superposition of $q(t)$ and $d(t)$



(b) Processed SQAM baseband output

Figure 2 SQAM baseband signal shaping process using the double-interval pulse overlapping concept. (Note: $T_s = 2T_b$ is the symbol interval, where T_b is the bit interval)

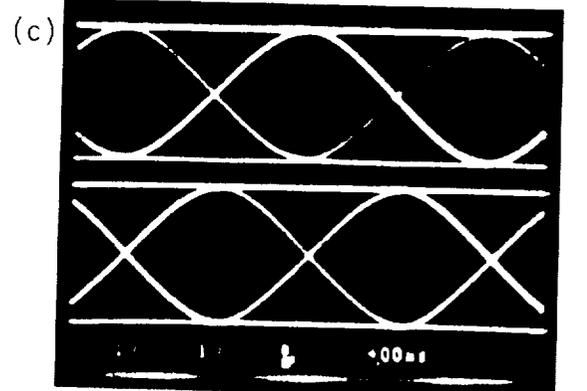
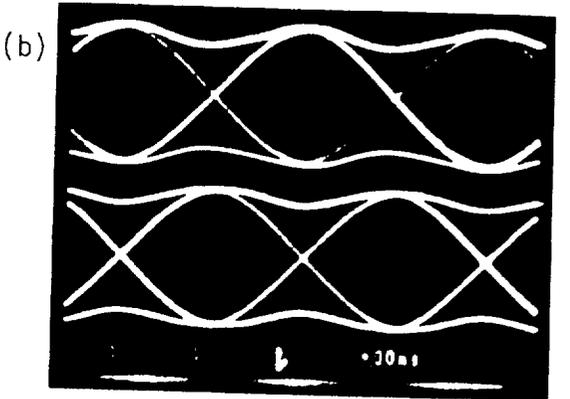
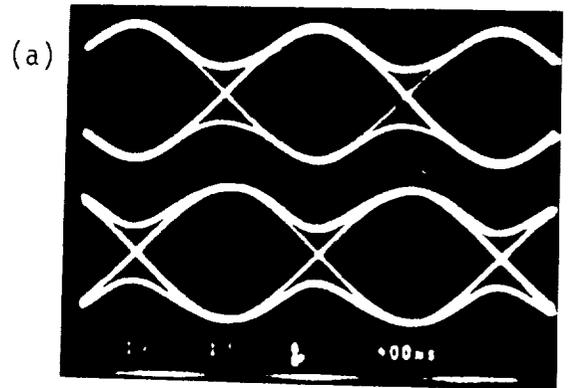
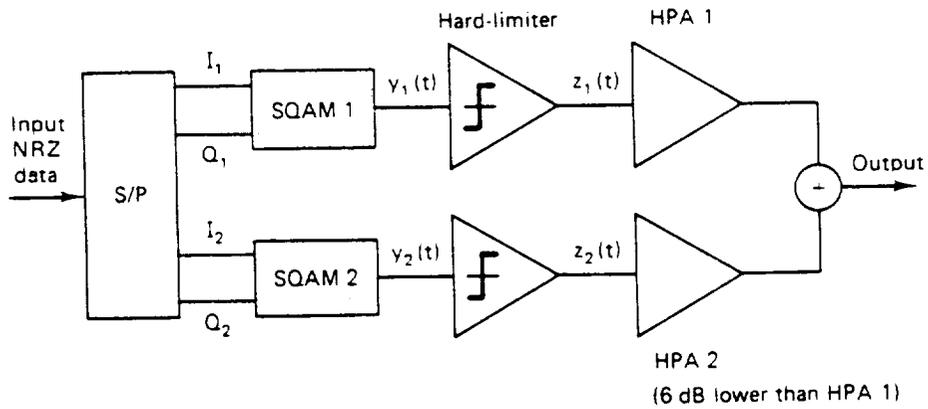


Figure 3 Experimental measured eye patterns (I- and Q-channel) of SQAM baseband signals of a 128-kb/s modem in a linear channel. (a) $A = 0.7$. (b) $A = 0.85$. (c) $A = 1.0$. These eye patterns were measured at the transmitter, prior to modulation (Vertical: 1 V/division; horizontal: 4 μ s/division.)



**HPA 1 and HPA 2 are operated in a saturation mode

Figure 4: Block diagram of 16-SQAM modulator

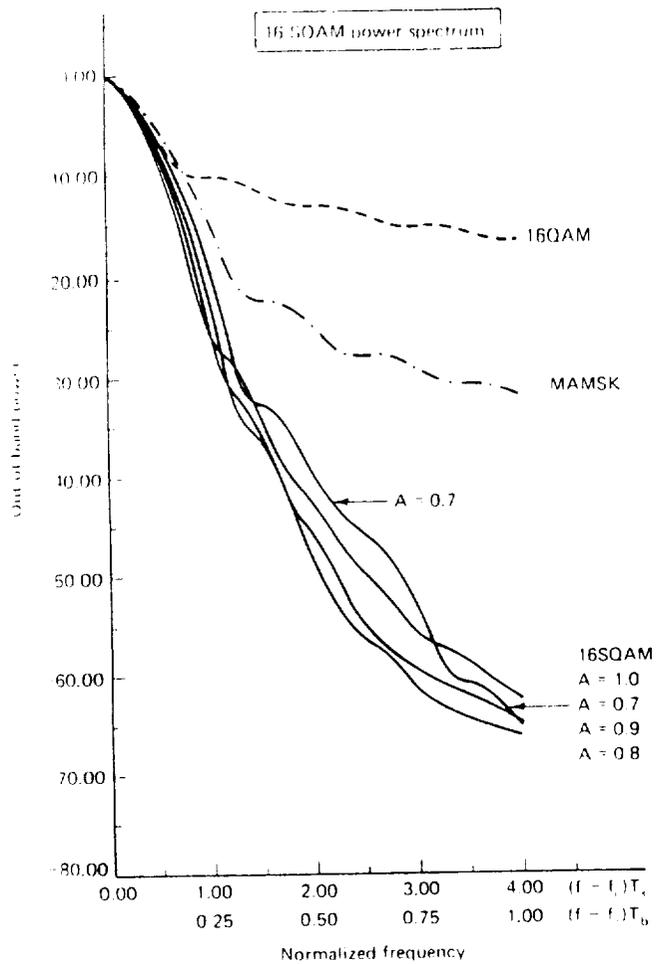


Figure 5: Out-of-band-to-total-power ratios of 16-SQAM, MAMSK and 16-QAM signals in a nonlinear (hard-limited) channel

NON-LINEAR PHASE FILTERS FOR DIGITAL SATCOM SYSTEMS

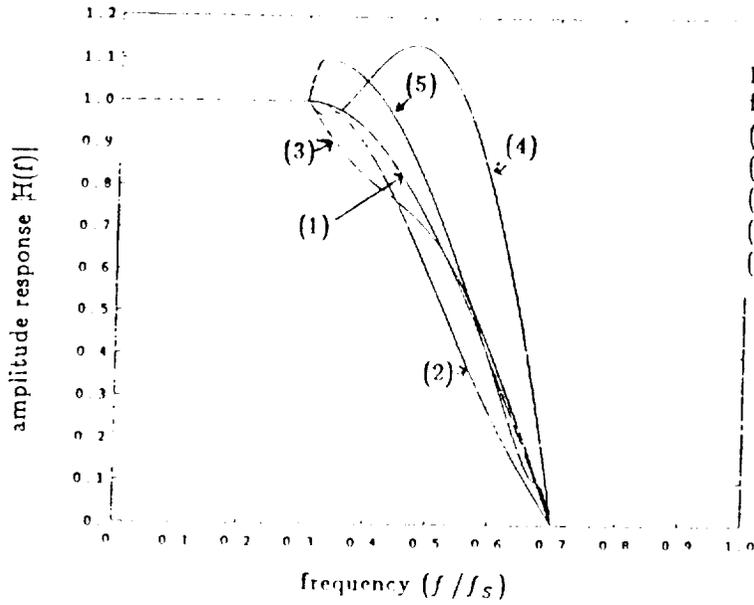


Figure 6 Amplitude responses of several nonlinear phase ISI-free filters using the following functions from Table I III. ($\alpha=0.4$ is assumed.)

- (1) $G_0(f), U_2(f), V_1(f)$
- (2) $G_0(f), U_2(f), V_2(f)$ ($b=0.3$)
- (3) $G_0(f), U_1(f)$ ($k=1$), $V_4(f)$ ($a=0.3, b=0.5$)
- (4) $G_0(f), U_1(f)$ ($k=1$), $V_3(f)$ ($a=4$)
- (5) $G_3(f)$ ($\beta=0.35, g=1.1$), $U_2(f), V_1(f)$

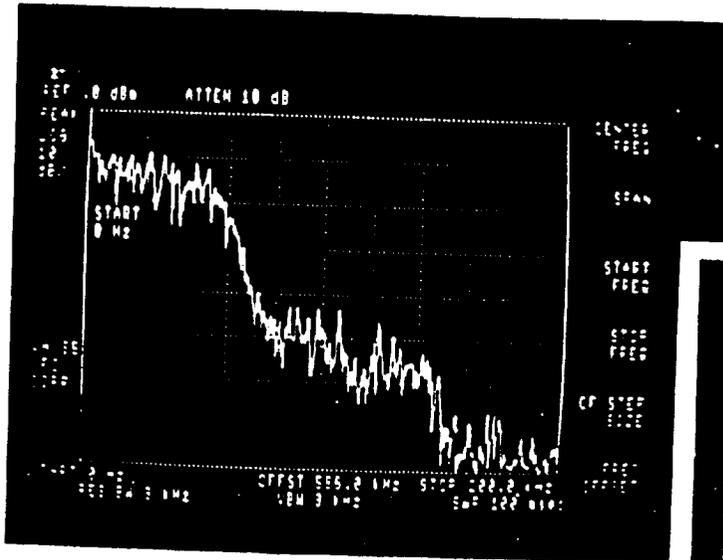


Figure 7 Power Spectral Density of the PRBS signals filtered by the filter in Figure 6. Bit rate = 100kb/s is used which corresponds to clock rate of 400kHz.

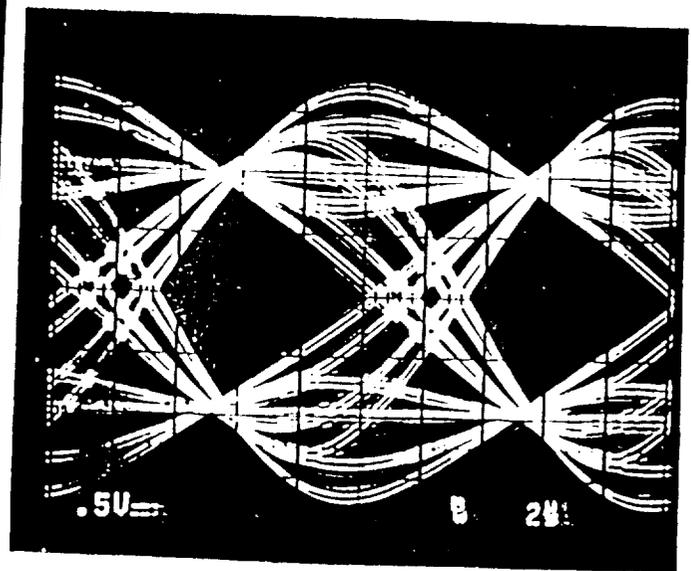


Figure 8 Eye diagram of the PRBS filtered by the filter in Figure 6. Bit rate = 100kb/s is used. Without noise

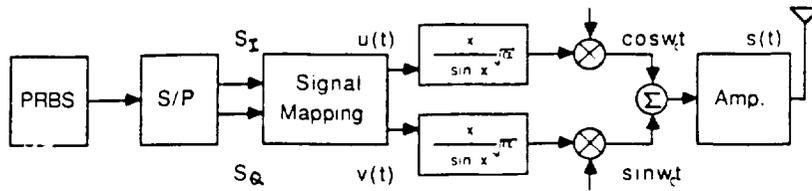


Figure 9: Block diagram of the transmitter of the $\pi/4$ -QPSK modem systems [2]

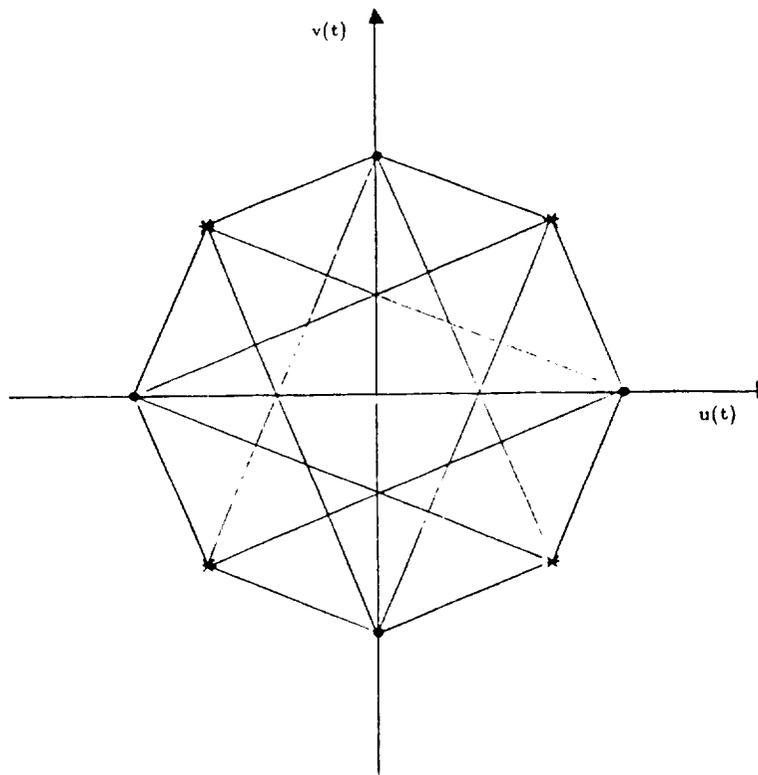


Figure 10 Possible phase states of the $\pi/4$ QPSK modulated carrier at sampling instants. The connections between two states indicate the possible phase transition.

* $T = 2nT_s$

. $t = (2n+1)T_s$

T_s : symbol duration

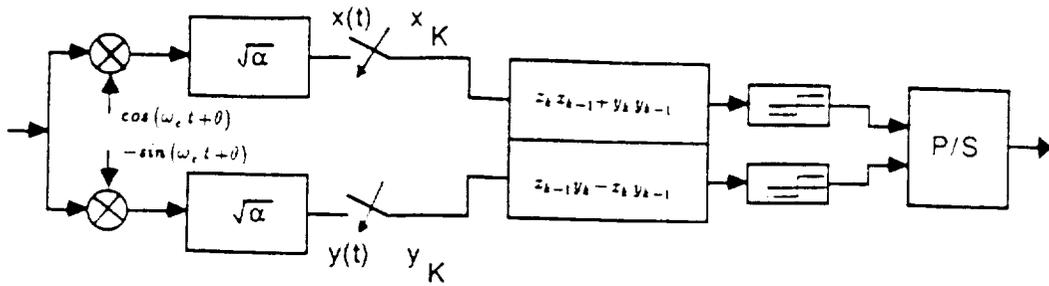


Figure 11: Block diagram of the baseband differential detector.

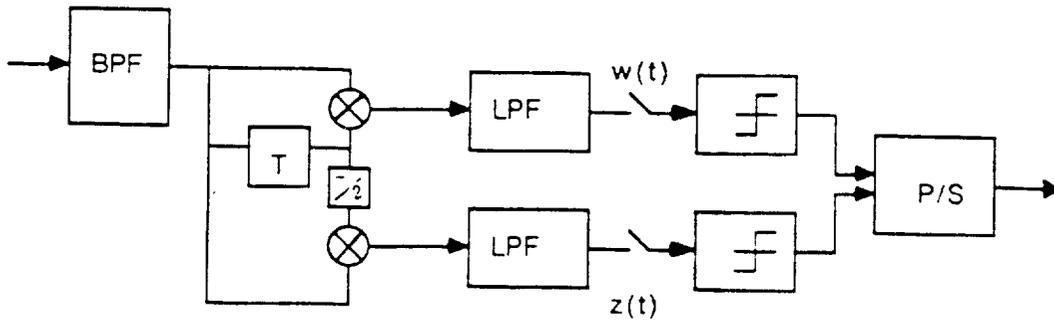


Figure 12: Block diagram of the IF band differential detector employing delay line and mixers.

BPF is assumed to have square-root raised-cosine roll-off.

LPF is assumed to be ideal brick-wall with $BW = 2(1+\alpha)f_N$

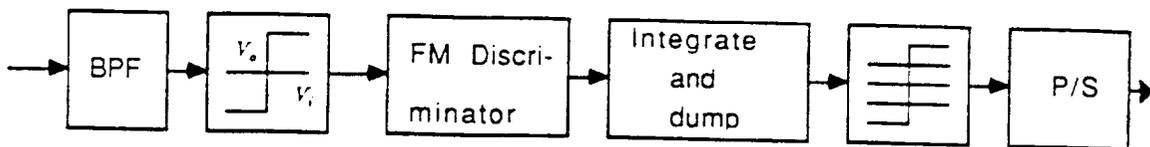


Figure 13: Block diagram of the FM-discriminator.

Module 2π is used in the threshold detector [2].

REFERENCES FOR THIS PRESENTATION

(Limit to two references)

- 1) K. Feher, Ed: "Advanced Digital Communications Systems and Signal Processing Techniques," Prentice-Hall, Englewood Cliffs, NJ 07632, 1987.
- 2) C. L. Liu, K. Feher: "Noncoherent Detection of $\pi/4$ -QPSK Systems in a CCI-AWGN Combined Interference Environment," Proc. of the IEEE-VTC-89, April 29-May 3, 1989 (pp. 83-94), San Francisco, CA, May 1989.



PROGRAMMABLE RATE MODEM UTILIZING DIGITAL SIGNAL PROCESSING TECHNIQUES
 (SBIR-PHASE 1 CONTRACT #NAS3-25336)

Arad Naveh
 TIW Systems, Incorporated
 Sunnyvale, California 94089

PROJECT SUMMARY

The engineering development study to follow was written to address the need for a Programmable Rate Digital Satellite Modem capable of supporting both burst and continuous transmission modes with either BPSK or QPSK modulation. The preferred implementation technique is an all digital one which utilizes as much digital signal processing (DSP) as possible. The majority of this report consists of outlining design trade-offs in each portion of the modulator and demodulator subsystem and of identifying viable circuit approaches which are easily repeatable, have low implementation losses and have low production costs.

TECHNICAL AREAS THAT WERE INVESTIGATED UNDER THIS CONTRACT:

- TRANSMIT DSP DATA FILTERS
- TRANSMIT CLOCK SYNTHESIS
- CARRIER SYNTHESIZER
- DEMODULATOR'S AUTOMATIC GAIN CONTROL
- RECEIVE DSP DATA FILTERS
- SATELLITE LINK RF OSCILLATOR PHASE NOISE IMPACT ON CARRIER RECOVERY OF PROGRAMMABLE RATE DIGITAL SATELLITE MODEMS
- MODEM FREQUENCY CONVERSION AND RECEIVE SIDE CARRIER SELECTION
- CARRIER RECOVERY
- TIMING RECOVERY AND DATA SAMPLING

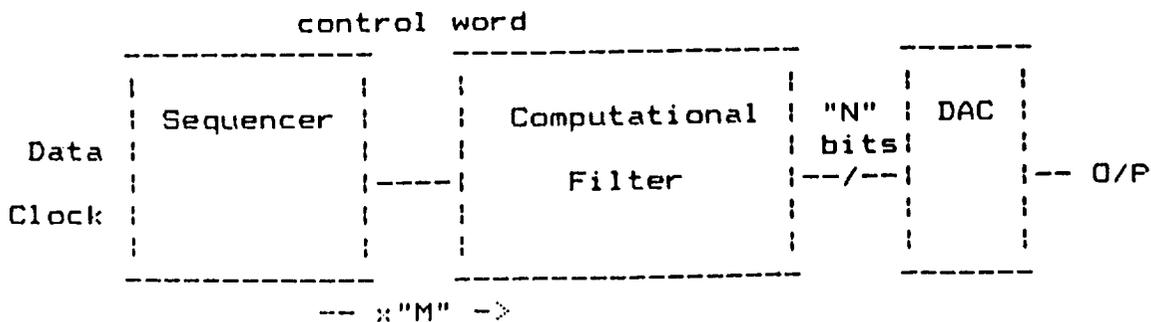


Figure 1. Transmit Data Filter Block Diagram

Table 1. Number of FIR Coefficients Verses Alpha Factor

Classical Alpha Factor	Normalized Transition Width	Number of Coefficients	Coefficients Phase Linear Requirement
1.0	.5	7.0	7
.9	.45	7.8	9
.8	.4	8.8	9
.7	.35	10.0	11
.6	.3	11.7	13
.5	.25	14.0	15
.4	.2	17.5	19
.3	.15	23.3	25
.2	.1	35.0	35
.1	.05	70.0	71

It is apparent by the data tabulated in Table 1 that as more restrictions are placed on the amount of excess bandwidth the DSP filter design must be capable of many more coefficients. It should be noted that Table 1 above is only an estimation and that depending on the values of the coefficients selected and the quantization level of the design that these estimates may need to be increased.

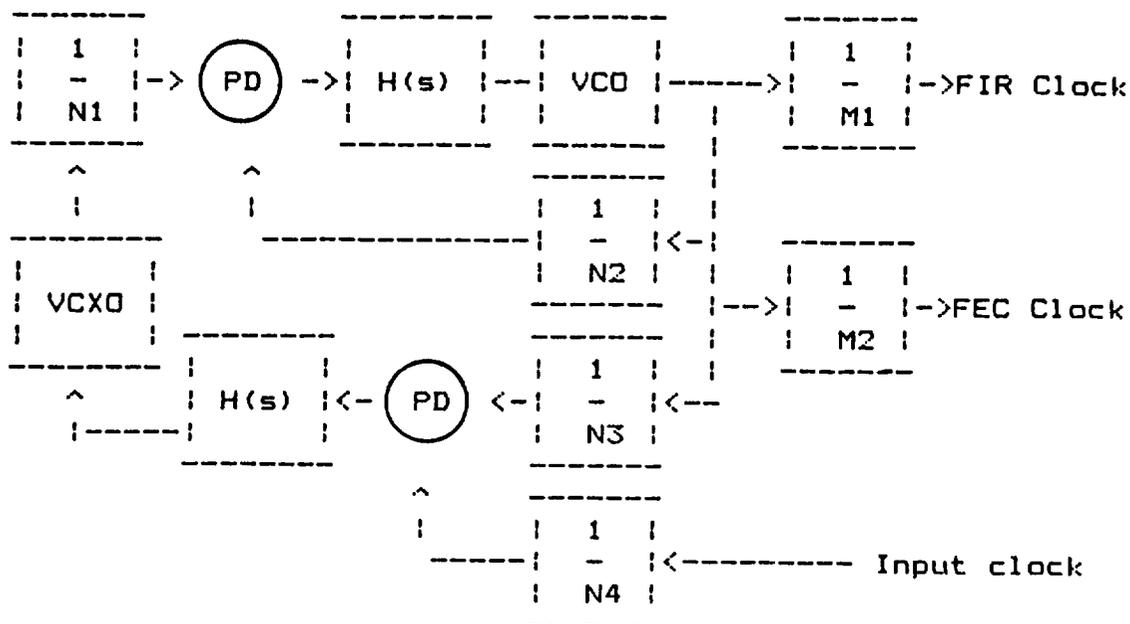


Figure 2. Multiloop Synthesizer for Clock Generation

SATELLITE LINK RF OSCILLATOR PHASE NOISE IMPACT ON CARRIER
RECOVERY OF PROGRAMMABLE RATE DIGITAL SATELLITE MODEM

The carrier recovery network used in coherent demodulation of BPSK/QPSK signals must have sufficient bandwidth to track the phase noise of the down link translated carrier to minimize performance degradations caused by RMS phase error jitter. On the other hand, the larger this bandwidth the less signal to noise improvement, i.e., the higher the thermal noise performance degradations at low E_b/N_0 's. Based upon these conflicting requirements a minimum carrier recovery bandwidth can be identified which is dependent on the RF frequency band used and the specific carrier recovery implementation. Once this bandwidth is identified, the respective lower data rate limit can be identified.

For Ku-Band (14/12 GHz) transmission INTELSAT documents IESS-308 and IESS-405 define worst case phase noise density masks for earth stations processing digital carriers with data rates up to 2048 KBS. Figures 5 and 6 depict these masks for the spacecraft and earth station frequency converters respectively. Also shown in Figure 5 is a plot of the composite satellite link. For K_A band operation (30/20 GHz) the composite phase noise density will be shifted higher by about 6-8 dB.

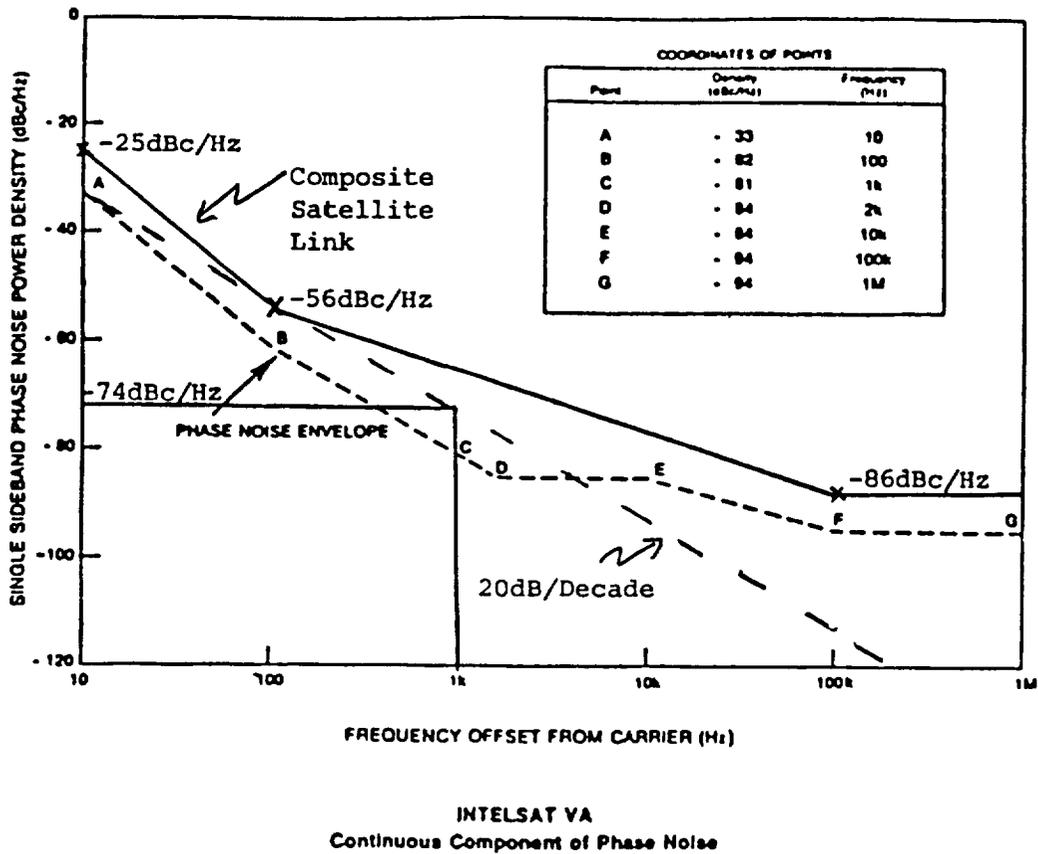
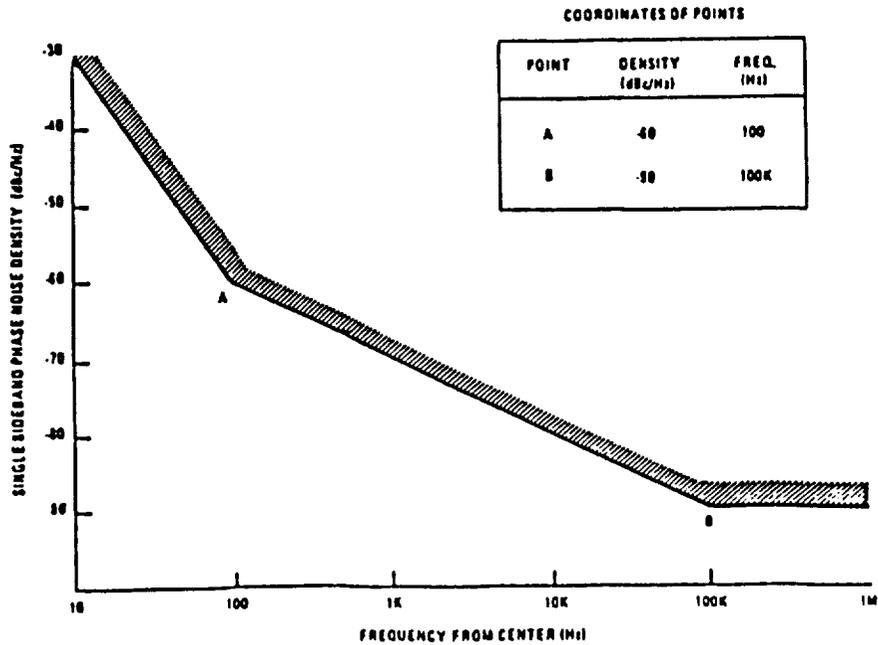


Figure 5



CONTINUOUS SINGLE SIDEBAND PHASE NOISE REQUIREMENT
(for carriers with information rates less than or equal to 2.048 Mb/s)

Figure 6

Table 2 from reference ⁽¹⁾ depicts the magnitude of tracking errors for a second order loop with 0.707 damping factor.

Table 2

**PHASE-LOCKED TRACKING OF PHASE NOISE FOR A
PHASE-LOCKED LOOP WITH DAMPING $\zeta = 0.707$,
AND NOISE BANDWIDTH $B_n = 0.53\omega_n$**

Type of Phase Noise	Phase-Noise Spectral Density	Phase Error — Second-Order Phase-Locked Loop, $\zeta = 0.707$ $\sigma_e^2 = \int_0^\infty \frac{\omega^4/\omega_n^4}{1 + (\omega/\omega_n)^4} G_p(f) df$
Frequency flicker noise	$\frac{k_a}{f^3}$	$\frac{k_a \pi^3}{\omega_n^2} = \frac{k_a \pi^3}{(1/0.53)^2 B_n^2} = \frac{8.71 k_a}{B_n^2}$
White frequency noise	$\frac{k_b}{f^2}$	$\frac{3.70 k_b}{B_n}$
White phase noise	$k_c, f < f_h$	$k_c f_h$

(1) "Digital Communications By Satellite" by James J. Spilker, Jr., 1977 Prentice Hall, Inc., (Pages 336 through 357).

Inspection of the composite satellite link phase noise spectral density shown in Figure 5 identifies K_A and K_C as follows:

$$K_A = \left(\text{Log}_{10}^{-1} \frac{-25\text{dB}}{10} \right) (10 \text{ Hz})^3$$

$$K_A = 3.16$$

and

$$K_C = \left(\text{Log}_{10}^{-1} \frac{-86\text{dB}}{10} \right)$$

$$K_C = 2.51 \times 10^{-9}$$

Since the plot shows a 10dB/decade not 20dB/decade rolloff between 100 Hz to 100 KHz, a worst case value of -74dBc/Hz at 1 KHz will be used to determine K_B since this value intersects the composite curve at the 100 Hz specification point.

TABLE 3

BN (Hz)	$\sigma_{\epsilon C}$			$\sigma_{\epsilon A}$	$\sigma_{\epsilon B}$	σ_{ϵ} TOTAL = RMS PHASE JITTER		
	$f_H = 25 \text{ KHz}$	$f_H = 50 \text{ KHz}$	$f_H = 100 \text{ KHz}$			$f_H = 25 \text{ KHz}$	$f_H = 50 \text{ KHz}$	$f_H = 100 \text{ KHz}$
10Hz	$7.9 \times 10^{-3} \text{ RAD}$	$1.12 \times 10^{-2} \text{ RAD}$	$1.58 \times 10^{-2} \text{ RAD}$	$5.2 \times 10^{-1} \text{ RAD}$	$1.2 \times 10^{-1} \text{ RAD}$	$5.3 \times 10^{-1} \text{ RAD}$ (30.6°)	$5.3 \times 10^{-1} \text{ RAD}$ (30.6°)	$5.3 \times 10^{-1} \text{ RAD}$ (30.6°)
100Hz	$7.9 \times 10^{-3} \text{ RAD}$	$1.12 \times 10^{-2} \text{ RAD}$	$1.58 \times 10^{-2} \text{ RAD}$	$5.2 \times 10^{-2} \text{ RAD}$	$3.8 \times 10^{-2} \text{ RAD}$	$6.5 \times 10^{-2} \text{ RAD}$ (3.7°)	$6.5 \times 10^{-2} \text{ RAD}$ (3.7°)	$6.63 \times 10^{-2} \text{ RAD}$ (3.8°)
200Hz	$7.9 \times 10^{-3} \text{ RAD}$	$1.12 \times 10^{-2} \text{ RAD}$	$1.58 \times 10^{-2} \text{ RAD}$	$2.6 \times 10^{-2} \text{ RAD}$	$2.7 \times 10^{-2} \text{ RAD}$	$3.83 \times 10^{-2} \text{ RAD}$ (2.2°)	$3.9 \times 10^{-2} \text{ RAD}$ (2.2°)	$4.0 \times 10^{-2} \text{ RAD}$ (2.3°)
500Hz	$7.9 \times 10^{-3} \text{ RAD}$	$1.12 \times 10^{-2} \text{ RAD}$	$1.58 \times 10^{-2} \text{ RAD}$	$1.0 \times 10^{-2} \text{ RAD}$	$1.7 \times 10^{-2} \text{ RAD}$	$2.1 \times 10^{-2} \text{ RAD}$ (1.2°)	$2.27 \times 10^{-2} \text{ RAD}$ (1.3°)	$2.53 \times 10^{-2} \text{ RAD}$ (1.45°)
1000Hz	$7.8 \times 10^{-3} \text{ RAD}$	$1.12 \times 10^{-2} \text{ RAD}$	$1.58 \times 10^{-2} \text{ RAD}$	$5.2 \times 10^{-3} \text{ RAD}$	$1.2 \times 10^{-2} \text{ RAD}$	$1.5 \times 10^{-2} \text{ RAD}$ (0.87°)	$1.72 \times 10^{-2} \text{ RAD}$ (0.99°)	$2.05 \times 10^{-2} \text{ RAD}$ (1.2°)
2000Hz	$7.6 \times 10^{-3} \text{ RAD}$	$1.09 \times 10^{-2} \text{ RAD}$	$1.58 \times 10^{-2} \text{ RAD}$	$2.6 \times 10^{-3} \text{ RAD}$	$8.6 \times 10^{-3} \text{ RAD}$	$1.18 \times 10^{-2} \text{ RAD}$ (0.67°)	$1.4 \times 10^{-2} \text{ RAD}$ (0.81°)	$1.82 \times 10^{-2} \text{ RAD}$ (1.04°)
5000Hz	$7.1 \times 10^{-3} \text{ RAD}$	$1.06 \times 10^{-2} \text{ RAD}$	$1.54 \times 10^{-2} \text{ RAD}$	$1.0 \times 10^{-3} \text{ RAD}$	$5.4 \times 10^{-3} \text{ RAD}$	$9.0 \times 10^{-3} \text{ RAD}$ (0.51°)	$1.2 \times 10^{-2} \text{ RAD}$ (0.68°)	$1.6 \times 10^{-2} \text{ RAD}$ (0.94°)
10000Hz	$6.1 \times 10^{-3} \text{ RAD}$	$1.00 \times 10^{-2} \text{ RAD}$	$1.50 \times 10^{-2} \text{ RAD}$	$5.2 \times 10^{-4} \text{ RAD}$	$3.8 \times 10^{-3} \text{ RAD}$	$7.2 \times 10^{-3} \text{ RAD}$ (0.41°)	$1.07 \times 10^{-2} \text{ RAD}$ (0.61°)	$1.55 \times 10^{-2} \text{ RAD}$ (0.89°)

TABLE 3

RMS TRACKING PHASE JITTER BETWEEN
RECOVERED CARRIER AND PSK SIGNAL
VERSUS BN (PLL NOISE BANDWIDTH)

MODULATOR IMPLEMENTATION

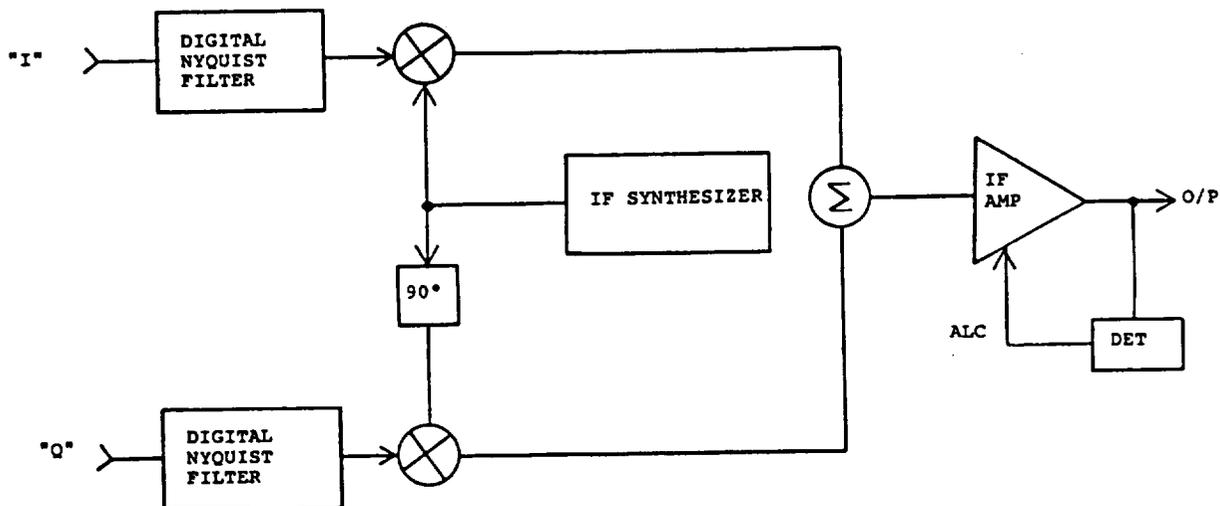


Figure 7a. Functional Block Diagram of Direct QPSK Modulator

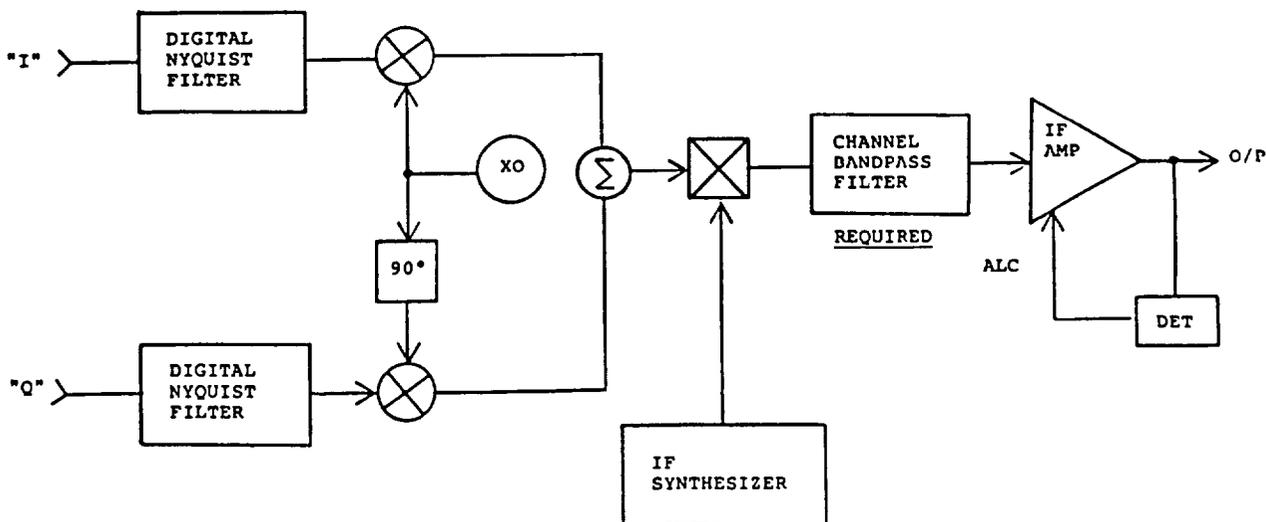


Figure 7. Functional Block Diagram of Frequency Translated QPSK Modulator

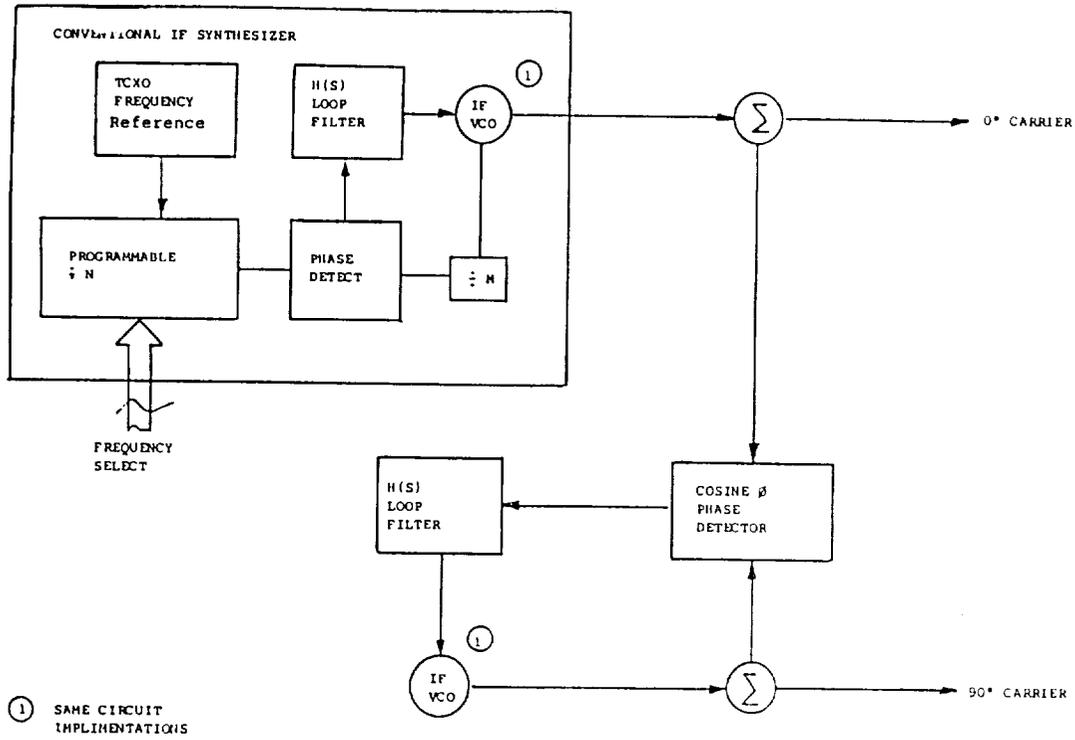


FIGURE 8
BROADBAND QUADRATURE
LOCAL OSCILLATOR GENERATOR

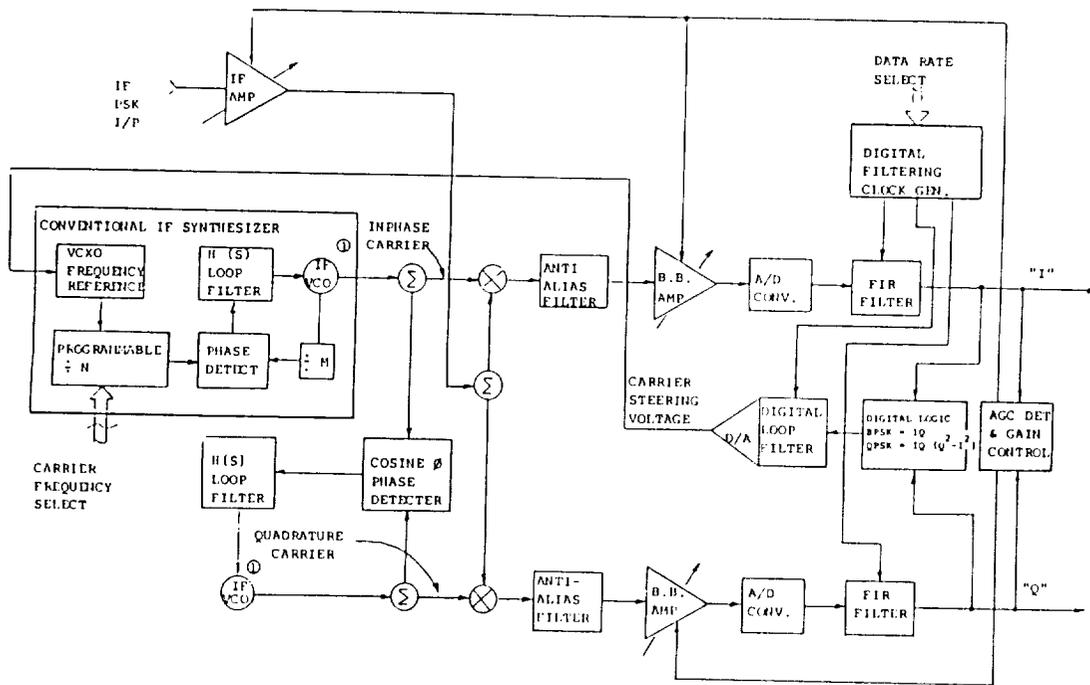


FIGURE 9
PROPOSED SIMPLIFIED BLOCK DIAGRAM
OF DIRECT DEMODULATION TECHNIQUE

CARRIER RECOVERY

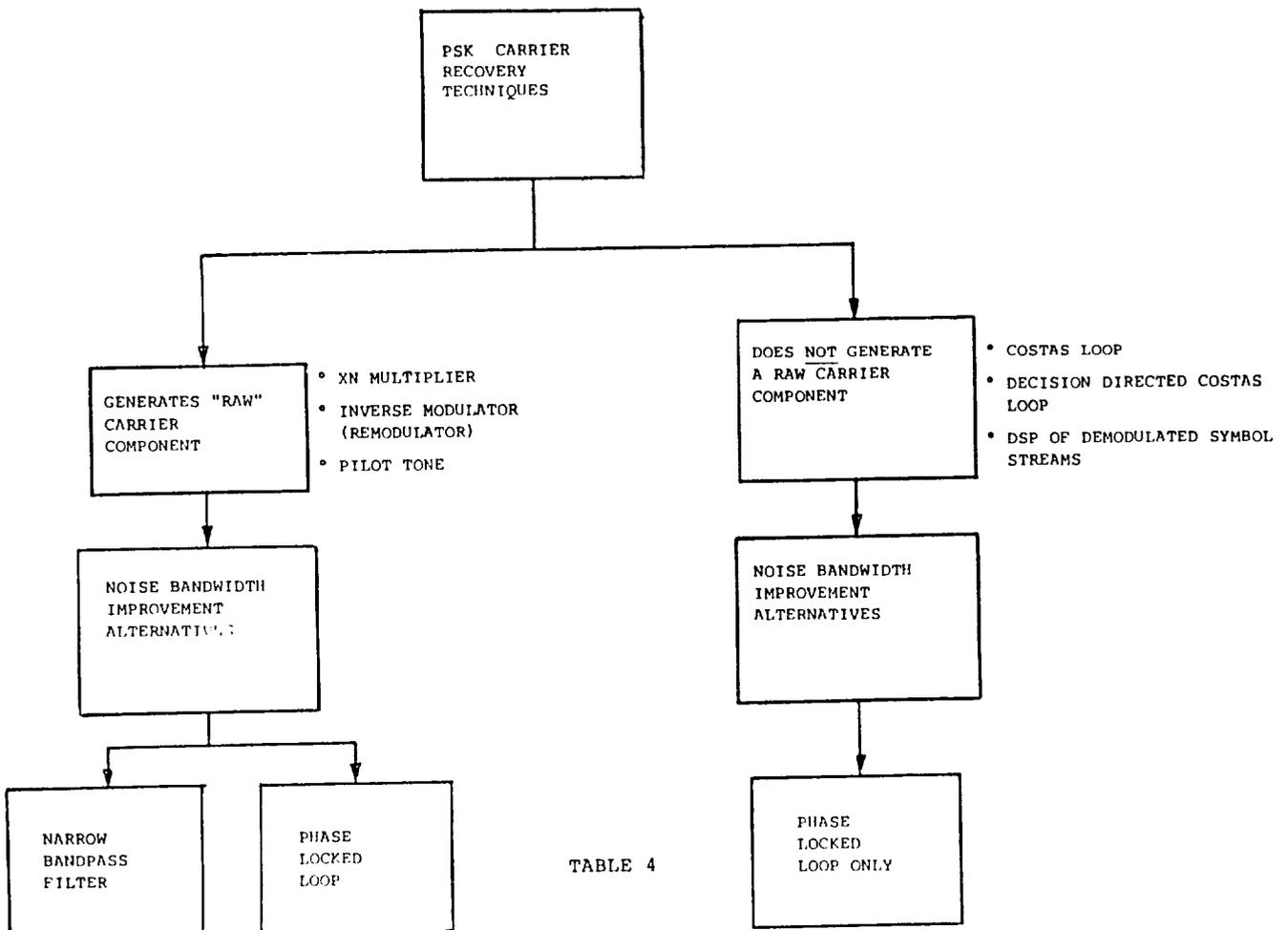
INTRODUCTION

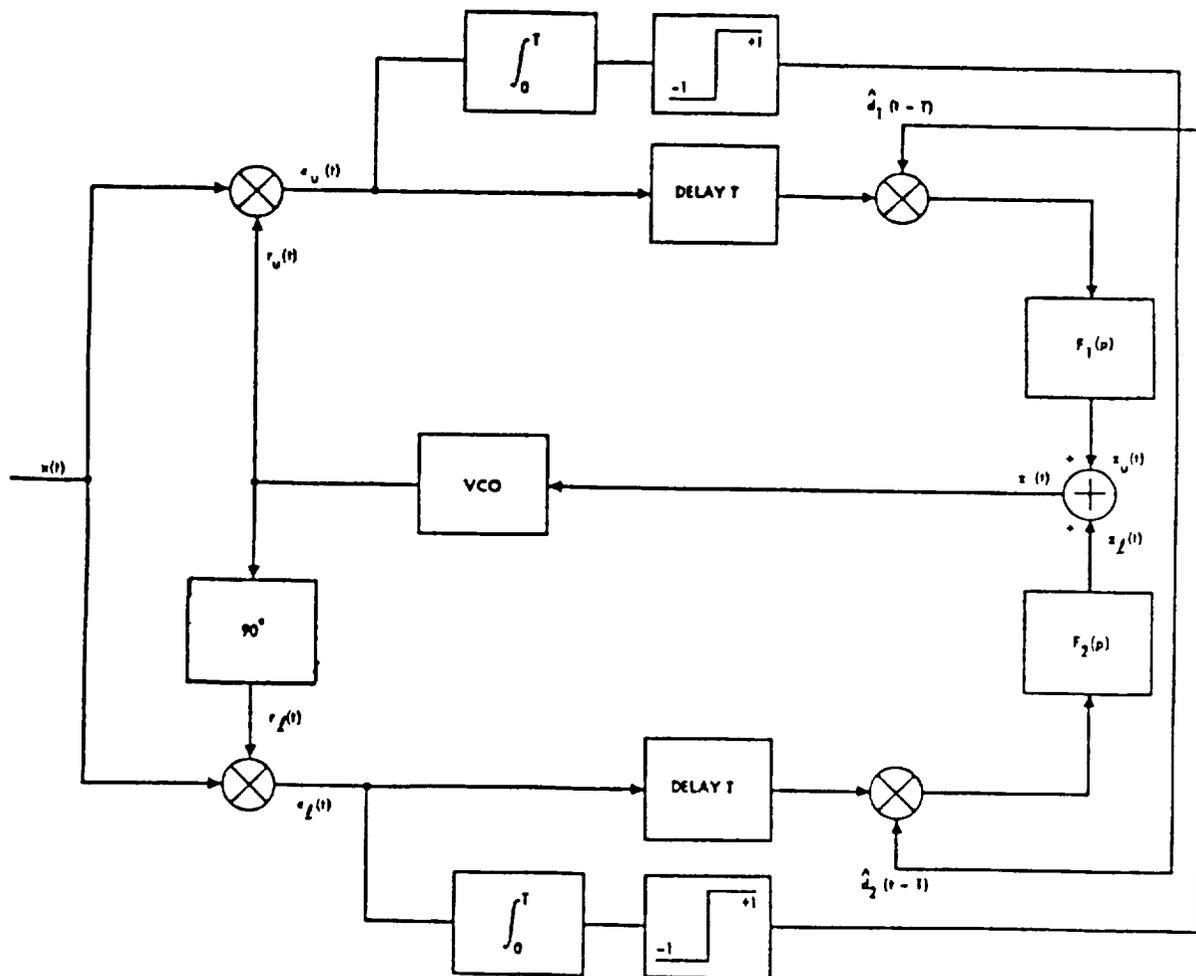
In general, Digital Satellite Modems are characterized by providing the lowest possible Bit Error Rate (BER) for a given Bit Energy per Noise Density (E_b/N_0). Typically these modems are implemented with robust BPSK or QPSK Modulation and high overhead Forward Error Correction such that error-less performance can be realized over the satellite link which is characterized with high noise.

In order to support this objective, these digital modems utilize Coherent Demodulation and optimum detection with low implementation losses. Coherent Demodulation is accommodated by multiplying the received PSK signal with a locally generated recovered carrier replica. This recovered carrier replica must have sufficient noise improvement quality and precise phase alignment with the specific PSK modulated signal being processed in order to support low implementation loss BER degradation. Since PSK is a suppressed carrier type of modulation, some type of non-linear signal processing is necessary to regenerate a coherent carrier reference. This process is the topic of this memo and is referred to as "Carrier Recovery".

We initiate our effort in this study area by assessing current and proposed Carrier Recovery schemes which are viable candidates for BPSK and QPSK Modulation. Next, we turn our attention towards the specific requirements of the work study, i.e., a Carrier Recovery implementation which:

- 1) Supports Programmable Data Rates;
- 2) Operates with BPSK or QPSK Modulation;
- 3) Supports both Burst and Continuous Modes of Operation;
- 4) Minimizes the constraints on Clock Recovery/Bit Synchronization;
- 5) Allows for digital filtering techniques prior to data detection;
- 6) Can be implemented with Digital Signal Processing Techniques as compared to Analog Signal Processing; and
- 7) Is viable in satellite communications.





Decision-Directed 4th Order Costas Loop with Integrate and Dump Filtering

Figure 12

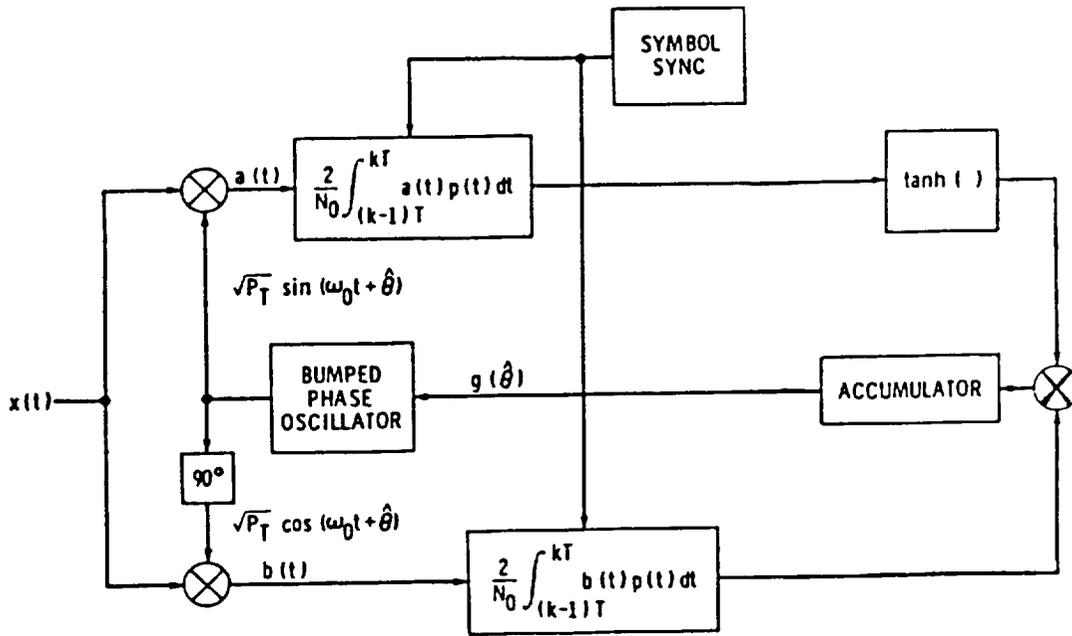


Figure 13a. The MAP Estimation Loop for Carrier Phase (BPSK)

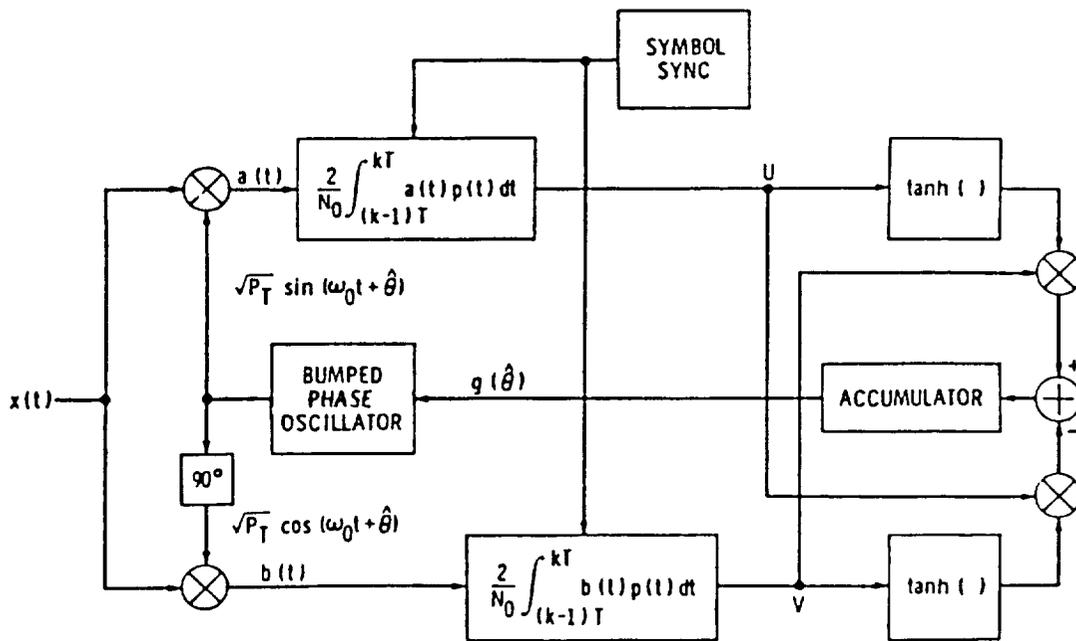


Figure 13b. The MAP Estimation Loop for Carrier Phase (QPSK)

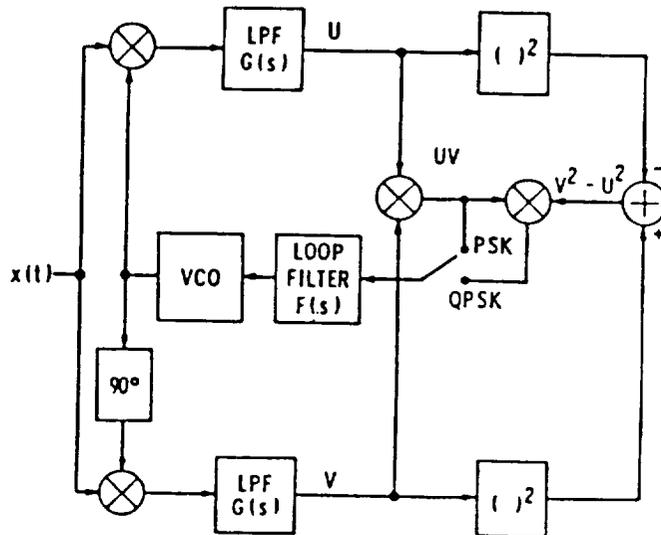


Figure 14. A Practical Realization of the MAP Estimation Loop, Passive Arm Filters, Small SNR

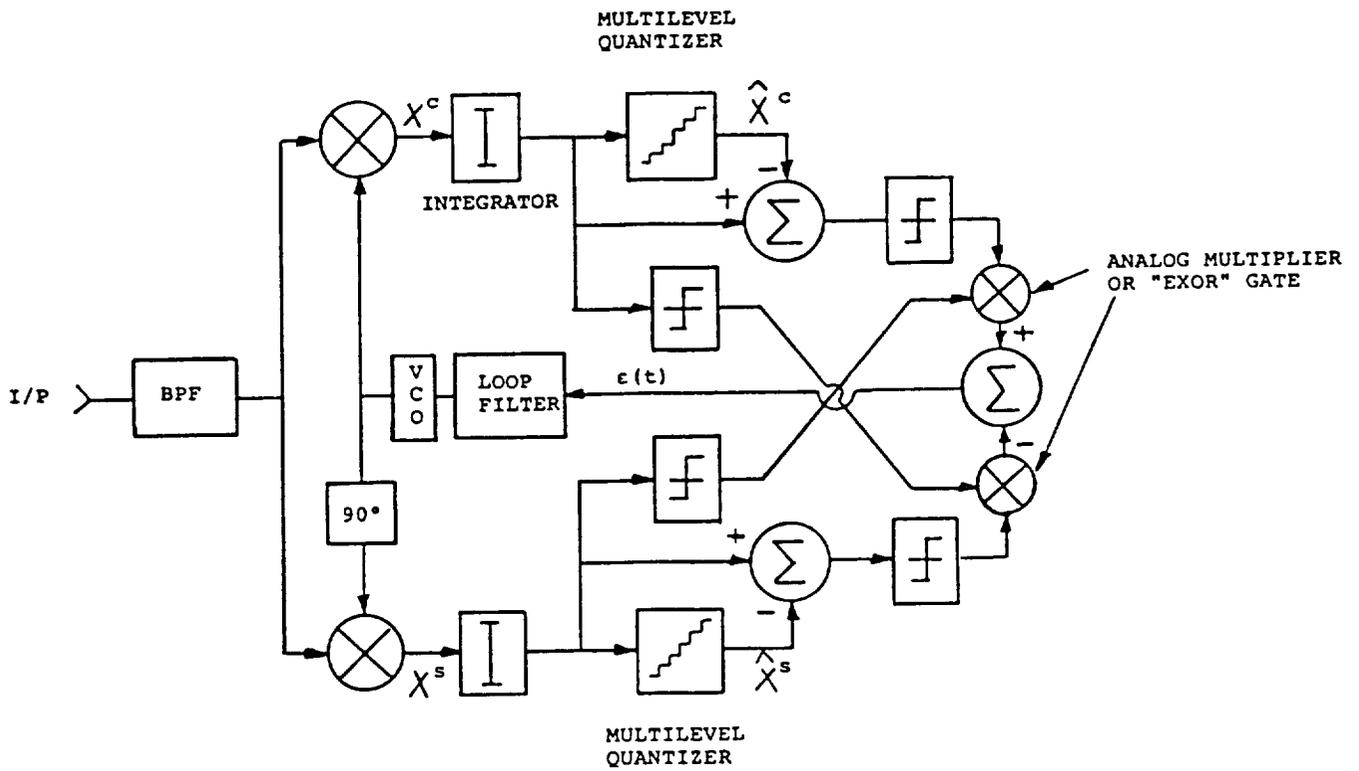


Figure 15. Block Diagram of the Carrier Recovery with Selective Gated PLL

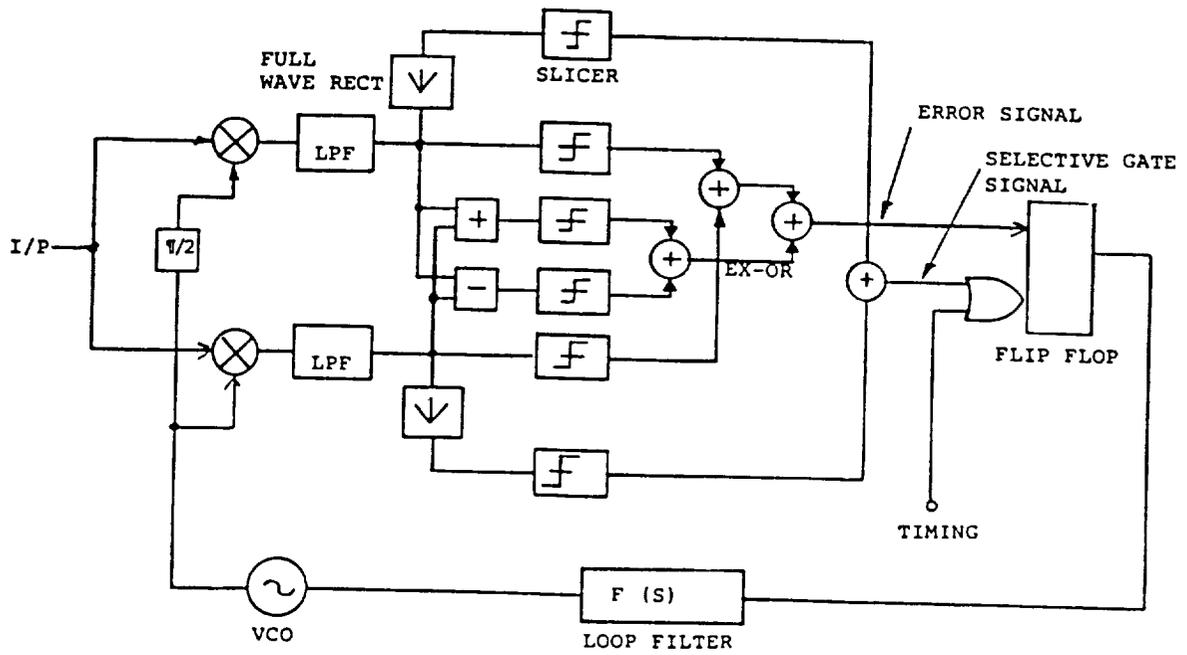


Figure 16. Proposed Carrier Recovery Loop Diagram

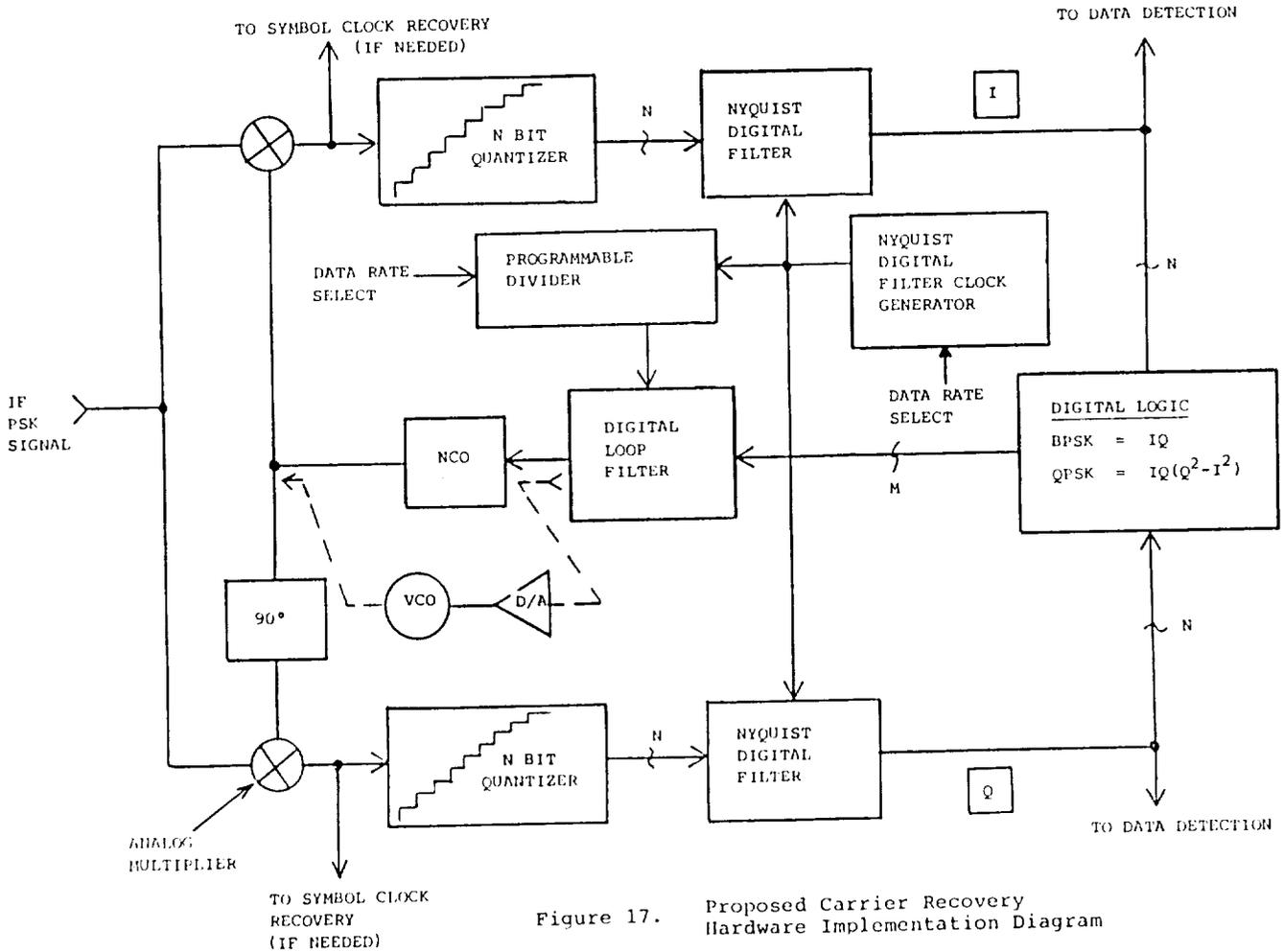


Figure 17. Proposed Carrier Recovery Hardware Implementation Diagram

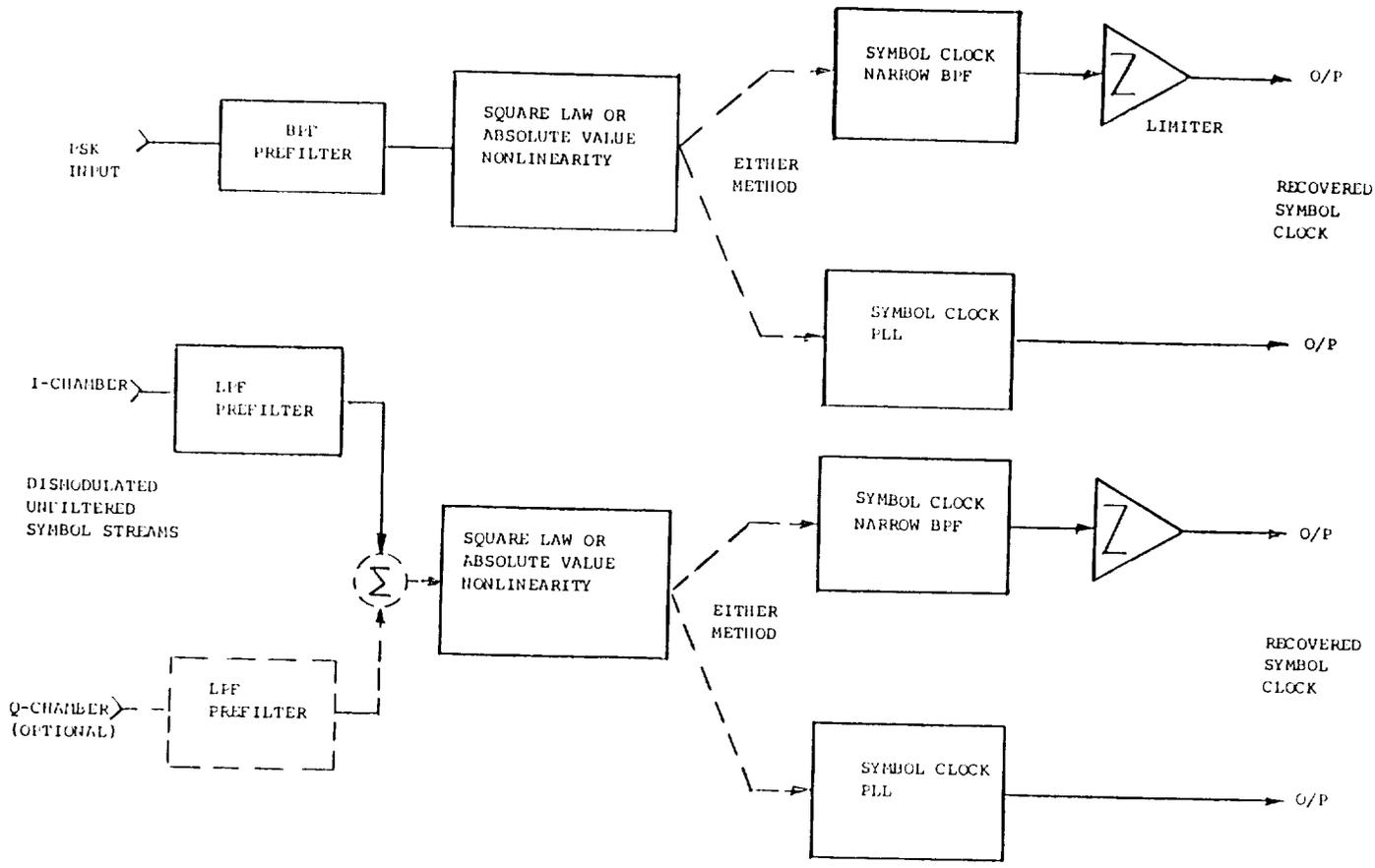
TIMING RECOVERY AND DATA SAMPLING

INTRODUCTION

The objective of this section is to identify the most favorable Timing Recovery Technique and its performance attributes which can be utilized by a Programmable Data Rate Digital Satellite Modem operating in a Multi-Carrier Transponder environment. We initiate our discussion by identifying the various types of Timing Recovery Techniques which are described in technical literature and used in digital communications. The operational characteristics and features of each Timing Recovery Scheme will be presented and a comparison to the study requirements will be made.

A candidate scheme will then be chosen based upon the one which offers the most favorable attributes. The performance impact of the candidate Timing Recovery Scheme on Soft Decision Data Sampling (detection) will also be assessed.

Lastly, viable hardware design techniques which utilize DSP Technology will be described for the various functions required in the implementation of the technique. This is concluded with an overall implementation diagram of the proposed Hardware Timing Recovery approach.



LPF - LOW PASS FILTER
 BPF - BANDPASS FILTER
 PLL - PHASE LOCKED LOOP

Figure 18

"SQUARE LAW"/"ABSOLUTE VALUE"
 NONLINEARITY
 TIMING RECOVERY SCHEMES

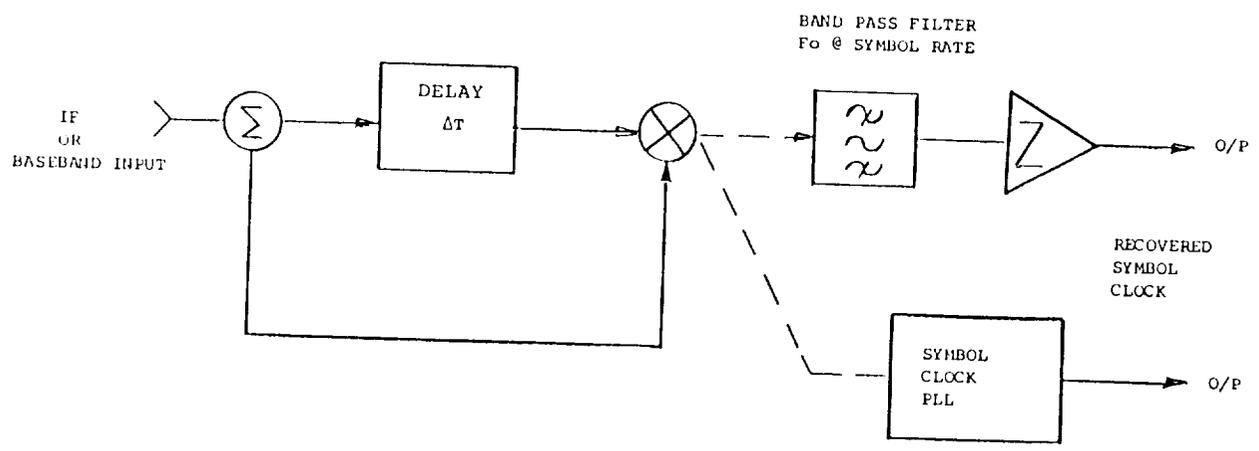


Figure 19

DELAY-LINE DETECTOR
 FUNCTIONAL BLOCK DIAGRAM

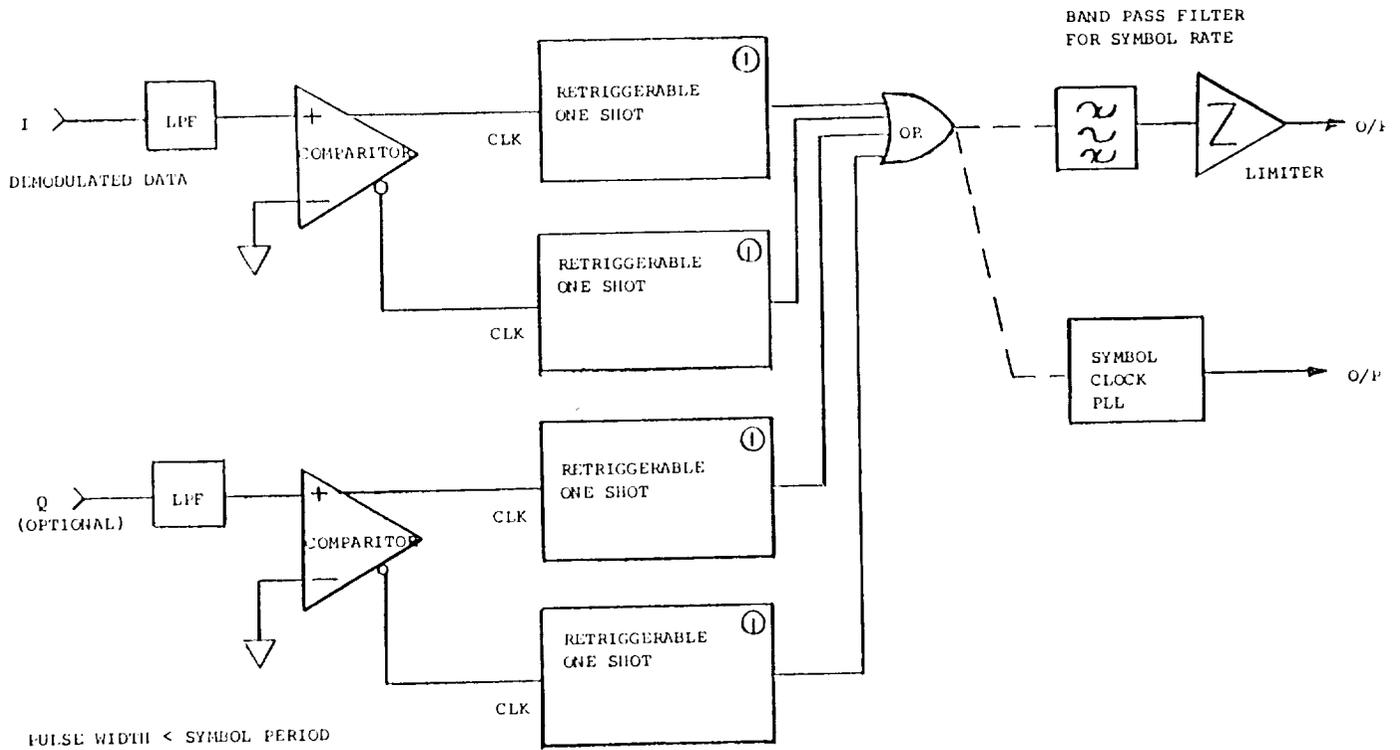


Figure 20
ZERO CROSSING DETECTOR
TIMING RECOVERY TECHNIQUE

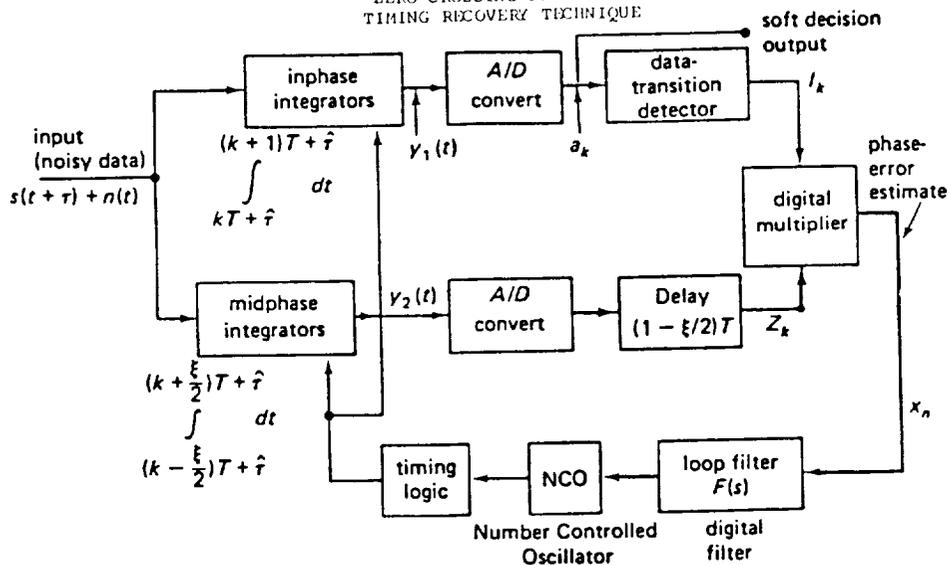


Fig. 8 In-phase/Mid-phase bit synchronizer with inphase and midphase channels. The input clock offset is τ , and the clock phase estimate is \hat{t} . The midphase integrator window width is ξT sec. The timing error is $\epsilon \triangleq \tau - \hat{t}$.

Figure 21

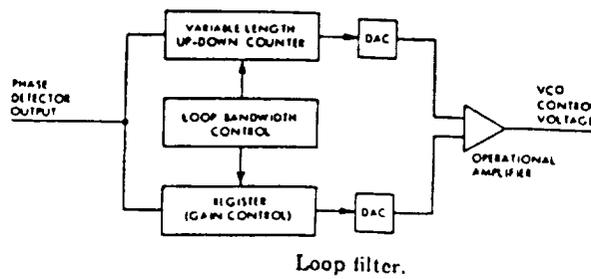
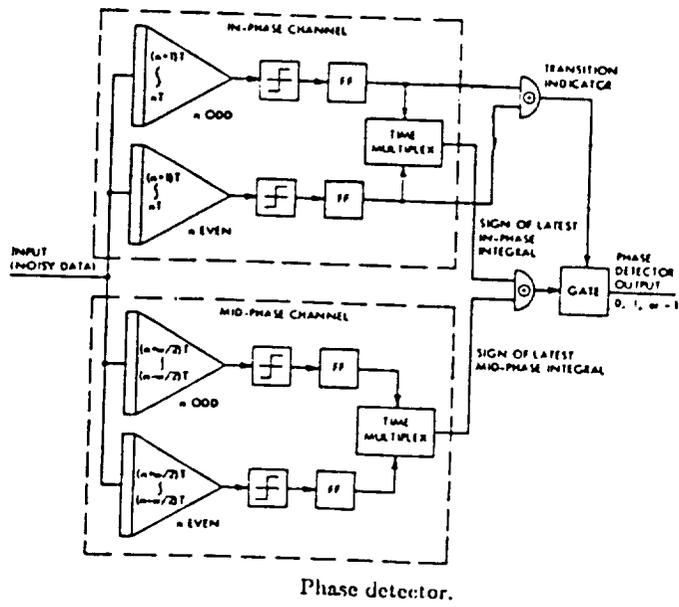
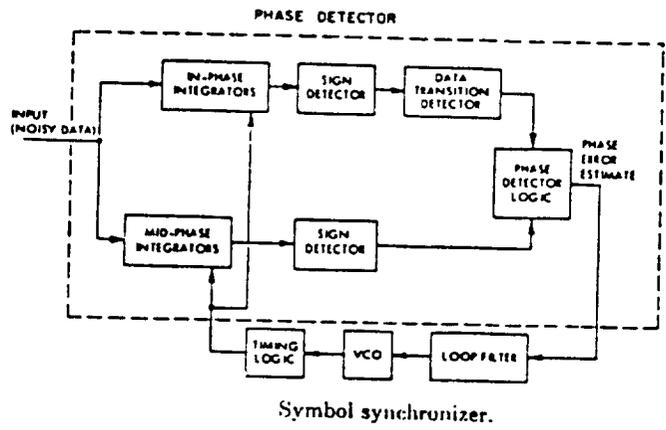
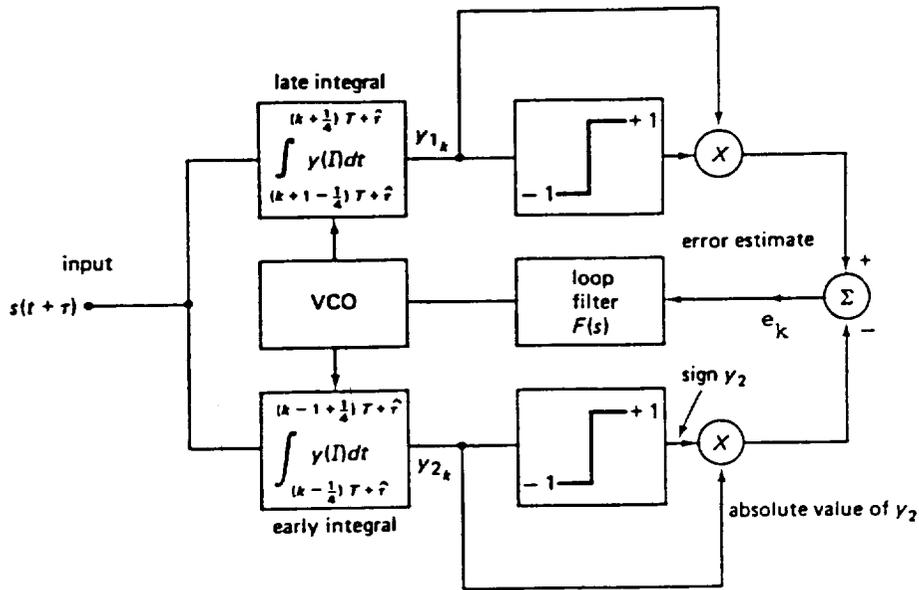
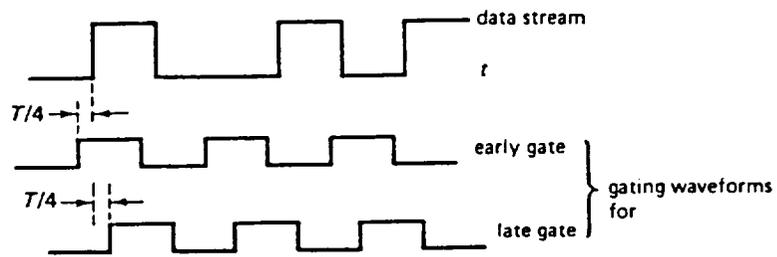


Figure 22

PRACTICAL IMPLEMENTATION OF DIGITAL TRANSITION TRACKING SYMBOL SYNCHRONIZER FROM REFERENCE 9



(a)



(b)

NOTE

$\Delta_0 T = \frac{T}{4}$
Shown

Block diagram and waveforms for an absolute-value early-late-gate bit synchronizer. (a) Block diagram; the $T/4$ overlap used can be shown to be optimum. (b) Waveforms for $\hat{\tau} = \tau$

Figure 23

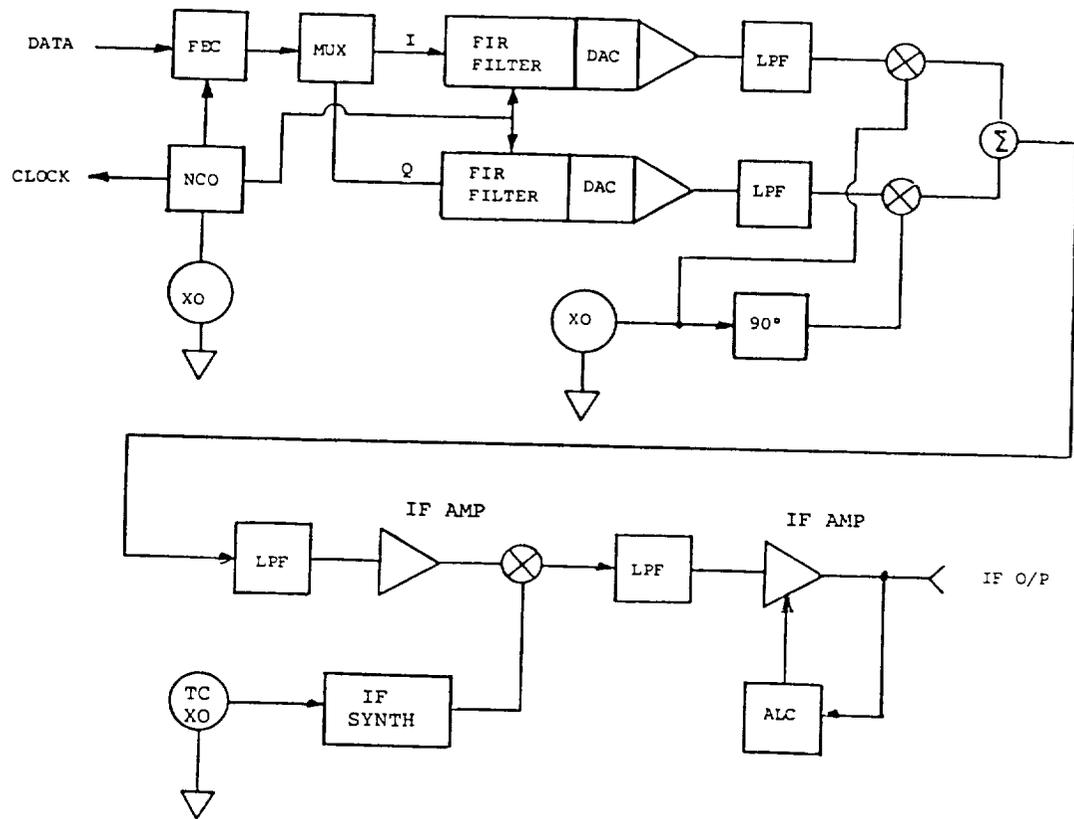


Figure 24

PROPOSED VARIABLE RATE MODULATOR BLOCK DIAGRAM

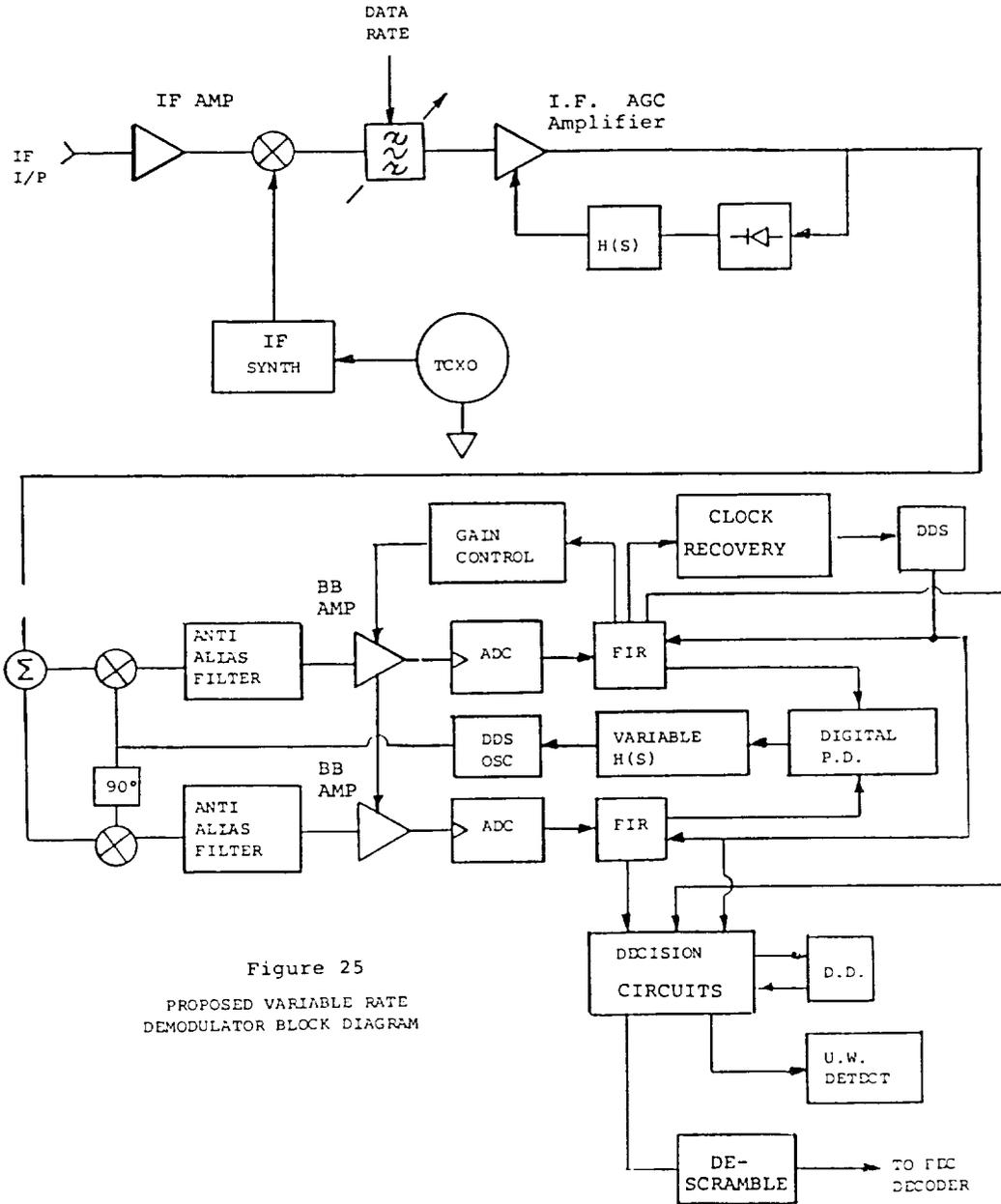


Figure 25
PROPOSED VARIABLE RATE
DEMODULATOR BLOCK DIAGRAM

The overall Block Diagrams of the modulator and demodulator suggested are:

Figure 24: PROPOSED MODULATOR

Figure 25: PROPOSED DEMODULATOR

N 9 2 - 2 2 0 1 2

MULTI-USER SATELLITE COMMUNICATIONS SYSTEM
USING AN INNOVATIVE COMPRESSIVE RECEIVER

Edward J. Staples
Amerasia Technology, Incorporated
Westlake Village, CA 91361

ABSTRACT

There is a need for an on-board simultaneous multi-channel demodulation system for a satellite communications system. Studies indicate that Convolve-Multiply-Convolve (CMC) filtering with surface acoustic wave (SAW) dispersive delay lines will eliminate the necessity of on-board satellite channelized filters or complex Fourier transform processors. The reason for choosing the CMC technique is its ability to perform Fourier transformations in a shorter time with less space and power consumption than digital Fourier transform processors.

Each ground terminal in this multi-users communications system is remotely located and operates independently, and hence a method of synchronizing the transmission of these users is presented which utilizes the existing Global Positioning Satellite (GPS) system. Each ground user is equipped with a low cost ground terminal that has a synchronization subsystem attached to it.

The system design of an on-board Multi-channel Receiver and Demodulator utilizes Quadrature Phase Shift Keying (QPSK) as the modulation technique. This technique provides the best figure of merit, i.e. the lowest transmitter power requirement per communication channel.

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INTRODUCTION

On-board satellite receiver/demodulators for multi-channel Frequency Shift Keyed (FSK) transmission require many narrowband filters to isolate each user's channel. When the requirement is for one hundred or more channels the problem becomes physically impossible. Also, since the users are at many different locations a system is required to synchronize the time of transmission of each user. A Convolve-Multiply-Convolve [Ref. 1] technique for simultaneous demodulation and regeneration of the transmitted FSK is under investigation. The implementation of this technique would eliminate the necessity of on-board satellite channelized filters. Synchronization is achieved by a processor that establishes the users position and timing with respect to the communications satellite by the use of timing signals broadcast from the Global Positioning Satellite (GPS) [Ref. 2] system as illustrated in Figure 1.

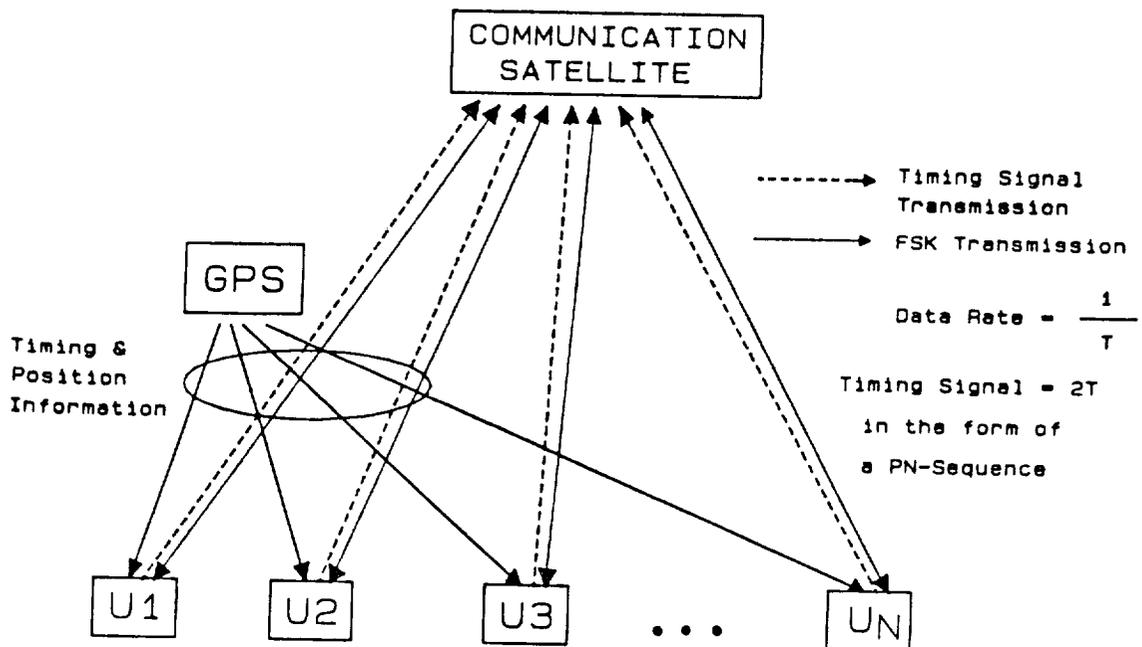


Figure 1- Communication network configuration under study.

Figure 2, illustrates the time/frequency diagram on-board the communications satellite where the timing signal is recovered on the satellite. N users are shown, each employing quaternary FSK (frequency shift keyed) modulation. Therefore, each user is assigned four frequencies within the transponder bandwidth and transmits two of the four at any instant in time. If the data rate of the message is $1/T$, T being the bit period, then the dwell time for each pair of frequencies is $2T$. In the C-M-C transform configuration a frequency expander is used. The frequency expander has a sweep time of $4T$ as shown in the figure.

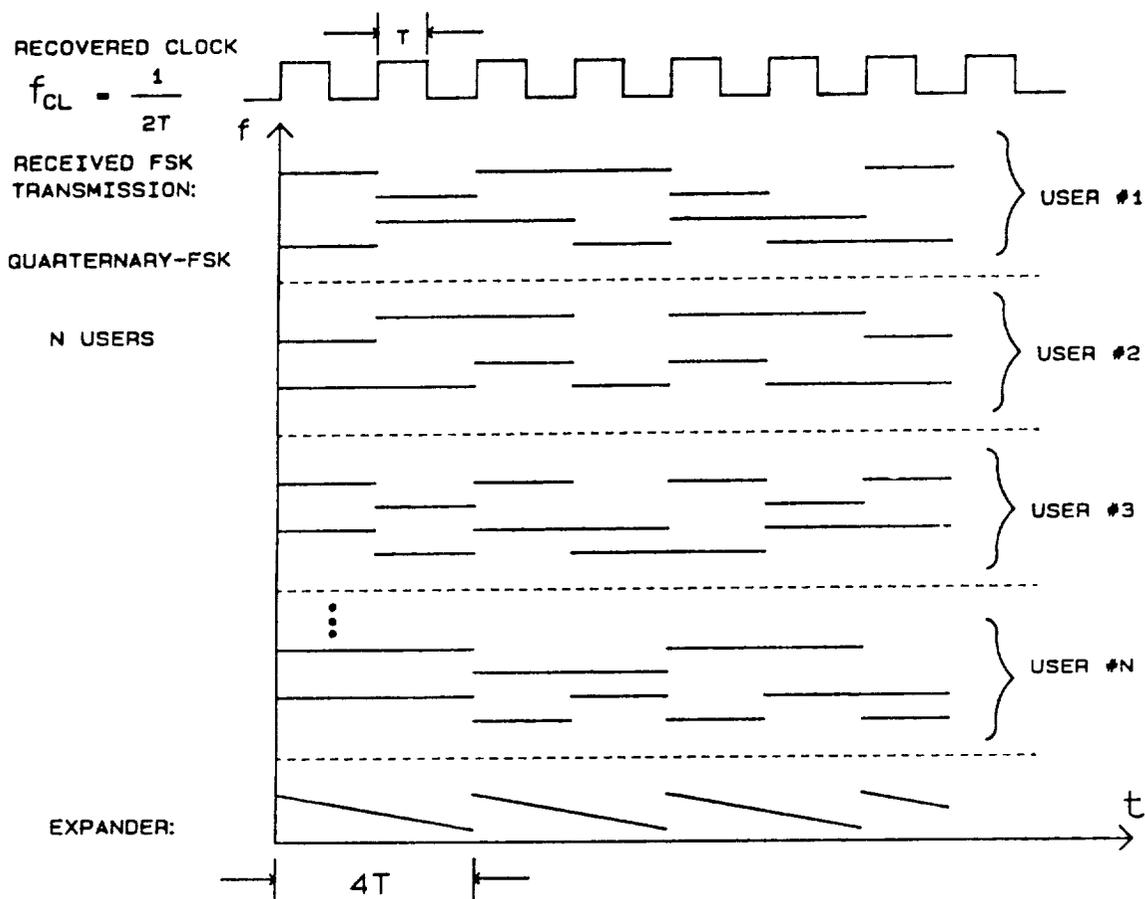


Figure 2- Frequency Time Diagram.

RECEIVER/DEMODULATOR

The basic receiver/demodulator system diagram is shown in Figure 3. The incoming signal is split into two parallel processors. One part is filtered to extract the timing signal. The timing recovery processor outputs three synchronous timing signals, that is, at the FSK symbol rate, data bit rate, and at M times the symbol rate. A timing adjust circuit is incorporated to compensate for any propagation delay difference in the two processors. The second part of the signal is processed by the C-M-C transform processor followed by the decision circuit. The front end of the C-M-C transform processor is a differential delay device (SAW), which has a delay property inversely proportional to the frequency of the input signal. A mixer is used to perform frequency multiplication between the received signal and the expander. This produces pulses corresponding to each incoming frequency. The pulses are aligned in time proportional to each frequency. This process periodically repeats every $2T$ seconds, and within each $2T$ interval all the data are time multiplexed to form a composite data stream.

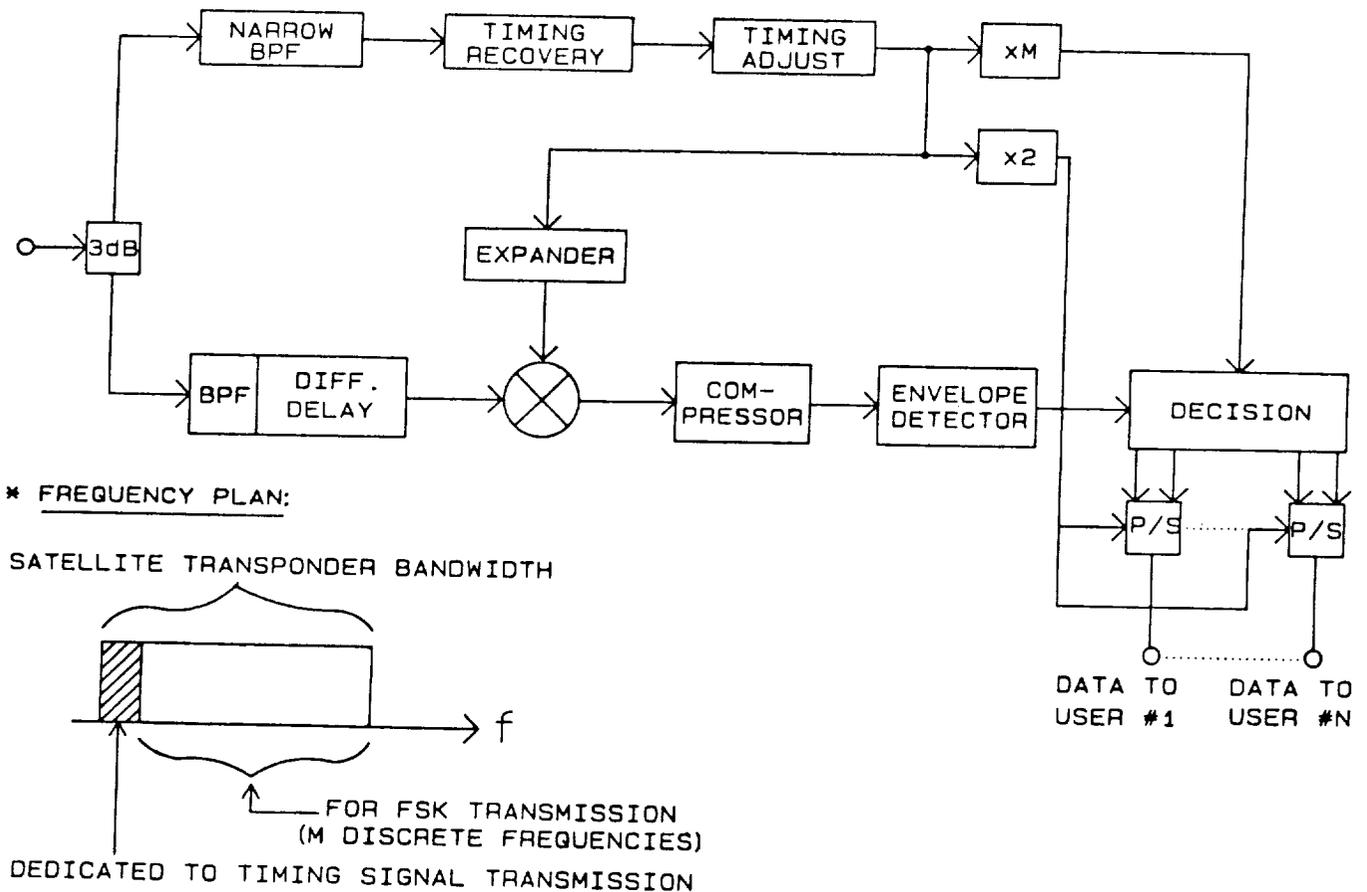


Figure 3-Receiver/Demodulator system.

The system design parameters are as follows:

- | | |
|---|-----------------|
| a. Number of users: | 200 |
| b. Type of modulation: | Quarternary FSK |
| c. Frequency separation: | 50 KHz |
| d. Data transmission rate: | 50 Kbps |
| e. Input frequency range: | 80 to 120 MHz |
| f. Number of simultaneous transmission frequencies: | 800 |

The ground based quarternary FSK transmitter transmits the data at the rate of 50 Kbps, hence the data bit period T is equal to 20 microseconds. This data bit stream is split into an "odd" and "even" data stream with a symbol period of $2T=40$ microseconds. Each symbol of the "odd" data stream is assigned a frequency, i.e. f_1 for "mark" and f_2 for "space". Similarly f_3 and f_4 are assigned to represent a "mark" or "space" respectively. Prior to transmission, the "odd" data stream is delayed by T with respect to the "even" data stream. Consequently, during the transmission of a symbol period there are only 400 frequencies transmitted.

The incoming FSK signals are first processed in a differential delay SAW filter. The SAW device is a dispersive delay line with a delay characteristic such that the high frequency signals are delayed less than the lower frequency signals. It is designed to obtain a "frequency-time delay" transfer function that is linear. In addition, it has also a bandpass characteristic with steep skirts approaching a rectangular shape. The latter is desirable in rejecting out-of-band signals adjacent to the operating frequency band. Following the differential delay unit is a multiplier, which is a frequency mixer. This mixer is driven by a frequency expander that repetitively sweeps its output frequency within a 40 MHz bandwidth over a period of $4T$ in a downward fashion, hence it is called a down chirp. At the output of the mixer the difference frequency signal is selected as shown in Figure 4. Consequently, the mixer output signal is a series of down chirps corresponding to each received FSK frequency. Each of these down chirps are 40 MHz wide, corresponding to the expander frequency sweep. A linear amplifier restores the level of the down chirps to a convenient level for further processing in the compressor. The compressor is also a SAW device designed to give an up chirp characteristic within a bandwidth of 40 MHz during a period of $2T$. If the received signal frequency band and the expander sweep frequency band is B ($B=40$ MHz), then the time bandwidth products of the differential delay unit and the compressor are equal to $2TB$. The transfer characteristic of the compressor is such that for each input down chirp, corresponding to each FSK signal, a frequency impulse is produced in time (within a period of $2T$) proportional to the FSK frequency location within the received frequency range. The radio frequency signal of the impulses is proportional to the input signal frequency and is removed by an envelope detector.

CONVOLVE-MULTIPLY-CONVOLVE FSK DEMODULATOR

The differential delay unit and the compressor filter are reflective array filters (sometimes called RACs, reflective array compressors). In this study a surface acoustic wave (SAW) dispersive filter constructed using an innovative single bounce technique and hyperbolically tapered transducers is being considered. The objective is to achieve a large time-bandwidth product (in the order of 3000) and low insertion loss. The insertion loss of the differential delay unit is approximately 35 dB and the compressor filter is projected to have an insertion loss of approximately 10 dB. In addition, the compression filter may contain internal amplitude weighting to improve sidelobe suppression and therefore prevent significant inter-channel cross talk.

The single bounce technique for obtaining pulse compression in a SAW filter [Ref. 3] is shown in Figure 4. The transducers are called hyperbolically tapered transducers because each active electrode is a section of a hyperbola. If x is the transverse position across the transducer, then the spacing between electrodes, as well as the wavelength varies as $1/x$ and the frequency is proportional to x . The surface wave emerges from the transducer as a narrow lobe with a width inversely proportional to the length of the transducer. The width of the acoustic beam is matched to the effective width of the reflective array and this eliminates the geometric mismatch loss. The advantages of the single bounce technique over the conventional two-bounce approach are: (1) lower insertion loss, (2) wider bandwidth, and lower manufacturing cost.

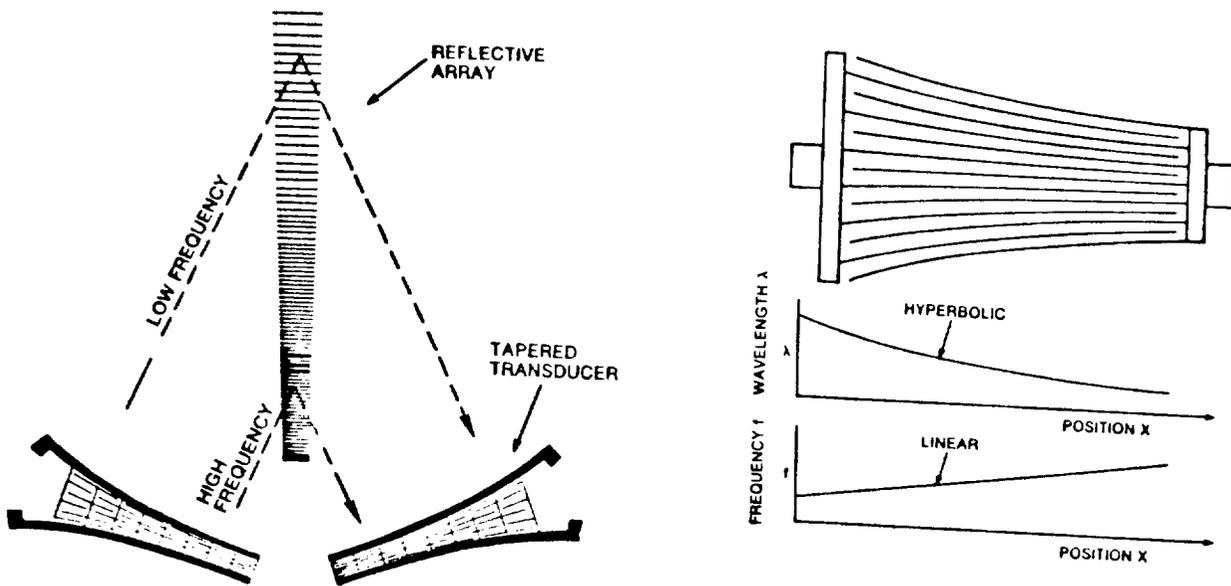


Figure 4- Single Bounce Dispersive SAW filter.

OPTIMUM MODULATION TECHNIQUES

A quaternary FSK modulation technique does not optimally use the available frequency bandwidth. Several other digital modulation techniques have been considered using an uplink performance criterion of 1×10^{-6} bit error rate (BER). The techniques considered were multi-tone FSK (up to 16), M-ary PSK (up to 16), quadrature amplitude modulation (4-QAM and 16-QAM), and quadrature partial response (QPR) modulation.

In comparing the Power/Channel requirements of all the modulation techniques, it was concluded that the optimum modulation technique is either QPSK or QPR. However, the equipment complexity of the QPSK system is relatively less than the QPR system. Therefore, QPSK modulation is the best choice for this application. In addition, it is desirable to operate the ground segment power amplifier at one dB compression, due to power efficiency considerations. To this effect, offset QPSK (OQPSK) provides the best solution, because a filtered OQPSK waveform when subjected to amplitude nonlinearity does not result in significant spectrum broadening as in the case of regular QPSK and/or MSK.

MULTICHANNEL OQPSK RECEIVER/DEMODULATOR

In this system, each user is assigned a carrier frequency. Assuming a data transmission rate of 64 Kbps per channel, the frequency carriers are separated by 64 KHz. As in the case of the multi-tone FSK system, all users' signals have to be in synchronism and timing signals transmitted with each transmission. This system will allow 625 channels occupy the entire 40 MHz satellite transponder bandwidth. Optimum detection is achieved by coherent demodulation. A differential coherent demodulation technique eliminates the need for carrier recovery and tracking circuits, thus reducing size and power requirements.

Each user transmitter operates on a preassigned carrier frequency, as shown in Figure 7. The data is initially split into odd and even data streams. The odd data stream consists of the odd bits of the original data, while the even data stream are the even bits. Note that the odd and even data streams are automatically offset by one data bit period relative to each other. If the input data bit period is T_b then the odd and even data symbol period is $T=2T_b$. Subsequently, each data stream is randomized, differentially encoded, and filtered (raised cosine), prior to quadrature modulation.

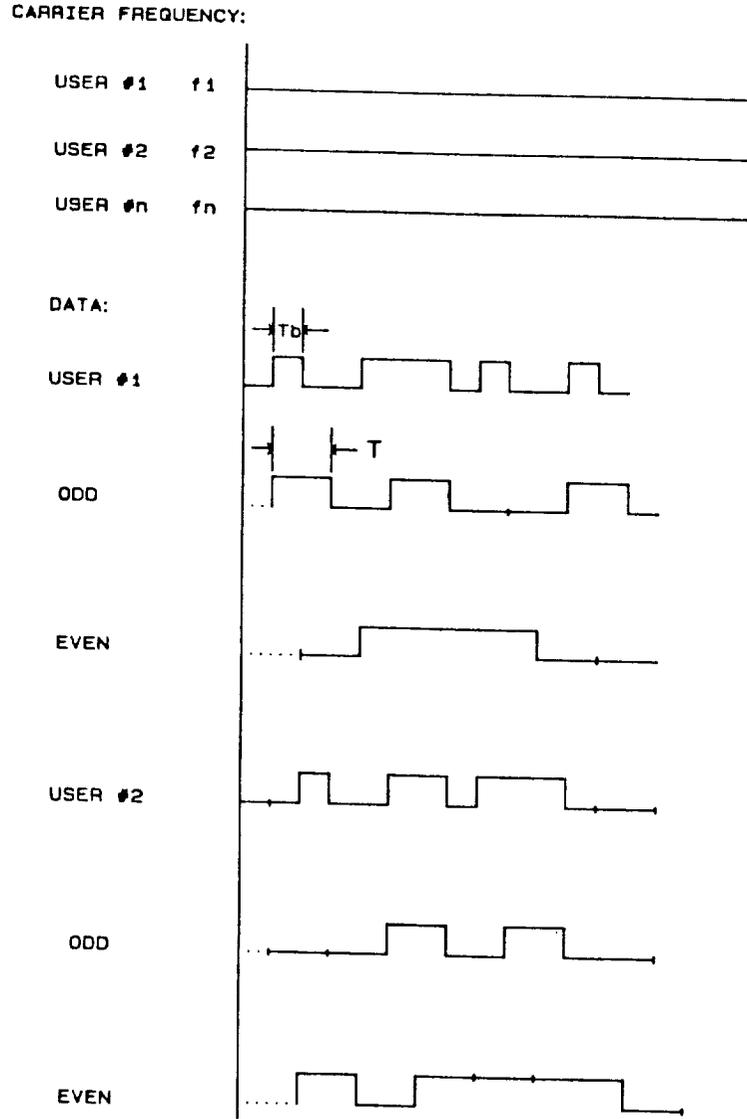
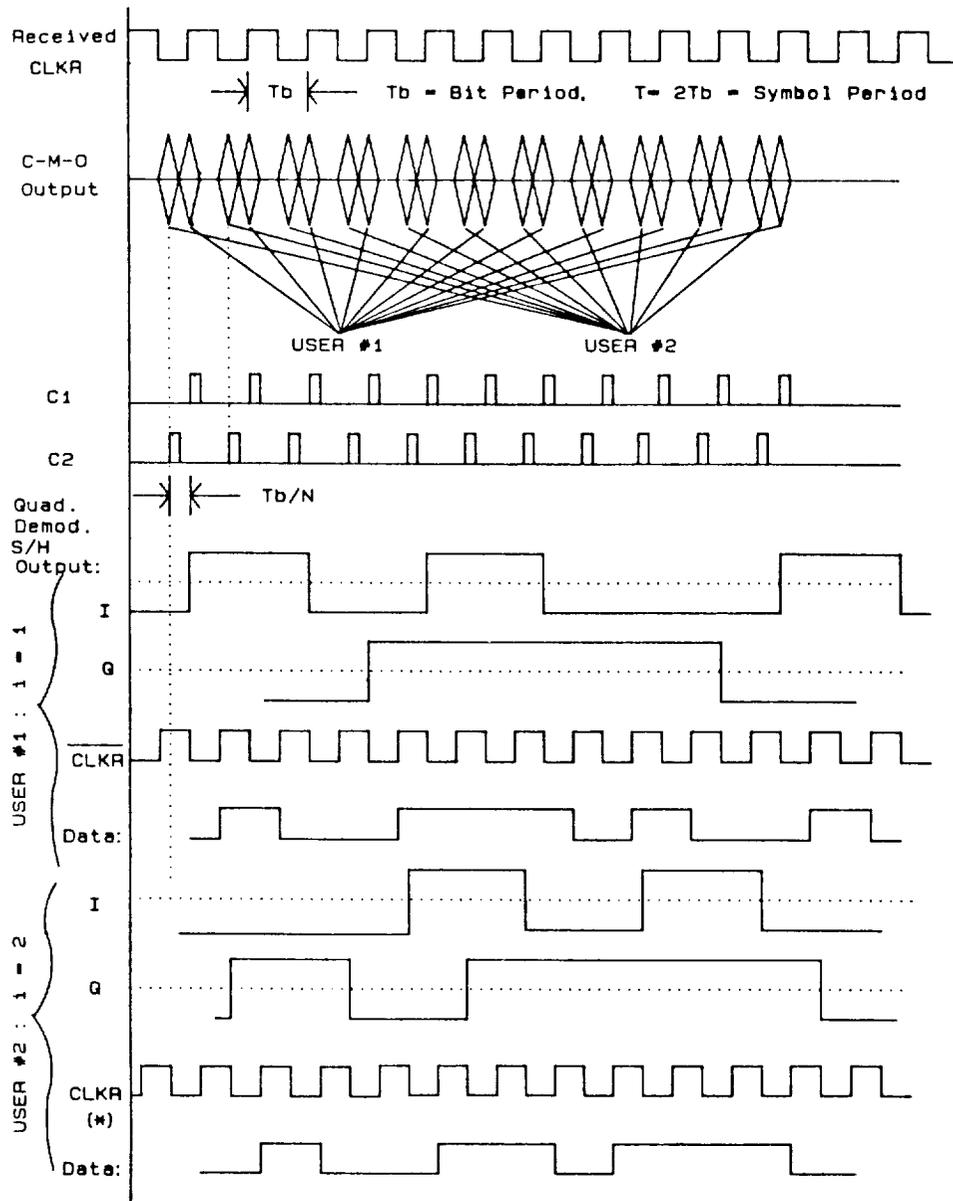


Figure 5- OQPSK Transmission

OQPSK DEMODULATOR/DETECTOR

The step by step process of demodulation and detection of the received OQPSK signal is depicted in Figure 8. The timing recovery process is identical to the process described for the FSK system. Signals received from various ground users are simultaneously transformed into pulses, corresponding to each user, by the C-M-C transformer. These pulses are spaced in time proportional to the user frequency. Each impulse, corresponding to each user periodically occurs every T_b second. Under each pulse is a radio frequency proportional to the input user frequency. The QPSK symbols imbedded in these pulses are related to the amplitude and phase of each received signal.



Notes:

1/ (*): CLKR delayed by:

$$T_b \times \frac{N - (i - 1)}{N}$$

2/ $i = \text{User Number } 1, 2, \dots, N.$

Figure 6- OQPSK Demodulation and Detection

CONCLUSION

From the study performed during the Phase-I program, it is concluded that the Convolve-Multiply-Convolve (CMC) chirp transformer allows for simultaneous demodulation of multichannel communications signals and is practically realizable. The large time-bandwidth product achievable (up to 3000) with low power and small size is the key advantage of using a CMC chirp transformer based upon SAW dispersive delay lines.

A multichannel digital communications system with an on-board satellite Multichannel Receiver/Demodulator with network synchronization provided by the Global Positioning Satellite system is proposed. The design of a quadrature frequency shift keyed system has been presented. It was found that, from the viewpoint of ground station power requirement associated with the allowable number of communication channels, quadrature phase shift keyed (QPSK) modulation offers the best performance. It is possible to compensate for the performance degradation imposed by temperature variations upon the SAW based CMC chirp transformer using an innovative circuit technique.

A complete QPSK system has been designed for the on-board Multichannel Receiver/Demodulator based upon chirp transformation techniques using SAW dispersive delay lines. The proposed system design also allows expansion for channel multiplexing and switching. It is recommended that a feasibility model of the Multichannel Receiver Demodulator for demonstration and proof of concept be constructed and tested.

The proposed system would expand the practical use and capabilities of satellite communication systems to the industrial, educational, scientific and health institutions. It would allow low cost ground terminals to link hotels, corporations, and other institutions that are not co-located. Similarly, it would allow universities, and research laboratories (scientific as well as medical), to exchange scientific information in an efficient manner. A direct benefit to NASA would be to link its research facilities by satellite, hence providing an efficient mechanism for better coordination.

LIST OF REFERENCES

1. R.C. Williamson, et.al., "A Satellite-Borne SAW Chirp-Transform System for Uplink Demodulation of FSK Communication Signals", Proceedings 1979 Ultrasonic Symposium.
2. James J. Spilker Jr., Digital Communications by Satellite, Prentice Hall.
3. L.P. Solie, "A New Low-Loss, Single Bounce, Reflective Array Filter Using Hyperbolically Tapered Transducers," Proceedings 1986 Ultrasonics Symposium.

N92-22013

FLEXIBLE HIGH SPEED CODEC

R.W. Boyd and W.F. Hartman
Harris, Government Systems Sector
Melbourne, Florida 32901

ABSTRACT

This project's objective is to develop and demonstrate an advanced high-speed coding technology that provides substantial coding gains with limited bandwidth expansion for several common modulation types. The resulting technique is applicable to several continuous and burst communication environments. Decoding provides a significant gain with hard decisions alone and can utilize soft decision information when available from the demodulator to increase the coding gain.

The hard decision codec will be implemented using a single application specific integrated circuit (ASIC) chip. It will be capable of encoding and decoding as well as some formatting and synchronization functions at data rates up to 300 megabits per second (Mb/s). Code rate is a function of the block length and can vary from 7/8 to 15/16. Length of coded bursts can be any multiple of 32 that is greater than or equal to 256 bits. Coding may be switched in or out on a burst-by-burst basis with no change in the throughput delay.

Reliability information, in the form of 3-bit (8-level) soft decisions, can be exploited using applique circuitry around the hard decision codec. This applique circuitry will be discrete logic in the present contract; however, ease of transition to LSI is one of the design guidelines.

This paper discusses the selected coding technique and describes its application to some communication systems. Performance with 4, 8 and 16-ary PSK modulation is also presented.

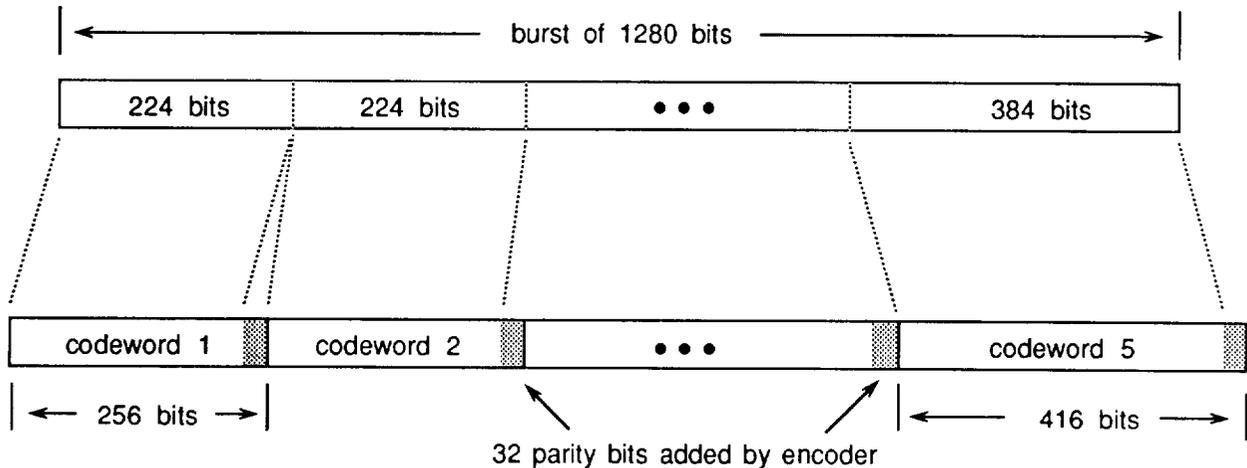
This work is funded by NASA Lewis Research Center under Contract #NAS3-25087;
Contract Manager: Robert Jones.

CODING TECHNIQUE

A triple error correcting Bose-Chadhuri Hacqenghem (BCH) code was chosen as providing the best compromise between coding gain and implementation complexity. It is possible to reach decoding speeds of 300 Mb/s with reasonable complexity using a pre-solved approach (ref. 1). A BCH codeword has a maximum length of 2^m-1 when defined over the Galois field $GF(2^m)$. The minimum possible value was chosen for m (9) in order to minimize hardware complexity. Twenty-seven parity bits are necessary to obtain a triple error correcting code (distance=7) with $m=9$. A 28th parity bit is used to simplify soft decision decoding, but provides no gain in a hard decision environment.

The number of overhead bits is padded out to 32 in order to simplify the numerology associated with coding. These extra 4 bits are not part of the code and are available for functions such as unique (synchronization) sequence transmission. The result is an encoder that appends 32 bits to the end of each codeword. Unaltered data precedes these overhead bits since the code is systematic. The number of data bits in a codeword is a multiple of 32 in the range of 224 to 480, resulting in codewords of from 256 to 512 bits.

An arbitrary length burst may be encoded by breaking the data into the appropriate number of 224 bits segments followed by one segment that can be up to 480 bits in length. Every segment is encoded separately, effectively adding 32 bits to each. The resulting overall code rate will be at least 7/8. Continuous mode simply uses consecutive (288,256) codewords.



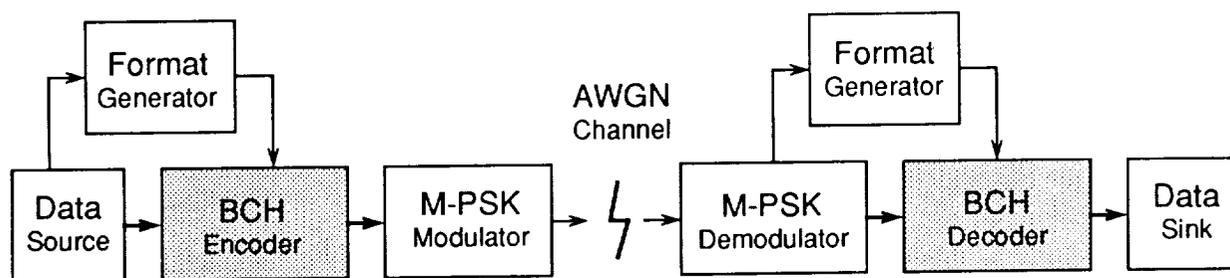
Partitioning a Burst Among Codewords

HARD DECISION CONFIGURATION

The ASIC codec can provide encoding and hard decision decoding at data rates up to 300 Mb/s in a stand-alone fashion, given a compatible interface. Data, both coded and uncoded, has a eight-wide interface with the codec chip (six-wide with 8-ary modulations). This is necessary to reduce the 343 Mb/s (maximum) channel rate to an 43 Mb/s interface rate. Also, a format generator, that directs overhead insertion while holding off new data, is assumed. This implies that data is received from the source (e.g. a queue) in bursts (at the channel rate) separated by blank intervals that allow parity insertion. The format generator may also indicate that the burst is not to be coded, in which case the encoder and decoder simply act as delay lines.

Generation of fractional rate clocks and the rate buffering that would be required to accept continuous data from the source and deliver encoded data at a higher rate is extremely difficult with arbitrary data rates. These functions must be provided externally if required in a specific application.

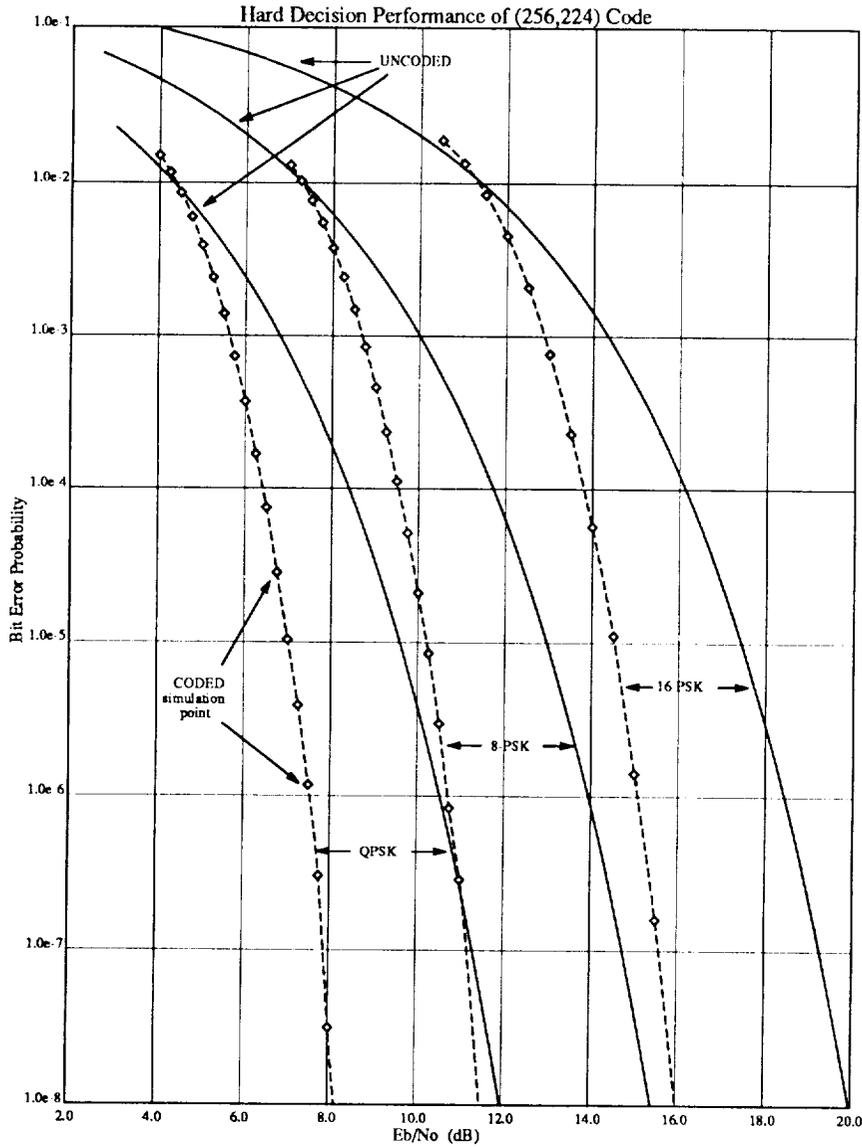
Encoder and decoder on single ASIC Chip



Stand Alone Codec Configuration (Hard Decisions)

HARD DECISION PERFORMANCE

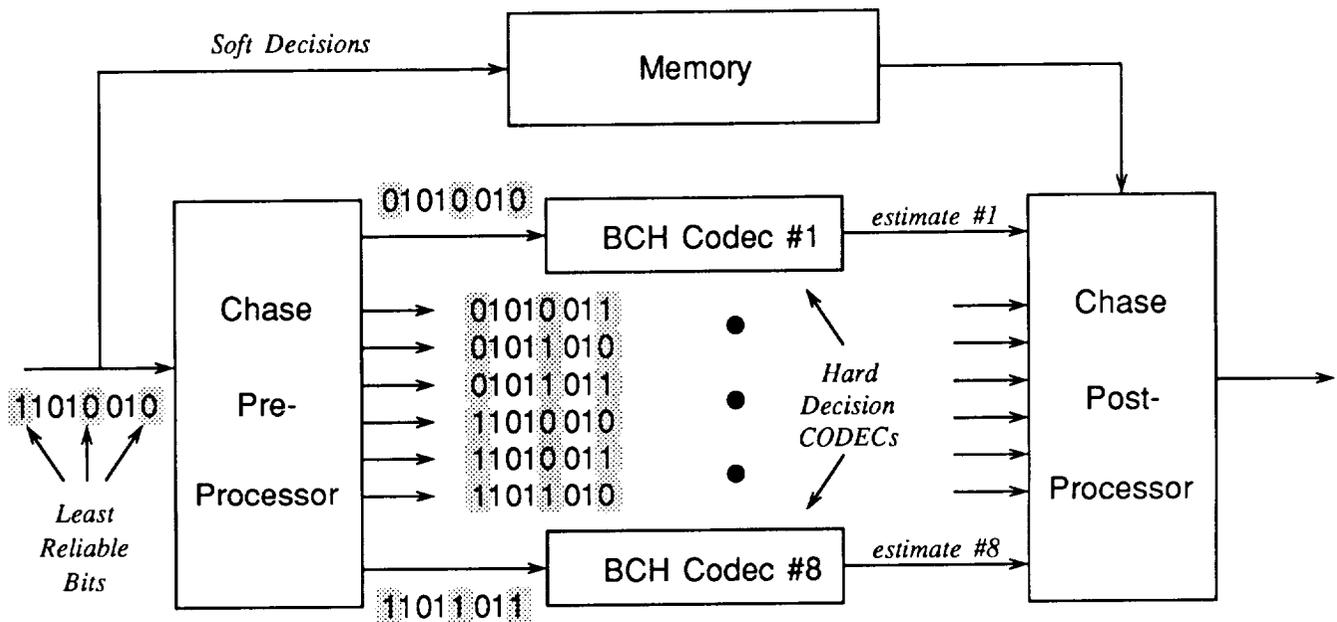
The figures below relate to the expected bit error rate (BER) after decoding when M-ary PSK modulation is used to communicate coded data over an additive white gaussian noise (AWGN) channel. Coding gain with hard decisions is seen to range from 2 to 4 dB in the operational range of $10^{-4} \leq \text{BER} \leq 10^{-8}$. Coding gain is a weak function of codeword length and is greatest for the shortest length (224 data bit) codeword.



Hard Decision Coding Gain (in dB)						
BER	(256,224) Code			(512,480) Code		
	QPSK	8-PSK	16-PSK	QPSK	8-PSK	16-PSK
10^{-4}	2.0	2.2	2.4	1.8	2.0	2.2
10^{-6}	3.0	3.2	3.4	2.8	3.0	3.2
10^{-8}	3.8	3.9	4.0	3.6	3.7	3.8

SOFT DECISION CONFIGURATION

A Chase (ref. 2) algorithm is employed to utilize soft decision information. Soft decision decoding requires hardware appliques as well as multiple hard decision codecs. The Chase preprocessor uses soft decision information to identify the three least reliably received bits of each codeword. It then generates eight sequences by letting the three least reliable bits take on all possible values. Each of these sequences is hard decision decoded to obtain (possibly different) estimates of the true codeword. A post-processor selects the most likely of these estimates by doing eight correlations, again using the soft decision information. In addition to pre- and post-processors, additional memory to buffer reliability information is required in the soft decision configuration.

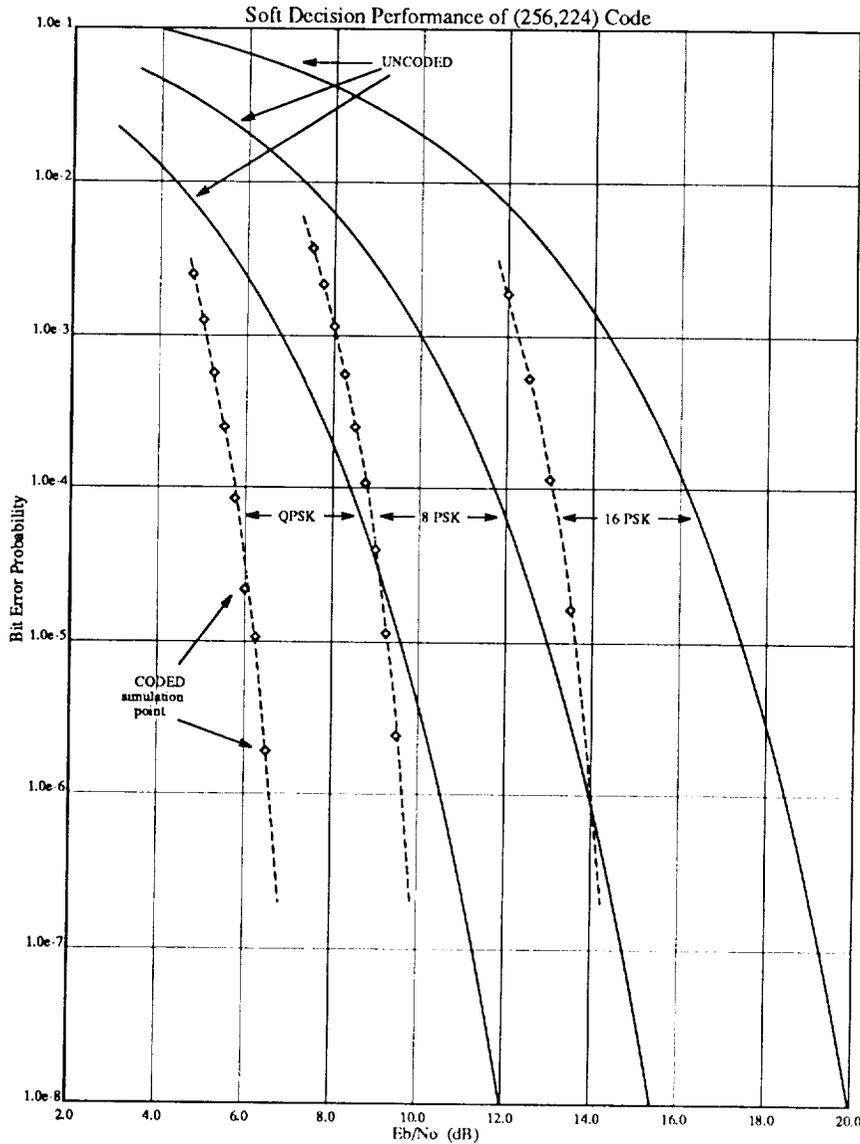


Chase Algorithm Decoder

The Chase decoder for this project will differ from the figure above in that it will only process four estimates. Using a 28th parity bit, performance can be maintained while cutting hardware complexity nearly in half by observing overall parity condition. It is also expected that a single ASIC chip will hold two complete hard decision codecs.

SOFT DECISION PERFORMANCE

The figures below relate to the expected bit error rate (BER) after decoding when M-ary PSK modulation is used to communicate coded data over an additive white gaussian noise (AWGN) channel. Coding gain with soft decisions is from .7 to 1.4 dB greater than with hard decisions alone. The data below corresponds to a Chase algorithm using 3 least reliable bits and analog metrics (infinite quantization).



Soft Decision Coding Gain (in dB)						
BER	(256,224) Code			(512,480) Code		
	QPSK	8-PSK	16-PSK	QPSK	8-PSK	16-PSK
10^{-4}	2.7	2.9	3.1	2.5	2.7	2.9
10^{-6}	4.0	4.3	4.5	3.8	4.1	4.3
10^{-8}	4.9	5.2	5.4	4.7	5.0	5.2

OBSERVATIONS

A high-speed, high-rate coding technique suitable for both burst and continuous communication systems has been presented. It can operate as a single chip hard decision codec or, with decoding appliques, can utilize soft decision information in the decoding process. Coding gains up to 4 dB are obtained in the hard decision mode, increasing to as much as 5.5 dB with soft decisions (at 10^{-8} BER).

Error correction coding has long been considered a good means to lower the required EIRP in communication systems having unlimited bandwidth. However, high-rate codes such as the one described are also well suited for bandwidth efficient systems. The codec rate and interface are matched to the larger signaling alphabets used for constrained bandwidth communications. Data has been given indicating that coding gain improves slightly with increasing modulation alphabet size. Even with the overhead required to insert parity bits, the net result is less power required to communicate a given data rate (say 300 Mb/s) over a fixed bandwidth channel (say 200 MHz).

The coding approach is extremely flexible by design. Hard decision operation supports several different interface modes at data rates less than 300 Mb/s. Soft decision performance can be enhanced by increasing the number of least reliable bits identified. Complexity of the Chase algorithm hardware can be reduced at data rates significantly less than 300 Mb/s by using a single hard decision codec to form multiple estimates.

It is believed that the coding approach and hardware resulting from this project will prove useful to a variety of high rate systems.

REFERENCES

- 1) Plokinghorn, F. Jr., "Decoding of Double and Triple Error Correcting Bose-Chaudhuri Codes," *IEEE Transactions on Information Theory*, October 1966, pp. 480-481.
- 2) Chase, D., "A Class of Algorithms for Decoding Block Codes With Channel Measurement Information," *IEEE Transactions on Information Theory*, January 1972, pp. 170-182.



PROGRAMMABLE DIGITAL MODEM

M. Kappes
COMSAT Laboratories
Clarksburg, Maryland 20871

DATA RATE RANGE AND OPERATIONAL MODES

SYMBOL RATE RANGE OF PDM:

- 1.92 - 75 MSYMBOLS/S

OPERATIONAL MODES:

- CONTINUOUS
- DEPENDENT BURST
- INDEPENDENT BURST

TEST AND DEMONSTRATION EQUIPMENT

FEATURES:

- PROVIDES MULTIPLE DATA STREAMS FOR HIGHER LEVEL FORMATS
- INSERTS PREAMBLES AND UNIQUE WORD STRUCTURES FOR BURST MODES
- GENERATES DATA AND CONTROL SIGNALS FOR INTERFERRING BURST MODULATOR
- PROVIDES CONTROL SIGNALS REQUIRED FOR DEMODULATOR OPERATION
- MEASURES BER AND UNIQUE WORD MISS RATE

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DATA RATE RANGE AND OPERATIONAL MODES

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- MEASURES BER AND UNIQUE WORD MISS RATE

PROGRAMMABLE DIGITAL MODEM

PROGRAM GOALS

DEVELOPMENT OF A MODEM WHICH IS:

- PROGRAMMABLE IN THE AREAS OF MODULATION FORMAT, DATA RATE, AND OPERATIONAL MODE
- FULLY DIGITALLY IMPLEMENTED
- LOW RECURRING COST
- SMALL SIZE

MODULATION FORMATS

REQUIRED FORMATS:

- QPSK, 8-PSK, 16-PSK

OPTIONAL FORMATS:

- OFFSET QPSK
- MSK
- 16-QAM

PDM DESIGN CHALLENGES

DEMODULATOR AGC, CARRIER, AND CLOCK RECOVERY STRUCTURE:

- MUST BE ADAPTABLE TO HANDLE DIFFERENT MODULATION FORMATS
- RECOVERY BANDWIDTHS MUST SCALE WITH DATA RATE
- OPERATION AT 75 MSYMBOLS /S AND 2 SAMPLES /SYMBOL REQUIRES 150 MHZ CLOCKING
- MINIMIZE POWER AND SIZE WHILE OPERATING AT THIS SPEED

DATA FILTERING:

- REQUIRES DIGITAL IMPLEMENTATION FOR DATA RATE FLEXIBILITY
- HIGH SPEED REQUIREMENT IMPOSES COMPLEXITY LIMIT ON FILTER

OPERATIONAL MODES:

- INDEPENDENT BURST MODE REQUIRES RATE FLEXIBLE ACQUISITION ALGORITHMS

SESSION IV

POSTER DISPLAYS AND TECHNOLOGY REVIEWS
CHAIR: W.D. IVANCIC

J.M. OTT, FORD AEROSPACE CORP.

J.K. WONG AND E.M. MROZEK, TRW, INC.

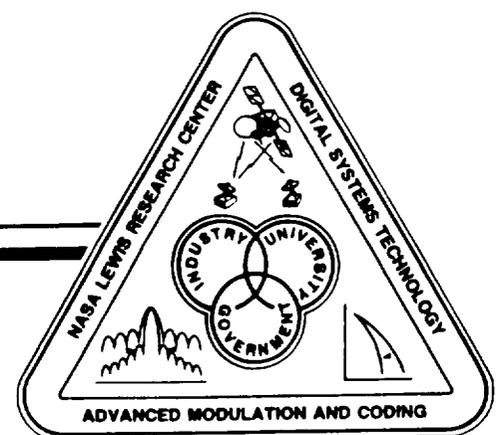
R. FANG, M. KAPPES, AND S. MILLER, COMSAT LABS

J.V. WERNLUND, HARRIS CORPORATION

C.R. RYAN, MOTOROLA, INC.

W.W. WU, INTELSAT

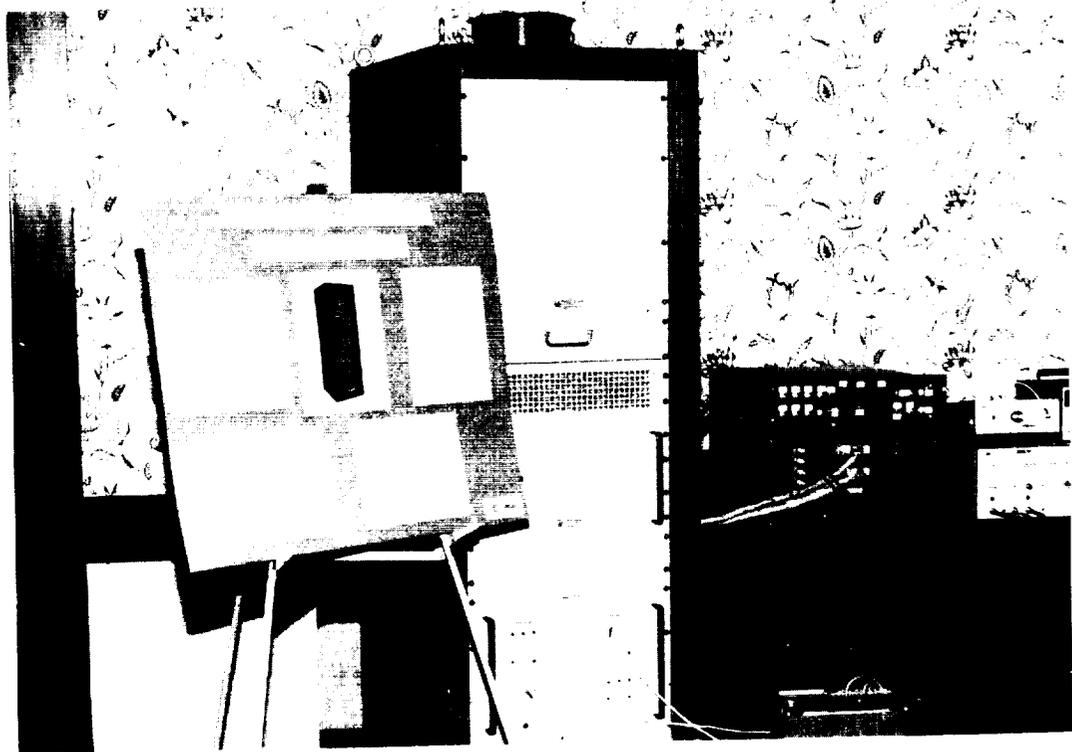
R.J. KERCZEWSKI, NASA LEWIS RESEARCH CENTER



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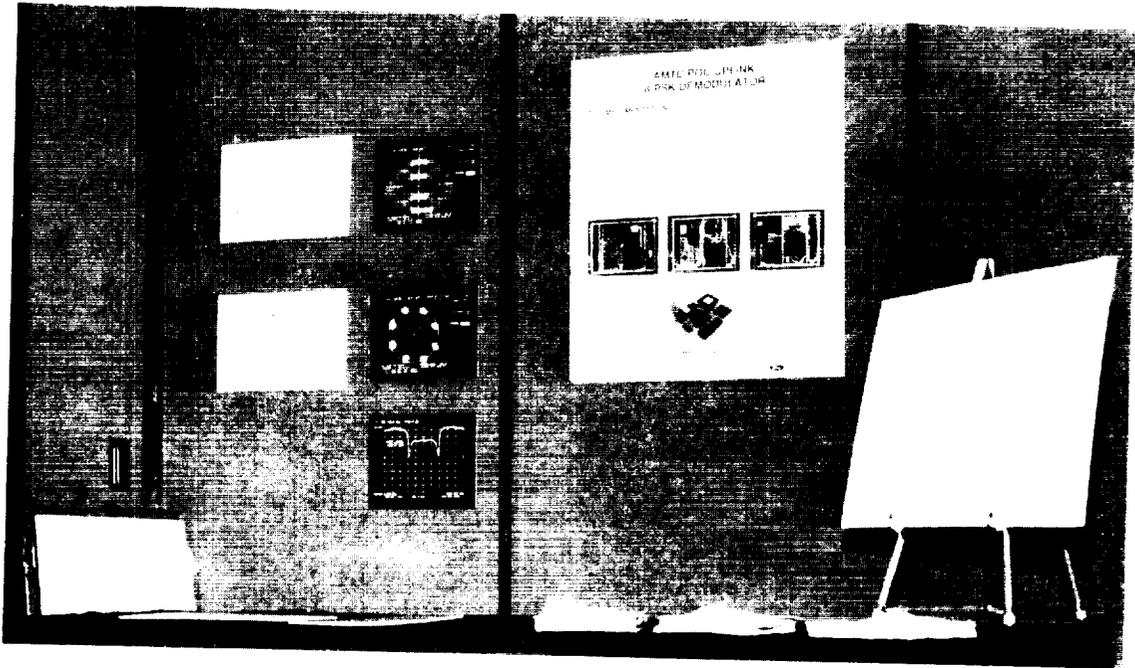


COMSAT Laboratories 225 Mb/s, Add-Compare-Select gate array test circuit and poster display.

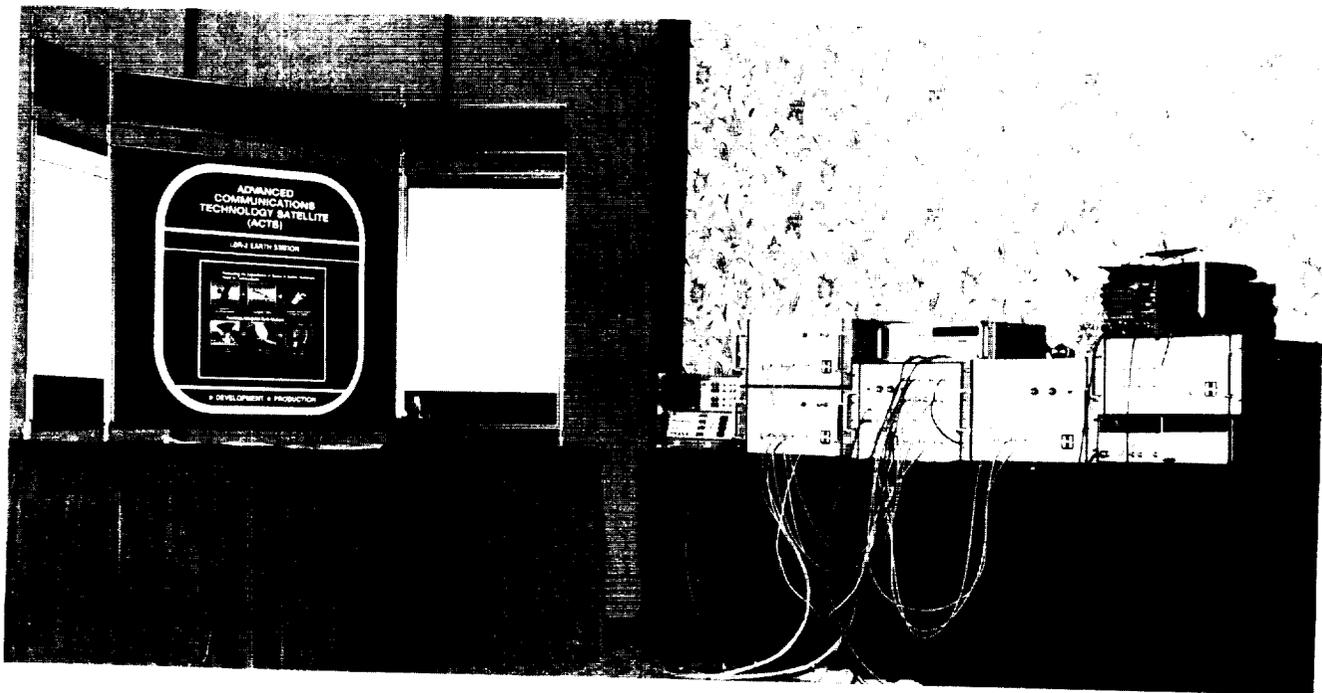


COMSAT laboratories rate 8/9 coded 8-PSK proof-of-concept system and poster display.

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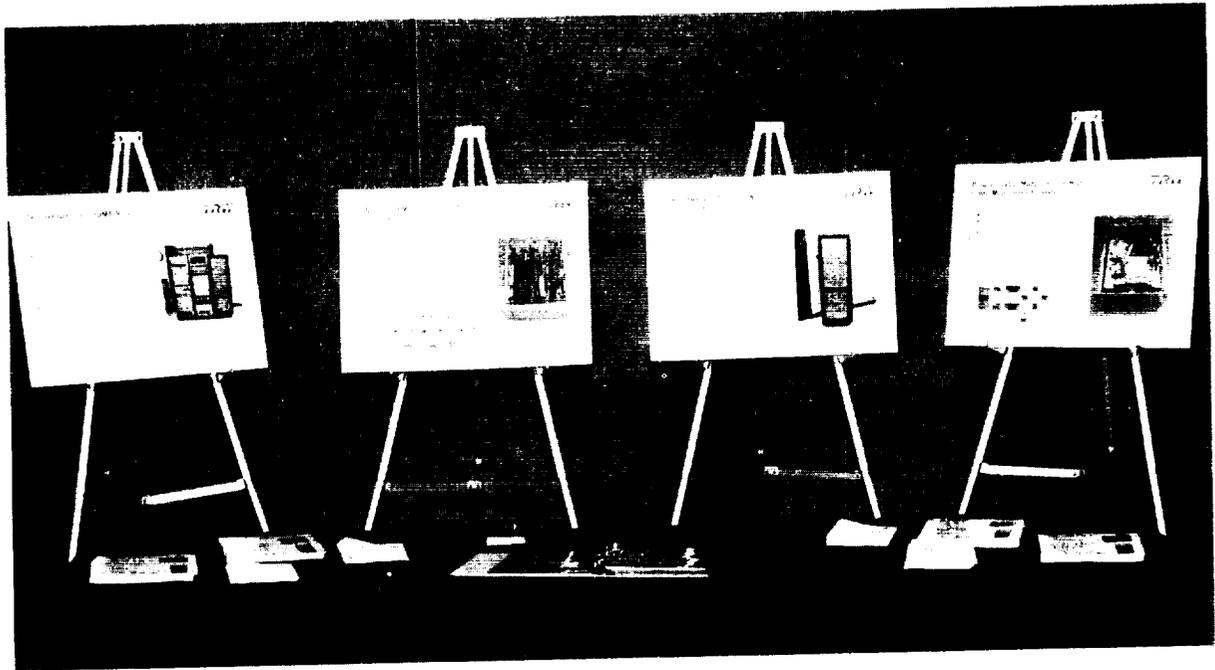


Ford Aerospace 8-PSK demodulator poster display.

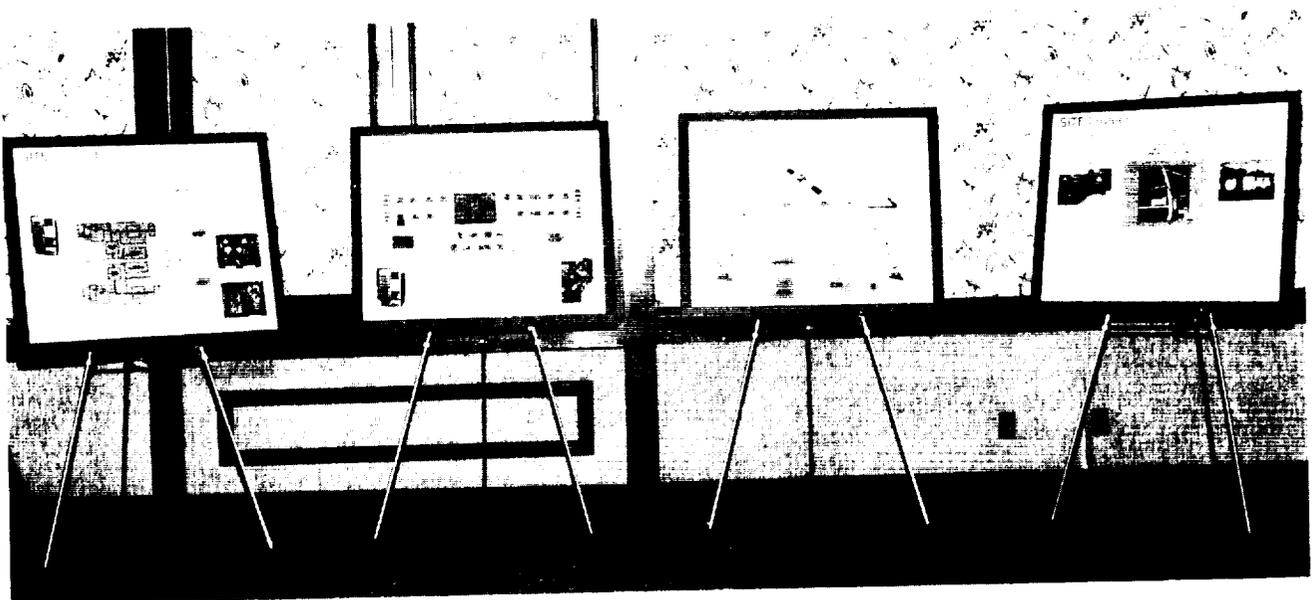


Harris Corporation rate 1/2 coded 16-CPFSK proof-of-concept demodulator and special test equipment and poster display for ACTS LBR-2 Earth Station.

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TRW Incorporated rate 3/4 coded 16 QAM posters.

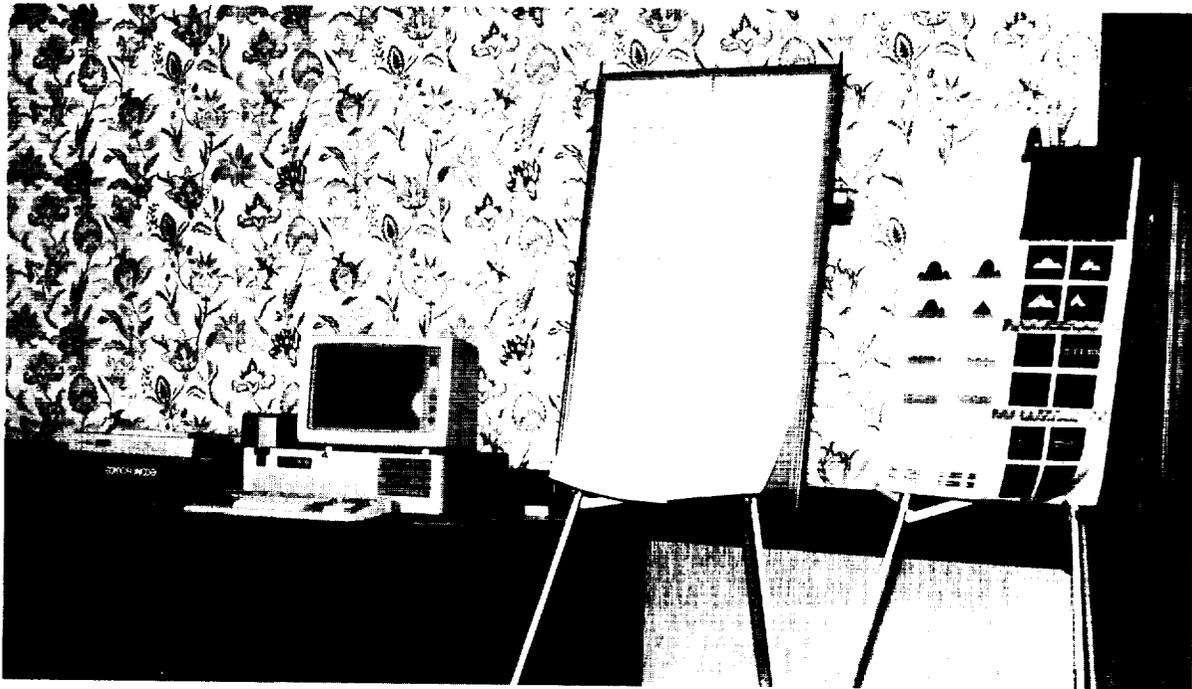


NASA Lewis Research Center Systems Integration, Test and Evaluation (SITE) Project poster display.

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Panel Members: S. Joseph Campanella, Panel Chair (COMSAT Laboratories); Frank Amoroso (Hughes Aircraft); Kamilo Feher (University of California); Peter Liu (Cyclotomics); Carl R. Ryan (Motorol Incorporated); Al Stern (General Electric)



Motorola Incorporated display and demonstration of computer aided design of communication systems.

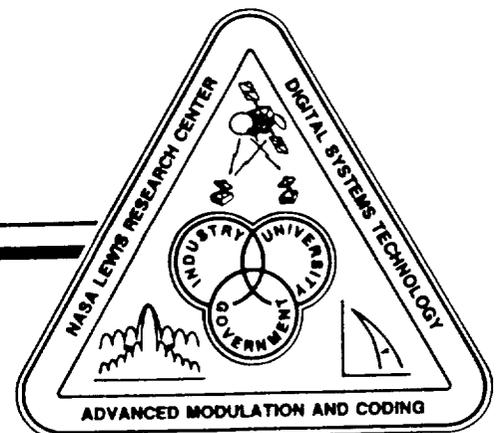
SESSION V

**OTHER ADVANCED MODULATION AND
CODING PROGRAMS
CHAIR: J.L. HARROLD**

**ATDRSS 300 MB/S MODEM PROGRAM
C.R. RYAN
MOTOROLA, INCORPORATED**

**MODULATION AND CODING TECHNOLOGY FOR DEEP SPACE
AND SATELLITE APPLICATIONS
J.H. YUEN AND W. RAFFERTY
CALIFORNIA INSTITUTE OF TECHNOLOGY**

**DIGITAL SYNCHRONIZATION AND
COMMUNICATION TECHNIQUES
W.C. LINDSEY
LINCOM CORPORATION**



SESSION V CONTINUED

**BANDWIDTH EFFICIENT CODING FOR
SATELLITE COMMUNICATIONS**

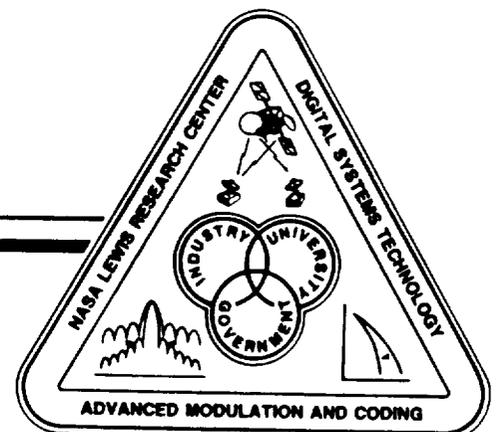
SHU LIN

UNIVERSITY OF HAWAII

D.J. COSTELLO, JR.

UNIVERSITY OF NOTRE DAME

W.H. MILLER, J.C. MORAKIS, AND W.B. POLAND, JR.
GODDARD SPACE FLIGHT CENTER



ATDRSS 300 MB/S MODEM PROGRAM

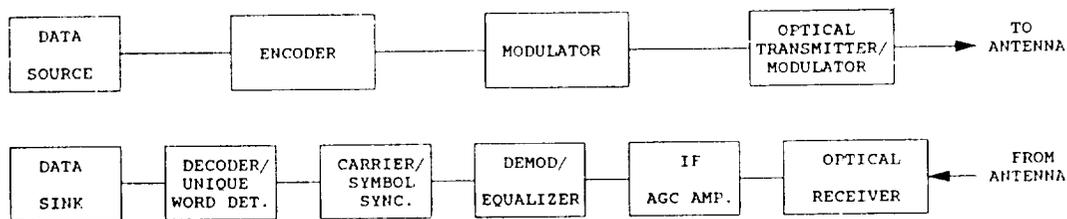
Dr. Carl R. Ryan
 Motorola Incorporated
 Chandler, Arizona 85248

ABSTRACT

The 300 Mbps modem has been developed by Motorola, Government Electronics Group, for direct application to the next generation high data rate TDMA communication system. This Modem utilizes continuous phase modulation combined with a restricted range Reed-Solomon Codec to achieve a bandwidth efficiency of 3 bits/sec/hz. The constant envelope amplitude signal allows one to operate the power amplifier in its saturation mode without significant spectral regrowth or bit error rate degradation.

1.1 INTRODUCTION

The 300 Mbps modem has been developed by Motorola, Government Electronics Group, for direct application to the next generation high data rate TDMA communication system. The 300 Mbps modem functional block diagram is shown in Figure 1.1. NASA envisions using the 300 Mbps modem capability for handling data from the Space Station being transmitted through the TDRSS system. The Space Station will be transmitting either 150 Mbps or 300 Mbps data through TDRSS to the White Sands ground station.



300 Mbps MODEM CONCEPTUAL BLOCK DIAGRAM
 Figure 1.1

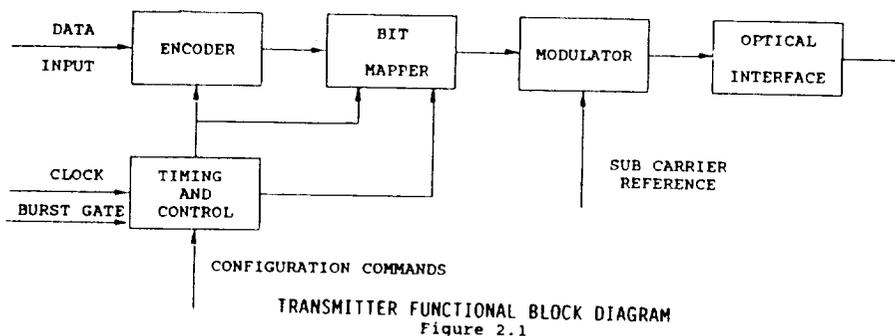
NASA has the responsibility of relaying this data from the White Sands ground station to Kennedy Space Center, Johnson Space Center and Goddard Space Flight Center for analysis. The 300 Mbps modem will be used to handle this redistribution of data. This system is expected to be deployed in the 1990's.

The 300 Mbps Modem performs all of the necessary functions required to transmit and receive a bandwidth-efficient continuous phase modulated signal. The 300 Mbps Modem consists of a Transmitter, Receiver, Data Source/Error Detector and Channel Simulator. The Data Source/Error Detector and Channel Simulator will be used for test and evaluation purposes only. The modem and STE will be user controlled via an IBM-compatible computer for monitoring and data collection purposes.

2.1 TRANSMITTER

The transmitter subsystem drawer consists of the necessary hardware to generate a bandwidth-efficient CPQPSK/4 modulated signal at an IF frequency of 440 MHz and a required RF bandwidth of 100 MHz. Figure 2.1 shows the functional block diagram of the

unit. The transmitter is comprised of the following six functional blocks: Timing Generator, Preamble Generator, System Controller, Encoder, Bit Mapper and Modulator. A description of each of these assemblies is provided in the following sections.



2.1.1 Timing Generator

The Timing Generator accepts the Burst Gate control signal and System Clock reference at its input. It generates all the internal control signals and clocks required by all functional blocks of the transmitter.

2.1.2 System Controller

The System Controller is used as the interface between the personal computer and the transmitter. It primarily interfaces with the Encoder and Bit Mapper for fallback transmission selection and down-loading of the Bit Mapper Mapping rule. The System Controller will be a commercially available hardware item.

2.1.3 Encoder

The restricted Reed-Solomon Encoder interlaces a forward error correcting block code into the input PN data stream in such a way that any single phase error in the receiver can be detected. The 5 bit per symbol Reed-Solomon code used has a block length of 130 bits (26 symbols). The restricted encoder effectively encodes the LSB only thereby reducing the hardware complexity required and providing an effective code rate very near one. The data to be encoded is derived from the gray coded phase states by XOR-ing the gray coded bits together to produce a checksum bit. Several checksum bits are used by the encoder to generate parity bits which are added to the data stream.

2.2 OPTICAL LINK

The up-link side is to receive a satellite-ready 440 MHz IF signal. It provides the necessary amplification to modulate a laser, and then transmits the modulated lightwave carrier over a 2 km fiber optic cable to the OPTO/IF unit. An optical receiver in the OPTO/IF unit converts the optical signal back to an analog 440 MHz IF signal. Additional amplification will be required to increase the converted signal to a 0 dBm power level for RF transmission.

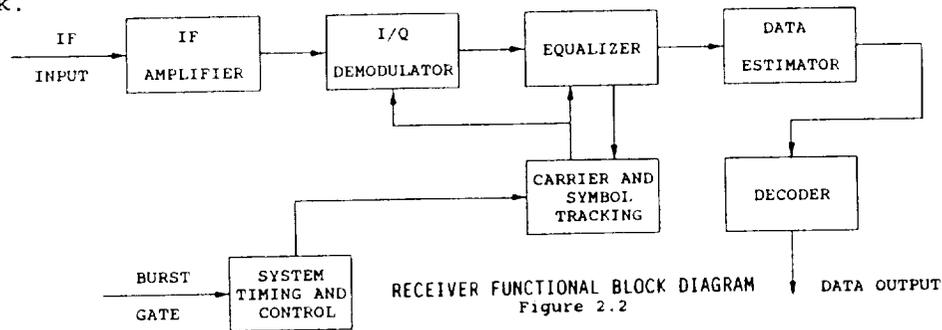
The down-link side receives a 440 MHz satellite signal and essentially performs the same function as the up-link side.

The ORTEL 3510A optical transmitter and ORTEL 4511A are the major components that comprise the optical link.

2.3 RECEIVER

The receiver subsystem drawer consists of the necessary hardware to amplify, demodulate, equalize, decode and detect a CPQPSK/4 modulated signal. Figure 2.2 shows the functional block diagram of the 300 Mbps Modem receiver. The receiver consists of the

following seven functional blocks: IF Amplifier/AGC, I/Q Demodulator, Decision Feedback Equalizer, Carrier Synchronizer, Symbol Synchronizer, Unique Word Detector and Restricted RS-Decoder. The following paragraphs provide a brief description of each functional block.



2.3.1 IF Amplifier/AGC

The IF Amplifier/AGC accepts the CPQPSK/4 modulated signal at its input. The 440 MHz IF signal is amplified such that the output is maintained at a constant output power. The IF Amplifier/AGC consists of a series of fixed and variable gain amplifiers which maintain a constant output power over a wide range of input power. The gain acquisition characteristics of the AGC circuitry will enable operation in a TDMA environment.

An external control signal will reset the incoming primary AGC loop to its maximum gain prior to each signal burst.

2.3.2 I/Q Demodulator

The Demodulator converts the incoming 440 MHz IF signal from the IF Amplifier/AGC to baseband inphase and quadrature signals. The 440 MHz LO signal is provided by an external fixed crystal reference.

2.3.3 Decision Feedback Equalizer

The equalizer receives a down converted baseband signal from the demodulator. The equalizer shall be 3 taps--1 leading, center, and 1 lagging taps--decision feedback equalizer with preset, manual, and adaptive tap adjustment capability.

The equalizer contains two parts: linear and nonlinear. The linear portion of the DFE is the same as a transversal equalizer. The nonlinear portion of the DFE contains a feedback network as a recursive equalizer. The feedback network of the DFE, however, contains a decision device that makes a hard decision from the output of the DFE. The resulting signal is delayed properly, scaled by the tap weights, and summed at the input junction of the equalizer.

3.1 300 MBPS MODEM OPERATIONS SYSTEM DESCRIPTION

The high data rate modem has been designed to provide for a 3 bits/hz/sec bandwidth efficiency along with various back-off modes to allow for optimizing the bit error rate (BER) and data rate performance for varying channel conditions.

The continuous phase modulation (CPM) format of the modulator provides a near constant envelope amplitude signal with very low side lobes. This constant envelope amplitude signal allows one to operate the down link power amplifier at or near its saturation limit without causing significant BER degradation or spectral side lobe regrowth that is normally observed in phase shift keying schemes like 8PSK. The use of high performance Reed-Solomon Codec optimized for the modulation format allows for efficient signal power utilization with less than 10% coding overhead. Table 2.1 provides the theoretical performance of the modem.

MODEM THEORETICAL PERFORMANCE CHARACTERISTICS
Table 2.1

Data Rate (MB/S)	No of Errors RS CODEC Corrects	Effective Code Rate	Symbol Rate (Mhz)	Modulation Index	Modulator Levels	Spectral Efficiency (Bits/Sec/hertz)	Eb/No for 10 ⁻⁶ BER (UNCODED)	Eb/No for 10 ⁻⁶ BER (CODED)	Relative Power Required
300	3	12/13	108.3	1/16	8	3	18 dB	13.8 dB	0 dB
200	2	12/13	108.3	1/8	4	2	14.1 dB	10.8 dB	-5.7 dB
100	1	12/13	108.3	1/4	2	1	10.6 dB	9.5 dB	-12.2 dB
250	3	14/15	107.1	1/16	8	2.5	16.5 dB	12 dB	-2.3 dB

3.1.1 Waveform Design and Coding

The range of performance characteristics is very large because of the built in flexibility of the codec/modulator combination. The diagram of Figure 2.1 illustrates the fundamental design approach of the modulator and is helpful in describing the various operating modes of the modem.

Three distinct functions are performed within the transmitter. These functions are:

1. Forward Error Correcting Coding

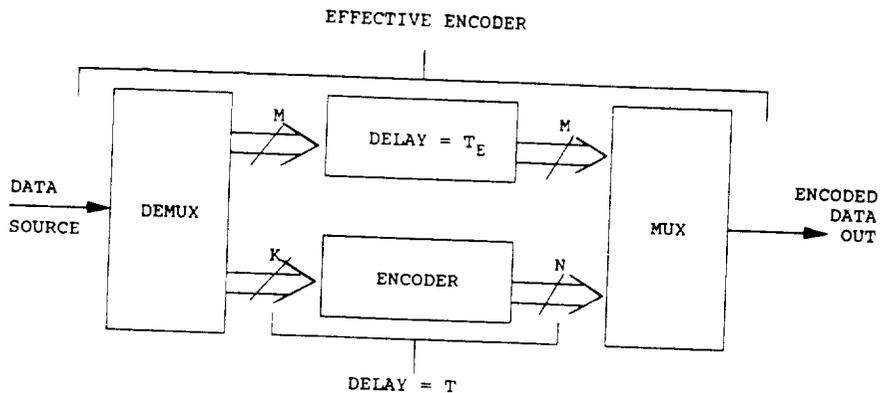
This encoder (illustrated in Figure 3.1) is a Reed-Solomon coder operating at a code rate of approximately 7/8. This coder is capable of correcting 3 bit errors and uses a block length of 32 symbols. Performance optimization is obtained by coding only the least significant data bits in the modulator.

2. Bit Mapper

The bit mapper provides the mapping necessary to convert the encoded data into a format required by the modulator. This bit mapper is the key to the designs flexibility of the modulator and allows one to operate at a variety of modulation indices. (See Figure 3.2 and Table 2.2)

3. CPM Modulator

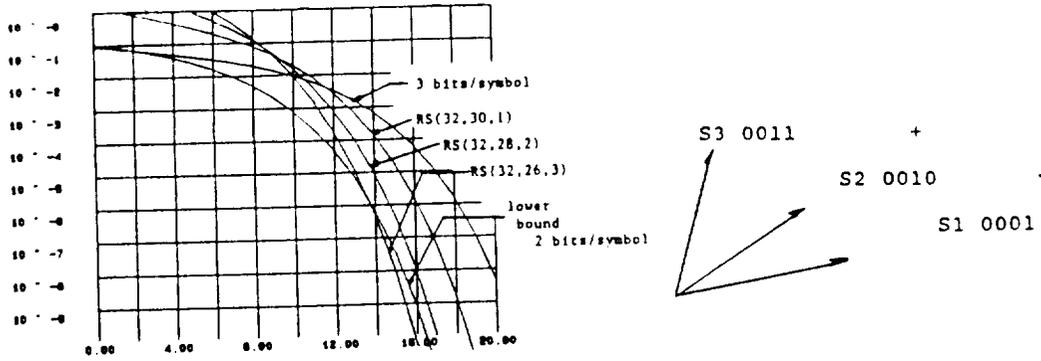
The CPM Modulator is actually an implementation of a four state 22.5° per phase state (M=4, h=1/16) modulator capable of operating at a rate of 350 mega symbols per second. The phase division and filtering scheme provides for very accurate phase state and phase trajectory control. The high symbol rate requirements are necessary to allow for the necessary phase control of the final output operating at approximately 110 MS/S.



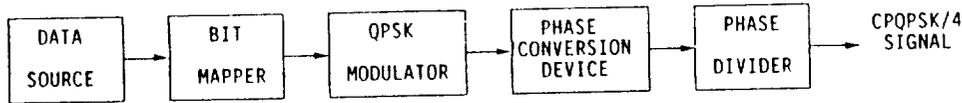
NOTE: ENCODER RATE (K/N) TYPICALLY 3/4, 2/3

TOTAL EFFECTIVE ENCODER RATE ($\frac{M+K}{M+N}$) TYPICALLY 10/11, 12/13

RESTRICTED RS ENCODER CONCEPTUAL BLOCK DIAGRAM
Figure 3.1



BER PERFORMANCE OF RESTRICTED CODED 3 BITS/SYMBOL SIGNAL
Figure 3.1(a)



BIT MAPPER AND CPQPSK/4 MODULATOR BLOCK DIAGRAM
Figure 3.2

PHASE TREE FOR CPQPSK/4
Table 2.2

input symbol	QPSK equivalent	CPQPSK/4 phase tree	output bit sequence (previous symbol = 2)
6	11 = 135°		1110011111
5	01 = 112.5°		1110010101
4	00 = 90°		1110000000
3	10 = 67.5°		1111101010
2	11 = 45°		1111111111
1	01 = 22.5°		1111010101
0	00 = 0°		1101000000
7	10 = -22.5°		1101001010

3.1.2 Other Operating Modes

Table 2.1 provides an indication of the baseline performance of the modem. The 108.33 MS/S reference was chosen on the basis of the actual channel availability. Operation at symbol rates less than the above values is a practical consideration; however, the optimum bandwidth efficiency will not be achieved and the symbol clock rate of the receiver must be changed accordingly to accommodate this reduced symbol rate operation.

3.2.2 Modulator

The bandwidth efficient continuous phase modulator is realized in hardware using Continuous Phase Quadrature Phase Shift Keyed (CPQPSK) signaling technique, [2] This signaling scheme also allows easy hardware implementation that approximates the ideal CPM signal with little Power Spectral Density (PSD) and Bit Error Rate (BER) probability degradation.

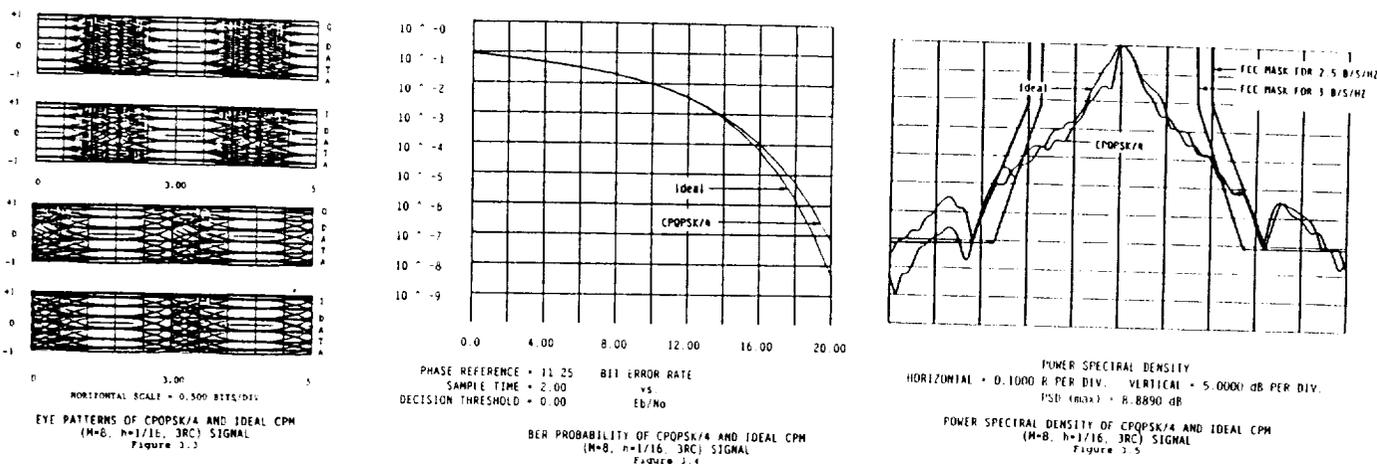
The CPQPSK modulator is derived from a QPSK modulator; however, the discrete phase trajectories of QPSK signal are converted through a phase conversion device to obtain smooth raised cosine phase trajectories and nearly constant envelope amplitude characteristic. CPQPSK signal approximates $M=4$, $h=1/4$, RC pulse CPM signals. But, it can be modified by phase dividing and bit mapping, referred to as CPQPSK/4 signaling technique, to obtain a CPM signal with $M=8$, $h=1/16$, 3RC pulse shape. The smaller modulation index, h , of $1/16$ is obtained by phase dividing the CPQPSK by 4. The modulation level, M , of 8 is obtained from the phase divided CPQPSK signal through the bit mapper.

Figure 3.4 shows a block diagram of the CPQPSK/4 modulator. It contains a QPSK modulator, phase conversion device, phase divider, and bit mapper. The bit mapper is responsible for mapping the message data into the phase divided CPQPSK signal constellation in such a way that the correct phase transitions and destination occurs. Thus, with the bit mapper controlling the signal phase paths through the phase divided CPQPSK modulator, $M=8$, $h=1/16$, 3RC CPM signal can be obtained.

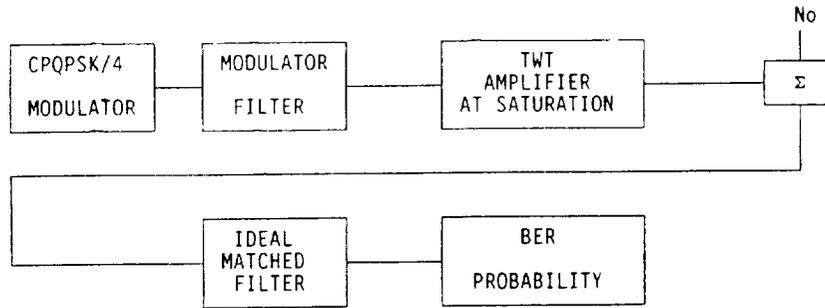
Figure 3.3, -4, and -5 show eye patterns, BER probabilities, and PSD, respectively, of CPQPSK/4 CPM signal and an ideal $M=8$, $h=1/16$, 3RC CPM signal. The eye patterns, Figure 3.3, of CPQPSK/4 show a close approximation to the ideal signal. Figure 3.4 indicates that there is only about 0.7 dB of E_b/N_0 degradation at 10^{-6} BER probability. There is also a little difference in the power spectral densities between the two signals, as shown in Figure 3.5. The CPQPSK/4 CPM signal generated this way will be referred to as 3 Bits/Symbol (B/S) signal for the rest of this report.

The FCC Bandwidth requirement mask, per reference [3], that specifies frequency attenuation of a signal about an assigned channel bandwidth is also shown in Figure 3.5. The frequency axis is normalized to data bit rate, R , at 300 MBPS. Thus, a channel bandpass bandwidth of $(1/3)R$ indicates a 100 MHz channel and $(1/4)R$ indicates a 125 MHz channel. If a signal transmitting at a data rate of 300 Mbps is transmitted through the 100 MHz and 125 MHz channel while meeting the FCC mask, then it represents 3 b/s/hz and 2.5 b/s/hz, respectively, bandwidth efficiency.

However, Figure 3.5 shows that PSD of 3 B/S signal does not meet the FCC mask for neither the 3 b/s/hz nor the 2.5 b/s/hz bandwidth efficiency. Compliance to the FCC mask is a necessary requirement for the 300 MBPS modem and, thus, the 3 B/S signal requires further processing. This motivates use of a modulator bandlimiting filter in order to meet the FCC mask.



The modulator bandlimiting filter can be selected by investigating its effect on the bandlimited 3 B/S signal as it is transmitted through a satellite transponder channel. Figure 3.6 shows a computer simulation set up where the ideal 3 B/S signal is filtered with a modulator filter and operated through a TWT amplifier at saturation. (The nonlinear amplifier is a device often used in a typical satellite channel and performance of the bandlimited 3 B/S signal transmitted through TWT amplifier at saturation must be evaluated.)



COMPUTER SIMULATION SET-UP BLOCK DIAGRAM
Figure 3.6

There are many candidates for selecting the type of modulator filter. Smooth frequency roll-off response filters, such as Butterworth and Chebychev filters, are usually a good choice since they are easily realized in hardware and since the frequency and group delay responses are well characterized. However, in a bandwidth limited channel, a Nyquist filtering is usually chosen in practice. Such ideal filters have sharp frequency attenuation skirts and well equalized group delay responses. They are not easily realized in hardware, however, and subject to careful implementation techniques to approximate the ideal filter responses. Nonetheless, they are readily available through filter vendors and newly emerging filter techniques, such as crystal filters and surface acoustic wave filters, make Nyquist filtering possible.

Therefore, a Nyquist filter with -3dB bandpass bandwidth of $(0.35)R$, is used in the simulation of modulator bandlimiting filter. The roll-off factor, α , of the filter defines the amount of bandlimiting. With the roll-off factor of the modulator filter varied, one can simulate the effect of the bandlimiting on the 3 B/S CPM signal through the satellite nonlinear channel. The noise is assumed to be White Additive Gaussian Noise (WAGN) and BER probability is measured through the ideal matched filter, which has a noise bandwidth of $(0.25)R$ and does not introduce any intersymbol interference. The resulting PSD bandpass out of band power (OBP) is shown in Figure 3.7. (The MSK signal and FCC mask for 3 and 2.5 b/s/hz channel is also shown as reference.) Figure 3.7 shows that PSD's of the bandlimited 3 B/S signal before the TWT amplifier meet both the 2.5 and 3 b/s/hz bandwidth mask for all roll-off factors of the filter. However, PSD after the TWT amplifier, operating at saturation, slightly exceeds the masks. The nonlinear device causes spectral regrowth on the signal and, would, nonetheless, require further bandlimiting after the TWT amplifier in order to limit the sideband energy.

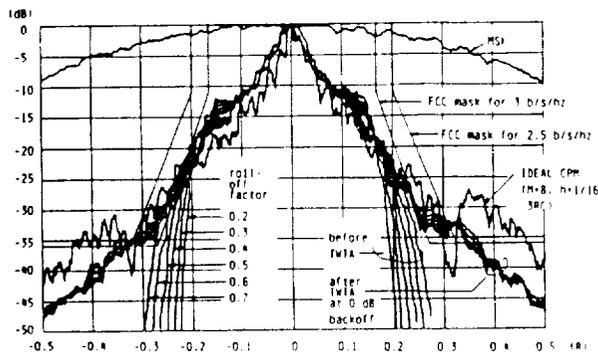


Figure 3.7(a)

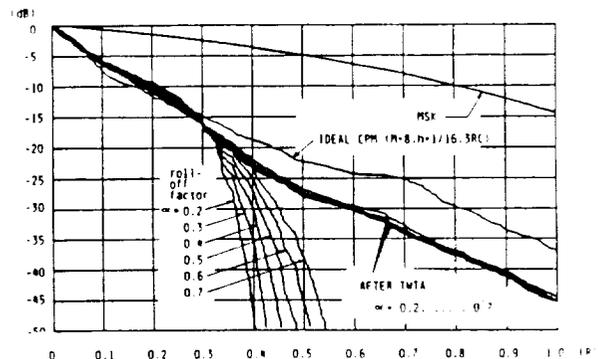


Figure 3.7(b)

The bandpass out of band power (OBP) of the bandlimited 3 B/S signal before and after TWT amplifier, in Figure 3.7, shows that the 3 B/S CPM signal is spectrally much narrower than MSK signal. The OBP after TWT amplifier, although less than that of the

ideal CPM signal, is about the same regardless the falloff factors of the modulator bandlimiting filter. However, the effect of the modulator filter is drastic. For example, at frequency of $(0.4)R$ away from $(0)R$, the OBP is as small as -45dB for a α of 0.2 , but it is as large as -24 dB for α of 0.7 .

Figure 3.8 shows peak-to-peak ripple, a worse case fluctuation of the power, of the bandlimited 3 B/S signal before TWT amplifier versus roll-off factor of the modulator filter. The bandpass OBP at -20 , -30 , and -40 dB is also shown. As expected, the ripple on the filtered signal decreases as the amount of bandlimiting decreases. However, the frequency at which the 99%, 99.9%, and 99.99% of the out of band power occur increases as the filter roll-off factor increases. As a reference, -20 dB bandpass OBP for MSK signal occurs at frequency of $(1.2)R$.

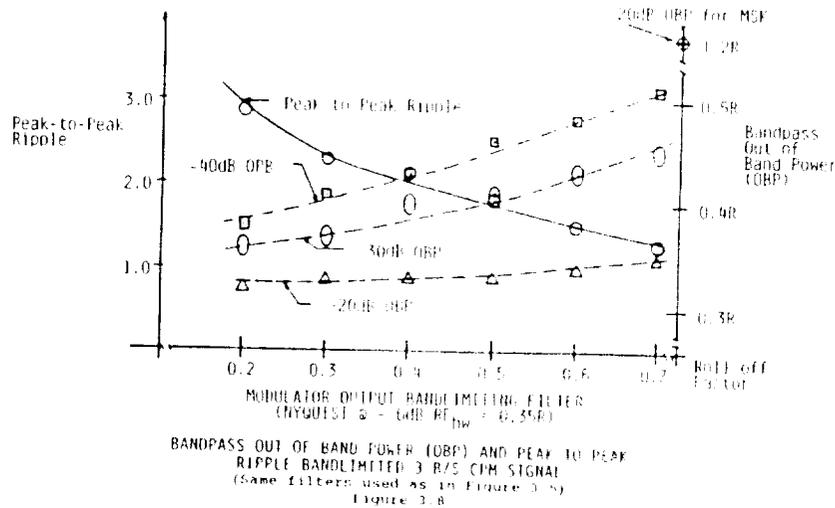
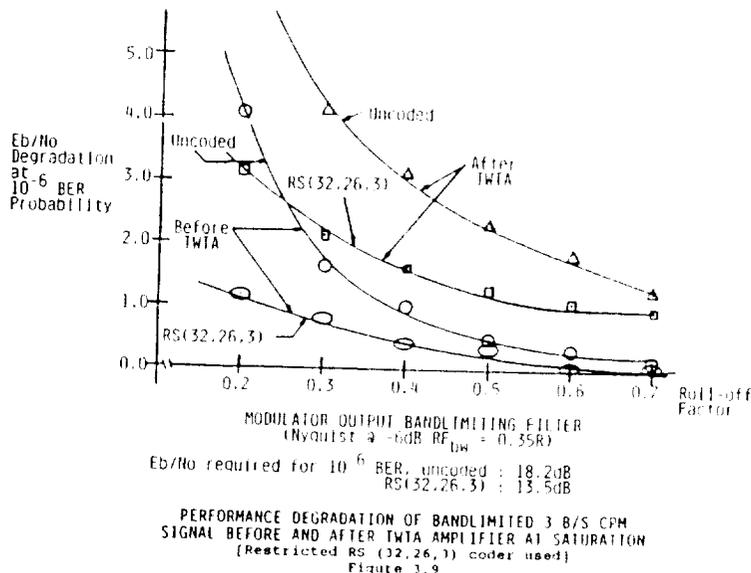
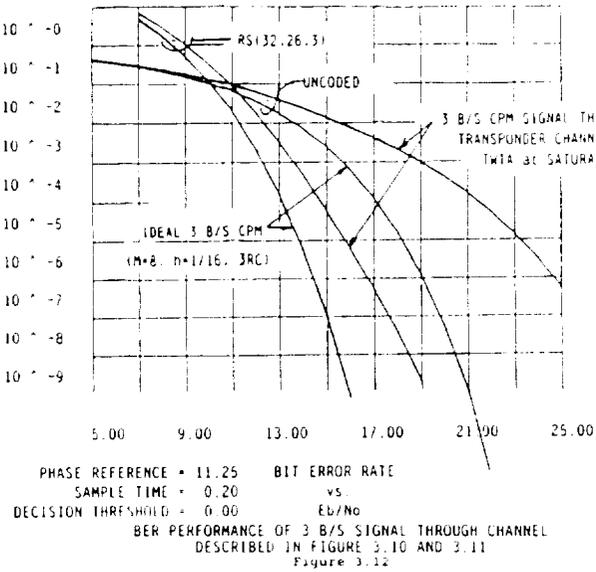
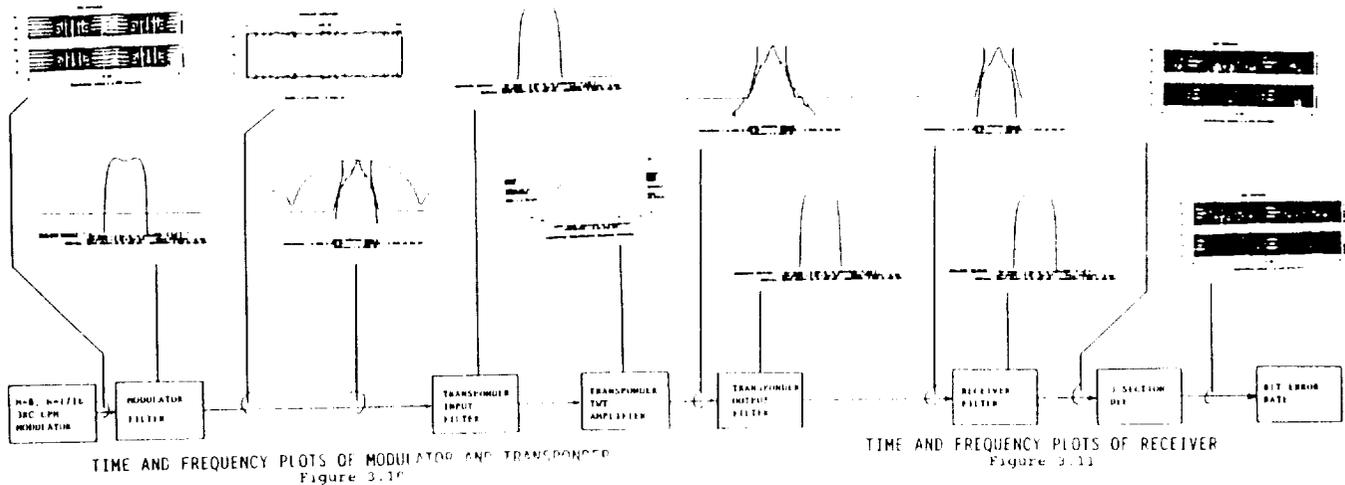


Figure 3.9 shows E_b/N_0 degradation of the bandlimited 3 B/S signal at 10^{-6} BER probability versus the roll-off factor of the modulator bandlimiting filter. A restricted Reed-Solomon coder, (discussed in next section), at code rate of 0.92 is used to assess the amount of BER improved against the uncoded BER performance. The performance degradation due to TWT amplifier operating at saturation is also shown. The graph shows that the degradation decrease as the amount of modulator bandlimiting decreases. However, the degradation due to the saturated TWT amplifier is at least 2 dB for the coded case and for the filter roll-off factor of at least 0.3 .



Therefore, the modulator bandlimiting filter degrades BER performance of 3 B/S signal as it is transmitted through TWT amplifier at saturation. The performance degradation can be improved by using error correction coding technique. The performance of 3 B/S signal can also be improved if the TWT amplifier is operated in its linear region. However, as satellites have limited power source, operating TWT amplifier linearly reduces the output power from the satellite drastically. This requires additional E_b/N_0 at the receiver such that the BER performance gained by operating TWT amplifier linearly not enough to justify the linear operation of the amplifier.

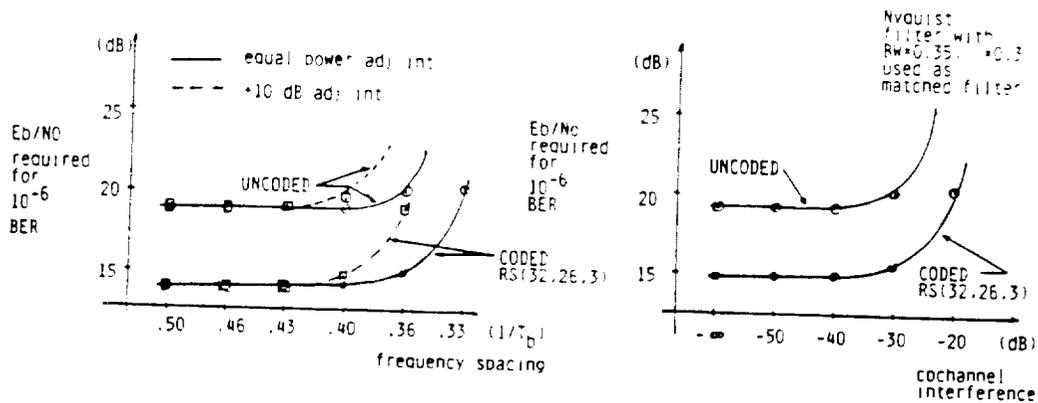
Figure 3.10 and 3.11 show the time and frequency domain plots of the simulation. The BER probability is also evaluated for coded case and E_b/N_0 degradation of about 2 dB is expected from the satellite channel distortion, as shown in Figure 3.12.



Thus, utilization of TWT amplifier operating at its saturation is possible when using the hardware realizable 3 B/S CPM signal with some modulator bandlimiting. In fact, 3 bits/sec/hz bandwidth efficiency, defined as transmitting 300 Mbps data through a 100 MHz bandwidth channel while meeting FCC mask is achievable with $M=8$, $h=1/16$, 3RC CPM signal only if the modulator bandlimiting filter and the transponder output mux filter is used. However, the modulator bandlimiting filter introduces envelope amplitude on the signal, which, inevitably, degrades the BER performance when operated through the nonlinear device at saturation.

Furthermore, the performance of the 3 B/S signal not only depended on the bandwidth requirement of the modulator bandlimiting filter, the FCC mask, and degradation due to TWT amplifier and the transponder filters, but also it depends on the amount of adjacent channel interference allowed. The signal's power spectral density could meet the FCC mask, have small envelope amplitude, and still, cause severe BER degradation when the adjacent channels are placed together closely, i.e. by symbol rate.

The BER performance is measured for various adjacent channel spacing. The result is shown in Figure 3.13. It shows the coded and uncoded E_b/N_0 degradation of 3 B/S CPM signal at 10^{-6} BER probability for equal and unequal power adjacent channel interference. The frequency spacing is also normalized to data rate, R , at 300 Mbps. The frequency spacing of the adjacent channel interference, however, is about $0.36R$ for the coded case for E_b/N_0 degradation of less than 0.5 dB.



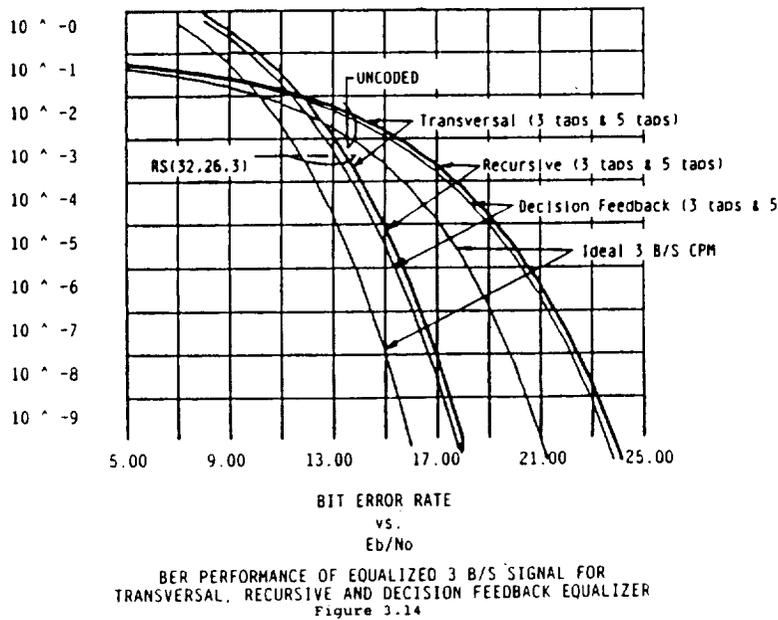
DEGRADATION DUE TO ADJACENT AND COCHANNEL INTERFERENCE
Figure 3.13(a)
Performance of 3 B/S Signal for
Adjacent Channel Interference

DEGRADATION DUE TO ADJACENT AND COCHANNEL INTERFERENCE
Figure 3.13(b)
Performance of 3 B/S Signal for
Cochannel Interference

Another channel impairment that degrades the BER performance is cochannel interference. Such interference, when large enough, causes a severe BER degradation as Figure 3.13(b) shows. For both the coded and uncoded case, cochannel interference of about 30 dB degrades the system performance by about 0.5 dB at coded BER of 10^{-6} . However, the BER degradation exponentially increases as the amount of the cochannel interference increases.

Another performance improving device to combat the intersymbol interferences is the equalizer. The equalization techniques are based on linear theory and often successful in correcting for multipath distortions as well as the ISI distortions. Typically, equalizers are used together with a receiver filter to not only correct for channel ISI and multipath distortions, but also it is used for desensitization of the critical receiver filter responses.

Transversal, recursive, and decision feedback equalizers are considered for performance improvement on the bandlimited 3 B/S signal. The channel is selected to be linear and the Nyquist filter with α of 0.3 is selected as the receiver filter. The BER performance of both 3 section and 5 section equalizers are shown in Figure 3.14. It can be seen that the 3 section equalizers are adequate and offer nearly the same performance as the 5 section equalizers. The decision feedback equalizer performs slightly better, by about 0.3 dB, than transversal or recursive equalizer. The coded performance is also shown.

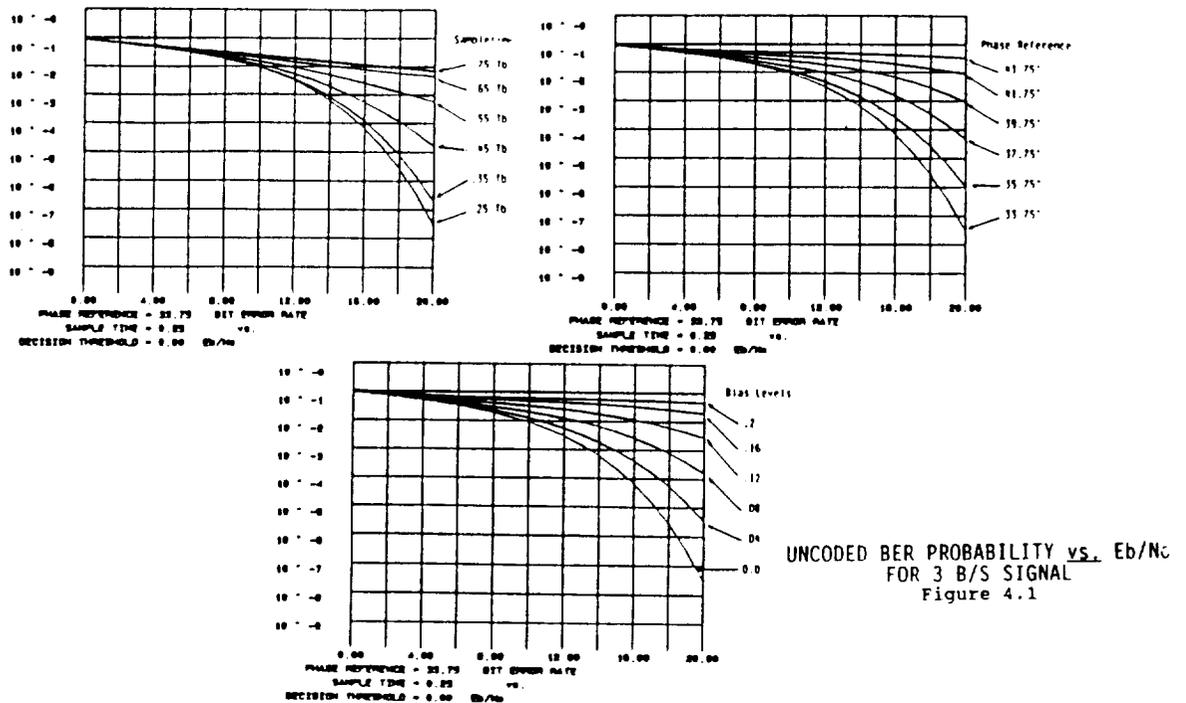


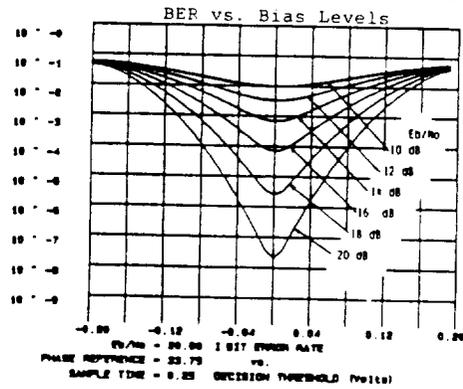
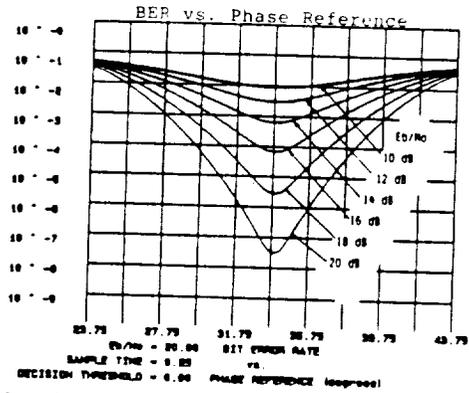
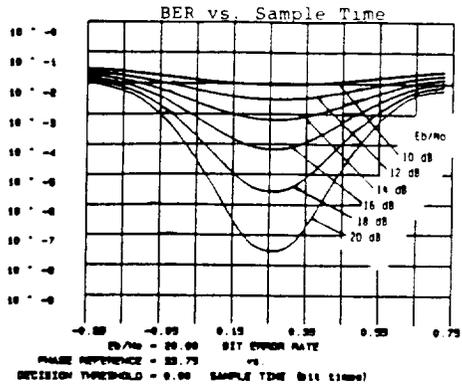
4.1 HARDWARE IMPAIRMENTS

A variety of factors contribute to the overall hardware performance as compared to the theoretical bound presented earlier. Realistic estimates of the hardware performance impairments have been made and presented in this section. These estimates are based on computer simulation, hardware measurements and observed performance characteristics of related equipment.

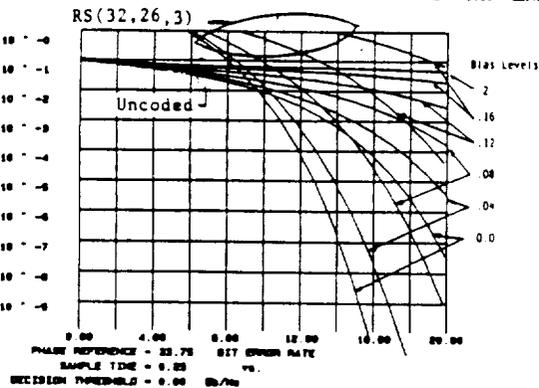
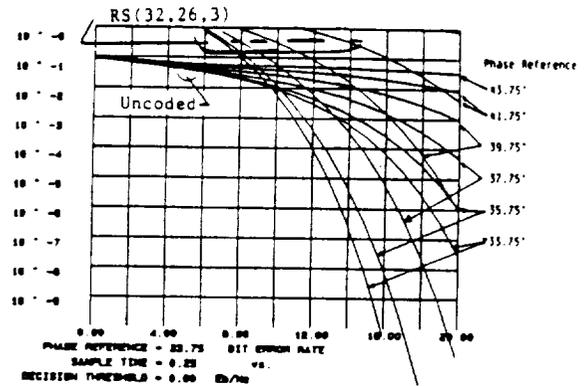
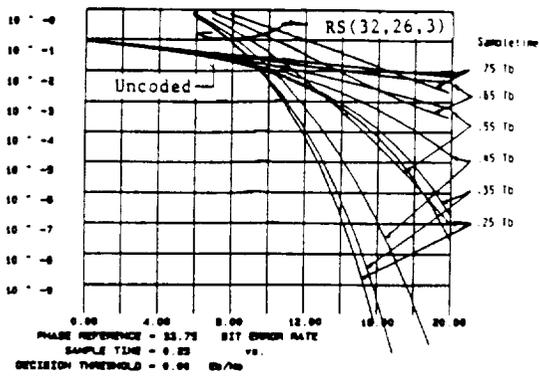
Figure 4.1 and Figure 4.2 show uncoded BER probability of 3 bits/symbol signal versus Eb/No. Receiver hardware impairment such as phase reference, sample time and bias level errors contribute to overall BER performance. 2° variation in the carrier phase reference, for example, can cause as much as 1.5 dB of degradation at uncoded 10₋₆ BER.

The BER probability degradation can be reduced by the use of error correcting hardware, as Figure 4.3 shows. It indicates that BER probability improvement can be seen as RS (32,30,1) CODEC is used.





UNCODED BER PROBABILITY vs. SAMPLE, PHASE AND BIAS ERRORS FOR 3 B/S SIGNAL
Figure 4.2



RS(32,26,1) CODED BER PROBABILITY vs. E_b/N_0 FOR 3 B/S SIGNAL
Figure 4.3

Table 4.1 provides the hardware impairment assessment for both the 2.5 bits/sec/hz and the 3 bits/sec/hz systems. The important bottom line on the performance assessment is that for coded 10^{-6} BER probability an E_b/N_0 of 18.55 dB will be required for 2.5 bits/sec/hz system and 21.65 dB for the 3 bits/sec/hz system.

HARDWARE IMPAIRMENT SUMMARY @ 10^{-6} BER
Table 4.1

PARAMETER	VALUE (comments)	DEGRADATION (dB)	
		2.5 B/s/hz	3 B/s/hz
MODULATOR PHASE ERROR	1°	.3	.3
CARRIER TRACK PHASE ERROR	2°	.75	.75
SYMBOL TIMING ERROR	(0.1)T _b	.2	.2
MATCHED FILTER MISMATCH		.4	.6
QUANTIZATION BIAS ERROR	5 BIT PHASE A/D (1%)	.3	.4
LIMITING IN IF	NON-IDEAL AGC & LIMITER	.1	.1
CHANNEL FILTER	UNEQUALIZED ISI	1.5	1.8
ADJACENT CHANNEL INT.	EQUAL AMPLITUDE, SEPARATED BY R _s	.5	2.0
CHANNEL NONLINEARITY	TWTA AT SATURATION	.5	.5
NET DEGRADATION		4.55	6.65
THEORETICAL E_b/N_0 REQUIRED FOR 10^{-6} BER		17.0	18.0
RESTRICTED CODEC GAIN		-3	-3
TOTAL E_b/N_0 REQUIRED FOR 10^{-6} BER		18.55	21.65

Acknowledgement

This paper is a summary of the ATDRS 300 MB/S Modem Program sponsored by NASA Goddard Space Flight Center under Contract #NAS5-30095. Major contributors to the report were Dr. Carl R. Ryan, Steve Kuh and Tyrone Strozier of the Motorola Strategic Electronics Division, Chandler, AZ.

References

- [1] C. Sundberg, "Continuous Phase Modulation," IEEE Comm. Mag., pp. 25-38, Apr. 1986.
- [2] S. Kuh & C. Ryan, "Continuous Phase Quadrature Phase Shift Keyed Signaling Technique," Milcom conf. 1988.
- [3] Code of Federal Regulations - Title 47, Telecommunications, The Office of the Federal Register National Archives and Records Administration, Washington, October, 1985.
- [4] S. Lin and P.J. Costello, Jr., "Error Control Coding". Engle Cliffs, New Jersey: Prentice - Hall, 1953.
- [5] W.W. Wu, David Haccour, Robert Peile, and Yasuo Hirata, "Coding for Satellite Communications," IEEE Journal on Selected Areas in Communications, Vol. SAC-5 No. 4, pp. 724-748, May 1987.
- [6] G. Maki, P. Owsley, K. Cameron, and J. Venbrux, "VLSI Reed Solomon Decoder Design," IEEE Communication Conference Proceedings, Vol. 3, October 1986.
- [7] C. Ryan and G. Huffman, "Baseband Implementation of Fast Acquisition Carrier Tracking Loop," Milcom conf. 1986.
- [8] C. Ryan, "Baseband Implementation of Fast Acquisition Symbol Synchronizer," Milcom conf. 1988.
- [9] R. Ziemer and C. Ryan, "Minimum-shift Keyed Modem Implementations for High Data Rates," IEEE Comm. Mag., vol. 21. no. 7, pp. 28-37, Oct. 1979.
- [10] F. Gardner, "Phase Lock Techniques," Wiley, New York, 1979.
- [11] T. Aulin, R. Rydbeck, and C. Sundberg, "Continuous Phase Modulation - Part II: Partial Response Signaling," IEEE Trans. on Comm., Vol. Com-29, No. 3, pp. 210-255, March 1981.
- [12] C. Ryan, A Hambley, and D. Vogt, "760-Mbit/s Serial MSK Microwave Modem," IEEE Trans. on Comm., Com-28, No. 5, pp. 771-777, May 1980.
- [13] R. Ziemer, C. Ryan, and J. Stillwell, "Conversion and Matched Filter Approximations for Serial Minimum Shift Keyed Modulation," IEEE Trans. Comm., pp. 495-509, March 1982.
- [14] C. Ryan and D. Jordan, "A Communication System Analysis Program for the IBM-PC," 5th PCCC 1986 Conference Proceedings, pp. 129-133, March 1986.
- [15] C. Ryan and D. Gottman, "A Phase Trajectory Converter for Partial Response Modulation," 1984 Midwest Symposium on Circuits and Systems, June 1984.
- [16] J. Anderson, T. Aulin and C. Sundberg, Digital Phase Modulation, Plenum, New York, 1986.
- [17] R. Blahut, "Theory and Practice of Error Control Codes", Reading, MA: Addison-Wesley, 1983.
- [18] W. W. Peterson and E. Weldon, "Error Correcting Codes", 2nd edition, Cambridge, MA: M.I.T. Pres, 1972.

**MODULATION AND CODING TECHNOLOGY
FOR DEEP SPACE AND SATELLITE APPLICATIONS**
(Invited Paper)

J. H. Yuen and W. Rafferty
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, CA 91109

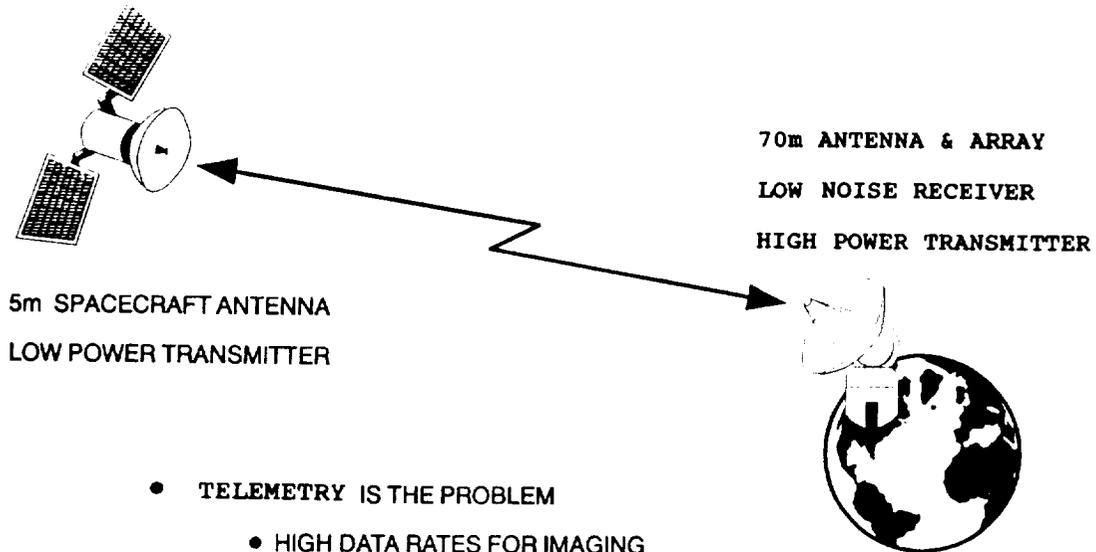
Abstract

Modulation and coding research and development activities at the Jet Propulsion Laboratory currently emphasize the following two areas: Deep Space Communications Systems and advanced near-earth Commercial Satellite Communications Systems. The Deep Space Communication channel is extremely signal-to-noise ratio limited and has long transmission delay. The near-earth (GEO and LEO) satellite channel is bandwidth limited with fading and multipath.

Recent code-search efforts at JPL have found a long constraint, low rate convolutional code (15, 1/6) which, when concatenated with a 10 bit Reed-Solomon (RS) code provides a 2.1 dB gain over that of the Voyager Spacecraft - the current standard. The new JPL code is only 2 dB from the theoretical Shannon limit. A flight qualified version of the (15, 1/6) convolutional encoder has been implemented on the Galileo Spacecraft - to be launched later this year. This will result in increased data return from Jupiter in the 1990s. A decoder for this class of codes is under development at JPL using parallel processing algorithms and VLSI technology. An Image Statistics Decoder (ISD) has been developed, which uses the source statistics of the image (or picture) to modify the standard Viterbi decoding algorithm in decoding convolutionally encoded Voyager images. This ISD, which provides as much as 3 dB coding gain in the region of interest, will be used as a backup decoder for Voyager's Neptune Encounter in August 1989. Other JPL activities in modulation and coding for deep space applications will also be discussed.

NASA has played a leading role in the development of satellite based, fixed and mobile communications for the U.S. with the work at JPL focused on the L-band, mobile link. This link has necessitated the development of a new highly bandwidth and power efficient digital modem. A unique 4.8 kbps, rate 2/3 8 DPSK Trellis Coded Modulation (TCM) scheme has been derived and implemented which is robust in the presence of Rician fading, and doppler shifts up to 10% of the transmitted symbol rate (2.4 ksps) for a basic 5 kHz channel width. A compatible 4.8 kbps speech compressor has also been developed which achieves good intelligibility, and sound "natural" at a low implementation complexity. New JPL activities in the Satcom area include: meeting personal communications needs at the turn of the 21st Century, by exploiting Ka-band; and developing the subsystem technology for the interconnection of satellite resources by using high rate optical inter-satellite links.

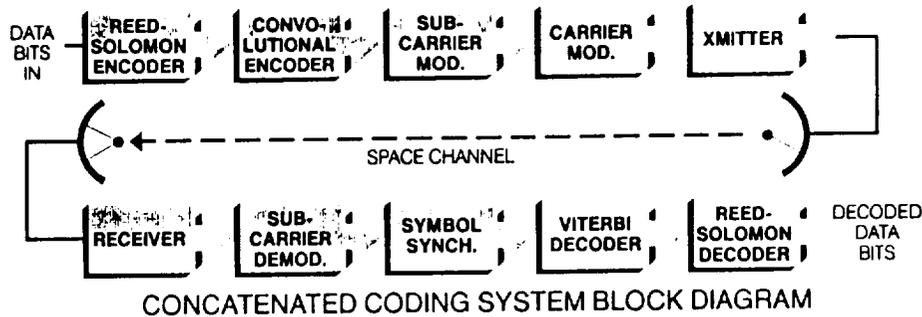
JET PROPULSION LABORATORY **DEEP SPACE COMMUNICATIONS**



- **TELEMETRY IS THE PROBLEM**
 - HIGH DATA RATES FOR IMAGING
 - LOW SNRs
- **CODING IS CRITICAL TO TELEMETRY**
 - ENCODERS MUST BE SMALL, LIGHT, LOW POWER
 - DECODERS TEND TO BE VERY COMPLEX

JET PROPULSION LABORATORY

THE 2 dB CODE SEARCH



- BASELINE PERFORMANCE: BER = 10^{-6}
- BASELINE CODE: VOYAGER AT URANUS

(7, 1/2) + 8-bit RS
Required $E_b/N_0 = 2.53$ dB

- SIMULATED PERFORMANCE OF CONCATENATED CODES WITH 10-bit REED-SOLOMON OUTER CODE

INNER CONVOLUTIONAL CODES	E_b/N_0	
(13, 1/4)	0.84 dB	
(13, 1/5)	0.68 dB	
(14, 1/4)	0.74 dB	
(14, 1/5)	0.57 dB	
(15, 1/4)	0.80 dB	
(15, 1/5)	0.50 dB	
(14, 1/6)	0.47 dB	
(15, 1/6)	0.42 dB	= 2.11 dB Gain

We search for codes that will provide significant improvement, say 2 dB, over our Voyager baseline system (7, 1/2) convolutional code as the inner code (with Viterbi decoding,) and an 8-bit (255, 223) Reed-Solomon code as the outer code. We use the criterion of minimizing required bit SNR, for a given value of desired BER, for the goodness of code. The code space is astronomically large for long constraint length low rate convolutional codes. Using educated guesses combined with the idea that good codes generate good codes, we selectively search for good codes. These codes performance are determined by computer simulation. The decoder complexity is manageable by using concurrent processing technique and VLSI technology.

JET PROPULSION LABORATORY

IMAGE STATISTICS DECODER (ISD)

INFORMATION SYMBOLS $\{b_1, b_2, \dots, b_n\}$

CODED SYMBOLS $\{s_1, s_2, \dots, s_m\}$

RECEIVED SYMBOLS $\{r_1, r_2, \dots, r_m\}$

$$D_j = |b_j - b_{j-1}|$$

σ^2 FUNCTION OF BIT SNR

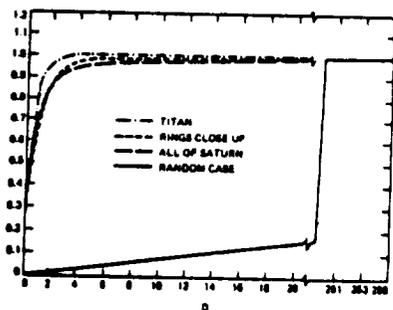
ISD MINIMIZES

$$\sum_1 \frac{(r_1 - s_1)^2}{\sigma^2} - \sum_j \ln P(b_j | D_j)$$

MINIMIZE THIS TERM

ONLY, IF INFORMATION BYTES

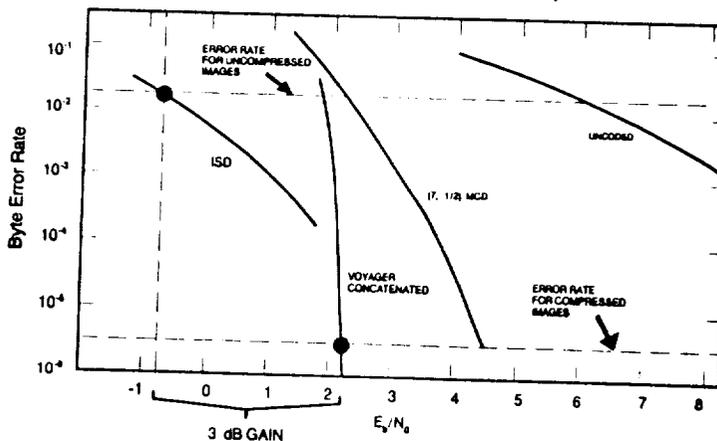
ARE ASSUMED INDEPENDENT



Distributions of Adjacent Pixel Variation D for 3 different Voyager Images and the random case

ISD PERFORMANCE

Image Byte Errors as Compared to Data Compression



Maximum likelihood (or Viterbi) assumes that all codewords are a priori equally likely to be transmitted, this decoding scheme retrieves the most likely sent codeword. In some cases, though, codewords are not all equally likely to be transmitted. In Voyager images, for example, pixel to pixel variations are not completely random. They are much more likely to be small than large. In this case, a decoder which makes use of the source statistics should perform better than a Viterbi decoder. (Image compression uses these statistics to lower the transmission rate and thus raise symbol SNR, but some Voyager images are sent uncompressed because of spacecraft limitations; also, an alternative would be valuable in the unlikely event of a data compressor failure before Neptune encounter in 1989.) This is exactly what our ISD does. It amounts to an additional term to the usual Viterbi decoder.

JET PROPULSION LABORATORY DE CODER

- Objectives:

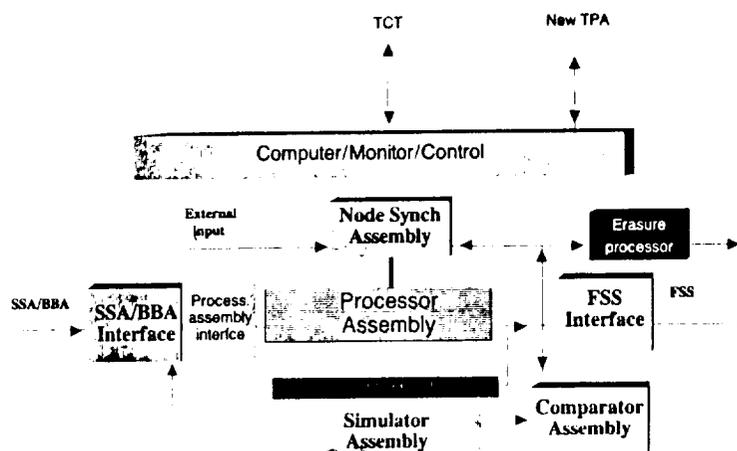
- ✓ Develop, Build, test, and demonstrate a prototype Viterbr decoder for the DSN capable of using (15,1/6) convolucional codes, leading to flight tests with Galileo's (15,1/4) encoder

- Requirements:

- ✓ Performance:

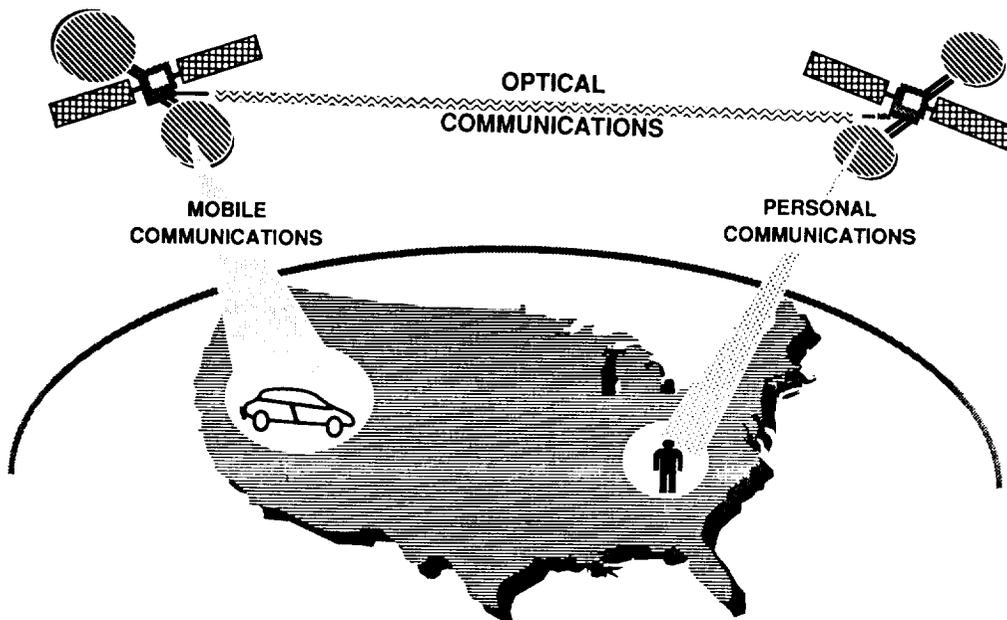
- Constraint length up to 15, programmable
- Code rate 1/2 to 1/6, programmable
- Data rate 1.1 Mbit/s (Galileo 115, 134 Kb/s)
- Node synch using frame synch pattern, programmable
- Node synch using metric growth rate
- Include full self-test capability

- ✓ DSN Compatible



The major complexity driver of the decoder is constraint length, since the amount of hardware is roughly proportional to the number of states which is 2 to the (K-1), where K is the constraint length. Hence, a decoder for K = 15 is approximately 256 times more complex than a decoder for K = 7. Using concurrent processing techniques, such a complex decoder can be built, with current VLSI technology, within reasonable size limitations. The decoder is under development. It will be ready in 1991, before Galileo reaches Jupiter in 1995.

JET PROPULSION LABORATORY
MODULATION & CODING FOR SATCOM APPLICATIONS



**MODULATION & CODING ARE CRITICAL TO
EFFICIENT USE OF SATELLITE RESOURCES**

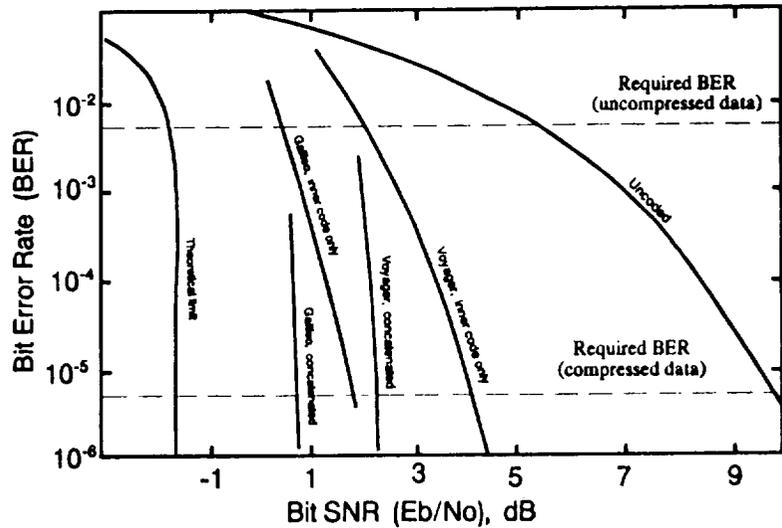
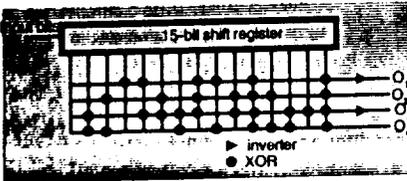
- BANDWIDTH
- POWER
- ORBITAL SLOT

JET PROPULSION LABORATORY

Performance of Galileo Codes

The new encoder....

✓ 26 resistors, 39 capacitors, 20 ICs

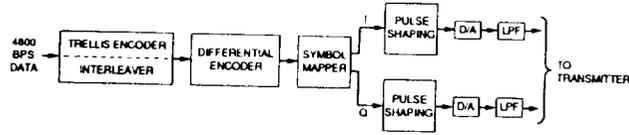


Due to the Space Shuttle Challenger's accident, the launch of the Galileo spacecraft to orbit Jupiter (and to drop a probe into the atmosphere of Jupiter) was delayed. The delay will require new trajectory that makes the communication distance from Galileo to Earth much longer than the original trajectory. We install a (15, 1/4) convolutional code on Galileo -- the RS code remains to be 8-bit (255, 223). This gives about 1.5 dB over the original (7, 1/2) code. This provides significant performance improvement with minimal impact on the existing Galileo design.

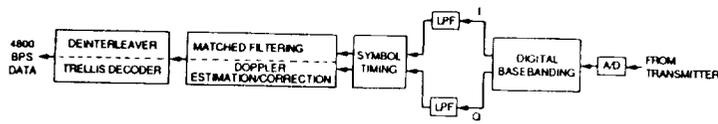


JET PROPULSION LABORATORY 4800 BPS 8DPSK TCM MODEM

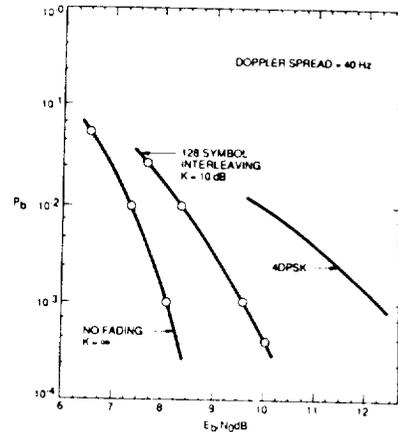
MODULATOR



DEMODULATOR

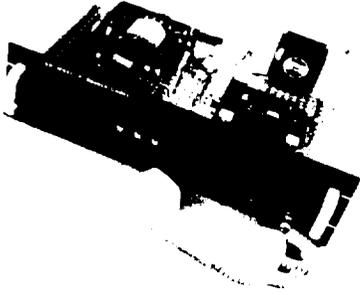


SIMULATION RESULTS

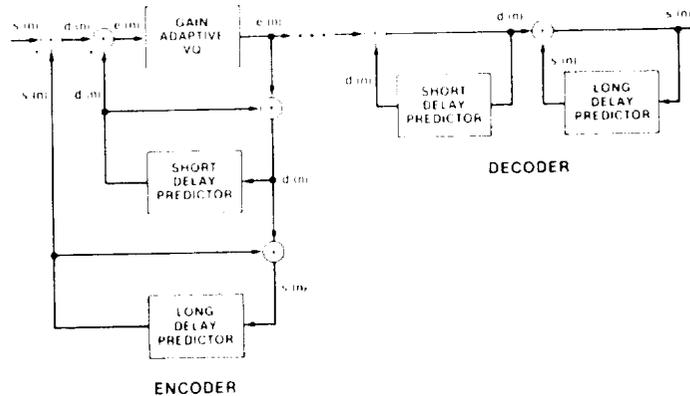


THE MSAT-X 8DPSK TCM MODEM IS A POWER AND BANDWIDTH EFFICIENT, NARROWBAND MODEM DESIGNED TO COMBAT THE PROPAGATION EFFECTS OF THE L-BAND LAND-MOBILE SATELLITE CHANNEL. THE TYPICAL CHANNEL IMPAIRMENTS CONSIST OF MULTIPATH (RICIAN) FADING AND VEGETATIVE SHADOWING. THE MODULATOR TRELLIS ENCODES, INTERLEAVES, AND DIFFERENTIALLY ENCODES THE INPUT DATA BEFORE CONVERTING THE DATA TO PULSE SHAPED I AND Q WAVEFORMS FOR TRANSMISSION THROUGH THE CHANNEL. THE DEMODULATOR IS IMPLEMENTED WITH A FEEDFORWARD ARCHITECTURE TO COMBAT THE EFFECTS OF FADES, AND EMPLOYS DIFFERENTIAL DETECTION USING A NOVEL MATCHED FILTERING AND DOPPLER ESTIMATION/CORRECTION ALGORITHM TO RECOVER THE TRANSMITTED DATA. THE DATA IS THEN DEINTERLEAVED AND DECODED TO PRODUCE AN ESTIMATE OF THE BASEBAND DIGITAL DATA. EXPERIMENTAL RESULTS HAVE SHOWN THAT THE CURRENT IMPLEMENTATION OF THE MODEM PERFORMS WITHIN 1 dB OF SIMULATION RESULTS.

JPL JET PROPULSION LABORATORY
4.8 kbps DIGITAL SPEECH COMPRESSION



**VECTOR ADAPTIVE PREDICTIVE CODING
 UC-SANTA BARBARA**

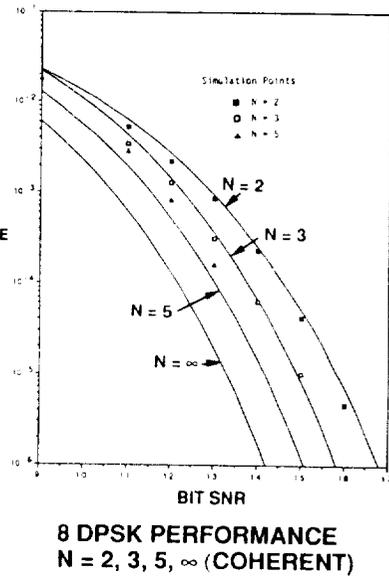
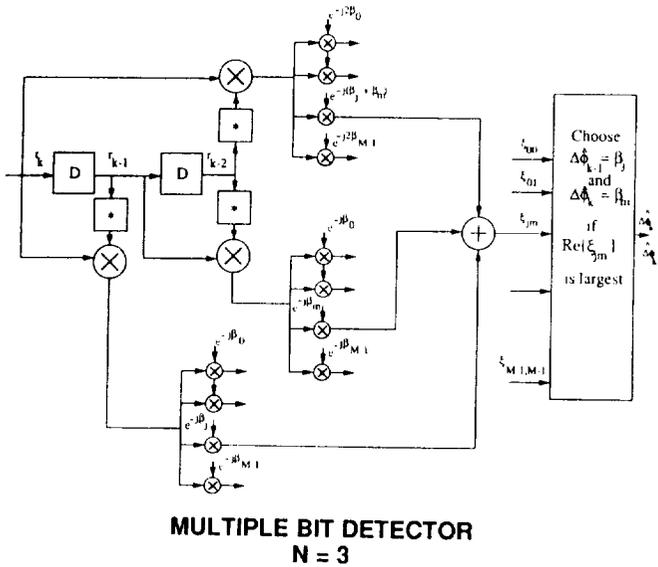


UCSB VECTOR ADAPTIVE PREDICTIVE CODING

THE VAPC ALGORITHM COMBINES LINEAR PREDICTION WITH VECTOR QUANTIZATION. ADAPTIVE LINEAR PREDICTORS ARE UTILIZED TO REMOVE REDUNDANCY FROM THE SPEECH WAVEFORMS. THE REMAINING PREDICTION ERROR IS THEN QUANTIZED BY EMPLOYING VECTOR QUANTIZATION. THE USE OF VECTOR QUANTIZATION ALLOWS THE CODING OF THE ERROR SIGNAL AT RATES BELOW ONE BIT PER SAMPLE -- AN ESSENTIAL CHARACTERISTIC FOR LOW BIT RATE COMPRESSION.

THE ENCODING PROCESS BEGINS WITH A LONG DELAY PREDICTOR TO REMOVE THE REDUNDANCY CORRESPONDING TO THE PITCH STRUCTURE OF SPEECH. A SHORT DELAY PREDICTOR FOLLOWS TO REMOVE INFORMATION ROUGHLY CORRESPONDING TO THE FORMANT STRUCTURE OF SPEECH. THE REMAINING ERROR SIGNAL IS QUANTIZED AS TIME SEQUENCES OR VECTORS BY EXHAUSTIVELY COMPARING THE ERROR VECTORS TO STORED VECTORS AND CHOOSING THE STORED VALUES THAT MINIMIZE THE MEAN SQUARED ERROR.

JET PROPULSION LABORATORY MULTIPLE SYMBOL DIFFERENTIAL DETECTION OF MPSK

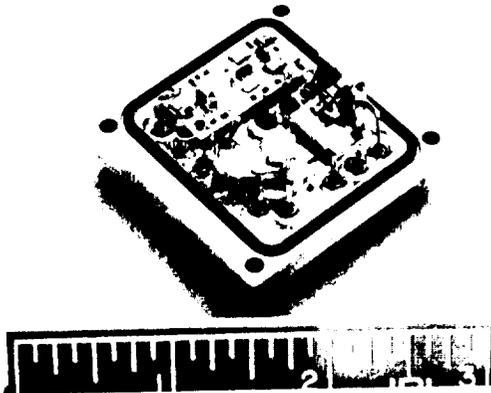


CONVENTIONAL DIFFERENTIAL DETECTION OF MPSK (MDPSK) USES THE PREVIOUS SYMBOL AS A DEMODULATION REFERENCE FOR THE CURRENT SYMBOL. THE ERROR PROBABILITY PERFORMANCE OF BINARY DPSK VARIES AS $\exp(-E_s/N_0)$.

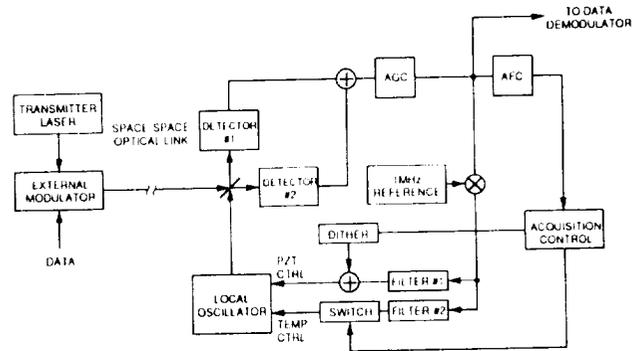
MULTIPLE SYMBOL DIFFERENTIAL DETECTION OF MPSK OBSERVES THE RECEIVED SIGNAL PLUS NOISE OVER N (MORE THAN TWO) SYMBOL INTERVALS. A MAXIMUM-LIKELIHOOD SEQUENCE ESTIMATION ALGORITHM IS USED TO DETECT THE CURRENT SYMBOL USING ALL OF THE PREVIOUS SYMBOLS. IT REQUIRES IDENTICAL DIFFERENTIAL ENCODING OF THE INPUT DATA PHASES AS FOR CONVENTIONAL (N=2) DIFFERENTIAL DETECTION. THE ERROR PROBABILITY VARIES BETWEEN THAT FOR CONVENTIONAL DIFFERENTIAL DETECTION AND COHERENT DETECTION. IN THE LIMIT OF INFINITE SYMBOL OBSERVATION, THE ERROR PROBABILITY BECOMES IDENTICAL TO THAT OF COHERENT DETECTION OF MPSK WITH DIFFERENTIALLY ENCODED INPUT PHASES. IN PRACTICE, WITH ONLY A FEW ADDITIONAL OBSERVATION INTERVALS, ONE CAN APPROACH COHERENT DETECTION PERFORMANCE.



JET PROPULSION LABORATORY ADVANCED OPTICAL MODULATION



FREQUENCY STABILIZED LASER WITH
TEMPERATURE AND PIEZO-ELECTRIC
TUNING CAPABILITIES



BLOCK DIAGRAM OF A COHERENT
OPTICAL LINK

THIS WORK IS FOCUSED ON THE KEY TECHNOLOGIES REQUIRED FOR THE DEVELOPMENT OF COHERENT FREE SPACE OPTICAL COMMUNICATIONS. RECENT DEVELOPMENTS OF FREQUENCY-STABILIZED SOLID STATE LASERS WILL PERMIT THE REALIZATION OF PHASE COHERENT FREE-SPACE OPTICAL COMMUNICATION SYSTEMS PREVIOUSLY NOT ACHIEVABLE WITH SEMICONDUCTOR LASERS. POTENTIAL DATA MODULATION SCHEMES FOR COHERENT OPTICAL LINKS INCLUDE PULSE POSITION MODULATION, FREQUENCY SHIFT KEYING AND PHASE SHIFT KEYING. CURRENTLY, WORK IS UNDERWAY FOR A LOW DATA RATE PHASE COHERENT SYSTEM DEMONSTRATION USING BINARY PPM. THE EVENTUAL GOAL IS TO DEVELOP THE TECHNOLOGY AND SYSTEM ARCHITECTURE SUITABLE FOR HIGH DATA RATE PSK SYSTEMS.

JET PROPULSION LABORATORY
OTHER ACTIVITIES

- 0 CPM/TRELLIS ENCODING
 - 0 MOBILE SATELLITE APPLICATIONS
 - 0 OFFERS GOOD POWER PERFORMANCE AND SPECTRAL EFFICIENCY
- 0 CODING DIVERSITY FOR SOUND BROADCASTING SATELLITE (SBSAT) APPLICATIONS
 - 0 TRELLIS CODING COMBINED WITH MULTIPLE SYMBOL DIFFERENTIAL DETECTION OF MPSK HAS ADVANTAGES OVER CONVENTIONAL DIFFERENTIAL DETECTION OF CONVOLUTIONALLY ENCODED MPSK
 - 0 ALLOWS MORE CHANNELS TO BE ACCOMMODATED WITHIN A GIVEN BANDWIDTH AND AVAILABLE SATELLITE POWER
 - 0 ENABLES DIVERSITY RECEPTION
- 0 VARIABLE RATE MODEM FOR HIGH FREQUENCY BAND PERSONAL ACCESS SATELLITE SYSTEM (PASS)
 - 0 A PRACTICAL WAY TO COMBAT RAIN ATTENUATION FOR HIGH FREQUENCY COMMUNICATIONS CHANNEL

CONTINUOUS PHASE MODULATION (CPM) HAS A CONSTANT ENVELOPE AND GOOD SPECTRAL PROPERTIES, I.E., LOW OUT-OF-BAND POWER. CPM COUPLED WITH TRELLIS ENCODING CAN EFFICIENTLY UTILIZE THE AVAILABLE SATELLITE POWER AND BANDWIDTH, BOTH OF WHICH ARE PRECIOUS FOR A MOBILE SATELLITE SYSTEM.

SOUND BROADCASTING SATELLITE (SBSAT) CHANNELS SUFFER FREQUENCY AND TIME SELECTIVE FADING, WHICH CAN BE OVERCOME THROUGH CHANNEL DIVERSITY, I.E., BY PROVIDING A LARGE NUMBER OF CHANNELS THAT USERS CAN SELECTIVELY TUNE IN. TRELLIS CODING COMBINED WITH MULTIPLE SYMBOL DIFFERENTIAL DETECTION OF MPSK HAS BETTER SPECTRAL EFFICIENCY AND POWER PERFORMANCE THAN CONVENTIONAL DIFFERENTIAL DETECTION OF CONVOLUTIONALLY ENCODED MPSK, HENCE MORE CHANNELS OR SELECTION FOR A GIVEN BANDWIDTH AND SATELLITE POWER.

A PERSONAL ACCESS SATELLITE SYSTEM (PASS) OPERATING AT KA-BAND WOULD PROVIDE A DIVERSITY OF SERVICES TO USERS IN CONUS USING SMALL HAND-HELD TERMINALS. TO COMBAT THE SEVERE RAIN ATTENUATION AT KA BAND, A VARIABLE RATE MODEM (.1- 4.8 KBPS) IS BEING INVESTIGATED. THIS MODEM CAN AUTOMATICALLY DETECT AND/OR INITIATE THE CHANGE OF DATA RATE WITHOUT NETWORK COORDINATION.

DIGITAL SYNCHRONIZATION AND COMMUNICATION TECHNIQUES

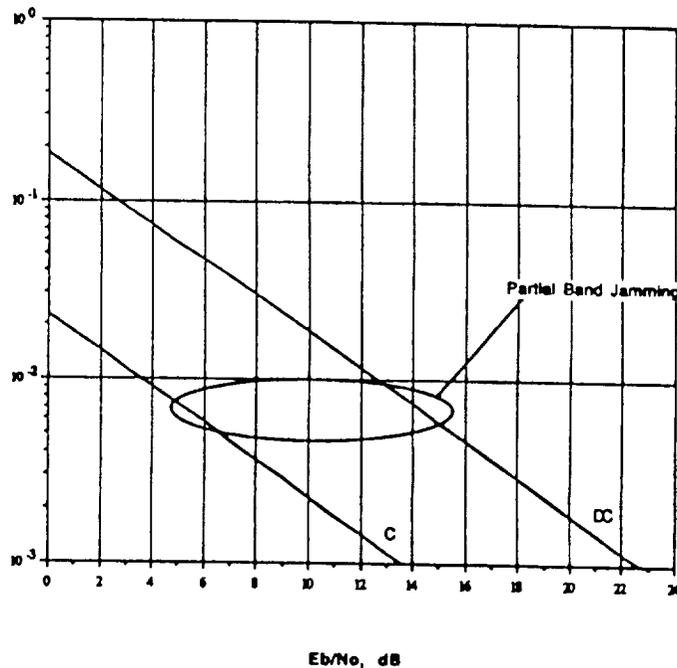
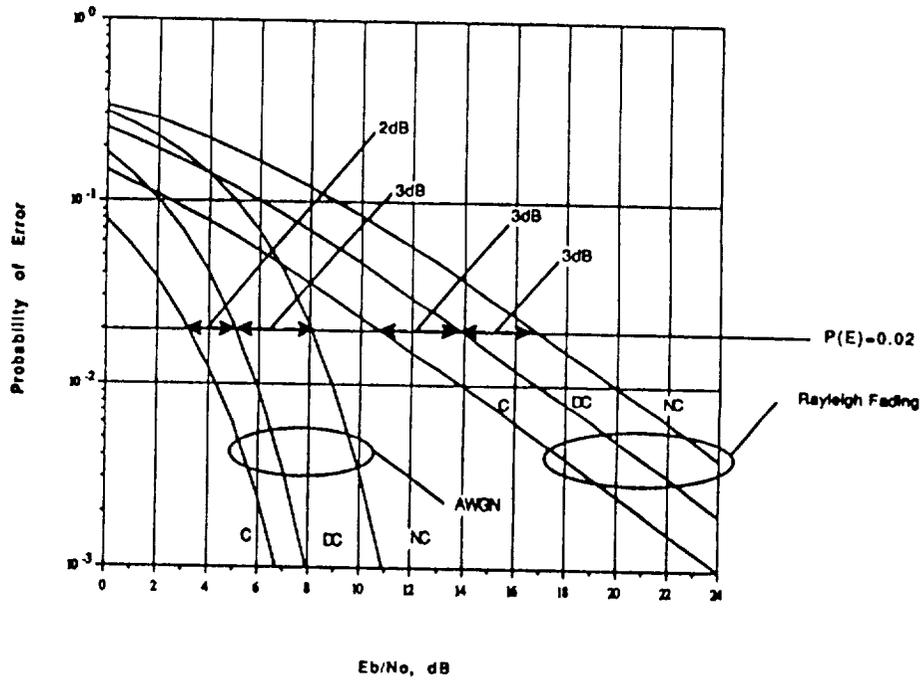
William C. Lindsey
Lincom Corporation
Los Angeles, California 90024

RESEARCH IN DIGITAL SYNCHRONIZATION AND COMMUNICATIONS

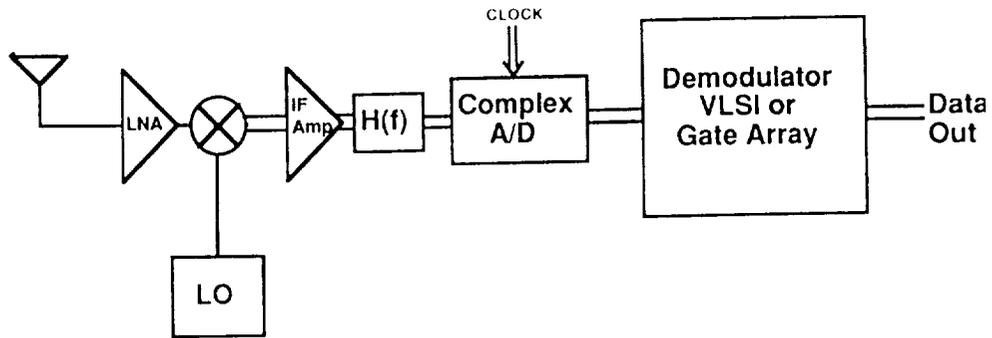
- DIGITAL CODING/MODULATION UNDER INVESTIGATION
 - MPSK (BPSK, QPSK, OQPSK, MSK)
 - MDPSK (DBPSK, DQPSK, ODQPSK, DMSK) } OFFSET VS NON-OFFSET
 - CONVOLUTIONAL CODES AND TRELLIS-CODED MODULATION
 - BANDWIDTH EFFICIENT
- CHANNELS UNDER INVESTIGATION
 - AWGN
 - RAYLEIGH/RICE/SCINTILLATION
 - JAMMED
- RESEARCH EMPHASIZES
 - ACQ {
 - RAPID ACQUISITION WITH HIGH PROBABILITY
 - AVOIDING HANG-UP DURING ACQUISITION
 - TRACK {
 - AVOIDING CYCLE SLIPPING
 - MINIMIZE TRACKING JITTER
 - ELIMINATE PHASE AMBIGUITIES
 - ACHIEVING PERFORMANCE OF CODED-COHERENT COMMUNICATIONS

DIGITAL SYNCHRONIZATION PROJECT MOTIVATION

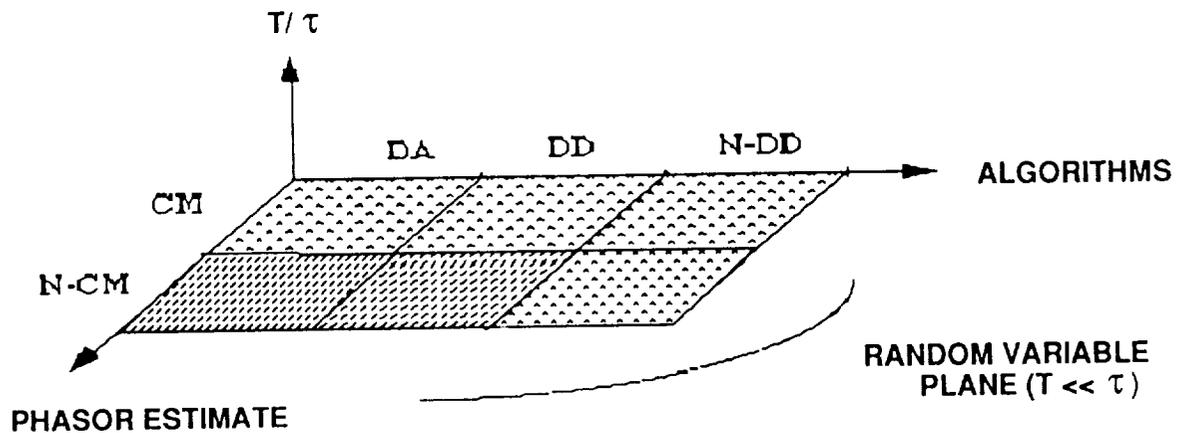
- FUTURE COMMUNICATION MODEMS ARE LIKELY TOO EMPLOY ALL DIGITAL IMPLEMENTATIONS AS THE DIGITAL SIGNAL PROCESSING SPEED BARRIER BETWEEN DIGITAL AND ANALOG HARDWARE RISES DUE TO EMERGING TECHNOLOGIES, E.G., VLSI.
- COHERENT (C) VS. DIFFERENTIALLY COHERENT (DC) VS. NONCOHERENT (NC) DETECTION IN MODEMS



Desired Modem Implementation



DIGITAL SYNCHRONIZATION PROBLEM SPACE



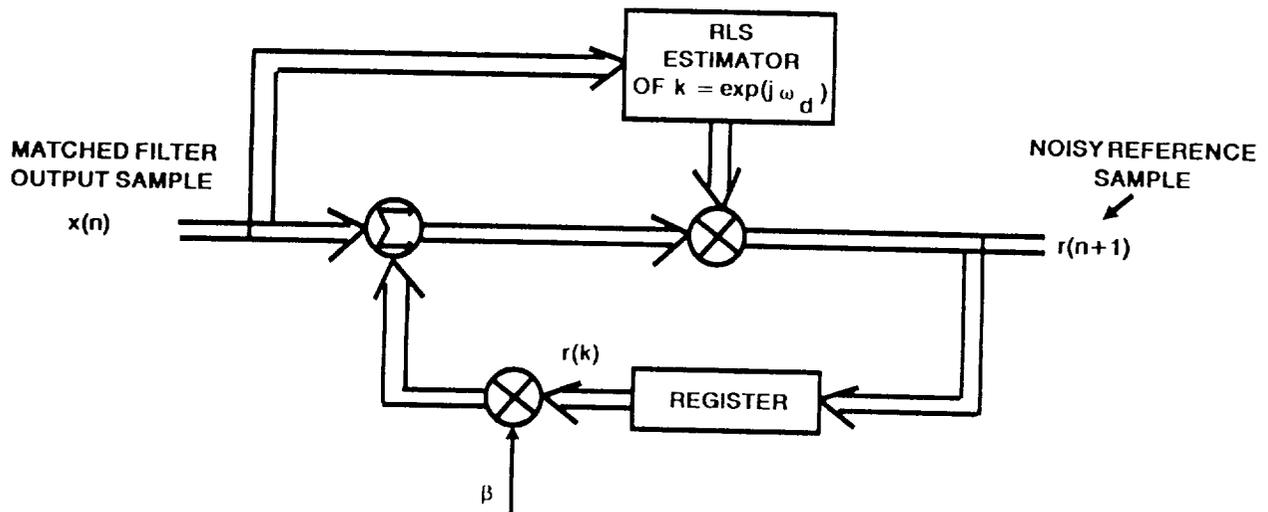
- CM: CONSTANT MODULUS
- N-CM: NON-CONSTANT MODULUS

- DA: DATA-AIDED
- DD: DECISION DIRECTED
- N-DD: NON-DECISION DIRECTED

SALIENT CHARACTERISTICS OF OPEN LOOP DIGITAL SYNCHRONIZERS

- DERIVED FROM ADAPTIVE FILTERING THEORY
- DO NOT REQUIRE LOCALLY GENERATED SYNC REFERENCE BY MEANS OF A VCO OR NCO
- SYNC REFERENCE IS NON-CONSTANT MODULUS
- DOES NOT REQUIRE A PHASE-ERROR MEASUREMENT TO UPDATE PHASE ESTIMATE

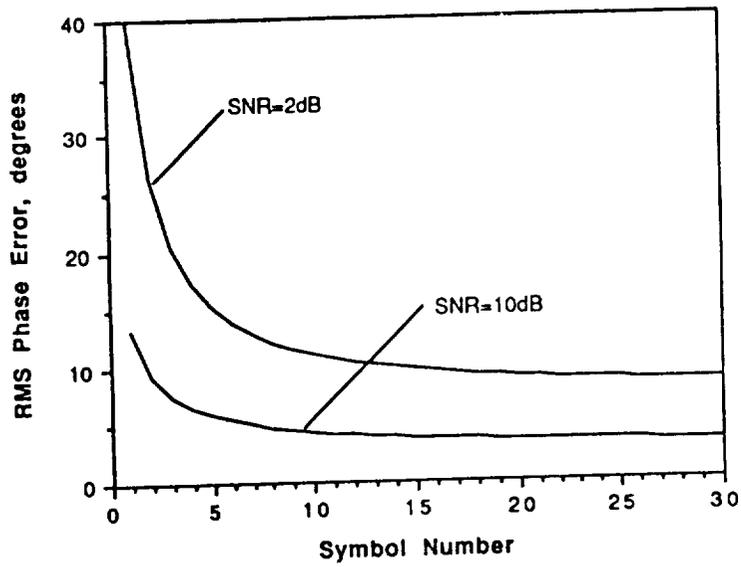
OPEN LOOP PHASE AND FREQUENCY ESTIMATOR



β - SAMPLE WEIGHTING FACTOR

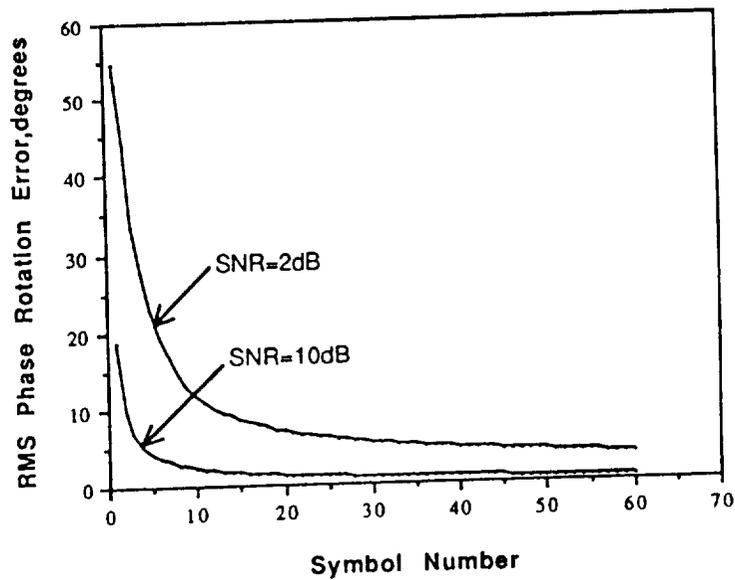
EXPONENTIALLY WEIGHTED PHASE ESTIMATOR LEARNING CURVES.

$$\beta = 0.875$$

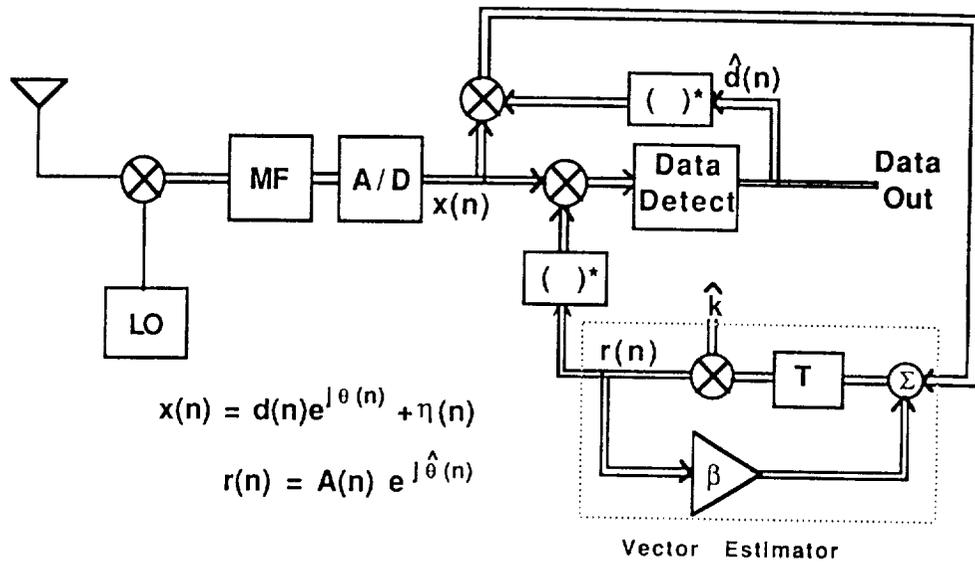


SYMBOL TO SYMBOL PHASE ROTATION LEARNING CURVE.

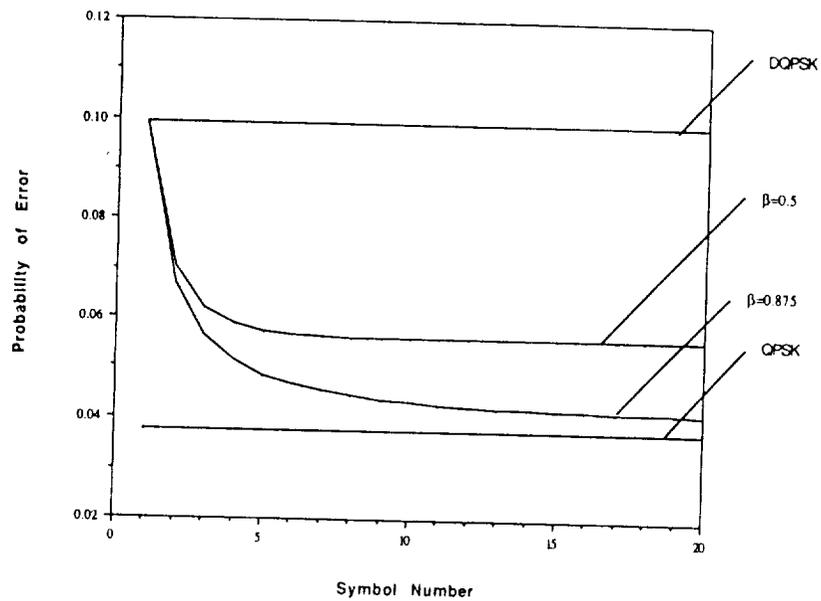
$$\omega_0 = 1.0 \text{ radians/symbol}$$



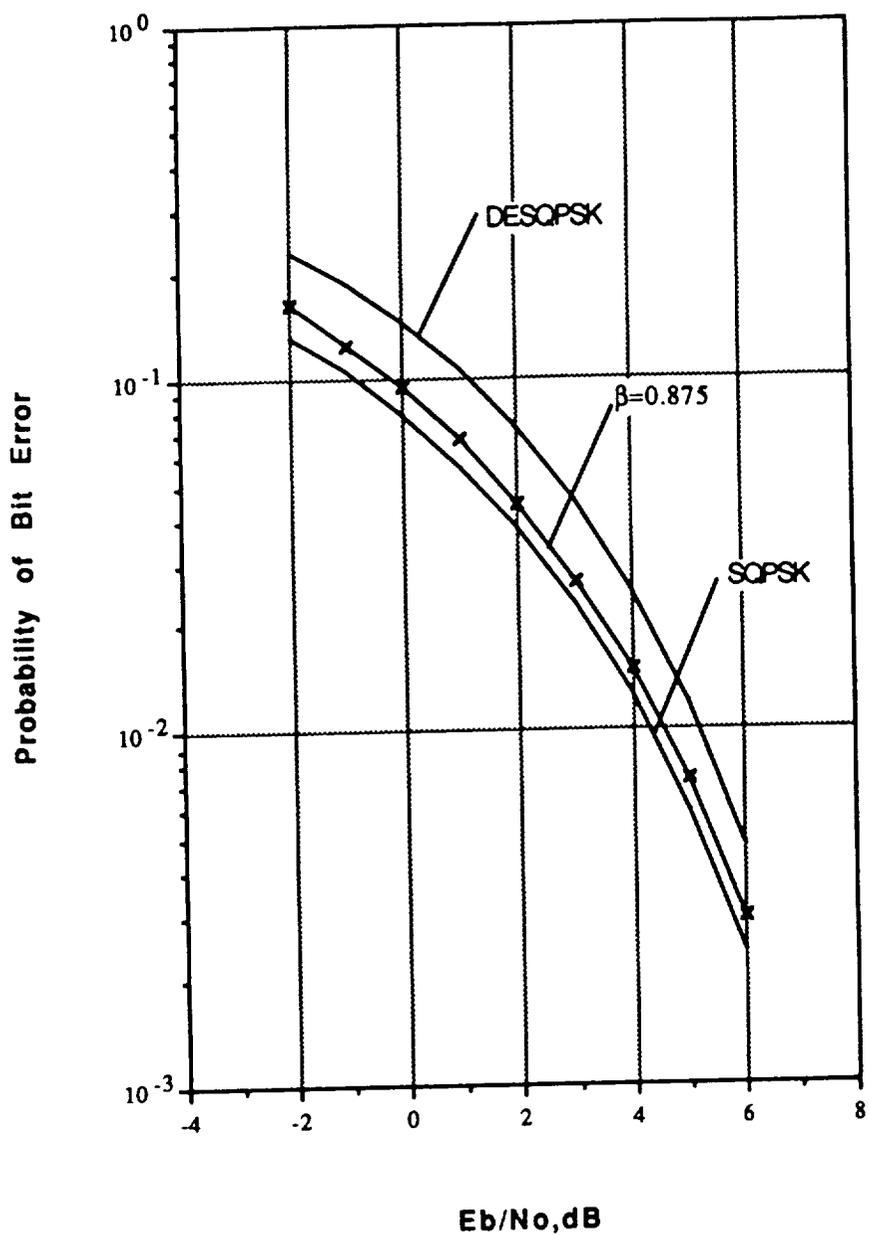
A Digital Receiver Structure Utilizing an Open Loop Estimator in a Decision-Directed Architecture



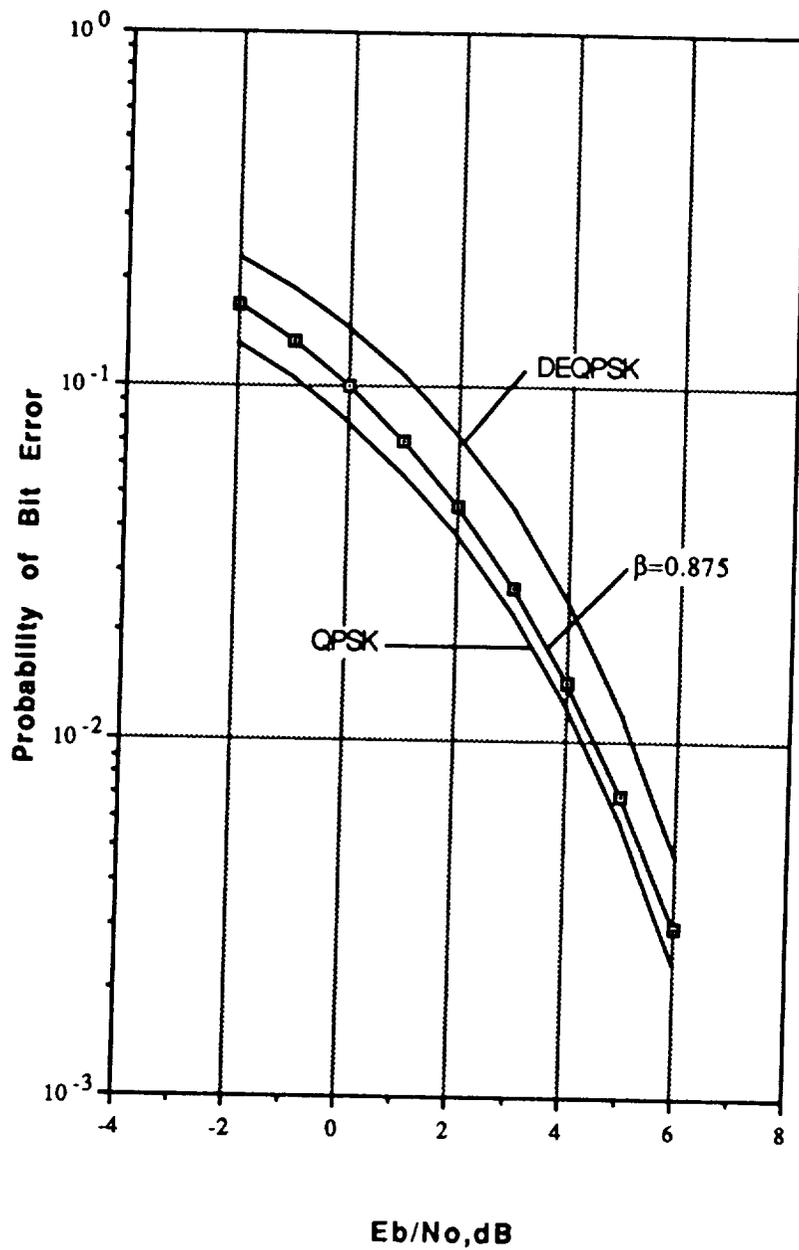
The BER Learning Curve of the Exponentially Weighted Estimator for QPSK Modulation ($E_b/N_0=2\text{dB}$)



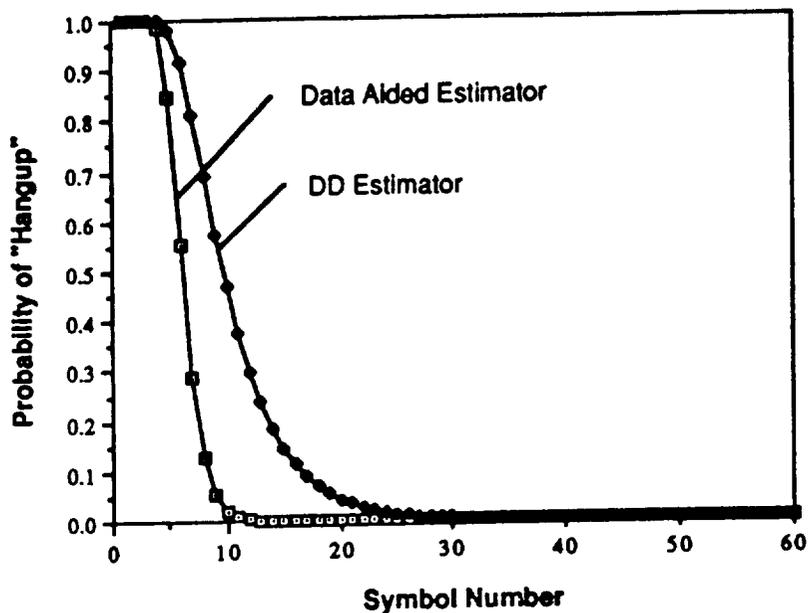
SIMULATED STEADY STATE WATERFALL CURVE OF THE EW DD ESTIMATOR FOR SQPSK MODULATION. $\beta = 0.875$



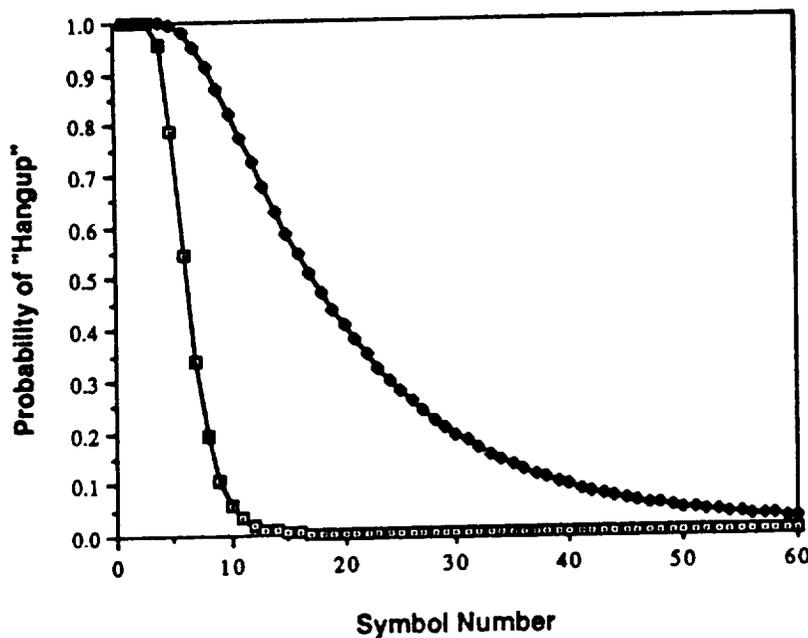
SIMULATED STEADY STATE WATERFALL CURVE OF THE EW DD ESTIMATOR FOR QPSK MODULATION. $\beta = 0.875$



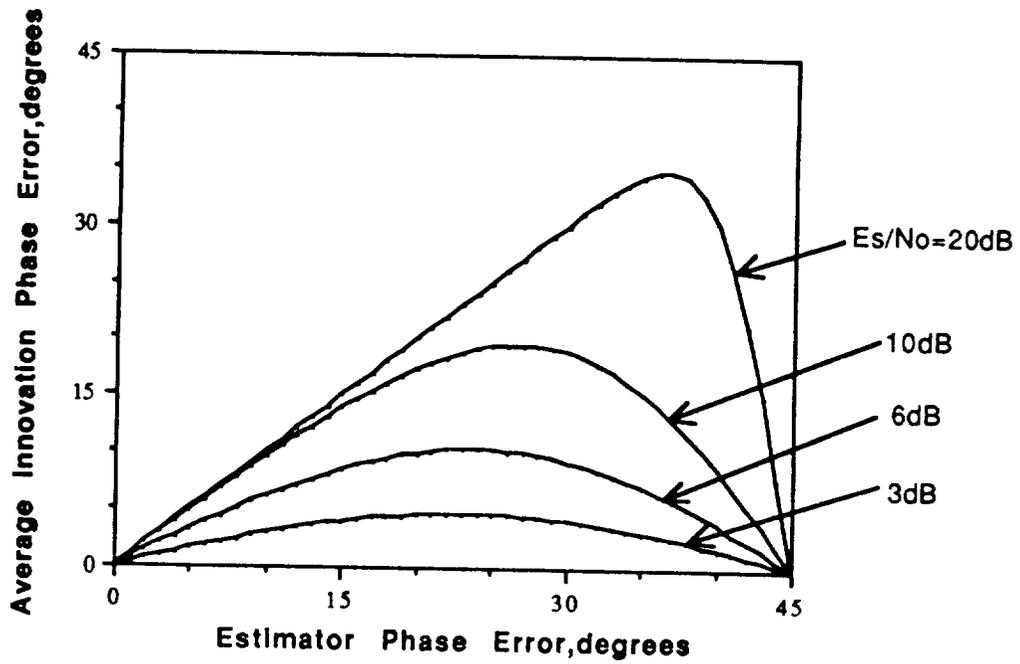
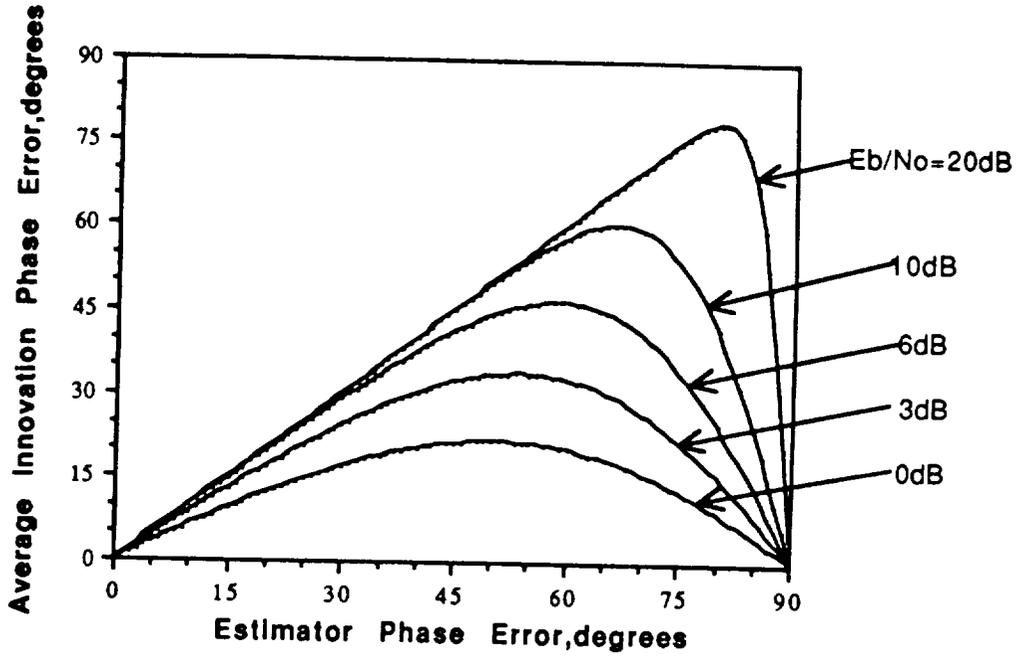
PROBABILITY OF REMAINING IN A HANGUP CONDITION FOR BPSK MODULATION. $R_b = 2\text{dB}$, $\beta = 0.875$.



PROBABILITY OF REMAINING IN A HANGUP CONDITION FOR QPSK MODULATION. $R_b = 2\text{dB}$, $\beta = 0.875$.



'S' CURVE FOR A DECISION-DIRECTED BPSK AND QPSK LOOP EW ESTIMATORS



Motivation For Research

- **Modems used in burst mode communication systems (TDMA or FHSS) or a fading channel typically use noncoherent demodulation techniques**
 - **PLL structures and fast acquisition with high probability requirements are not compatible**
 - **Coherent demodulation improves the performance**
- **Technology advances favor digital receiver structures**
 - **VLSI or gate array implementations can significantly reduce the cost, size, and possibly power consumption while improving the reliability of modems.**



Bandwidth Efficient Coding for Satellite Communications*

Shu Lin
University of Hawaii
Honolulu, Hawaii 96822

Daniel J. Costello, Jr.
University of Notre Dame
Notre Dame, Indiana 46556

Warner H. Miller
James C. Morakis
William B. Poland, Jr.
Goddard Space Flight Center
Greenbelt, Maryland 20771

RESEARCH PURPOSE

The **purpose** of this research is to devise an error control coding scheme to achieve **large coding gain** and **high reliability** by using coded modulation with **reduced** decoding complexity.

* Supported by NASA Grants NAG 5-931 and NAG 5-557.

CODED MODULATION ALONE

- To achieve a 3 to 5 dB coding gain and moderate reliability, the decoding complexity is quite modest.
- In fact, to achieve a 3 dB coding gain, the decoding complexity is quite simple, no matter whether **trellis coded modulation (TCM)** or **block coded modulation (BCM)** is used.
- However, to achieve coding gains exceeding 5 dB, the decoding complexity increases **drastically**, and the implementation of the decoder becomes very expensive and unpractical.

A BASIC QUESTION

- How can we achieve large coding gains and high reliability by using coded modulation with reduced decoding complexity ?

AN ANSWER

- Use coded modulation in conjunction with concatenated (or cascaded) coding.
- A good short bandwidth efficient modulation code (trellis or block) is used as the inner code and relatively powerful Reed–Solomon (RS) code is used as the outer code.
- With properly chosen inner and outer codes, a concatenated coded modulation scheme not only can achieve large coding gains and high reliability with good bandwidth efficiency but also can be practically implemented
- This combination of coded modulation and concatenated coding really offers a way of achieving the best of three worlds, reliability and coding gain, bandwidth efficiency and decoding complexity.

PROPOSED SCHEME

- A concatenated (or cascaded) coded modulation scheme.
- For NASA high-speed satellite communications for large data file transfer where very high reliability is required.
- The outer code C_2 is an (n_2, k_2) RS code with symbols from GF (2^b) .
- The outer code is **interleaved** to a **depth** of m .
- The inner code is a bandwidth efficient **block M-ary PSK** code of length n_1 and dimension
$$k_1 = mb.$$
- Under the same research project, we have investigated concatenated coding with TCM inner codes.

THE OVERALL CONCATENATED CODED MODULATION SCHEME

- The outer code C_2 is an (n_2, k_2) RS code over $GF(2^b)$, which is designed to correct t_2 or fewer symbol errors with $0 \leq t_2 \leq \lfloor (n_2 - k_2)/2 \rfloor$.
- The inner code C_1 is a 2^l -PSK code of length n_1 and dimension

$$k_1 = \sum_{i=1}^l k_{b,i}$$

where $k_1 = mb$.

- The outer code C_2 is interleaved to a depth of m .
- The encoding consists of two stages, the outer and inner encodings.
- The decoding consists of two stages, the inner and outer decodings.
- When the receiver fails to decode a received block, the block is erased and the receiver raises a **flag**.
- In the event of an erasure, we could either request a re-transmission or accept the erroneous block with alarm.

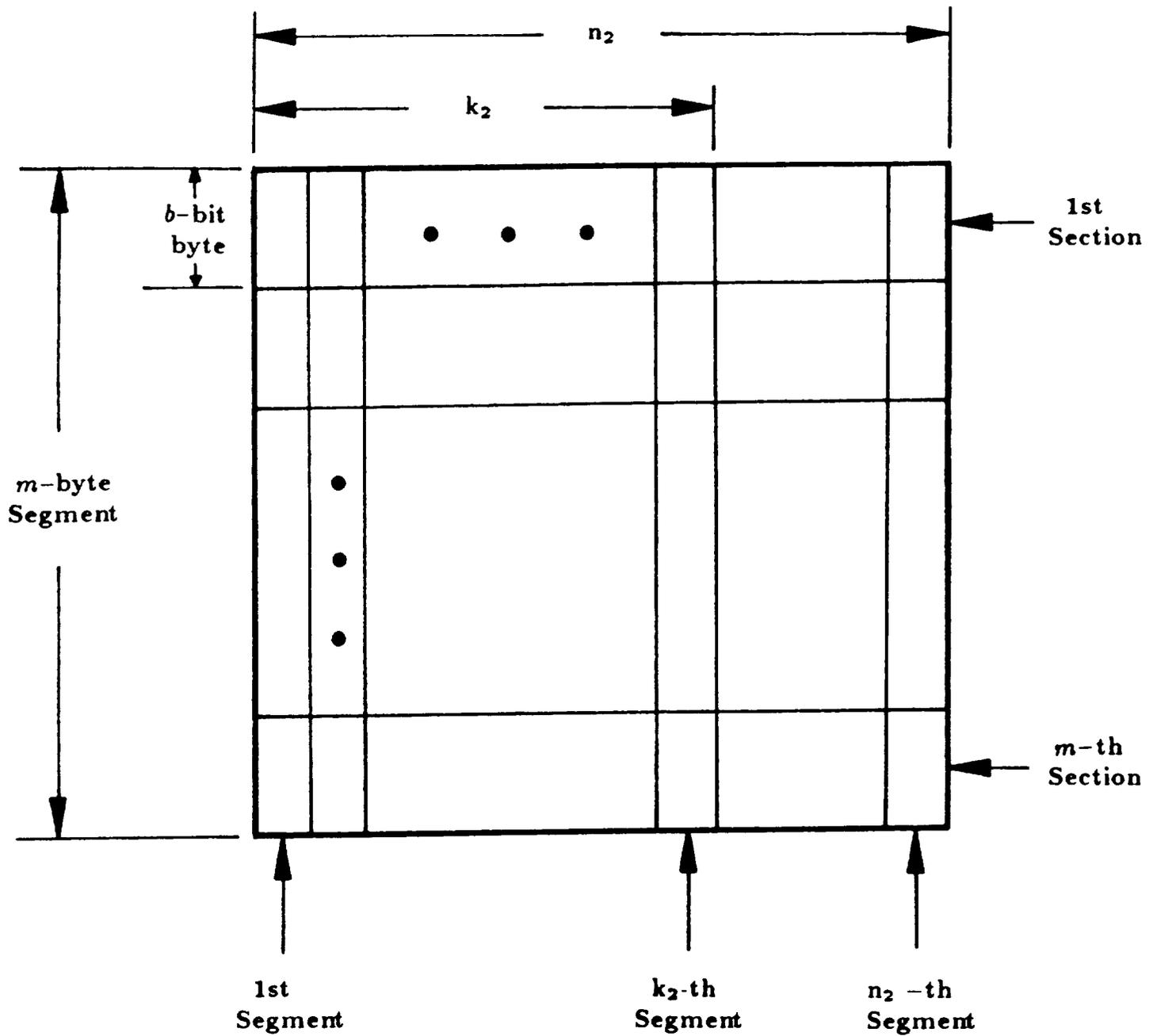


Figure 1 A Segment-Array

ERROR PERFORMANCE OF THE OVERALL SCHEME

- Let P_c , P_e , and P_{er} be the probabilities of a correct decoding, an erasure and an incorrect decoding for an entire received code block respectively.
- Lower bound on P_c and upper bounds on P_e , and P_{er} have been derived for an AWGN channel.
- Let \check{P}_c denote a lower bound on P_c .
- Then $1-\check{P}_c$ is an upper bound on the **total probability** of a decoding failure and a decoding error.
- Let \hat{P}_{er} denote an upper bound on P_{er} .
- The performance of the proposed concatenated coded modulation scheme is measured by the pair, \hat{P}_{er} and $1-\check{P}_c$.
- We can compute the coding gains of the proposed scheme over the uncoded QPSK modulation system either in terms of decoded **block-error rates** or in terms of decoded **bit-error rates**.

- For data file transfer, the block-error rates should be used as the measure of the error performance of the scheme.
- There are two types of bit-error rates, denoted $P_{b,1}$ and $P_{b,2}$.
- $P_{b,1}$ is computed based on the block error probability $P_{e,r}$ using the approximation,

$$P_{b,1} = (d_2 / 2n_2) \cdot P_{e,r}$$

- $P_{b,1}$ is a measure of bit-error performance of the proposed scheme when retransmission is allowed.
- $P_{b,2}$ is computed based on the total probability $1 - P_e$ of a decoding failure and a decoding error of a code block using the approximation,

$$P_{b,2} = (d_2 / 2n_2) \cdot (1 - P_e)$$

- $P_{b,2}$ is used as the measure of bit-error performance of the scheme when retransmission is not available or allowed.

TWO SPECIFIC CONCATENATED CODED MODULATION SCHEMES

SCHEME – I

- The outer code C_2 is the NASA standard (255,223) RS code over $GF(2^8)$ which has minimum distance 33. It is used to correct up to 16 symbol errors.
- The inner code C_1 is an 8-PSK code with $n_1 = 8$, $k_1 = 16$, $D[C_1] = 4$, $R[C_1] = 1$ and $\gamma[C_1] = 3$ dB (over uncoded QPSK).
- The outer code is interleaved to a depth of $m = 2$.
- The overall effective rate of the scheme is

$$R_{eff} = (k_2/n_2) \cdot R[C_1] = 0.875.$$

- The inner code has a 4-state trellis structure and can be decoded with a soft-decision Viterbi decoder.

ERROR PERFORMANCE

- With SNR = 9 dB/symbol (6.57 dB/infor. bit),

$$P_{e,r} \leq 6.28 \times 10^{-26}$$

$$1 - P_e \leq 4.95 \times 10^{-16}$$

- With SNR = 10 dB/symbol (5.57 dB/infor. bit),

$$P_{e,r} \leq 6.80 \times 10^{-41}$$

and $1 - P_e$ is very small.

CODING GAIN OVER QPSK

- At the block-error rate $= 10^{-7}$,

$$G_B = 8 \text{ dB/symbol.}$$

- At the block-error rate $= 10^{-10}$,

$$G_B = 9 \text{ dB/symbol.}$$

- At the bit-error rate $P_{b,1} = 10^{-12}$,

$$G_{b,1} = 9.80 \text{ dB/symbol (9.20 dB/infor. bit).}$$

The required SNR to achieve $P_{b,1} = 10^{-12}$ is 7.10 dB/symbol (4.60 dB/infor. bit).

- At the bit-error rate $P_{b,2} = 10^{-6}$,

$$G_{b,2} = 5.52 \text{ dB/symbol (4.94 dB/infor. bit)}.$$

The required SNR to achieve $P_{b,2} = 10^{-6}$ is 8.04 dB/symbol (5.61 dB/infor. bit).

- At the bit-error rate $P_{b,2} = 10^{-10}$,

$$G_{b,2} = 7.60 \text{ dB/symbol (7.02 dB/infor. bit)}.$$

The required SNR to achieve $P_{b,2} = 10^{-10}$ is 8.50 dB/symbol (6.07 dB/infor. bit).

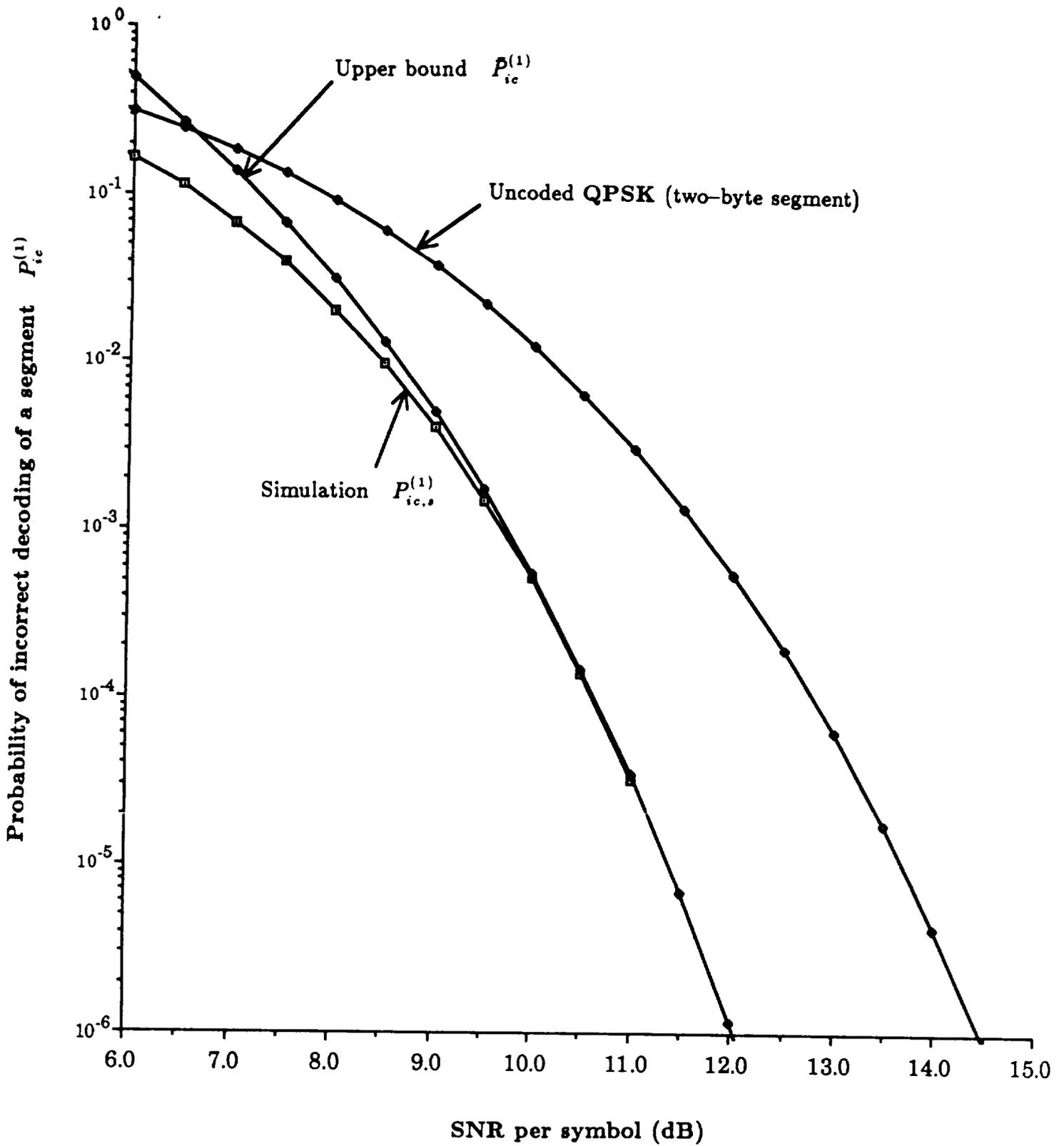


Figure 2 Error performance of the 4-state 8-PSK block code (the 4-th code in Table 1)

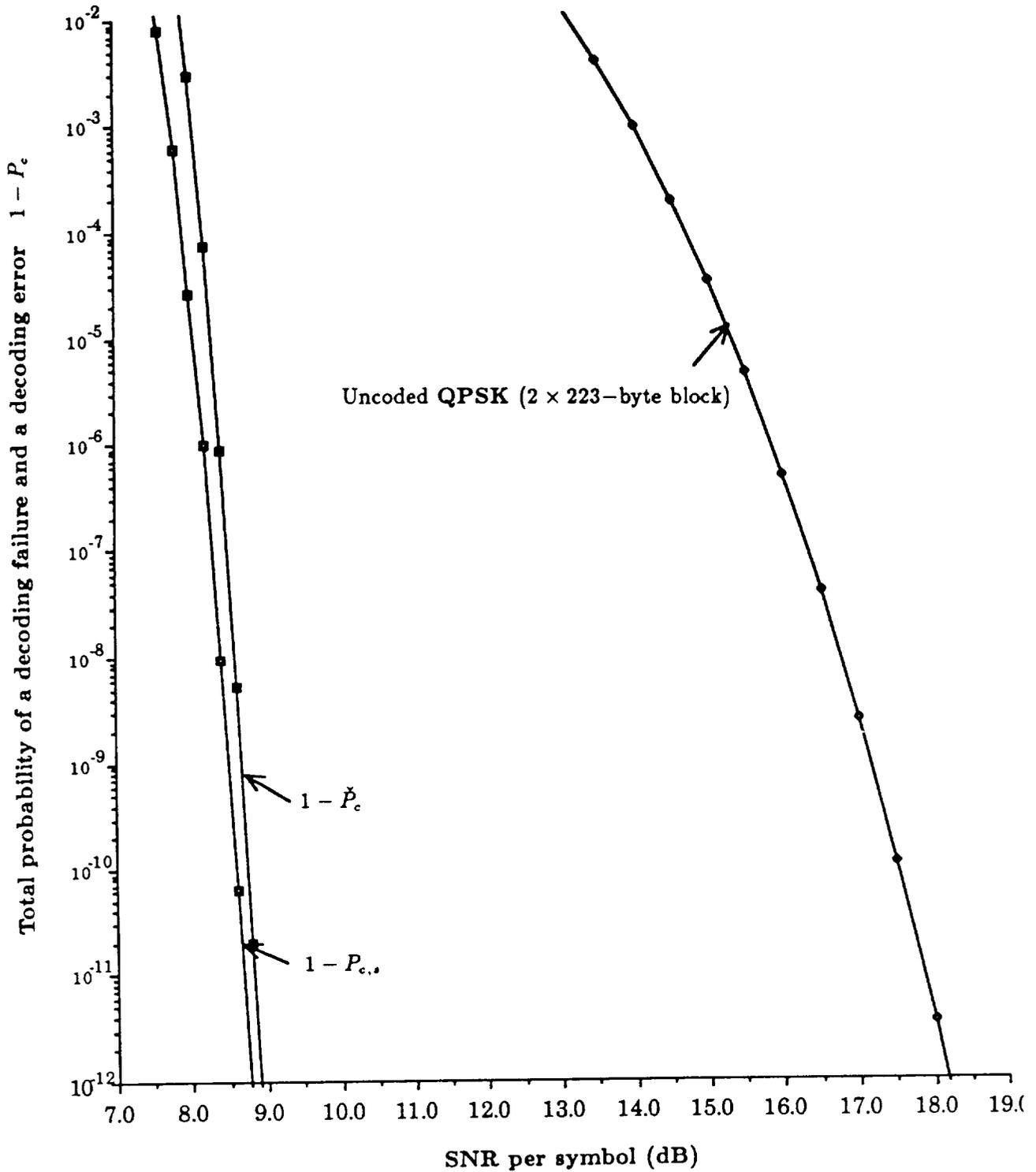


Figure 3 The total probability of a decoding failure and a decoding error for the concatenated coded modulation scheme with the (255,223) RS outer code and the 4-state 8-PSK block inner code (the 4-th code in Table 1)

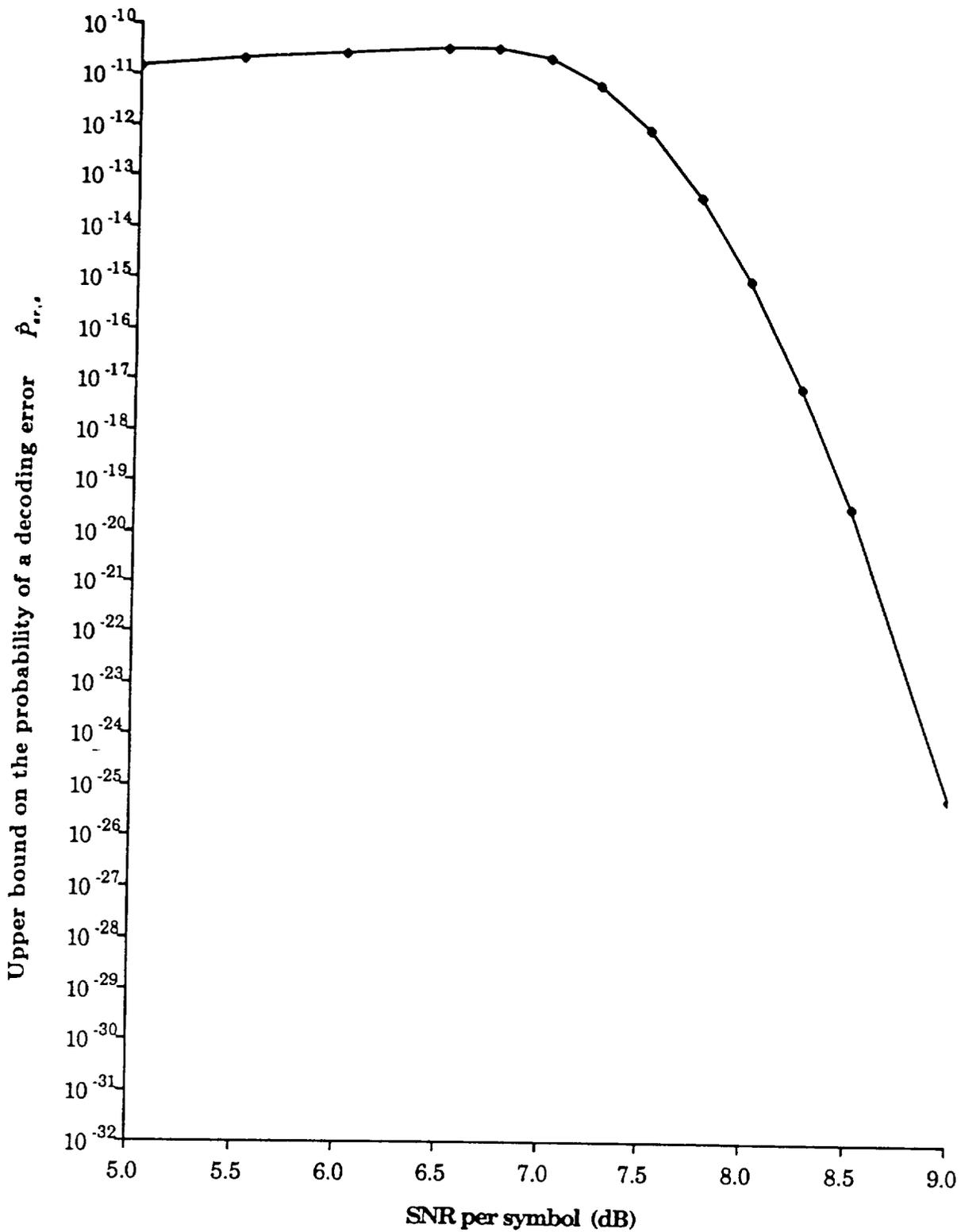


Figure 4 The probability of a decoding error for the concatenated coded modulation scheme with the (255,223) RS outer code and the 4-state 8-PSK block inner code (the 4-th code in Table 1)

SCHEME – II

- The outer code is the NASA standard (255,223) RS code over $GF(2^8)$.
- The inner code C_1 is an 8-PSK code of length 16 and dimension $k_1 = 36$ with $D[C_1] = 4$, $R[C_1] = 9/8$ and $\gamma[C_1] = 3.52$ dB (over uncoded QPSK).
- The outer code is interleaved to a depth of $m = 9$.
- The overall effective rate of the scheme is

$$R_{eff} = (223/255) \cdot (9/8) = 0.9838.$$

- The inner code has a 16-state trellis diagram which consists of two identical parallel 8-state trellis sub-diagrams with no cross connection between them.
- The probability of an incorrect decoding for this code is

$$\begin{aligned}
P_{ic}^{(1)} \leq & 248 \operatorname{erfc}(\sqrt{\rho}) + 1920 \operatorname{erfc}(\sqrt{2(2-\sqrt{2})\rho}) + 30720 \operatorname{erfc}\left(\frac{\sqrt{2(9-4\sqrt{2})\rho}}{2}\right) \\
& + 15360 \operatorname{erfc}\left(\frac{\sqrt{2(8-3\sqrt{2})\rho}}{2}\right) + 16384 \operatorname{erfc}(2\sqrt{(2-\sqrt{2})\rho}) \\
& + 245760 \operatorname{erfc}\left(\frac{\sqrt{3(8-3\sqrt{2})\rho}}{2}\right) + 262144 \operatorname{erfc}\left(\frac{\sqrt{2(16-7\sqrt{2})\rho}}{2}\right) .
\end{aligned}$$

- At the 10^{-6} decoded block error rate, this inner code provides a 2.20 dB real coding gain over the uncoded QPSK.

ERROR PERFORMANCE

- With SNR = 10 dB/symbol (or 7.06 dB/infor. bit),

$$P_e \leq 6.91 \times 10^{-41}$$

$$1 - P_e \leq 2.08 \times 10^{-12}$$

CODING GAIN

- At the block-error rate $= 10^{-7}$,

$$G_B = 7 \text{ dB/symbol.}$$

- At the block-error rate $= 10^{-10}$,

$$G_B = 8 \text{ dB/symbol.}$$

- At the bit-error rate $P_{b_1} = 10^{-31}$,

$$G_{b_1} = 15 \text{ dB/symbol.}$$

- At the bit-error rate $P_{b_2} = 10^{-10}$,

$$G_{b_2} = 6.26 \text{ dB/symbol (6.19 dB/infor. bit).}$$

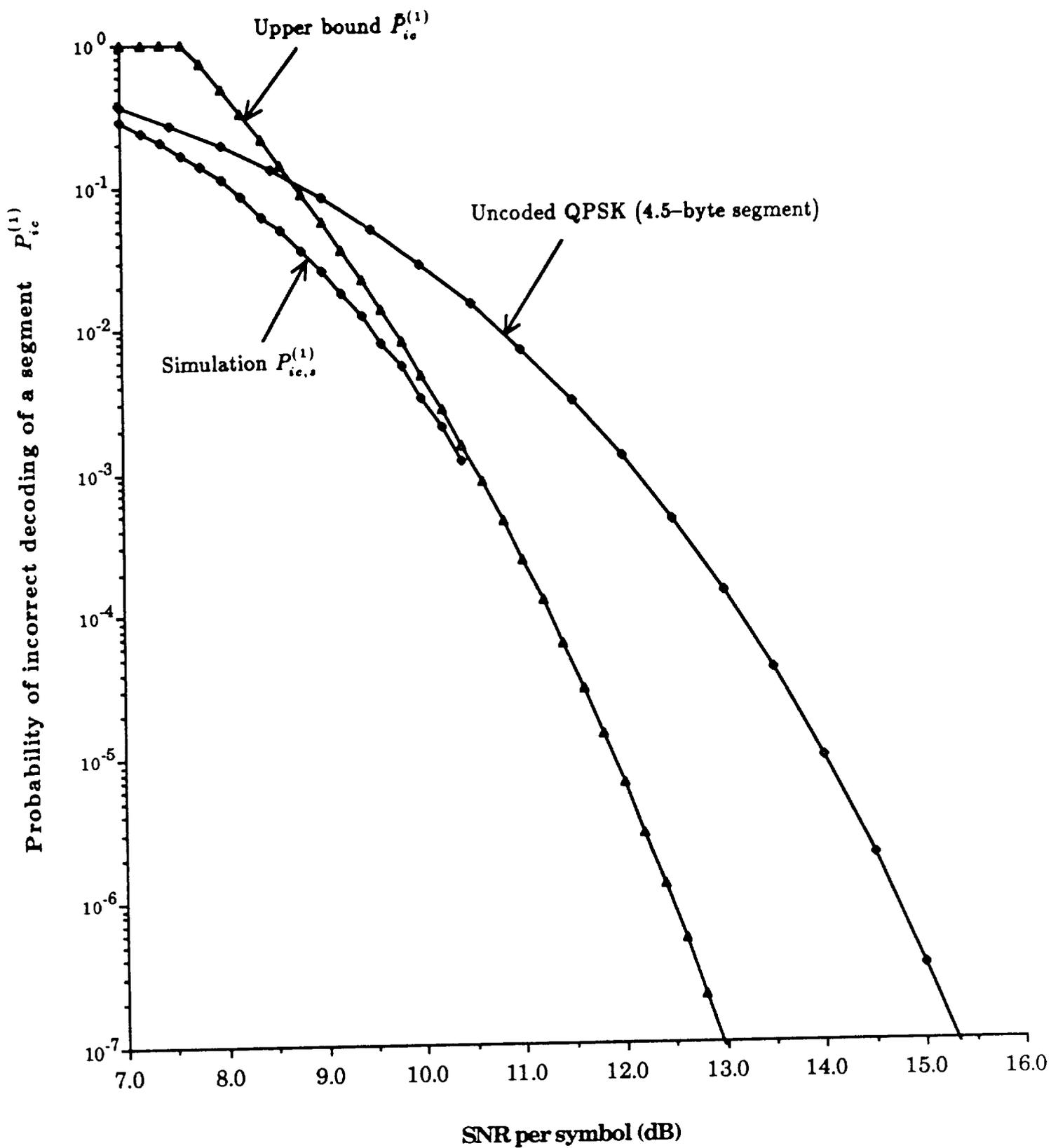


Figure 5 Error performance of the 16-state 8-PSK block inner code (the 5-th code in Table 1)

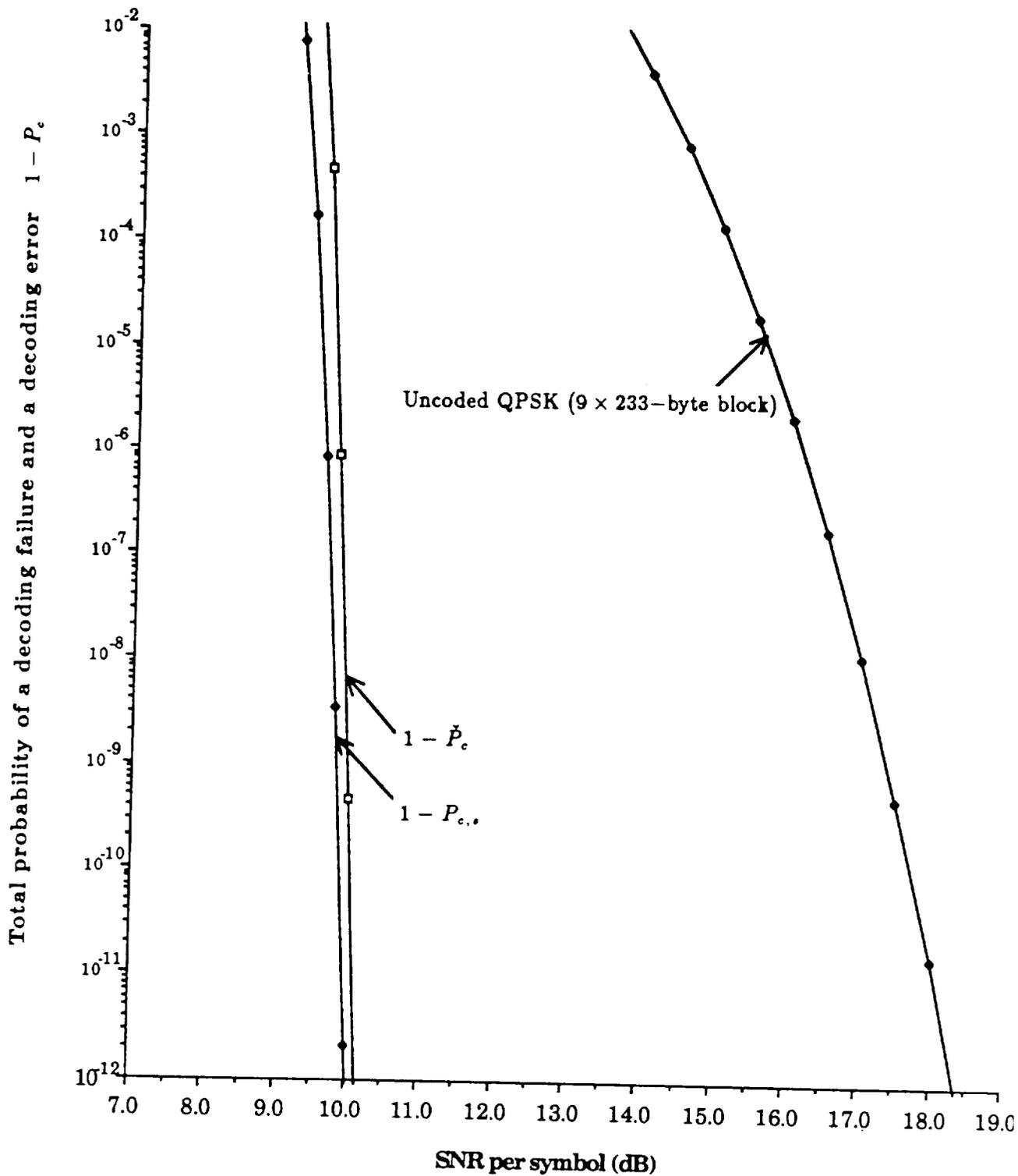


Figure 6 The total probability of a decoding failure and a decoding error for the concatenated coded modulation scheme with the (255,223) RS outer code and the 16-state 8-PSK block inner code (the 5-th code in Table 1)

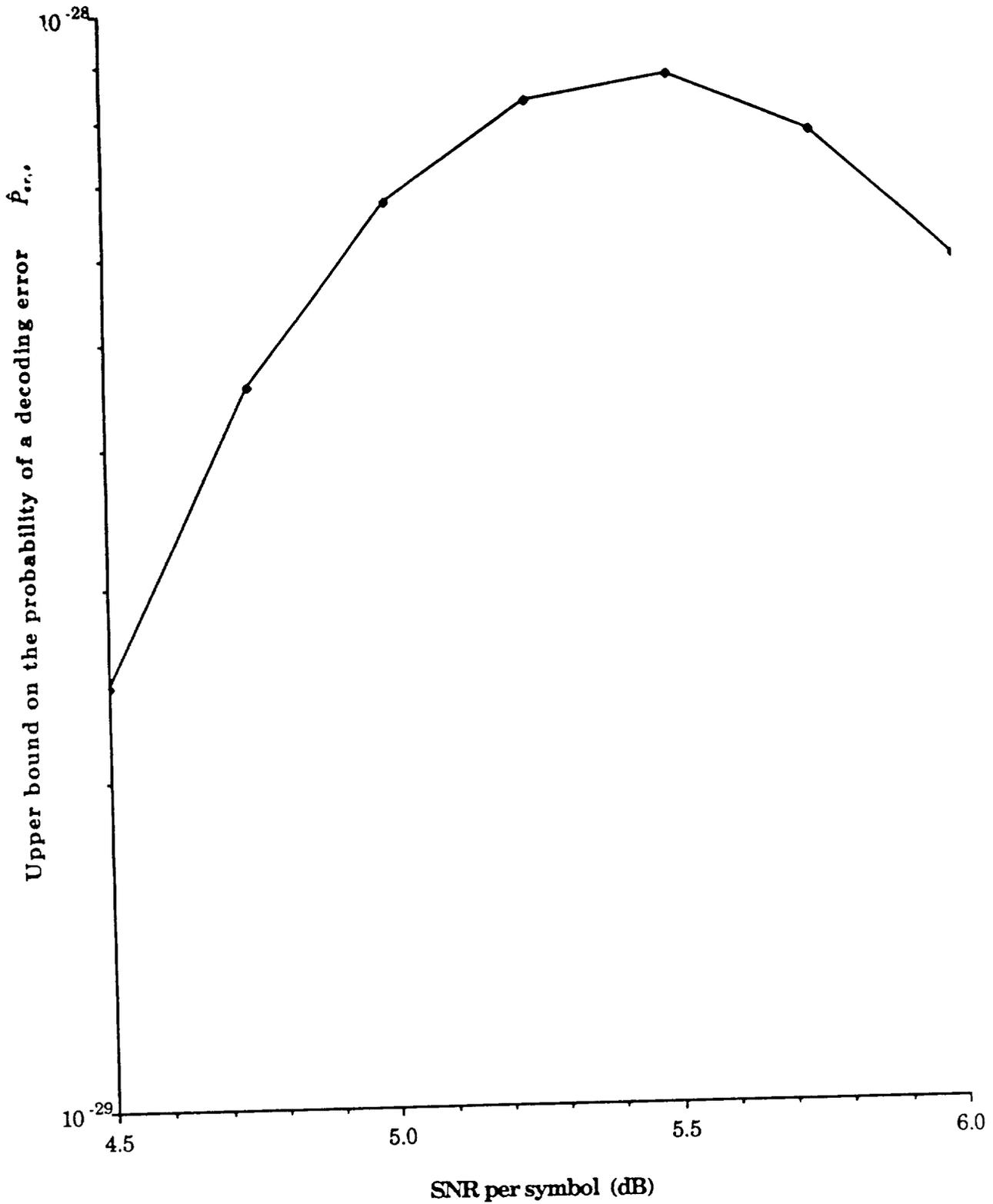


Figure 7 The probability of a decoding error for the concatenated coded modulation scheme with the (255,223) RS outer code and the 16-state 8-PSK block inner code (the 5-th code in Table 1)

REMARK

- The inner code decoder can be implemented to perform both decoding and **erasure** operations.
- In this case, the outer code decoder is devised to correct both symbol errors and erasures.

SESSION VI

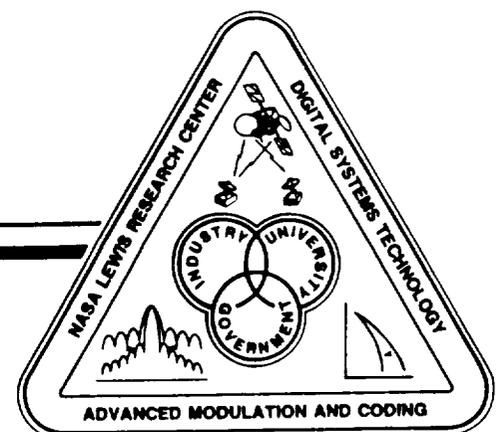
**TECHNOLOGY NEEDS/OPPORTUNITIES FOR
FUTURE MISSIONS
CHAIR: J.W. BAGWELL**

**FUTURE COMMUNICATIONS SATELLITE APPLICATIONS
J.W. BAGWELL
NASA LEWIS RESEARCH CENTER**

**ADVANCED TRACKING AND DATA RELAY SATELLITE SYSTEM
D. STERN
NASA HEADQUARTERS**

**INTERNATIONAL COMMUNICATIONS SATELLITE SYSTEMS
W.W. WU
INTELSAT**

**MODULATION AND CODING USED BY A
MAJOR SATELLITE COMMUNICATIONS COMPANY
K.H. RENSHAW
HUGHES COMMUNICATIONS, INCORPORATED**



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FUTURE COMMUNICATIONS SATELLITE APPLICATIONS

James W. Bagwell
NASA Lewis Research Center
Cleveland, Ohio 44135

SWITCHED POINT-TO-POINT NARROWBAND COMMUNICATIONS

CHARACTERISTICS:

SMALL/LOW COST TERMINALS

SINGLE HOP COMMUNICATIONS

VOICE COMPATIBLE

FULL MESH NETWORKING

ISDN COMPATIBLE

POSSIBLE LIMITED USE OF FULL MOTION VIDEO

TARGET APPLICATIONS:

VOICE/DATA NETWORKS BETWEEN PLANTS AND OFFICES IN A CORPORATION

DATABASE NETWORKING FOR COMMERCIAL AND SCIENCE USERS

CELLULAR RADIO INTERNODAL VOICE/DATA NETWORKING

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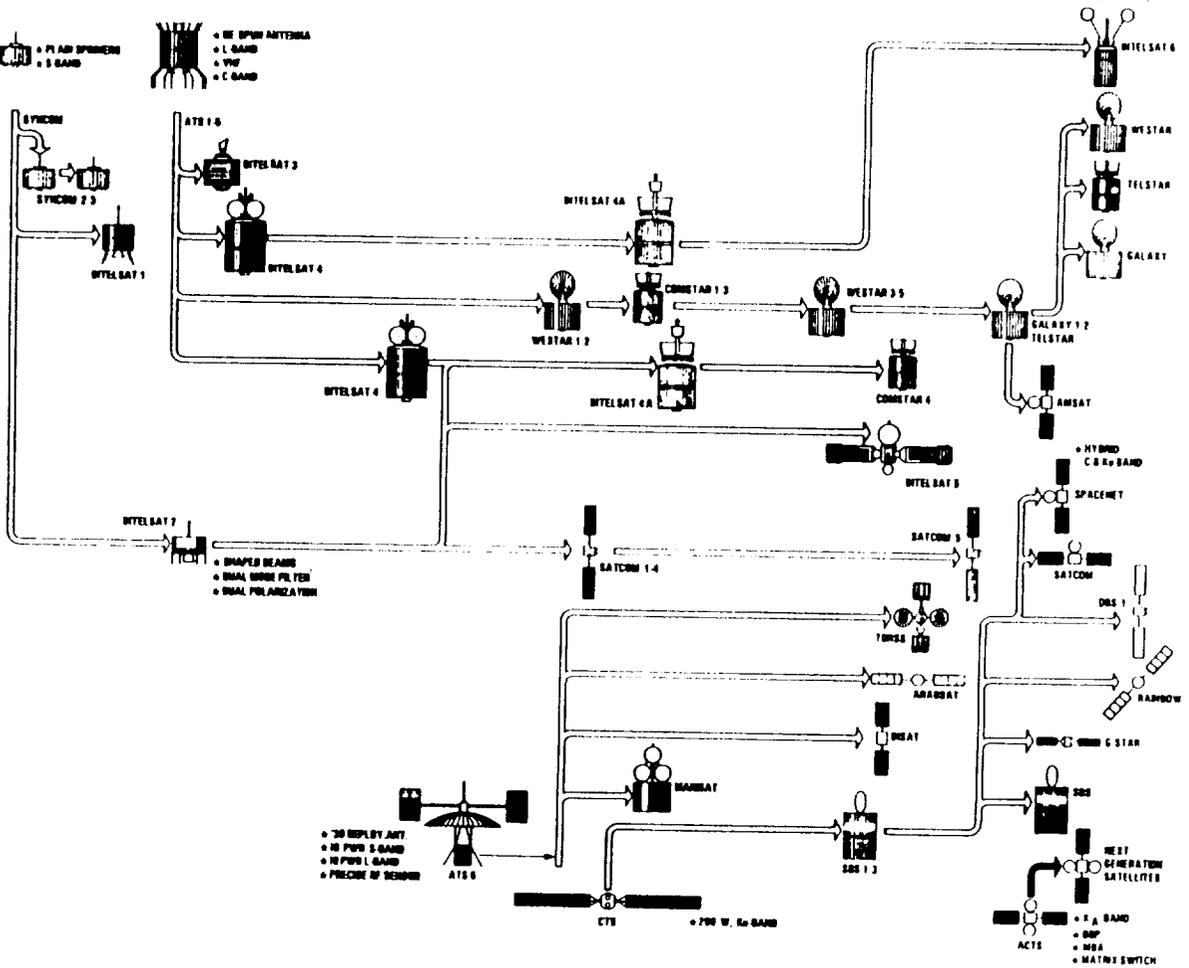
COMMUNICATIONS SATELLITES GENESIS

LAUNCH DATES 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87

NASA
R&D
SPINNERS

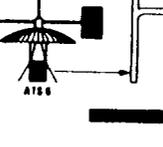
- PLAN SPINNERS
- S BAND

- 16 SPIN ANTENNA
- L BAND
- VHF
- C BAND



NASA
R&D
3-AXIS

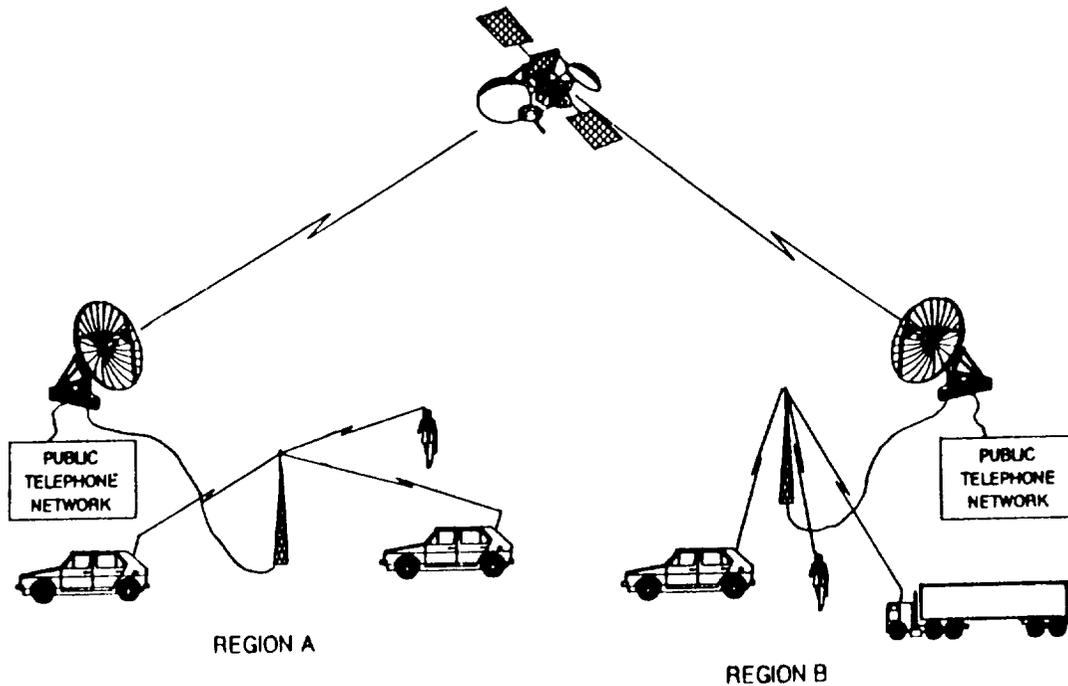
- 30 DEPLOY ANT
- 16 PWR S BAND
- 16 PWR L BAND
- PRECISE RF SENSOR



- 700 W. S-BAND

- NEXT GENERATION SATELLITES
- S BAND
- SSP
- HSA
- MATRIX SWITCH

CELLULAR RADIO INTERNODAL NETWORK



COMMUNICATION SATELLITES

CHARACTERISTICS COMPARISON

CURRENT

- 0 CONUS COVERAGE ANTENNAS
- 0 BENT PIPE TRANSPONDERS
- 0 C AND Ku BAND
- 0 LIMITED BANDWIDTH
- 0 LARGE EARTH TERMINALS
- 0 STAR NETWORKS

FUTURE

- 0 SPOT BEAM & SCANNING ANTENNAS
- 0 REGENERATIVE PROCESSING TRANSPONDERS
- 0 Ka BAND
- 0 UNCONGESTED
- 0 SMALL EARTH TERMINALS
- 0 MESH NETWORKS

BUSINESS/RESIDENTIAL VIDEO PHONE SERVICE

CHARACTERISTICS:

LOW COST TERMINALS LOCATED AT CABLE HEAD ENDS
TRAFFIC FROM TERMINALS SWITCHED/ROUTED THROUGH SATELLITE
SINGLE HOP TO ANY OTHER TERMINAL IN CONUS
VIDEO CAMERA REQUIRED AT EACH RESIDENCE
USES TELEPHONE CIRCUITS FOR AUDIO

ADVANTAGES:

USES EXISTING HOME TELEVISION SET AND TELEPHONES
USES EXISTING CATV DISTRIBUTION SYSTEMS
PROVIDES VALUE ADDED SERVICE FOR CABLE TV SUPPLIERS
SATELLITE & TERMINAL COSTS SPREAD OVER LARGE CUSTOMER BASE

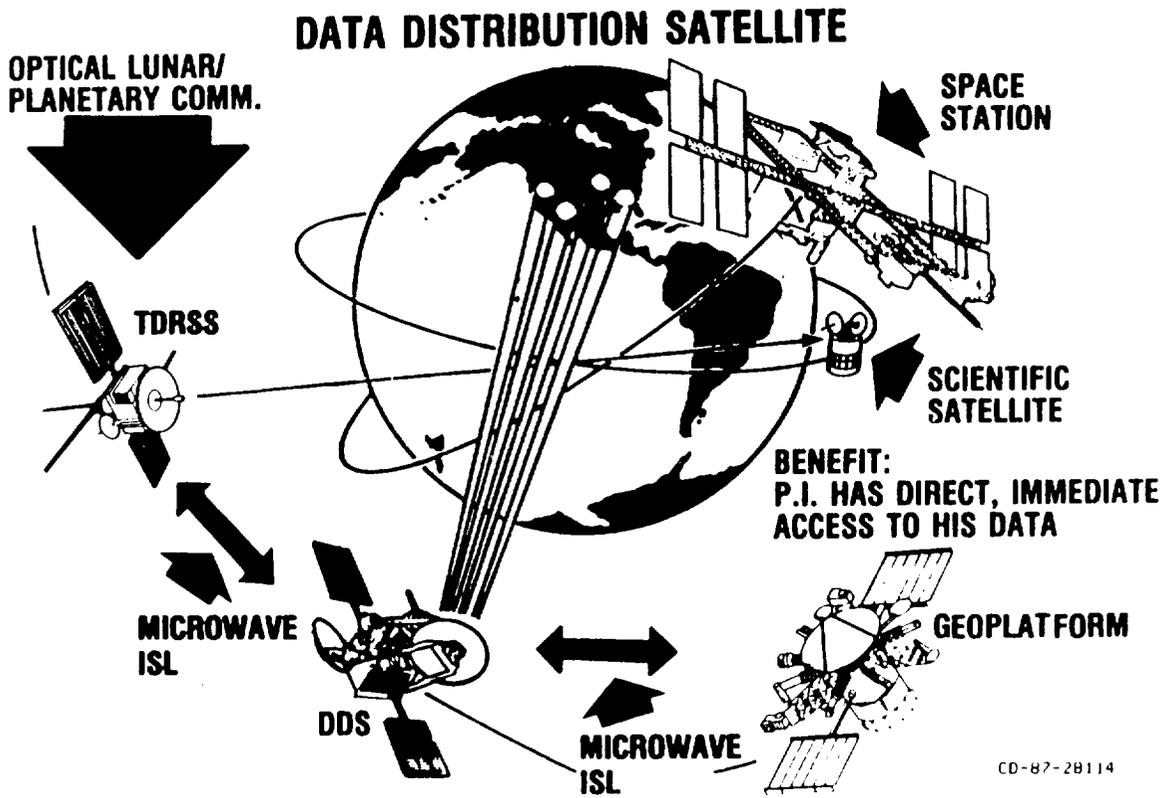
DISADVANTAGES:

REQUIRES REVERSE CHANNEL REPEATERS
MAY EVENTUALLY BE DISPLACED BY OPTICAL FIBER

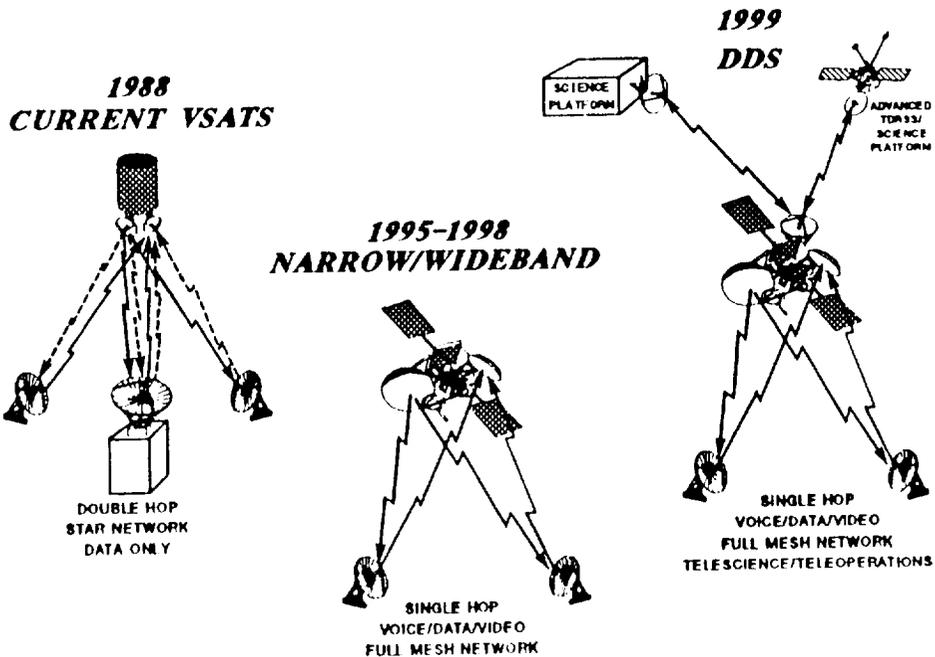
COMMUNICATION SYSTEMS CHARACTERISTICS

- 27.5-30.0 GHz UPLINK 17.7-20.2 GHz DOWNLINK
- TDMA WITH DAMA
- MW MATRIX SWITCH MODE
220 MSPS UPLINK 220 MSPS DOWNLINK
(NOTE-EXPERIMENTS POSSIBLE AT ANY BIT RATE AND
MODULATION IN EITHER TDMA OR FDMA FORMAT)
- BASEBAND PROCESSOR MODE
FOUR-27.5 MSPS TWO-110 MSPS DOWNLINKS
TWO-110 MSPS UPLINKS
- SSK MODULATION IN BASEBAND PROCESSOR MODE
- $\leq 10^{-6}$ BER
- FADE MARGIN:

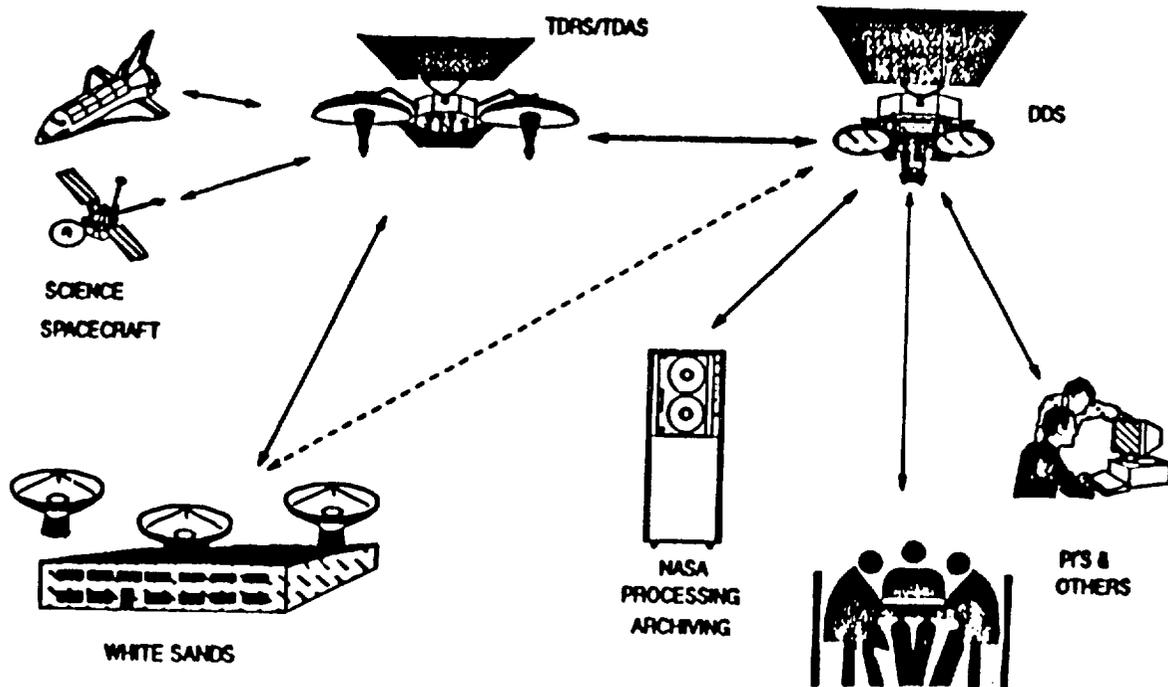
	<u>MWMS MODE</u>	<u>BBP MODE</u>
UPLINK	18 dB	15 dB
DOWNLINK	8 dB	6 dB
- FADE SENSING 20 AND 30 GHz DOWNLINK BEACONS
- 20 GHz TWTA
POWER 43 W
- 30 GHz FET LOW NOISE AMPLIFIER 5 dB MAX NOISE FIGURE



EVOLUTION OF OPERATIONAL SYSTEMS



POSSIBLE DDS SYSTEM



CELLULAR RADIO INTERNODAL SERVICE

CHARACTERISTICS:

LOW COST TERMINAL LOCATED AT CELL ANTENNA SITE TRAFFIC FROM TERMINALS SWITCHED/ROUTED THROUGH SATELLITE SINGLE HOP TO ANY OTHER TERMINAL IN CONUS

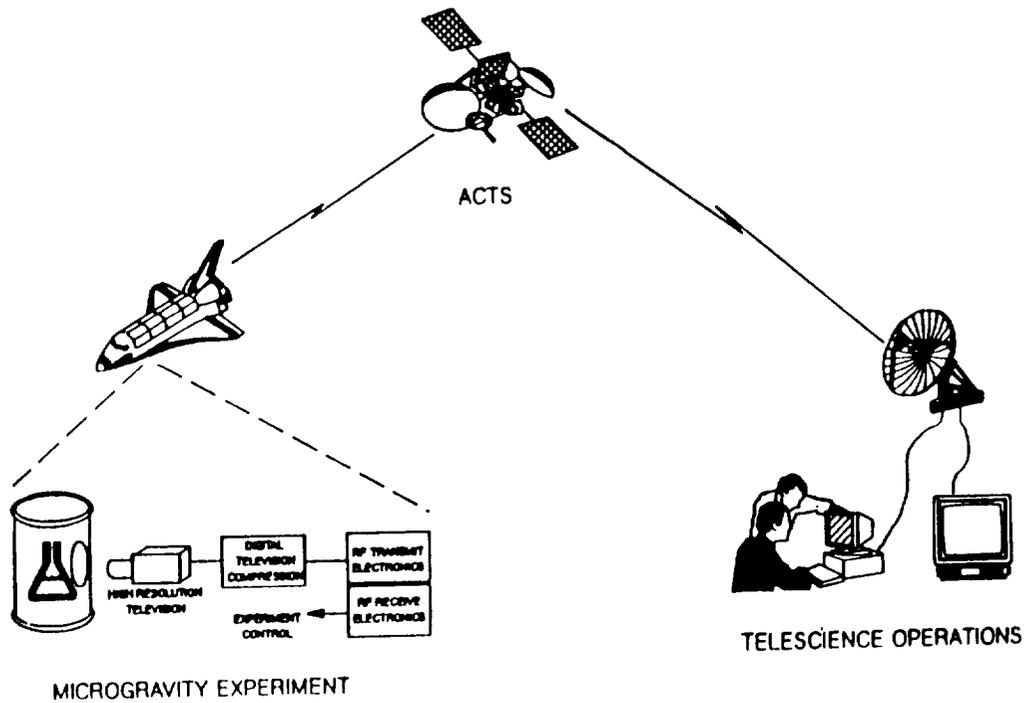
ADVANTAGES:

USES IN-PLACE MOBILE SERVICE
TAKES ADVANTAGE OF ESTABLISHED CUSTOMER BASE/MARKET
AVAILABILITY OF ADEQUATE BANDWIDTH/NO FREQUENCY ALLOCATION PROBLEM
COST EFFECTIVE MOBILE RADIOS ALREADY AVAILABLE
PROVIDES BYPASS OF TERRESTRIAL TOLL NETWORK
DIRECT VOICE QUALITY LINK BETWEEN MOBILE USERS
INTERCONNECTION OF CELLS IN NEWLY LICENSED RURAL AREA

DISADVANTAGES:

COMPETES WITH TERRESTRIAL TOLL SERVICES

TELESCIENCE EXPERIMENT



SWITCHED POINT-TO-POINT WIDEBAND COMMUNICATIONS

CHARACTERISTICS:

SMALL/LOW COST TERMINALS

SINGLE HOP COMMUNICATIONS

VOICE/VIDEO COMPATIBLE

FULL MESH NETWORKING

ISDN COMPATIBLE

EXTENSIVE AVAILABILITY OF REDUCED BANDWIDTH CHANNELS FOR VIDEOPHONES

SIGNIFICANT NUMBER OF CHANNELS AVAILABLE FOR FULL MOTION VIDEO

TARGET APPLICATIONS:

VOICE/VIDEO/DATA NETWORKS BETWEEN CORPORATE PLANTS AND OFFICES

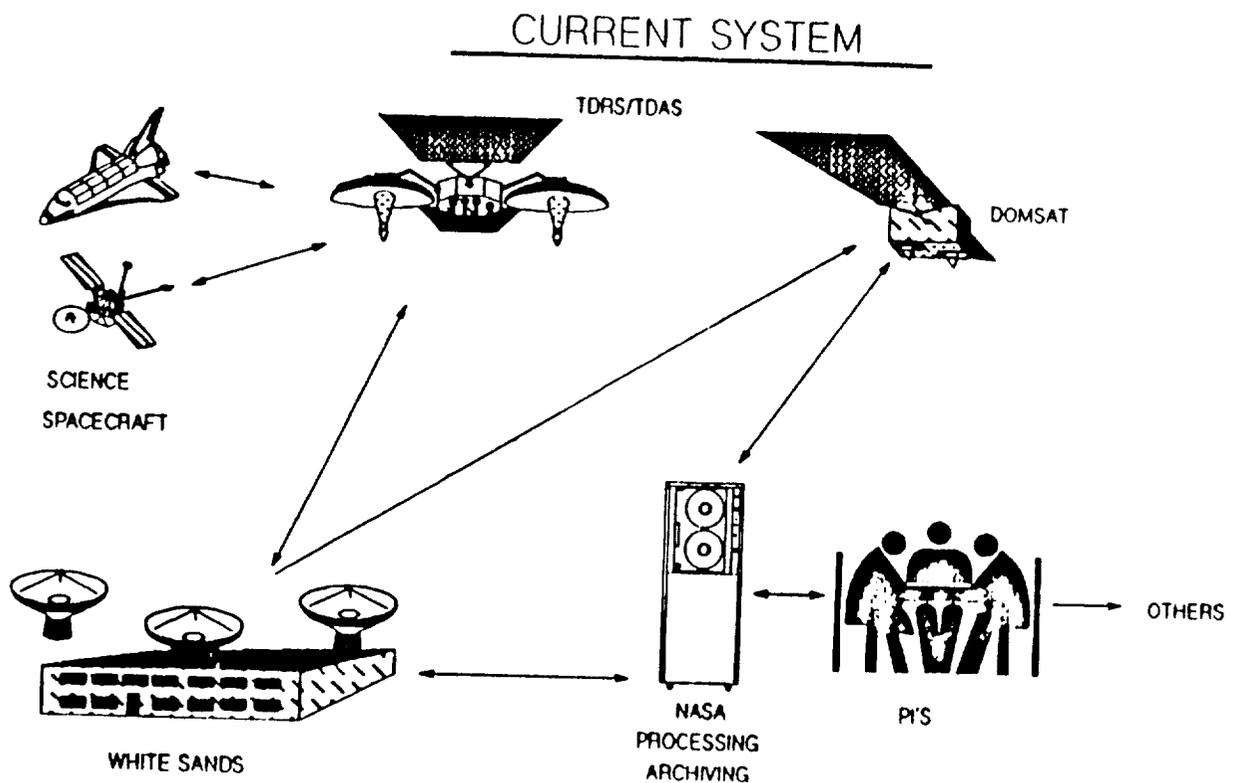
IMAGE DATA NETWORKING FOR COMMERCIAL AND SCIENCE USERS

CABLE TV INTERNETTING FOR DIRECT TO/FROM HOME VIDEOPHONE SERVICE

COMMUNICATION SATELLITES

INTRODUCTION

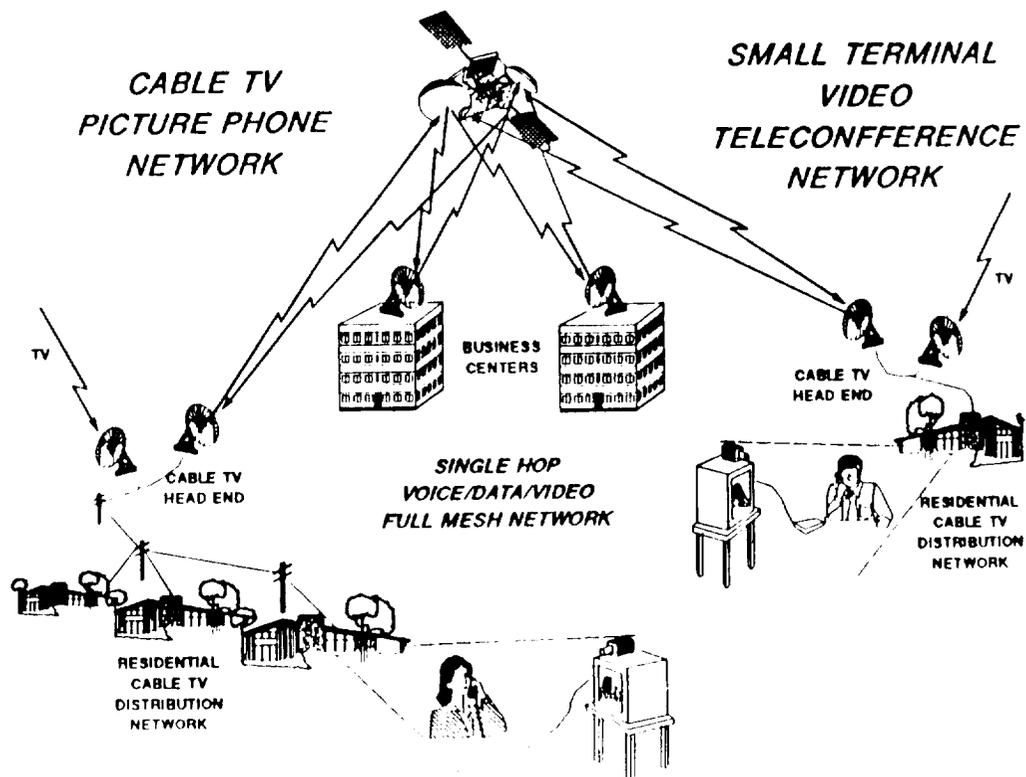
- o NASA INTRODUCED THE FIRST AND ONLY (AS OF NOW) PROFITABLE USE OF SPACE WHEN IT LAUNCHED THE FIRST COMMUNICATION SATELLITE IN 1963
- o SINCE THEN, THROUGH BOTH NASA AND INDUSTRY INNOVATION THE COMMUNICATION SATELLITE INDUSTRY HAS GROWN TO PROVIDE \$3.5 B/YR. IN REVENUES AND TO BE ONE OF MAJOR GLOBAL INFLUENCE
- o THE INFORMATION AGE IS MAKING NEW DEMANDS
- o TERRESTRIAL FIBER OPTICS IS BECOMING A COMPETITOR
- o NEW COMMUNICATION SATELLITE TECHNOLOGIES PROMISE TO MEET INCREASING DEMANDS AND ENABLE NEW SERVICES



COMMUNICATION SATELLITES

CONCLUSION

- 0 COMMUNICATION SATELLITES PLAYED KEY ROLE IN ENABLING INFORMATION ERA AND CREATING ONE GLOBAL COMMUNITY
- 0 NEW TECHNOLOGIES SUCH AS TERRESTRIAL FIBER OPTICS WILL COMPETE AND FORCE MARKET SHIFTS
- 0 NEW EMERGING INFORMATION AND COMMUNICATION NEEDS WILL INCREASE DEMAND
- 0 NEW MODULATION AND CODING TECHNOLOGIES WILL BE IN INCREASING DEMAND TO ENABLE AND ENHANCE THESE NEW SERVICES



COMMUNICATION SATELLITES

ADVANTAGES

- 0 EASE IN SETTING UP LINK
- 0 BROADCAST MODE
- 0 TRANSPORTABLE/MOBILE
- 0 DISTANCE INSENSITIVE

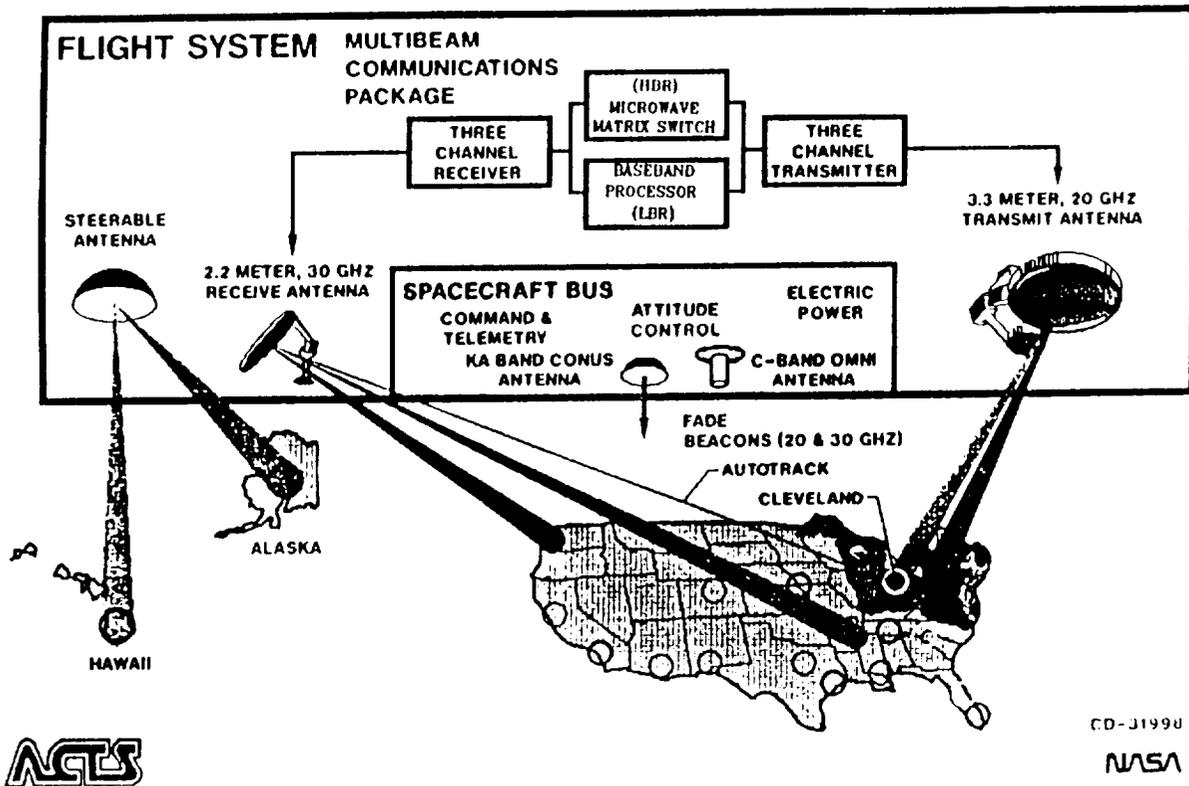
LIMITATIONS

- 0 BANDWIDTH
- 0 DELAY
- 0 PATH LENGTH

BENEFITS TO NASA

- 0 OFFERS SOLUTION TO NASA'S BURGEONING NEED FOR ADVANCED HIGHER CAPACITY TELECOMMUNICATIONS SYSTEMS TO SUPPORT FUTURE SHUTTLE, SPACE STATION, AND SCIENCE NEEDS.
- 0 WILL INFUSE STATE-OF-THE-ART SATELLITE TECHNOLOGY INTO NASA'S CONTINUED MODERNIZATION OF ITS INFORMATION SYSTEMS NETWORK.
- 0 GREATLY IMPROVED ACCESS BY PI'S AND OTHERS TO SPACE SCIENCE DATA, BOTH REAL-TIME AND ARCHIVED.
- 0 WILL ENABLE "SPACE" TO BECOME A PART OF EXPERIMENTER AND EDUCATOR'S LABORATORY OR CLASSROOM THROUGH TELEPRESENCE (MONITORING & CONTROL OF EXPERIMENTS).

Functional Overview of the ACTS Flight Segment



COMMUNICATION SATELLITES

BENEFITS OF NEW MODULATION AND CODING TECHNOLOGIES

- 0 CONSERVE BANDWIDTH
- 0 CONSERVE POWER
- 0 IMPROVE LINK AVAILABILITY
- 0 IMPROVE INFORMATION INTEGRITY
- 0 IMPROVE INFORMATION SECURITY

COMMUNICATION SATELLITES

CURRENT APPLICATIONS

- 0 TELEVISION PROGRAM DISTRIBUTION
- 0 LONG HAUL TELEPHONE
- 0 DATA TRANSMISSION
- 0 BUSINESS COMMUNICATIONS (STAR NETWORK)

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ADVANCED TRACKING AND DATA RELAY SATELLITE SYSTEM

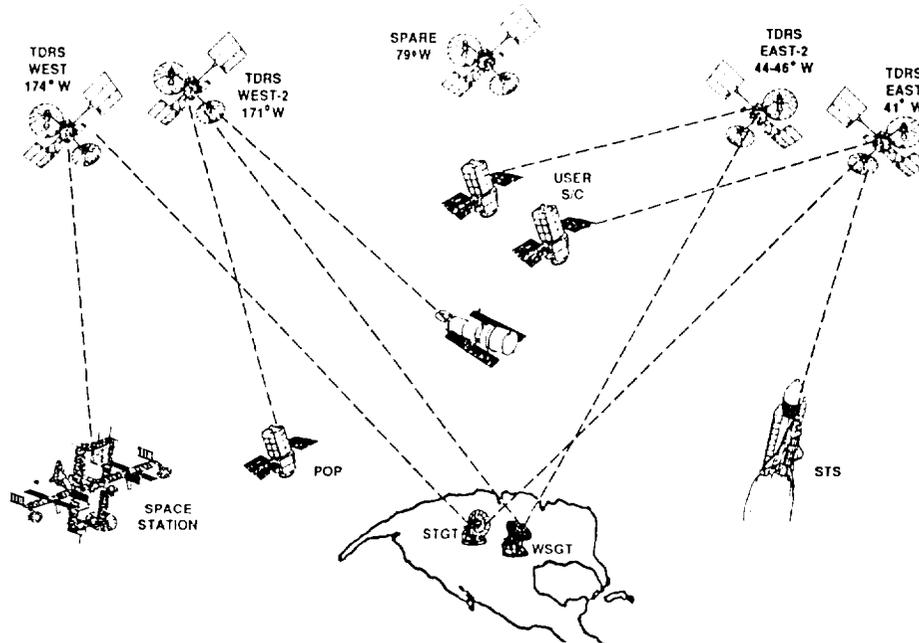
Daniel Stern
NASA Headquarters
Washington, D.C. 20546

ADVANCED TDRSS

PURPOSE:

- Provide NASA needs for satellite tracking and communications through the year 2012
- Maintain and augment the current TDRS System when available satellite resources are expended in the latter part of the next decade
- Provide the necessary ground upgrade to support the augmented services
- Introduce new technology to reduce system life-cycle cost.

ATDRSS Configuration



TDRS LAUNCH SCHEDULE

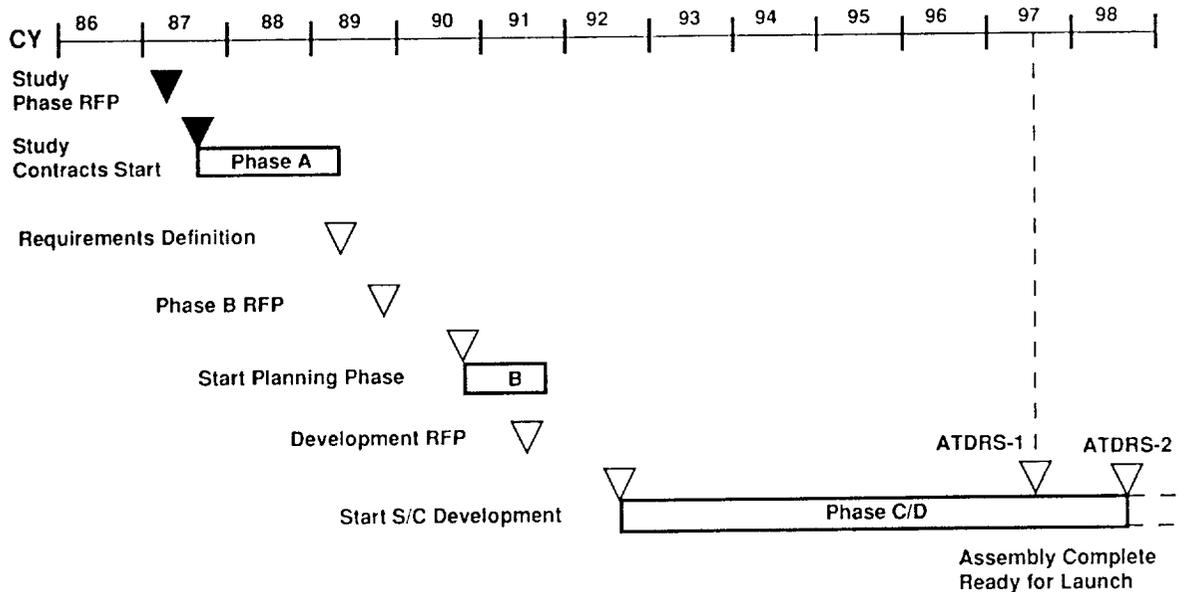
TDRS 1 - Launched 4/83; Degraded Capability
TDRS 2 - Lost in Challenger accident 1/86
TDRS 3 - Launched 9/88
TDRS 4 - Launched 3/89; replaced F-1

TDRS 5 - In orbit spare in 1990
TDRS 6 - Ground spare or fourth satellite in constellation
TDRS 7 - Replacement spacecraft; available 1992
TDRS 8 - Optional spacecraft; not available before 1994
ATDRS - Advanced TDRS; not available before July 1997

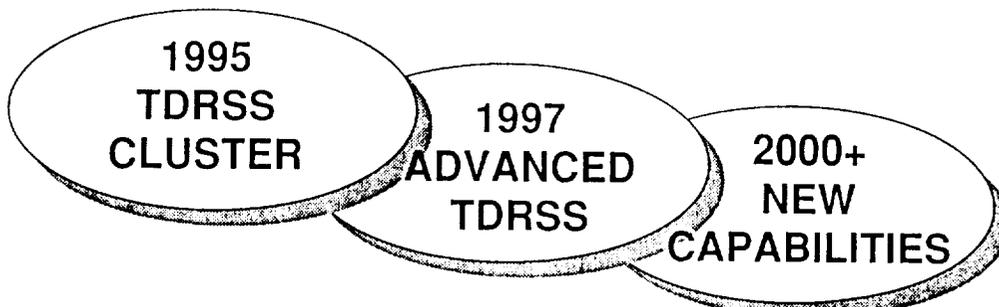
ADVANCED TDRSS STATUS

- Completed 18-month Conceptual Design Studies (Phase A) in March; Ford, GE, Hughes, Lockheed, TRW
- Phase B RFP to be released in August 1989 for a competitive award to multiple contractors
- Delivery of the first ATDRS is planned for July, 1997

ATDRSS PROGRAM SCHEDULE



TDRSS EVOLUTION



- Capability Increase to 8 SA's with 4th Spacecraft
- 8 SA's
- Enhanced S-Band
- Ka-User SGL
- Satellite Expansion Capability
- Navigation Beacon (study)
- 650 MBPS Return
- Geo. Coverage
- Increased Spacecraft autonomy
- Demand Access (study)
- Cross Links
- Direct Data Distribution
- Laser Links
- Interoperability with Foreign DSR's

POTENTIAL SERVICES UNDER EVALUATION

	<u>Status</u>
• Cost vs. benefit of closing the zone of exclusion	Defer
• Increased single access capacity (>300 Mb/sec)	✓
• Direct downlink to some locations or users	Defer
• Demand Access on MA channels	Study
• Interoperability with other data relay satellite systems	Defer
• Increased satellite reliability and redundancy	✓
• GEO user coverage	✓
• Command/Navigation Broadcast (Beacon)	Study
• Pre-Operational Demonstration (Satellite Expansion)	✓

TDRSS / ATDRSS BASELINE SERVICE COMPARISON

Single Access	Max. Rate (MBPS)	No. of Channels	
		1996 TDRSS Cluster	2003 Advanced TDRSS
S-Band	FWD.....0.3	8	4* + Spare
	RTN.....6		
Ku-Band	FWD.....25	8	4* + Spare
	RTN.....300		
Ka-Band	FWD.....50	8	4* + Spare
	RTN.....650		
Total No. of Independent Pointable Antennas		8	8 + 2 Spare

	TDRSS	ATDRSS
Multiple Access	FWD.....4 @ 10 KBPS RTN.....20 @ 50 KBPS	8 @ 10 KBPS (+3 dBW) 12 @ 3 MBPS**

	TDRSS	ATDRSS
Tracking Accuracy	150 M, 3 σ	Study improvement to 50M, 3 σ

* Minimum- possibly larger ** MA Gain equal to TDRS Single Access - S-Band

QPSK

- Expansion to Ka-Band obviates need for highly bandwidth-efficient modulation techniques
- Minimizes User and Spacecraft impact

ATDRSS MODULATIONS

Telecommand:

SQPN and data

- PN Range and Command Channel
PN Spread for ≤ 300 KBPS
- New 50 MBPS Ka-Band is
Balanced SQPSK

Telemetry:

- DG1, mode 1+2

SQPN and data

- PN Spread at Lower Rates

- DG1, mode 3

PSK in quadrature

- Only I-Channel is PN Spread

- DG2

BPSK, QPSK, SQPSK

- Unbalanced and Balanced Mode
- SQPSK Used for Equal
I & Q Data Rates

ATDRSS SIGNAL PARAMETERS

- Bent-Pipe as TDRS
- 1×10^{-5} BER
- Convolutional Encoding/Viterbi Decoding
at 1/2 & 1/3 rates for some modes as in TDRS
 - User can provide own End-to-End Encoding

CONCLUSIONS

- **No ATDRS Spacecraft Requirement for New Modulation Techniques**
- **Data Rate of 650 MBps is Required**
 - **Opportunities Exist for Applications of Advanced Modulation Techniques for Ground Data Distribution**
- **Space Station Freedom Requirement for 650 MBps Data Some Time After the Year 2000**

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INTERNATIONAL COMMUNICATIONS SATELLITE SYSTEMS

William W. Wu
INTELSAT
Washington, D.C. 20546

ABSTRACT

Ten satellite systems for international communication are briefly described. Modulation and coding schemes on some of these systems are highlighted.

An invited paper to be presented at the Advanced Modulation and Coding Technology Conference, sponsored by NASA Lewis Research Center, June 21-22, 1989.

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1.0 Introduction

After a quarter century of innovation, development, cooperation and services, satellite communications have had significant world wide impact and brings people closer than ever before. International satellite communications has increased by a factor of more than one hundred. Nearly two hundred countries and territories use satellite for television, radio, telephone and data services. As technology advances, service requirements and traffic patterns change, the interests of satellite communication communities also change. Among the changes is the creation of multiple international communication satellite systems.

In this paper an attempt is made to highlight these systems. Among the international systems considered are:

- INTELSAT
- INMARSAT
- MOLNIYA - STATIONAR
- EUTELSAT
- ORION
- ARABSAT
- ASIASAT
- ASTRA
- PANAMSAT
- HISPASAT

Although some of these systems are regional, in this paper a system is referred to as international if its operation is beyond the boundary of a single nationality. Otherwise they are referred to as domestic or national systems. A glance at some of the synchronous orbit satellites is shown in Figure 1 [1].

2.0 INTELSAT

INTELSAT is the international telecommunication satellite cooperative established by the world wide treaty. With 15 satellites the INTELSAT system covers all three oceanic regions over the globe. Its membership contains 115 countries and link together more than 165 countries and territories. At present, there are more than one thousand ground stations utilizing INTELSAT's space segments. Technically, INTELSAT was the first to use channelized repeater in INTELSAT IV, the first to exploit spatial re-use of frequencies in IS-IVA, the first to combine spatial and polarization frequency re-use in INTELSAT V, the first to implement high speed TDMA and SS/TDMA in INTELSAT VI, the first to use a linearizer in INTELSAT VII. Most of all, all INTELSAT digital systems employed error correcting codecs. A number of these codecs have been introduced into other international communication satellite systems.

To meet traffic demand the following INTELSAT systems have been implemented:

- FDMA/FM
- SPADE, SCPC
- IBS
- INTELNET
- TDMA
- IDR
- VISTA

Some of these systems are well known, others can be found in references [2, 3, 4, 5]. The INTELSAT gateway stations are shown in Table 1. The six INTELSAT satellite series are summarized in Table 2. The main features of INTELSAT VII is shown in Table 3. No new modulation and coding schemes have been proposed through the TDMA system to be operated on INTELSAT VII.

All INTELSAT digital systems employ phase modulation. For SPADE and SCPC systems rate $3/4$ self-orthogonal convolutional code with threshold decoding is used for 48 kbps data, the rate $7/8$ convolutional code are used for 56 kbps data. The (128, 112) BCH code of 120 Mbps is implemented in the INTELSAT TDMA system. The (24, 12) Golay code is used for digital speech interpolation assignment messages. For INTELSAT's IBS both rate $1/2$ and rate $3/4$ punctured convolutional codes with soft decision Viterbi decoding are part of the system. Operated from 64 kbps to 45 Mbps the INTELSAT Intermediate Data Rate (IDR) system has a constraint length 7 convolutional punctured code of code rate $3/4$ with Viterbi decoding [6].

3.0 INMARSAT

The system was established in 1979 and operational in 1982 for the purpose of international maritime communication. Today the INMARSAT system provides services to more than 70 countries. Among one of the most forward looking international organization INMARSAT not only provides services to ships in all three oceanic regions, but also is in the process of providing land mobile as well as aeronautical applications. In a recent paper on mobile satellite services Mr. Olof Lundberg, the Director General of INMARSAT set the tone for international co-ordination, co-operation and competition [7]. Coordination for networks operate within the allocated and limited L-band is essential, because such networks have been planned by Australia, Canada, France Japan, Mexico, Papua-New Guinea, U.S., U.S.S.R. as well as INMARSAT. Cooperation among the network providers, users and manufacturers can enhance the marketability and unify the compatibility. Competition can keep cost low and the quality of service high.

The INMARSAT system consists of the space segment, coast stations, and stations on ships. For the space segment INMARSAT currently leases capacity on various satellites, such as MARISAT of

COMSAT General, MARECS of ESA (European Space Agency), as well as INTELSAT satellites. At present there are 13 coastal earth stations coordinated by the Operations Control Center in London provide services to more than 4,000 ship stations. Most of these stations are 1.0 m in diameter, with 23 dB gain. The system supports data transmission up to 56 kbps [8].

Due to small antenna size on ships and severe fading environment error coding becomes essential. Comprehensive transmission channel modeling, analysis and simulation were provided by researchers at DFVLR. In addition, modulation and coding scheme for maritime satellite channel were evaluated. BPSK with differential coding were selected, and rate 1/2 constraint length 7 convolutional with interleaved Viterbi decoding as well as multiple burst error correcting Reed-Solomon code were recommended [9]. At present the INMARSAT system contains a (63, 57) BCH code for assignment and request messages, a (63, 39) BCH code for channel request messages. The ship-to-shore 56 kbps data transmission uses the convolutional code with soft decision. Rate 3/4 decoders are also implemented [6].

4.0 MOLNIYA-STATSIONAR

At least one hundred MOLNIYA satellites, over three series, were built and launched by the Soviet Union since 1965. Since 1970 MOLNIYA systems have provided international services mostly to neighboring U.S.S.R. countries. Since 1975 STATIONAR satellites have been continuously launched into the 80's.

STATIONAR satellites have associated a number of ground station networks including Orbita, Ekran and Moskva. Both MOLNIYA and STATIONAR satellite systems operated on the Intersputnik network for international communication. The Intersputnik network includes most communist east European and Asian nations with close relation to the Soviet Union such as Cuba.

Among other technical details the MOLNIYA and STATIONAR satellites differ in orbits. MOLNIYA systems operate on an elliptical inclined orbit and 62-65 degree inclination for power conservation and earth coverage. The STATIONAR satellites are operated on the synchronous equatorial orbit. The STATIONAR has three system variations: RADUGA, EKTRAN, and GORIZONT. Each system variation has a number of series.

For example, Raduga 20, EKTRAN 20 or GORIZONT 20. The STATIONAR satellites operation 5.7/6.2 GHz and 3.4/3.9 GHz bands. Although it is difficult to get detail information on these satellites some data is available from the U.S. Congressional Research Reports on Soviet Space Programs and other references cited by Martin [10]. As far as modulation and coding are concern, it is most likely phase modulation with convolutional coding have been used for their digital systems. This is judged from other scientific journals published in the U.S.S.R.

5.0 EUTELSAT

With 26 signatories the system was formally established in 1985 by the European Conference of Post and Telecommunication Organization (CEPT) and operated from Paris. Just as NASA has the mandate to support U.S. industry, EUTELSAT was created to promote satellite technology in Europe. From technical viewpoint EUTELSAT has had close association with the European Space Agency (ESA). The EUTELSAT TDMA system is operational since 1987.

The EUTELSAT system has four satellites in orbit and each satellite has ten transponders. Each transponder has 80 MHz or 72 MHz usable bandwidth. The system is operated at Ku-band. Each EUTELSAT satellite has three spot beams with both vertical and horizontal polarization. The second version of the EUTELSAT system is scheduled to be operational in 1990. The revised system has five satellites totaling sixteen transponders, nine of them with 36 MHz bandwidth and system is capable of controlling 29 traffic stations and each station can monitor 7 transponders. The countries (stations) can communicate through this system are: Austria (Aflenz), Belgium-Netherlands-Luxembourg (Lessive), Cyprus (Makarios), France (Bercenay-en-othé), Germany (Usingen), Italy (Fucino), Portugal (Sintra), Spain (Guadalajara), Sweden-Denmark-Finland-Norway (AEGSTA), Turkey (Ankara), and United Kingdom (Madley) [11, 12]. Seven of the transponders have 72 MHz usable bandwidth with a 50W TWTA, the EUTELSAT II has the unique switchable beam coverages. For narrow spot beam 50 dBW e.i.r.p. from the satellite is obtainable. For wide beam, coverage, 44 dBW is expected at edge of coverage. With EUTELSAT II satellites, the TDMA stations have diameters of 11m with G/T of 37 dB/K. The modulation for EUTELSAT digital systems is QPSK, and the error coding is the rate 7/8 (128, 112) BCH code as used in the INTELSAT TDMA system. Except the transmission rate of the EUTELSAT system is lower at 24.576 Mbps.

6.0 ORION

The ORION satellite system is planned to be implemented for international public telecommunication services between U.S., the U.K. and other possible countries in North America and Europe. To be expected operational in 1992 the ORION satellites are to be located at 322.5°E/37.5°W and 313°E/47.0°W in orbit. These satellites use 14 GHz for uplink and 11.45 - 12.2 GHz and 12.5-12.75 GHz for downlink. Each ORION satellite has 34 transponders in eight fixed beams. The bandwidth of each satellite is 2 GHz. Every satellite is to be operated at Ku-band. The satellites are designed to operate in both horizontal and vertical polarizations. The system is designed to provide digital services primary to VSAT stations with size from 1.2m to 1.8m. TVRO stations are of 0.85m. The maximum e.i.r.p. of a ORION satellite is 54.7 dBW.

Modulation for the ORION depends on the carrier type and information rate. For television services there are 17.5, 30, and 36 MHz analog FM bandwidths with frequency deviations of 7.5, 19 and 25 MHz respectively. Digital video is transmitted at 44.7 Mbps with QPSK. For information rates of less than 8 Mbps both BPSK and QPSK can be used. For data rate at 8 Mbps 8 OPSK will be used, For data rates between 40 Mbps to 60 Mbps, 16 QAM is proposed. For 140 Mbps, 64 QAM modulation will be implemented. Depending on the modulation scheme both rate 1/2 and rate 3/4 convolutional codes are used for error corrections.

7.0 Concluding Remarks

Based on Westar VI series satellites the first ASIASAT system is due to launch in the Spring of 1990 by the Chinese Long March III. The northern beam of ASIASAT intends to cover most China, India, Japan and the Northern part of Southeast Asia. The southern beam covers Thailand, Pakistan and may be Iran. Half of the ASIASAT system capacity may be expected to be used for television distribution.

ASIASAT has twenty four 36 MHz bandwidth transponders with dual polarization frequency reuse. Transmitters are operated at 3702 to 4198 MHz and the receivers are operated at 5927 to 6423 MHz. At edge of coverage the e.i.r.p per transponder is 34.5 dBW.

ARABSAT came into existence at the end of 1976 through the twenty two countries of the League of Arab States. Two satellites were launched in 1984. The technology of ARABSAT satellite centered around INTELSAT V and Telecom I. The communication subsystem uses C-band with one additional downlink at 2.5 GHz. Modulation is FM without channel coding.

ASTRA is operational since February 1989. The system is a Luxembourg based broadcasting network for the European continent. There are scrambling devices used in ASTRA system to black out the unintended receivers. 50,000 TVRO with such decoder are expected in 1989.

PanAmSat has been operational since June 1988 with a 24 - hour-per-day English language news service through Cable News Network(CNN). PanAmSat is in the process to expand the coverages to Peru, the Dominican Republic and Costa Rica, The digital carriers of PanAmSat system can also be operated from 64 kbps to 2.0 48 Mbps with QPSK modulation throughout. Error correcting. Code used are rate 1/2 constraint length 7 convolutional codes either with Viterbi decoding or sequential decoding. The choices of modulation and coding in the PanAmSat system are actually left to the users.

HISPASAT is recently proposed for 1992 by Spain to provide television services covering not only the country of Spain, but also Europe, North and South America. Thus it is classified here

as an international system. HISPASAT intends to use 1.2m to 4.5m earth stations at Ku band, and 2.0m to 2.5m antennas for television receive only. At C-band the system intends to have 2.6m to 7.0 earth stations. Technical details such as modulation and coding are not yet available.

From a brief review on international satellite communication systems in this paper, it is not very exciting to report the fact that with all the variation and technological advancement in modulation and error coding, very little has been actually introduced into these practical systems. It is time for modulation and coding experts to educate system decision makers to look beyond what has been done and to show what can be done. The NASA Conference on Advanced Modulation and Coding Technology is an important forum not only for sponsored industry briefing, but also a focal point of new modulation and coding techniques to be recommended for future satellite applications world wide.

References:

- [1] Pelton, J. and Wu, W. W. "The Challenge of 21st Century Satellite Communications: INTELSAT Enters the Second Millennium", IEEE Journal on Selected Areas in Communications, Vol. SAC-5, No. 4, May 1987
- [2] Wu, W. W., Elements of Digital Satellite Communication, Vol. I 1984, Vol. II 1985, Computer Science Press
- [3] Perillan, L. B. and Wu, W. W., "INTELSAT Services and Their Evolution" Proceedings of 1987 ICC.
- [4] Special Issue on INTELSAT TDMA/DSI, International Jr. on Satellite Comm. Vol. 3, No. 1 @ 2, Jan/June 1985
- [5] Special Issue on IDR, Intl. Jr. Satellite Comm., Vol. 6. No. 4, Oct/Dec 1988.
- [6] Wu, W. W., Haccound, D., Peile, R and Hirata, Y., "Coding for Satellite Communications", IEEE Journal on Selected Areas in Communication, Vol, SAC-5 No. 4, May 1987.
- [7] Lundberg, O. "Mobile Satellite Services: International Co-ordination, Co-operation and Competition" Proceeding of the mobile satellite conference, May 1988.
- [8] Ghais, A., Berzins, G., and Wright, D., "INMARSAT and the Future of Mobile Satellite Services", IEEE Jr. of selected Areas in Satellite Communications Vol. SAC-5, No. 4 May 1987.
- [9] Hagenauer, J., Dolainsky, F., Lutz, E., Papke, W., and Schweikert, R. "The Maritime Satellite Communicatio Channel - Model, Performance of Modulation and Coding", IEEE Jr. of selected Areas in Satellite Communications Vol. SAC-5, No. 4 May 1987.
- [10] Martin, D. Communication Satellites 1958-1988, Aerospace Corporation, 1988.
- [11] Carsuro, A. "The European Telecommunications Satellite Organization", Satellites International Macmillan Press Ltd. 1988
- [12] Celebiler, M., Fiedler, S., and Fresia "Testing of a TDMA System: The EUTELSAT Experience:", ICDS-7, Munich, May 1986.

TABLE 1: INTELSAT GATEWAYS

Type	Earth Station Standard	Antenna Size (m)	Minimum G/T (dB/°K)	Services	Frequency Bands (GHz)
LARGE (Country)	A	15-32	35.0	Telephony, data TV, IBS	6/4
	C	11-30	37.0	Telephony, data TV, IBS	14/11&12
	B	11-13	31.7	Telephony, data TV, IBS	6/4
INTER- MEDIATE (Teleport)	F-3	9-10	29.0	Telephony, data IBS, TV	6/4
	E-3	8-10	34.0	Telephony, data IBS, TV	14/11&12
	F-2	7-8	27.0	Telephony, data IBS, TV	6/4
	E-2	5.0-7.0	29.0	Telephony, data IBS, TV	14/11&12
SMALL (Business)	F-1	4.5-5	22.7	IBS, TV	6/4
	E-1	3.5	25.0	IBS, TV	14/11&12
	D-1	4.5-5.5	22.7	VISTA	6/4
VSAT TVRO	G	0.6-2.4 1.2-11	5.5 16	INTELNET TV	6/4;14/11&12 6/4;14/11&12
DOMESTIC	Z	0.6-32	5.5-16	Domestic	6/4;14/11&12

TABLE 2: INTELSAT SERIES

INTELSAT DESIGNATION	I	II	III	IV	IV-A	V	V-A	VI
Year of First Launch	1965	1967	1968	1971	1975	1980	1985	1989
Prime Contractor	Hughes	Hughes	TRW	Hughes	Hughes	Ford Aerospace	Ford Aerospace	Hughes
Width Dimension, m (Undeployed)	0.7	1.4	1.4	2.4	2.4	2.0	2.0	3.6
Height Dimension, m (Undeployed)	0.6	0.7	1.0	5.3	6.8	6.4	6.4	6.4
Launch Vehicles	Thor Delta	Thor Delta	Thor Delta	Atlas Centaur	Atlas Centaur	Atlas Centaur or Ariane 1, 2	Atlas Centaur or Ariane 1, 2	Ariane 4 or Commercial Titan
Design Lifetime, Years	15	3	5	7	7	7	7	14
Bandwidth, MHz	50	130	300	500	800	2,144	2,250	3,300
Capacity								
Voice Circuits	240	240	1,500	4,000	6,000	12,000	15,000	120,000
Television Channels	—	—	—	2	2	2	2	3

TABLE 3: INTELSAT VII MAIN FEATURES

- 3 dB more E.I.R.P. than IS-VA

Hemi	29.0	→	33 dBW
Global	26.5	→	29 dBW
Zone	29.0	→	33 dBW
C-Spot	NEW		(36.3 dBW)
Ku-Band Spot	41.0	→	45 dBW

- C-Band all SSPA
Better linearity
- Ku-Band TWTA/Linearizer
Better linearity → more capacity
3 Spot Beams
- More flexible for domestic connectivity
- TDMA

**Modulation and Coding Used
By A Major Satellite Communications Company**

K.H. Renshaw
Hughes Communications Incorporated
El Segundo, California 90245

ABSTRACT

Hughes Communications Inc. is a major satellite communications company providing or planning to provide the full spectrum of services available on satellites. All of the current services use conventional modulation and coding techniques that were well known a decade or longer ago. However, the future mobile satellite service will use significantly more advanced techniques. JPL, under NASA sponsorship, has pioneered many of the techniques that will be used.

THE COMPANY

Hughes Communications, Inc. owns and operates nine satellites, and has marketing rights to three more. The fleet is being expanded through launches and operating agreements, and by the end of 1989 HCI will own or have marketing responsibility for 12 satellites in orbit plus two more awaiting launch on the ground. The company owns and operates three Leasat satellites, with a fourth to be launched in the fall of 1989. The company also owns the three Galaxy C band satellites, the three Westar C band satellites, and a spare C band satellite on the ground. HCI also has marketing rights to the SBS K band satellites. Two are in orbit and the third will be launched next year.

The modulation and coding used on these nine satellites is representative of that used in the fixed satellite service industry as a whole.

CATEGORIES OF CUSTOMERS

HCI's customers have use commitments that vary from transponder ownership for the life of the satellite through half-hour transponder rentals to transmission of a single data packet. The Galaxy I satellite is used almost exclusively by cable TV broadcasters who purchased "condominiums" of transponders and actually own hardware on the satellite. On the other satellites, there are a number of companies who have long term leases of groups of transponders, single transponders, or partial transponders. Some of these operate their own networks while others pay for end-to-end turnkey service. HCI also has a substantial business in leasing transponders by the hour to broadcasters for sporting events and to companies that provide services

such as video conferencing.

In the near future, HCI, as an owner of the American Mobile Satellite Corporation, will be offering mobile packet data services to trucking companies and others requiring short paging, position, or status message transmissions. These users will pay by the packet. In the early 1990's, mobile digital voice service will be offered to the general public as a compliment to cellular radio service.

INVENTORY OF CODING AND MODULATION

Analog modulation fills the majority of the C band satellite transponders. FM transmission of NTSC TV is used with a single carrier per transponder. There is also a small amount of FM/FM telephony and a few FM audio broadcast feeds.

The digital modulation falls into four groups:

- 60-Mbps, QPSK telephone trunk modulation;
- Single or double 1.544-Mbps T-1 modulation;
- 300-bps to 56-kbps VSAT BPSK or QPSK modulation; and
- 150-bps to 19.2-Kbps spread-spectrum modulation.

The 60-Mbps telephone trunk modems use QPSK and occupy a full 34-Mhz transponder. As required by telephone practice, they are operated at a 10^{-7} BER. The links have a large margin to provide a high link availability. Error correction coding is not necessary because of the high link margins designed into the telephone system. These modems are available off the shelf from several companies. The technology needs for this service are generally well met. Relatively few of these modems are purchased every year.

The T-1 network modems are also operated at a 10^{-7} BER. The modems offer rates from 56 kbps to 3.152 Mbps and coding rates of 1/2, 3/4, or 7/8 convolutional coding. Typical link margins are 5 dB above the 10^{-6} BER requirement. Organizations currently purchasing these modems are concerned primarily with cost and number of features offered. The technology needs are well met. The total number of T-1 modems in use on satellite circuits is probably in the hundreds.

The VSAT modems business is booming. There are tens of thousands now in use and thousands more are being sold every year. These modems use rate 1/2 coding to provide a 10^{-7} BER on links with very little margin. This market is also cost and features driven; technology is not an issue.

Spread spectrum modems are used extensively. There are thousands of these modems now in service. A 2.456-Mcps direct sequence modulation is used to mitigate interference to/from adjacent satellites or terrestrial microwave stations. A broadcast service is offered at 19.2 kbps and an interactive service is offered at 153.6 kbps on the outbound link and 1200 bps on the return link. Spread-spectrum modems are also used by a position-fixing service that transmits spread-spectrum ranging signals simultaneously from three or four satellites. The data

rate is only 150 bps because only information attendant to the position fixing function is transmitted.

The mobile packet data modems will use BPSK at 300 or 600 bps. Rate 1/2 convolutional coding is used. The modems are designed to be compatible with INMARSAT Standard C. This same modem design will be used in a worldwide market. Only a few prototype modems now exist but several thousand are on order. By the mid 1990's hundreds of thousands of these units will be in use.

There is a competing packet data service that uses SSMA. This system uses a combination of frequency modulation, frequency hopping and direct sequence modulation to mitigate against adjacent satellite interference. The data rate is 22, 44, or 32 bps with rate 1/3 coding in the hub-to-mobile direction and 4960.3 bps with rate 1/2 coding on the return link.

In the future, a mobile digital voice service will be offered. Final modulation and coding techniques have not yet been determined. Voice coding to 4800 bps will be standard, while 9600-bps voice coding will be offered at a higher cost. The highest performance modems demonstrated to date have been designed and tested under NASA sponsorship at JPL. Those modems use rate 7/8 trellis coded 8DQPSK to provide 4800-bps service in a 5-kHz channel.

Consideration is also being given to providing mobile digital voice services with direct-sequence spread-spectrum modulation. Services using 8-Mcps QPSK with rate 1/3 convolutional coding have been demonstrated. Services using 1 to 2-Mcps rates are also being considered.

NASA sponsored a conference on mobile FDMA and CDMA architectural issues at JPL in March of 1989. Papers presented showed that CDMA allowed substantially more satellite capacity than FDMA. System operators are currently evaluating the conference results.

OBSERVATIONS REGARDING C BAND AND Ku BAND MODEMS

The modulation and coding technology used in the the C band and Ku band fixed satellite services is quite mature. Engineers specifying modems are generally more concerned with special features, cost, and delivery than getting the last fraction of dB performance. For all services except the 60-Mbps telephone trunk services, satellites generally have more bandwidth available than required. The satellites' power is not great enough to support the number of carriers required to fill the bandwidth. The next generation of satellites in the 1990's will have greater power and may fill the available bandwidth. More bandwidth efficient modulation and coding techniques will then be if the bandwidth is filled.

OBSERVATIONS REGARDING MOBILE SATELLITE TERMINAL MODEMS

NASA-JPL support of industrial R&D programs and propagation research has benefited U.S. industry. The work on modems and mobile antennas is the only U.S. source of performance data that can be used in system planning. The results of the work on radio propagation research has revolutionized the treatments of link margins. In 1985, 1988, and 1989, NASA

conferences for industry have transferred Government-sponsored technology to the private sector and have encouraged the exchange of ideas between conference participants. The timing of R&D programs has been excellent. NASA sponsored the effort early enough for U.S. industry was able to do the early research leading to products, but not so early that the technology was obsolete by the time markets were developed.

SUMMARY OF MODULATION AND CODING NEEDS AND OPPORTUNITIES

In summary, the current modulation and coding needs of commercial fixed satellite services are well met by industry. However, the next generation of satellites will require a new generation of modems which will then be available from industry.

In contrast, the modulation and coding needs of mobile satellite services are not currently being filled. Since standardization of modulation and coding techniques will be finalized by 1991, there is still room for innovative new techniques to be accepted for the first generation system in the next two years.

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13. ABSTRACT (Maximum 200 words) A conference on advanced modulation and coding technology development for space communications applications, sponsored by NASA Lewis Research Center, was held in Cleveland, Ohio on June 21-22, 1989. The objectives, approach, and status of all current Lewis-sponsored industry contracts and university grants are presented. The first section contains overviews of the Lewis space communications program, and advanced modulation and coding projects were presented. In the second section on bandwidth efficient modulation, the status of four contracts for development of proof-of-concept modems is reviewed by the contractors. The third section contains a review of modulation and coding work done under three university grants, two small business innovative research contracts, and two demonstration model hardware development contracts. The fourth conference session consisted of poster displays and hardware demonstrations; it is not reviewed herein. The last section of these proceedings addresses technology needs and opportunities for future missions. The final session of the conference was a panel discussion of issues related to the state of modulation and coding technology development; the content of the panel discussion is not contained in this conference publication.			
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