DIGITAL SYNCHRONIZATION AND COMMUNICATION TECHNIQUES

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RESEARCH IN DIGITAL SYNCHRONIZATION AND COMMUNICATIONS

- DIGITAL CODING/MODULATION UNDER INVESTIGATION
  - MPSK (BPSK, QPSK, OQPSK, MSK) OFFSET VS NON-OFFSET
  - MDPSK (DBPSK, DQPSK, ODQPSK, DMK)
  - CONVOLUTIONAL CODES AND TRELLIS-CODED MODULATION
  - BANDWIDTH EFFICIENT

- CHANNELS UNDER INVESTIGATION
  - AWGN
  - RAYLEIGH/RICE/SCINTILLATION
  - JAMMED

- RESEARCH EMPHASIZES
  ACQ
  - RAPID ACQUISITION WITH HIGH PROBABILITY
  - AVOIDING HANG-UP DURING ACQUISITION
  - AVOIDING CYCLE SLIPPING
  TRACK
  - MINIMIZE TRACKING JITTER
  - ELIMINATE PHASE AMBIGUITIES
  - ACHIEVING PERFORMANCE OF CODED-COHERENT COMMUNICATIONS
DIGITAL SYNCHRONIZATION PROJECT MOTIVATION

- FUTURE COMMUNICATION MODEMS ARE LIKELY TO EMPLOY ALL DIGITAL IMPLEMENTATIONS AS THE DIGITAL SIGNAL PROCESSING SPEED BARRIER BETWEEN DIGITAL AND ANALOG HARDWARE RISES DUE TO EMERGING TECHNOLOGIES, E.G., VLSI.

- COHERENT (C) VS. DIFFERENTIALLY COHERENT (DC) VS. NONCOHERENT (NC) DETECTION IN MODEMS
Desired Modem Implementation

DIGITAL SYNCHRONIZATION PROBLEM SPACE

CM: CONSTANT MODULUS
N-CM: NON-CONSTANT MODULUS
DA: DATA-AIDED
DD: DECISION DIRECTED
N-DD: NON-DECISION DIRECTED

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SALIENT CHARACTERISTICS OF OPEN LOOP DIGITAL SYNCHRONIZERS

- Derived from adaptive filtering theory
- Do not require locally generated sync reference by means of a VCO or NCO
- Sync reference is non-constant modulus
- Does not require a phase-error measurement to update phase estimate

OPEN LOOP PHASE AND FREQUENCY ESTIMATOR

\[ x(n) \rightarrow \text{MATCHED FILTER OUTPUT SAMPLE} \]

\[ r(n+1) \rightarrow \text{NOISY REFERENCE SAMPLE} \]

\[ RLS \text{ ESTIMATOR OF } k = \exp(j \omega_d) \]

\[ \beta - \text{SAMPLE WEIGHTING FACTOR} \]
EXPONENTIALLY WEIGHTED PHASE ESTIMATOR LEARNING CURVES.

\[ \beta = 0.875 \]

SYMBOL TO SYMBOL PHASE ROTATION LEARNING CURVE.

\[ \omega_0 = 1.0 \text{ radians/symbol} \]
A Digital Receiver Structure Utilizing an Open Loop Estimator in a Decision-Directed Architecture

\[ x(n) = d(n)e^{j\theta(n)} + \eta(n) \]
\[ r(n) = A(n)e^{j\hat{\theta}(n)} \]

The BER Learning Curve of the Exponentially Weighted Estimator for QPSK Modulation (E_b/N_o=2dB)
SIMULATED STEADY STATE WATERFALL CURVE OF THE EW DD ESTIMATOR FOR SQPSK MODULATION. $\beta = 0.875$

![Diagram showing the probability of bit error against Eb/No, dB for SQPSK and DESQPSK with $\beta = 0.875$.]
SIMULATED STEADY STATE WATERFALL CURVE OF THE EW DD ESTIMATOR FOR QPSK MODULATION. $\beta = 0.875$
PROBABILITY OF REMAINING IN A HANGUP CONDITION FOR BPSK MODULATION. \( R_b = 2\, \text{dB}, \beta = 0.875 \).

PROBABILITY OF REMAINING IN A HANGUP CONDITION FOR QPSK MODULATION. \( R_b = 2\, \text{dB}, \beta = 0.875 \).
'S' CURVE FOR A DECISION-DIRECTED BPSK AND QPSK LOOP EW ESTIMATORS

![Graph showing the 'S' curve for a decision-directed BPSK and QPSK loop EW estimators. The graphs depict the average innovation phase error versus estimator phase error for different Eb/No and Es/No values.](image)

- For Eb/No = 20dB:
  - Average Innovation Phase Error, degrees
  - Estimator Phase Error, degrees

- For Es/No = 20dB:
  - Average Innovation Phase Error, degrees
  - Estimator Phase Error, degrees
Motivation For Research

- Modems used in burst mode communication systems (TDMA or FHSS) or a fading channel typically use noncoherent demodulation techniques
  - PLL structures and fast acquisition with high probability requirements are not compatible
  - Coherent demodulation improves the performance

- Technology advances favor digital receiver structures
  - VLSI or gate array implementations can significantly reduce the cost, size, and possibly power consumption while improving the reliability of modems.