DIGITAL SYNCHRONIZATION AND COMMUNICATION TECHNIQUES

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RESEARCH IN DIGITAL SYNCHRONIZATION AND COMMUNICATIONS

- DIGITAL CODING/MODULATION UNDER INVESTIGATION
  - MPSK (BPSK, QPSK, OQPSK, MSK)
  - MDPSK (DBPSK, DQPSK, ODQPSK, DMSK)
  - CONVOLUTIONAL CODES AND TRELLIS-CODED MODULATION
  - BANDWIDTH EFFICIENT

- CHANNELS UNDER INVESTIGATION
  - AWGN
  - RAYLEIGH/RICE/SCINTILLATION
  - JAMMED

- RESEARCH EMPHASIZES
  - ACQ: RAPID ACQUISITION WITH HIGH PROBABILITY
    - AVOIDING HANG-UP DURING ACQUISITION
  - TRACK: AVOIDING CYCLE SLIPPING
    - MINIMIZE TRACKING JITTER
    - ELIMINATE PHASE AMBIGUITIES
    - ACHIEVING PERFORMANCE OF CODED-COHERENT COMMUNICATIONS
DIGITAL SYNCHRONIZATION PROJECT MOTIVATION

• FUTURE COMMUNICATION MODEMS ARE LIKELY TO EMPLOY ALL DIGITAL IMPLEMENTATIONS AS THE DIGITAL SIGNAL PROCESSING SPEED BARRIER BETWEEN DIGITAL AND ANALOG HARDWARE RISES DUE TO EMERGING TECHNOLOGIES, E.G., VLSI.

• COHERENT (C) VS. DIFFERENTIALLY COHERENT (DC) VS. NONCOHERENT (NC) DETECTION IN MODEMS
Desired Modem Implementation

DIGITAL SYNCHRONIZATION PROBLEM SPACE

CM: CONSTANT MODULUS
N-CM: NON-CONSTANT MODULUS
DA: DATA-AIDED
DD: DECISION DIRECTED
N-DD: NON-DECISION DIRECTED
SALIENT CHARACTERISTICS OF OPEN LOOP DIGITAL SYNCHRONIZERS

- DERIVED FROM ADAPTIVE FILTERING THEORY
- DO NOT REQUIRE LOCALLY GENERATED SYNC REFERENCE BY MEANS OF A VCO OR NCO
- SYNC REFERENCE IS NON-CONSTANT MODULUS
- DOES NOT REQUIRE A PHASE-ERROR MEASUREMENT TO UPDATE PHASE ESTIMATE

OPEN LOOP PHASE AND FREQUENCY ESTIMATOR

\[
x(n) \xrightarrow{\text{MATCHED FILTER OUTPUT SAMPLE}} x(n) \xrightarrow{\text{RLS ESTIMATOR OF } k = \exp(i \omega_d)} \xrightarrow{\text{REGISTER}} r(n+1) \xrightarrow{\text{NOISY REFERENCE SAMPLE}} r(n+1)
\]

\( \beta \) - SAMPLE WEIGHTING FACTOR
EXPONENTIALLY WEIGHTED PHASE ESTIMATOR LEARNING CURVES.

\[ \beta = 0.875 \]

![Graph showing the learning curve for exponentially weighted phase estimation with SNR=2dB and SNR=10dB.](image)

SYMBOL TO SYMBOL PHASE ROTATION LEARNING CURVE.

\[ \omega_0 = 1.0 \text{ radians/symbol} \]

![Graph showing the learning curve for symbol to symbol phase rotation with SNR=2dB and SNR=10dB.](image)
A Digital Receiver Structure Utilizing an Open Loop Estimator in a Decision-Directed Architecture

\[ x(n) = d(n)e^{j\theta(n)} + \eta(n) \]
\[ r(n) = A(n) e^{j\hat{\theta}(n)} \]

The BER Learning Curve of the Exponentially Weighted Estimator for QPSK Modulation (Eb/N0=2dB)

[Graph showing BER learning curve for QPSK and different values of \(\beta\)]
SIMULATED STEADY STATE WATERFALL CURVE OF THE EW DD ESTIMATOR FOR SQPSK MODULATION. $\beta = 0.875$
SIMULATED STEADY STATE WATERFALL CURVE OF THE EW DD ESTIMATOR FOR QPSK MODULATION. $\beta = 0.875$
PROBABILITY OF REMAINING IN A HANGUP CONDITION FOR BPSK MODULATION. $R_b = 2\text{dB}, \beta = 0.875$.

PROBABILITY OF REMAINING IN A HANGUP CONDITION FOR QPSK MODULATION. $R_b = 2\text{dB}, \beta = 0.875$. 
'S' CURVE FOR A DECISION-DIRECTED BPSK AND QPSK LOOP EW ESTIMATORS

![Graph showing the 'S' curve for BPSK and QPSK loop EW estimators with varying signal-to-noise ratios (Eb/No and Es/No). The graphs display the average innovation phase error in degrees as a function of the estimator phase error in degrees. The curves are labeled for different signal-to-noise ratios: 20dB, 10dB, 6dB, 3dB, and 0dB for both BPSK and QPSK.]
Motivation For Research

- Modems used in burst mode communication systems (TDMA or FHSS) or a fading channel typically use noncoherent demodulation techniques
  - PLL structures and fast acquisition with high probability requirements are not compatible
  - Coherent demodulation improves the performance

- Technology advances favor digital receiver structures
  - VLSI or gate array implementations can significantly reduce the cost, size, and possibly power consumption while improving the reliability of modems.