EMBEDDED MULTIPROCESSOR TECHNOLOGY FOR VHSIC INSERTION

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VHSIC SPACEBORNE MULTIPROCESSING

ADVANTAGES
• High Speed
• Fault-Tolerant
• Ada Language
• Maturing Component Base
NASA MULTIPROCESSOR TECHNOLOGY

OBJECTIVE
Develop multiprocessor system technology providing user-selectable fault tolerance, increased throughput, and ease of application representation for concurrent operation.

APPROACH
Develop graph management mapping theory for proper performance, model multiprocessor performance, and demonstrate performance in selected hardware systems.
MULTIPROCESSING TECHNOLOGY

Concurrent Processing Theory

ATAMM

TMR
Multiple processor types
Multiple graphs

GMOS
-1st Cut
-TMR/Simp
-Ada

VHSIC
Breadbrd
(EDM)

VHSIC
(ADM)

GVSC

RH-32

ADAS Multiprocessor Modeling
Graph Management Operating System (GMOS)

**Features**

- Distributed O/S and Nodes
- Real-Time Node Assignment
- Application Graph
- Node-Selectable Fault Tolerance
- Ada
- VHSIC 1750A

**Processor Assignment for Node Execution**
GMOS FUNCTIONAL FEATURES

• EXECUTES DIRECTED GRAPH - SINGLE GRAPH
  - MULTIPLE GRAPH

• GRAPH NODE CRITICALITY - TMR OR SIMPLEX

• GRAPH NODE SCHEDULING

  A) DATA DRIVEN - EVENT FLAG
  - SEMAPHORE (MULTIPLE EVENTS)
  - AND/OR LOGIC

  B) DEMAND DRIVEN - PERIODIC TIMER
  - ONE-SHOT TIMER

• BACKUP NODE ALLOCATION

• FAULTY PROCESSOR EXCLUSION, SELF TEST, REBOOT
ALGORITHM TO ARCHITECTURE MAPPING MODEL (ATAMM)

• A strategy for the real-time assignment of the nodes of a data-driven algorithm graph to parallel processors

• Based on Petri-Net marked graph theory

• Aimed at large-grain graph applications

• Provides:
  - deadlock-free performance
  - optimum time performance
  - operating system rules
  - performance prediction
ALGORITHM MARKED GRAPH (AMG)
FOR 7-NODE EXAMPLE GRAPH

LEGEND:
○ = TOKEN

Name

Time
NODE MARKED GRAPH (NMG) FOR DATA HANDLING

READ

PROCESS

WRITE

Tr → T3 → Tw

N3

T3 → N3
TBO = TIME BETWEEN SUCCESSIVE OUTPUTS

\[ TBO_M = \text{MINIMUM VALUE FOR TBO} \]

\[ = \text{MAX (TIME/NO. TOKENS)} \]

\[ = 6/2 = 3 \]
PROCESSOR REQUIREMENT PLOT
(SEVEN PROCESSORS AVAILABLE)

+ COMPLETION OF A NODE
■ COMPLETION OF NODE N5
PROCESSOR REQUIREMENT PLOTS

A) ONE PROCESSOR AVAILABLE

B) TWO PROCESSORS AVAILABLE

C) THREE PROCESSORS AVAILABLE

D) FOUR PROCESSORS AVAILABLE

E) FIVE PROCESSORS AVAILABLE

F) SEVEN PROCESSORS AVAILABLE
PERFORMANCE MARGIN

Throughput (Arbitrary Units)

No. of Processors

Max
NORMALIZED THROUGHPUT
VERSUS
NUMBER OF PROCESSORS

THROUGHPUT

1 2 3 4 5 6 7 8 9

NUMBER OF PROCESSORS

MAXIMUM PARALLELISM
(PERFORMANCE OF PURELY PARALLEL GRAPHS)

7-NODE GRAPH MARGIN
(ATAMM)

ACTUAL PERFORMANCE

IDLE TIME

OVERHEAD
ATAMM PROVIDES A NEW CAPABILITY SET

- Mathematically proven lock-free performance
- Operating system rules to manage the assignment of graph nodes to processors
- Prediction of graph's performance bounds
  - Maximum data rate
  - Maximum number of processors
  - Dependency of data rate on number of processors
# ATAMM DEVELOPMENT/DEMO PLANS

<table>
<thead>
<tr>
<th>STATUS</th>
<th>FEATURE</th>
<th>DEMO</th>
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<tr>
<td>Initial ATAMM</td>
<td>o Single graphs</td>
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<td>o Simplex</td>
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<td>o Identical processors (HW &amp; SW)</td>
<td>ADM</td>
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<td>Current Update</td>
<td>o Triple Modular Redundant (TMR)</td>
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<td>o Graph optimization for specific no. processors</td>
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<td>Future Features</td>
<td>o Multiple graphs</td>
<td>GVSC</td>
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<td></td>
<td>o Multiple iterations of the same graph</td>
<td>and/or</td>
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<td></td>
<td>o Multiple processor types</td>
<td>RH-32</td>
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<td></td>
<td>o Variable node-latency times</td>
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MAJOR RESEARCH THRUST FOR FY90

- Implement ATAMM Rules into KOS
  - Simpler operating system than previous GMOS
  - Use Westinghouse Directed Graph Tool
  - Use 1553B to provide data I/O and monitor graph status
  - Improved version of Ada compiler
  - 2.5 MIPS VHSIC ADM 1750A processor

- Demo/Evaluate with Ada Algorithms
  - Test Algorithm (Scan-to-scan track correlation for SDIO)
  - Time-simulated graphs
  - Simplex/TMR
  - Fault injection and continued processing
MULTIPROCESSOR INTERFACE DIAGRAM

MICROVAX II
- COMPILATION
- DOWNLOAD
- DEBUG

IEEE 488

CPU 1

1553B

PC/AT
- CONTROL
- DATA IN/OUT
- GRAPH STATUS
- INSERT FAULTS
- RESULTS
- DISPLAY

CPU 2

CPU 3

CPU 4

MULTIPROCESSOR

PI BUS

194
V1750A ADM
Chassis/Module
- 1.25μ CMOS VHSIC
- μ-Coded CPU Plus 256K RAM
- Surface-Mounted Devices; Dual Board Module
- 5.88 x 6.44 Inches (SEM-E)
MAJOR PROGRAM MILESTONES

1) Integrate/Demo ATAMM and SDIO Algorithm on Avionics Advanced Development Model (ADM) FY 90

2) Adapt/Demo ATAMM-Based OS on GVSC FY 91

3) Expand ATAMM Capability and Adapt/Demo on RH-32 FY 94