

# Vertical Bloch Line Memory

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## *Extended Abstract-*

Vertical Bloch Line (VBL) Memory is a recently conceived, integrated, solid-state, block-access, VLSI memory which offers the potential of  $1\text{Gbit}/\text{cm}^2$  a real storage density, gigabit per second data rates, and submillisecond average access times simultaneously at relatively low mass, volume, and power values when compared to alternative technologies. VBLs are micromagnetic structures within magnetic domain walls which can be manipulated using magnetic fields from integrated conductors. The presence or absence of VBL pairs are used to store binary information. At present, efforts are being directed at developing a single-chip memory using  $25\text{Mbit}/\text{cm}^2$  technology in magnetic garnet material which integrates, at a single operating point, the writing, storage, reading, and amplification functions needed in a memory. This paper describes the current design architecture, functional elements, and supercomputer simulation results which are used to assist the design process.

The current design architecture uses three metal layers, two ion implantation steps for modulating the thickness of the magnetic layer, one ion implantation step for assisting propagation in the major line track, one NiFe soft magnetic layer, one CoPt hard magnetic layer, and one reflective Cr layer for facilitating magneto-optic observation of magnetic structure. Data are stored in a series of elongated magnetic domains, called stripes, which serve as storage sites for arrays of VBL pairs. The ends of these stripes are placed near conductors which serve as VBL read/write gates. A major line track is present to provide a source and propagation path for magnetic bubbles. Writing and reading, respectively, are achieved by converting magnetic bubbles to VBLs and vice versa. The output function is effected by stretching a magnetic bubble and detecting it magnetoresistively.

Experimental results from the past design cycle created four design goals for the current design cycle. First, the bias field ranges for the stripes and the major line needed to be matched. Second, the magnetic field barrier between the stripe and the read/write gates needed to be reduced. Third, current conductor routing needed to be improved to reduce occurrences of open-circuiting, short-circuiting, and eddy-current shielding. Fourth, a modified Co-alloy was needed with an increased coercivity and controlled magnetization to allow VBL stabilization to occur without affecting stripe stability.

## 1 Introduction

Vertical Bloch line (VBL) memory [1],[2],[3] is a solid-state, radiation-hard, nonvolatile, block access, magnetic VLSI memory. Research and development efforts for this novel memory are being pursued in the United States, Europe, and Japan. Table 1 shows the potential storage density that is achievable with VBL memory. The densities are a function of stripe width and line feature width, which are defined respectively by the magnetic garnet material and the lithographic process.

	$L_f = 1\mu m$	$L_f = 0.5\mu m$	$L_f = 0.1\mu m$
$s_w = 5\mu m$	10Mbits/cm <sup>2</sup>	20Mbits/cm <sup>2</sup>	100Mbits/cm <sup>2</sup>
$s_w = 2\mu m$	25Mbits/cm <sup>2</sup>	50Mbits/cm <sup>2</sup>	250Mbits/cm <sup>2</sup>
$s_w = 1\mu m$	50Mbits/cm <sup>2</sup>	100Mbits/cm <sup>2</sup>	500Mbits/cm <sup>2</sup>
$s_w = 0.5\mu m$	100Mbits/cm <sup>2</sup>	200Mbits/cm <sup>2</sup>	1000Mbits/cm <sup>2</sup>
$s_w = 0.25\mu m$	200Mbits/cm <sup>2</sup>	400Mbits/cm <sup>2</sup>	2000Mbits/cm <sup>2</sup>

In a VBL memory, information is stored using VBL pairs in magnetic stripe domains in magnetic garnets. The presence or absence of a vertical Bloch line pair in a bit-cell location defines a binary "1" and "0," respectively. Input to the chip is performed by converting currents into magnetic bubbles and then into VBL pairs. Output sensing is performed by converting VBL pairs into magnetic bubbles and sensing magnetic bubbles magnetoresistively.

## 2 Present Device Design

### 2.1 Fabrication

The present design uses the magnet garnet,  $(BiYGdHoCa)_3(FeGeSi)_5O_{12}$ , as the storage medium. The thickness, stripe width, collapse field, saturation magnetization, and anisotropy field of the film is approximately  $2.4\mu m$ , 230 Oe, 450 Oe, and 1800 Oe, respectively. The film is grown epitaxially on a non-magnetic gadolinium-gallium-garnet (GGG) substrate. These films are transparent but also have a large Faraday rotation, so that magnetic stripes, magnetic bubbles, and, under certain conditions, VBLs can be observed magneto-optically with polarized light using the Faraday effect in a polarized light microscope.

The magnetic garnet has perpendicular magnetic anisotropy so that magnetization lies perpendicular to the film plane, with the bulk of the film magnetized in one direction, and the stripes in the opposite direction. A magnetic domain wall is the boundary between the stripe magnetization and the magnetization of the rest of the film. A twist of magnetization in the domain wall in the plane of the film is a VBL, and two such twists form a VBL pair. If the chirality, or sense of rotation, of the VBLs in the wall is the same, the VBL pair is stable, with a size calculated to be much less than  $1\mu m$ . The VBL pair is bound together energetically by VBL demagnetizing field energy and magnetic exchange energy.

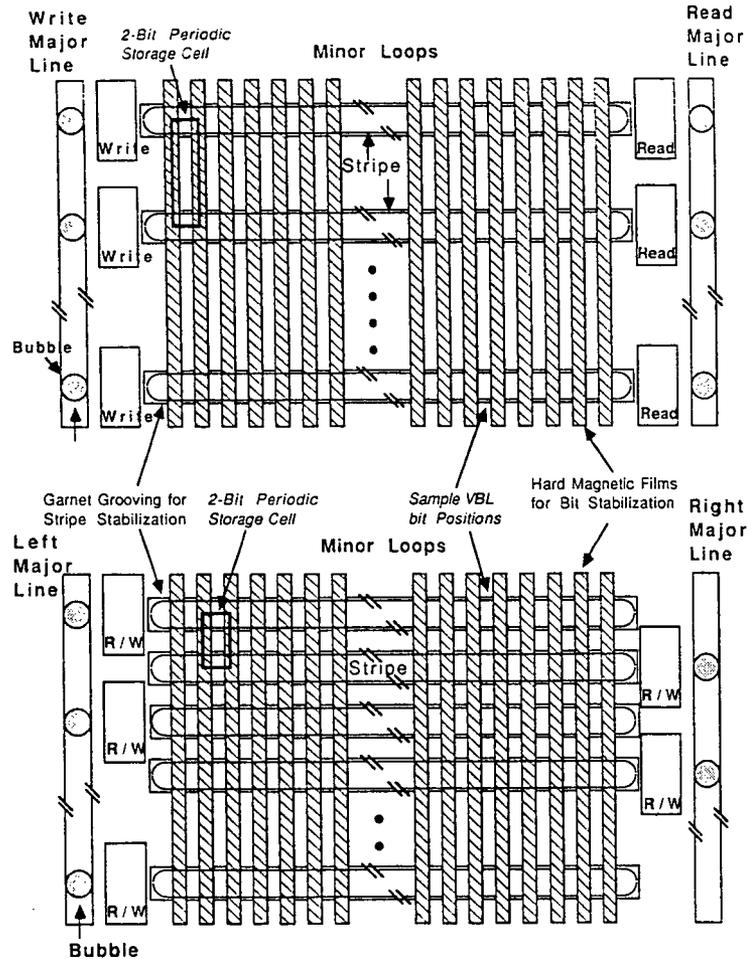
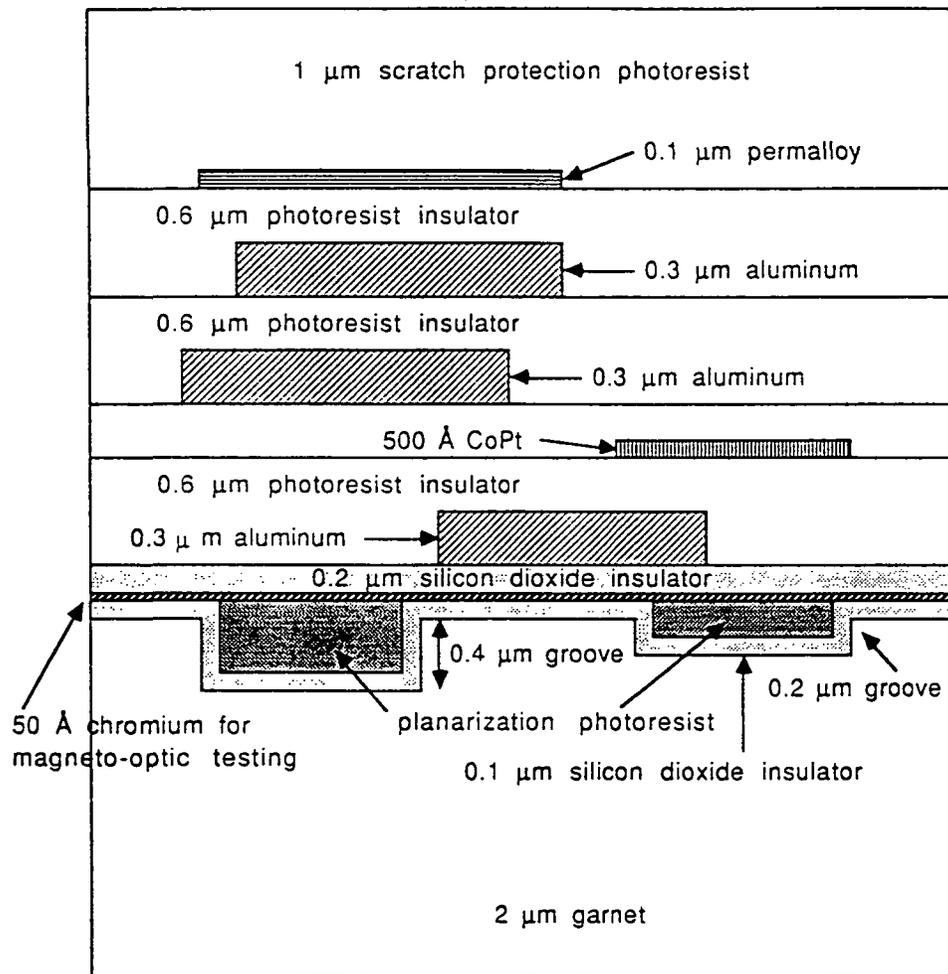


Figure 1: Schematic VBL architecture

The present device is divided into four main functional areas. First, the VBL storage area is designed to confine and stabilize stripe domains. Second, read/write gates are needed to convert VBLs to bubbles and vice versa. Third, a major line is needed for propagating bubbles which are used for input and output. Fourth, the output detector is needed for generating the output signal voltage. Typical architectures for a VBL chip are shown schematically in Figure 1

The present device is built with ten mask layers as shown in Figure 2. Three metal mask layers are used for providing the contact pads and conductors which control the stripe generator, read/write gates, bubble generator, and major line.  $SiO_2$  and photoresist are used for insulating metal layers, and a window mask is used to open vias and contacts when needed between metal layers. Two ion implantation mask steps, using  $150keVNe^+$  ions at a dosage of  $4 \times 10^{15} ions/cm^2$ , are used so that, after etching, grooves which are  $0.2\mu m$  and  $0.4\mu m$  thick are created in the garnet film which create stable locations for VBL stripe domains in the presence of the applied bias field. An additional ion implantation mask layer is used in the major line to inhibit VBL formation in the input/output bubbles. A permalloy ( $Ni_{0.8}Fe_{0.2}$ ) mask deposition is used to develop a magnetoresistive sensor which

## Process Option

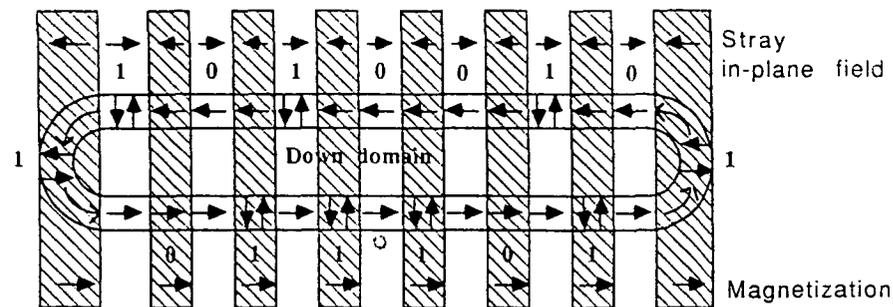


## Note:

1. Total of 10 masks are required.
2. Planarization is done by coating 0.6 μm photoresist, thermal flow the photoresist, then etch back.
3. Window mask is used five times to pattern all the photoresist and the scratch protection insulation layers.

**Figure 2: Current VBL fabrication process cross-section**

Counter-clockwise stripe without static in-plane field



In-plane field stabilized stripe

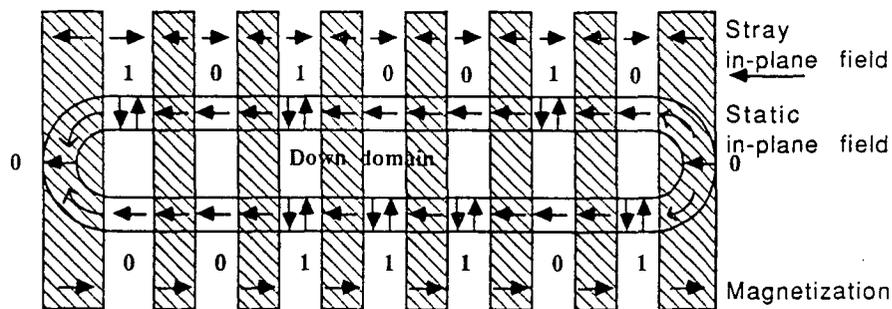


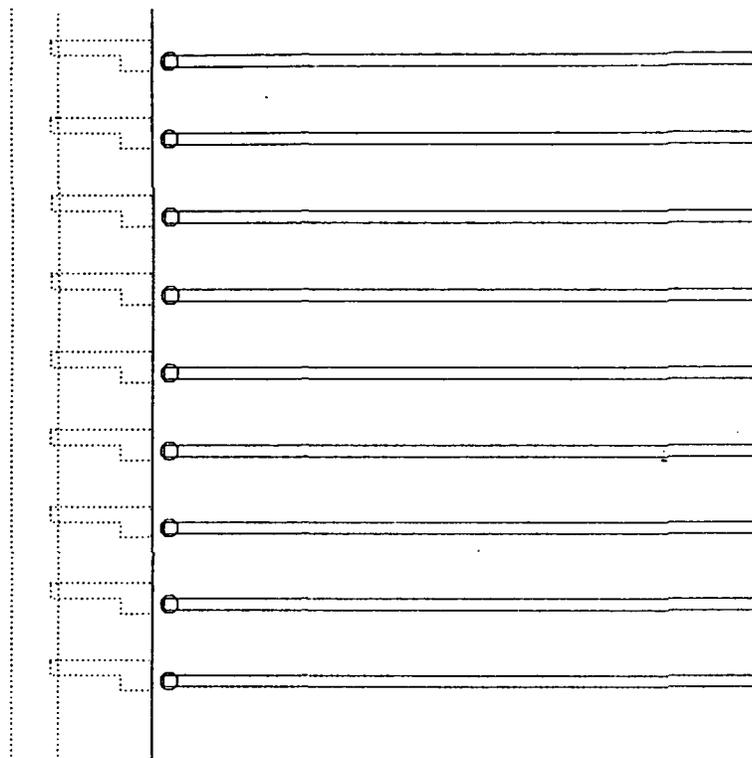
Figure 3: Schematic of VBL stripe storage structure

senses magnetic bubbles at the output and produces output voltages. A cobalt-alloy (i.e. CoPt) mask deposition is used for creating bit cells for VBL pairs along the walls of stripe domains. In test chips, a 5 nm thick Cr mirror layer is used to assist in stripe, bubble, and VBL observation using the magneto-optic Faraday effect during testing.

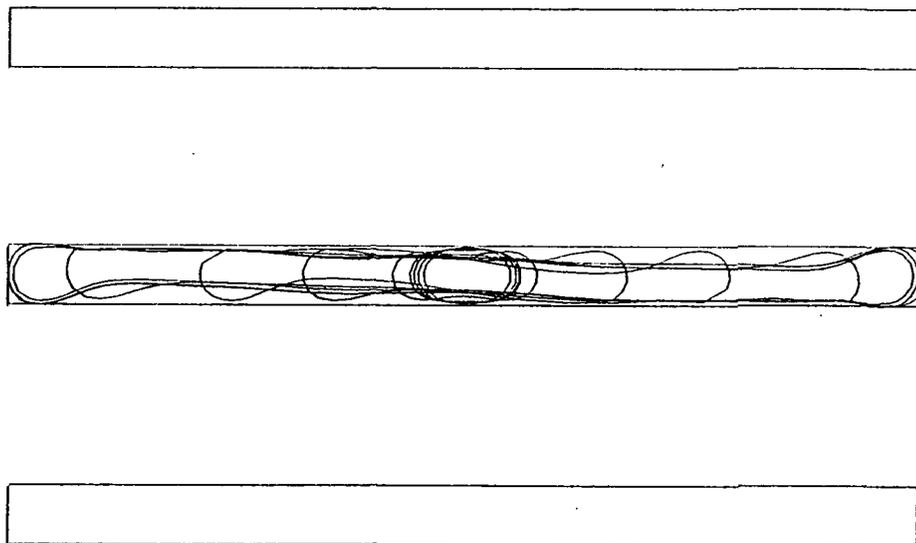
Supercomputer simulations [4],[5] which compute the effect of magnetic fields on magnetic domains, such as with stripe grooving, the major line, and the major line expander, are used heavily to assist in device design. VBL chip layouts are performed on an HP workstation and IBM PC/AT computers. Layouts are converted into fabrication masks via CIF and GDS II formats.

## 2.2 Stripe and Bit Stabilization

Data in the form of VBL pairs are stored in the domain walls of arrays of stripe domains as depicted in Figure 3. The stripes are physically located in grooved regions in the garnet, as shown in the partial design layout in Figure 4, which allows selecting the bias field so that stripes are stable when the other chip functions, including the major line, are operating. The demagnetizing field produced by the bias field at the edge of grooved regions serves to attract the stripe end and produce a stabilizing, effective edge-affinity magnetic field. The formation of stable stripes from nucleated isolated bubbles in grooved garnet is shown in Fig. 5. Computations were performed at 1 nsec time steps, and the computed stripe domain shape is shown at 40 nsec intervals.



**Figure 4: Layout of Garnet Grooving Structure for Stripe Stabilization**



**Figure 5: Supercomputer Time-Evolution Simulation of Stable Stripe Formation**

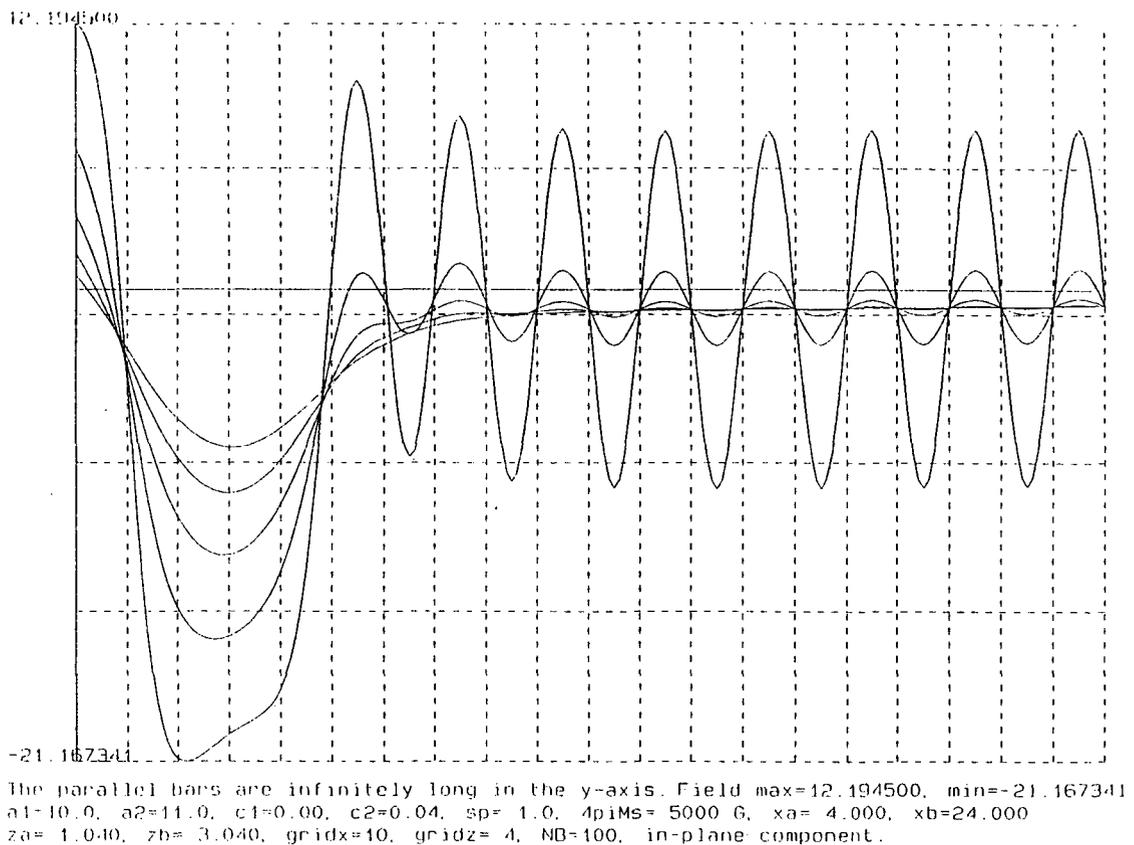


Figure 6: Computed Periodic Magnetic Field Profile of VBL Bit-Stabilization Cells

Bit stabilization is used to stabilize VBL pairs along the stripe. A periodic potential is placed along the stripe by an array of CoPt bars. For the CoPt, the saturation magnetization, coercivity, geometry, and spacing from the garnet are chosen to provide a sufficient field of approximately 5 Oe at the VBL stripe. This field value is currently considered to be enough to provide fields which create potential wells for the VBL pairs without disrupting the VBL pairs and moving stripes away from their groove-stabilized positions. The computed bit stabilization field profile at the end of an array is shown in Figure 6. The distance between the CoPt and the garnet film is a parameter. The periodicity in the field profile is clearly evident.

Propagation of the VBL pairs, around the bit cells and to the read/write gates, can be achieved in two ways. First, a vertical pulse field can be applied which presses, or rocks, the stripe against the groove wall which gyrotropically causes VBL pairs to propagate down the stripe. Second, an in-plane field can be applied which directly causes VBL pairs to advance along the stripes' walls.

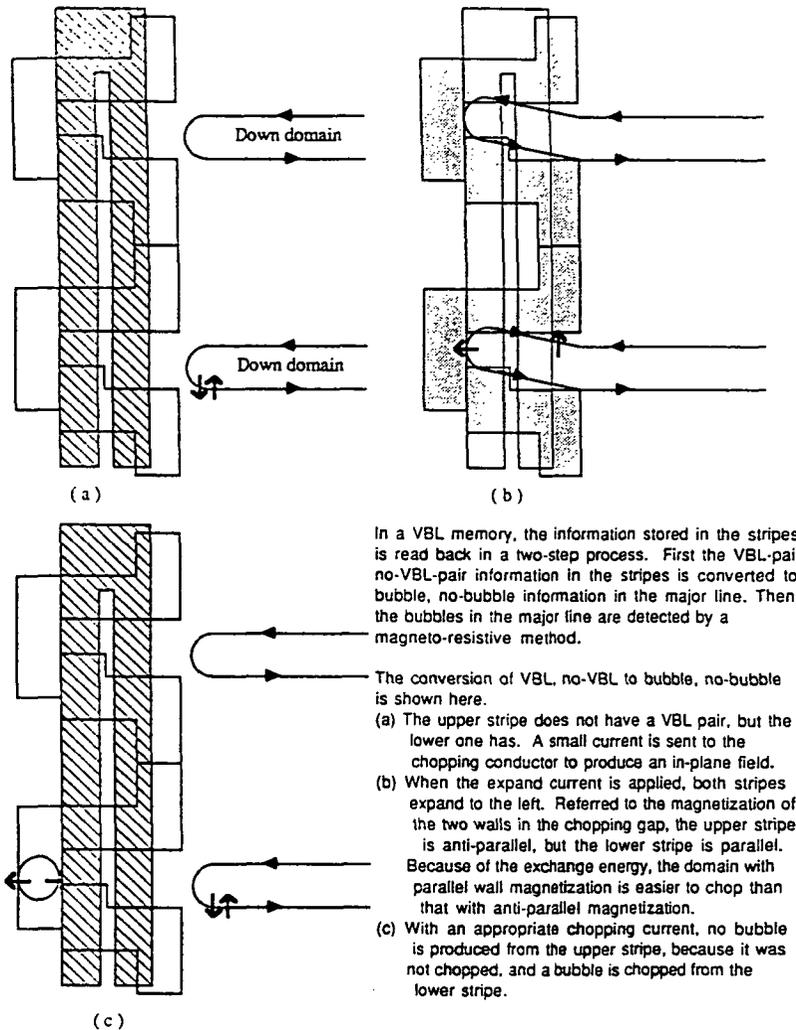


Figure 7: Depiction of VBL read process

### 3 Read/Write Gates

Read/write gates are used to convert VBL pairs in stripes into bubbles during the read process, and convert bubbles into VBL pairs during the write process. It is necessary to read and write both "1's" and "0's" correctly. Nondestructive readback is achieved by using a current in conductors to bring the end of a stripe out of its groove into the read write gate and into the presence of another conductor, as shown in Figure 7. If no VBL pair is present at the end of the stripe, the sense of the magnetization direction in the stripe wall causes the stripe to be difficult to chop with the field from a conductor because of exchange energy. The stripe is then returned to its stable position in the grooving. However, if a VBL pair is present, one VBL would be brought into the read/write gate while the other VBL would remain in the grooving, so the chirality of the stripe wall would be in the same direction which would readily allow it to be chopped. The chopped portion of the stripe becomes a bubble which can be propagated to the output for sensing, while the stripe returns to the grooved region and recreates a VBL pair leaving the information intact.

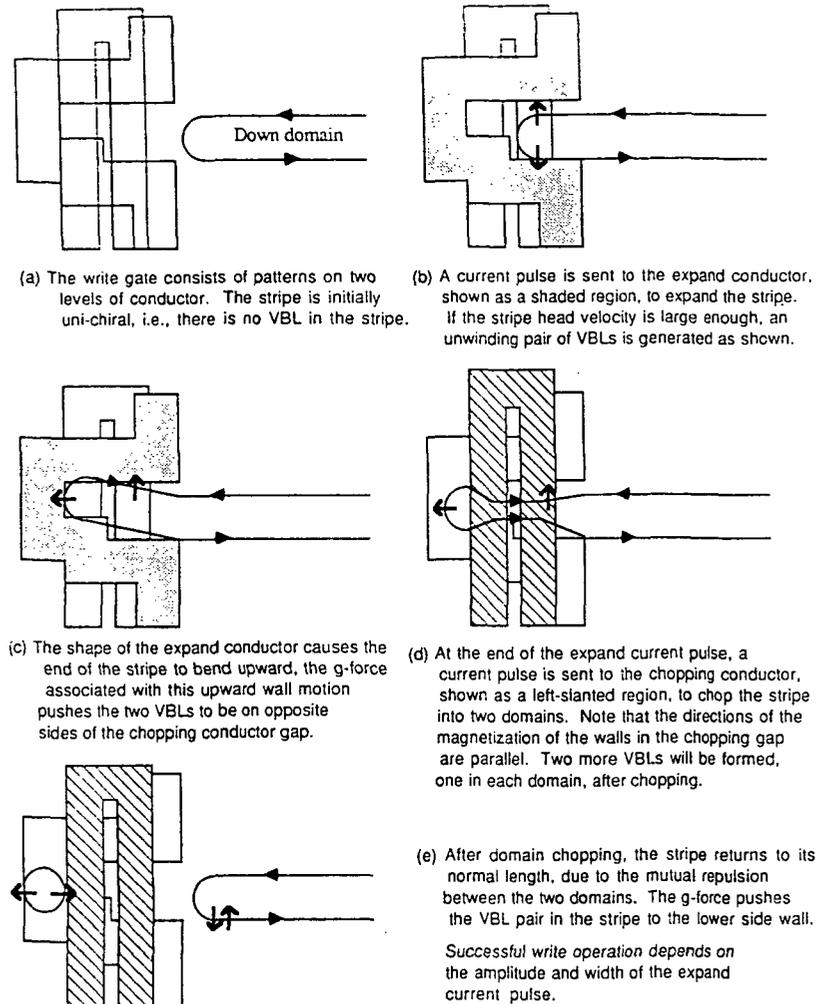


Figure 8: Depiction of VBL pair writing process

Writing is achieved by bringing a bubble from the nucleator and major line to the desired read/write gate. The writing process is shown in Figures 8 and 9. If a bubble is present, when the stripe is subjected to a field to bring it into the read/write gate, the stripe does not get drawn into the read/write gate because of magnetostatic repulsion between the bubble and the end of the stripe. Therefore, no writing to the stripe occurs. But if a bubble is not present, the stripe is brought rapidly into the read write gate which inserts a VBL pair into the stripe, and the stripe is then allowed to relax into the grooving.

### 3.1 Major Line and Output Detector

The major line consists of a bubble nucleator for converting input signal currents into bubbles, a track for propagating bubbles from the nucleator to the read write gates and from the read write gates toward the output, an output detector for converting the demagnetizing field from bubbles into output voltages, and an expander which is used to stretch a bubble to a desired length to provide a satisfactory signal-to-noise ratio at the output. These structures are now discussed.

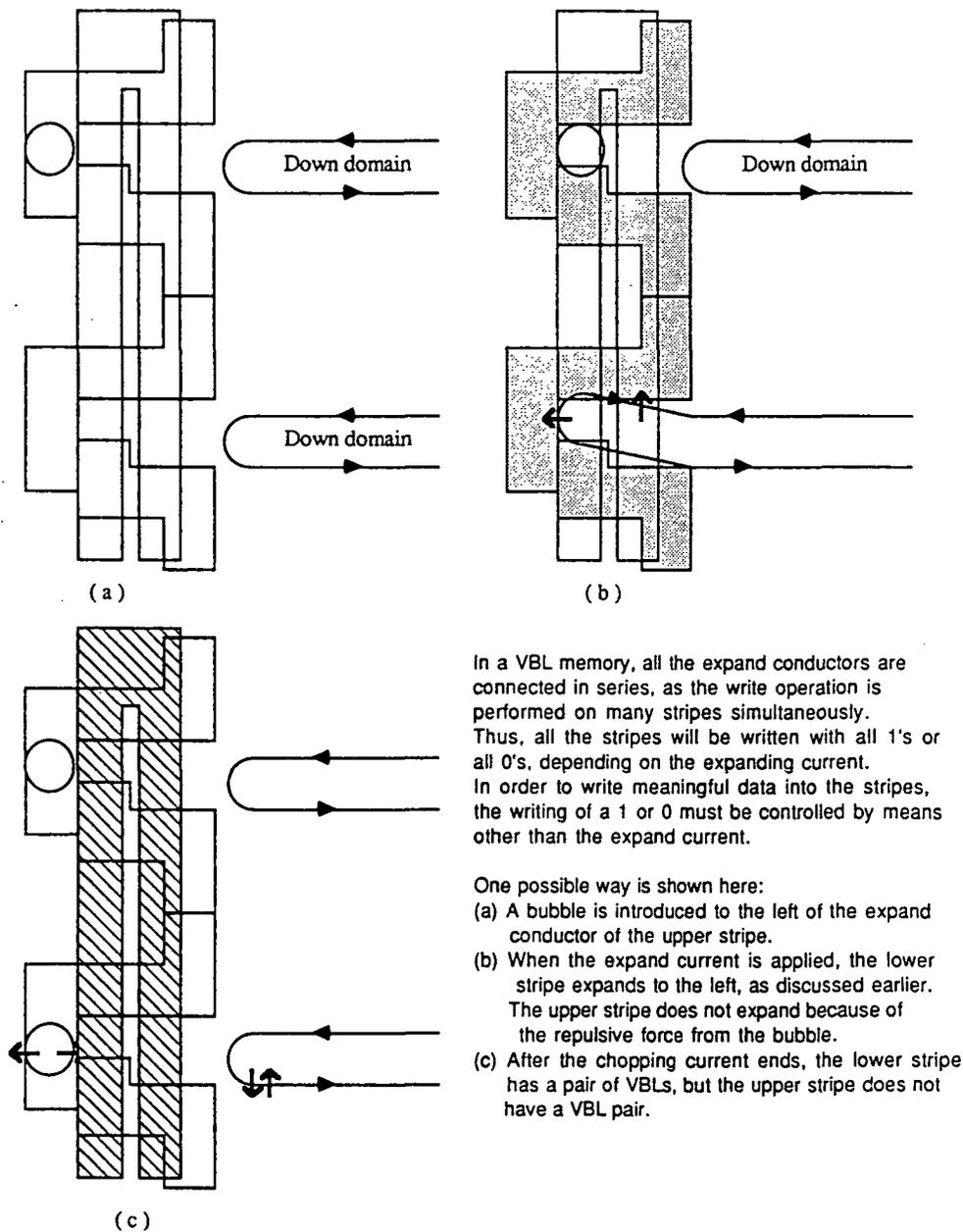
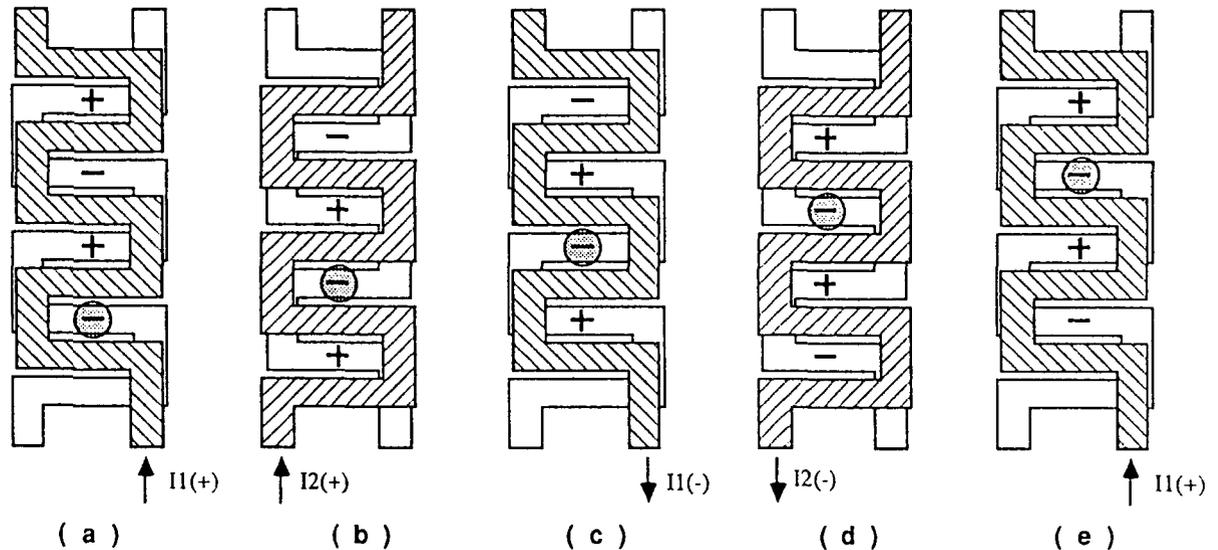


Figure 9: Depiction of binary VBL write process



A current in a zig-zag conductor, as shown in (a), produces an alternating magnetic field pattern which attracts or repels bubbles in sites along the conductor. By staggering two conductor patterns as shown, and alternating the current sent to each conductor, a track is defined which can propagate bubbles. Due to the low inductance of the conductor sheet, such a propagator can be operated at a very high frequency.

Figure 10: Principle of bubble propagation in a dual-conductor major line

A hairpin conductor is used for the nucleator. When a current is applied, such a conductor produces a magnetic field which is concentrated at the center of the hairpin. This field is used to generate bubbles which are used to transmit binary information to the VBL stripes via the read/write gates.

The propagation track in the major line consists of two levels of conductors. Each conductor is a serpentine arrangement of hairpin conductors which provide local magnetic field variations which form "waves" of stable positions for the bubbles down the track. The conductors are physically phase shifted by 90 to effect propagation. The principle of operation of the major line is shown in Figure 10. The layout of the major line track, along with the bubble nucleator and two read/write gates and grooves, is shown in Figures 11 and 12. Figure 12 shows the functional, two-metal major line and Figure 11 shows the major line with just one metal to help visualization.

The output detector consists of a rectangular strip of permalloy which is magnetoresistive. When a magnetic field as from a magnetic bubble is placed near the sensor, the resistance changes. When a reference current is issued to the sensor, the presence or absence of a bubble induces two different voltage levels to be generated which define binary

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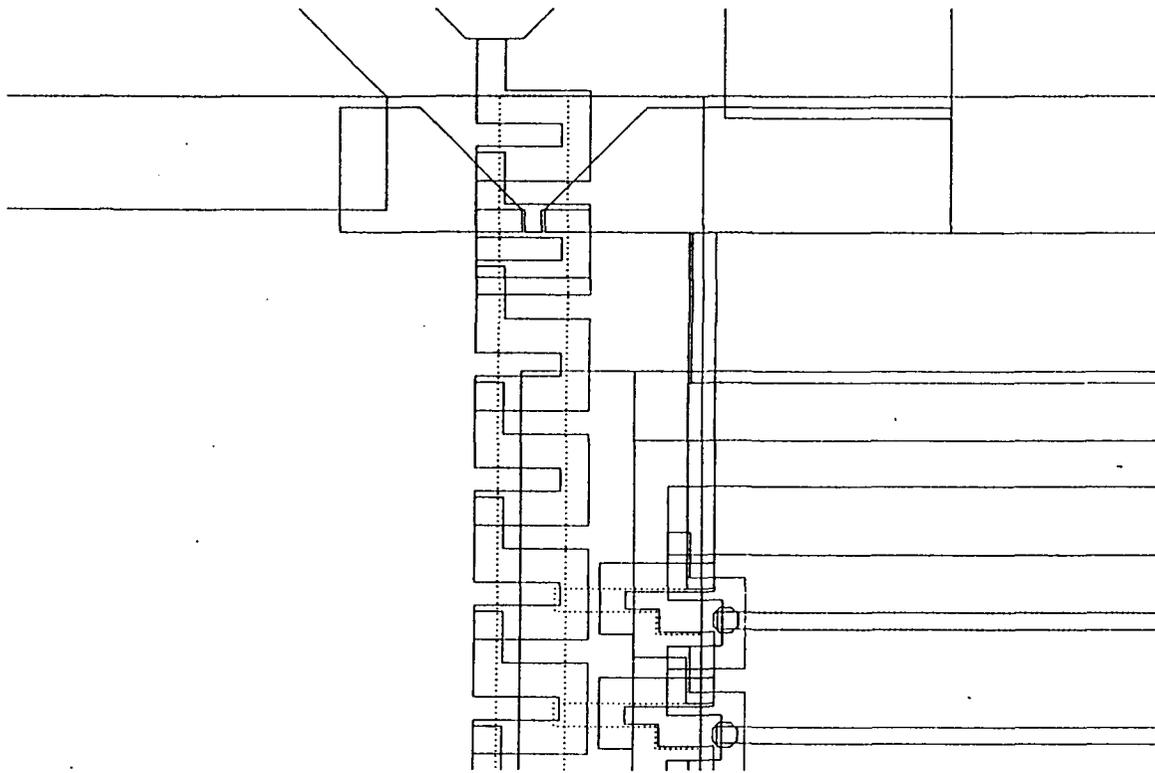


Figure 11: Layout showing nucleator, major line and two read/write gates and tow stripe grooves. only one major line conductor is shown for visibility

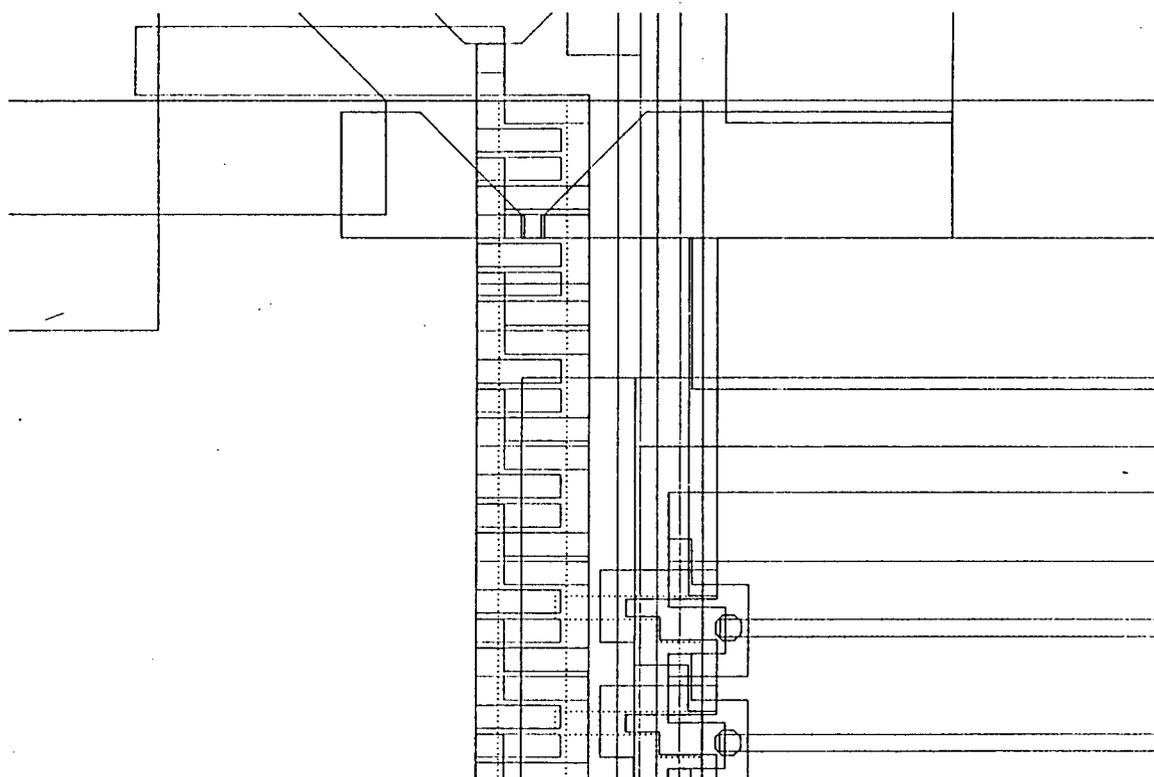


Figure 12: Layout showing nucleator, major line and two read/write gates and tow stripe grooves. Both major line conductors are shown

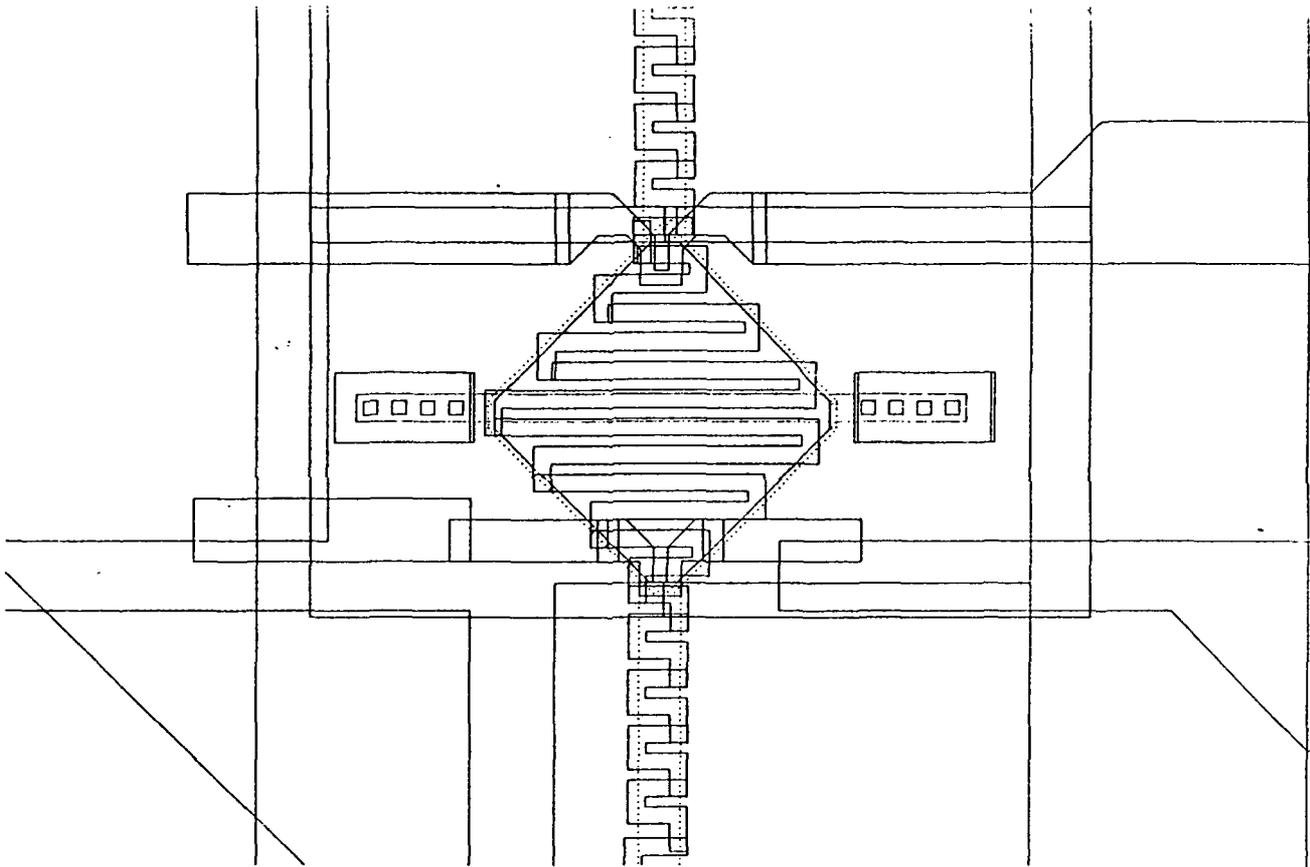


Figure 13: Layout of a VBL expander and output detector

"1's" and "0's." If it is necessary to maximize common-mode rejection from stray magnetic fields, two magnetoresistive sensors, including the actual sensor and a dummy sensor, are used which can be measured differentially. Since the signal from the magnetoresistive sensor is increased if longer elements with greater electrical resistance are used, the sensor length can be increased. Bubbles can be stretched in length to provide fields for the lengthened sensor by widening the bubble track as the bubble approaches the sensor. The combined output sensor and expanded major line are shown in Figure 13, where only one metal is shown in the major line for clarity. A supercomputer simulation, shown at 40 nsec intervals after being computed at 1 nsec intervals, of a bubble being stretched and then unstretched as it passes the expander and detector is shown in Figure 14.

## 4 Experimental Results

Sample experimental results of chip functions from past designs are now presented. [6],[7] These data were taken on test chips using a  $4.76\mu m$  thick  $(BiYSmLu)_3(FeGa)_5O_{12}$  garnet

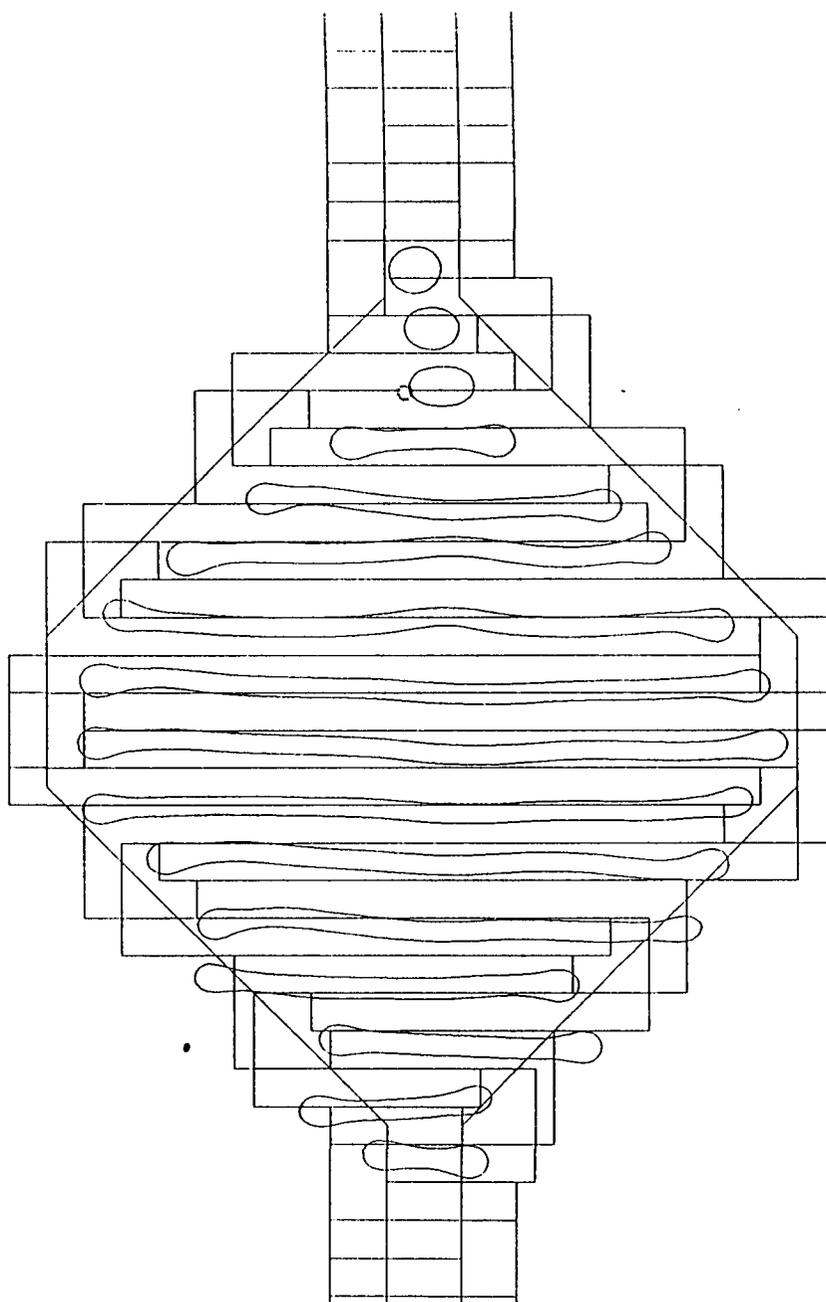


Figure 14: Supercomputer time evolution simulation of an expanding bubble in a major line expander and output detector

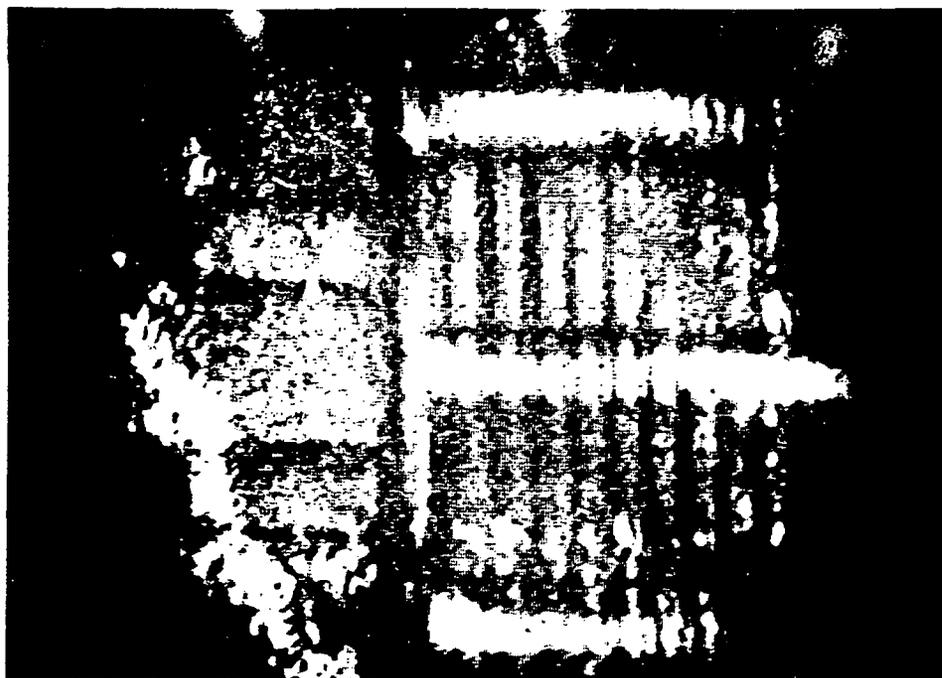


Figure 15: Photograph of stable stripes near the read/write gate end in a VBL test chip

film with a saturation magnetization of  $200Oe$ , zero-field stripe width of  $4.67\mu m$ , characteristic length of  $0.61\mu m$ , domain wall mobility of  $350cm/sec/Oe$ , anisotropy field of  $1350Oe$ , coercivity of  $1.1Oe$ , and collapse field of  $100Oe$ .

Figures 15, 16, and 17 show stabilized stripes in grooves, respectively, near read/write gates at the end of a groove, near the center of the stripe groove, and near the other end of the stripe away from a read/write gate. The stripes are observed with the magneto-optic Faraday effect as white strips against a green background caused by the illuminating laser light source. The dark bars running perpendicular to the stripes are cobalt bit stabilization bars. Figure 16 shows the conductor that was used to nucleate the stripes.

Figure 18 shows, in white, a nucleated bubble and a second bubble propagating along the major line. The nucleated bubble is large, because of the large reverse magnetic field which produces the bubble. As the bubble propagates away from the nucleator, the bubble diameter reduces to a nominal diameter dictated by the film and the applied bias field. Figure 19 shows bubbles in the major line further down the track. Bubbles and stretched bubbles in the expander portion of the major line near the output detector are shown as white spots and strips Figure 20.

## 5 Conclusion

VLSI designs, simulation results, and experimental results have been presented which describe current work on the storage and input/output functions for solid state, high density, nonvolatile, radiation hard, block access Vertical Bloch Line (VBL) memory. Such a memory offers the potential of achieving  $1Gbit/cm^2$ . Three metallizations are used along with three ion implantation steps, one permalloy magneto-resistive sensor deposition, and one

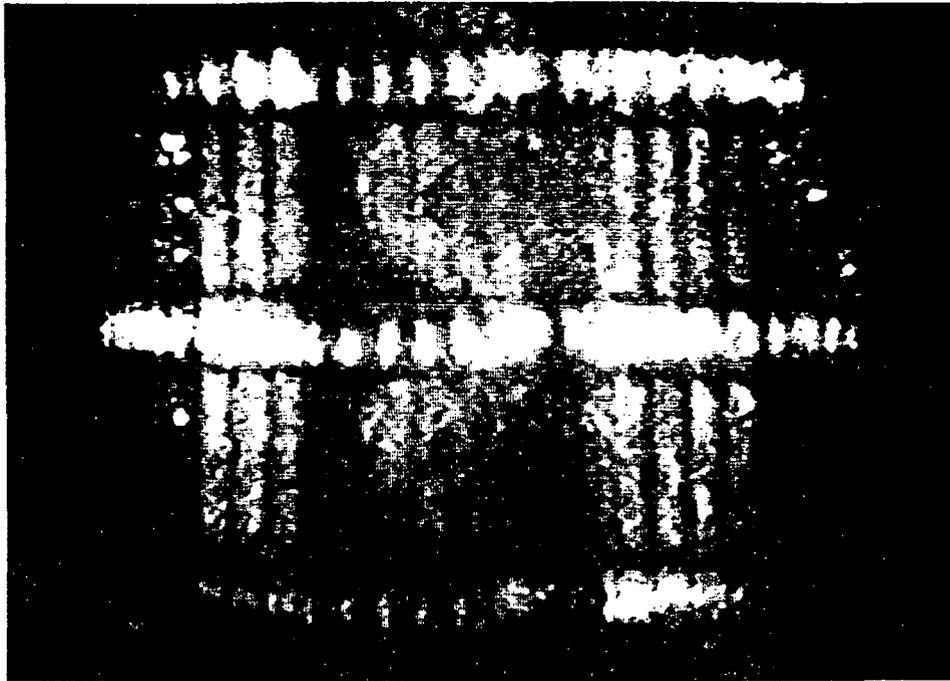


Figure 16: Photograph of stable stripes at the stripe's center near the stripe nucleator in a VBL test chip

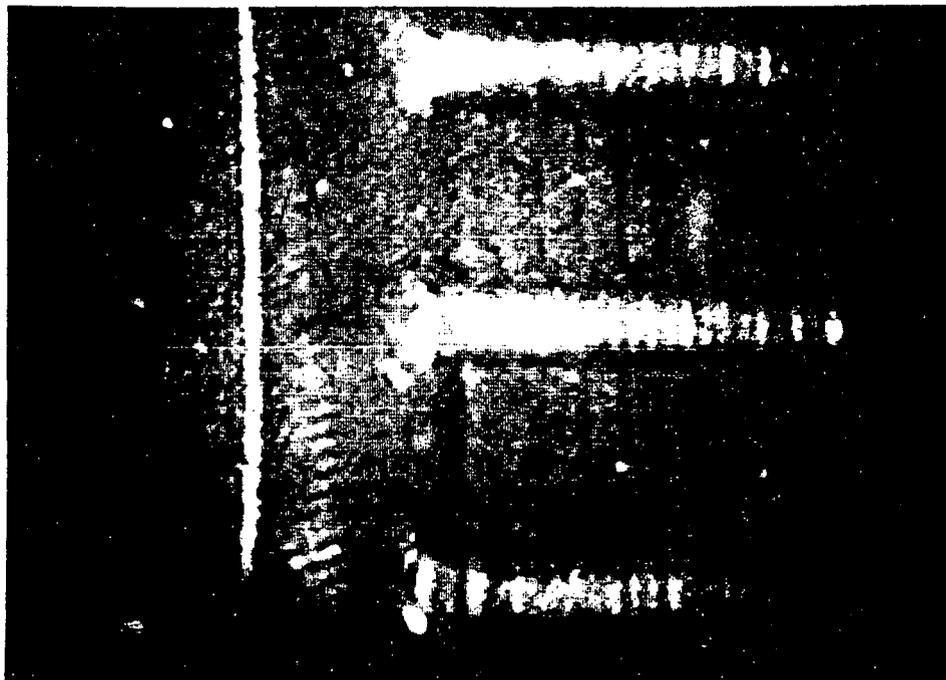


Figure 17: Photograph of stable stripes at an end away from read/write gates in a VBL test chip

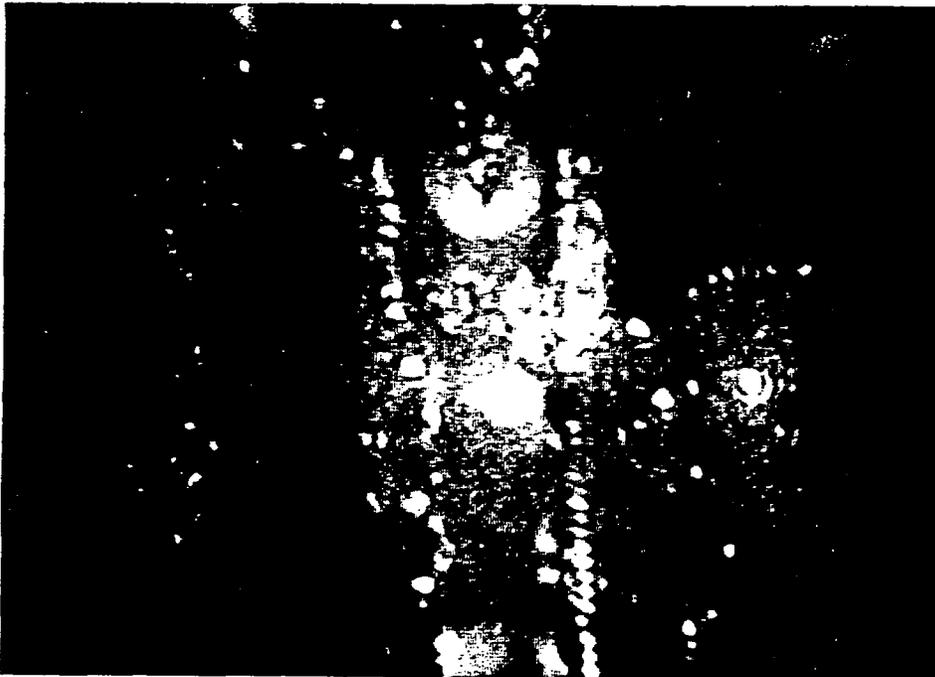


Figure 18: Major line and nucleator under operation

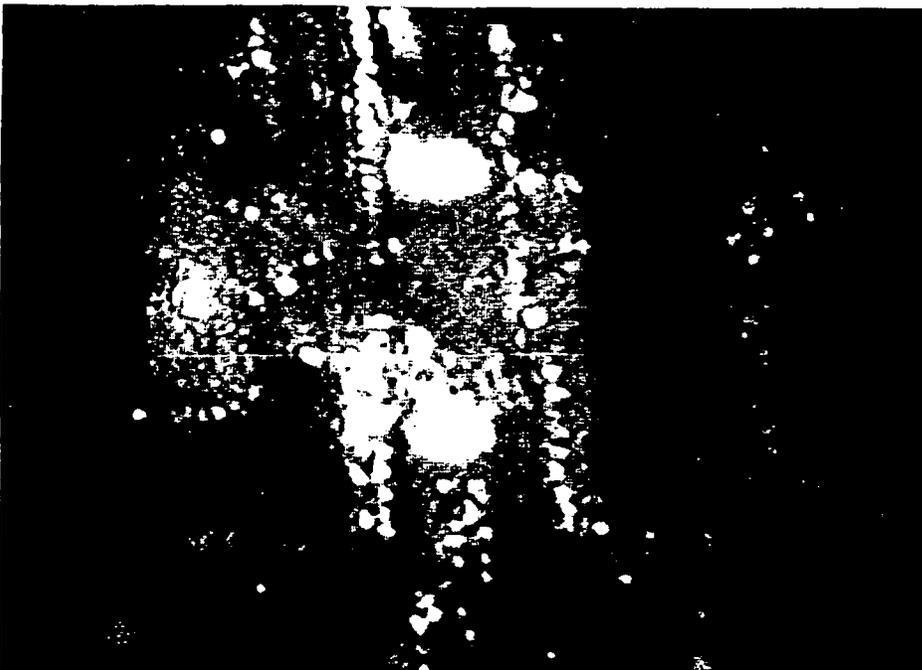


Figure 19: Major line under operation near the center of the major track



Figure 20: Major line and the major line expander under operation

CoPt bit-stabilization deposition. Previous and current experimental results and super-computer simulations indicate that individual storage, read/write gate, and input/output functions are feasible. Present work is aimed at integrating all necessary memory functions on a single chip to achieve simultaneous operation, a unique operating point, and a fully-functional single chip memory.

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