

IRVINE SENSORS CORPORATION

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June 1991**

**HYMOSS SIGNAL PROCESSING FOR
PUSHBROOM SPECTRAL IMAGING**

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16. Abstract The objective of the Pushbroom Spectral Imaging Program was to develop on-focal plane electronics which compensate for detector array non-uniformities. The approach taken was to implement a simple two point calibration algorithm on focal plane which allows for offset and linear gain correction. The key on focal plane features which made this technique feasible was the use of a high quality transimpedance amplifier (TIA) and an analog-to-digital converter for each detector channel. Gain compensation is accomplished by varying the feedback capacitance of the integrate and dump TIA. Offset correction is performed by storing offsets in a special on focal plane offset register and digitally subtracting the offsets from the readout data during the multiplexing operation. A custom integrated circuit was designed, fabricated and tested on this program which proved that nonuniformity compensated, analog-to-digital converting circuits may be used to read out infrared detectors. Irvine Sensors Corporation (ISC) successfully demonstrated the following innovative on-focal-plane functions that allow for correction of detector non-uniformities: Most of the circuit functions demonstrated on this program are finding their way onto future ICs because of their impact on reduced downstream processing, increased focal plane performance, simplified focal plane control, reduced number of dewar connections, as well as the noise immunity of a digital interface dewar. The potential commercial applications for this integrated circuit are primarily in imaging systems. These imaging systems may be used for: security monitoring systems, manufacturing process monitoring, robotics, and for spectral imaging when used in analytical instrumentation.					
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TABLE OF CONTENTS

1.0	PROJECT SUMMARY	1
2.0	INTRODUCTION	2
2.1	On-FPA Signal Processing	3
2.1.1	New versus Conventional Design Approach	4
2.1.2	Uniqueness of Design Circuitry	4
2.2	Program Approach	6
2.3	Program Results	6
2.4	Summary Conclusion	6
3.0	ELECTRICAL DESIGN	7
3.1	Requirements Analysis	7
3.1.1	Transimpedance Calculations	9
3.2	Circuit Descriptions	10
3.2.1	Operational Modes	10
3.2.2	Calibration Sequence	12
3.2.3	Analog Circuit	13
3.2.4	Digital Circuit	23
3.2.5	Power Dissipation	28
4.0	PHYSICAL DESIGN	30
4.1	IC Layout Criteria	30
4.2	IC Layout Floor Plan	30
4.3	IC Layout Details	30
4.4	Interface Control	33
5.0	IC TESTING	34
5.1	Test Equipment	34
5.1.1	Dewar Assembly	34
5.1.2	Focal Plane Control Unit	39
5.2	Test Results	47
5.2.1	First Iteration Analog Results	48
5.2.2	Second Iteration Results	52
5.2.3	Third Iteration Results	52
5.2.4	Electro-Optical Test	63
6.0	CONCLUSIONS	69

LIST OF FIGURES

Figure 2-1.	Pushbroom spectral imaging focal plane Block Diagram	2
Figure 2-2.	LWIR PV HgCdTe detector responsivity sample (Honeywell)	3
Figure 2-3.	The integrate and dump TIA	5
Figure 3-1.	Preliminary Block Diagram	8
Figure 3-2.	MWIR background flux	9
Figure 3-3.	Current due to background flux	10
Figure 3-4.	TIA gain initialization	11
Figure 3-5.	Flow diagram for the gain control logic	12
Figure 3-6.	Tetrode single ended amplifier	14
Figure 3-7.	Tetrode single ended amplifier Bode plot	15
Figure 3-8.	Single ended amplifier Bode plot	15
Figure 3-9.	Transmission gate switch	16
Figure 3-10.	NFET switch	16
Figure 3-11.	Spice analysis of transmission gate based current setting circuitry	17
Figure 3-12.	Spice analysis of NFET switch based current circuitry	17
Figure 3-13.	Binary weighted feedback capacitors	19
Figure 3-14.	Lowpass filter schematic	19
Figure 3-15.	Filter response with both poles at 320 Hz	20
Figure 3-16.	Filter response with 1st pole at 320 Hz & 2nd at 40 Hz	20
Figure 3-17.	Dynamic comparator with sample and hold schematic	21
Figure 3-18.	Relevant comparator voltages	22
Figure 3-19.	Dynamic comparator current vs. time	22
Figure 3-20.	Pushbroom digital Block Diagram	23
Figure 3-21.	Single slope A/D converter Block Diagram	24
Figure 3-22.	On-focal-plane A/D converter Block Diagram	25
Figure 3-23.	Offset and gain control logic Block Diagram for the Pushbroom IC	27
Figure 3-24.	Predicted power dissipation with a ± 3 volt power supply	29
Figure 4-1.	Pushbroom spectral imaging IC floor plan	31
Figure 4-2.	TIA/Filter critical cell	31
Figure 4-3.	Comparator critical cell	32
Figure 4-4.	Block diagram of the ADC registers	32
Figure 4-5.	One-bit section of the ADC registers	33
Figure 5-1.	Block Diagram of test equipment	35
Figure 5-2.	Test article fixture with a Pushbroom spectral imaging IC ready for immersion into an open mouth dewar	36
Figure 5-3.	Test being performed at liquid nitrogen temperatures	36
Figure 5-4.	Analog dewar cable	37
Figure 5-5.	Digital dewar cable	38
Figure 5-6.	Opto-isolation and buffer circuit between IC serial output data and data acquisition computer	40
Figure 5-7.	Computer interface box internal cable	41
Figure 5-8.	Feed through daughter board and connector	42
Figure 5-9.	Rack mounted level shifter	43
Figure 5-10.	Pushbroom level shifter (single channel schematic)	45
Figure 5-11.	Analog input box simulated detector input and level shift	46
Figure 5-12.	Detector common voltage generator	47
Figure 5-13.	Microphotograph of the Pushbroom IC	47
Figure 5-14.	Oscilloscope picture of TIA operation	48
Figure 5-15.	Amplifier closed loop gain for 1st iteration IC	49
Figure 5-16.	Amplifier transfer function for 1st iteration IC	49
Figure 5-17.	Filter frequency response for 1st iteration IC	50
Figure 5-18.	Oscilloscope picture of comparator operation	51
Figure 5-19.	Comparator trip voltage as a function of input level for 1st iteration IC	51

LIST OF FIGURES

Figure 5-20.	End-to-end analog transfer function of 1st iteration IC	52
Figure 5-21.	Pushbroom offset compensation test	55
Figure 5-22.	Transfer function from TIA input to digital output at the two extreme TIA settings	56
Figure 5-23.	IC output vs. gain set capacitance	57
Figure 5-24.	Calculated error in capacitance at each major gain set step	58
Figure 5-25.	Digital output as a function of time during a full scale gain adjustment	58
Figure 5-26.	Resolution of the ADC as a function of input voltage	60
Figure 5-27.	ADC linearity	61
Figure 5-28.	Pushbroom linearity	62
Figure 5-29.	End-to-end resolution	62
Figure 5-30.	CEC I-V plot of typical InSb detector (vendor data)	64
Figure 5-31.	I-V plot of two typical InSb detectors (ISC measurements)	65
Figure 5-32.	InSb RoA vs. temperature	66
Figure 5-33.	D^* vs. frequency for InSb detector 12G, @0mV bias	66
Figure 5-34.	D^* bias/InSb HYMOSS Chan 125, 114	67
Figure 5-35.	Voltage out vs. irradiance InSb	68

LIST OF TABLES

Table 2-1.	On Focal Plane Readout Electronics test results	6
Table 3-1.	Pushbroom Spectral Imaging requirements	8
Table 5-1.	Correlation between IC current and analog functionality	61

LIST OF APPENDIXES

APPENDIX A Digital Interface Control Document

1.0 PROJECT SUMMARY

The objective of the Pushbroom Spectral Imaging Program was to develop on-focal plane electronics which compensate for detector array non-uniformities. The approach taken was to implement a simple two point calibration algorithm on focal plane which allows for offset and linear gain correction. The key on focal plane features which made this technique feasible was the use of a high quality transimpedance amplifier (TIA) and an analog-to-digital converter for each detector channel. Gain compensation is accomplished by varying the feedback capacitance of the integrate and dump TIA. Offset correction is performed by storing offsets in a special on focal plane offset register and digitally subtracting the offsets from the readout data during the multiplexing operation. A custom integrated circuit was designed, fabricated and tested on this program which proved that nonuniformity compensated, analog-to-digital converting circuits may be used to read out infrared detectors.

Irvine Sensors Corporation (ISC) successfully demonstrated the following innovative on-focal-plane functions that allow for correction of detector non-uniformities:

- 1) Gain correction from $\pm 50\%$ to less than 1%
- 2) Offset correction from 100% to less than 0.05%
- 3) On Focal plane A to D conversion at 1000 Hz Frame Rate with 11 bits resolution
- 4) Focal plane mode switching, including calibration mode, through a Digital Signal Processor (DSP) compatible serial port.

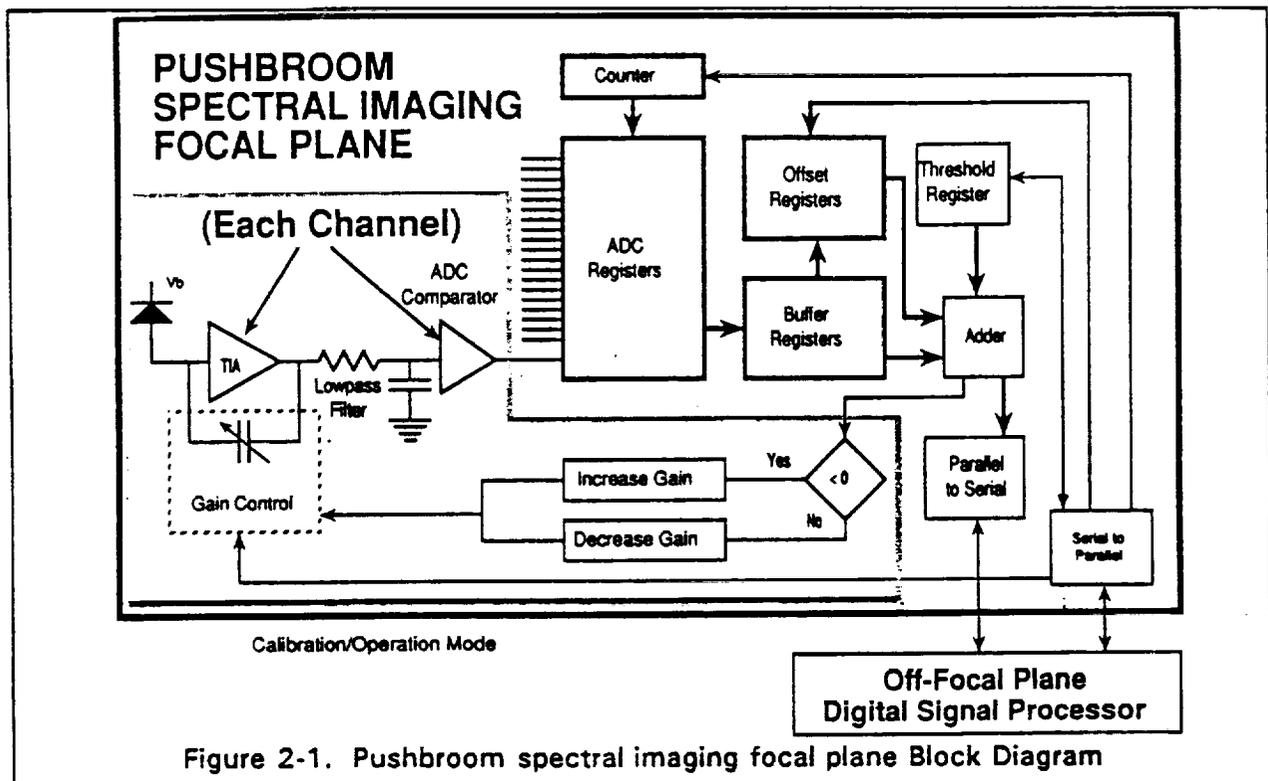
Most of the circuit functions demonstrated on this program are finding their way onto future ICs because of their impact on reduced downstream processing, increased focal plane performance, simplified focal plane control, reduced number of dewar connections, as well as the noise immunity of a digital interface dewar.

The potential commercial applications for this integrated circuit are primarily in imaging systems. These imaging systems may be used for: security monitoring systems, manufacturing process monitoring, robotics, and for spectral imaging when used in analytical instrumentation.

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2.0 INTRODUCTION

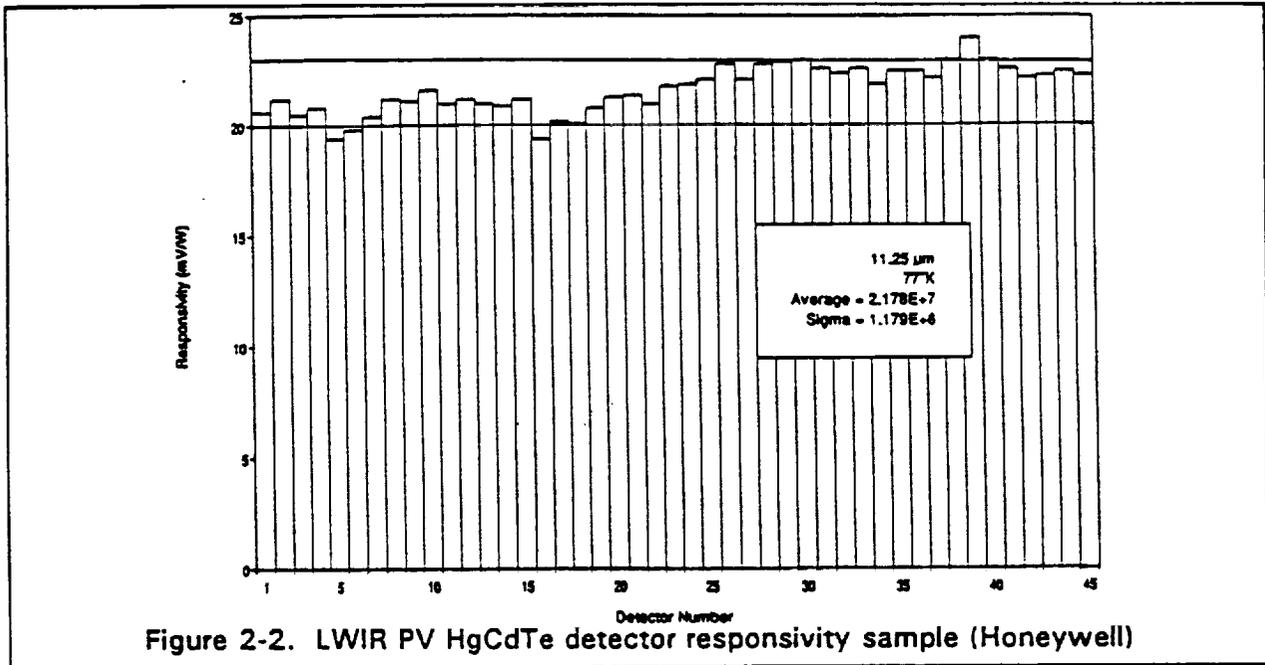
Pushbroom spectral imaging applications present unique problems in implementing an effective, efficient sensor system. ISC's approach focuses primarily on the removal of focal plane non-uniformities (gain and offset correction) prior to the transport of data off the focal plane. As shown in Figure 2-1, gain correction is performed at the detector interface, while offset correction is performed when the data is multiplexed off the focal plane. This approach provides the greatest potential for effective data compression routines and minimizes the preparation for data analysis. Each detector is followed by a transimpedance amplifier (TIA), lowpass filter, and analog-to-digital converter (ADC).



By removing focal plane nonuniformity artifacts prior to data compression, image entropy (amount of unpredictability in data) is significantly reduced. Thus, all data compression algorithms become significantly more effective. Spacecraft power requirements will be reduced by lowering the data bandwidth in the downlink. In earlier efforts to expand the design space, various schemes of data compression and data storage on the spacecraft have been used. However, the fixed pattern noise inherent in the focal plane adds entropy to the data. Figure 2-2 shows the variation typical of HgCdTe IR detector arrays. This

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provides a lower limit to the efficiency of data compression algorithms. For instance, the pixel-to-pixel differences in the scene are often a low value, providing a "compact" data set and leading to data compression algorithms of modest utility which have good noise immunity. However, the addition of the fixed pattern noise present on most infrared solid state sensors generally renders such modest data compression schemes ineffectual. Thus, the removal of non uniformities on the focal plane not only relieves ground data processing loads, but also reduces downlink bandwidth (with concurrent reduction in spacecraft power requirements) and reduces spacecraft data storage requirements.



A side benefit of the implementation used on the circuit developed on this program is the ability to perform first order differencing on the focal plane. This is accomplished by calibrating the offset control using the previous frame's data. In a scanning system, this means differencing adjacent pixels in the image. In a staring system, this represents frame differencing. For low cost systems, the requirement for a high performance computer to perform image compression is reduced while still enjoying the benefits of a lower data bandwidth.

2.1 On-FPA Signal Processing

Switched capacitor circuits are used in the on-focal plane signal processing electronics to allow real time changes. These changes are either implemented by changing the clock frequencies supplied to the circuit or by sending a new command word to the focal plane.

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This allows in-flight mode changes where spatial resolution, temporal sampling rates, encoding depth, and power dissipation may be controlled and traded off in real time as the mission proceeds. For instance, a low power, low resolution "survey" mode may be used in early portions of a flight. High resolution, wide dynamic range studies are then reserved for regions of particular interest on later orbits. Nonuniformity removal on the spacecraft enhances this interactive mode of earth resource investigations by making the data easily accessible to scientists on the ground since post-processing requirements are greatly reduced.

2.1.1 New versus Conventional Design Approach

Conventional focal planes provide wide bandwidth, low level, wide dynamic range video signals through the dewar wall. Such systems are inherently noise susceptible, and engender the levying of tight RFI emission standards on spacecraft subsystems. Improvement of sensor noise immunity provides one method by which overall system cost savings may be achieved. The relaxation of non-sensor noise standards could lower spacecraft weight since some shielding may be removed. A reduction in weight translates directly into cost savings and longer mission lifetimes.

Inclusion of nonuniformity removal and analog-to-digital conversion on the focal plane simplifies system testing. The imaging subsystem consists of a focal plane in a dewar and a digital focal plane controller. System partitioning will lead to focal planes which are each characterized as a complete functional subsystem, which have a minimum of interface complexity.

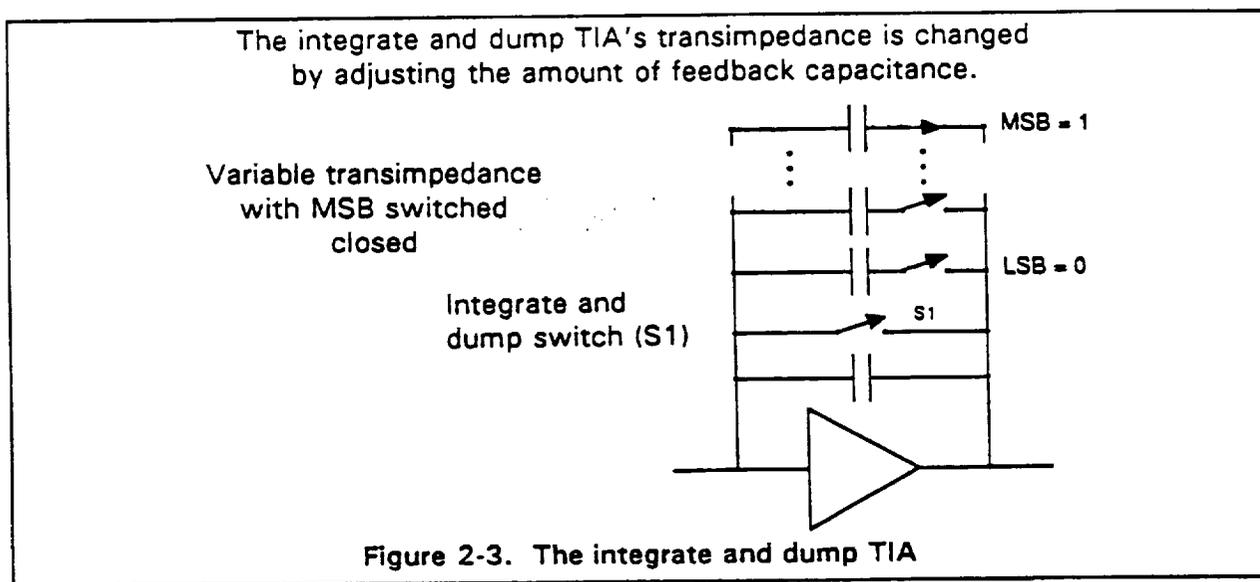
With this approach, all interfaces to the dewar are digital (except for three (3) low frequency triangle wave control signals used to generate bias currents on this IC) and therefore testable by digital pattern generators and data acquisition systems. Conventional focal planes are not as well suited in this regard due to the analog nature of their video interface, and the complex analog interactions between the controller and focal plane assembly. Eventually, ISC hopes to ultimately eliminate the low frequency triangle waves through the future development of a digital bias current generator.

2.1.2 Uniqueness of Design Circuitry

The unique portions of the circuitry developed on this program relate to performing on-focal-plane gain and offset calibration. Gain correction is implemented in the transimpedance amplifier, while offset correction is performed as the digital data is multiplexed off the focal plane.

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Gain correction is provided by using a high performance integrate and dump transimpedance amplifier. By varying the amount of feedback capacitance in the amplifier, Figure 2-3, the transimpedance (or gain) of the amplifier can be varied. Each amplifier's is adjusted to compensate for the inherent variations in the responsivity from detector to detector. Accomplished on a per detector basis, this results in a uniform photon to voltage transfer function across the array. Since this is a first order correction, higher order non-uniformities are minimized by providing a constant detector bias (usually zero volts) for all photon levels (*Nonlinear Compensation For Responsivity Nonuniformities In Cadmium Mercury Telluride Focal Plane Detector Arrays For Use In The 8 To 12 μm Spectral Region*, G.V. Poropat, *Optical Engineering*, August 1989, Vol. 28 No. 8). ISC's design addressed this issue, by modifying an existing single ended design to a tetrode configuration to provide more open loop gain.



Offset correction is provided by storing the digital output of the focal plane in memory. During each readout, the stored value is subtracted from the current value. If the stored value represents the output of the focal plane when exposed to a cold reference field, then offset correction is performed. If the stored value represents the output of the previous frame, then frame to frame differencing is performed. Thus, the same circuitry provides the ability to perform both offset correction and frame to frame differencing.

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2.2 Program Approach

The first step in the program was to review and verify the system requirements developed in the Phase I program. From this set of system requirements, a specification for the IC was developed. Using the specification, the requirements for each of the circuit cells (i.e., TIA, lowpass filter, comparator, etc.) were established. The circuit cells were then designed and simulated extensively using computer aided design tools. When possible, individual circuit cells were fabricated on test IC's to verify performance predictions and investigate possible tradeoffs. Finally, a 32 channel IC suitable to be used with detectors was laid out, fabricated, and tested.

2.3 Program Results

A to D conversion and gain and offset correction circuitry were tested and found to meet the design criteria. Excellent results were obtained from the testing of the IC in spite of a problem which caused large substrate currents. While these large substrate currents caused some limits on the end-to-end performance of the IC, the innovative features of the IC were tested and verified. The results of these tests are summarized in Table 2-1.

Table 2-1. On Focal Plane Readout Electronics test results

Gain Correction	$\pm 50\%$ to 1%
Offset Correction	25% to 0.05%
ADC Resolution	11 bits
ADC Linearity	≤ 0.12 LSB's

2.4 Summary Conclusion

ISC has successfully demonstrated the ability to provide non-uniformity correction on the focal plane. The gain correction circuitry operates as predicted and shows promise of providing even better than a 0.5% residual gain non-uniformity. The offset correction circuitry operated as predicted and was implemented in a fashion that should allow for data compression to occur on the focal plane. The measured resolution of the analog-to-digital converter appears to be test equipment limited at this time since the best theoretical performance for the test setup was 11.5 bits. Finally, the ability to control how the focal plane operates through a Digital Signal Processor compatible serial interface was demonstrated.

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3.0 ELECTRICAL DESIGN

The circuit design effort began with the Phase I contract when the overall block diagram was established for the Pushbroom spectral imager. The preliminary block diagram is shown in Figure 3-1. During Phase II this design was modified to increase the data RAM storage to 14 bits (the maximum possible A-to-D resolution allowed for by the design is 14 bits) with 12 bits for offset RAM, and for providing control and data output through a serial port. The revised block diagram is shown in Figure 2-1. The signal from each detector is amplified by its own integrating transimpedance amplifier (TIA). This TIA has a bank of parallel capacitors and switches in its feedback loop, labeled gain control in the diagram. The gain control is used to compensate for detector-to-detector variations in responsivity by allowing for adjustment of the value of feedback capacitance for each channel. The output of the TIA is filtered by a low pass filter. A source follower is used as a buffer, and the output voltage is converted into a digital word and loaded into the 14 bit data RAM. The 12 bit offset word is subtracted from the 14 bit data word in order to compensate for offset variation from detector-to-detector. The result is compared digitally to a 14 bit threshold word. Threshold excessions are transferred off of the detector array and used in further processing. A provision is provided to output uncompensated data from the focal plane by setting the threshold register to zero, and initializing the offset and gain registers.

3.1 Requirements Analysis

A systems requirements analysis was performed in the Phase I effort. The resulting criteria for the Pushbroom spectral imaging IC is shown in Table 3-1. The details of the circuit design are based on inputs from the systems requirements analysis. The systems requirements that have the biggest impact on the IC design are the operating bandwidth and spectral interval. The higher the operating bandwidth the higher the integrate and dump frequency needs to be in order to insure a flat frequency response. However, as the integration period becomes shorter, smaller feedback capacitors are required in order to obtain the necessary TIA output voltage. The smaller the feedback capacitor becomes, the more difficult the capacitive gain compensation implementation becomes, due to parasitic capacitances. Further complicating the situation is the fact that a design goal requires the IC to operate in a Pushbroom spectral imaging system where the photon flux on any one detector will be significantly less than a normal Pushbroom imager, i.e., the spectral imaging operates at a much narrower spectral bandwidth than does a wide band Pushbroom imager.

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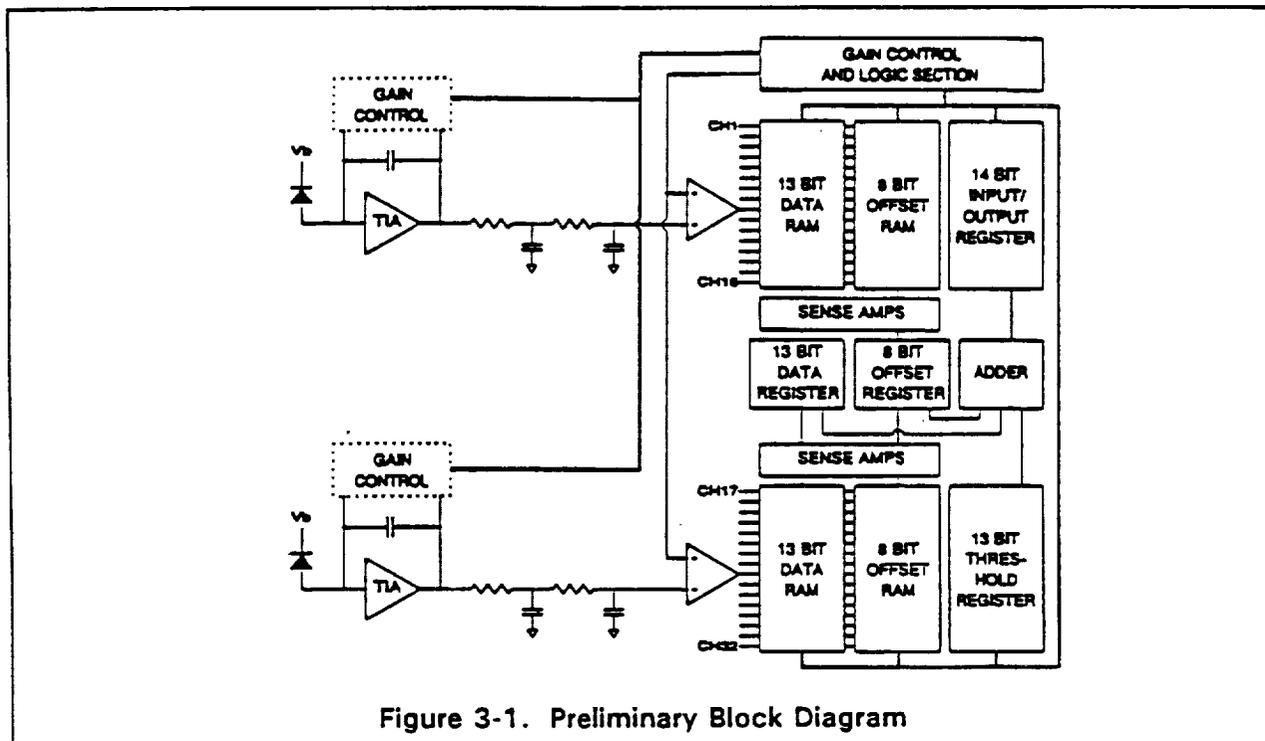


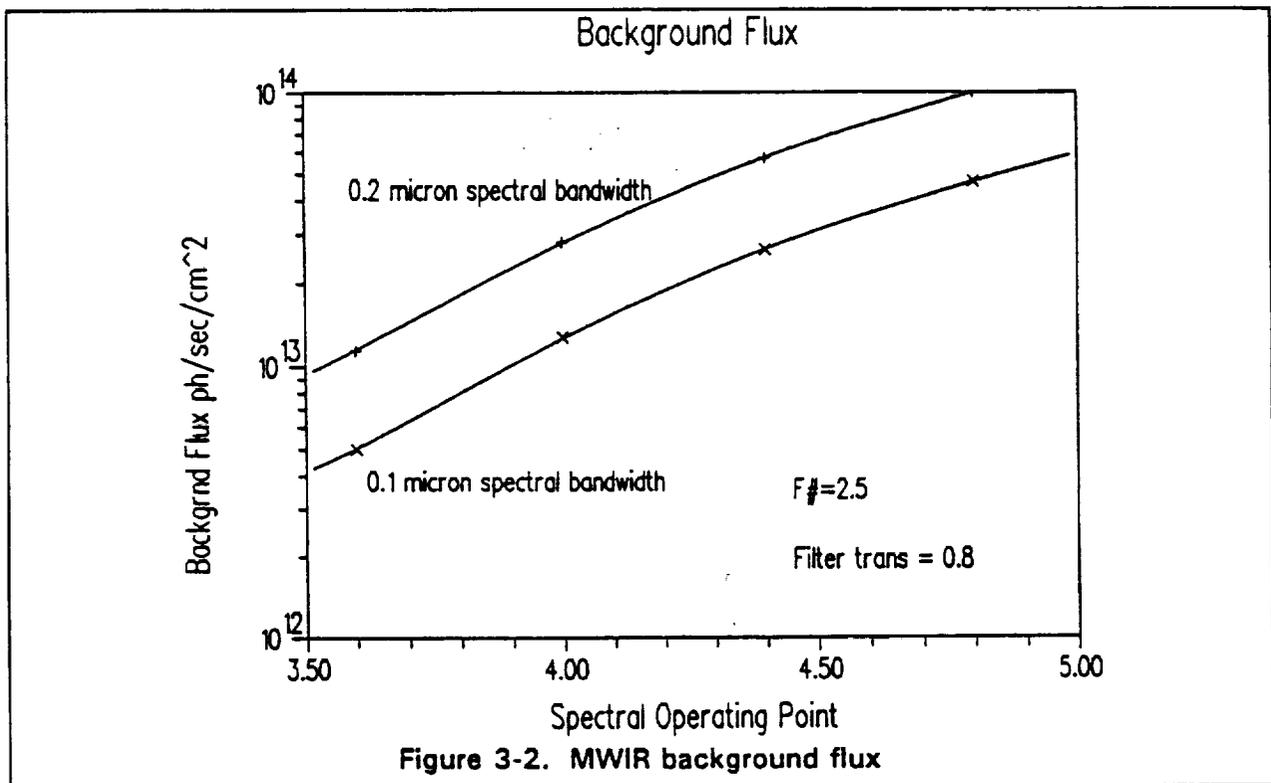
Figure 3-1. Preliminary Block Diagram

	Near-Term Design Criteria	Long-Term System Goal
Detector Dwell Time (Sec)	0.012	0.0025
Filter Pole Position (Hz)	40	200
Sample Rate (Hz)	200	1,000
Detector Options	HgCdTe (PV) InSb (PV) PbSe (PC)	HgCdTe (PC)
Detector Compensation Capabilities		
Nonuniformities (%)	15	25
Offsets (%)	15	25
Calibration Accuracy (%)	< 1.0	0.1
Linearity Deviation (%)	< 1.0	0.1
Dynamic Range		
Before ADC (dB)	72	100
After ADC & Calibration (dB)	60	78 (13 bits)
Module Data Rate (MHz)	6	33

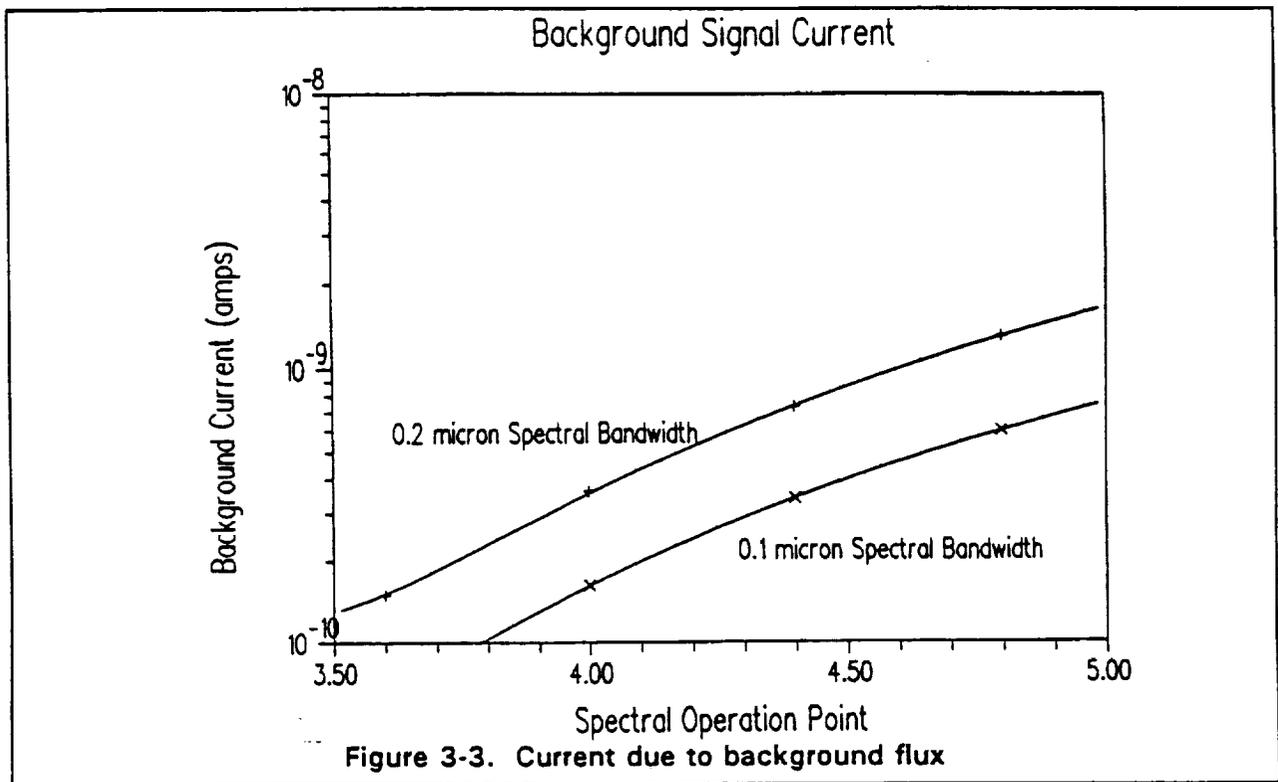
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3.1.1 Transimpedance Calculations

The background flux and photo currents were calculated for both the MWIR and LWIR regions. Figure 3-2 shows the background flux for 0.2 and 0.1 micron spectral bandwidths in the MWIR region. The data assumes that the system is looking at an earth background through an F# 2.5 telescope and that the filter is cooled to the focal plane temperature of 77° Kelvin. Figure 3-3 shows the resulting background current that can be expected. With a nominal feedback capacitance of 2.3 pf and a 0.25 msec integration period used in the IC design, 1 nanoamp of current will result in an output voltage of 0.11 volts. Larger output voltages are possible by decreasing the frame rate below the design goal of 1 KHz. Analysis done in the 8-12 micron region during the Phase I contract indicated that the photocurrent will be 10 times higher, giving a maximum output voltage of 1.1 volts. Additional gain is possible in the ADC portion of the circuit so that even with MWIR detectors full scale performance is still possible.



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3.2 Circuit Descriptions

3.2.1 Operational Modes

The Pushbroom IC calibration procedure is performed using five distinct operational modes of the IC; normal mode, offset initialization, TIA gain initialization, offset calibration, and TIA gain calibration. The IC can operate in more than one mode at a time, i.e. the TIA modes are independent of the offset modes and vice versa. However, in order to correctly perform a gain and offset calibration sequence, the operating sequence must be in a specific order.

The calibration algorithm relies on starting from a known state for proper operation, thus before the first modes are used the Threshold Register must initialize. The Threshold Register is initialized by setting it to zero. This is accomplished by loading in a zero from off the IC along with the appropriate control word through the serial port.

3.2.1.1 Normal Mode

Normal operation of the IC is the default configuration. This mode of operation is characterized by no changes being made to either the gain control settings or the offset registers. While, the IC turns on in a random mode, it is set to the normal mode and both the

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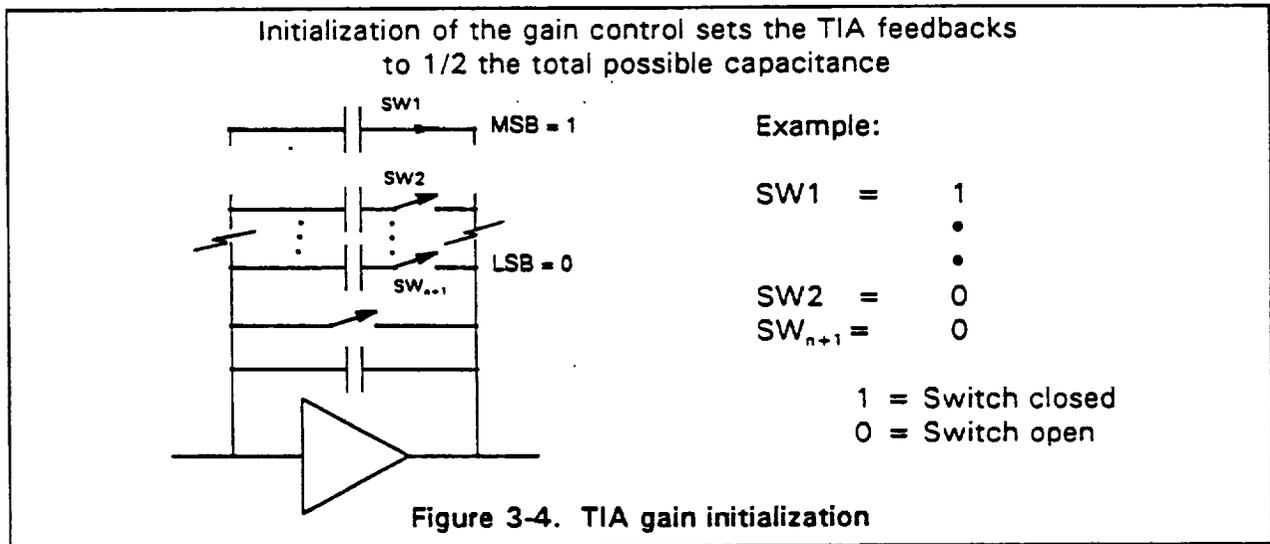
offset and gain initialization modes must be used for the IC to be in a known state. During normal operation, as the data is multiplexed off the IC, the stored offsets for that pixel and the threshold for the focal plane are subtracted from the current value. If the threshold is exceeded, the value is still multiplexed off of the IC, but it is a negative number.

3.2.1.2 Offset Initialization

The offset initialization mode is accomplished by continuously resetting the counter to zero while in the offset calibration mode during an entire frame of data collection. This results in all the ADC Buffer Registers containing the lowest digital word, zero.

3.2.1.3 TIA Gain Initialization

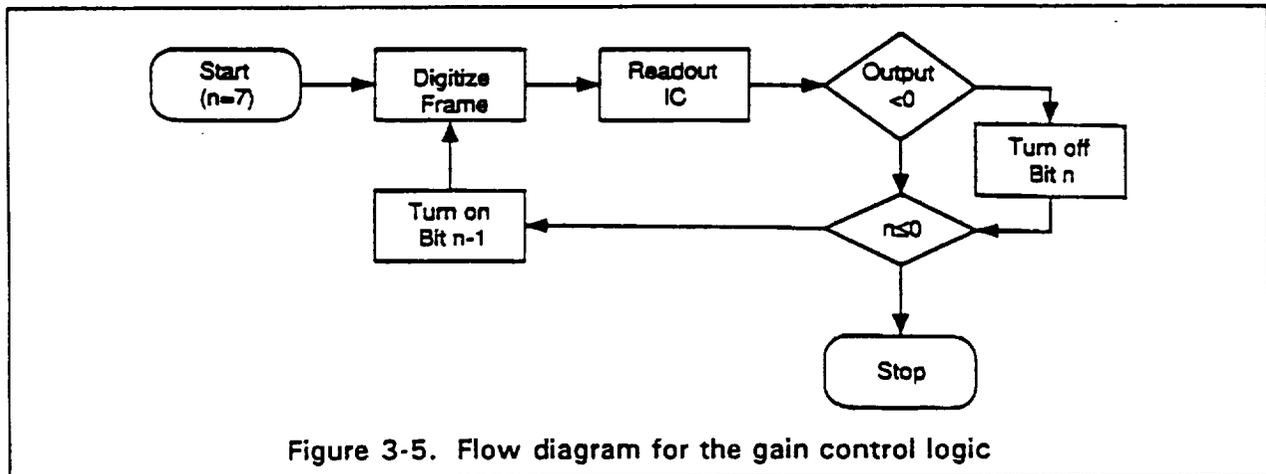
The gain initialization mode sets the gain control switches in each TIA feedback to a 1000 0000 binary word (Figure 3-4). This results in approximately one-half of the variable capacitance of the TIA feedback being connected in parallel to the main integrating capacitor. Not only does this set the gain to a known midrange value, but prepares the TIA for the gain calibration mode.



3.2.1.4 Gain Calibration

The gain calibration mode implements a Successive Approximation Routine (SAR) to set the gain of each TIA. The gain control flow diagram is shown in Figure 3-5. This mode takes at least 8 frames of operation to perform its calculation. During each frame, the current bit of the gain control switch logic of each TIA is set according to whether the output of the IC is positive or negative. Because the gain initialization mode sets the most significant bit to one, the algorithm for the first seven frames are identical.

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The output of the IC will indicate whether the output signal is above or below the threshold loaded into the Threshold Register. The gain control logic will sample the output of the adder and determine the value of the sign bit. If the sign bit is one, a negative output, it indicates that the TIA has too little gain. Thus the gain control logic will open the first switch in the gain control feedback and close the second switch in the gain control feedback (lower capacitance equals more TIA gain). If the output of the adder sign bit is zero, indicating the TIA has too much gain, the gain control logic will close the first switch and close the second switch (more capacitance equals less TIA gain). This loop is continued until all TIAs in the IC have undergone a check on the first level of the SAR for too much or too little gain. During the next frame of data, the second level of the SAR sequence is checked for too much or too little gain. On the eighth frame of gain calibration, the logic allows only the current bit to be set according to the output of the IC and prevents the setting of any other bit to one. After eight frames ($n = 7$ to $n = 0$) of data, each of the gain control switches have been set to the correct value on each TIA.

3.2.2 Calibration Sequence

Typically the IC will be powered up and cycled through the initialization modes. After the initialization, the IC can continue to output raw data, or go through a calibration sequence. The calibration sequence consists of a specific series of operating modes.

3.2.2.1 Offset Calibration

When the IC is in the offset calibration mode, the data from the Data Registers are transferred to the Offset Registers. Being in the normal data mode and the offset calibration mode simultaneously, results in the data from the Buffer Registers being transferred to both

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the Data and Offset Registers. The offset calibration sequence consists of the modes previously discussed. The IC is placed in the normal data mode and a cold shutter or mirror is placed in front of the focal plane. The output of the IC during the conversion mode is the offset voltage. The IC is then commanded into the offset calibration mode which transfers the data from the Data Registers into the Offset Registers. The IC is again placed in the normal data mode. If the cold calibration source is left in front of the focal plane, the output of the IC during this operation should be zero.

3.2.2.2 Gain Calibration

The gain initialization mode is the first mode used in the gain calibration sequence to insure that the gain of the TIAs are at a mid level value. The Threshold Register is loaded with an appropriate value based on the warm calibration source temperature. The value will be determined by the off focal plane signal processor utilizing data previously collected or by using the average output value of the array while looking at the warm calibration source. The average value of the array can be used as the target gain setting because all of the IC gains are at their midpoint value due to the gain initialization step. The IC is then put into the gain calibration mode. While this mode can be accomplished in only 8 frames, more frames will usually be used in each of the SAR settings so that the gain changes can propagate through the low pass filter, hold and data registers.

3.2.2.3 Calibration Convergence

After the gain calibration sequence, the offset calibration will be repeated because changing the gain of the TIAs will also change the offsets. However, after 3 to 4 iterations, both the gain and offsets will converge to within 0.1% of their final value. A more detailed analysis of this algorithm is covered in the Phase I final report.

3.2.3 Analog Circuit

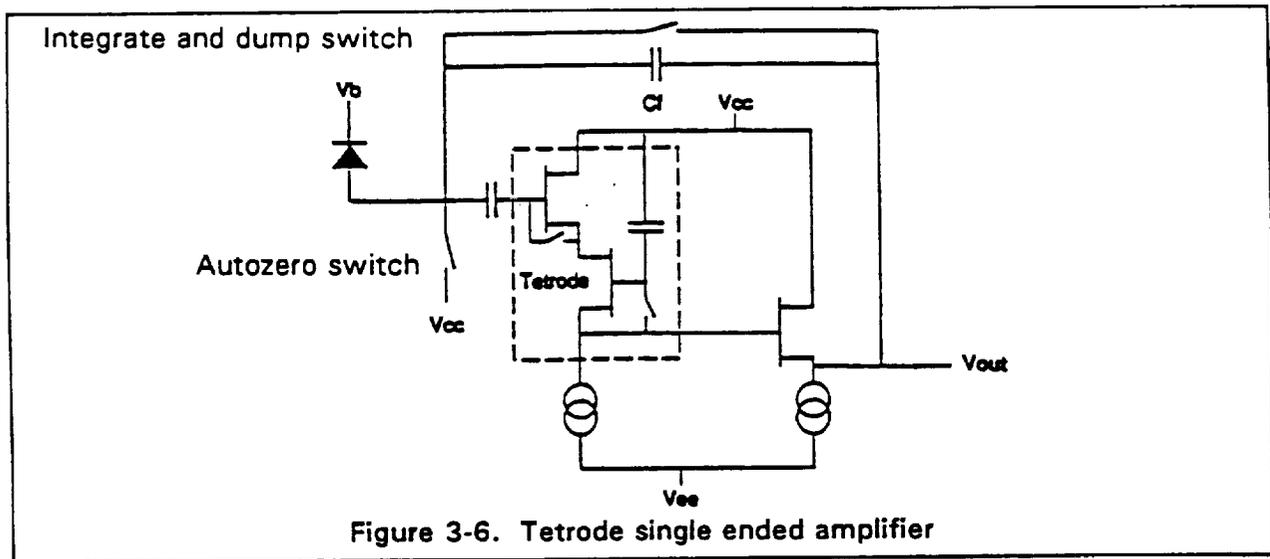
Results from the requirements analysis and calibration study performed in the Phase I effort indicated that the basic circuit designs for the amplifier and digital multiplexer would be adequate to begin detailed design work. The control logic, gain and offset compensation, and analog filter would require completely new design effort.

3.2.3.1 Transimpedance Amplifier

A very important criteria for the amplifier and its feedback network is to have a linear response. Linearity is enhanced by increasing the open loop gain of the amplifier. During the detailed design of the TIA, the open loop gain was increased by 20 dB by changing the

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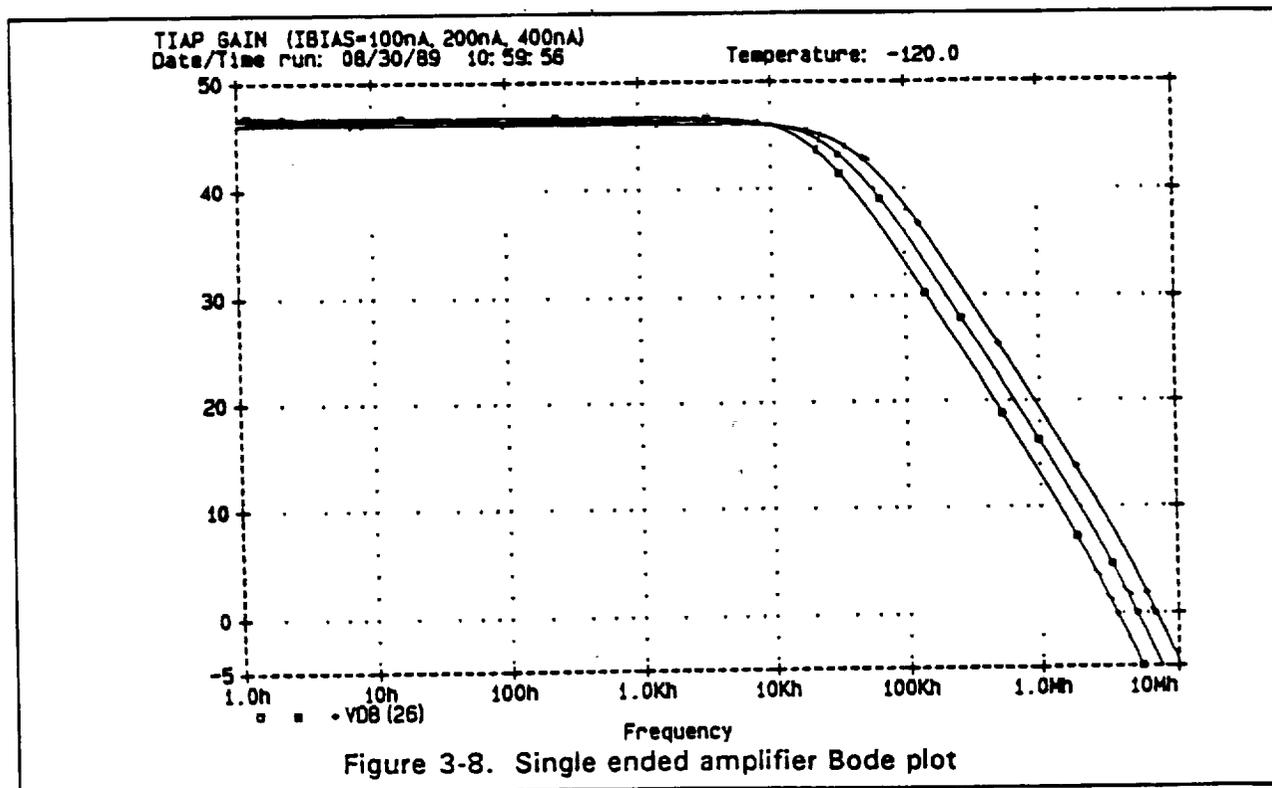
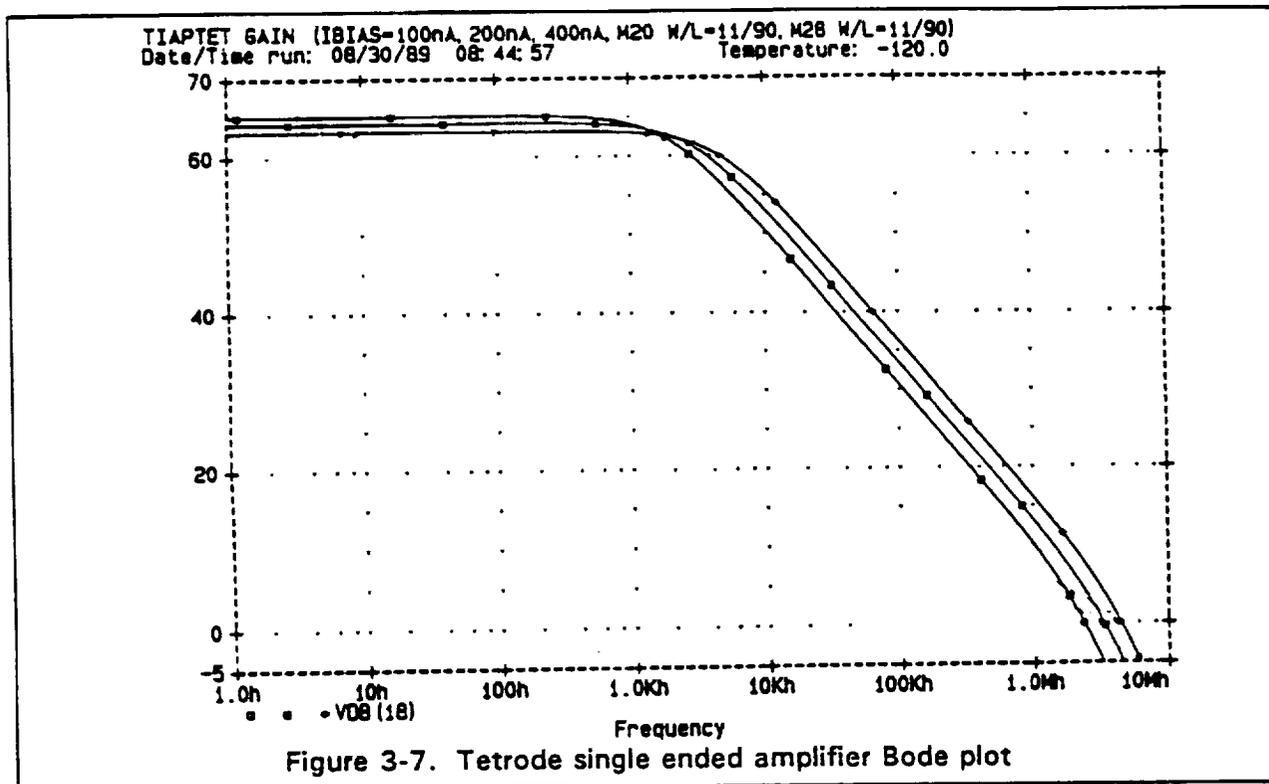
configuration from the normal single ended amplifier to the tetrode configuration shown in Figure 3-6. An existing single ended amplifier configuration in the ISC critical cell inventory was designed for MWIR detectors in a staring application. These requirements dictated a much larger feedback capacitor and lower bandwidth. Because of the smaller background flux and higher frequency response present in this application, the feedback capacitor must be reduced to approximately 2 pf in order to provide an adequate output voltage. Figures 3-7 and 3-8 show the gain versus frequency response of the single ended p-tetrode amplifier and the previous single ended p-amplifier. The open loop gain of the p-tetrode amplifier has increased by approximately 20 dB, while the unity gain frequency point has stayed the same. In both cases, the -3 dB gain frequency is much greater than 500 Hz, the highest signal frequency possible with the maximum per pixel sample rate of 1000 Hz, specified in the design criteria.



At the same time the single ended amplifier was modified into a tetrode configuration, the FET models used in the SPICE analysis were changed to reflect the latest information from MOSIS on their Orbit 2 μm double poly process. The biggest impact the FET model changes had was in the operation of the bias current setting circuit.

An innovative feature of the amplifier shown in Figure 3-6 is that a single transmission gate is used to provide bias. No device matching is required, as would be the case in a current mirror configuration. This allows operation of ISC focal plane IC designs over temperature and radiation extremes because the circuit bias currents and therefore every

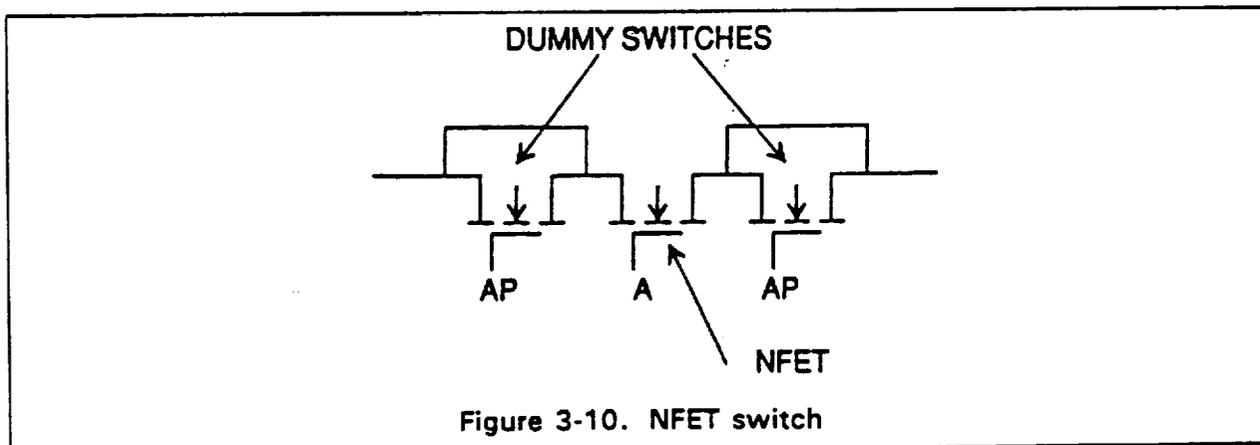
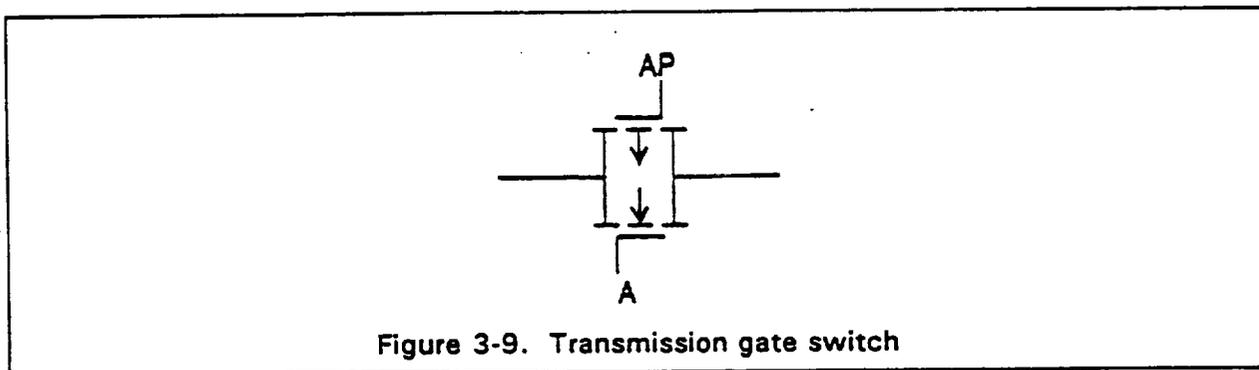
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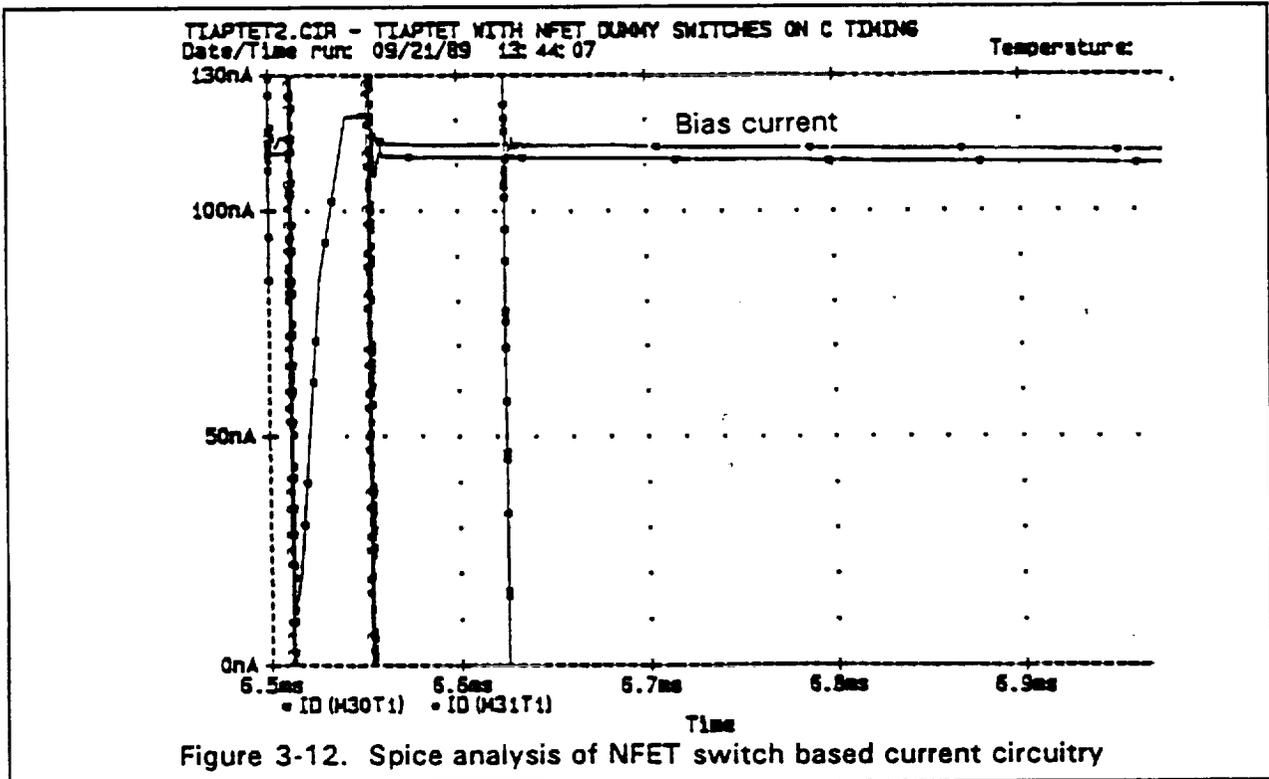
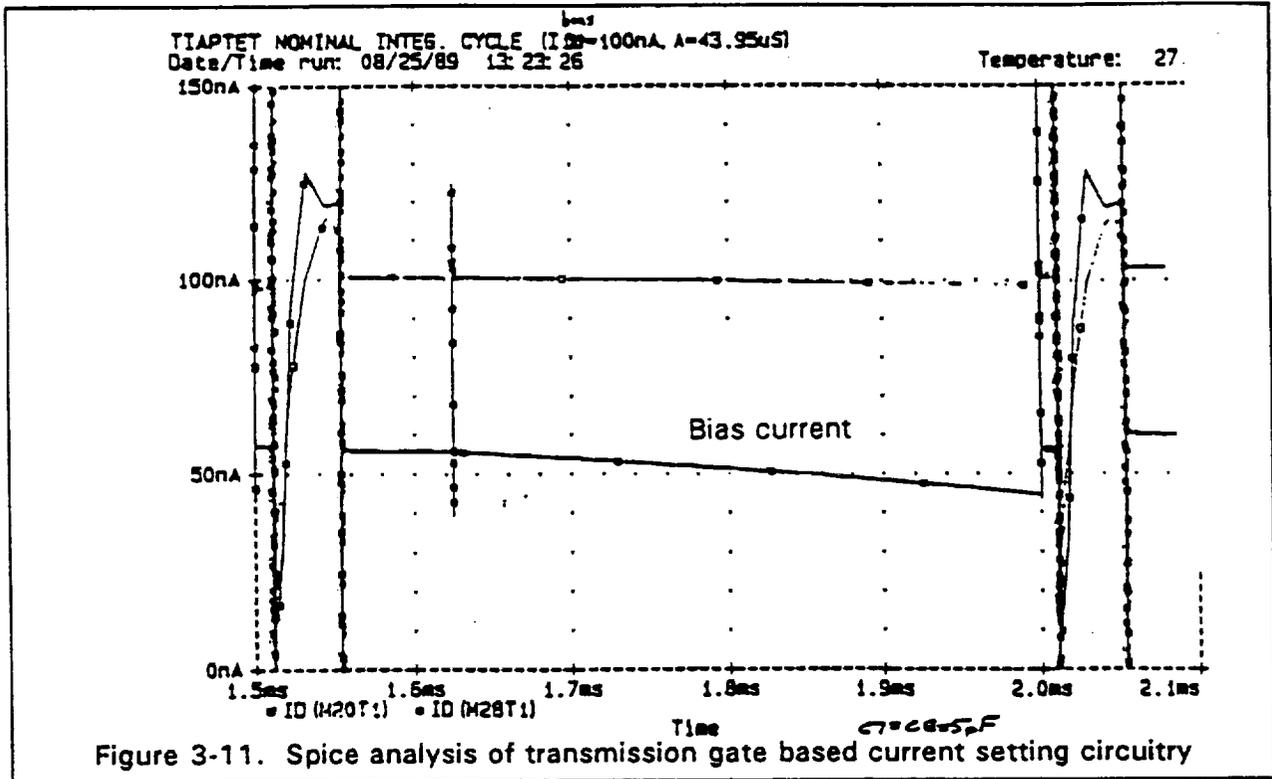
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amplifier in the IC is operated identically. For single ended amplifiers the method involves disconnecting the bias FET's from the circuit, establishing the proper operating point and then reconnecting them to the amplifier. Therefore, threshold shifts over a large range can be tolerated without degrading the proper performance of the circuit. Device level radiation testing indicates that circuits of this type should continue working at total doses on the order of 100 Krads when fabricated using a commercial 2 μ m process and over 1M rad with a rad hard process (HYMOSS[®] Focal Plane Optimization [Contract #F33615-87-C-1448]).

In the past, this was accomplished by using transmission gates shown schematically in Figure 3-9. However, the latest SPICE parameters indicated that less than half the theoretical current was being generated due to charge injection losses (labeled as bias current in Figure 3-11). While the circuit will probably operate at room temperature, such a large deviation from the predicted value is not acceptable, especially for circuits designed to operate at 77° K. When these transmission gates are replaced with NFETs and dummy switches, shown schematically in Figure 3-10, the bias currents are set properly to 120 nanoamps as shown in Figure 3-12.



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The last issue which remained in the amplifier design was the type of adjustable feedback network to include. The approaches considered for adjustable feedback included; varying the duty cycle of the integrate and dump clock, voltage controlled capacitors, and switching in discrete amounts of capacitance in several steps. The later method was chosen as the most appropriate technique for low noise operation.

Because of the choice of a 2.3 pf nominal feedback capacitor value, it was felt that the limitation on performance would be from variations in the parasitic capacitance resulting from the layout geometries. The method used to assure that the gain could be controlled monotonically was to divide the discrete capacitor values into combinations of a single unit capacitor. In this way the parasite capacitance associated with each unit capacitor could be assumed to be equal and factored into the capacitance calculation. In this design that unit capacitor was 0.073 pf. The approach shown in Figure 3-13 created a binary weighted network by using 16, 8, 4, and 2 unit capacitors in parallel for each of 4 legs and 1, 2, 4, and 8 unit capacitors in series for each of the remaining 4 legs. This results in the legs having the following capacitance values; 1.168 pf, 0.584 pf, 0.292 pf, 0.146 pf, 0.073 pf, 0.0365 pf, 0.0183 pf, and 0.0091 pf. The value of capacitance is set by the gain control logic and held by TIA gain control switches.

This results in a feedback capacitance range of $2.3 \text{ pf} \pm 1.16 \text{ pf}$. With the smallest discrete capacitance unit of 0.0091 pf this implies that the circuit can correct variations of up to $\pm 50\%$ to less than 0.5%. This exceeds the design criteria established in Phase I of correcting variations of $\pm 25\%$ to less than 1%. One of the goals in the testing of the circuit was to predict the likely limit of gain correction using this technique.

3.2.3.2 Low pass Filter

The low pass filter follows the transimpedance amplifier in the signal processing chain. The filter designed for this circuit is of the switched capacitor type with a modification of the conventional clocking technique. The filter has two low pass poles which are clocked independently. The first pole is set by clocking it synchronously with the TIA integrate and dump cycle. This allows the first pole clocking to act as a sample and hold on the amplifier output. The second pole is then set independently by a separate clock which is optimized to the sample rate of the analog to digital converter.

Figure 3-14 shows the two (2) pole passive filter schematic as implemented on the IC. The filter and source follower are located on the bottom half of the diagram and the bias set circuit is located on the top half of the diagram. Figure 3-15 shows the transient analysis results for the filter with the first and second pole set at 320 Hz. With the second pole set to 40 Hz and maintaining the first pole at 320 Hz, the 6 dB attenuation frequency is now moved to 40 Hz, Figure 3-16.

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Binary weighted feedback capacitors made up of numerous combinations of unit capacitors to assure monotonicity.

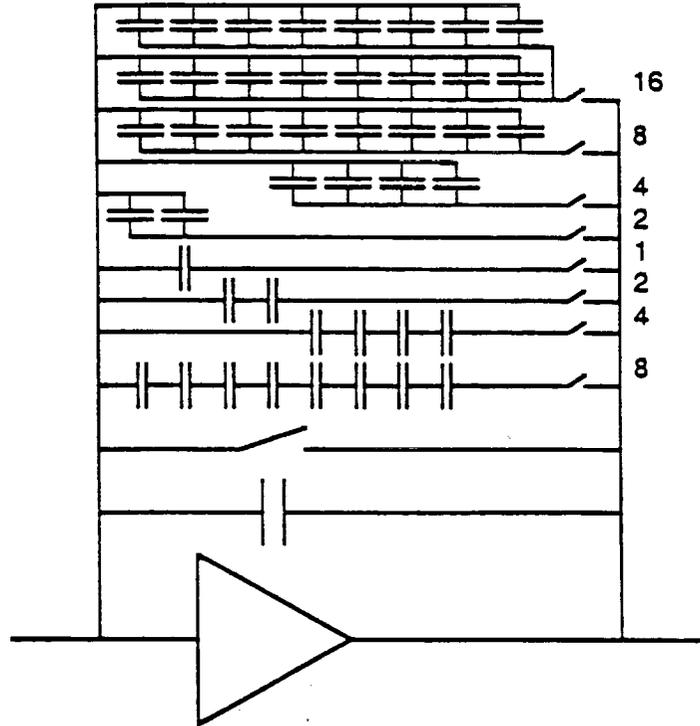


Figure 3-13. Binary weighted feedback capacitors

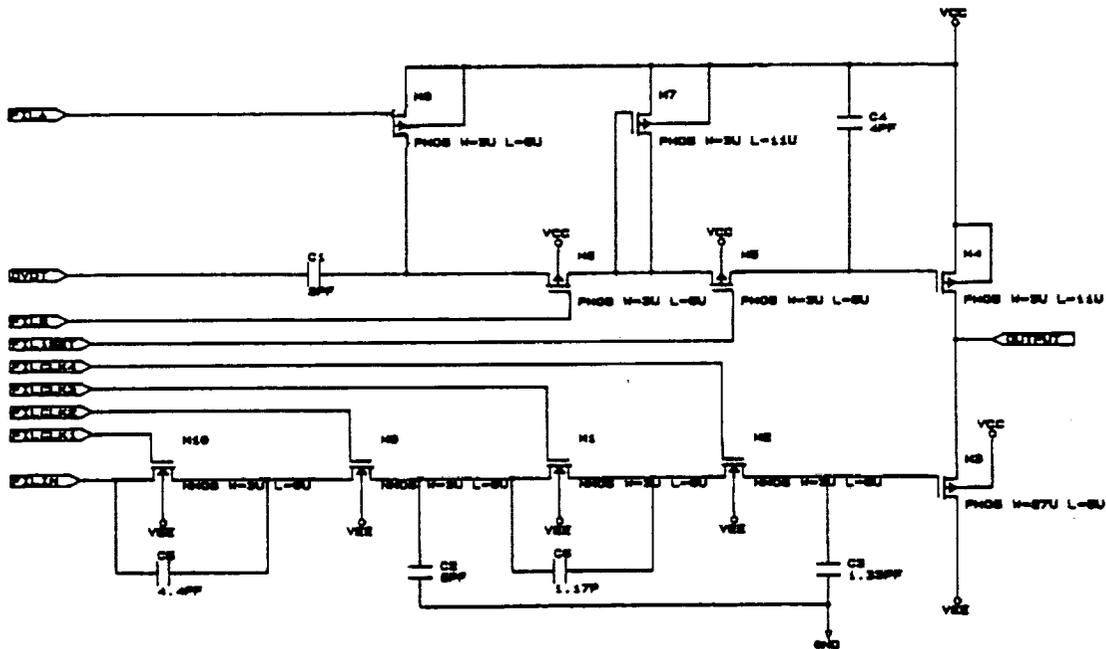
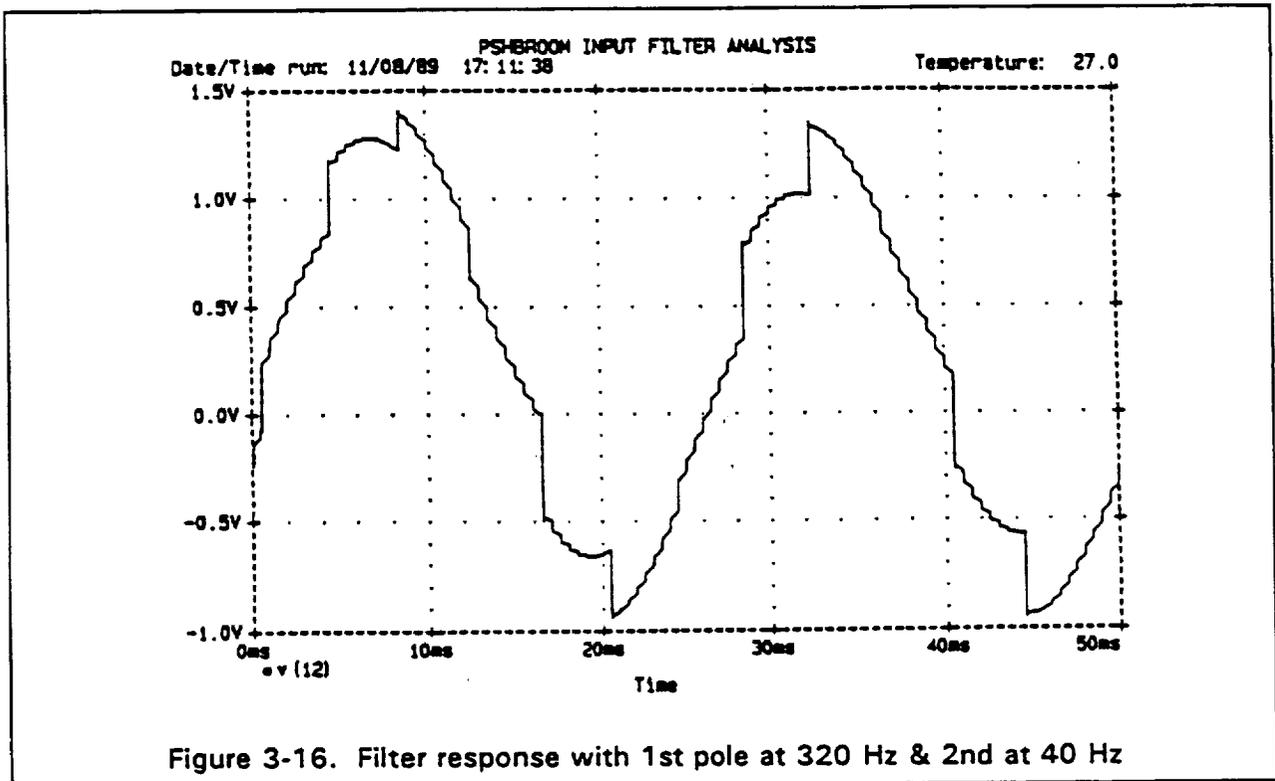
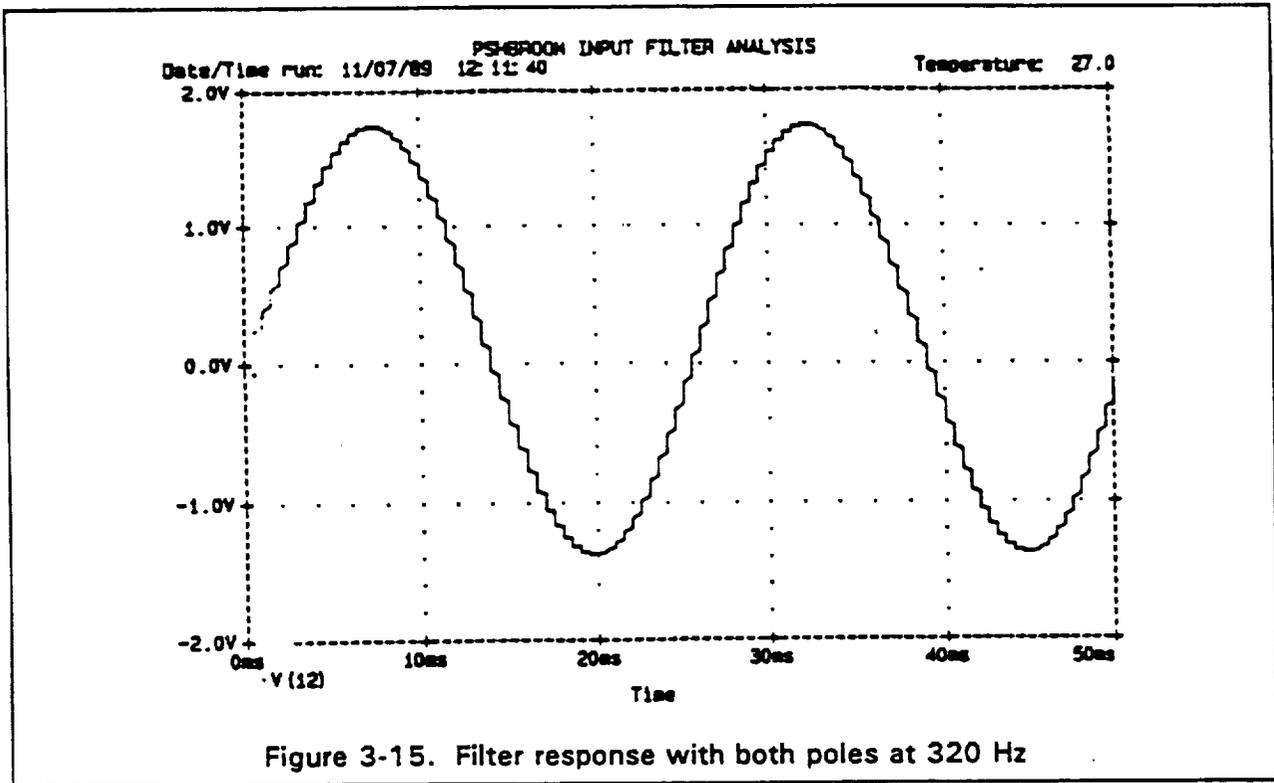


Figure 3-14. Lowpass filter schematic

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3.2.3.3 Comparator

The final analog critical cell is the ADC comparator shown in Figure 3-17. The single slope ADC uses an autozero dynamic comparator. The dynamic comparator has been specifically optimized for on-focal-plane applications.

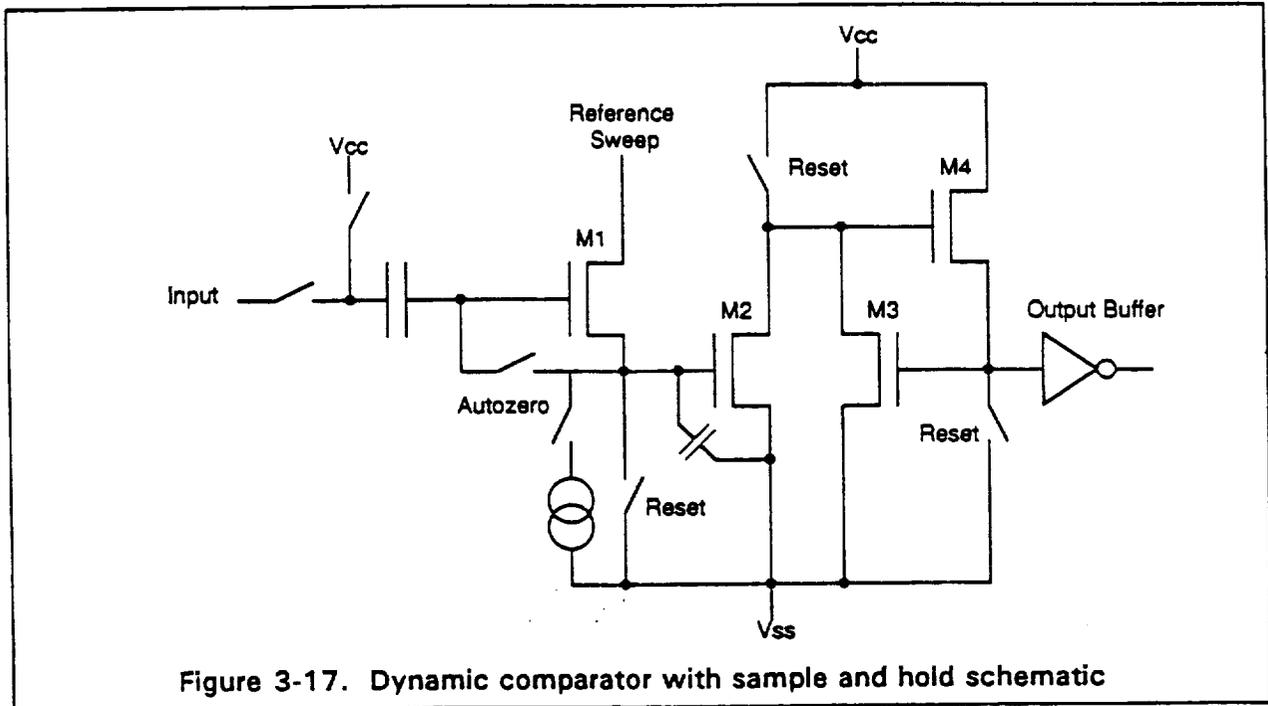


Figure 3-17. Dynamic comparator with sample and hold schematic

A simplified timing diagram of the comparator operation is shown in Figure 3-18. The auto-zero circuit works to create an input voltage that is less than the threshold voltage of the M1 FET by a voltage equal to the difference between Vcc and the sample voltage. After the autozeroing has taken place, the reference sweep is taken to its lowest value and the circuit reset. The reference sweep must be at its lowest value to insure that the comparator will not immediately trigger after the reset pulse. The reference sweep then starts, and when it becomes greater than the input to the comparator by the threshold voltage of M1, M1 starts conducting and charges up the gate-source capacitance of M2. M2 then turns on which causes the voltage at the gate of M4 to decrease thereby turning M4 on. M3 provides positive feedback to M4 thereby reducing the transition time. It should be noted, that during this conversion there is no DC current path established in the comparator, only the charging and discharging of the gate-source capacitance of the FETs in the circuit. The only time a DC current is established, is during the autozeroing of the circuit. A SPICE output showing

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current draw as a function of time for one cycle is illustrated in Figure 3-19. The DC current during the autozero operation corresponds to two (2) microwatts per channel. However, the autozero sequence uses only 10% of the conversion cycle, thus resulting in an average power dissipation of only 0.2 microwatts per channel for the comparators.

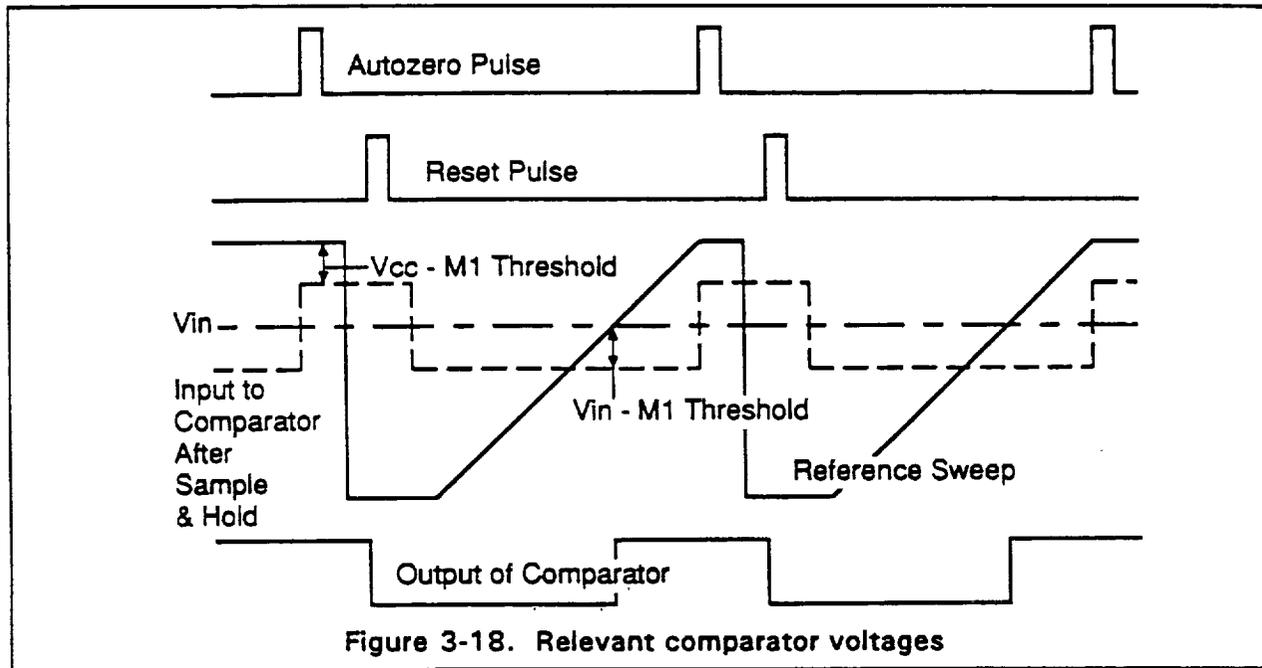


Figure 3-18. Relevant comparator voltages

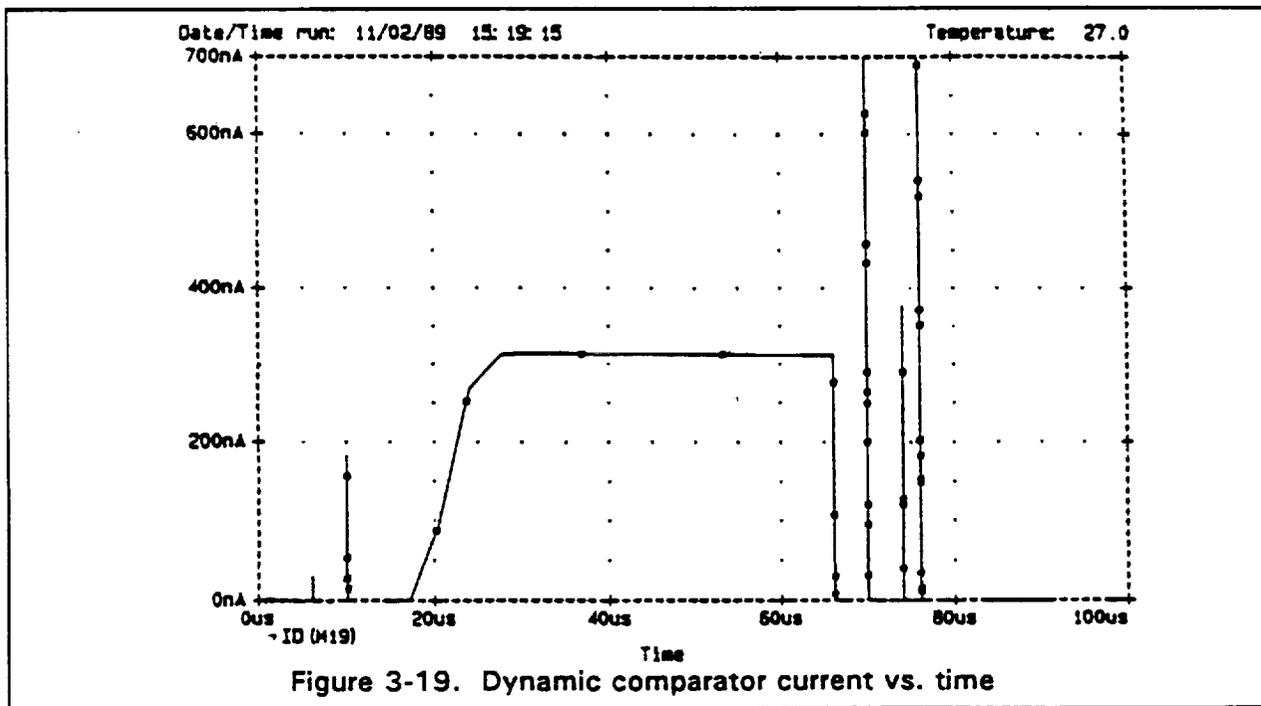
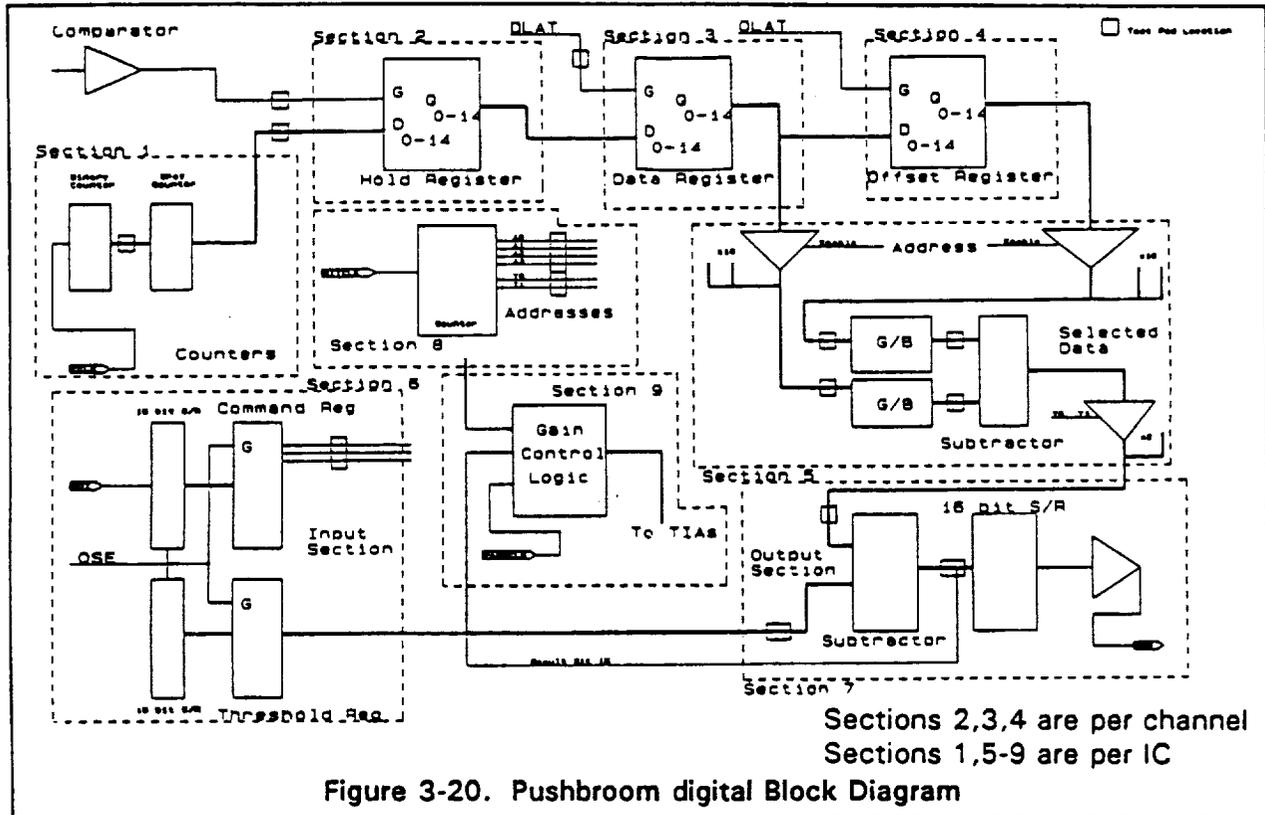


Figure 3-19. Dynamic comparator current vs. time

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3.2.4 Digital Circuit

The block diagram in Figure 3-20 illustrates the digital portions of the IC. The major blocks in the digital section are the data registers, adder, parallel to serial conversion, and digital counter. The data registers (buffer, data, offset and threshold registers) are all of similar design. In addition the digital circuitry also includes the digital mode logic, gray to binary and binary to gray converters.



3.2.4.1 Analog-to-Digital Converter

The analog-to-digital (ADC) converter bridges both the analog and digital design. The comparator, which is the major component of the ADC is described in the previous analog section. The operation of the ADC is presented in this section.

A block diagram of a single slope ADC and timing diagram is shown in Figure 3-21. The major component of this type of ADC is the comparator at which the unknown analog voltage is compared to an analog reference voltage. A ramp voltage is fed into one terminal of the comparator. When this ramp voltage equals the unknown voltage the comparator output switches from a plus to a minus level. The ramp voltage is generated by an integrating

amplifier. The conversion cycle begins when the integrator is reset. A continuously running clock signal is now allowed to be totaled in a counter. When the ramp voltage equals the unknown voltage, the comparator switches state and disables the counting circuit. The number of counts registered is proportional to the time between the reset and the comparator switching. If the ramp voltage is linear, the number of counts registered is proportional to the unknown voltage. The resolution of the ADC can be adjusted to cover a narrower or wider analog input range by varying the magnitude of the reference sweep.

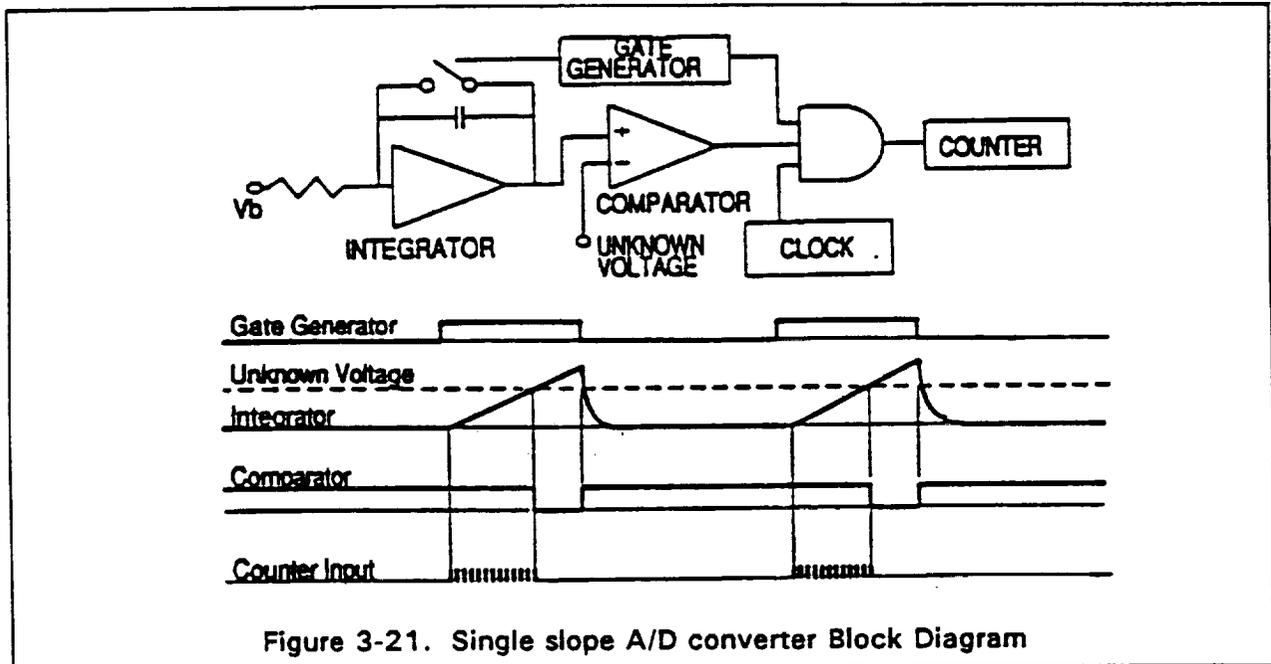


Figure 3-21. Single slope A/D converter Block Diagram

ISC has altered the traditional single slope ADC, as shown in Figure 3-22, for use with a focal plane array where many channels need to be converted per IC. This approach differs from the traditional single slope converter in one major respect. The counter is replaced by memory. The switching of the comparator causes the memory to be disabled. The counter feeds digital words into the memory array (one for every channel). At the moment the comparator switches, the memory is disabled, thus capturing that count. If the counter is synchronized to the ramp voltage, the same proportionality between the captured count value and the unknown voltage will occur as in the traditional single slope ADC. Synchronization is possible by triggering the start of the ramp with the same pulse that starts the counter. The ramp voltage is generated off of the IC. One comparator is incorporated into each detector unit cell. This allows the comparators to operate with a low duty cycle, hence, reduced power dissipation.

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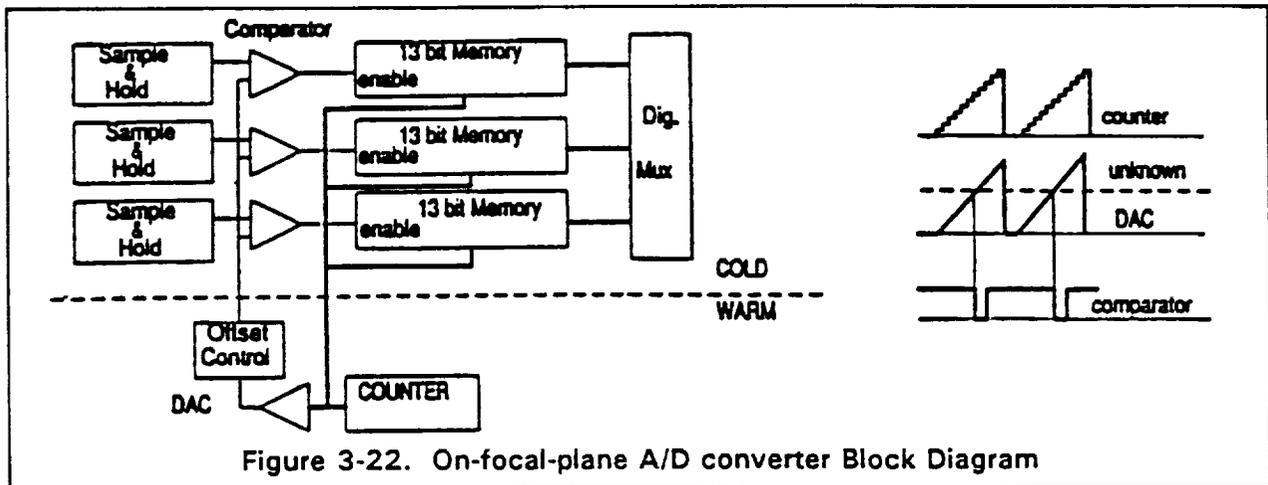


Figure 3-22. On-focal-plane A/D converter Block Diagram

Because of the type of detectors the amplifier was designed for, larger photon flux results in a more negative output. This results in the comparator switching sooner, not later, for larger signals. By causing the counter to count backwards, larger values will result from the higher photon flux.

3.2.4.2 Output Multiplexer and Offset Correction

Offset correction and thresholding occur during the multiplexing of the data off the focal plane. The operation starts at the end of the previous frame when the data register is commanded to accept new data from the buffer registers. During offset calibration, the offset registers are simultaneously commanded to accept new data from the data registers and thus the buffer registers. If the focal plane is looking at a cold reference source, these values represent the offsets generated by the detectors and focal plane electronics.

The addressing for the multiplexers is generated by a counter driven by the serial output bit clock. Since the IC has 32 channels and the output is a 16 bit two's complement number, 512 counts are required to multiplex the data off the IC. As each channel is addressed, an adder is presented with the actual data from the data register, and the two's complement from the offset register. This results in the stored offset being subtracted from the previous frame's data. The output of this adder is then connected to another adder that has as its other input the two's complement of the threshold word. The output after threshold subtraction is then loaded into a serial shift register and clocked off the focal plane.

Two types of offsets can be removed on focal plane; a global offset and a detector to detector offset. The global offset affects all detectors equally. This type of offset would be used if a very large DC signal is present in all the data such as due to a large background flux.

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The global offset is removed by loading the value of the offset into the Threshold Register and subtracting it from all of the data. Global offsets up to full scale can be removed in this manner. Channel to channel offsets are expected to be very much less than full scale. Channel to channel offsets can be corrected to 12 bits (the offset register word length). The least significant bit of offset correction was assumed to be random at the time of the design, because the least significant bit of the raw data is only accurate to $\pm 1/2$ bit. Given the error source in the raw data, the LSB of the offset register was permanently tied to zero. This still preserves the $\pm 1/2$ bit uncertainty in the offset correction algorithm and the capability to offset correct with a dynamic range of 12 bits.

3.2.4.3 Control Logic

The control section of the digital circuitry is the most complex portion of the IC. It must accept a serial data input, determine the proper mode of operation, and monitor the output of the IC. The schematic for the control section is shown in Figure 3-23. For a detailed description of the signals shown on the schematic refer to the interface control document attached as Appendix A.

Offset control, the top of Figure 3-23, is the easiest of the two to implement since it does not involve a feedback loop. The control simply has to determine from bit 9 (OFFLEN) of the input control word whether or not to enable the offset registers (OLAT) at the same time the data registers (DLAT) are enabled. FRMSYNC is used to insure that it occurs at the end of the frame.

Offset register initialization is performed by insuring that the buffer registers all contain zero when the offset registers are enabled. This mode is entered by setting bit three (3) (HLDRAMP) to one (1). This causes the counter to be held in reset continuously during the frame.

The gain control logic is more complicated (bottom Figure 3-23) because it involves feeding back the digital output of the IC to the analog transimpedance amplifier. Four signals control the gain initialization and calibration process: ABNORMAL, to enable the changing of gain capacitors; PASSCLK, to set the control to perform gain calibration; TIAINIT, to set the control to perform gain initialization, and RSLT, the sign bit from the current output word. The first three of the signals originate from off the focal plane and are shifted in through the serial port. All timing is derived from FRMSYNC and BITCLK to insure that the operation synchronizes the addressing for both the TIA gain capacitors and the output multiplexer.

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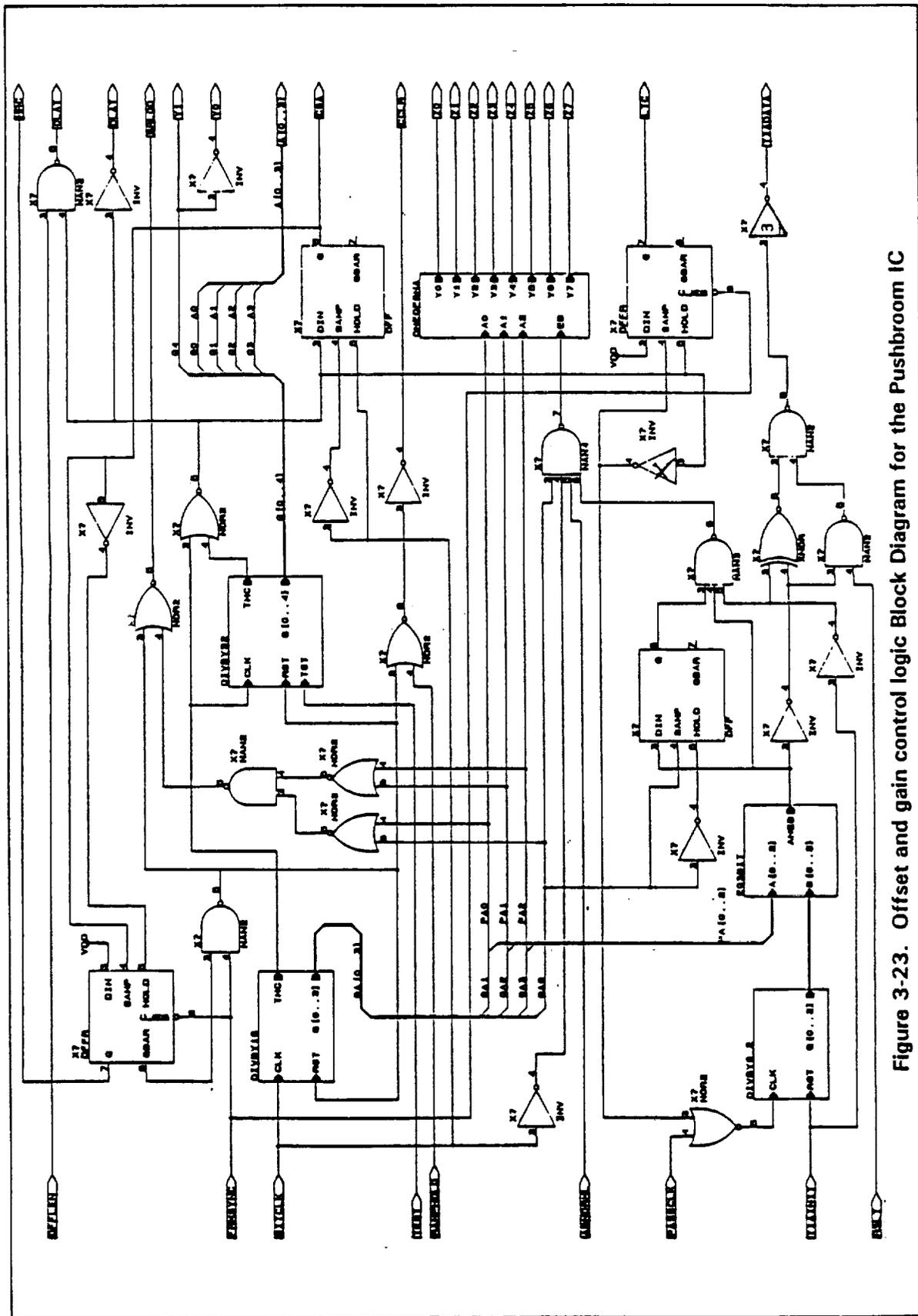


Figure 3-23. Offset and gain control logic Block Diagram for the Pushroom IC

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Gain initialization performs two functions. It sets the gain of each TIA to its midrange value and it resets the counter that addresses the individual gain capacitor latches. The gain initialization process occurs in one frame by using eight (8) of the clock periods, out of the 16 that BITCLK uses to readout the data, to address each of the gain capacitor latches in the current TIA. TIADATA is equal to one for the first clock and then zero for the next seven (7).

Gain calibration is similar to gain initialization, but with some additional features. The first change is that the RSLT line is now used to control the setting of the gain capacitor latches. The other is that the PASSCLK signal is combined with FRMSYNC to clock a counter that determines which of the gain capacitor latches will be enabled to accept a new value during the current frame. Thus while all gain capacitor latches are addressed during each frame, as during gain initialization, the PASSCLK counter determines which ones will be enabled.

The rest of the gain calibration logic uses the circuitry described above to implement the SAR. During each frame in which PASSCLK and ABNORMAL are high, the logic will set the currently addressed bit according to the value of RSLT and then set the next bit to one.

3.2.5 Power Dissipation

As stated above, the ADC comparator is predicted to consume 0.2 microwatts of average power per channel. The power of the TIA and low pass filter are designed to be 1.2 and 0.8 microwatts per channel respectively. This results in a total power dissipation of 2.2 microwatts per channel for the analog portion of the circuitry.

Simulations have shown that for digital logic, switching current per node is 1 microamp per MHz with 5 volt power supplies. The majority of the power dissipation is expected to occur in the counters and registers of the IC. For the counters (and the binary to gray converter) approximately 4 nodes on average will change states during each clock period. Because 16 detectors share the same counter and binary to gray converter, this works out to 0.25 nodes per MHz per channel. Nodes within the ADC Buffer Registers will also change state with the counter, until the comparator turns the register off. For an average scene with values equal to one half of full scale, 0.5 nodes will change state per clock period. This implies that for every clock period, 0.75 nodes will change state on average. Therefore the power dissipation of the digital section is predicted to be 0.75 microamps per MHz per channel times 5 volts or 3.75 microwatts per MHz per detector.

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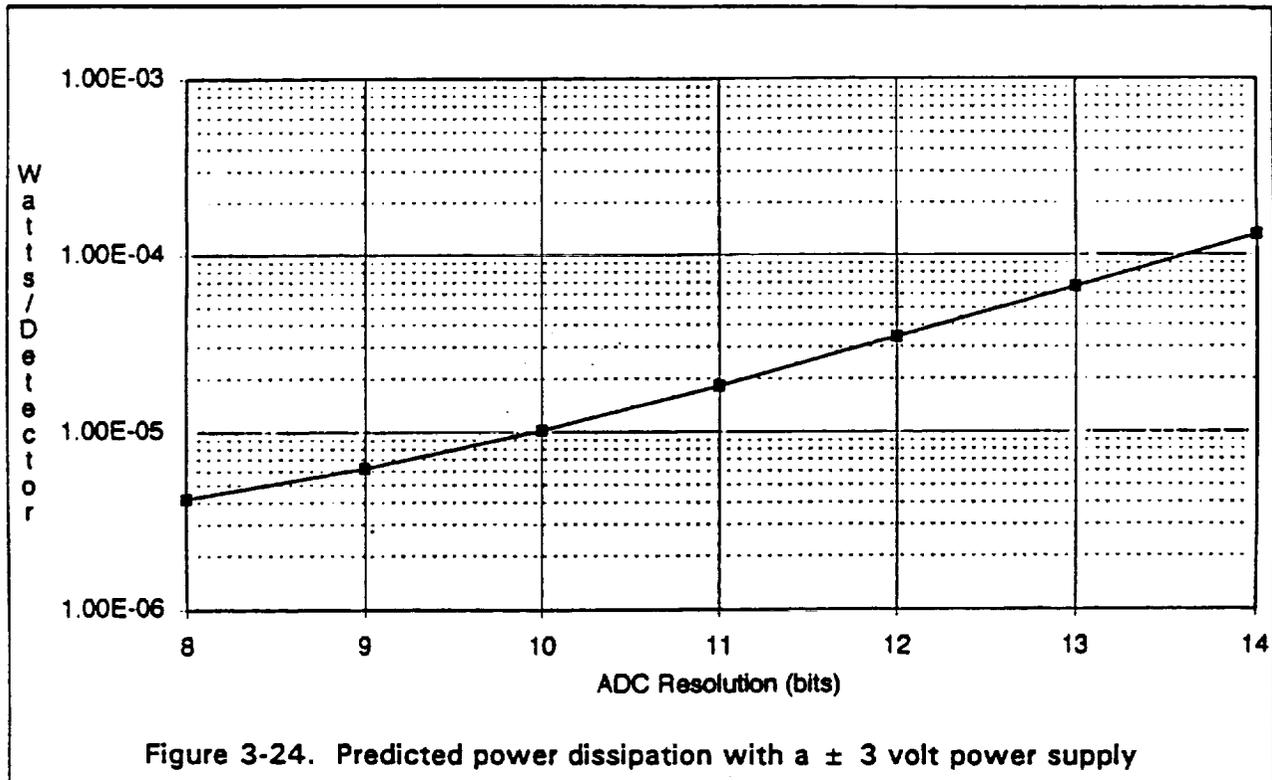
The clock frequency is derived from the resolution and the frame rate of the focal plane by the following equation:

$$\text{Master Clock} = 2^n * F$$

Where: n = the resolution of the conversion in bits

F = the frame rate of the focal plane

Figure 3-24 shows this relationship for a ± 3 volt power supply where frame rate is 1000 Hz.



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4.0 PHYSICAL DESIGN

4.1 IC Layout Criteria

The IC was fabricated by the MOSIS (Metal-Oxide-Silicon Implementation System) service. This service is a very cost effective means of prototyping ICs. Many IC design houses submit data base tapes to MOSIS where they are combined and fabricated together on one wafer. Each designer then receives a small quantity of his own parts diced from the combined wafer. It was determined that the MOSIS 2 micron, double poly, P-well process be selected for fabrication. This is a frequently scheduled MOSIS fabrication and would allow for easy conversion to a radiation hardened process. The die size was also fixed by the decision to go through the MOSIS service. The largest IC possible is 9500 x 9000 microns. ISC elected to fit a 32 channel IC into this space. These geometries would show feasibility of designing a similar circuit with 128 channels in the 0.5 x 0.5 inch format that ISC uses in its HYMOSS Z-technology focal plane modules and is compatible with present tooling.

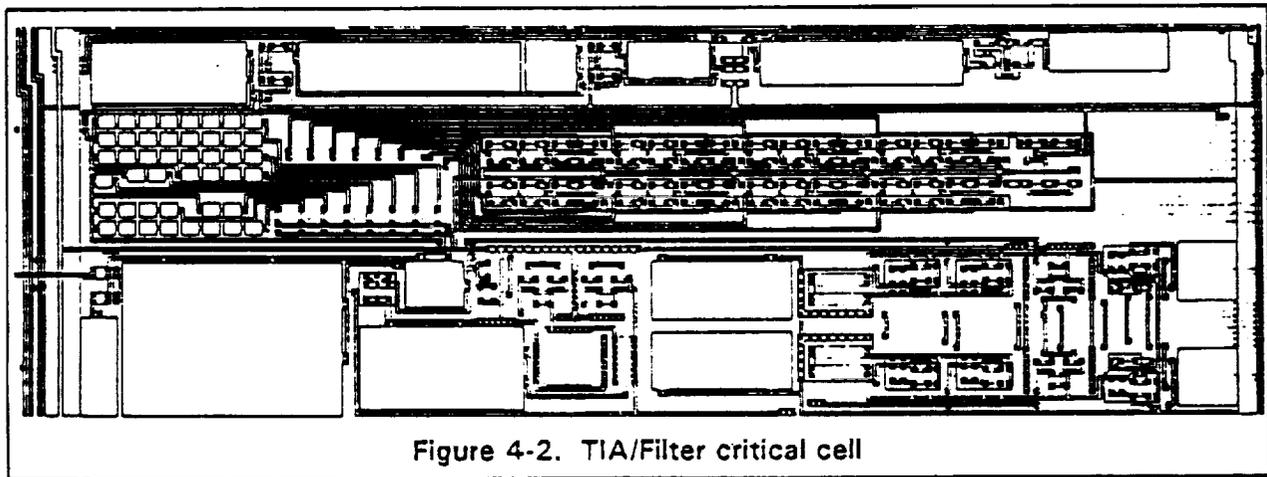
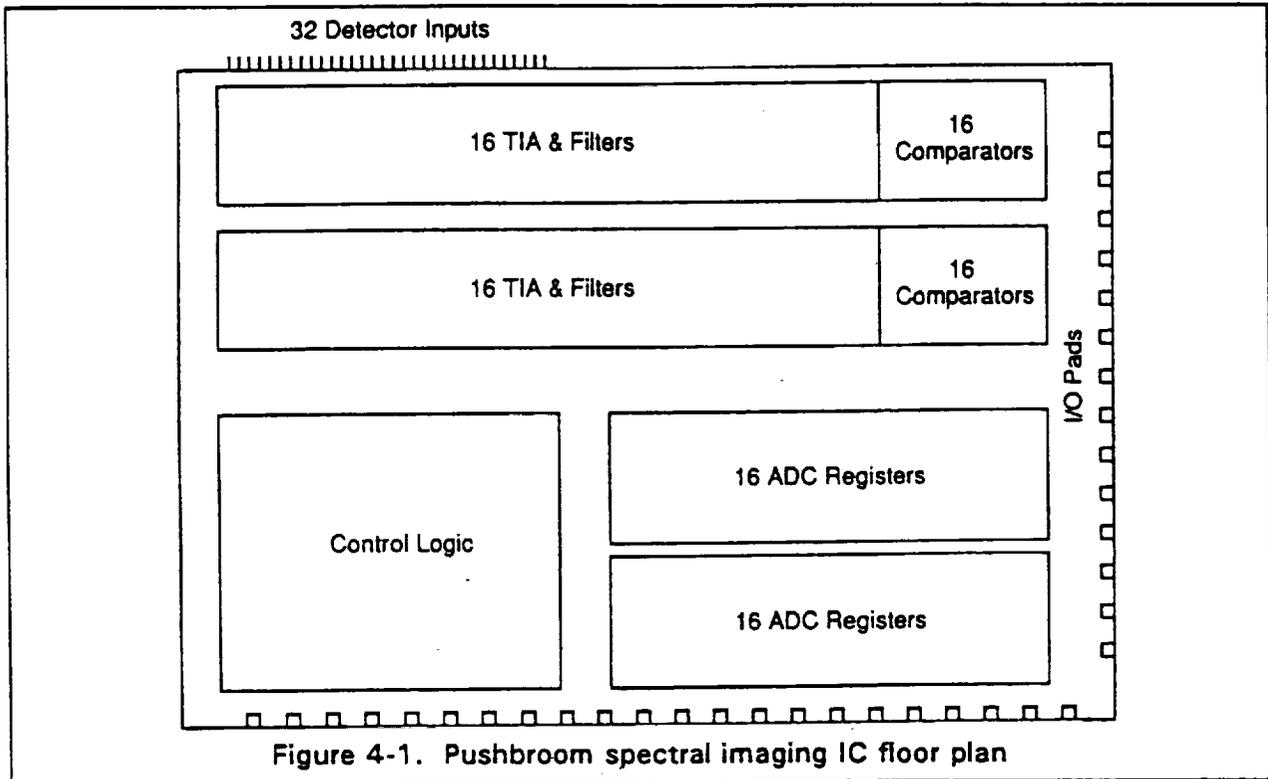
4.2 IC Layout Floor Plan

The Pushbroom Spectral Imaging IC consists of the following functional blocks: TIAs and low pass filters, ADC comparators, ADC registers, and the control logic. The layout of the major functional blocks on the IC is shown in Figure 4-1. Each of the major blocks consists of several smaller critical cells which in themselves can consist of even more critical cells. This is known as hierarchical layout. The TIA and low pass filter functional blocks consists of 16 TIAs, low pass filters and associated interconnect, of which the TIA consists of a single ended P-tetrode amplifier and feedback network. The comparator functional block consists of the 16 ADC comparator critical cells and the associated interconnect. The ADC register functional block consists of 16 ADC registers, counter, adder, gray to binary converter, and binary to gray converter. Each of the 16 ADC registers consists of two 14 bit Buffer and Data Registers, and one 12 bit Offset Register. The control logic for the IC consumes the rest of the open space on the IC, except for the overhead and I/O.

4.3 IC Layout Details

The layout of the critical cells are shown in this section. The TIA and low pass filter have been designed as one critical cell. This cell is then repeated 16 times for each functional block. The layout of the TIA/filter critical cell is shown in Figure 4-2. The filter is located on the upper portion of the figure and the TIA on the lower. The gain compensation capacitors and gain control switches are arranged in the center of the critical cell.

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Shown on the same scale in Figure 4-3 is the comparator. The largest features in the comparator is the 13 pf input autozero capacitor and the 3 pf bias set capacitor.

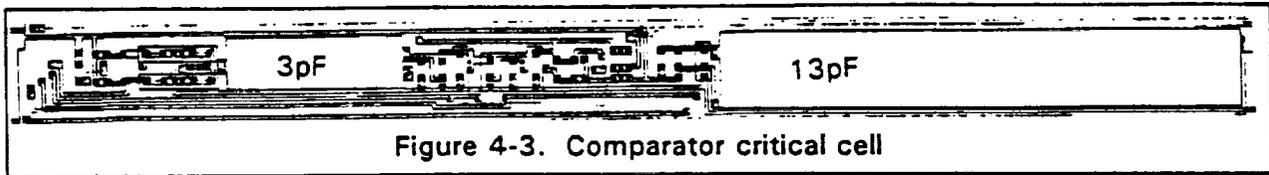


Figure 4-3. Comparator critical cell

The main circuit cell for the digital section of the IC consists of 16 channels of the ADC registers. A floor plan representing the layout is shown in Figure 4-4. The ADC registers consist of the Buffer, Data, and Offset registers. The number of bits in each register was taken from the proposed specification and the physical layout limits. The output of the IC was chosen to be a 16 bit serial word to interface with standard data acquisition hardware. It was decided to increase the size of the ADC registers up to the layout limits of the IC. Sixteen bits of data was too large for an efficient layout, but 14 bits, one more than the proposed specification goal of 13 bits, was possible for the Buffer and Data Registers. The Offset Registers were limited to 12 bits (with the LSB always equal to zero) because of other circuit needs. The three registers were interleaved in the layout so that the corresponding bit positions of each register were adjacent. This minimizes the interconnect necessary to transfer data from the Buffer to the Data Registers and from the Data to the Offset Registers. Figure 4-5 shows the symbolic layout for one bit of the three registers. Each bit is comprised of a latch. The channel read select switch is comprised of two inverting tri-state buffers.

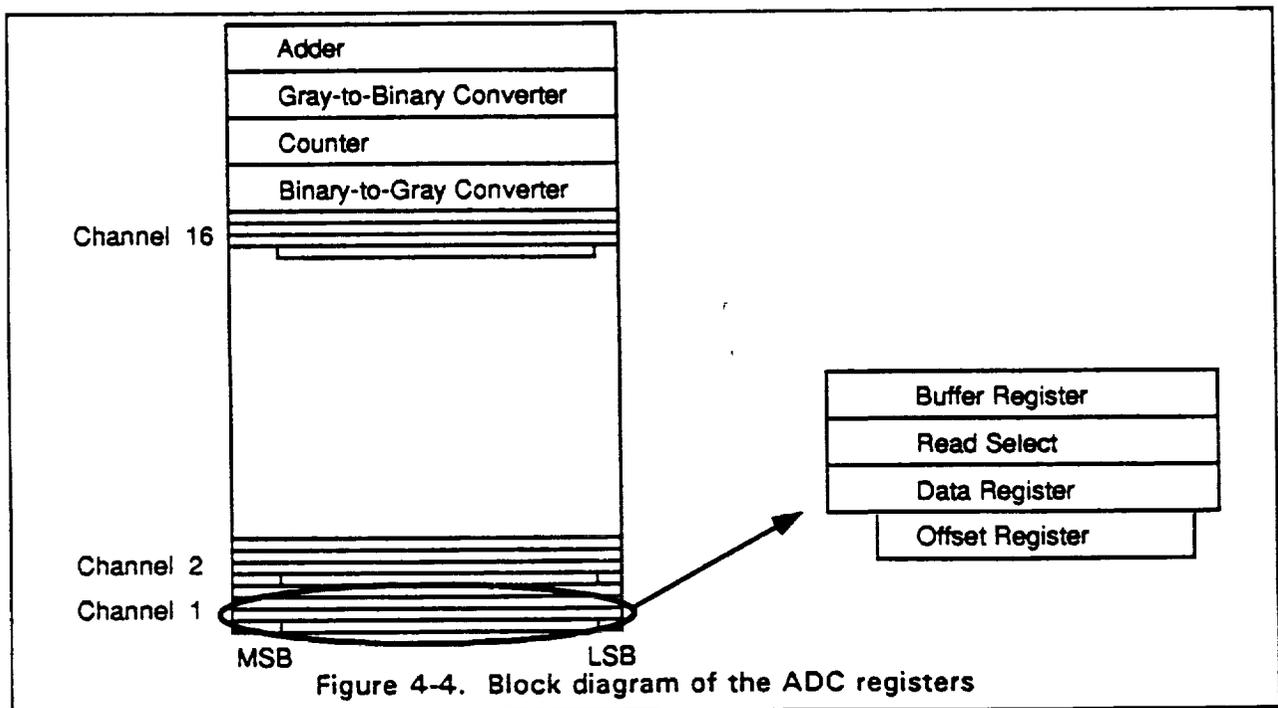


Figure 4-4. Block diagram of the ADC registers

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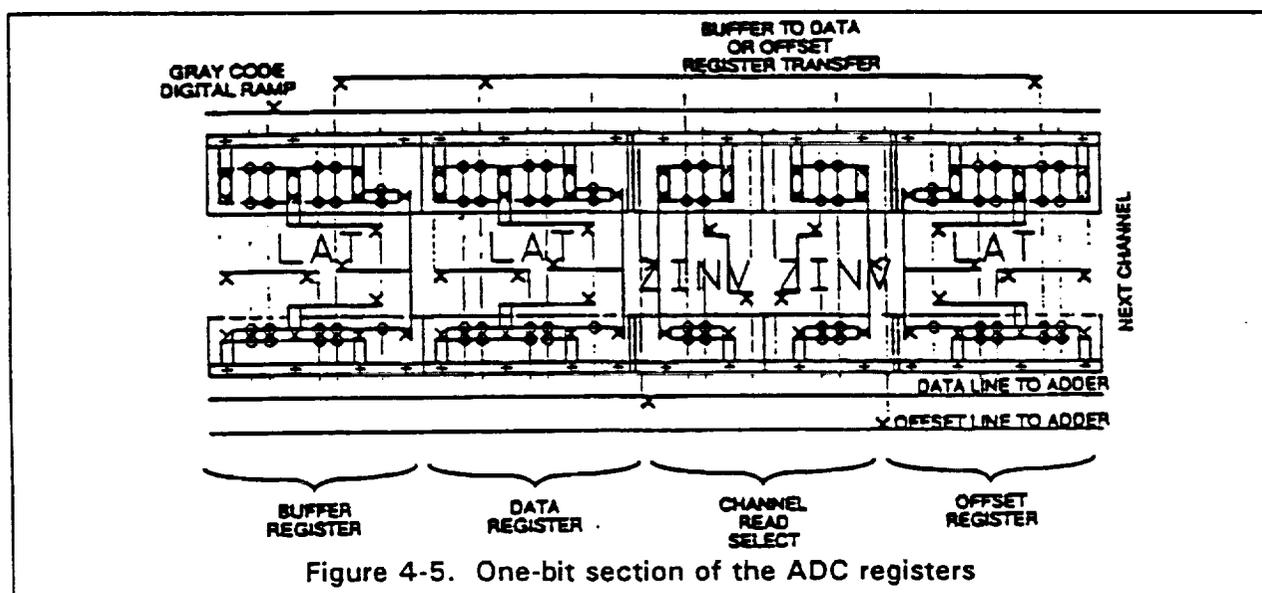


Figure 4-5. One-bit section of the ADC registers

Associated with the ADC registers are several on-focal plane support circuits. A counter generates the digital ramp from a master clock. The digital ramp is synchronized with the off-focal plane generated analog ramp by a frame sync pulse. Because the output of the comparators is asynchronous to the digital ramp, capturing the binary encoded digital ramp can cause large errors if the output occurs while the ramp is changing from one digital value to the next. Therefore, the counter output goes into a binary to gray converter to insure that the largest errors are held to less than $+ 1/2$ LSB. When the data is read out of the Data Register it goes through a gray to binary converter before the offset correction adder. The data from the Offset Register is similarly readout, with the exception that the 1's complement is transferred to the adder. This results in the offset being subtracted from the current data.

4.4 Interface Control

An interface control document is provided in Appendix A which describes the signal names and intended function. The document covers the IC in several sections. These sections are: digital control section, serial data I/O section, converter section, TIA interface section, filter interface section, and comparator interface section.

5.0 IC TESTING

Near the end of the IC design phase, the design of the test equipment was started. This allowed for the test equipment and testing procedures to have an impact on the design. Once the design of the IC was established, the fabrication and checkout of the test equipment was started.

Testing of the IC followed the typical method of first checking each of the circuit cells versus the computer simulations. For the TIAs this meant checking the output versus time in addition to frequency and noise measurements. Digital circuitry typically is tested at a higher level of integration to begin with due to its complexity. As discrepancies from the simulations are found, more detailed probing of the circuit is then used to determine the cause of the discrepancy.

5.1 Test Equipment

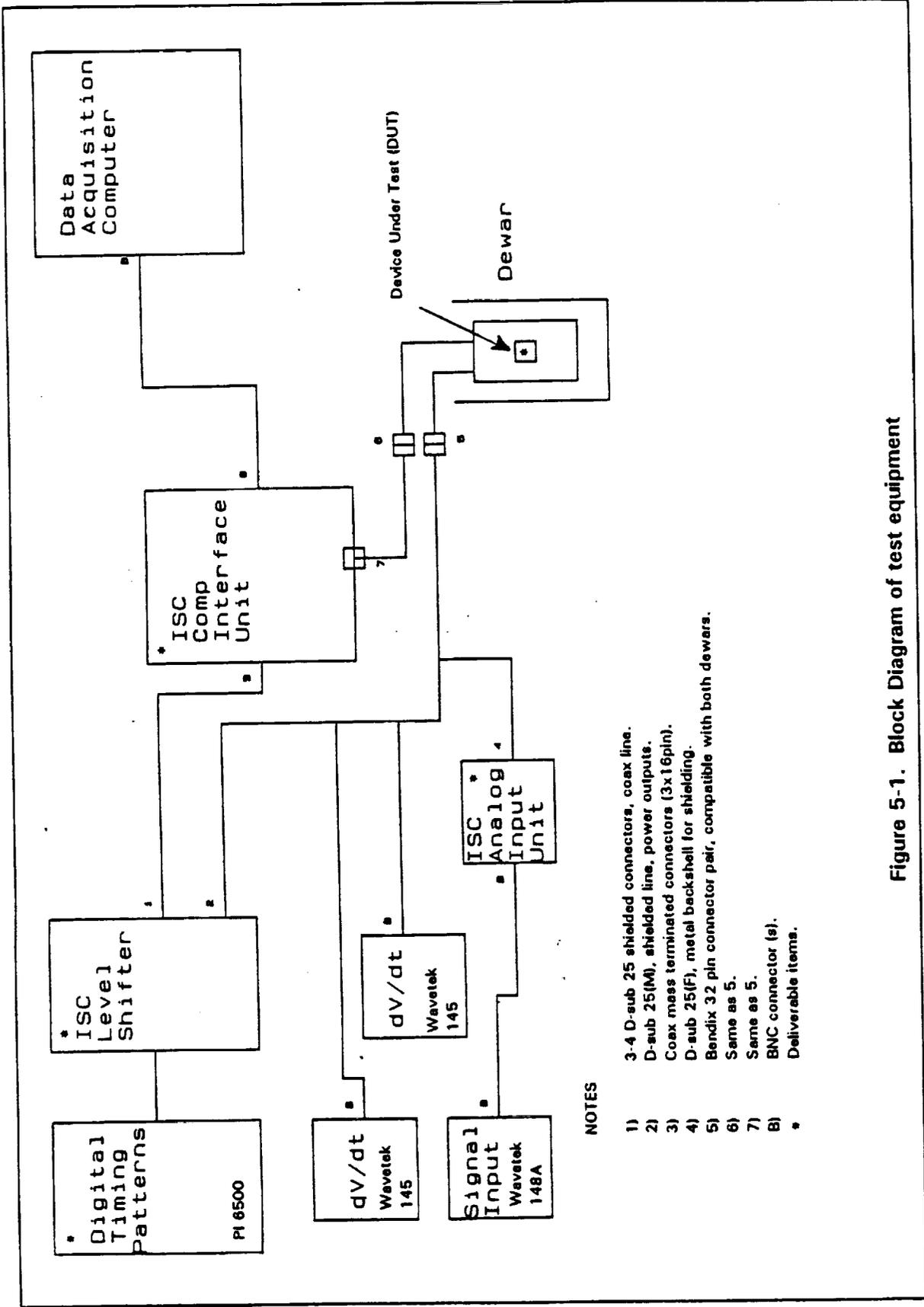
The test equipment consists of the Focal Plane Control Unit (FPCU), the Data Acquisition Computer, and the Dewar assembly. The focal plane control unit is comprised of three ISC fabricated components (Level Shifter, Analog Input Unit, and Computer Interface Unit), Pulse Instruments Pattern Generator and Three WaveTek Signal Generators. A block diagram of the test Equipment is shown in Figure 5-1.

5.1.1 Dewar Assembly

The entire system revolves around the dewar assembly. Two types of dewar assemblies were envisioned for this program. The first dewar assembly consisted of an ISC owned open mouth dewar, dewar wiring board, and test article fixture. It was designed for both preliminary check out and ambient and cryogenic circuit testing. The open mouth dewar allows for cryogenic temperatures by total immersion of the test article fixture into the liquid nitrogen. Figure 5-2 and Figure 5-3 shows the actual test article fixture and a test being performed at liquid nitrogen temperatures. Analog and Digital signals to the IC are kept segregated until very near the IC. Therefore, two connectors exit each dewar assembly, one for the analog and one for the digital signals. Wiring diagrams are shown in Figures 5-4 and 5-5 for the analog and digital cables. Both connections are made on Bendix circular connectors for reliability of connections.

A second dewar was procured for use in electro-optical testing. This side looking, pour fill dewar was fitted with two 32 pin Bendix connectors. The design of external cabling was kept consistent between the open mouth dewar and the electro-optical test dewar.

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NOTES

- 1) 3-4 D-sub 25 shielded connectors, coax line.
- 2) D-sub 25(M), shielded line, power outputs.
- 3) Coax mass terminated connectors (3x 16pin).
- 4) D-sub 25(F), metal backshell for shielding.
- 5) Bendix 32 pin connector pair, compatible with both dewars.
- 6) Same as 5.
- 7) Same as 5.
- 8) BNC connector (s).
- * Deliverable items.

Figure 5-1. Block Diagram of test equipment

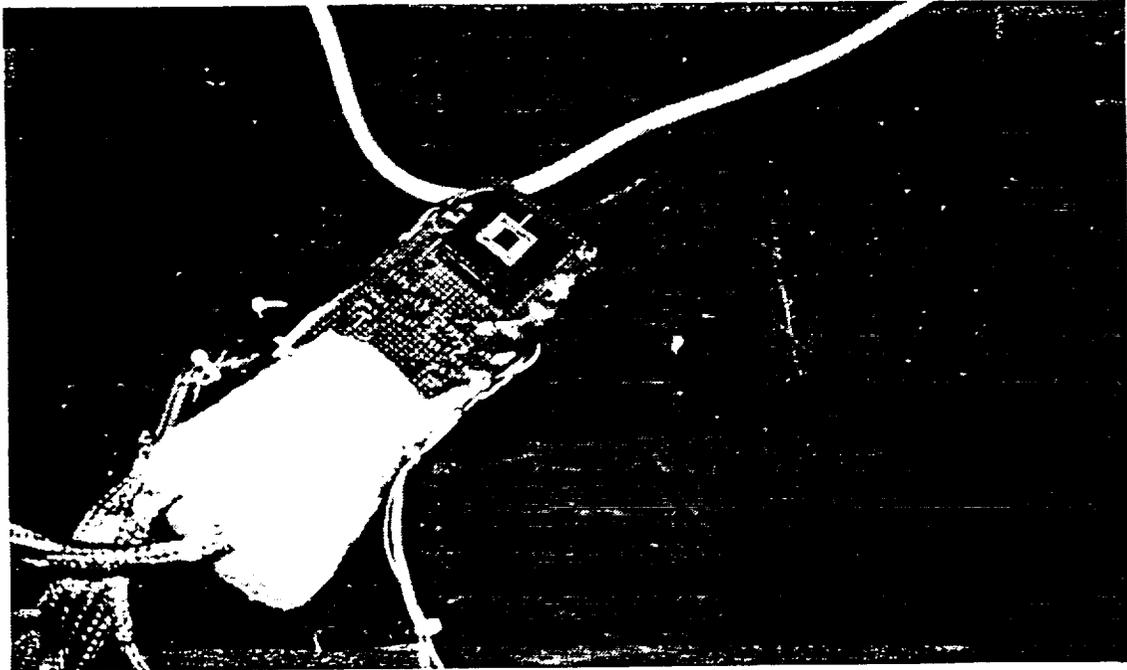


Figure 5-2. Test article fixture with a Pushbroom spectral imaging IC ready for immersion into an open mouth dewar

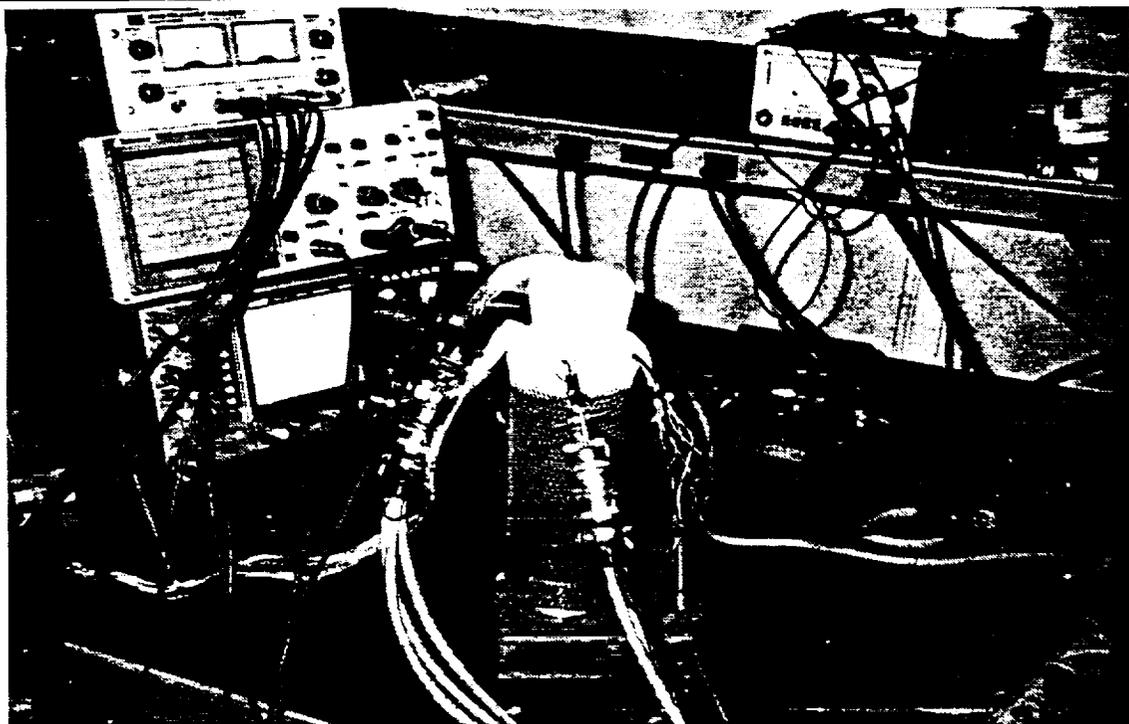


Figure 5-3. Test being performed at liquid nitrogen temperatures

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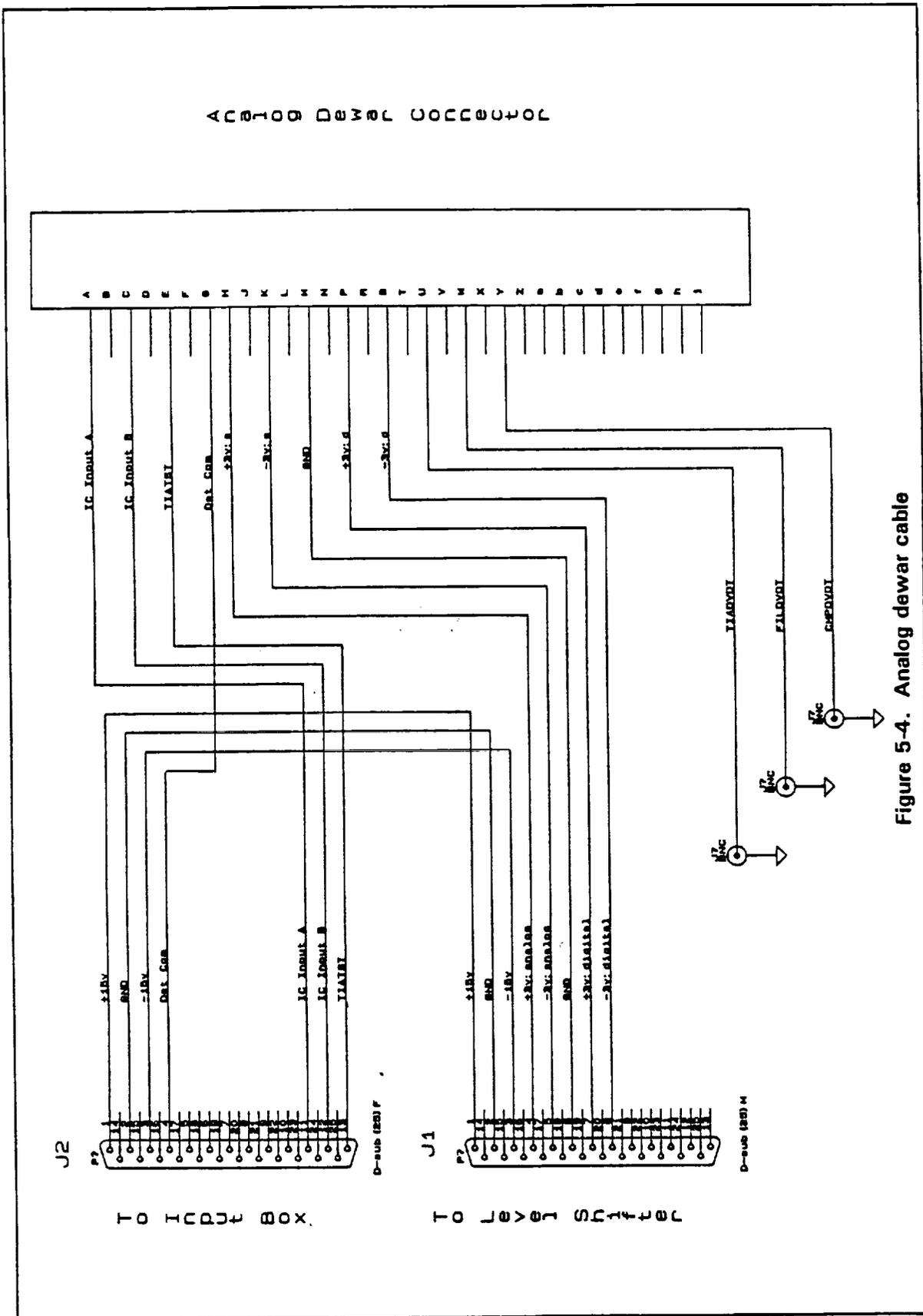


Figure 5-4. Analog dewar cable

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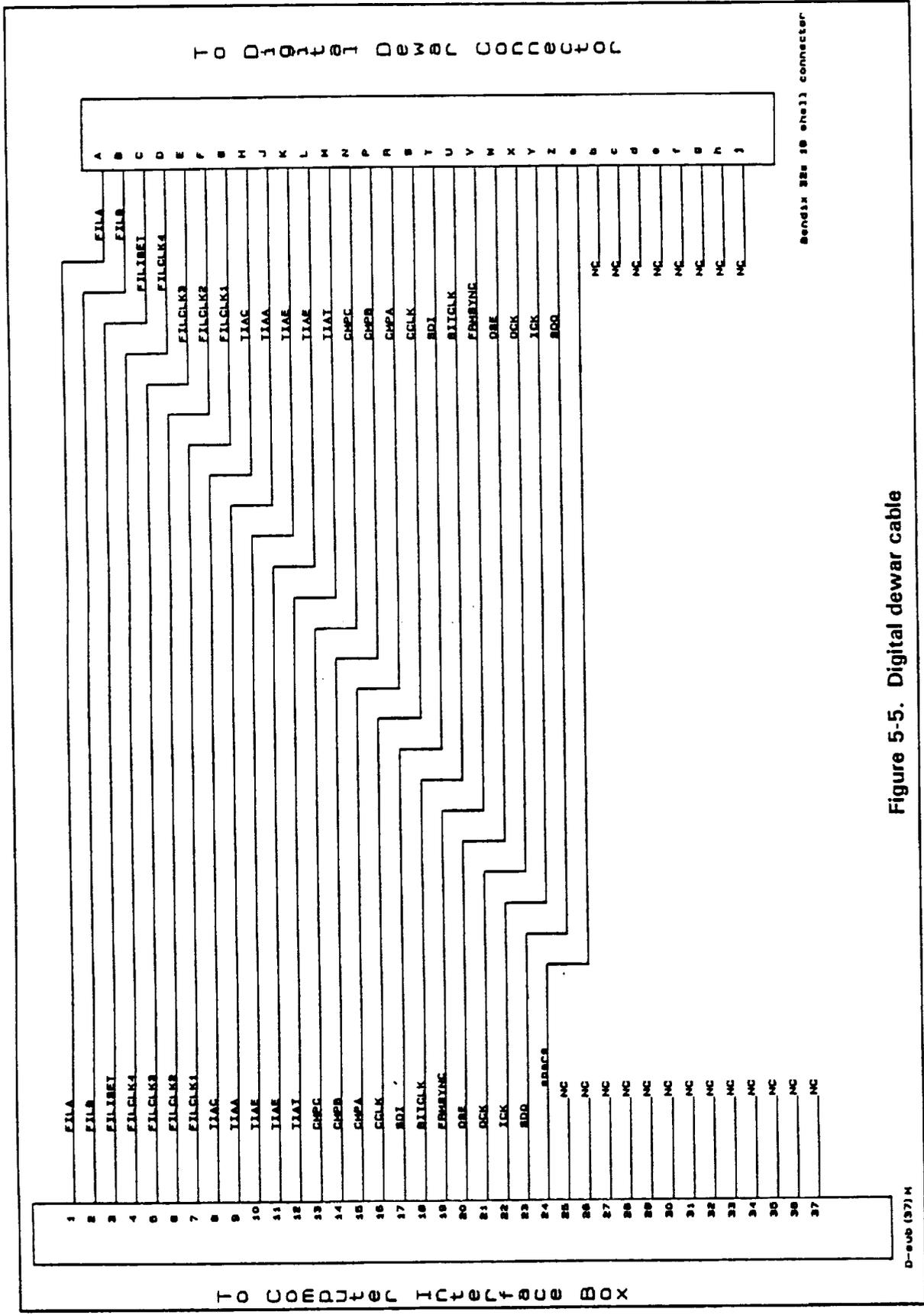


Figure 5-5. Digital dewar cable

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5.1.2 Focal Plane Control Unit

5.1.2.1 Computer Interface Unit

The digital connections from the dewar assembly goes through a cable to the Computer Interface Unit. This unit serves three purposes:

- 1) Acts as a feedthrough for all digital dewar Input/Output leads,
- 2) Buffers and isolates the IC data line so that data acquisition computer noise will not cause interference,
- 3) Level shifts IC timing signals for input into the data collection board.

Cabling requirements for this unit mandated that it be line powered.

The analog connector/cable has several connection points. Several inputs are wired direct through BNC connectors. Two D subminiature connectors are also connected to this cable which allow for interface with the Level Shifter and the Analog Input Unit. The function of the Level Shifter interface is to provide IC power (± 3 volts to both analog and digital sections), and to provide power to the Analog Input Unit (± 15 volts).

This unit was also designed to provide buffering action and optical isolation of the IC serial output data to a data acquisition computer's digital signal processor. This circuit is shown in Figure 5-6.

The Computer Interface Unit branches in two directions from the digital connector. This is shown in Figure 5-7. In the direction of the Data Acquisition Computer, there is a cable which attaches to a DSP (Digital Signal Processor) board within the computer. A feedthrough daughter board, fabricated by ISC, is part of this system as shown in Figure 5-8. The function of this board is to bypass a mandatory A/D converter function and feed data directly into the DSP chip on board.

5.1.2.2 Level Shifter

The path from the Computer Interface Unit leads to the Level Shifter. The function of this unit is to produce the ± 3 volts timing signals given a TTL level input which is generated by the Pattern Generator. The level shifter has been designed and tested to switch in less than 160 nanoseconds. The fastest signal used for the Pushbroom IC is 250 nanoseconds.

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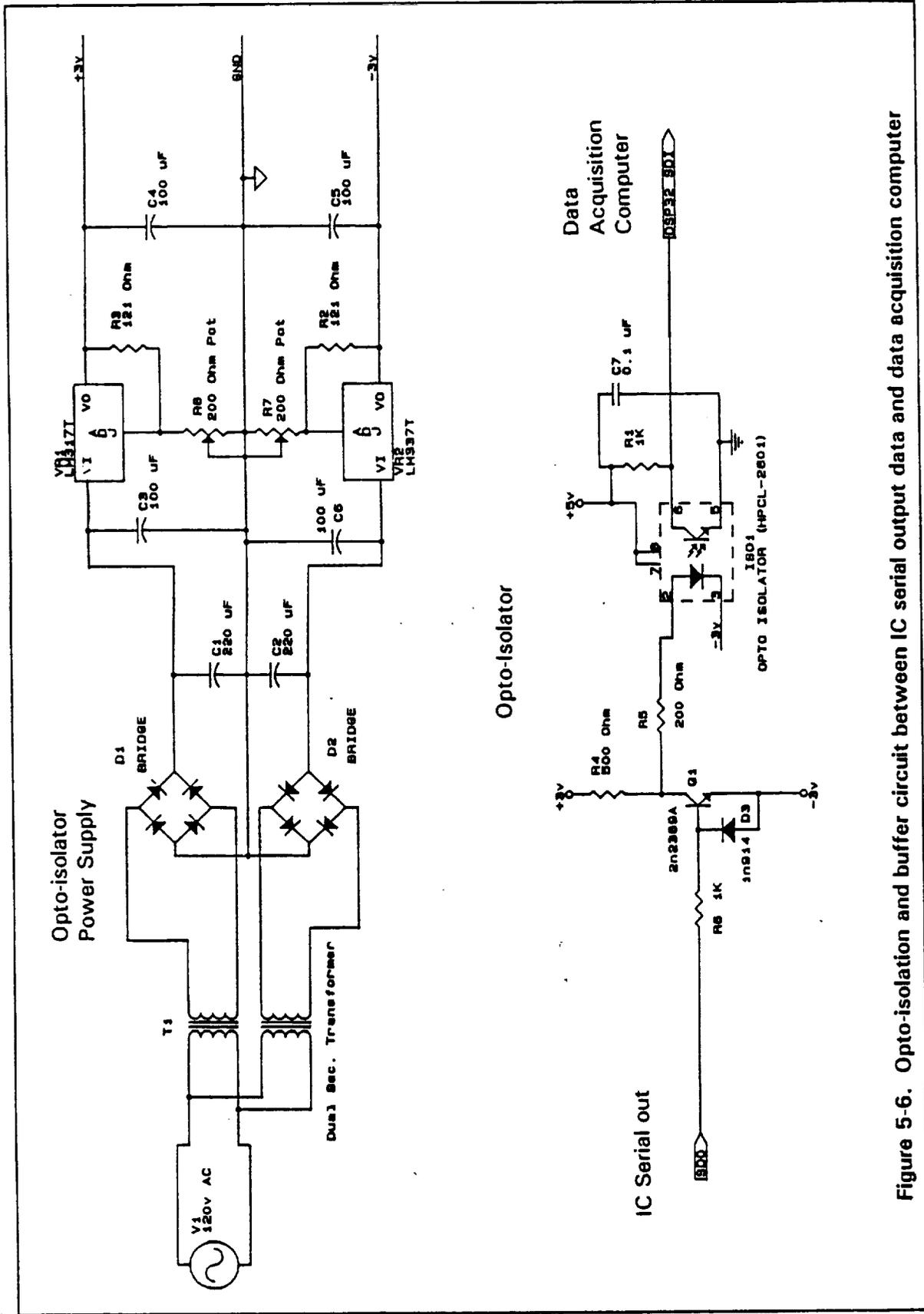
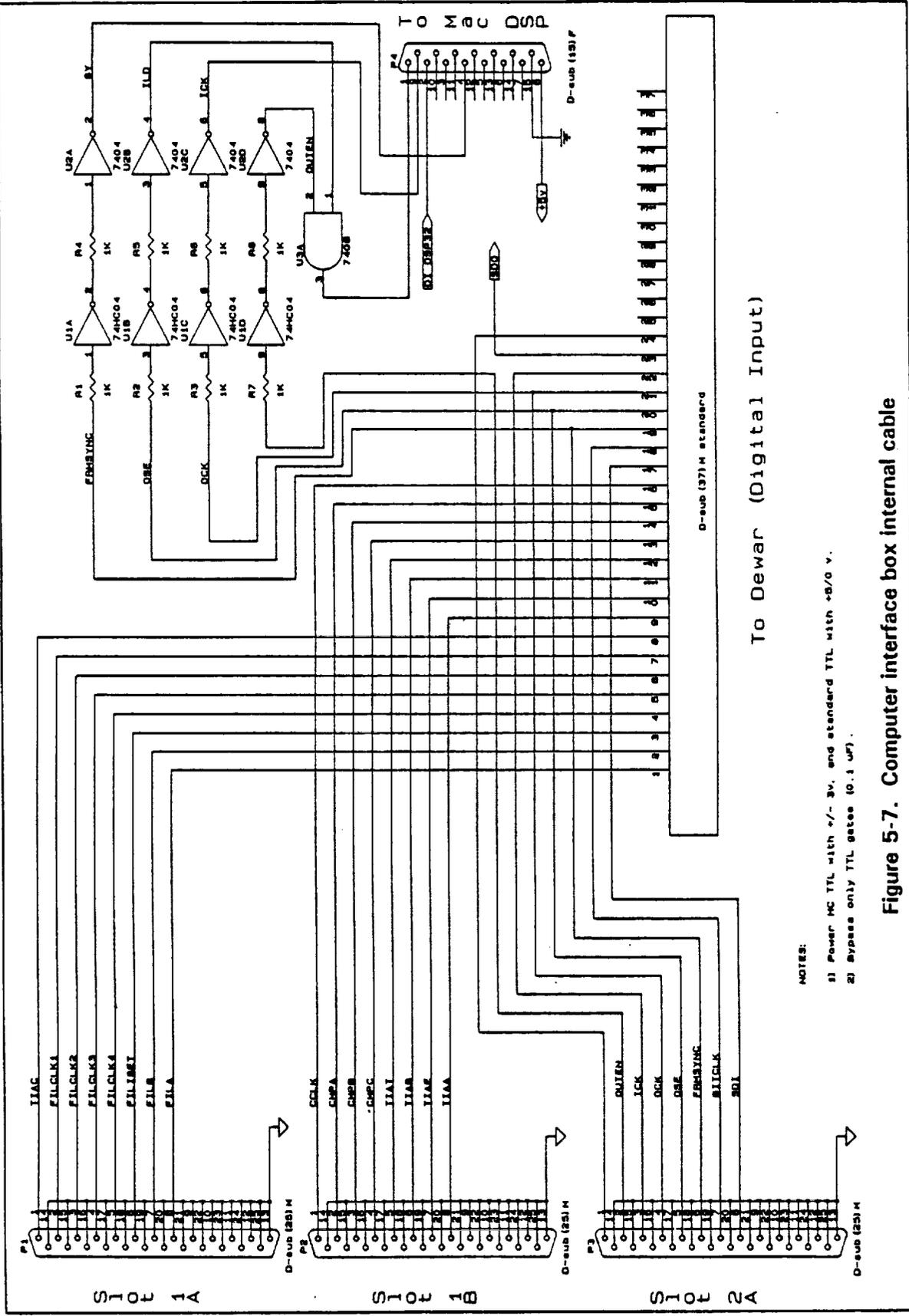


Figure 5-6. Opto-isolation and buffer circuit between IC serial output data and data acquisition computer

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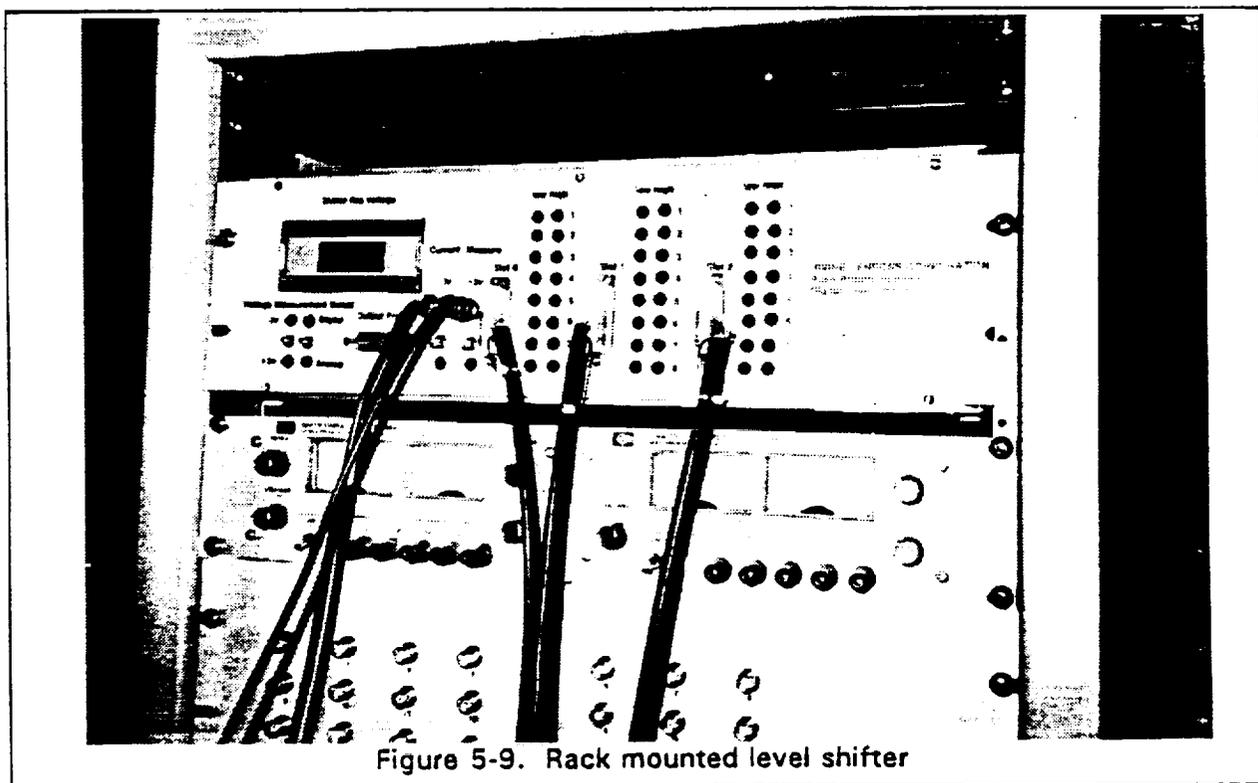
NOTES:
 1) Power MC TTL with +/- 3V, and standard TTL with +5/0 V.
 2) Bypass only TTL gates (0.1 uF).

Figure 5-7. Computer interface box internal cable

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The Level Shifter Unit has been designed to be a semi-modular, stand alone unit which shifts 24 input TTL level signals simultaneously. It has several boards with eight shifting channels each, as well as internal/external power supplies. It has been configured to also supply secondary test equipment power as well as power to the Pushbroom IC.

Each channel of the unit is equipped with two LEDs which will illuminate alternately depending on the present level of output. Figure 5-9 shows the actual level shifter in a rack mount. This unit was conceived to shift signals from 0 to 5 volts to -3 to + 3 volt signals as noise free as possible to prevent performance degradation of the analog portion of the Pushbroom IC. Analog switching FETs were chosen as the level shifting drivers instead of digital switches for several reasons. First, analog components are designed with lower noise output stages than the digital components. Second, analog ICs in general have a greater drive capability (both in current and across capacitance) than that of a digital gate. Since line parasitic capacitance is what generally leads to output transients, the greater the drive capability the lower the associated oscillations. Third, since analog ICs in general do not switch as fast as digital ICs, there is less overshoot and thus less associated ringing.



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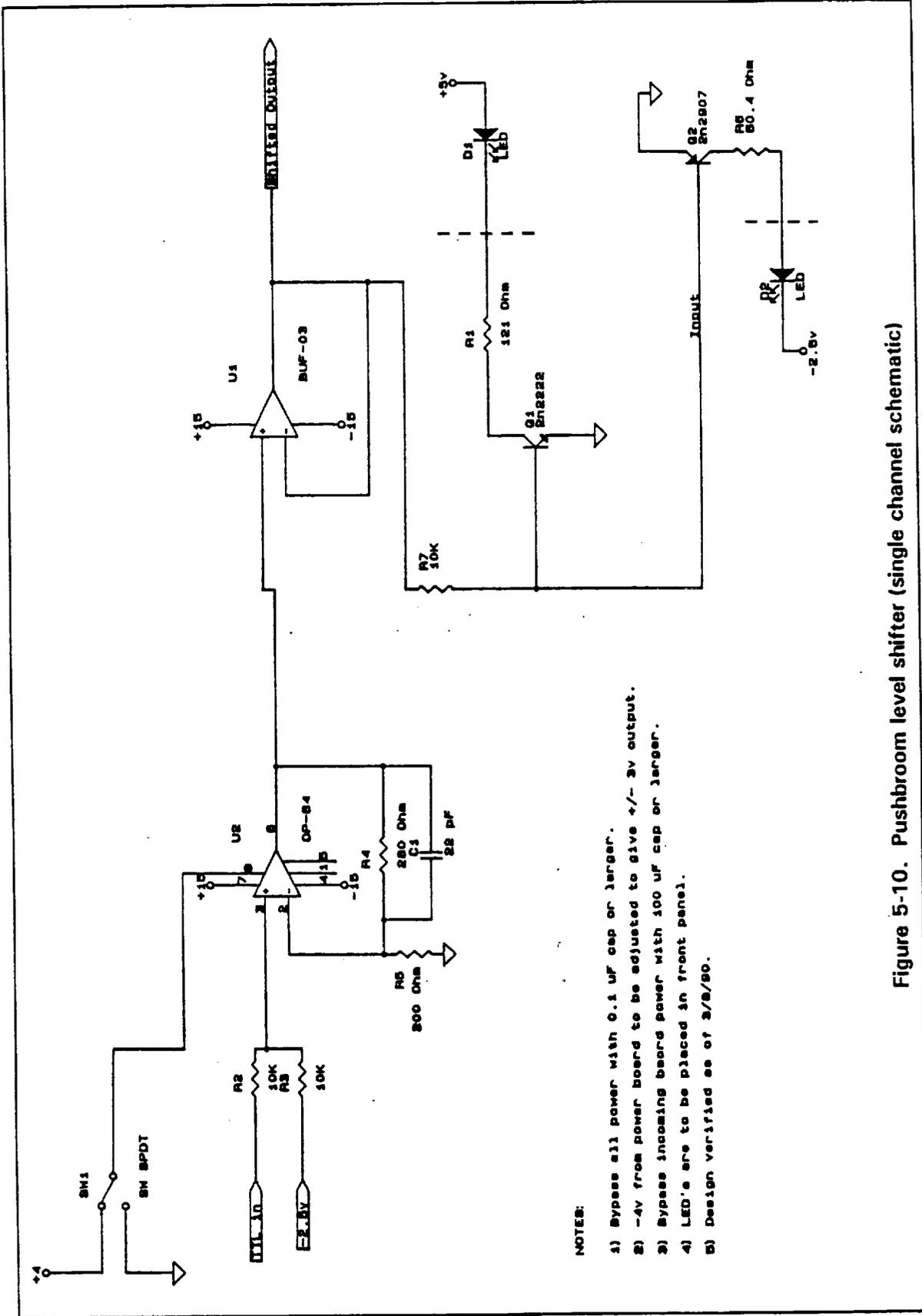
The amplifiers are operated in a non-inverting summing configuration, which literally shifts the TTL input signal down and then slightly amplifies it to give a 6 volt peak to peak swing. This circuit is shown in Figure 5-10. This configuration allows the circuit to be operated from a + 15 volt supply.

The amplifier chosen, OP-64, has a slew rate of 160V/microsecond, which yields a transition around 70 nanoseconds. Because the circuit board connections are made with wire wrap and wire lengths are up to 6 inches, parasitic capacitance has increased the transition time to 160 nanoseconds, however, this is adequate for meeting the maximum switching frequency requirement of 1 MHz.

5.1.2.3 Analog Input Unit

The unit is used as the source of all analog input signals. It has been segregated so that crosstalk with switching signals will be kept to an absolute minimum.

The unit has two types of amplifier circuits. The first takes two low frequency signals which are used to simulate detector inputs to alternating channels, and shifts them to above the +3 volt detector common level. This circuit is shown in Figure 5-11. A 110 Megohm resistor is in line with each detector input, and the current generated by a voltage slightly above the detector common voltage is the TIAs input. The variations in the resistor values from channel to channel simulate the responsivity variations of the detector. The second circuit is a buffer configuration that can be trimmed to +3 volts \pm 100 millivolts. This circuit is shown in Figure 5-12. This buffer circuit supplies the detector common voltage.



- NOTES:
- 1) Bypass all power with 0.1 uF cap or larger.
 - 2) -4v from power board to be adjusted to give +/- 3v output.
 - 3) Bypass incoming board power with 100 uF cap or larger.
 - 4) LED's are to be placed in front panel.
 - 5) Design verified as of 3/8/80.

Figure 5-10. Pushbroom level shifter (single channel schematic)

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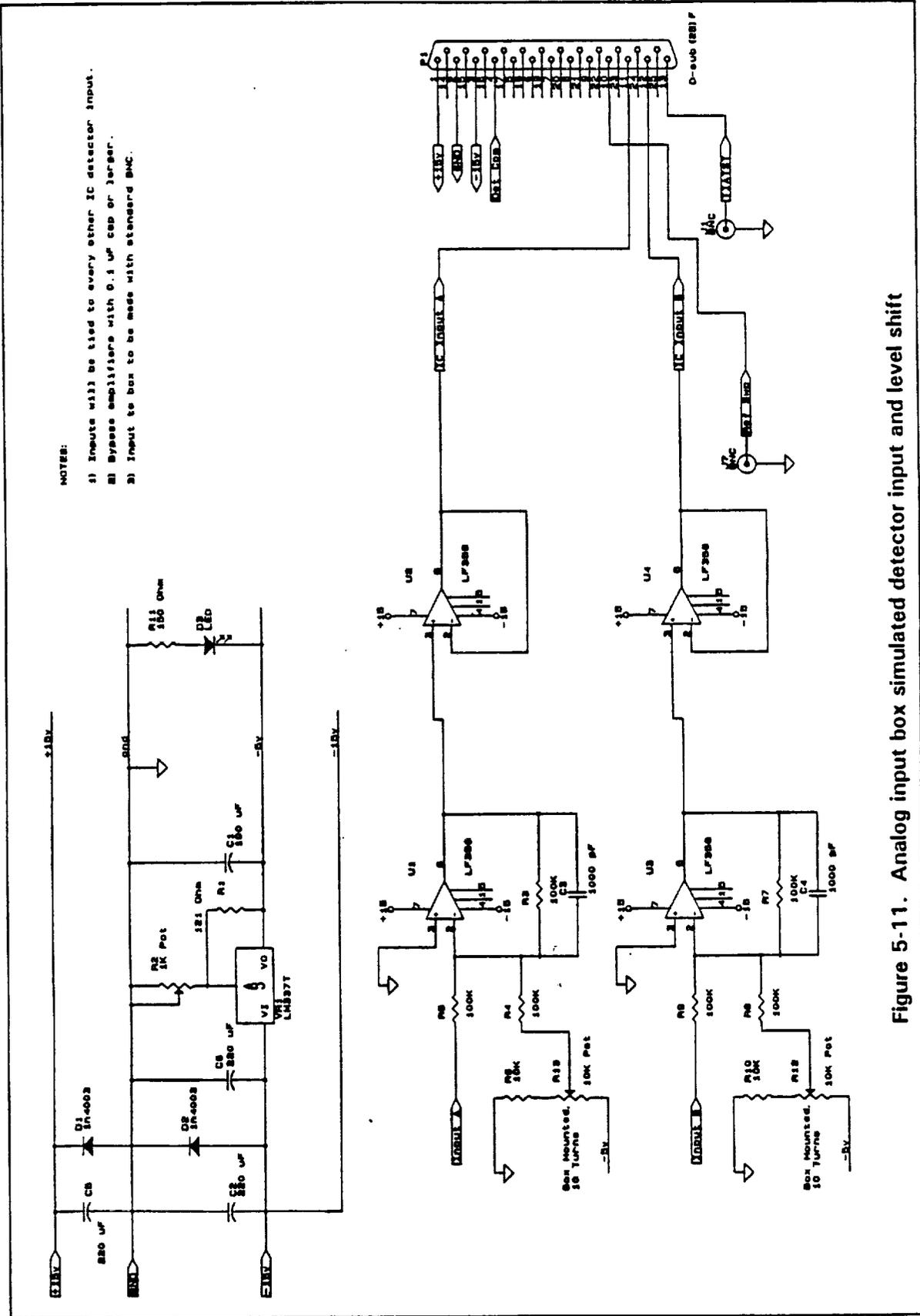


Figure 5-11. Analog input box simulated detector input and level shift

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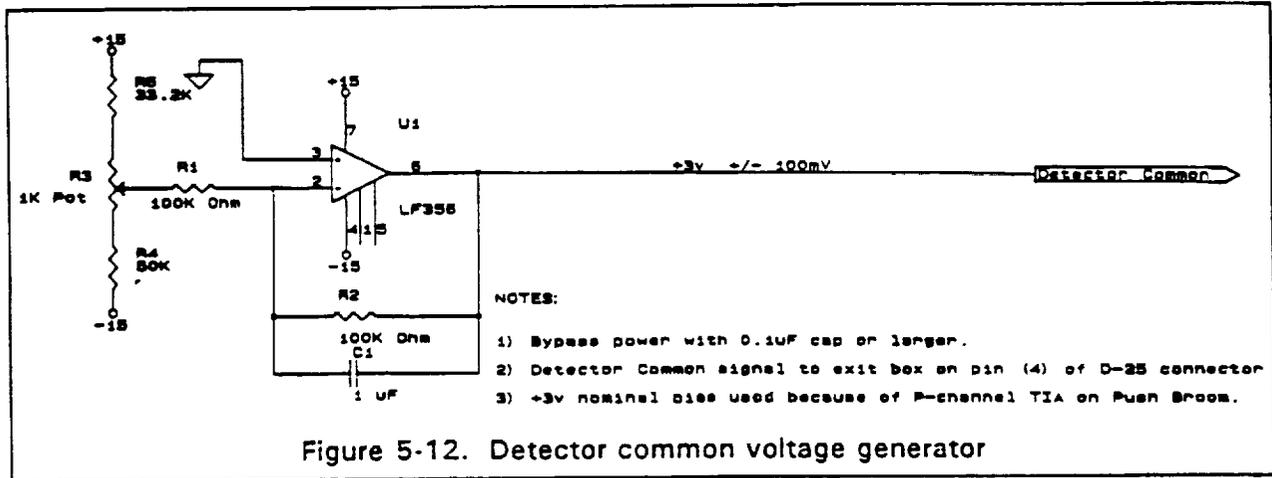


Figure 5-12. Detector common voltage generator

5.2 Test Results

Figure 5-13 shows a microphotograph of the Pushbroom IC. Three iterations of this IC were fabricated and tested. The first iteration yielded very good results on the analog portion of the IC (TIA, Filter, and Comparator). The second iteration allowed for the clean up of digital layout errors. The third iteration produced end-to-end working ICs which demonstrated A to D conversion, and gain and offset correction functions for use on the focal plane.

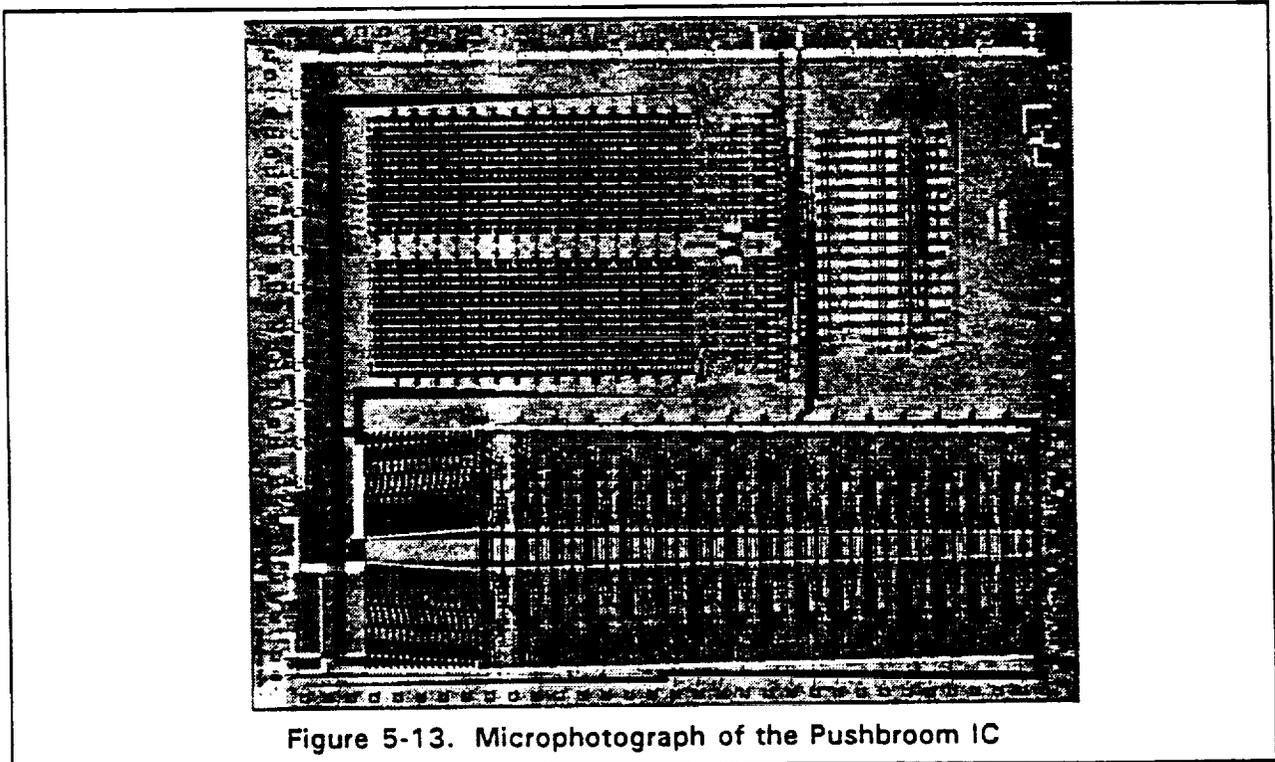


Figure 5-13. Microphotograph of the Pushbroom IC

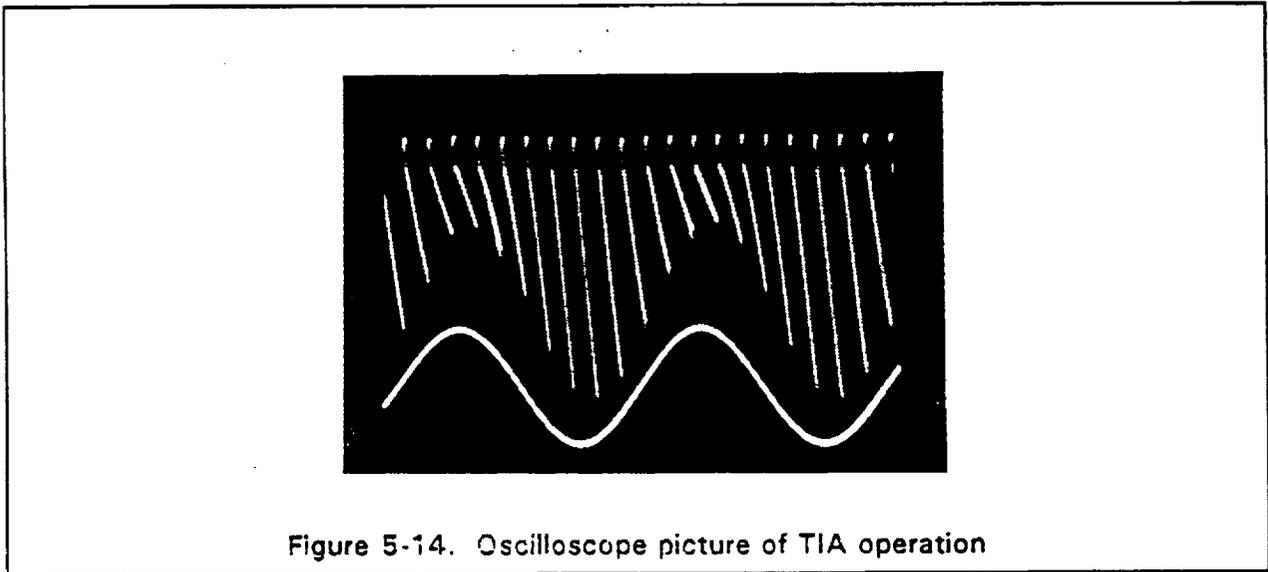
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5.2.1 First Iteration Analog Results

The analog portion of the IC consists of the TIA, filter, and comparator. Data was measured on the TIA linearity, bandwidth, and transimpedance; the filter gain and bandwidth; and the comparator linearity and resolution. All analog tests were performed by microprobing inside the IC on special test points established for this purpose. The measurements indicated that the analog critical cells were functioning, however the test setup, including the microprobing inside the IC, introduced significant noise. Thus, the linearity and comparator resolution were not as good as the final iteration results.

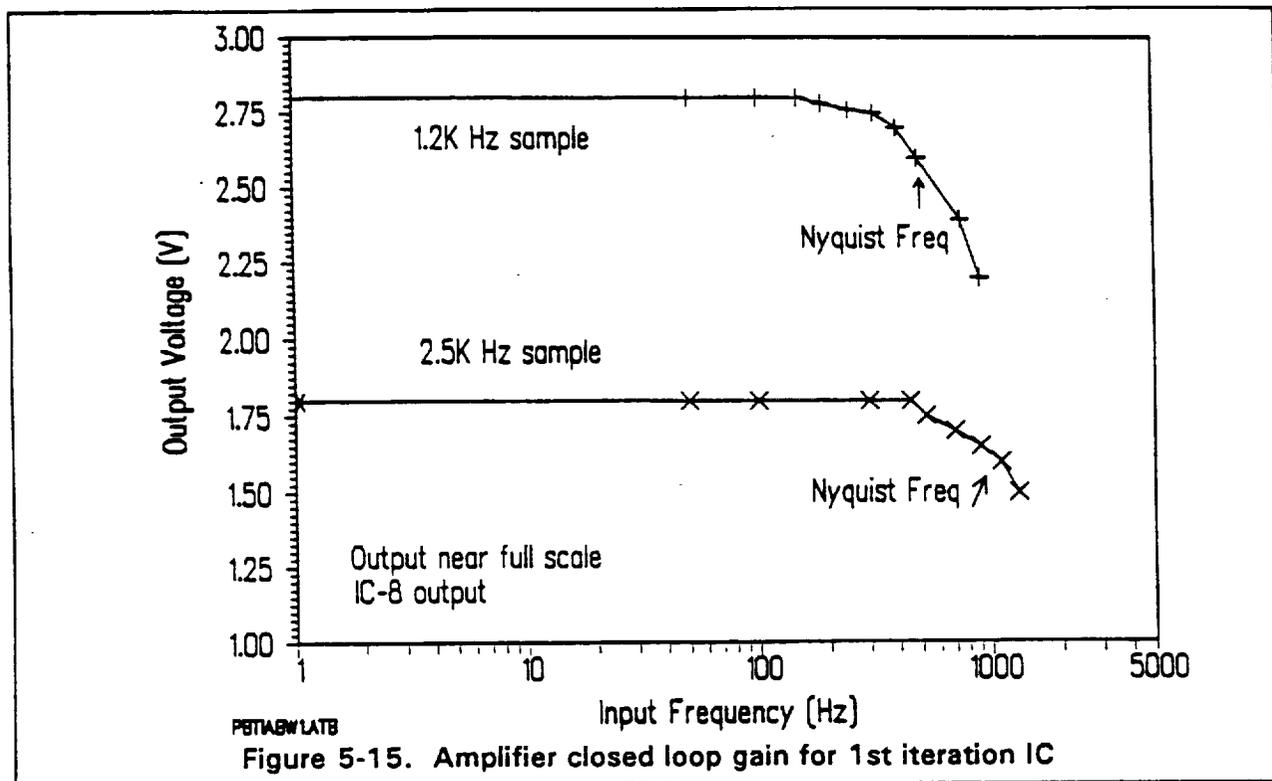
5.2.1.1 TIA Tests

TIA operation is shown in Figure 5-14. The integration and dump signals follow the input sine wave shown in the bottom trace of the oscilloscope picture. By varying the TIA integration and dump cycle period, two aspects of the amplifier are seen in Figure 5-15. First by reducing the integration period (increasing the sample rate from 1.2 KHz to 2.5 KHz) the TIA output signal is reduced for the same level of input signal. Second by increasing the sample rate the closed loop bandwidth is increased.



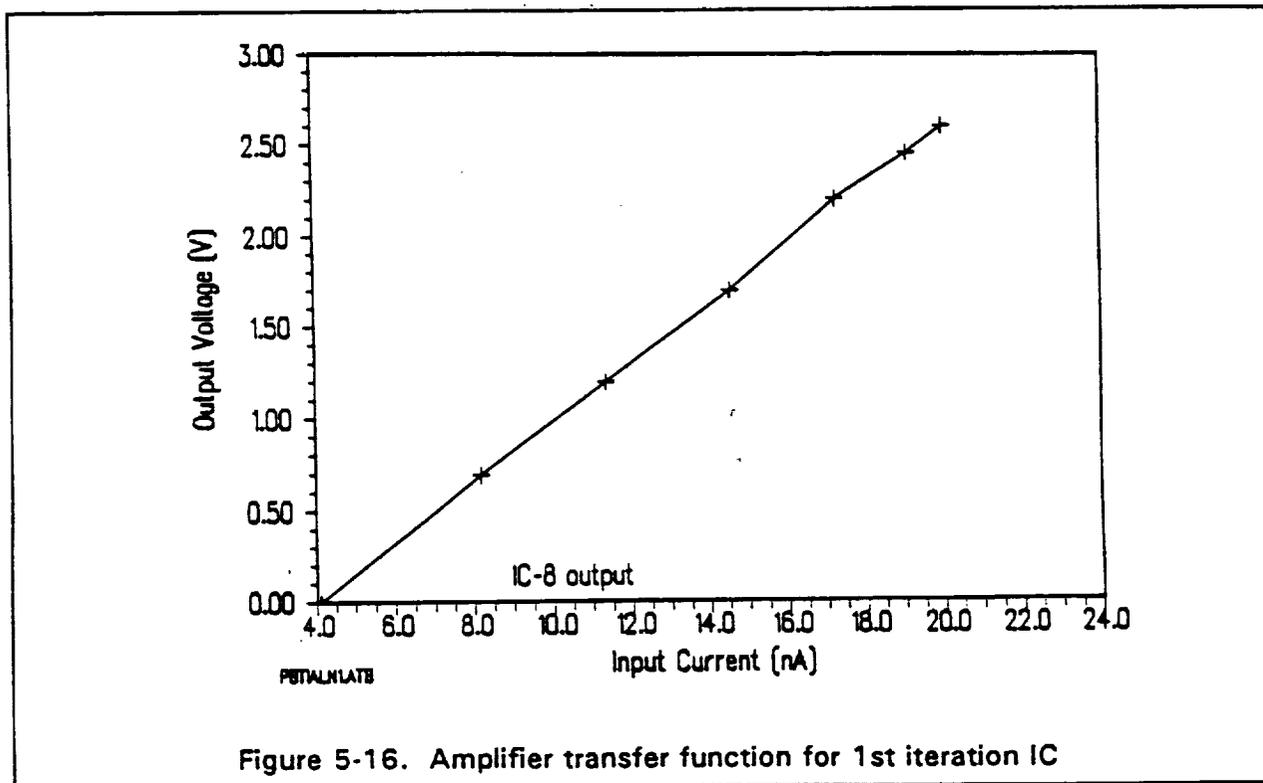
The results of the linearity test are shown in Figure 5-16. The output voltage of the amplifier was measured as a function of the input current. The maximum deviation from a straight line was 4.2%. The transimpedance was also measured during this test to be 133 Megohms.

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PETALNLAB

Figure 5-15. Amplifier closed loop gain for 1st iteration IC



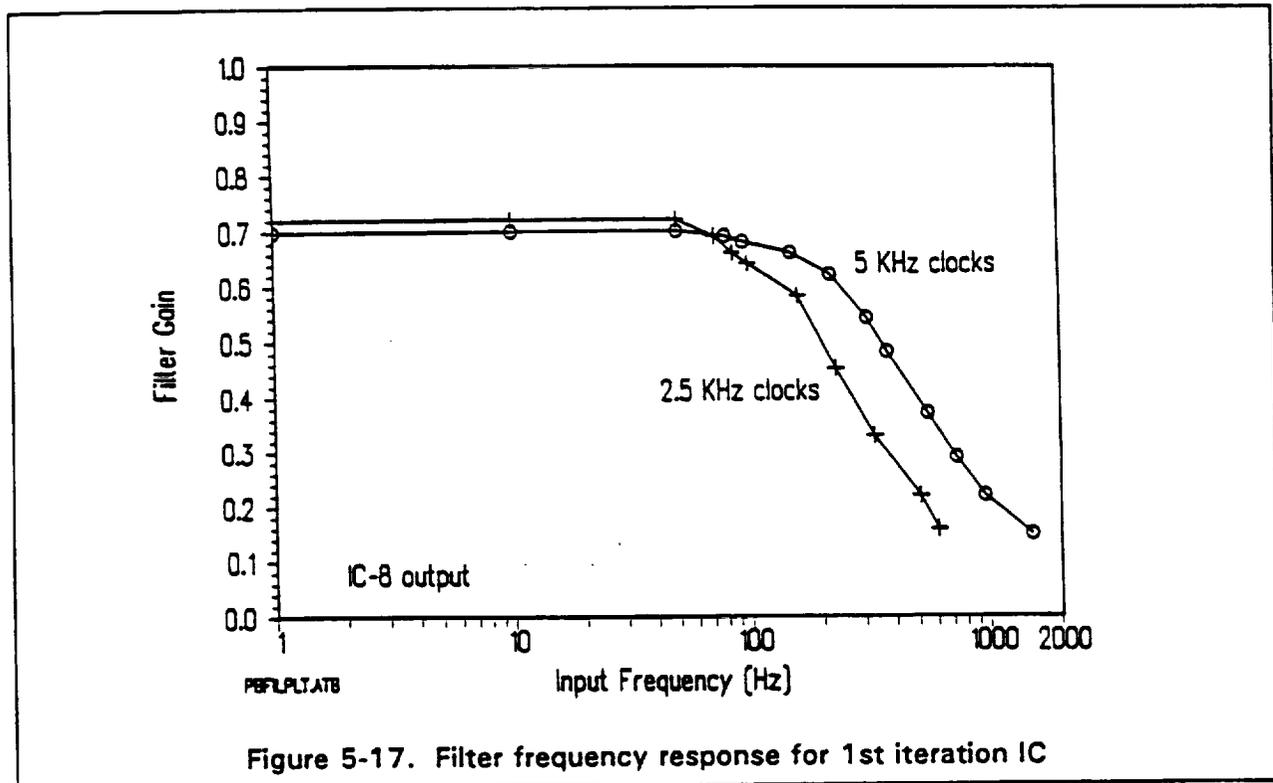
PETALNLAB

Figure 5-16. Amplifier transfer function for 1st iteration IC

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5.2.1.2 Analog Filter

Test data taken on the filter is shown in Figure 5-17. Three parameters of the filter operation can be seen in this data. The filter response is a function of the clock frequency. Faster sample rates increase the filter roll off frequency. The filter gain is approximately 0.7 and the filter 3 dB roll off is 400 Hz.



5.2.1.3 Comparator

The operation of the comparator is shown in Figure 5-18. The triangular wave in the photograph is the analog ramp signal. The comparator output signal is seen to trip high to low at the same point in the ramp sweep. The comparator is reset, low to high, at the end of the ramp sweep. The noise on the comparator can be determined by feeding a DC signal into the comparator and measuring the jitter of the comparator trip position. The jitter in time corresponded to a resolution of 9 bits in this first iteration. The linearity measurement for the comparator is shown in Figure 5-19. The trip voltage was noted as a function of the input level to the comparator. The deviation from a straight line of the comparator is 5.8% for the first iteration IC.

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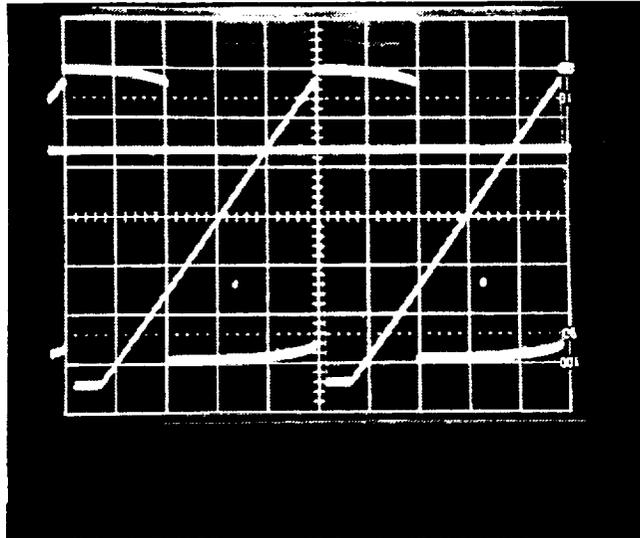


Figure 5-18. Oscilloscope picture of comparator operation

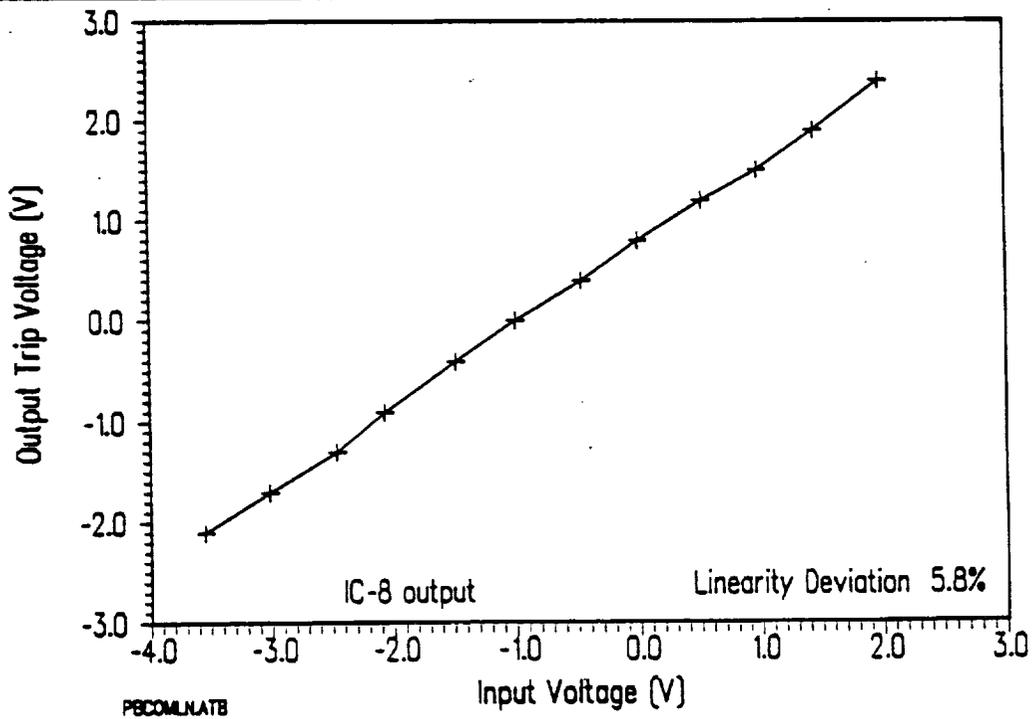
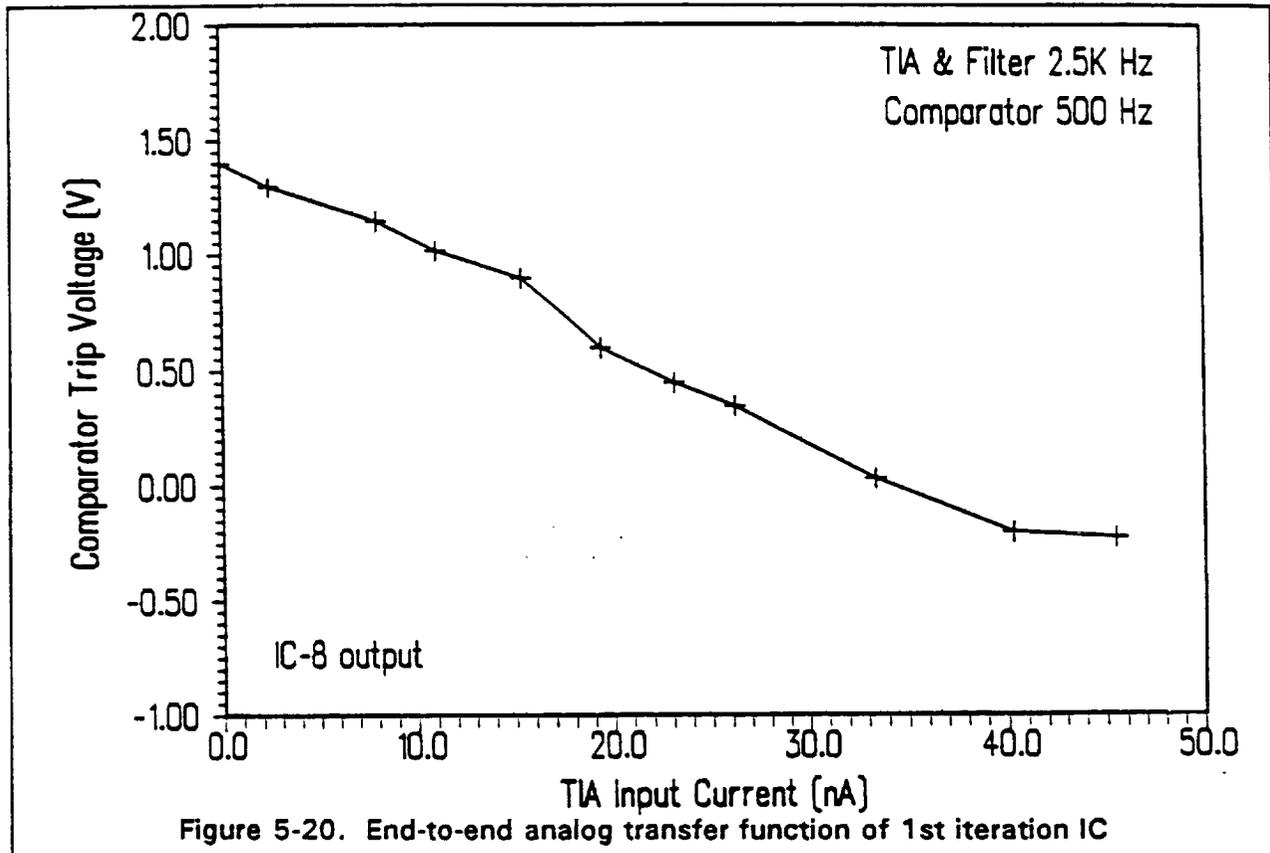


Figure 5-19. Comparator trip voltage as a function of input level for 1st iteration IC

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5.2.1.4 Analog End to End

The final test performed on the first iteration IC was an end to end test of the analog section to verify signal interface between each of the critical cells. This test data is shown in Figure 5-20. The transfer function compares the input current of the TIA to the output trip voltage of the comparator. The transfer function deviation from a straight line is 10%.



5.2.2 Second Iteration Results

The second iteration IC contained a few layout errors which prevented end-to-end operation. Instead of devoting time testing this IC, hours were saved for testing a third iteration IC. The primary cause of failure was layout errors. This problem has since been corrected by utilizing computerized layout validation.

5.2.3 Third Iteration Results

The third iteration results were very good. Gain and offset correction accuracy met the design criteria. The A to D converter operated very linearly with 11 plus bits of resolution at 1000 Hz frame rate. All operational modes of the IC were functional. Crosstalk between channels was less than expected. Minor problems still exist with the IC. These include a

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failed serial output (backup parallel output did function properly), and excessive leakage current in the input protection diodes (data and command signals still pass through the input protection unaffected). While these problems caused some testing difficulties and some performance degradation, very good results were still obtained.

5.2.3.1 Digital Cell Testing

The initial focus of the iteration testing program was to validate the operation of the digital cells. The following sections details the operation of each of the critical digital cells.

5.2.3.1.1 Digital Ramp Counter

Initial testing of this cell was done with a 1 MHz clock, producing a maximum ADC resolution of 10 bits at 1 KHz. During later phases of testing, this clock was increased to 4 MHz to increase the maximum ADC resolution to 12 bits. Individual component testing of the counter showed their ability to work up to 22 MHz which would allow for a resolution testing of up to 14 bits at 1 KHz.

When the counter frequency was increased from 1 MHz to 4 MHz, several changes to the test equipment layout were required to reduce the noise of the circuit. Initially, the 4 MHz clock caused a large amount of noise (up to 500 mV) on the analog signals, including the comparator output. Using standard shielding and digital terminating techniques, the noise problem was reduced to a manageable level. Using RG-148 coaxial cable and two 330 ohm terminating resistors reduced the noise by over 500%. In addition, the analog input lines were shielded in a similar way for the first time. The TIA input resistor, used to simulate the detector, was moved closer to the IC and its impedance increased from 110 to 220 M Ω . These steps resulted in approximately the full theoretical performance of 12 bits.

5.2.3.1.2 Buffer Latches

The buffer latches were tested and found to be fully functional. The previous iteration of the IC had problems with both the counter reset and the data latch control. The first indications of proper on-chip ADC was observed in these latches.

5.2.3.1.3 Data and Offset Latches

This cell is identical to the temporary latches in function, but its control is different. There were errors in the control section that impacted this cell on the second iteration. All of these errors involved the control lines DLAT and OLAT, which commands the data to move from the Buffer to the Data and from the Data to the Offset latches respectively. Testing both in the control section and within the cell proved that it was now fully operational.

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5.2.3.1.4 Binary to Gray and Gray to Binary Converters

These devices are in place to limit the asynchronous comparator error of the ADC to 0.5 bits. They convert the binary counter to graycode so that there is only theoretically 1 bit transitioning at any one time.

5.2.3.1.5 Subtractors

As with the previous iteration, these devices functioned properly. They can only be correctly tested by freezing the timing at a point, and then comparing the two inputs and the output. A test technique problem exists when probing these devices. The charge on the probe can cause the data in the latches to change. Therefore, it is possible to change the data with the act of probing on the test points. In normal operation this does not occur.

5.2.3.1.6. Address Generator

There are two major groups of buffers on the IC, each controlled by the address counter that originates in the control section. The first set of buffers selects one of 16 channels in both the high and low slots. The IC is laid out as two mirror image groups of 16 channels. This data is gray to binary converted, offset subtracted, and placed on the gates of the second set of buffers. The second set of buffers selects one of the two available data sets from the high or low slots. This data is then threshold subtracted and loaded into the serial output shift register. All addressing schemes and buffers are operating properly.

5.2.3.1.7 Serial Input (Command and Threshold Register)

As a back-up precaution to the serial input technique, a parallel input was also added. The parallel input was largely not required because the serial input section was nearly fully functional. The threshold register could receive input, and all but one of the serial command register latches also functioned properly. Each of the serial command register latches is identical, so that the only logical explanation for the failure of one latch is that another IC error that connects to the output of the latch forced the data to remain always low. This command bit, ABNORMAL, is the command for the TIA gain set to begin, during later tests it was driven from off the chip, via the parallel input line.

5.2.3.1.8 Serial Data Output

The serial data output appeared to be completely inoperative. This function did not operate on the previous iterations. Two indications of the failure were found during testing. First, the SRL0D line, which causes the parallel data to be loaded into the serial output register, was found to be working improperly. No immediate cause for the problem has been found. As a backup precaution, a parallel output was provided on this iteration of the IC and

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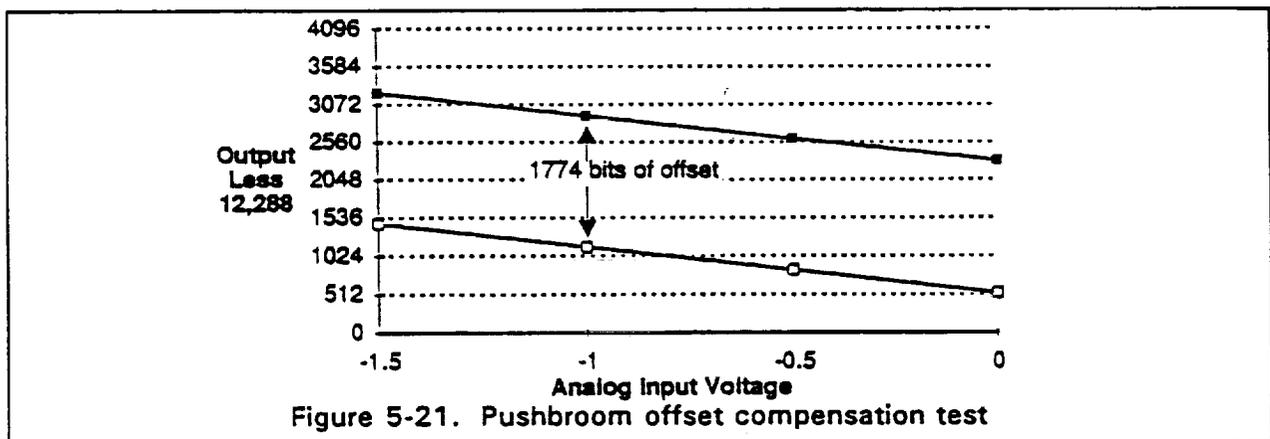
used throughout the testing to gather results. Second, the large output buffer stage was found to have a very large current draw. These minor defects did not impact further data gathering as a backup means of getting the data off of the IC was utilized.

5.2.3.2 IC Operation

5.2.3.2.1 Offset Correction

On chip offset compensation is a relatively simple circuit. The user inputs a command (via the serial data input stream and the command register) when an appropriate detector input is applied to store the systems' offset. Each of the 32 channels contains its own offset register, so theoretically the digital output of all channels will be the same at this detector input level. In the output sequence for each channel, the data register is subtracted from this offset register to give an offset corrected value. In the case of the Pushbroom IC, the data register contains 14 bits and the offset register contains 12 bits with the LSB equal to zero. For these tests the counter was operated at 4 MHz. This allows for the IC dynamic range to be 12 bits at the testing frame rate of 1000 Hz. Thus, even though the data registers are 14 bits, only 12 bits are used.

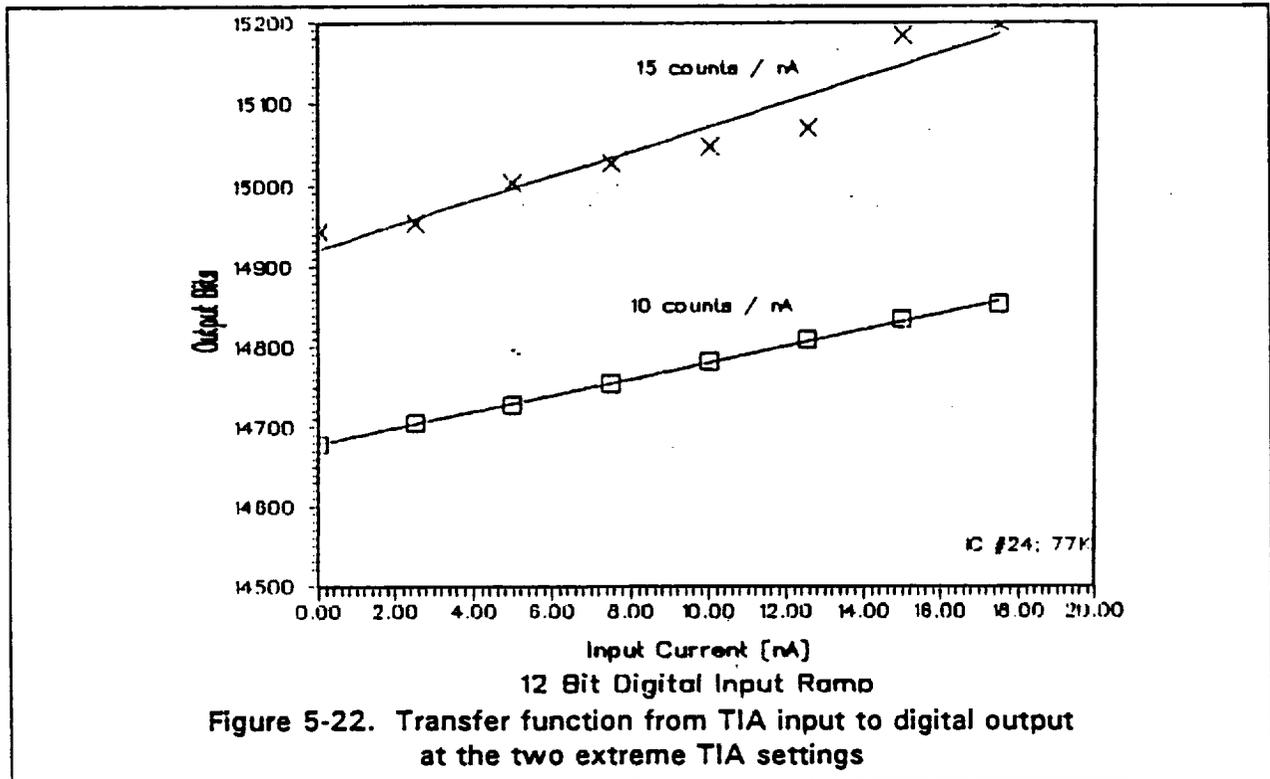
Testing of this cell consisted of two parts. First, it was verified that both the counter and offset register were functional by setting the offset register to a minimum (0) and then a maximum (4096) and observing the effect on the output word (data). Next, a stable point along the output curve was chosen to provide a predictable offset. Data was taken both with and without this offset number set. Analysis of the output curves shows that, as expected, no gain (slope) change is present while the DC offset change is. Figure 5-21 graphically depicts the events of this test. This test verified that the offset compensation worked to $\pm 1/2$ LSB up to its design dynamic range of 12 bits.



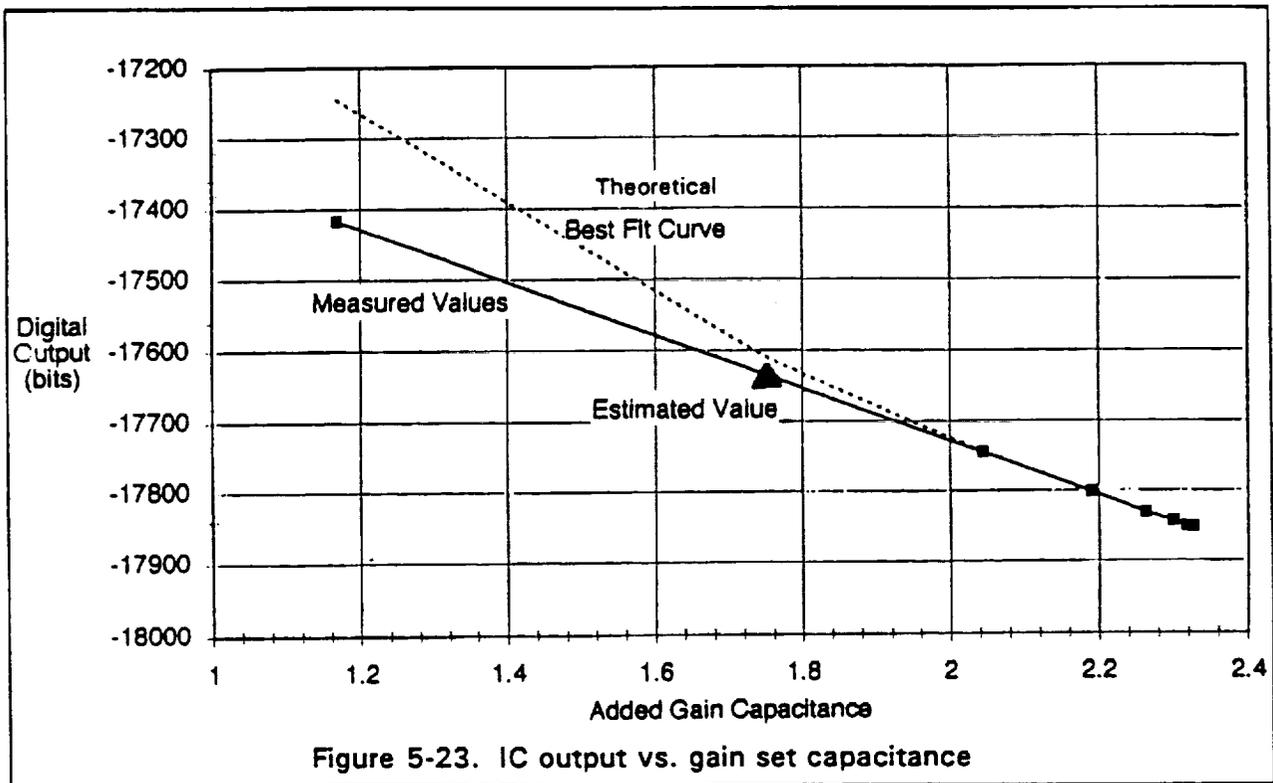
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5.2.3.2.2 Gain Correction

The goal of testing this cell was to demonstrate two parameters. First, the maximum gain switching ability shows the dynamic range of the gain set. This is important because it shows how close any two channels must be in initial gain in order to have no deviation in output after gain calibration. The second parameter tested for was "gain adjustment linearity." Output at any stable point with a significant detector input should show a theoretical change for each level of TIA gain change. Figures 5-22 and 5-23 show the results. In Figure 5-23 comparison in gain slopes was made by comparing the best fit straight lines of each of the curves. This figure shows that the maximum gain variance is 50%. Each stage of gain was set independently as shown in Figure 5-23. Unfortunately, it was not possible to switch out the MSB gain set capacitor, nor just set the first and second MSBs. Therefore, these two points were not used to calculate the best fit curve.



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The capacitance error for each of the gain set capacitors was calculated by determining the additional capacitance required to move the data point to the value estimated using the best fit value. Since this additional capacitance is cumulative, the previous capacitance is subtracted to get the error for a particular gain set capacitor. The results of these calculations are shown in Figure 5-24. No value is shown for capacitor number two since it could not be observed. Except for the MSB capacitor, all the errors are less than the smallest gain capacitor of 0.0091 pf. This implies that for this limited sample, that the gain non-uniformities should be correctable to less than 1%.

Another test was conducted on this circuit to see if there were any residual effects from switching the gain. The goal of the test was to observe the data before, during, and after a full scale gain change to see if any overshoot, undershoot, or "ringing" occurred in the channel electronics. As may be seen in Figure 5-25, there were no residual effects. However, the data points only represent every fifth TIA integration cycle, since the TIA runs five (5) times faster than the ADC.

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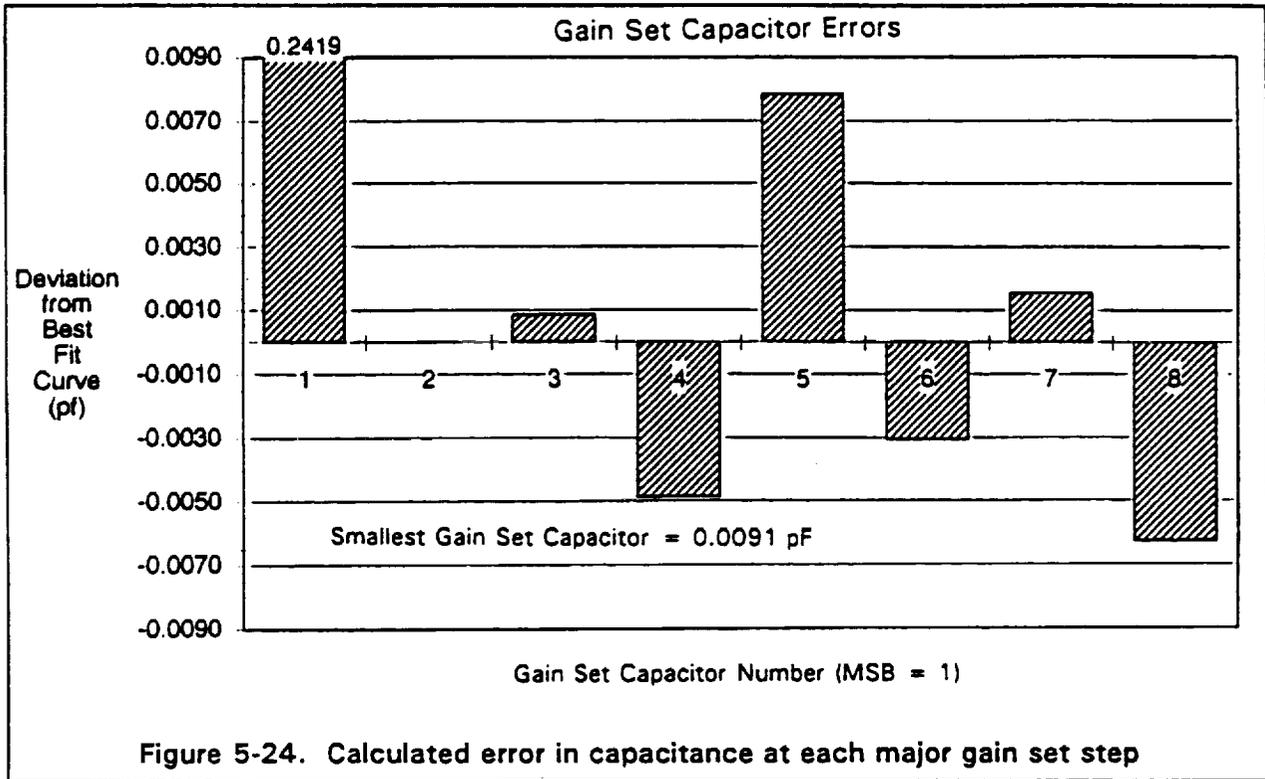


Figure 5-24. Calculated error in capacitance at each major gain set step

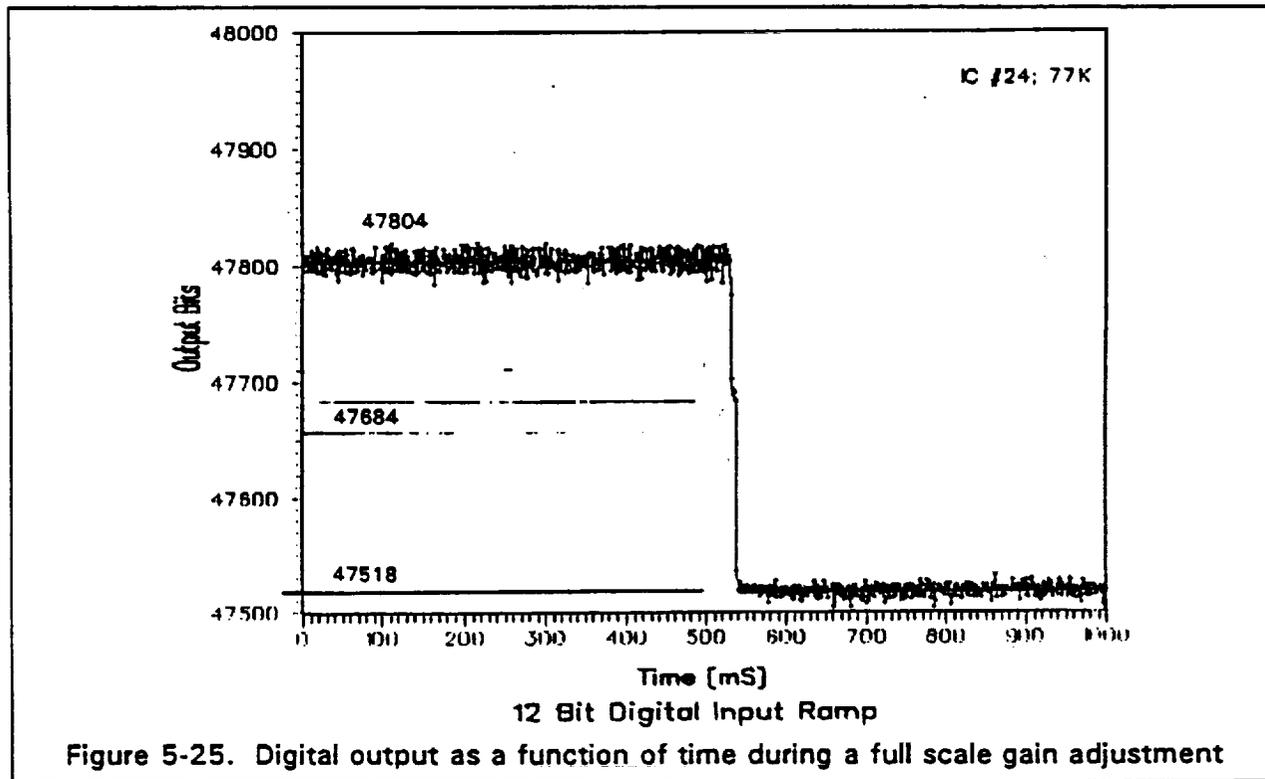


Figure 5-25. Digital output as a function of time during a full scale gain adjustment

5.2.3.2.3 Analog-to-Digital Converter

A digital data capture board and some custom software was used to input the Pushbroom digital data into an AT computer. An analysis was made based on the raw data obtained. The planned approach to use a DSP board operating inside an Apple MacIntosh computer was not possible due to the inoperable serial output section of the IC. The computer to IC interface was made through an interface box which has CMOS inputs and TTL outputs. Since there were no output drivers on the parallel output of the IC, special care was taken to remove any noise sources and present the IC output with a high impedance input. All data was obtained while the IC was at liquid nitrogen temperatures, i.e., 77° K.

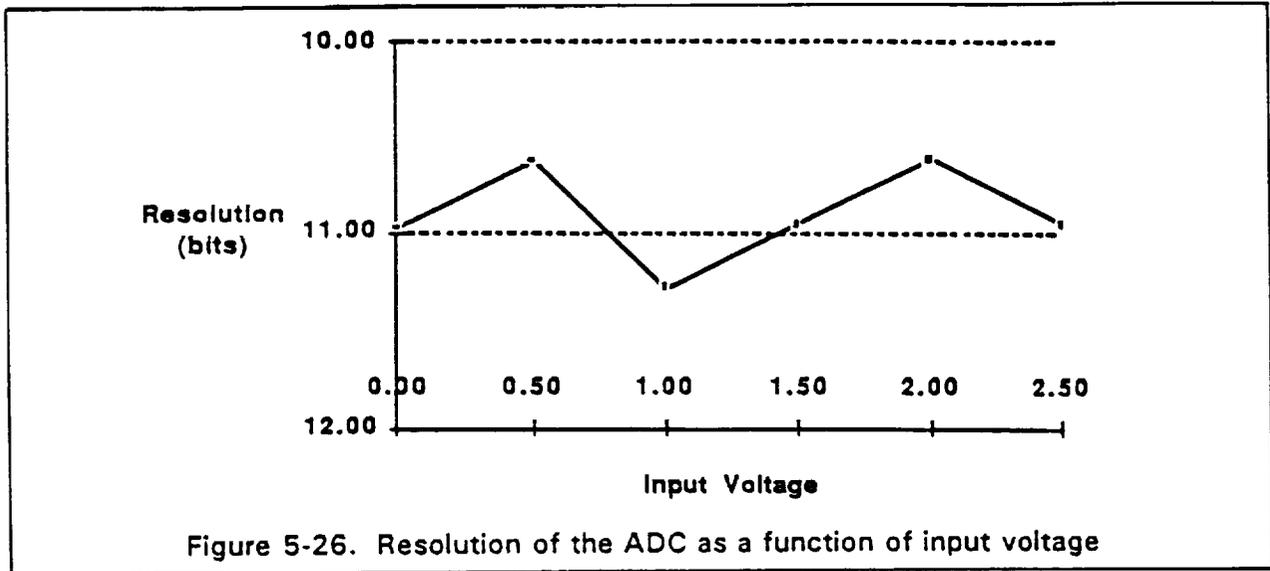
Most data sets were taken as the average of 1024 points. This amount of data is a reasonable balance between accuracy and volume of data collected. The on chip counters count in reverse order. In other words, they start with 16,532, and count down to 0. For accuracy purposes, most plots will show data from 12,500 to 16,000. When a 12 bit counter clock was used, the lowest count possible is 12,436.

Resolution was measured using a direct comparator input. An analog DC voltage was applied to this input in steps, and the output was collected 1024 times. A one sigma calculation was performed on this data, and the result in bits of resolution was calculated when compared to the full scale ramp count.

The on chip digital ramp counter was set to count 12 bits. This means that if the ADC were perfect, its one sigma value would be equal to less than 0.5. The ADC would have 12 bits of resolution. The one sigma number is an expression of the spread of the numbers in counts. Counts relate to bits by the expression $2\sigma_{\text{counts}} = 2^{\text{bits}}$, where σ_{counts} is the standard deviation in counts and bits is n bits. Bits of resolution can be calculated by subtracting bits from the maximum resolution. An example of this could be as follows: the raw data shows a one sigma number from the 1024 points collected to be four (4). The bits corresponding to four (4) counts is three (3). Subtracting the spread in bits, three (3), from the maximum resolution, 12, the resultant is nine (9) bits of resolution. Figure 5-26 shows that an ADC resolution near 11 bits results from the comparator to the output of the IC.

The lack of crosstalk or comparator switching noise can be deduced from the resolution graph. The IC has 32 channels all operating in parallel. For these tests only one channel is driven with an input voltage. The 31 channels which have no inputs all switch near zero input level. The resolution data does not suggest any degradation in the region where most of the comparators are tripping compared to a region of input voltage where only the channel of interest is switching.

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To measure the linearity of the system, 1024 data points were collected (the same points as used in the resolution measurement). The average of these points became a single data point along the linearity curve. As expected, using many data points yielded a very precise number. The deviation from a best fit straight line was 0.008% or 0.12 LSB. A best fit calculation was used as any variations in gain will be compensated for during the gain calibration operation. As can be seen in Figure 5-27, the curve is linear over nearly the entire dynamic range. The range used in the calculation was -2.5V to +1V.

5.2.3.2.4 End-to-End Results

End-to-end yield on this IC was low, approximately 15%. The low yield was driven by the low yield in the analog section of the IC. This was not the case in the two earlier IC iterations. The low yield is attributed to the large substrate currents caused by the leakage in the input protection diodes. Due to either a process variation or a mistake in the generation of the mask data, the input protection diodes appear to have a power supply short. While this problem does not prevent the external clock signals from reaching the circuitry, it does produce the large substrate currents. These currents made the IC susceptible to latchup and it is thought to have contributed to the low yield. The effect of the substrate current on TIA yield and functionality is shown in Table 5-1. The input protection diode cell functioned properly on the two previous iterations of the Pushbroom IC.

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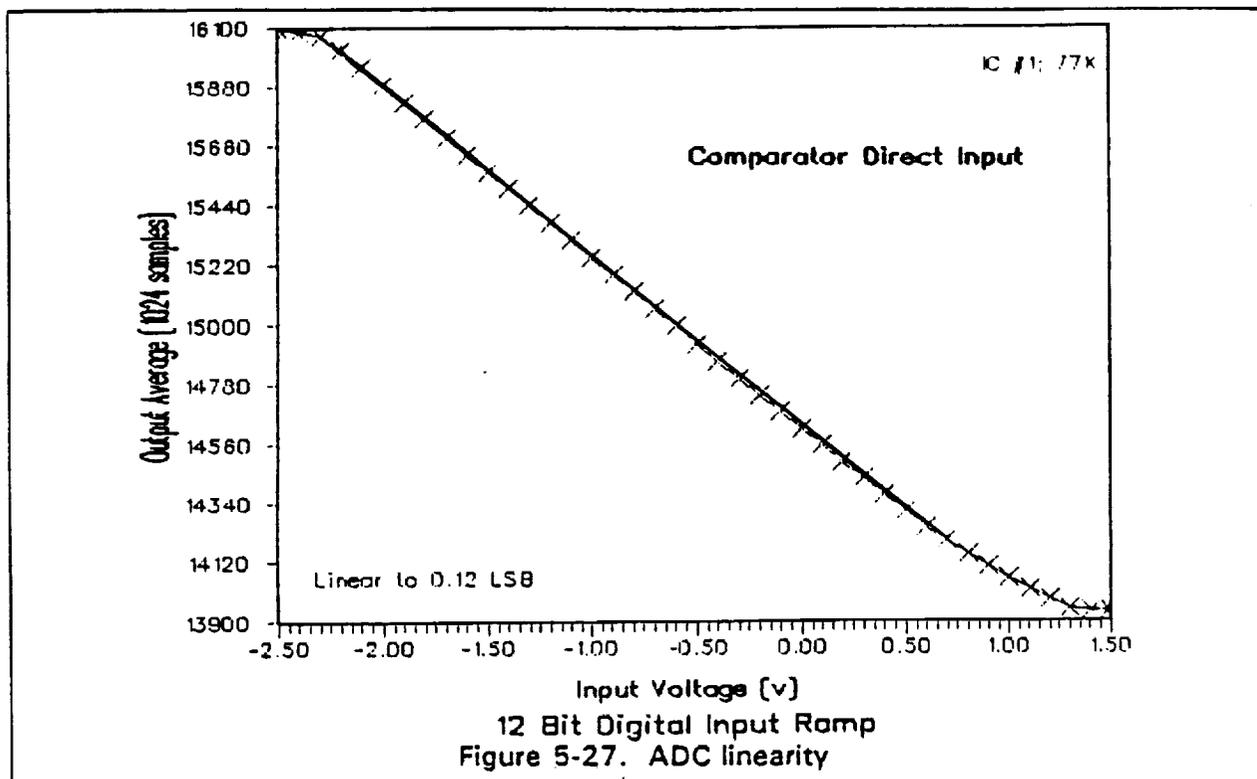
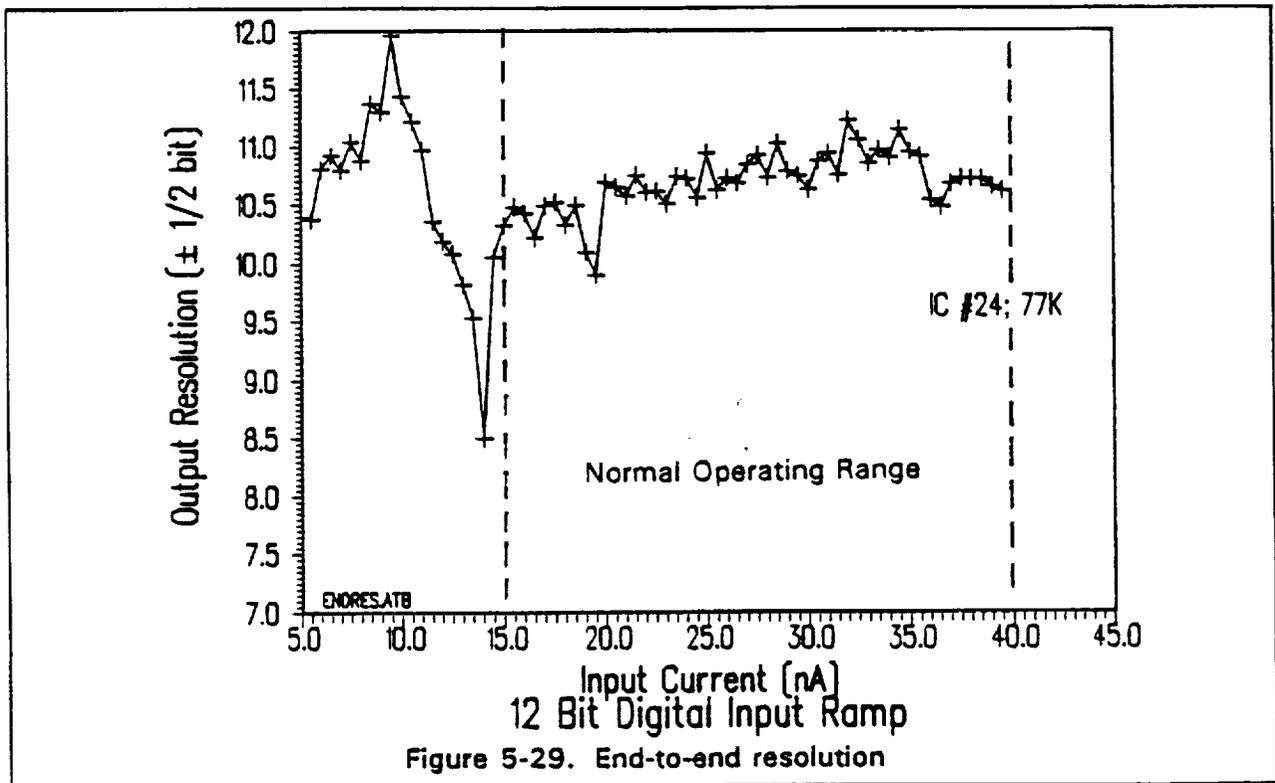
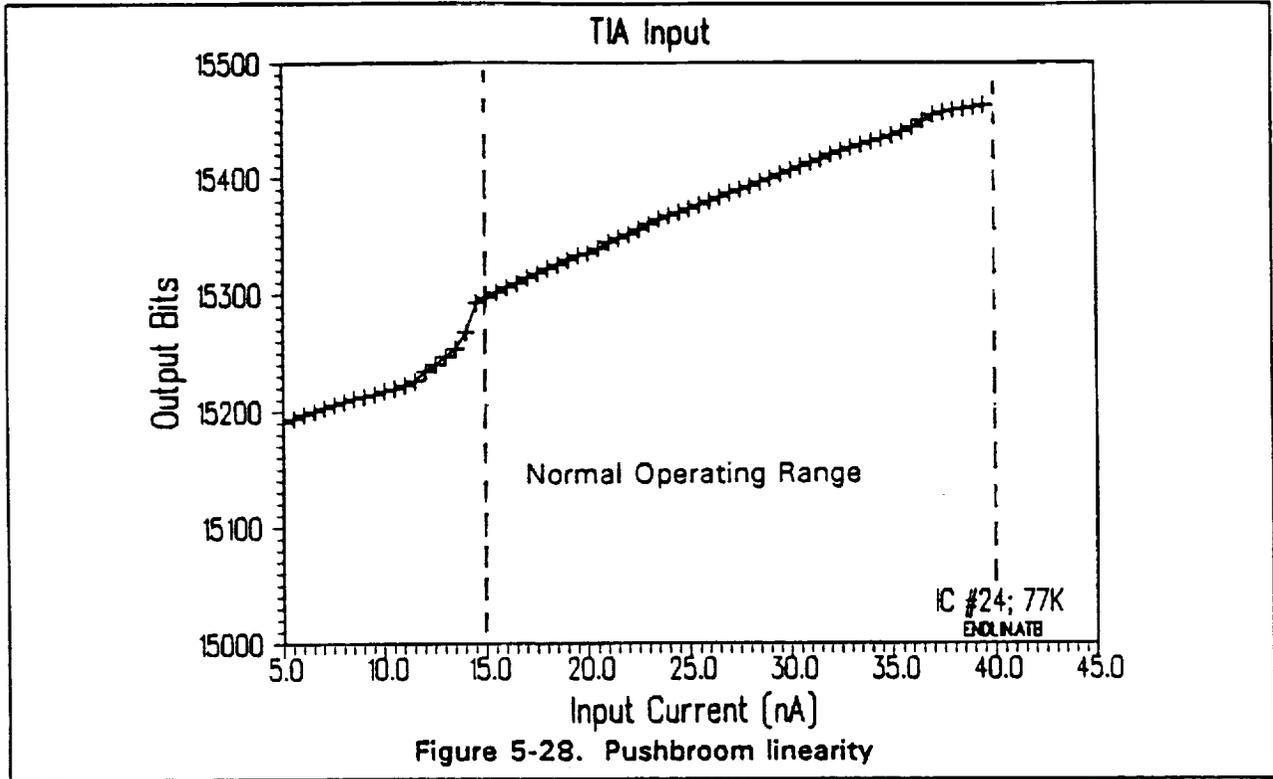


Table 5-1. Correlation between IC current and analog functionality

IC Current	Function of TIA
150 to 220 mA	TIA normal
220 to 270 mA	No Analog Operation
270 to 325 mA	No Digital TIA Timing Operation

The results of the end-to-end testing are shown in the linearity and resolution graphs in Figures 5-28 and 5-29 respectively. Note that the large deviations in linearity occur where the peaks of lower resolution also occur. Because these peaks are not evenly spaced they are unlikely to be caused by any on chip timing signals. The theories to the source of the nonlinearities are speculative at this point. The results may be a result of the limited sample tested or due to the substrate currents. TIA nonlinearities were not present to this extent in the earlier iterations. In the areas surrounding the noise peaks, the end to end resolution is between the 10 to 11 bits found in testing the analog to digital converter separately. This give some confidence that the digital section is not corrupting the analog section.

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Data contained herein are subject to the warning restrictions on the cover page of this report.

5.2.4 Electro-Optical Test

While the developed IC was not appropriate for integration with detectors, it is helpful to review E-O testing of similar ISC on-focal-plane ICs. These IC designs consisted of TIA, filter and analog MUX.

Line arrays of InSb, PbSe, and HgCdTe have been coupled to ISC on-focal-plane electronics in past programs with good success. The typical procedure followed is to compare basic vendor measured data with ISC measured data. The most convenient data to compare is the RoA product. An example of RoA data from Cincinnati Electronics Corporation for a 32 element line array of InSb is shown in Figure 5-30. This data shows an IV curve and RoA product versus temperature.

Normally the data is validated with a Hewlett Packard Parametric Analyzer. IV curves from the parametric analyzer are shown in Figure 5-31 for the same 32 element InSb line array. Typically ISC data will confirm the vendor's RoA data as shown in Figure 5-32.

Probably the most important measurement which shows the proper operation of the electronics is D^* . This is a measure of the signal to noise ratio at the output of the electronics. A typical D^* measurement with the detectors biased at zero volts is shown in Figure 5-33 for InSb detectors. At frequencies less than 1 Hz, the detector and electronics $1/f$ noise begins to increase with no similar increase in signal. Thus the D^* is reduced. Bias can play an important role in D^* measurements. Long wavelength cutoff HgCdTe are very sensitive to back bias. The more back bias the more $1/f$ noise measured. InSb is less sensitive to back bias and in some cases the D^* can actually improve due to the increased resistance at reverse bias as shown in Figure 5-34.

Other important measurements demonstrating the utility of the readout electronics are Dynamic Range and Crosstalk. Typical dynamic range and crosstalk measurements of InSb detectors are shown in Figure 5-35. This figure shows the system output in volts rms plotted against the irradiant power, the top curve is a channel with a detector input, while the bottom curve is the adjacent channel on the IC, terminated with a resistor. The ratio of the two curves give a crosstalk value of 0.42%. The knee of the upper curve is 2.7 volts rms, this yields a dynamic range of 2×10^4 when divided by the rms noise of 192 microvolts.

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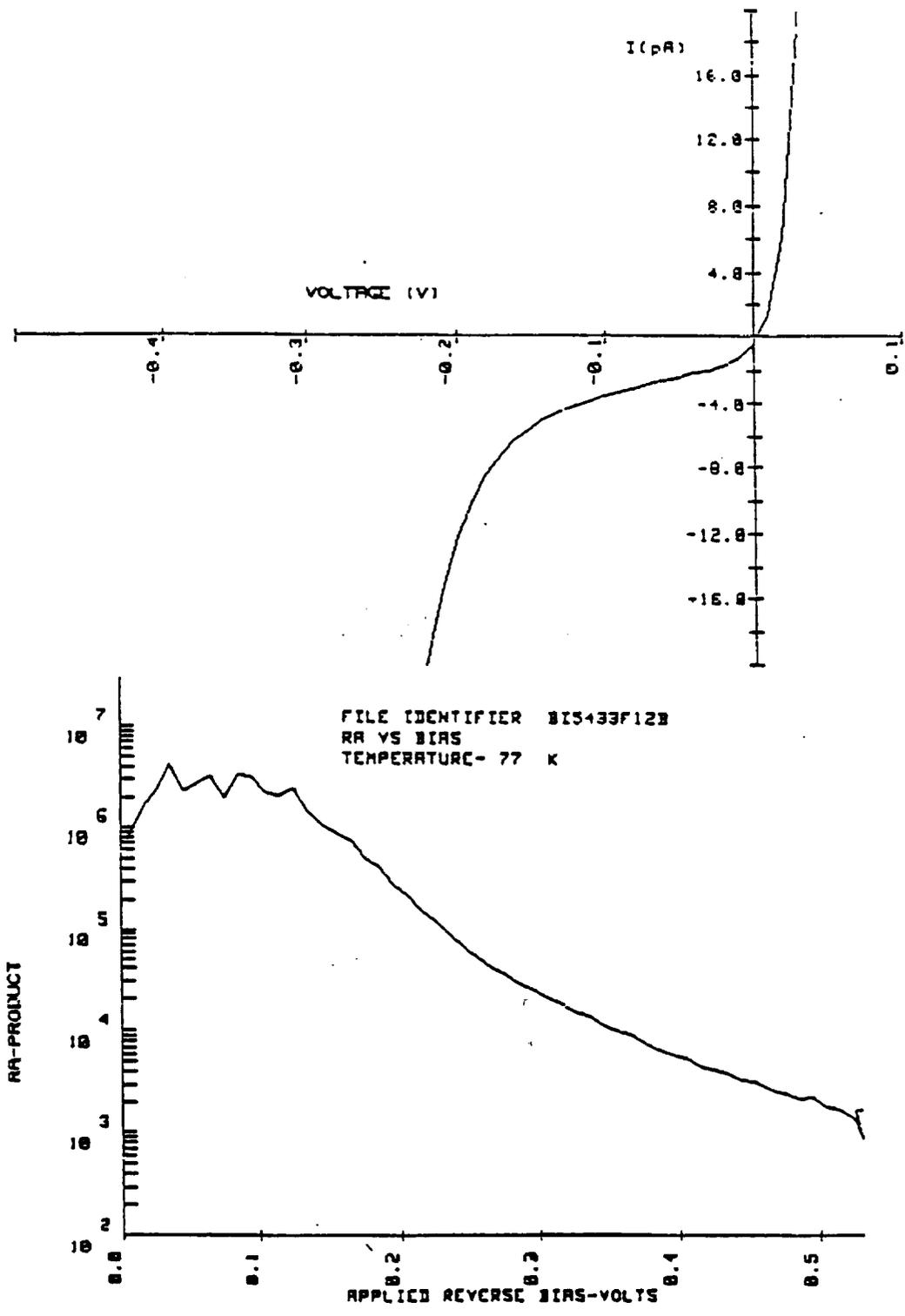
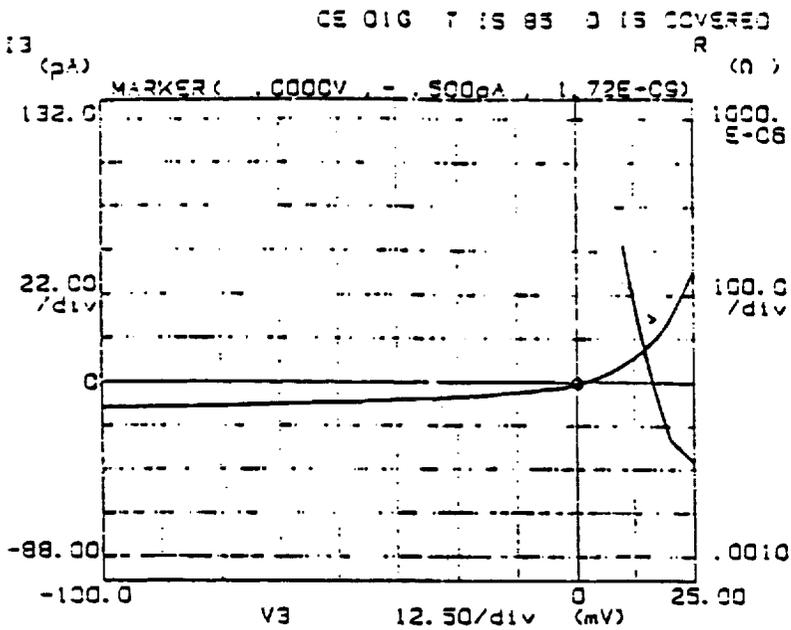


Figure 5-30. CEC I-V plot of typical InSb detector (vendor data)

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***** GRAPHICS PLOT *****

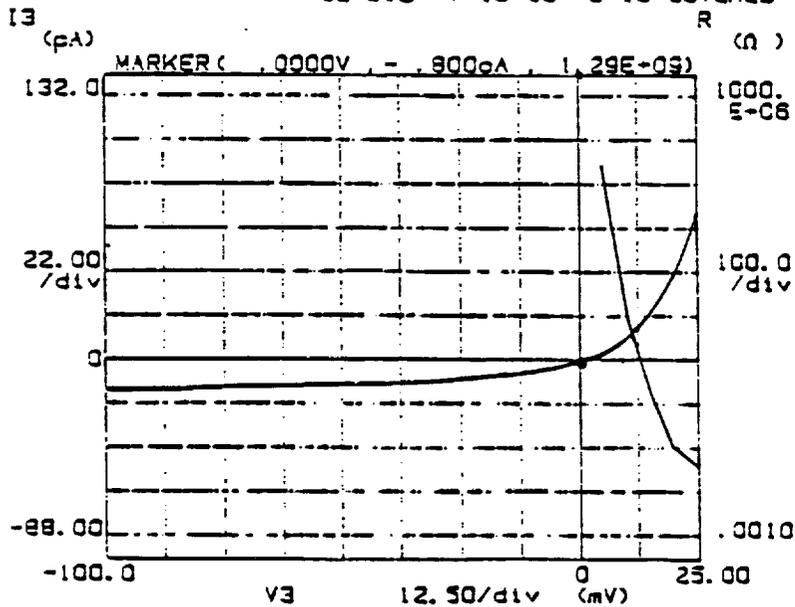


Figure 5-31. I-V plot of two typical InSb detectors (ISC measurements)

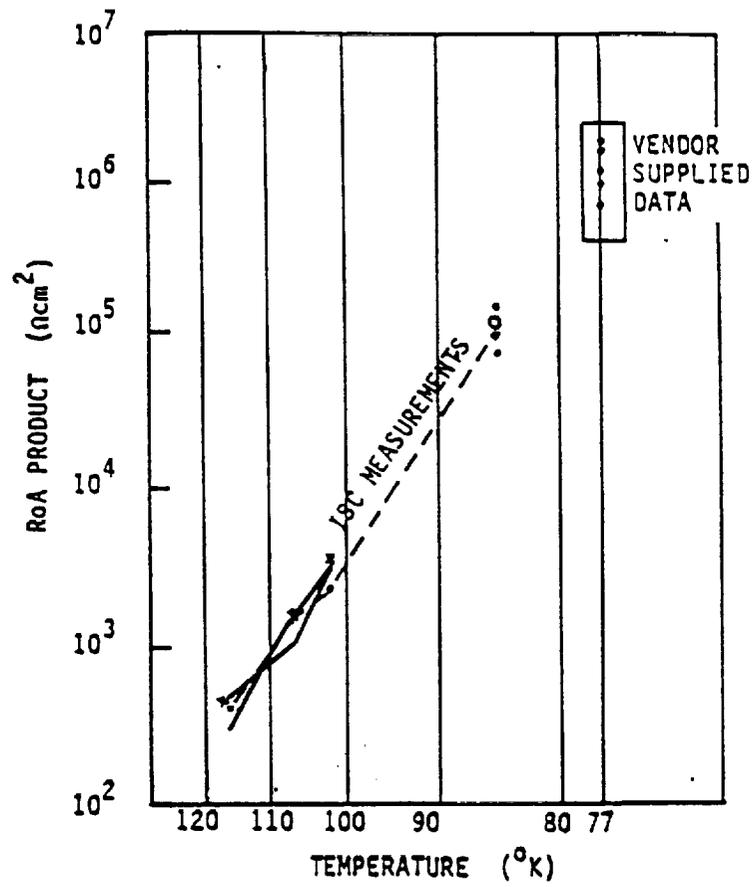


Figure 5-32. InSb RoA vs. temperature

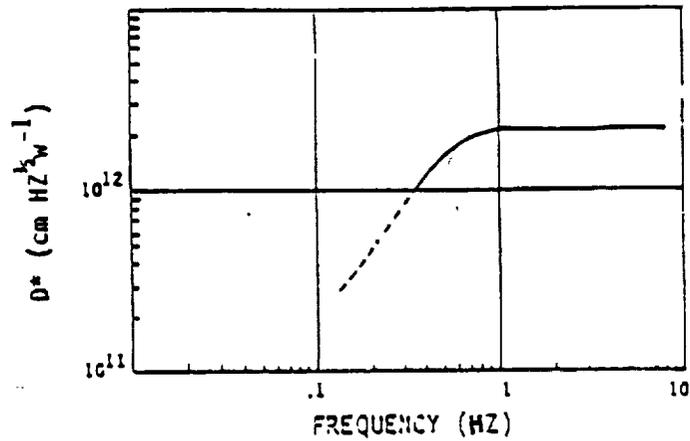


Figure 5-33. D^* vs. frequency for InSb detector 12G, @0mV bias

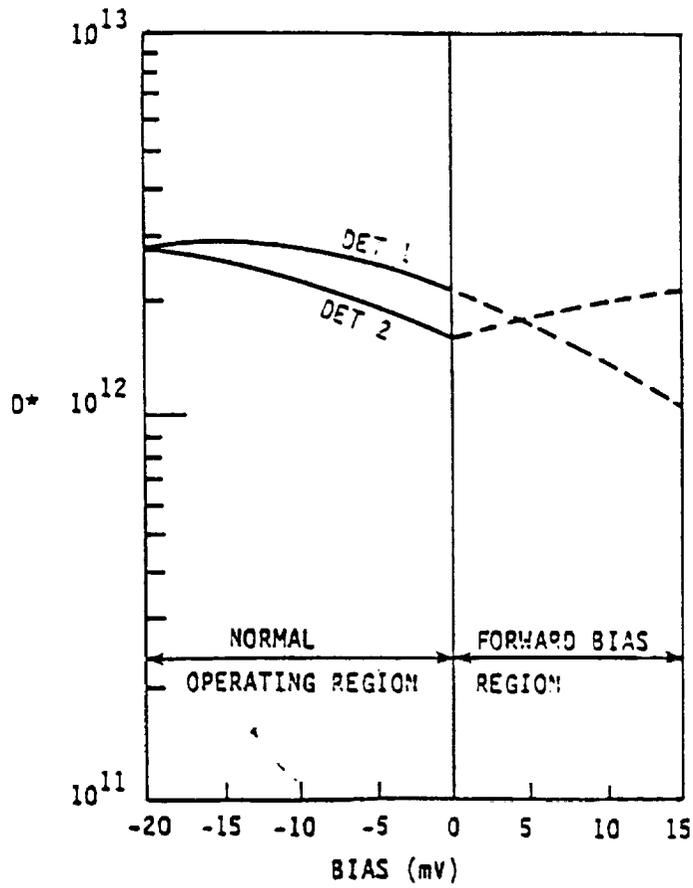


Figure 5-34. D^+ bias/InSb HYMOSS Chan 125, 114

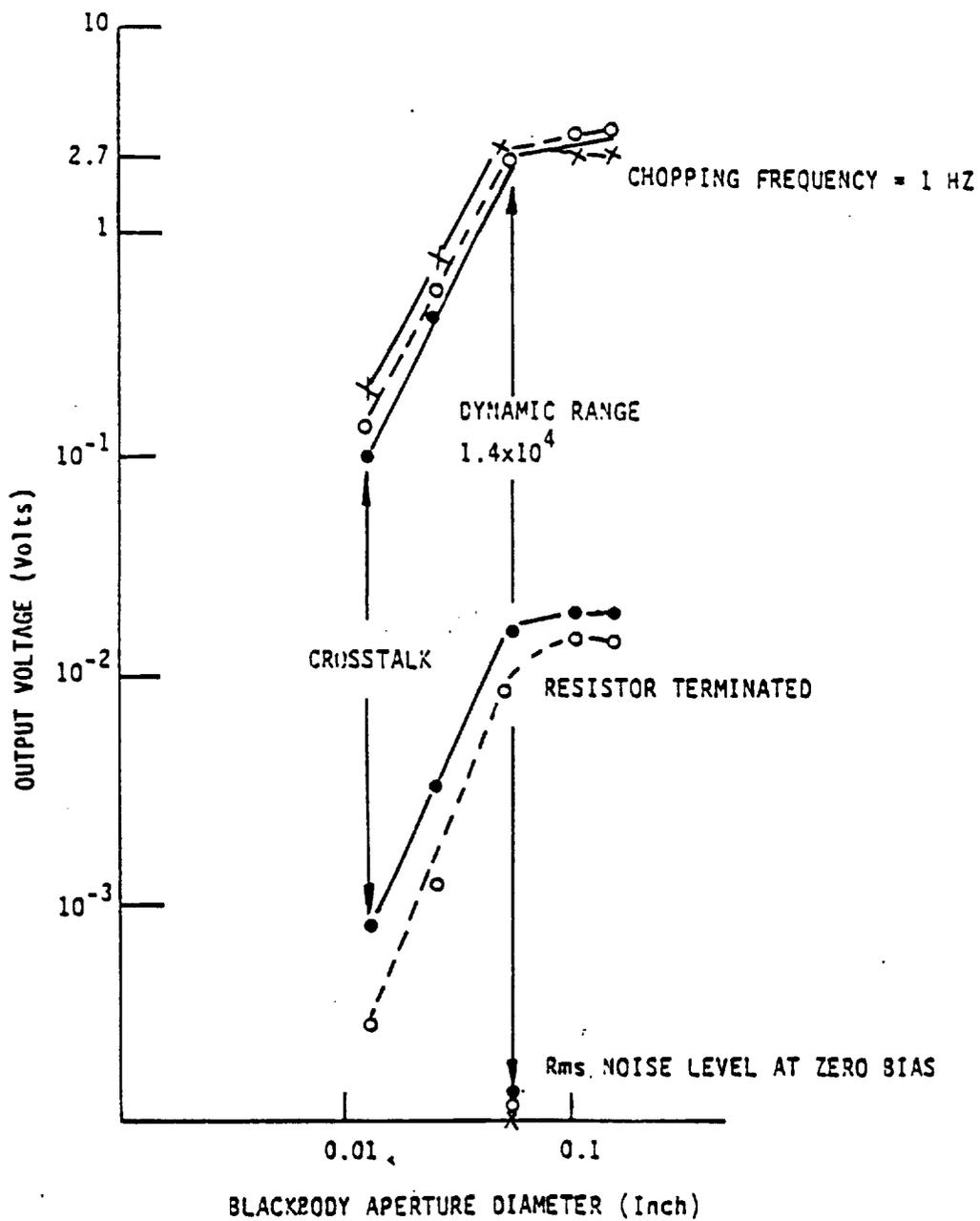


Figure 5-35. Voltage out vs. irradiance InSb

6.0 CONCLUSIONS

The goal of this program has been to establish a new standard for on focal plane signal processing. By applying the readout electronics to a Pushbroom scanner application, a set of specifications or circuit design goals were established.

ISC has extended the state of the art in on focal plane signal processing by applying a unique nonuniformity compensation algorithm in hardware together with on focal plane analog to digital conversion into an IC which approaches all the goals established at the onset of the program.

Sample rates of 1000 Hz have been demonstrated at 77° Kelvin. The upper extent of the sample rate has not been investigated at this point.

Analog to digital conversion of greater than 11 bits has been demonstrated. A limited amount of testing precluded conversion resolution greater than 12 bits. Additional testing and improved test equipment would determine the design's ultimate limits.

Gain and offset correction have been demonstrated at 8 bits and 11 bits respectively. Gain changes in the capacitive feedback TIA as effected by as little as 0.09pf capacitance changes were measured. Offset corrections down to 2 LSBs have been demonstrated.

Digital multiplexing at a rate of 32 times 1000 Hz has been demonstrated. No crosstalk was observed between 32 on chip analog-to-digital converters operating asynchronously.

Each channel of the readout electronics contained a high open loop gain p-tetrode type capacitive feedback transimpedance amplifier.

ISC continues to apply the results of this program to circuit designs focused on readout of a mosaic array of PbSe detectors for a missile seeker application. The gain and offset correction make the use of low cost lead salt detectors practical in future applications.

Serial input command word implementation has been demonstrated. Parallel output data has been demonstrated.

This complex circuit design has been challenging and not without problems. Three iterations of the IC were required to achieve the final performance described. Minor problems still exist on the IC which if corrected would further enhance the IC performance.

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APPENDIX A
Digital Interface Control Document

Data contained herein are subject to the warning restrictions on the cover page of this report.

A1.0 DIGITAL INTERFACE CONTROL DOCUMENT

The purpose of this section is to define the interface signals of the digital portion of the 32 channel Pushbroom integrated circuit. The location of the externally supplied signals are shown in Figure A1. Those signals shown in the larger font are required for operating in the IC. Those in the smaller font are either for connecting to the detector array or for debugging purposes. These signals will not normally be brought outside the dewar. The digital portion can be divided into three blocks:

- 1) Control (A2DCNTRL);
- 2) Serial Data In/Out (SERIFACE);
- 3) Converter (CAESER). Additionally, the Converter consists of two identical sections, each handling sixteen channels (PIZZA).

A1.1 Control Section

The control section contains all of the circuits necessary to implement the control and sequencing of the Pushbroom Circuit. Generally, inputs to the control section originate in the serial I/O section. Outputs from the control go to all portions of the chip. The control uses a single power supply whose positive voltage is designated VDD and whose negative voltage is designated VSS. Logic levels HIGH and LOW are to be near VDD and VSS, respectively.

CONTROL INTERFACE SIGNALS

- BITCLK** External input which drives the timing of the control section. All state changes within the control take place after the low-to-high transition of BITCLK. A complete frame of operation requires a minimum of 16 bits * 32 channels = 512 BITCLKs. After this, the control idles, waiting for FRMSYNC.
- FRMSYNC** External input which causes the control to be reset at the beginning of each frame of operation. When FRMSYNC is low, all counters and flags are kept in reset. While FRMSYNC is high, the control executes the operations of a frame as defined by the states of the other inputs.
- OFFLEN** A control signal originating in the serial I/O section which, when high (Bit 9 = 1), enables the offset latch at the end of the frame.
- TEST** A control signal originating in the serial I/O section which, when high (Bit 11 = 1), causes the frame to be shortened for testing purposes.

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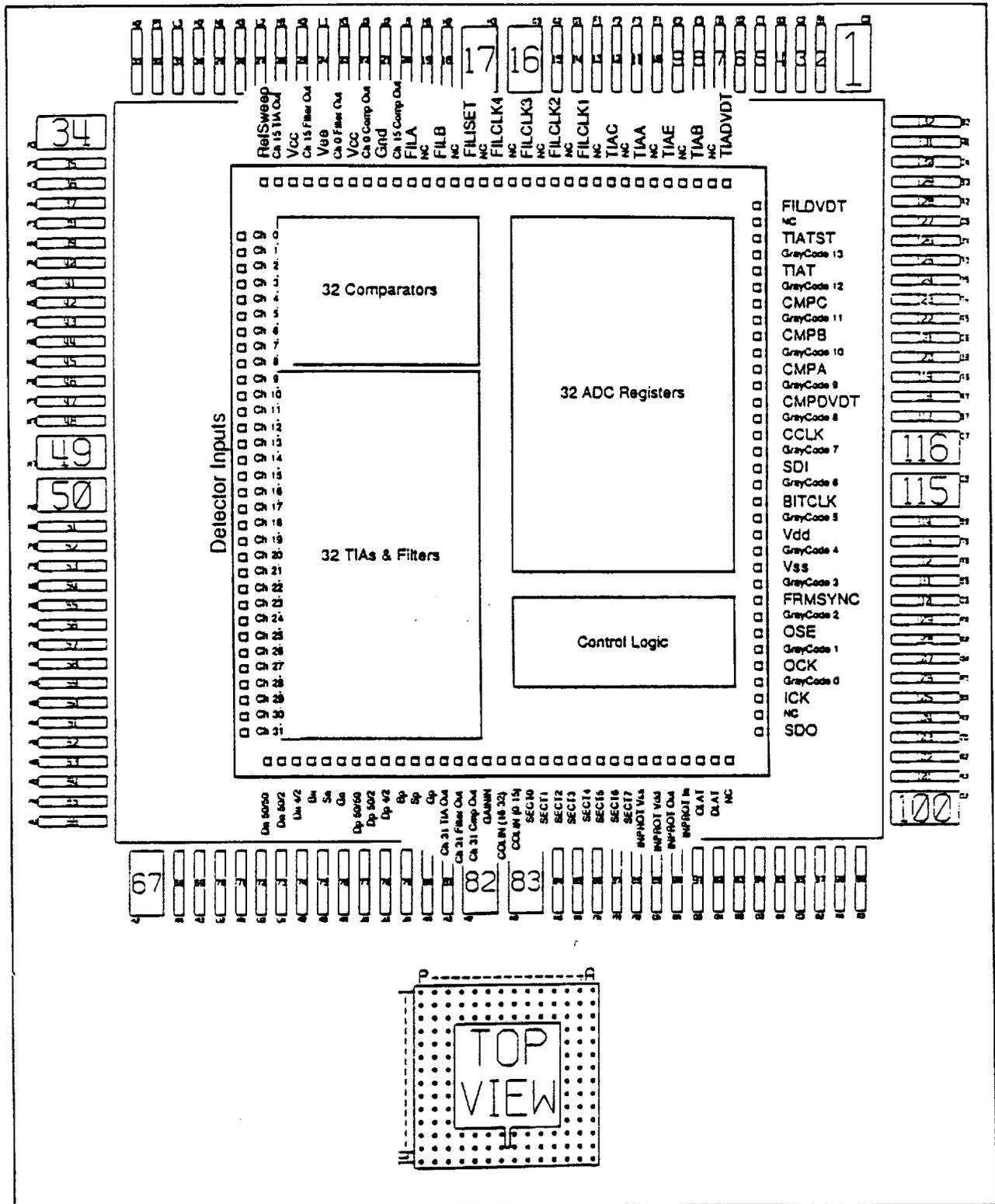


Figure A1. Pushbroom test IC I/O

Data contained herein are subject to the warning restrictions on the cover page of this report.

- RAMPHOLD A control signal originating in the serial I/O section which, when high (Bit 3 = 1), causes the digital ramp counter in the converter to be held in reset.
- ABNORML A control signal originating in the serial I/O section which, when high (Bit 13 = 1), enables TIA gain programming.
- PASSCLK A control signal originating in the serial I/O section which, when low (Bit 7 = 1), enables the progression of the TIA gain programming sequence.
- TIAINIT A control signal originating in the serial I/O section which, when high (Bit 5 = 1), causes the TIA gain initialization sequence to occur.
- RSLT The output of the most significant (sign) bit of the threshold subtractor in the serial I/O section which controls whether the gain of the TIA is to be increased or decreased during the gain setting sequence. This signal is high when the result of the DATA-OFFSET-THRESHOLD calculation is negative and, when high, causes the gain setting capacitor being addressed to be switched "in".
- HRC A control output to the serial I/O section which, when high, clears the command holding register at the end of each frame.
- DLAT A control output to the converter which, when low, causes all data latches to accept new data. This will occur at the end of each frame.
- OLAT A control output to the converter which, when low, causes all offset latches to accept new data. This will occur at the end of a frame if enabled by OFFLEN. Note that this signal is low simultaneously with DLAT which causes the data to be loaded with the same data as DLAT. In the future, it may be possible to stagger DLAT and OLAT so that frame differencing can occur (OLAT before DLAT).
- SRL0D A control output to the serial I/O section which, when high, puts the output data register in "load" mode.
- Y1, Y0 Control outputs to the converter which each select one of the two 16-channel sections as well as one of the two banks of TIAs for programming. Y0, when high, selects the section containing channels 0 - 15. Y1, when high, selects the section containing channels 16 - 31. The two signals are complementary.

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A0...A3	Control outputs to the converter which form an address in the range of 0 - 15 for the selection of data from the converter for application to the threshold subtractor as well as the selection of the TIA to be programmed. A3 is the most significant bit.
CGA	A control output to the serial I/O section which, when high, causes the command register to accept new data. This occurs at the end of each frame.
CCLR	A control output to the converter which, when high, causes the digital ramp counter to be held in reset.
Z0...Z7	Control outputs to the TIAs which, when low, cause the currently addressed TIA to accept the state of TIADATA. Z0 enables the latch associated with the most significant bit of the TIA gain setting (SECT7).
LTC	A control output to the converter which, when high, overrides the comparator inputs to the converter, effectively causing a conversion if none has yet occurred. This happens at the end of each frame so that resetting functions cannot upset the conversion data until it has been transferred to the data and offset registers.
TIADATA	A control output to the TIAs which determines whether the gain of the TIA (GAININ) is to be increased or decreased during the gain setting sequence. This signal, when low, causes the gain setting capacitor being addressed to be switched "in".

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A1.2 Serial Data I/O Section

The Serial Data I/O Section contains the circuits necessary to accept a serial and command data stream from an external source and to present this data to the control section in a fashion which allows the orderly progression of the operating algorithm. The serial data I/O section also contains the circuitry which performs the final subtraction in the DATA-minus-OFFSET-minus-THRESHOLD calculation and sends the result externally as a serial data stream. The serial data I/O section uses a single power supply whose positive voltage is designated VDD (+3V) and whose negative voltage is designated VSS (-3V). Logic levels HIGH and LOW are to be near VDD and VSS, respectively.

SERIAL DATA I/O INTERFACE SIGNALS

SDI External data input to the serial command and data registers. Data on this line must be stable while ICK makes a low-to-high transition. Data consists of 16-bit words, sent most significant bit first. If data is sent, it precedes the command. The command word bits have the following functions:

BIT 15	-	1 = Data present (MSB)
BIT 14	-	Not used
BIT 13	-	1 = Set ABNORML
BIT 12	-	Not used
BIT 11	-	1 = Set TEST
BIT 10	-	Not used
BIT 9	-	1 = Set OFFLEN
BIT 8	-	Not used
BIT 7	-	1 = Set PASSCLK Low
BIT 6	-	Not used
BIT 5	-	1 = Set TIAINIT
BIT 4	-	Not used
BIT 3	-	1 = Set HLDRAMP
BIT 2	-	Not used
BIT 1	-	1 = Immediate (Do not wait for next frame)
BIT 0	-	Not used

A command word consisting of all zeroes causes "normal" converter operation.

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ICK	External clock input for the command and data registers. Data on the SDI input is captured due to a low-to-high transition on ICK.
OSE	External input which causes the data in the command and (optionally, under control of command bit 15) data registers to be stored in the holding registers. The transfer occurs due to a low-to-high transition of OSE. Data remains in the holding register until the next OSE load, while the command is cleared to all zero at the beginning of each frame.
HRC	An input from the control section which, when high, clears the command holding register at the end of each frame.
OLD	An input from the control section (SRLOD) which, when high, puts the output data register in "load" mode. When OLD is low, the output data register operates in "shift" mode.
OCK	External clock input for the serial output data register. Data from the register will change after a low-to-high transition of OCK. If the output data register is in "load" mode, new data will be loaded into the register due to a low-to-high transition of OCK. Note, this clock must have the same frequency as the BITCLK, since the BITCLK determines which channel is being read out by the OCK.
SO...S15	The 15-bit result (S15 is not used) of the DATA-minus-OFFSET calculation from the converter. S0 is the least significant bit.
CGA	An input from the control section which, when high, causes the command register to accept new data. This occurs at the end of each frame.
SDO	The output from the serial output register. Timing of the data on SDO is supplied by OCK.
RSLT	The output of the most significant (sign) bit of the threshold subtractor which controls whether the gain of a TIA is to be increased or decreased during the gain setting sequence. This signal is high when the result of the DATA-minus-OFFSET-minus-THRESHOLD calculation is negative and, when high, causes the gain setting capacitor being addressed to be switched "in" by the control section.

Data contained herein are subject to the warning restrictions on the cover page of this report.

- ABNORML A signal to the control section which, when high, enables the TIA gain programming pulses.
- TEST A signal to the control section which, when high, causes the frame to be shortened for testing purposes.
- OFFLEN A signal to the control section which, when high, enables the offset latch at the end of the frame.
- PASSCLK A signal to the control section which, when low, enables the progression of the TIA gain programming sequence.
- TIAINIT A signal to the control section which, when high, causes the TIA gain initialization sequence to occur.
- HLDRAMP A signal to the control section (RAMPHOLD) which, when high, causes the digital ramp counter in the Converter to be held in reset. When both HLDRAMP and OFFLEN are set to 1 the offset and data registers are set to zero.

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A1.3 Converter Section

The Converter Section contains all of the functions associated with the digital side of the analog-to-digital conversion operation. These include a fourteen-bit digital ramp counter, binary-to-gray and gray-to-binary converters, comparator-controlled latches to store the ramp value at the instant when the comparator trips, as well as two sets of latches to hold this data as a data or offset value, and finally, a fourteen-bit subtractor to perform the first operation in the DATA-minus-OFFSET-minus-THRESHOLD calculation. The converter section uses a single power supply whose positive voltage is designated VDD and whose negative voltage is designated VSS. Logic levels HIGH and LOW are to be near VDD and VSS, respectively.

CONVERTER INTERFACE SIGNALS

CMPA0-CMPA15

CMPB0-CMPB15 Comparator output signals, one per channel, which, when high, allow the digital ramp to be accepted by the holding latches of the converter. When the signal goes low, the state of the digital ramp at that time is held in the latches. The CMPAx signals are associated with the SELA selector input to the converter and the CMPBx signals are associated with the SELB selector input.

DGATE An input from the control section (DLAT) which, when low, causes all data latches to accept new data from the holding latches. This will occur at the end of each frame.

OGATE An input from the control section (OLAT) which, when low, causes all offset latches to accept new data from the data latches. This will occur at the end of the frame, if enabled.

CCLK External clock input for the digital ramp counter. The counter state changes due to a low-to-high transition on CCLK. There may be a maximum of $2^{14}-1$ CCLK cycles per frame.

CCLR An input from the control section which, when high, causes the digital ramp counter to be held in reset.

SELA, SELB Inputs from the control section (Y0, Y1) which each select data from one of the two 16-channel converter sections to be applied to the threshold subtractor in the serial I/O section. For the 32-channel Pushbroom chip, SELA is connected to Y0, and SELB is connected to Y1.

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- REGADD0...REGADD3 Inputs from the control section (A0...A3) which form an address in the range of 0 - 15 for the selection of data from the converter for application to the threshold subtractor. A3 is the most significant bit.
- S0...S15 The 15-bit result (S15 is not used) of the DATA-minus-OFFSET calculation to be applied to the threshold subtractor in the serial I/O section. S0 is the least significant bit.

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A2.0 ANALOG INTERFACE SIGNALS

The purpose of this section is to define the interface signals necessary to operate the 32-channel Pushbroom integrated circuit. Figure A1 shows the location of the externally supplied signals on the 32 Channel IC.

A2.1 TIA Interface Signals

The TIA section is composed of 4 different cells or sections. They are:

- 1) P-TYPE TETRODE TIA
- 2) GAIN CONTROL LOGIC
- 3) CAPACITOR ARRAY
- 4) ROW SELECTION LOGIC

P-TYPE TETRODE TIA

The signals that interface to the TIA are defined below. There are eleven control signals, two input signals, one output signal and two power supplies. All the control signals for the TIA are generated off-focal plane except for those ending in P. The digital signals are inverted at the input pad from the buffered off-focal plane signal. All digital off-focal plane control signals are buffered by two inverters in series.

- TIAA,TIAAP Isolates amplifier FET from current source circuit. HIGH (+3V) for 66 μ sec
- TIAB,TIABP Shorts drain to gate of current source FET and releases reset on DVDT capacitor. HIGH (+3V) for 58 μ sec - each side 4 μ sec inside TIAA
- TIAC,TIACP Enables the DVDT current to the current source FET. HIGH (+3V) for 50 μ sec - each side 8 μ sec inside TIAA
- TIAE,TIAEP Resets TIA input node to +3V, shorts drain to gate of amplifier FET (auto-zero). LOW (-3V) for about 100 μ sec - goes LOW before TIAA goes HIGH by 4 μ sec and returns HIGH 30 μ sec after TIAA returns LOW
- DVDTTIA Voltage ramp used to set bias current. A positive going voltage ramp from -3V to +3V which is 66 μ sec long and starts when TIAA goes HIGH

Data contained herein are subject to the warning restrictions on the cover page of this report.

TIAT, TIATP Control signal used to enable either the detector input or a common test input to the TIA. If TIAT is positive (+3V), the detector input is enabled. If TIAT is negative (-3V), the TIATEST input is enabled. The TIATEST input is common to all 32 TIA's.

VCC +3v analog power supply.

VEE -3V analog power supply.

GAIN CONTROL LOGIC

The gain control logic consists of 8 latches which enable/disable the eight binary weighted gain capacitors in the feedback loop of the TIA. This section has fourteen interface signals that are defined below. There are eight section select signals (SECT7-SECT0), a data input (GAININ) a row select (ROWIN) and column select (COLIN) signal, the output (LATCHOUT) which enables the P-FET in the capacitor array and the two power supplies.

The section select signals are connected to the TIA control outputs from the control interface. SECT7 is connected to Z0, SECT6 to Z1, ..., SECT0 to Z7.

- SECT7 Enables the 8th data latch to input its gain capacitor in parallel with the TIA. This is enabled in series with the enable for the one TIA selected by the row and column select. A LOW (-3V) enables this latch. (This is the MSB bit.)
- SECT6 Enables the 7th data latch to input its gain capacitor in parallel with the TIA. This is enabled in series with the enable for the one TIA selected by the row and column select. A LOW (-3V) enables this latch.
- SECT5 Enables the 6th data latch to input its gain capacitor in parallel with the TIA. This is enabled in series with the enable for the one TIA selected by the row and column select. A LOW (-3V) enables this latch.
- SECT4 Enables the 5th data latch to input its gain capacitor in parallel with the TIA. This is enabled in series with the enable for the one TIA selected by the row and column select. A LOW (-3V) enables this latch.
- SECT3 Enables the 4th data latch to input its gain capacitor in parallel with the TIA. This is enabled in series with the enable for the one TIA selected by the row and column select. A LOW (-3V) enables this latch.

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SECT2 Enables the 3rd data latch to input its gain capacitor in parallel with the TIA. This is enabled in series with the enable for the one TIA selected by the row and column select. A LOW (-3V) enables this latch.

SECT1 Enables the 2nd data latch to input its gain capacitor in parallel with the TIA. This is enabled in series with the enable for the one TIA selected by the row and column select. A LOW (-3V) enables this latch.

SECT0 Enables the 1st data latch to input its gain capacitor in parallel with the TIA. This is enabled in series with the enable for the one TIA selected by the row and column select. A LOW (-3V) enables this latch. (This is the LSB bit.)

GAININ This is the data signal which allow the gain capacitor to be enabled or disabled. A LOW (-3V) enables and a HIGH (+3V) disables the gain capacitor.

COLIN This signal is NEEDED with ROWIN which produces a signal that enables the second series gate (which in conjunction with the enable from SECT7-SECT0 from above) allows each weighted capacitor to add to the feedback loop of the TIA. This signal is HIGH (+3V) to enable its section. This signal is NEEDED with ROWIN, therefore ROWIN also must be HIGH (+3V) to enable the appropriate section.

ROWIN This signal is NEEDED with COLIN which produces a signal that enables the second series gate (which in conjunction with the enable from SECT7-SECT0 from above) allows each weighted capacitor to add to the feedback loop of the TIA. This signal is HIGH (+3V) to enable its section. This signal is NEEDED with COLIN, therefore COLIN also must be HIGH (+3V) to enable the appropriate section.

LATCHOUT This signal enables/disables the series P-FET which allows each capacitor to add its binary weight to the feedback capacitor of the TIA. A LOW (-3V) at GAININ loads a LOW into the latch which ENABLES this FET.

VCC +3v analog power supply.

VEE -3V analog power supply.

Data contained herein are subject to the warning restrictions on the cover page of this report.

CAPACITOR ARRAY

The capacitor array consists of eight binary weighted capacitors. There are four interface signals. Two connections to parallel the TIA feedback capacitor at the input side (CAPPO) and the output side (TIAOUT), the control signal from the gain control latch (LATCHOUT) and VCC (sub-tie).

- CAPPO This is the common node of the 8 gain capacitors. It connects to the input side of the main feedback capacitor for the TIA, which is also the input node for the TIA.
- TIAOUT This is the common node of the 8 gain capacitors which is in series with a P-FET that is enabled/disabled under the control of the logic generated by the above defined signals.
- LATCHOUT This signal enables/disables the series P-FET which allows each capacitor to add its binary weight to the feedback capacitor of the TIA. A LOW (-3V) at GAININ loads a LOW into the latch which ENABLES this FET.
- VCC +3v analog power supply. (Used as a SUBSTRATE-TIE)

ROW SELECT LOGIC

The row select logic is physically placed in a long narrow column which is positioned at the right side of the TIA/FILTER cells. The cell is composed of sixteen NAND gates (one for each row) and each NAND is followed by an INVERTER to produce the correct polarity signal. There are twenty six interface signals:

- 1) 8 input decoder lines (4 inputs-S0,S1,S2,S3 and their inverses - SOP, S1P, S2P, S3P) that are decoded into a 1 of 16,
- 2) 16 output lines (ROWIN) and
- 3) 2 power supplies -VDD (+3V digital) and VSS (-3V digital).

S0,SOP Input decoder lines (LSB)
S1,S1P Input decoder lines
S2,S2P Input decoder lines
S4,S4P Input decoder lines (MSB)

Data contained herein are subject to the warning restrictions on the cover page of this report.

The codes for S0 to S3 are listed below with the MSB first.

The code 0000 enables ROWIN for row 0 of the TIA's

The code 0001 enables ROWIN for row 1 of the TIA's

The code 0010 enables ROWIN for row 2 of the TIA's

. . .

. . .

. . .

The code 1110 enables ROWIN for row 14 of the TIA's

The code 1111 enables ROWIN for row 15 of the TIA's

ROWIN0...ROWIN15 A HIGH (+3V) enables the respective TIA row.

VDD +3v digital power supply.

VSS -3V digital power supply.

Data contained herein are subject to the warning restrictions on the cover page of this report.

A2.2 Filter Interface Signals

The FILTER section is composed of one cell. This is a 2-pole low-pass filter with a source follower output. There are twelve interface signals to this section. Four input clocks, four controls to set up the bias current, one input, one output, and two power supplies. The four input clocks and the four controls are generated off-focal plane.

FILCLK1	Non-overlapping clock for 1st pole, used with FILCLK2. These two signals can not be HIGH (+3V) at the same time.
FILCLK2	Non-overlapping clock for 1st pole, used with FILCLK1. These two signals can not be HIGH (+3V) at the same time.
FILCLK3	Non-overlapping clock for 2nd pole, used with FILCLK4. These two signals can not be HIGH (+3V) at the same time.
FILCLK4	Non-overlapping clock for 2nd pole, used with FILCLK3. These two signals can not be HIGH (+3V) at the same time.
FILA	Controls reset FET for the DVDT capacitor. A LOW (-3V) resets the FET, should be HIGH (+3V) for the duration of the DVDTFIL ramp signal (66 μ sec long).
FILB	Controls series FET for the DVDT input to be passed to the current set FET. A HIGH (+3V) resets the FET, should go LOW (-3V) about 2 μ sec after FILA goes HIGH (+3V) and should return HIGH (+3V) about 2 μ sec before the end of the DVDTFIL ramp.
FILSET	Controls series FET for the bias voltage to be passed to the source follower stage. For reset, this signal is HIGH (+3V). To update the holding capacitor for the source follower, this signal should be pulsed LOW (-3V) for 4 μ sec. The pulse should go LOW about 12 μ sec before the end of the DVDTFIL ramp and should return HIGH about 8 μ sec before the end of the ramp.
DVDTFIL	Voltage ramp used to set bias current. A negative going voltage ramp from +3V to -3V which is 66 μ sec long and starts when TIAA goes HIGH.
FILIN	This is the input signal which comes from the output of the TIA. The output of the TIA is an integrated voltage which should range from approximately +0.5V to -2.5V.
FILOUT	This is the output signal from the filter which feeds into the comparator circuit. This source follower output will be approximately 1V higher than the TIA output signal.

Data contained herein are subject to the warning restrictions on the cover page of this report.

A2.3 Comparator Interface Signals

This circuit is a single slope comparator with an auto-zero function which captures its own offset. There are twelve interface signals to this section. Seven controls signals (A, AP, B, BP, C, CP, DVDTCMP), a reference sweep signal (REFSWEEP), an input (VIN), an output (COMPOUT) and two power supplies. All the control signals for the Comparators are generated off-focal plane except for those ending in P. The digital signals are inverted at the input pad from the buffered off-focal plane signal. All digital off-focal plane control signals are buffered by two inverters in series.

- CMPA,CMPAP** These signals are used to reset the regenerative section of the comparator circuit. For the reset mode of the comparator, Signal A should go HIGH (+3V) and AP should go LOW (-3V) for a duration of about 4 μ sec starting at 70 μ sec and ending at 74 μ sec.
- CMPB,CMPBP** These signals are used to establish the bias current and to reset one side of the input capacitor to capture the offset. Signal B should go HIGH (+3V) and BP should go LOW (-3V) for 56 μ sec starting at 10 μ sec and returning at 66 μ sec.
- CMPC,CMPCP** These signals are used to sample the input into the comparator. Signal C is also used to keep the current source FET off during operation so that no DC current is flowing. Signal C should go LOW (-3V) and CP should go HIGH (+3V) at 6 μ sec and return at 76 μ sec.
- DVDTCMP** Voltage ramp used to set bias current. A positive going voltage ramp from -3V to +3V which is 66 μ sec long and starts at 4 μ sec and ends at 70 μ sec.
- REFSWEEP** This is a very low noise reference ramp which is compared to the value of the input signal and when equal will cause the comparator to switch its output state. During reset, this signal is HIGH (+3V) from 0 μ sec to 69 μ sec, then returns LOW until it starts its positively going ramp at 100 μ sec. VIN - This is the sampled input signal from the output of the filter circuit. The value of this signal should range between +1.5V to -1.5V.
- COMPOUT** This is the comparator output signal. It is reset HIGH (+3V) during the reset mode and will go LOW (-3V) when the REFSWEEP signal equals the sampled input (VIN).
- VCC** +3v analog power supply.
- VEE** -3V analog power supply.

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