An SEU Immune Logic Family

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Abstract - A new logic family, which is immune to single event upsets, is described. Members of the logic family are capable of recovery, regardless of the shape of the upsetting event. Glitch propagation from an upset node is also blocked. Logic diagrams for an Inverter, Nor, Nand and Complex Gates are provided. The logic family can be implemented in a standard, commercial CMOS process with no additional masks. DC, transient, static power, upset recovery and layout characteristics of the new family, based on a commercial 1µm CMOS N-Well process, are described.

1 Introduction

Historically, the emphasis on Single Event Upset (SEU) research has been devoted to memory circuits [1]–[16]. Memory circuits perform vital functions in any digital system, as program stores, temporary registers and as elements of state machines which control digital circuits. An SEU, or soft error, caused by a charged particle striking a diffusion region in a memory element can prove catastrophic to an electro-mechanical system which relies upon that memory element for communication or control. Great effort has been made to find memory structures which are immune to SEUs, or at least mitigate the effects of an upsetting event. The design of SEU immune memories, whether RAM or Flip-Flops, has tended to ignore system level problems, such as an SEU of a combinational logic gate which is sampled by a memory circuit, or an upset of a control signal such as a clock line or mux select. It has been shown [17,18] that transients propagated out of or into memory elements is indeed a real problem. Research, to find general logic gate structures which are SEU immune, has been primarily limited to resistive or capacitive hardening, which are basically low pass filtering approaches [17,19,20]. Kang and Chu [21] present a logic/circuit design approach but the CMOS inverter buffers are susceptible to particle hits on the p-type diffusion. The pre-charged output node is susceptible to a particle strike on the n-type diffusion if the pulldown chain does not evaluate low. More recently [16] and [22] have presented memory cells based on logic/circuit design techniques. Only [22] addresses the issue of glitch propagation.

This paper presents a complete logic family which is SEU immune. Members of the family are constructed, using logic/circuit design techniques, to recover from an SEU, regardless of the shape of the upsetting event. It is also shown that the logic family can prevent glitch propagation from an upset node. The logic family can be implemented in a standard, commercial CMOS process without any additional processing steps. The DC,
transient, static power, upset recovery and layout characteristics of the new family, based on a commercial 1μm CMOS N-Well process, are presented in this paper.

Section 2 provides circuit configurations of members of the logic family, including an Inverter, 2-input Nand, 2-input Nor, 3-input OrNand and a 3-input AndNor. In addition, a description of the SEU recovery mechanism is presented and a means for extending this mechanism to logic structures in general is provided. DC characteristics of the SEU immune inverter are described in Section 3. Noise margins, gain characteristics and the effects of device ratioing and threshold voltages are discussed. Section 4 provides simulation results which show that the SEU recovery mechanism is independent of the duration or shape of the upsetting event. Blocking of glitch propagation is also presented. Section 5 presents circuit switching speed results based on pair-delay simulations. The effects of device ratioing on switching speed are also discussed. Static power considerations are presented in Section 6 and physical layout issues are presented in Section 7. Section 8 provides a summary and conclusions.

2 An SEU Immune Logic Family

The literature related to SEU immune combinational logic is sparse and has provided few clues as to what would be necessary to design a logic family which provides immunity to single event upsets. Whitaker has, however, provided a concise summary of fundamental concepts which can be used in the design of SEU immune memory circuits [22]. First, information must be stored in two different places. This provides a redundancy and maintains a source of uncorrupted data after an SEU. Second, feedback from the uncorrupted location of stored data must cause the lost data to recover after a particle strike. Finally, current induced by a particle hit flows from the n-type diffusion to the p-type diffusion. If a single type of transistor is used to create a memory cell then p-transistors storing a 1 cannot be upset and n-transistors storing a 0 cannot be upset. An understanding of these three concepts and close examination of the memory circuit presented in [22] has provided the key to the design of an SEU immune logic family.

Figure 1 is a transistor level logic diagram of an SEU immune inverter. The inverter consists of two transistor networks, a p-channel network and an n-channel network. All devices are enhancement mode transistors. The inverter is a two input/two output logic device with \( P_o \) driving only p-channel devices and \( N_o \) driving only n-channel devices. Node \( P_{out} \) can provide a source of 1's which cannot be upset and node \( N_{out} \) provides a source of 0's which cannot be upset. Transistor M2 is sized to be weak compared to M1 and transistor M3 is sized to be weak compared to M4. The SEU recovery mechanism works as follows. When the inputs to the inverter are 0, \( P_{out} \) and \( N_{out} \) are at a 1. In this state only \( N_{out} \) can be corrupted by an upset. If \( N_{out} \) is hit, driving the node to a 0, transistor M2 will turn on but cannot overdrive M1. \( P_{out} \) will remain at a 1, transistor M3 will remain on, pulling \( N_{out} \) back up to a 1. Conversely, if \( P_{in} \) and \( N_{in} \) are 1, \( P_{out} \) and \( N_{out} \) will be at 0 and only \( P_{out} \) can be upset. If \( P_{out} \) is hit, driving the node to a 1, transistor M3 will turn on but being weak compared to M4, \( N_{out} \) will remain pulled down to a 0.
The inverter follows the fundamental principles for SEU immunity and is therefore made SEU immune.

It is readily apparent that the inverter design concepts can be applied to any logic gate to provide SEU immunity. Figures 2, 3, 4 and 5 are the transistor level logic diagrams of a two-input NAND, two-input NOR, three-input OrNand and three-input AndNor respectively. In general, an SEU immune logic gate, implemented with this technique, requires $2n + 2$ transistors, $n$ being the number of gate inputs. In comparison, classical CMOS requires $2n$ transistors to implement a gate.

The logic family described here can provide transient suppression of an upset event as well as recovery from the upset. Networks of logic gates are connected such that $P_{out}$ only drives p-channel devices and $N_{out}$ only drives n-channel devices. If $P_{out}$ is upset, driving the node to a 1, the p-transistor being driven will be turned off momentarily without affecting the output of the following stage. If $N_{out}$ is upset, driving the node to a 0, the n-transistor being driven will be turned off momentarily without affecting the output of the following stage.

The above description obviously overlooks some of the circuit design issues which would be faced by someone wishing to design with this logic family. The family, although implemented in a CMOS process is ratioed logic, with a ratioing occurring between transistors M1 and M2 and between transistors M3 and M4. This logic family, therefore, bears a closer resemblance to NMOS than it does to CMOS. Additionally, threshold voltages become a design issue because of the enhancement mode transistors being used to pull up $N_{out}$ and to pull down $P_{out}$. Design implementation issues related to ratioing and threshold voltages are presented in the following sections.

3 Inverter DC Characteristics

The DC transfer function, \( \frac{V_{out}}{V_{in}} \), of an inverter provides several useful pieces of information about a logic family. Noise margin, inverter gain and inverter switch points are all characteristics which can be determined from a plot of $V_{out}$ versus $V_{in}$. A DC transfer function plot can also show if hysteresis is present. The SPICE [23] circuit simulator was
used to generate DC transfer functions for the SEU immune inverter described in Section
2. Results of these simulations will be presented here.

In a classical family of logic, such as NMOS, PMOS or CMOS a transistor $\beta$ is defined
to be the product of the process gain factor, $K'$, and the transistor aspect ratio, $\frac{W}{L}$. That
is $\beta_{TRAN} = K'(\frac{W}{L})$. The inverter $\beta$ is defined as the ratio of the pullup $\beta$ and the pulldown
$\beta$, or $\beta_{INV} = \frac{\beta_{pul}}{\beta_{pul}}$. The logic family described in Section 2 is a ratioed logic family. In
this case the ratioing occurs between the same type devices, and the $K'$ term cancels in
$\beta_{TRAN}$. Therefore, $\beta_{TRAN} = \frac{W}{L}$. In this case it is more useful to define transistors as
strong (M1,M4) and weak (M2,M3), instead of the traditional pullup and pulldown. To
complicate matters further, $\beta_{INV}$ now has two components, $\beta_N$ and $\beta_P$ which are not
necessarily equal. For the simulations presented here, $\beta_{INV} = \beta_N = \beta_P = \frac{\beta_{STRONG}}{\beta_{WEAK}}$.

As weak is a relative term and it was unknown what effect ratioing would have on
DC characteristics, simulations were run over 16 process parameter/voltage/temperature
cases on 15 values of $\beta_{INV}$ ranging from $\frac{1}{2}$ to $\frac{2}{1}$. Table 1 lists the 16 simulation cases. It
was necessary to run these 16 cases in order to determine what effect processing variations
would have on the SEU immune inverter. The temperature and voltage ranges cover those
required by military specifications of integrated circuits.

Once the DC simulations where performed, an inverter gain and noise margin analysis
was undertaken. It is known that ratioed logic, particularly when threshold voltage effects
are involved, has lower noise margins than non-ratioed CMOS logic. Ratioing will also
effect the gain of a logic gate. If the gain is too low a signal will die out after only a few
logic stages. In the case of the SEU immune inverter, under the WCLVLVT case, gains of 1 or

<table>
<thead>
<tr>
<th>NAME</th>
<th>PARAMETER SET</th>
<th>VOLTAGE RANGE</th>
<th>TEMP.</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCLVHT</td>
<td>SLOW N SLOW P</td>
<td>4.1V</td>
<td>140°C</td>
</tr>
<tr>
<td>WCHVHT</td>
<td>SLOW N SLOW P</td>
<td>5.5V</td>
<td>140°C</td>
</tr>
<tr>
<td>WCLVL</td>
<td>SLOW N SLOW P</td>
<td>4.1V</td>
<td>-55°C</td>
</tr>
<tr>
<td>WCHVL</td>
<td>SLOW N SLOW P</td>
<td>5.5V</td>
<td>-55°C</td>
</tr>
<tr>
<td>BCLVHT</td>
<td>FAST N FAST P</td>
<td>4.1V</td>
<td>140°C</td>
</tr>
<tr>
<td>BCHVHT</td>
<td>FAST N FAST P</td>
<td>5.5V</td>
<td>140°C</td>
</tr>
<tr>
<td>BCLVL</td>
<td>FAST N FAST P</td>
<td>4.1V</td>
<td>-55°C</td>
</tr>
<tr>
<td>BCHVL</td>
<td>FAST N FAST P</td>
<td>5.5V</td>
<td>-55°C</td>
</tr>
<tr>
<td>FNSPLVHT</td>
<td>FAST N SLOW P</td>
<td>4.1V</td>
<td>140°C</td>
</tr>
<tr>
<td>FNSPHVHT</td>
<td>FAST N SLOW P</td>
<td>5.5V</td>
<td>140°C</td>
</tr>
<tr>
<td>FNSPLVL</td>
<td>FAST N SLOW P</td>
<td>4.1V</td>
<td>-55°C</td>
</tr>
<tr>
<td>FNSPHVL</td>
<td>FAST N SLOW P</td>
<td>5.5V</td>
<td>-55°C</td>
</tr>
<tr>
<td>SNFPLVHT</td>
<td>SLOW N FAST P</td>
<td>4.1V</td>
<td>140°C</td>
</tr>
<tr>
<td>SNFPHVHT</td>
<td>SLOW N FAST P</td>
<td>5.5V</td>
<td>140°C</td>
</tr>
<tr>
<td>SNFPLVL</td>
<td>SLOW N FAST P</td>
<td>4.1V</td>
<td>-55°C</td>
</tr>
<tr>
<td>SNFPHVL</td>
<td>SLOW N FAST P</td>
<td>5.5V</td>
<td>-55°C</td>
</tr>
</tbody>
</table>

Table 1: DC Transfer Function Simulation Cases
Table 2: Noise margin and inverter gain variations

<table>
<thead>
<tr>
<th>Noise Margin Low</th>
<th>Low 0.20V $\beta_{INV} = \frac{1}{4}$ BCHVHT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>High 0.74V $\beta_{INV} = \frac{1}{2}$ FNSPVLVT</td>
</tr>
<tr>
<td>Noise Margin High</td>
<td>Low 0.30V $\beta_{INV} = \frac{1}{3}$ SNFPLVHT</td>
</tr>
<tr>
<td></td>
<td>High 1.07V $\beta_{INV} = \frac{1}{2}$ WCLVLT</td>
</tr>
<tr>
<td>Inverter Gain Variations</td>
<td>Low 1.6</td>
</tr>
<tr>
<td></td>
<td>High 11.3</td>
</tr>
</tbody>
</table>

less were attained for $\beta_{INV}$ of $\frac{1}{8}$ and $\frac{1}{4}$. Additionally negative noise margins were attained for $\beta_{INV}$ of $\frac{1}{6}$, $\frac{1}{5}$ and $\frac{1}{4}$. These $\beta$s are of course unusable in a design. Both noise margin low (immunity from positive spikes) and noise margin high (immunity from negative spikes) were analyzed for $P_{out}$ and $N_{out}$. Table 2 provides a summary of this analysis.

The inverter DC simulations eliminated 5 $\beta_{INV}$ from further consideration and showed that several more could prove marginal in a design. With the DC analysis complete, the SEU recovery ability of the inverter could be investigated. The results of this investigation are presented Section 4.

4 SEU Recovery Results

To verify the SEU recovery ability and the transient suppression characteristics of the SEU immune inverter, described in Section 2, SPICE simulations were run over the same 16 cases described in Section 3. Both $P_{out}$ and $N_{out}$ were tested. Since inverters with $\beta_{INV} < \frac{1}{4}$ where rejected during DC analysis only 10 $\beta_{INV}$, ranging from $\frac{1}{3}$ to $\frac{8}{9}$, were simulated at this stage. The SEU immunity of the logic family was shown to be independent of processing parameters, temperature or supply voltage. The error recovery mechanism is provided by the logical feedback of transistors M2 and M3 and the ratioing of transistor strengths. The recovery mechanism is also not dependent upon the wave shape of the current pulse which upsets the node.

The simulation circuit used to test the recovery mechanism consisted of a chain of 3 identical inverters. No parasitic capacitance other than self-capacitance and that seen at the inputs to the next stage was added to the circuit. The inputs to the first inverter were set up to the proper initial conditions. A voltage controlled current source was connected to the node to be upset. This provided a means to inject charge into the node without attaching any parasitic capacitance. Additionally an ideal diode, emulating the parameter dependent source/drain to substrate/well diodes, was attached to the node. This diode did not create any additional capacitance. A current pulse, with a duration of 10ns, and a magnitude sufficient to forward bias the source/drain diode, was applied to the node. The 10ns pulse width was chosen because it was longer than the propagation delay.
2.3.6

delay through the inverter as well as being longer than a real SEU. Recovery from an SEU was shown to be independent of parameter/voltage/temperature cases. Although all $\beta_{INV}$ cases recovered, SEU recovery time was dependent upon $\beta_{INV}$. Faster recovery times were noted for $\beta_{INV} > \frac{1}{2}$.

Besides being able to recover from an upset event an SEU immune logic family must be able to suppress the propagation of transients out of the upset node. Due to the P-net driving P-net and N-net driving N-net configuration described in Section 2, the logic family presented in this paper should be able to suppress glitches caused by an SEU. SPICE simulations verified that this is the case. The simulation circuit used to test transient suppression was the same as that used for testing upset recovery. In this case, however, a 1ns current pulse was applied to the upset node. This pulse duration is closer to what one would expect from a real SEU. Transient suppression was measured at the output of the inverter being driven by the upset node. If the magnitude of the glitch on this output was within the noise margin, for the parameter/voltage/temperature case and $\beta_{INV}$ being simulated, the transient was considered suppressed. Results of these simulations indicated that transient suppression was dependent upon simulation cases as well as $\beta_{INV}$. In fact, any $\beta_{INV} \leq \frac{1}{4}$ was rejected as unusable, in a design, due to poor transient suppression abilities.

The seven ratios with $\beta_{INV} > 1$ remaining after the SEU recovery/transient suppression simulations were subjected to a transient analysis to determine switching speeds of the SEU immune logic family. These results are presented in Section 5.

5 Transient Analysis of the SEU Immune Inverter

With a modern CMOS process it is possible to attain inverter gate delays of 1ns or less. For an SEU immune logic family to be of interest to the VLSI design community the inverter described in Section 2 should have a gate delay at least in the ns range. Transient analysis simulations show that this is possible. SPICE simulations were run over the same 16 cases described in Sections 3 and 4. The simulation circuit was a chain of 7 identical inverters. Each inverter was loaded with a 1000pF linear capacitor. This large capacitor swamped out any voltage dependent capacitors associated with transistor source/drain regions as well as gate capacitances seen by the inverter outputs. The first inverter in the chain was excited by a step function, and pair delay information was extracted from the output. A pair delay is defined to be the delay, measured from mid-point to mid-point of the voltage swing, through a pair of inverters. This delay contains both a time delay rise and a time delay fall. In non-ratioed logic, such as classical CMOS, inverters are designed to have equal rise and fall times. In a ratioed logic family it is not always possible to design for equal rise and fall times, therefore pair delay information is more useful. In this case 4 pair delay values were computed, delay from a rising edge and from a falling edge, for both $F_{out}$ and $N_{out}$. The longest delay of these was chosen as the worst case delay. At the outset it was unknown which parameter/voltage/temperature case would prove to be that of worst case speed. In classical CMOS it would be WCLVHT. For this logic family
Pairdelay Chart \((C_{\text{load}} = 1000pF, \text{Delay} = \mu s)\)

<table>
<thead>
<tr>
<th>(\beta_{\text{INV}})</th>
<th>2.4(\mu m)</th>
<th>4.8(\mu m)</th>
<th>7.2(\mu m)</th>
<th>9.6(\mu m)</th>
<th>12.0(\mu m)</th>
<th>14.4(\mu m)</th>
<th>16.8(\mu m)</th>
<th>19.2(\mu m)</th>
<th>21.6(\mu m)</th>
<th>24.0(\mu m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>143</td>
<td>54</td>
<td>34</td>
<td>25</td>
<td>19</td>
<td>16</td>
<td>14</td>
<td>12</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>(2)</td>
<td>107</td>
<td>41</td>
<td>26</td>
<td>19</td>
<td>15</td>
<td>12</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>(3)</td>
<td>90</td>
<td>35</td>
<td>22</td>
<td>16</td>
<td>13</td>
<td>11</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>(4)</td>
<td>82</td>
<td>32</td>
<td>20</td>
<td>15</td>
<td>12</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>(5)</td>
<td>75</td>
<td>29</td>
<td>18</td>
<td>13</td>
<td>11</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>(6)</td>
<td>70</td>
<td>27</td>
<td>17</td>
<td>12</td>
<td>10</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>(7)</td>
<td>66</td>
<td>25</td>
<td>16</td>
<td>12</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 3: Pair delay results.

it also proved to be WCLVHT. Simulations were run on all of the surviving \(\beta_{\text{INV}}\)s, with ten different transistor widths, ranging from 2.4\(\mu m\) to 24.0\(\mu m\). Pair delay charts for each \(\beta_{\text{INV}}\) were constructed. A table of pair delay versus transistor width is provided in Table 3. As expected, because delay is inversely proportional to width, pair delays decrease as a function of transistor width. Speed, another useful design measure, is the linear function, \(\frac{1}{\text{delay}}\).

From the results of the SEU recovery ability, described in Section 4, and the pair delay information in this section, it would seem that \(\beta_{\text{INV}} = \infty\) would be the best choice. However, as in all engineering endeavors there is a practical limit to the choice of \(\beta_{\text{INV}}\). Both power dissipation and physical layout constraints must be considered. Section 6 and Section 7 will discuss these issues, as they relate to the SEU immune inverter.

### 6 Static Power

In Section 2 it was stated that the SEU logic family presented in this paper was, in some regards, more closely related to NMOS than CMOS. Due to the ratioing between the normal transistors and the feedback transistors, and the effects of threshold voltages, this logic family dissipates static power. SPICE simulations were run, with the same cases described in previous sections, to characterize this power dissipation, and the effects of \(\beta_{\text{INV}}\) on it. As expected, power dissipation increased with \(\beta_{\text{INV}}\). The power dissipation was worst under BCHVLT conditions for both input high and input low conditions. Static power consumption may place a limit on the number of SEU immune gates which can be placed on an integrated circuit.

### 7 Physical Layout

The SEU immune logic family presented in this paper can be implemented in a standard CMOS process, using standard layout design rules. The family does, however, have characteristics which make physical layout of the family different than a classical CMOS layout. A classical inverter, for example, requires a minimum of two lines, the input and the output, crossing the well boundary. The SEU immune inverter has two separate inputs, \(P_{\text{in}}\) and \(P_{\text{out}}\).
and \( N_{\text{out}} \), but they need not cross the well boundary. However, there are two feedback lines which must cross. Additionally, both VDD and VSS are required for both n-transistors and p-transistors, whereas a classical inverter only requires one power supply for each transistor type. The signal connections are more complicated in the SEU immune logic family than in classical CMOS. In addition, the SEU immune logic family has two more transistors than does classical CMOS. One should, therefore, expect that layout densities would be less for the SEU immune logic family. As designers acquire more experience with layout considerations the attained densities should improve.

8 Summary and Conclusions

This paper presented a complete logic family which is SEU immune. Members of the family are constructed, using logic/circuit design techniques, to recover from an SEU, regardless of the shape of the upsetting event. It was also shown that the logic family can prevent glitch propagation from an upset node. The logic family can be implemented in a standard, commercial CMOS process without any additional processing steps. The DC, transient, static power, upset recovery and layout characteristics of the new family, based on a commercial 1\( \mu \)m CMOS N-Well process, were presented.

This logic family makes the design of completely SEU immune integrated circuits possible. The simulation results presented in this paper should prove useful to designers who need to implement SEU immune systems.

A test chip, which will be used to verify the simulations presented here, is currently being defined.

Acknowledgement

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References


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Figure 2: SEU Immune two-input NAND.
Figure 3: SEU Immune two-input NOR.

Figure 4: SEU Immune three-input OrNand.

Figure 5: SEU Immune three-input AndNor