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Smart Vision Chips: An Overview

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1. Four Working Analog VLSI Vision Chips
 - (a) Time-Derivative Retina (Delbrück & Mead)
 - (b) Zero-Crossing Chip (Bair & Koch)
 - (c) Resistive Fuse (Harris & Koch)
 - (d) Figure-Ground Chip (Luo, Koch & Mathur)
2. Work in Progress
3. Conceptual and Practical Lessons Learned

Silicon Retina that Computes a Pure Temporal Derivative

T. Delbrück and C. Mead, 1991

- Array of 68 by 43 adaptive, high-gain, logarithmic photoreceptors, implemented in analog CMOS.
- No spatial interactions.
- Array has low offsets and consumes about 4 *mW* power.
- Array has very **small** fill-factor ($< 3\%$).

1-D Chip that Computes Edges

W. Bair and C. Koch, 1991

- 64 pixel, logarithmic photoreceptors in analog CMOS.
- Each resistive grid implements low-pass filter $\tilde{G}(\omega) = \frac{1}{1+\lambda\omega^2}$. where λ is given by the resistances.
- Chip computes thresholded zero-crossing between two resistive networks (implementing a band-pass filter).
- Output is 63 bit word, indicating presence of edge between adjacent pixels.

Smoothing 2-D Data in the Presence of Discontinuities

J. Harris, C. Koch and J. Luo, 1990

- Algorithmic justification: If values of some variable (for example, depth, hue, intensity) between two adjacent pixels is similar, then smooth away the difference (since it is most likely caused by unavoidable image noise). If the difference is above a threshold, then preserve it, since it is most likely caused by a **discontinuity** between the two locations.
- These constraints can be implemented within a single two-terminal device, the **resistive fuse**.
- Device has nonlinear I-V relationship, similar to an electrical fuse.
- Deterministic annealing can be carried out by dynamically adjusting the I-V relationship.
- Performance of a 20 by 20 pixel analog CMOS chip is shown.

Segregating a “Figure” from “Ground”

J. Luo, C. Koch and B. Mathur 1992

- 48 by 48 pixel resistive grid with configurable switches in analog CMOS.
- Off-chip circuitry detects—possibly incomplete—edges and sets switches appropriately.
- Voltage inside one (or more) figures clearly demarcates them from surrounding pixels.
- Resistive network has natural boundary completion property.

Work in Progress: Computing Motion

- Differential methods to compute velocity (e.g. $v = -I_t/I_x$) are numerically ill-conditioned and require very accurate components.
- Correlation methods to estimate velocity (e.g. $I(x, t) \times I(x + \Delta x, t + \Delta t)$) are robust but expensive in VLSI.
- Computing velocity in the temporal pulse domain appears very promising (Sarpeshkar, Bair and Koch, 1993).
- Special-purpose analog motion sensors can be built for estimating **time-to-contact**, **observer heading**, **discontinuities in the optical flow** and other qualitative features of the optical flow field.
- Exploiting Green's theorem

$$\int_A \nabla \cdot \mathbf{V}(x, y) dx dy = \int_C \mathbf{V} \cdot \mathbf{n} ds$$

to compute τ (time-to-collision) in a very robust manner (using a single sensor).

Work in Progress: Neuromorphic Systems

- Carver Mead emphasizes analog VLSI as a medium to model and understand the nervous system (**synthetic neurobiology**).
- Mahowald and Douglas (1991) have successfully built **pyramidal cells** in analog CMOS, including dendritic trees, EPSPs and IPSPs and nonlinear membrane conductances.
- Koch, Douglas, Sejnowski and Lisberger are involved in long-term project to build a complete **oculo-motor system** (including two retinae on movable platform, superior colliculus, brain stem nucleus for eye plant, and cortical areas) based upon the visual system of primates.

What Lessons Have We Learned

- Conception, design and fabrication of smart vision chips **must** go hand-in-hand with the design of the appropriate vision algorithms.
- It is crucial to understand what types of computations map naturally onto analog hardware and which ones are better suited to *Turing universal* digital machines (e.g. motion analysis).
- Important to integrate adaptation and learning abilities at all levels of the circuitry (from photoreceptors to output).

What Should We Do

- Principal limitation of today's circuits is **not** small array size ($< 100 \times 100$ pixels) but lack of further on-chip processing power.
- Do not emphasize development of very costly basic fabrication and circuit technology at the expense of inexpensive algorithmic development and implementation.
- Development of interchip communication protocols (e.g. Mahowald and Mead's event-driven addressing scheme).
- Design not just smart add-on's, but complete, autonomous systems.

