FPGA Based Reconfigurable ATM Switch Test Bed

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Network Performance Evaluation

- Seeking optimal configuration
- Difficult in general:
  - performance effected by switch architecture, network topology, protocols, incoming traffic patterns etc.
  - system characterized by many stochastic processes
Traditional Approach

- Theoretical model with closed-form solution
  - extremely simple model; e.g., M/M/1 queue
- Theoretical model without closed-form solution
  - with an analytical procedure to obtain solution
  - more realistic, but still with lots of assumptions and approximations
- Prototyping physical system
  - expensive, inflexible
  - technology may not exist yet

Software simulation

- can model at any level of abstraction
- require several orders of magnitude of CPU clocks to simulate 1 real-time clock
- e.g., experience from an earlier ATM switch project
  » it takes 0.1 to 1 m sec to simulate the operation of one cell (using BoNES Designer Software in Sun Sparc II)
  » it will require more than 100 days to measure a buffer with a cell loss probability of $10^{-7}$
# Hardware Emulation

- Use hardware to accelerate simulation
- Construct customized circuit to model various network components
- Recent advances in FPGA (Field Programmable Gate Array) technology make this possible
  - FPGA: "generic logic" that can be configured to different functions by loading different files
  - a chip can accommodate circuit with 100,000 gates
  - synthesis CAD software simplifies implementation

# Test Bed Highlights

- Model the operation of an ATM-like switch based network in an FPGA board
- Model data-link level functionality (such as buffer management, congestion control etc.)
- Use a host PC to control and monitor the operation of the FPGA board
- Most design, synthesis, and simulation are based on industrial standard VHDL language
- Design goal: modular, scalable, reconfigurable
Design Environment

Test Bed Architecture
Abstract Sheared-Memory Switch

- Model after a shared-memory ATM switch
- Process only the cell header
- Perform only data-link level functionality
- Include control circuit, FIFO buffer and status circuit.
- Incorporate three buffer management schemes: complete sharing, complete partition, and sharing with maximal queue length

Detailed Switch Diagram
Traffic Generator

- Cell format:
  - header only (destination port etc.)

- Traffic generator
  - Cell trigger generator
    » deterministic arrival
    » Poisson arrival
    » Markov modulated Poisson arrival
  - Cell destination port generator
    » uniformly distributed
    » unbalanced

Data Collection Circuit and User Interface

- Data collection circuit
  - gather statistics on total cell arrival, cell loss due to global buffer overflow, and cell loss due to FIFO overflow

- User interface
  - Hardware: PC ISA bus interface in FPGA board; all registers of test bed can be accesses as PC’s memory
  - Software: C routines to download configuration file to the FPGA board, to set up the test bed, to monitor the board operation and to retrieve collected data
Initial Results

- Test bed was designed to study cell loss probability of various memory management schemes
- It was fitted into one 100,000-gate FPGA board
- Performance
  - max clock about 15 MHz
  - can emulate about 3 M cell arrivals per sec (1.2 G bits per sec)
  - 5.5 min to emulate $10^9$ cell arrivals
- Emulation increases speed by a factor of $10^3$ to $10^5$

Example: System Load vs Cell Loss Probability w/ Different Buffer Sizes in an 8x8 Switch
Conclusions

- Advances in FPGA make hardware emulation feasible for performance evaluation
- Hardware emulation can provide several orders of magnitude speed-up over software simulation
- Due to the complexity of hardware synthesis process, development in emulation is much more difficult than simulation and requires knowledge in both networks and digital design