K–Band Power Embedded Transmission Line (ETL) MMIC Amplifiers for Satellite Communication Applications

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Abstract

The design, fabrication, and performance of K-band high-efficiency, linear power pHEMT amplifiers implemented in Embedded Transmission Line (ETL) MMIC configuration with unthinned GaAs substrate and topside grounding are reported. A three-stage amplifier achieved a power-added efficiency of 40.5% with 264 mW output at 20.2 GHz. The linear gain is 28.5 dB with 1-dB gain compression output power of 200 mW and 31% power-added efficiency. The carrier-to-third-order intermodulation ratio is - 20 dBc at the 1-dB compression point. A RF functional yield of more than 90% has been achieved.

Summary

Emerging mobile satellite communication systems require MMIC components that are efficient, small-size, and suitable for low-cost antenna array implementations. Our Embedded Transmission Line (ETL) MMIC concept first reported in [1] utilizes matching circuits with transmission lines and lumped passive components (resistors, series/shunt capacitors, and spiral inductors) embedded in a low-K dielectric (polyimide) medium coated over the active devices. The quasi-hermetic nature of the ETL MMIC simplifies the packaging requirement. Highly uniform performance from a K-band low-noise amplifier design and state-of-the-art noise performance from a Ka-band MMIC design were reported [2]. In this paper, we further report the development of power ETL MMIC amplifiers suitable for spaceborne phased array antenna implementation using flip-chip mounting technique in multilayer circuits [3]. AlGaAs/InGaAs on GaAs pseudomorphic high electron mobility transistor (pHEMT) with 0.25 μm long T-gate was used. The ETL MMIC design is based on 25 μm thick polyimide and 25-mil thick GaAs substrate. No backside processing such as substrate thinning, plating, and through-substrate vias is required. This greatly simplifies the processing steps and reduces the production cost. Figure 1 shows the dual-channel K-band three-stage ETL MMIC power amplifiers with a chip size of 100 × 180 mils. Two identical amplifiers are laid out side by side on the same chip to simplify array packaging. Several designs with different device sizes were used to meet the different power element requirement of the array. The circuit designs are such that the same RF I/O’s and bias pad locations are used to simplify the module routing requirements. The top picture shows the top-side ground with RF I/O’s and bias pads. The bottom picture shows the underlying circuitry with the top 25-μm thick polyimide layer removed. With the exception of RF input/output pads and gate/drain pads, a solid ground plane is available for ease of connecting to other components without bondwires.

One three-stage amplifier design has cascaded 100 μm/300 μm/600 μm gate width pHEMTs. Figure 2 shows a SEM photograph of the output 600 μm device prior to the polyimide coating. The device size ratio was chosen, based on trade-off among gain, efficiency, power, and intermodulation distortion requirements. Optimum source and load impedance from large-signal load-pull and third-order intermodulation load-pull were used in the amplifier designs. The on-chip bias network allows the use of a single gate voltage and a single drain voltage for power supply requirement simplification in modules. On-wafer small-signal and large-signal characterizations, including two-tone distortion were performed on both discrete devices and MMIC amplifiers. Since the devices and MMICs were not flipped (i.e., topside ground with the heat flows through the thick GaAs substrate), even better performance than that reported here with the on-wafer characterization should be achievable, once the wafer is diced and MMIC flip-chip mounted.
Figure 3 shows the small-signal gain-frequency response of four amplifiers with each taken from four different 3-inch wafers biased at the same gate and drain voltages. It is seen that the response is very uniform over the design bandwidth of 19 GHz to 22 GHz. With a drain voltage of 3 V, the gain is 27 to 30 dB. Figure 4 shows the power performance of the amplifier as a function of input drive level. The linear gain is nearly 30 dB (at 19 GHz) with a power-added efficiency of 40.5% with 264 mW output at 20.2 GHz. The 1-dB gain compression output power is 200 mW with 31% PAE. It is to be noted that these excellent results can be achieved with a drain bias of only 5 V. With flip-chip mounting and a higher drain voltage, even higher output power is expected. Figure 5 shows the two-tone test with 0.5 MHz separation for the two signals at 19 GHz at a drain bias of 5 V and two different gate biases (i.e., -0.4 V and -0.5 V). At 1-dB gain compression, the C/I3 ratio is ~ 20 dBc. At 5-dB back-off from saturation, the C/I3 ratio is ~ 28 dBc. Other amplifiers with output device of 1200 µm gatewidth had up to 500 mW output at 19 GHz with scaled C/I3 performance. RF functional yield as high as 90% was achieved on these amplifiers.

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References


Figure 2: SEM Photo Taken on the Output 600 μm Device Prior to Polyimide Coating

Figure 3: Small-Signal Gain-Frequency Response of MMICs from Four Wafers (Vg = -0.5 V, Vd = 3 V, Id ~ 100 mA)

Figure 4: Performance of a Three-Stage K-Band ETL MMIC Amplifier (Vg = -0.5 V, Vd = 5 V, Id ~ 125 mA)

Figure 5: Gain Compression and Two-Tone Distortion Characteristics of a K-Band ETL MMIC Amplifier (Vd = 5 V, solid line: Vg = -0.5V, Iq = 123 mA, dotted line: Vg = -0.4 V, Iq = 160 mA)
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**Abstract**
The design, fabrication, and performance of K-band high-efficiency, linear power pHEMT amplifiers implemented in Embedded Transmission Line (ETL) MMIC configuration with unthinned GaAs substrate and topside grounding are reported. A three-stage amplifier achieved a power-added efficiency of 40.5% with 264 mW output at 20.2 GHz. The linear gain is 28.5 dB with 1-dB gain compression output power of 200 mW and 31% power-added efficiency. The carrier-to-third-order intermodulation ratio is -20 dBc at the 1-dB compression point. A RF functional yield of more than 90% has been achieved.

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