EMI IMMUNITY TESTING
THRESHOLD DEFINITION

![Threshold Definition Diagram]

- **Vout**
  - High: 2.0 v
  - Unk: 0.8 v
  - Low

- **EMI**
  - SIG
  - Vt1 Immunity Lvl
  - Vt2 Immunity Lvl

Diagram: Logic gate with inputs H and H, output L.
THRESHOLD DEFINITION

Vout

2.0 v

0.8 v

EMI

SIG
BIAS TEE CALIBRATION SET-UP
EMI IMMUNITY LEVELS

Chart 1. EMI IMMUNITY LEVEL
7400 NAND GATES

Immune Level [dBm]

-10.0 -5.0 0.0 5.0 10.0 15.0 20.0 25.0 30.0

Frequency [MHz]

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V_o=V_{t1}
V_o=V_{t2}
70's Data
EMI IMMUNITY LEVELS

Chart 2. EMI IMMUNITY LEVEL
74ALS00 NAND GATES

Frequency [MHz]

Immune Level [dBm]

-10.0  -5.0  0.0  5.0  10.0  15.0  20.0  25.0  30.0

- Vo=Vt1
- - Vo=Vt2
- - - 70's Data
NAND vs. AND GATE IMMUNITY

Chart 1. EMI IMMUNITY LEVEL
7400 NAND GATES

Chart 2. EMI IMMUNITY LEVEL
74ALS00 NAND GATES

Chart 3. EMI IMMUNITY
74LS00 NAND GATES

Chart 4. EMI IMMUNITY LEVEL
7408 AND GATES
TP vs. OC IMMUNITY LEVELS

Chart 7. EMI IMMUNITY LEVEL
7404 TOTEM POLE INVERTER

Chart 8. EMI IMMUNITY LEVEL
74LS04 TOTEM POLE INVERTER

Chart 9. EMI IMMUNITY LEVEL
7405 OPEN COLLECTOR INVERTER

Chart 10. EMI IMMUNITY
74LS05 OPEN COLLECTOR INVERTER
7805 VOLT REG IMMUNITY

Chart 11. EMI IMMUNITY LEVEL
7805 VOLTAGE REGULATOR

Chart showing EMI immunity level for the 7805 voltage regulator. The graph plots Immune Level [dBm] against Frequency [MHz], with lines indicating different conditions labeled as Vo=Vt1, Vo=Vt2, and 70's Data.
# SEVENTIES CHIP SET

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<th>Type</th>
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<td>Comparators</td>
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<td><strong>TOTAL NUMBER TYPES</strong></td>
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