INTEGRATED CIRCUIT IMMUNITY

DOD E³ Program Review
11-14 April 2000

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EMI IMMUNITY TESTING
THRESHOLD DEFINITION

Vout

2.0 V

0.8 V

EMI

SIG
BIAS TEE FUNCTION

DC & Msnt

EMI Sig In → EMI Sig

DC & Msnt ←
BIAS TEE CALIBRATION SET-UP
EMI IMMUNITY LEVELS

Chart 1. EMI IMMUNITY LEVEL
7400 NAND GATES

![Graph showing EMI immunity levels with frequency on the x-axis and immune level in dBm on the y-axis. Different lines represent different levels and conditions.]

- **Vo=Vt1**
- **Vo=Vt2**
- **70's Data**
EMI IMMUNITY LEVELS

Chart 2. EMI IMMUNITY LEVEL
74ALS00 NAND GATES

Frequency [MHz]

Immune Level [dBm]

- - - Vo=V1
--- Vo=V2
--- 70's Data
NAND vs. AND GATE IMMUNITY

Chart 1. EMI IMMUNITY LEVEL
7400 NAND GATES

Chart 2. EMI IMMUNITY LEVEL
74ALS00 NAND GATES

Chart 3. EMI IMMUNITY
74LS00 NAND GATES

Chart 4. EMI IMMUNITY LEVEL
7408 AND GATES

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J. Sketoe, Boeing Co.
A. Clark, NASA, MFSC
TP vs. OC IMMUNITY LEVELS

Chart 7. EMI IMMUNITY LEVEL
7404 TOTEM POLE INVERTER

Chart 8. EMI IMMUNITY LEVEL
74LS04 TOTEM POLE INVERTER

Chart 9. EMI IMMUNITY LEVEL
7405 OPEN COLLECTOR INVERTER

Chart 10. EMI IMMUNITY
74LS05 OPEN COLLECTOR INVERTER
7805 VOLT REG IMMUNITY

Chart 11. EMI IMMUNITY LEVEL
7805 VOLTAGE REGULATOR

[Graph showing immunity level vs. frequency]
# SEVENTIES CHIP SET

<table>
<thead>
<tr>
<th>TTL:</th>
<th>7400, 7402, 7404, 7405, 7408, 7432, 7450, 7473, &amp; 7479</th>
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<td>CMOS:</td>
<td>4011A, 4011B, 4007A, 4007B, 4001A, &amp; 4013A</td>
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<td>Line drvr/rcvr:</td>
<td>8830/8820, 9614/9615, 55109/55107A, &amp; 55110</td>
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<td>Voltage Reg:</td>
<td>(3-pin) 309, 320, 78M05, (8-pin) 300, &amp; 305</td>
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<tr>
<td>Comparators:</td>
<td>306, 311, 339, 360, 710, &amp; 760</td>
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<td><strong>TOTAL NUMBER TYPES</strong></td>
<td></td>
<td>38</td>
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