FPGAs in Space Environment and Design Techniques

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Goals

- Brief overview of the radiation environment
- What type of radiation effects are there?
- How are devices tested?
- How should the results be interpreted?
- How can we protect our systems?

Outline

- Environment and Effects
- Total Dose
- Single Event Upset
- Single Event Latchup
- Single Event Transient
- Antifuse and Rupture
- Protons
- Loss of Functionality
- Miscellaneous
Environment and Effects

Components of the Natural Environment

- Transient
  - Galactic Cosmic Rays
  - Hydrogen & Heavier Ions
  - Solar Particle Events
    - Protons & Heavier Ions
- Trapped
  - Electrons, Protons, & Heavier Ions
- Atmospheric & Terrestrial Secondaries
  - Neutrons

GCRs: Integral LET Spectra
CREME 96, Solar Minimum, 100 mils (2.54 mm) Al

Types of Single Event Effects

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Radiation</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>SEU</td>
<td>Single Event Upset</td>
<td>Single Event Set</td>
</tr>
<tr>
<td>SET</td>
<td>Single Event Transient</td>
<td>Single Event Set</td>
</tr>
<tr>
<td>SETS</td>
<td>Single Event Setback</td>
<td>Single Event Set</td>
</tr>
<tr>
<td>SEGR</td>
<td>Single Event Gate Repair</td>
<td>Single Event Set</td>
</tr>
<tr>
<td>SEL</td>
<td>Single Event Long-Last</td>
<td>Single Event Set</td>
</tr>
<tr>
<td>SEI</td>
<td>Single Event Ionization</td>
<td>Single Event Set</td>
</tr>
<tr>
<td>MBE</td>
<td>Multiple Bit Error</td>
<td>Multiple Bit Error</td>
</tr>
<tr>
<td>SBP</td>
<td>Single Bit Permanent</td>
<td>Single Bit Permanent</td>
</tr>
</tbody>
</table>

Event Effects

LET (MeV·cm²/mg)
Total Dose

Recombination, Transport, and Trapping of Carriers

GSFC Total Dose Facility

Example TID Static Bias Board Supports In Situ Testing

MIL-Std-883 Method 1019.5

Annealing allowed for parametric failures, not for functional failures. 1019.5 also allows for low dose rate testing.

A14100ANEC TID TEST - Room Temp Anneal
DC 384 - UCL084 Lot Split
Post 20 krad(Si) Exposure @ 2.45 rad(Si)/Min
Annealed August 3, 1999

Graph showing annealing temperature over time.
Second Generation System - Overview

Typical TID Run

TID Run - Extended

TID Run - Runaway

Charge Pump and Isolation FETs
In Situ Functional Testing

Note: Some cases showed failure at less than 20 mA current with current jumps of 6-8 mA.

Icc Transient - Peak Current

Note: Some lots higher, some lower.
Shielding Effectiveness

Dose Rate Effects on Xilinx 0.25μm Technology

Total Ionizing Dose Effect on 0.18μm Technology

TID Testing Results

• 0.60μM OTP PROM Technology
  - TID evaluation performed on XQR1701L
  - device parametric shifts affected decoder speed
  - field oxide leakage determined TID of 60krads
  - device fully functional at end of dose
  - no data loss/gain as a result of TID
  - 100°C anneal fully restored device
  - room temp anneal showed no rebound

Xilinx PROM Response to TID

Xilinx PROM Response to TID
**In Situ measurement of Propagation Delay**

Real-time Digitized Input and Output Waveforms

Before irradiation: $t_{out} = 155\text{ns}$

After accumulating 99 krads: $t_{out} = 360\text{ns}$

**Total Dose Effects on FLASH Switch**

- Ionizing radiation discharge the floating gate
  - Increase Off-state NMOS transistor resistance, increase
  - Increase OFF-state NMOS sub-threshold leakage, increase
  - Increase ON-state NMOS transistor resistance, increase
  - Increase RC delay in the data path
Single Event Upset (SEU)

Definitions

**Single Event Upset (SEU)** is a change of state or transient induced by an ionizing particle such as a cosmic ray or proton in a device. This may occur in digital, analog, and optical components or may have effects in surrounding circuitry. These are "soft" bit errors in that a reset or rewriting of the device causes normal behavior thereafter. A full SEU analysis considers the system effects of an upset. For example, a single bit flip, while not damaging to the circuitry involved, may damage the subsystem or system (i.e., initiating a pyrotechnic event).

**Definitions**

**Linear Energy Transfer (LET)** is a measure of the energy transferred to the device per unit length as an ionizing particle travels through a material. The common unit is MeV-cm²/mg of material (Si for MOS devices).

**LET threshold (LETₜₚ) is the minimum LET to cause an effect. The JEDEC recommended definition is the first effect when the particle fluence = 10⁷ ions/cm².**

**Interaction of a Cosmic Ray and Silicon**

**SEE Test Setup**

**Cross section (σ)** is the device SEE response to ionizing radiation. For an experimental test for a specific LET, σ = Errors/(ion fluence). The units for cross section are cm² per device or per bit.

**Asymptotic or saturation cross section (σₚₑₗₑ)** is the value that the cross section approaches as LET gets very large.

**Sensitive volume** refers to the device volume affected by SEE-inducing radiation. The geometry of the sensitive volume is not easily known, but some information is gained from test cross section data.

**SEE Test Setup**

A Single Event Effects Test Setup

Vacuum Chamber

Phosphor/Phosphor tube (particle counter)

Berkeley 86-inch Heavy Ion Cyclotron Shifter

Device being tested

Test Electronics

Control Computer
Figure 16. Cross section-LET curve for a commercial A54XX32-A. Few SEUs were detected for the hardened device at an LET ≥ 60 MeV-cm²/mg.

Figure 2. Standard master-slave flip-flop.
Figure 3. K-Latch schematic, simplified. The asynchronous structure and interlocks eliminate the need for a free running clock to scrub SEUs.

Figure 5. Simplified test circuitry logic.

<table>
<thead>
<tr>
<th>Simplex vs. TMR Reliability</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>TMR</th>
<th>0.99999999</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simplex</td>
<td>0.9999999</td>
</tr>
</tbody>
</table>

SRAM Switch Technology

- Increase internal latch delay.
- No upset when response time > recovery time.
- Poly-resistor has high temperature coefficient.
- Poly-resistance has large process variation.
XQR4036XL SEU Cross Section

SRAM Memory Sizes

Virtex FPGA Static Heavy Ion SEU Sensitivity

An upset in configuration control logic register was observed

Weibull Curve for Average POR
Heavy Ion Cross-section

XQR1701L PROM

(Data provided by Saab Ericsson Space)
XQR1701L PROM

Address Fail - x4093

UT4090

- User flip-flops hardened
- I/O flip-flops not hardened
- RAM blocks not hardened

SEU in PAL - Large X-Section

22V10C PALs - flip-flop cross-section (divide by 8 to get per flip-flop)

Solar Flare and SEU Rates

<table>
<thead>
<tr>
<th># of nodes</th>
<th>input status</th>
<th>module design</th>
<th>LET threshold</th>
<th>signal</th>
<th>IONIZED TRAPPED</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>102</td>
<td>0-2</td>
<td>C</td>
<td>25</td>
<td>1E-4</td>
<td>7.32E-4</td>
<td>1.33</td>
</tr>
<tr>
<td>60</td>
<td>0-2</td>
<td>E</td>
<td>45</td>
<td>1E-7</td>
<td>4.2E-7</td>
<td>0.16</td>
</tr>
<tr>
<td>60</td>
<td>0-2</td>
<td>D</td>
<td>45</td>
<td>1E-7</td>
<td>4.2E-7</td>
<td>0.16</td>
</tr>
</tbody>
</table>

Note effect of logic state on SEU Rate.

Shielding Cosmic Rays

Software Support for SEU-Hardening

- Synopsis Design Compiler
- Synplicity Synplify
- NASA-GSFC 'Macro Substitution'
- Actmap & Actgen
Single Event Latchup (SEL)

Definitions

**Single Event Latchup (SEL)** is a potentially destructive condition involving parasitic circuit elements forming a silicon controlled rectifier (SCR). In traditional SEL, the device current may destroy the device if not current limited and removed "in time." A "microlatch" is a subset of SEL where the device current remains below the maximum specified for the device. A removal of power to the device is required in all non-catastrophic SEL conditions in order to recover device operations.

**Latchup Basics**

**EPI Layer, Latchup, and Ion Range**

**SEL - QL3025 0.35 μm**

**Chip Express Latchup Comparison**
**SEL** Variability

<table>
<thead>
<tr>
<th>Sel No.</th>
<th>Lot No.</th>
<th>D.C.</th>
<th>Threshold (mA)</th>
<th>Protracted Latchup Allowed?</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>A2</td>
<td>17F1641</td>
<td>340</td>
<td>12.9</td>
<td>1711 (2)</td>
</tr>
<tr>
<td>B1</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>B2</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>B3</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>B4</td>
<td>17F1641</td>
<td>356</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>B5</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>B6</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>C1</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>D1</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
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<tr>
<td>D2</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
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<tr>
<td>D3</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
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</tr>
<tr>
<td>D4</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
<tr>
<td>D5</td>
<td>17F1641</td>
<td>365</td>
<td>12.9</td>
<td>1756 (1)</td>
</tr>
</tbody>
</table>

**SEL** Summary for A1020B. A large set of parts from multiple lots were tested, showing a wide range of SEL and latchup currents. Some latchups were destructive with either higher $E_{th}$ or functional failure.

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**Distribution of Peak Latchup Currents for the A1020B (MEC)**

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**Single Event Latchup**

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**Single Event Latchup Ion Energy Dependence**

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**Latchup Summary**

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Size/Voltage</th>
<th>Threshold (MeV cm$^2$/mg)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>RH1020</td>
<td>1.0 μm / 5.0</td>
<td>&gt; 74</td>
<td>Destructive</td>
</tr>
<tr>
<td>QL24X21B</td>
<td>0.65 μm / 5.0</td>
<td>&lt; 18</td>
<td>Destructive</td>
</tr>
<tr>
<td>RT54X1692</td>
<td>0.8 μm / 2.3</td>
<td>&gt; 120</td>
<td>Destructive</td>
</tr>
<tr>
<td>AS4522A</td>
<td>0.25 μm / 1.5</td>
<td>High</td>
<td>Destructive</td>
</tr>
<tr>
<td>QVH250</td>
<td>0.8 μm / 5.0</td>
<td>&gt; 52</td>
<td>Low</td>
</tr>
<tr>
<td>CX2041</td>
<td>0.6 μm / 2.5</td>
<td>&gt; 37</td>
<td>Low</td>
</tr>
<tr>
<td>CX2001</td>
<td>0.35 μm / 1.3</td>
<td>Lowest</td>
<td>Low</td>
</tr>
<tr>
<td>AS45X16*</td>
<td>0.35 μm / 3.3</td>
<td>&gt; 74</td>
<td>Destructive</td>
</tr>
<tr>
<td>QL2052</td>
<td>0.35 μm / 3.3</td>
<td>&lt; 11</td>
<td>Destructive</td>
</tr>
<tr>
<td>XQR468X*</td>
<td>0.35 μm / 3.3</td>
<td>&gt; 100</td>
<td>Destructive</td>
</tr>
</tbody>
</table>
Ex. SEL Detection and Clearing

Figure 5.1 AMP310P Layout sketch

Note that FPGA have high I/O count with diodes to \( V_{cc} \) and GND in most cases.
Single Event Transient (SET)

Critical Transient Width vs Feature Size for Unattenuated Propagation

Double Clocking As a Result of Heavy Ion Induced Pulse

Clock Upset Instrumentation

Clock Upset Cross Section RH1020
Frequency Dependence of Clock Upset

![Graph showing frequency dependence of clock upset]

SET in PAL

![Graph showing SET in PAL]

Driver Contention Due to CSRAM Upset

![Diagram showing driver contention due to CSRAM upset]

Mode 1 Transient Upset

- Transient pulse higher than half VDC will propagate
- $Q_{\text{th}} = 0.05 \mu C$, or $\text{LET}_{\text{th}} = 2 \text{MeV-cm}^2/\mu\text{g}$ for the worst case
Antifuse Technology

ONO Antifuse
Poly/ONO/Poly
Heavy as doped Poly/N++
Thickness controlled by CVD outside
Programmed - 18V
Typical Tone - 85 A
R = 100 - 500 ohms

TD Amorphous Silicon Antifuse
‘Pancake’ Stack Between Metal 2 and 3
Designed for 3.6V Operation in 5mm Of gates FPGA
‘Logic’ Devices Program at ~10V
‘Deviante’ Devices Program at ~30V
Thickness - 500 - 1000 A
R = 50 - 100 ohms

Quicklogic ViaLink Antifuse

Antifuse Construction

Antifuse Radiation Effects

• Unprogrammed Reliability is the Key Concern
  - ONO
  - Amorphous Silicon (AS)

• Manufacturers:
  - Actel (ONO, Silicon) FPGA
  - L-M (ONO) PROM
  - Pico Systems (AS) Programmable Substrate
  - Quick Logic (AS) FPGA
  - UTMC (AS) PAL, FROM

Gate Rupture

Comparison of Rupture Currents

Figure A1: Applied voltage field for ZEUS as a function of the LET for various gate oxide thicknesses. For this data the breakdown field increases significantly for the thicker oxides (after [Ref.17]).

ONO Antifuse
Amorphous Silicon Antifuse Rupture
Substrate $\alpha$-Silicon Antifuse F/A Using Liquid Crystal

ONO Antifuse Breakdown - FA

Mag = 5X
Mag = 20X
Mag = 100X

Heavy Ion Damage and Failure Analysis

M2M Antifuse Device
ONO Antifuse Device

Antifuse Failure Thresholds

Antifuse Improvements
- Decrease Electric Field Strength
  - Thicker Antifuses (RH1020, RH1280)
  - Low Bias Voltage (L-M PROM)
- Antifuse "Recipe"
  - (RT54SX16, RH54SX16, RT54SX32)
- Minimize Bias Time
  - (UTMC PROM)
- Reduce Sensitivity
  - Differential Measurements (UTMC PROM)
Dielectric Antifuse Cross Sections

ONO Antifuse Testing with Iodine (LET=40)
Bias = 5.5 VDC
Normal Incidence

Unhardened
Hardened

Antifuse Rupture

Figure 1: Summary of antifuse rupture data. Results range at LET = 500 MeV-cm²/mb with a hardened ONO and Bare. One, 'un' ranges at an MCD and Bare, 100% used at LET = 100 MeV-cm²/mb.
Protons

Proton Testing at UC Davis

I_{cc} Damage During Proton Testing
ASIC and Antifuse FPGA

Note: Different scales for each run.

A 1280XL Proton Results

A 1280A Proton Upsets

From Luddred Martin/Actel

\( S \) module threshold = 35 MeV
\( C \) and Modified 3 > 148 MeV
<table>
<thead>
<tr>
<th>Device Type</th>
<th>Size/Voltage</th>
<th>Est. X-sec</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1280A</td>
<td>1.0 μm / 5.0</td>
<td>~ 137 x 10^-15</td>
<td>19 Parts Tested</td>
</tr>
<tr>
<td>RH1020</td>
<td>1.0 μm / 5.0</td>
<td>&lt; 2 x 10^-15</td>
<td></td>
</tr>
<tr>
<td>RH1280</td>
<td>0.8 μm / 5.0</td>
<td>~ 4 x 10^-15</td>
<td>S-Module</td>
</tr>
<tr>
<td>QYH500</td>
<td>0.8 μm / 3.3</td>
<td>&lt; 0.5 x 10^-15</td>
<td>No upsets det.</td>
</tr>
<tr>
<td>RT54SX16</td>
<td>0.6 μm / 3.3</td>
<td>~ 6 x 10^-15</td>
<td></td>
</tr>
<tr>
<td>QL3025</td>
<td>0.35 μm / 3.3</td>
<td>&lt; 4 x 10^-15</td>
<td>No upsets det.</td>
</tr>
<tr>
<td>A54SX16</td>
<td>0.35 μm / 3.3</td>
<td>~ 3 x 10^-15</td>
<td></td>
</tr>
<tr>
<td>JT22VP10</td>
<td>7 μm / 5.0</td>
<td>~ 2 x 10^-11</td>
<td>Cypress die</td>
</tr>
</tbody>
</table>

**Virtex FPGA Static Proton SEU Sensitivity**

Configuration control logic register upset noted at 63MeV.
Definitions

Single Event Functional Interrupt (SEFI) is a condition where the device stops operating in its normal mode, and usually requires a power reset or other special sequence to resume normal operations. It is a special case of SEU changing an internal control signal. One example would be a DRAM entering the test mode defined by JEDEC. Another example is a microcircuit with IEEE 1149 1 JTAG circuitry leaving the TEST_LOGIC_RESET state and loading an unintended instruction into the instruction register (IR). Like other SEUs, the system effects must be properly analyzed. For example, a JTAG upset can cause the device to draw high currents or turn inputs into an output. The latter could, for example, drive a clock line to ground, thus, an independent clock signal should be used for the TCLK pin on devices without the optional TRST* pin.

FRAM Memory Functionality

**Loss During Heavy Ion Test**

![Diagram of FRAM Memory Functionality](image-url)

**DRAM Modes**

DRAM Special Test and Operational Modes

This standard defines a scheme for controlling a series of special modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control, and exit from the special modes. In addition, it defines a basic special test mode plus a series of other special test and operational modes.

**TEST MODES** are those that implement some special test of measurement function or algorithms designed to enhance the ability of the Vendor or User to determine the integrity of, or to characterize, the part.

**OPERATIONAL MODES** are those that alter the operational characteristics of the part but do not interfere with its function as a storage device and are intended to be used in system operation.

JEDEC Standard No. 21-C, page 3 9 5 1, Revision 4

**DRAM Refresh**

**CAS# BEFORE RAS# REFRESH** is a frequently used method of refresh because it is easy to use and offers the advantages of a power savings. Here's how CBR REFRESH works. The device contains an internal counter which is initialized to a random count when the device is powered up. Each time a CBR REFRESH is performed, the device refreshes a row based on the counter, and then the counter is incremented. When CBR REFRESH is performed again, the next row is refreshed and the counter is incremented. The counter will automatically wrap and continue when it reaches the end of its count. There is no way to reset the counter. The user does not have to supply or keep track of row addresses.

Since CBR REFRESH uses the internal counter and not an external address, the address bus is powered down. For power-sensitive applications, this can be a benefit because there is no additional current used in switching address lines on a bus, nor will the DRAMs pull extra power if the address voltage is at an intermediate state.

JEDEC Standard No. 21-C, page 3 9 5 1, Revision 4

Adapted from: JEDEC Standard No. 21-C, page 3 9 5 1, Revision 4

Adapted from: Micro Technical Note TN-06-36, "Various Methods of DRAM Refresh."
IEEE JTAG 1149.1

Shift Register is undefined in TEST-LOGIC-RESET State

IEEE JTAG 1149.1 TCLK

The CLK pin may turn into an output driving low, clamping the oscillator's output to a logic '0'. The TAP controller can not reset and restore I/O operation. Most FPGAs do not have the optional TRST* pin. Note TRST*, when present, has a pull-up.

IEEE JTAG 1149.1 - Scan Path

IEEE JTAG 1149.1 - Scan I/O Cell

System Logic

JTAG Upset Effect - Step Load

TCK and TMS=1 Not Guaranteed Solution

JTAG Upset Effect - Step Load

Second Distinct Failure Mode
JTAG Upset Effect - TCK On

Sample of 3 JTAG 'Upsets'

SEE Results - Loss of Functionality
Atmel AT28C010 EEPROM, D/C 9706

Type I Errors
- Manifested by the appearance of repeated errors, once the first error had been detected during low irradiation. Here, the first error appeared at some point in time, which was a function of reading cycles ("cycle" is defined in Section I) after the exposure had started. Thereafter, we observed one error every few cycles.
- Errors were stored independently at various address locations.
- Simultaneously with the observation of the first error, the device bias current increased to 26 mA from 20 mA (nominal, pre-error condition). The bias current continued to be 26 mA until the reading process stopped. At that time, the current became 0.2 mA (quiescent level).
- When the device was read again (without power-cycling), the bias current returned to 26 mA and errors appeared again (even without the beam).
- If the power to the device was shut off and re-started again (power-cycled), the device again functioned properly (i.e., no errors).
- In one instance, we monitored the irradiation without power-cycling for a longer time, until the device no longer showed any errors. It appeared that the affected bit underwent additional upset, returning to the original polarity and thereby correcting the problem.

Type II Errors
- Manifested by "00" in all address locations, once the first "00" was read.
- These errors could be removed only by power-cycling the device.

Type III Errors
- Characterized by occasional errors in a byte, which appeared once in many cycles. There was no "after-effect" for this type of error. In other words, one error appeared independently once in a while.
- Caused by an upset in the output buffer.

Atmel AT28C010 EEPROM, D/C 9706

Atmel AT28C010 EEPROM, D/C 9706

X28HC256 CMOS EEPROM
Xicore, D/C 9140

Atmel AT28C010 EEPROM, D/C 9706

Xicore, D/C 9140
Loss of Functionality
Serial PROM

- Xilinx XQR1701L
  - 10% saturated intercept at LET = 6 MeV-cm²/mg, 1.2×10⁻⁵ cm²/device


Loss of Functionality
Processors

- Processor simply stopped functioning without showing any observable bit errors.
- Noticed lookup in many microprocessors including MG80C186, MG80C286, and XC68302.
- Sensitivity to lookup was essentially independent of the test programs.

LVDO Regulator Failure

FRAM Memory Functionality Loss During Total Dose Test
EDAC Techniques

<table>
<thead>
<tr>
<th>EDAC Method</th>
<th>EDAC Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parity</td>
<td>Single bit error detect</td>
</tr>
<tr>
<td>Cyclic Redundancy Check (CRC)</td>
<td>Detects if any errors have occurred in a given structure</td>
</tr>
<tr>
<td>Hamming Code</td>
<td>Single bit correct, double bit detect</td>
</tr>
<tr>
<td>Reed-Solomon Code</td>
<td>Corrects multiple and consecutive bytes in error</td>
</tr>
<tr>
<td>Convolutional Code</td>
<td>Corrects isolated burst noise in a communication stream</td>
</tr>
<tr>
<td>Overlying Protocol</td>
<td>Specific to each system. Example: retransmission protocol</td>
</tr>
</tbody>
</table>

From LaBel

Control-Error Protection Schemes

<table>
<thead>
<tr>
<th>Protection Method</th>
<th>Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog Timer</td>
<td>If not reset within the designated interval, perform some function (usually a system reset).</td>
</tr>
<tr>
<td>Redundancy</td>
<td>Two equivalent systems operate on the same data. If the two systems disagree, a system reset is performed.</td>
</tr>
<tr>
<td>Lookstep</td>
<td>Two devices in a system are clocked simultaneously, and which are provided common inputs. If the devices disagree, perform a system reset.</td>
</tr>
<tr>
<td>Voting</td>
<td>Use three or more devices to perform the same function. If one device disagrees with the rest, use the remaining devices to determine the next system state.</td>
</tr>
<tr>
<td>Repetition</td>
<td>A system must provide the same data more than once to perform some action. Used, for instance, to lower the risk of an inadvertent spacecraft command being executed.</td>
</tr>
</tbody>
</table>
**Definitions (1)**

**Single Event Upset (SEU)** is a change of state or transient induced by an ionizing particle such as a cosmic ray or proton in a device. This may occur in digital, analog, and optical components or may have effects in surrounding circuitry. These are "soft" bit errors that a reset or rewriting of the device causes normal behavior thereafter. A full SEU analysis considers the system effects of an upset. For example, a single bit flip, while not damaging to the circuitry involved, may damage the subsystem or system (i.e., initiating a pyrotechnic event).

**Single Hard Error (SHE)** is an SEU which causes a permanent change to the operation of a device. An example is a permanent stuck bit in a memory device.

**Definitions (2)**

**Single Event Functional Interrupt (SEFI)** is a condition where the device stops operating in its normal mode, and usually requires a power reset or other special sequence to resume normal operations. It is a special case of SEU changing an internal control signal. One example would be a DRAM entering the test mode defined by JEDEC. Another example is a microcircuit with IEEE 1149.1 JTAG circuitry leaving the TEST_LOGIC_RESET state and loading an unintended instruction into the instruction register (IR). Like other SEUs, the system effects must be properly analyzed. For example, a JTAG upset can cause the device to draw high currents or turn inputs into an output. The latter could, for example, drive a clock line to ground, thus, an independent clock signal should be used for the TCLK pin on devices without the optional TRST* pin.

**Definitions (3)**

**Single Event Latchup (SEL)** is a potentially destructive condition involving parasitic circuit elements forming a silicon controlled rectifier (SCR). In traditional SEL, the device current may destroy the device if not current limited and removed "in time." A "microlatch" is a subset of SEL where the device current remains below the maximum specified for the device. A removal of power to the device is required in all non-catastrophic SEL conditions in order to recover device operations.

**Single Event Burnout (SEB)** is a highly localized burnout of the drain-source in power MOSFET's. SEB is a destructive condition.

**Definitions (4)**

**Single Event Gate Rupture (SEGR)** is the burnout of a gate insulator in a power MOSFET. SEGR is a destructive condition.

**Linear Energy Transfer (LET)** is a measure of the energy transferred to the device per unit length as an ionizing particle travels through a material. The common unit is MeV-cm²/kg of material (Si for MOS devices).

**LET threshold (LETₜₘ)** is the minimum LET to cause an effect. The JEDEC recommended definition is the first effect when the particle fluence = 10⁷ ions/cm²

**Definitions (5)**

**Cross section (σ)** is the device SEE response to ionizing radiation. For an experimental test for a specific LET, σ = #errors/(ion fluence). The units for cross section are cm² per device or per bit.

**Asymptotic or saturation cross section (σₘₐₓ)** is the value that the cross section approaches as LET gets very large.

**Sensitive volume** refers to the device volume affected by SEE-inducing radiation. The geometry of the sensitive volume is not easily known, but some information is gained from test cross section data.