PCB Design With HDL Designer

- Motivation
  - Time savings
  - Money savings
  - Simplicity

- Approach
  - Use single tool for PCB and FPGA design
  - More FPGA designs than PCB designers
    - Use HDL designer for schematic capture
PCB Design With HDL Designer
Design Process

- PCB Design Process (Minimal):
  - Schematic Capture
  - Displaying Reference Designators and Component Information on Schematic
  - Netlist Creation and Conversion
PCB Design With HDL Designer
Schematic Capture - Symbols

- Part Symbols
  - HDL Symbol Editor
    - Part Name
    - Part Number
    - Package Type
    - Pin Name (or Port Name)
    - Pin Number
Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

Generic Declarations

pin_a0 string "1"
pin_b0 string "2"
pin_o0 string "3"
pin_o1 string "4"
pin_b1 string "5"
pin_o1 string "6"
pin_gnd string "7"
pin_o3 string "8"
pin_b3 string "9"
pin_o3 string "10"
pin_o2 string "11"
pin_b2 string "12"
pin_o2 string "13"
pin_vcc string "14"
port_num string "port_x08"
pkg_type string "dpl4"
PCB Design With HDL Designer
Schematic Capture – Schematic Diagrams

- Schematic Diagrams

- HDL Block Diagram Editor

  - Part Information from Part Symbol
    - Pin Number
    - Package Type
    - Part Number

  - Connection Information
    - Nets
    - Reference Designators
PCB Design With HDL Designer
Schematic Capture – Schematic Diagrams

Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

Declarations
Ports
a : end_logic
b : end_logic
c : end_logic
d : end_logic

Diagram Signals
SIGNAL Vcc : end_logic
SIGNAL gnd : end_logic

pin_o0 = "1" (string)
pin_b0 = "2" (string)
pin_o1 = "3" (string)
pin_a1 = "4" (string)
pin_b1 = "5" (string)
pin_o2 = "6" (string)
pin_b2 = "7" (string)
pin_o3 = "8" (string)
pin_b3 = "9" (string)
pin_a0 = "10" (string)
pin_b0 = "11" (string)
pin_a2 = "12" (string)
pin_b2 = "13" (string)

pin_vcc = "14" (string)

port_num = "port_o0" (string)
pkg_type = "dip4" (string)

my_project_lib
A08
I1

<tlafourcode>

<table>
<thead>
<tr>
<th>test circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>--------------</td>
</tr>
<tr>
<td>--------------</td>
</tr>
</tbody>
</table>

MARLUG
PCB Design With HDL Designer
VHDL Coding

- Issue – Where to include Pin Numbers in VHDL?
  - Comments
    - Possible
  - VHDL Attributes
    - Good Approach but not displayed on Block Diagrams in HDL Designer
  - VHDL Generics
    - Chosen Approach but displays pin numbers as a block of text
PCB Design with HDL Designer
Netlist Conversion

Issue – How can a PADS netlist be produced?

– Comments

– Possible

– VHDL Attributes

– Good Approach but not displayed on Block Diagrams in HDL Designer

– VHDL Generics

– Chosen Approach but displays pin numbers as a block of text

```
GENERIC (  
    pin_a0 : string := "1";
    pin_o0 : string := "2";
    pin_a1 : string := "3";
    pkg_type : string := "dip14";
    part_num : string := "part_ac04"
);
```
Conclusion

- Approach can be used PCB design
  - Would like Vendor to study modifications to HDL Designer
    - Schematic Display
    - PCB netlist output options
    - Design Rule Checking
    - Part List Generation