PCB Design With HDL Designer

- Motivation
  - Time savings
  - Money savings
  - Simplicity

- Approach
  - Use single tool for PCB and FPGA design
  - More FPGA designs than PCB designers
    - Use HDL designer for schematic capture
PCB Design With HDL Designer
Design Process

- PCB Design Process (Minimal):
  - Schematic Capture
  - Displaying Reference Designators and Component Information on Schematic
  - Netlist Creation and Conversion
PCB Design With HDL Designer
Schematic Capture - Symbols

- Part Symbols
  - HDL Symbol Editor
    - Part Name
    - Part Number
    - Package Type
    - Pin Name (or Port Name)
    - Pin Number
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Schematic Capture – Schematic Diagrams

- Schematic Diagrams

- HDL Block Diagram Editor

  - Part Information from Part Symbol

    - Pin Number
    - Package Type
    - Part Number

  - Connection Information

    - Nets
    - Reference Designators
PCB Design With HDL Designer
Schematic Capture – Schematic Diagrams

- Package List
  - Library ieee
  - Use ieee.std_logic_1164.all;
  - Use ieee.std_logic_arith.all;

- Declarations
  - Ports
  - a : std_logic
  - b : std_logic
  - c : std_logic

- Diagram Signals
  - Vcc : std_logic
  - GND : std_logic

```
pin_o0 = "1" (string)
pin_p0 = "2" (string)
pin_n0 = "3" (string)
pin_o1 = "4" (string)
pin_b1 = "5" (string)
pin_c0 = "6" (string)
pin_p0 = "7" (string)
pin_o3 = "8" (string)
pin_b3 = "9" (string)
pin_o1 = "10" (string)
pin_p3 = "11" (string)
pin_o2 = "12" (string)
pin_b2 = "13" (string)
pin_vcc = "14" (string)
part_num = "part_ac08" (string)
pkg_type = "dip14" (string)
```
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VHDL Coding

v Issue – Where to include Pin Numbers in VHDL?

– Comments

  v Possible

– VHDL Attributes

  v Good Approach but not displayed on Block Diagrams in HDL Designer

– VHDL Generics

  v Chosen Approach but displays pin numbers as a block of text
PCB Design with HDL Designer
Netlist Conversion

- Issue – How can a PADS netlist be produced?
  - Comments
    - Possible
  - VHDL Attributes
    - Good Approach but not displayed on Block Diagrams in HDL Designer
  - VHDL Generics
    - Chosen Approach but displays pin numbers as a block of text

```vhdl
GENERIC (
    pin_a0 : string := "1";
    pin_o0 : string := "2";
    pin_a1 : string := "3";
    pkg_type : string := "dip14";
    part_num : string := "part_ac04"
);
```
Conclusion

- Approach can be used PCB design
  - Would like Vendor to study modifications to HDL Designer
    - Schematic Display
    - PCB netlist output options
    - Design Rule Checking
    - Part List Generation