CMOS Ultra Low Power
Radiation Tolerant
(CULPRiT)
Microelectronics

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Ultra Low Power and Radiation
Tolerance/Hardness

- Space Electronics needs Radiation Tolerance or
  Hardness to withstand the harsh space environment:
  high-energy particles can change the state of the
  electronics or puncture transistors making them dis-
  functional
- Many ways to deal with the requirement:
  - Shielding: increased weight, volume, not very effective for
certain energy range
  - Employing redundant component: majority voting in TMR
  - Component design: use of clever circuit design within each
  component
Radiation Tolerant and Radiation Hard

**Radiation Hard**
- 1Meg rads Total Dose
- No latchup
- SEU ~ 40LET

**Radiation Tolerance**
- 100K rads Total Dose
- No latchup
- SEU ~ 40LET

**CULPRiT**
- ~ 1 Meg rad expected
- No latchup
- SEU ~ 40 LET

Radiation Tolerance/Hardness By Design

Technology development started 92 by GSFC:
- Commercial foundry based
- SEU tolerance by circuit design
- Latchup through guard bar layout
- Total dose @ whatever one could get

ASIC chips designed by RHBD flew on the following missions:
- HST, HOST, Landsat7, TERRA, EO-1, TIMED, CONTOUR, NOAA-N
ULP Fundamentals

- Current CMOS Power
  - > 90% dynamic
  - < 10% static
- ULP
  - 50% dynamic
  - 50% static

Reducing supply voltage (Vdd) and controlling back-bias voltage to transistor

⇒ Reduces threshold voltage
⇒ Reduces dynamic power

Technology development started in '97

1M Transistor Design
(Constant 5X Overdrive)

![Graph showing power consumption at different supply voltages](image-url)
**Power Comparisons**

- Up to 30x savings in power for ULP part
- Power savings increases with frequency
  - Static power of ULP parts exceeds that of 3.3V part
  - More power consumed switching at high voltages
- Dynamic power of ULP with 3.3V pads is much less than 3.3V part. Power consumption dominated by pad power.

**CULPRiT Validation in Space**

- A CULPRiT Reed-Solomon channel encoder operating at 0.5 volt was validated on NASA’s ST5 in 2006
  - Over 300 million telemetry frames processed by the CULPRiT part without single failure
Potential Power Savings on ST5/NMP Using RT ULP

Note: Sub-systems power is specified for the digital part only
Analog portion is included in "Others"

Potential ULP Savings to EO-1

Study performed by Ron Muller, John Oberich
The "Domino" Effect on Spacecraft Design

- Reduce System Power Requirement
- Reduce ACS Requirement
  - Reaction wheels
  - Torque bars
  - Thrusters
- Reduce Mass
  - Solar array
  - Batteries
  - Power conditioning
  - Heat sinks
- Reduce Propulsion Requirements
  - Launch vehicle
  - Delta-V engine
  - Fuel

Mission Level Design Options

Study and graphics by John Derright

RT ULP Processors Designed

- ST5 CULPRiT technology uses 0.35µm CMOS at AMI
- Other ULP ASICs fabricated at 0.35µm AMI:
  - Lossless compression chip, selected for EO-3 demo (CULPRiT)- (program de-scoped)
  - 8051 micro-controller (CULPRiT)
  - C50 DSP chip (ULP only)
  - 500 Mhz Correlator (CULPRiT) for GSFC’s radiometer development
  - Cross correlator (CULPRiT) for the Lightweight Rainfall Radiometer which processes cross-correlation among 25 channels, <1 watt over 200 Msamples/sec
**New Development: ULT**

- Ultra Low Temperature testing on CULPRiT Reed-Solomon encoder conducted in Sept., 2006 at GSFC
  - Chip working at 20°K at 50Mbps
    - Lower power (2.5mW) and frequency (6.25Mhz) at ULT
    - Operating parameters changed significantly
  - MOSFET parameter analysis shows improved operating characteristics
    - Transconductance increased
    - Threshold voltage increased
    - Leakage reduced
    - Device operates more like ideal MOSFETs

**Transconductance Curve: Green at 300k, Blue at 30k**

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**New Development: CULPRiT2**

- 2nd generation CULPRiT2 in development: 0.18μm, 0.13μm SOI at ASI/Cypress
  - Test chip in fabrication
  - Motorola ColdFire CULPRiT2 in design
  - Success promises future subsystem-on-chip (SOC) concept for spacecraft electronics modules.
  - Potential to reduce supply voltage to 0.25 volts