A delta-doped hybrid advanced detector (HAD) is provided which combines at least four types of technologies to create a detector for energetic particles ranging in energy from hundreds of electron volts (eV) to beyond several million eV. The detector is sensitive to photons from visible light to X-rays. The detector is highly energy-sensitive from approximately 10 keV down to hundreds of eV. The detector operates with milliwatt power dissipation, and allows non-sequential readout of the array, enabling various advanced readout schemes.

24 Claims, 7 Drawing Sheets
FIG. 5

- delta-doped potential well
  width ~ 5Å

FIG. 6

- delta-doped CCDs
- Bare Si reflection limit
DELTA-DOPED HYBRID ADVANCED DETECTOR FOR LOW ENERGY PARTICLE DETECTION

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of the U.S. Provisional Application Nos. 60/052,382, filed on Jul. 14, 1997, which is incorporated herein by reference.

STATEMENT AS TO FEDERALLY SPONSORED RESEARCH

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 U.S.C. 202) in which the Contractor has elected to retain title.

BACKGROUND AND SUMMARY OF THE INVENTION

When an energetic particle passes through silicon, a trail of electron-hole pairs is created along the particle’s path. Similarly, X-ray photons produce a cloud of electron-hole pairs near the location of the photon’s absorption. For high energy particles and X-rays (above 10 keV), it has been observed that one electron-hole pair is created for every 3.61 eV of energy deposited in the silicon. This value comes from the 1.1 eV required to raise an electron over the silicon band gap, plus the kinetic energy of the electron and hole required by the quantum mechanical rules of momentum conservation. This means that the amount of charge generated by a particle is directly proportional, within a statistical variation, to the energy lost by a particle in the silicon (for particles that pass completely through the silicon) or to the particle’s total energy (for particles that stop in the silicon). Particle energies can therefore be found from the number of generated electron-hole pairs. The particle’s direction of incidence can be also be found, by constructing a “pin-hole camera” and dividing the detector into individual pixels. The direction is found by determining in which pixel the charge was collected.

The detection of single low energy particles (such as protons with energies between 100 eV and 10 keV found in the solar wind) typically requires a detector that can collect the charge produced by such particles and which can then be read out with sufficient signal to noise ratio. When low energy particles enter a silicon detector, they tend to create a charge cloud very near the surface. Surface fields in ordinary silicon detectors tend to sweep this charge cloud to the surface where it is captured by surface states and neutralized by recombination before it can be collected for detection. In addition, conventional readout schemes are often too noisy and too slow to allow for adequate resolution of particle energies and complete separation of individual particle events. Finally, many detector schemes require thinning of the silicon detector material, which can be difficult, expensive, and time consuming.

FIG. 1 shows a silicon “PIN” diode structure used as a particle detector. One region 12 is doped p-type, and another region 14 is n-type. Between them in an “intrinsic” region 16 that is very lightly doped. The term “PIN” describes this p-type, intrinsic, n-type layer structure. By applying a negative potential 18 to the n-type region and a positive potential to the n-type region, an electric field is created that depletes the intrinsic region of any free electrons or holes. After the initial depletion, no current normally flows, since the region between the conducting n-type and p-type regions is depleted of carriers.

When a particle or photon is absorbed in the intrinsic region, the electron-hole pairs that the particle generates are swept away from the intrinsic region, with the holes going toward the p-type region and the electrons toward the n-type region. The total number of electron-hole pairs produced is proportional to the particle’s incident energy. This creates a current flow that can be detected by detector 11. Alternatively, the collected charge can be collected by a capacitor, producing a detectable voltage.

Several parameters affect device performance, including dead layer thickness, depletion region thickness, device capacitance, and readout speed and flexibility. Dead-layer Thickness

As an energetic particle penetrates silicon, it gradually loses its energy and generates electron-hole pairs. The electron-hole pairs generated in the depletion region will be separated by the applied electric field and detected. However, the depletion region does not extend completely to the surface. There is a “dead layer” near the surface, and electron-hole pairs generated in this region will be collected with only limited efficiency, or not at all. This is particularly important for the detection of low energy particles, since low energy particles penetrate only a short distance into the silicon before their energy is dissipated, and thus all of the electron-hole pair generation is relatively near the surface.

The dead layer has two components, the undepleted silicon layer and the surface depletion layer. The undepleted layer includes the n-type or p-type layer in the PIN structure that is not depleted by the applied electric field. Some thickness of undepleted silicon is needed to serve as a contact in order to apply the electric field. Since it is undepleted, this region is field free, and there is an abundance of majority carriers, both factors contributing to loss of signal. The abundance of majority carriers makes it likely that the device must rely on diffusion alone to remove minority carriers from the region. This means a significant fraction of the generated minority carriers will not be detected, but will remain in the undepleted region until they recombine.

There will also be a region at the surface depleted by the surface states. In contrast to the main depletion region set up by the applied electric field, the electric field that exists in the surface depletion region drives generated carriers to the surface or to the undepleted region where they recombine, rather than to the opposite electrodes where they can be detected.

Depletion Layer Thickness

The thickness of the main depletion region determines the fraction of charge collected for high energy particles and the collection efficiency for hard X-rays. If the material is too thin, high energy particles will travel completely through the depletion region without being stopped, and so only a fraction of their energy will be deposited there. Similarly, a thin depletion layer will provide a small collection volume for high energy X-rays, and a significant fraction of the X-ray photons will not be detected, instead being either completely transmitted or absorbed in insensitive parts of the detector.

Also, for back illuminated devices, the generated carriers must travel from the back to the front side without recombining. This requires that the device be depleted from the front to the back. The thickness of the wafer must be such that it can be depleted from front to back with a practical applied voltage.
Device Capacitance

The amount of charge collected is dependent on the energy of the particle or photon. This produces a voltage equal to the charge divided by the capacitance of the detector. The larger the capacitance, the smaller the voltage signal for a given charged particle. Since the readout electronics normally have a fixed noise voltage, and the voltage signal must be larger than this voltage noise for proper discrimination, the detector capacitance determines the minimum detectable charge for a given readout voltage.

Readout Speed and Flexibility

The particles impinge randomly on the detector array, each particle generating a charge proportional to its energy. If the collector detects 1000 electrons in one read cycle, however, it cannot discriminate between 1 particle that generates 10000 electrons, or 10 particles that each generate 100 electrons. Therefore, the detector readout must be fast enough so that only one (or at most a few) events happen per each pixel per readout cycle.

A delta-doped hybrid advanced detector (“HAD”) is provided which includes a diode array formed from high resistivity silicon. A high energy particle passing through the silicon generates a cloud of electron-hole pairs that can be collected as signal charge. The construction of the detector allows the detector to see low energy particles and high energy particles simultaneously.

The detector uses the delta-doping scheme first developed for delta-doped charge coupled devices (“CCDs”). Delta-doping places a highly doped layer at the surface to terminate the charge-collecting region to extend throughout the thickness of the device. The high resistivity diodes of the HAD can accomplish this without requiring thinning, eliminating the difficult processing step as well as leaving a large collection volume for detecting X-rays and high energy particles that can be collected as signal charge. The construction of the detector allows the detector to see low energy particles and high energy particles simultaneously.

The detector uses the delta-doping scheme first developed for delta-doped charge coupled devices (“CCDs”). Delta-doping places a highly doped layer at the surface to terminate the charge-collecting region to extend throughout the thickness of the device. The high resistivity diodes of the HAD can accomplish this without requiring thinning, eliminating the difficult processing step as well as leaving a large collection volume for detecting X-rays and high energy particles that can be collected as signal charge. The construction of the detector allows the detector to see low energy particles and high energy particles simultaneously.

A new pixel guarding technique may be used to preserve a low effective input capacitance on the APS readout, even with relatively large bump bond pads on the input node. This preserves the high conversion gain which results in high away collected charge to reset the pixel after the readout is performed.

A delta-doped hybrid advanced detector (“HAD”) is provided which includes a diode array formed from high resistivity silicon. A high energy particle passing through the silicon generates a cloud of electron-hole pairs that can be collected as signal charge. The construction of the detector allows the detector to see low energy particles and high energy particles simultaneously.

The capacitance of the detector surface, and is only a single atomic sheet. This single atomic layer of high doping allows the detector to see low energy particles and high energy particles simultaneously.

The capacitance of the detector surface, and is only a single atomic sheet. This single atomic layer of high doping allows the detector to see low energy particles and high energy particles simultaneously.

An APS is made using the complementary metal oxide silicon (“CMOS”) process and/or other techniques, such as NMOS, that are compatible with CMOS. Since this is the standard technology used for the fabrication of computer chips and analog integrated circuits, industrial foundries exist that can fabricate APS chips, requiring only a computer-generated layout design file. The CMOS process can be used to make integrated circuit diodes, as well as p-channel and n-channel field-effect transistors. The APS is ordinarily a very important component of silicon photodiode or photogate collects image charge produced by visible light, and the signal receives power amplification from an fitter transistor amplifier in each pixel. Two additional transistor switches are used in the pixel. One connects each pixel in turn to a readout line, allowing circuitry to raster scan through the array. The other transistor drains away collected charge to reset the pixel after the readout is completed.
bonds, and readout electronics.

Other advantages will be apparent from the description below and the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a known silicon PIN diode for detecting energetic particles.

FIG. 2 shows a schematic cross-section of the delta-doped HAD. The detector diode array is connected through indium bump bonds to a CMOS APS readout electronics chip.

FIG. 3 shows an electrical schematic cross-section of the delta-doped HAD, including the detector diode array, bump bonds, and readout electronics.

FIG. 4 shows a schematic cross-section and band structure of a detector before delta doping.

FIG. 5 shows a schematic cross-section of a detector diode after delta doping.

FIG. 6 shows a plot of the quantum efficiency of a thinned, backside-illuminated, and delta-doped CCD as a function of incident light wavelength.

FIG. 7 shows a layout of a CMOS APS readout chip according to an embodiment of the present invention.

FIG. 8(a) shows a schematic of a prior art readout pixel.

FIG. 8(b) shows a schematic of a guarded bump-bonded pixel according to an embodiment of the present invention.

DETAILED DESCRIPTION

The structure of the delta-doped HAD 20 according to an embodiment of the present invention is shown in FIG. 2. A detector diode array 20 according to an embodiment of the present invention is fabricated from high-resistivity silicon connected through indium bump bonds to a readout array fabricated using a standard foundry CMOS process.

The diode array 20 is fabricated from a wafer of high resistivity silicon approximately 300 μm thick that is very lightly p-doped, to a concentration of about 10^{12} dopant atoms per cubic centimeter. A bulk 22 of this wafer remains undoped, and forms the intrinsic or “I” region. An exposed first surface 24 of the diode array 20 is uniformly delta-doped with dopants of a first conductivity, such as boron, forming a continuous “P” region. The opposite second side of the wafer is pixelated into a number of separate diodes 26 using a number of dopants of a second conductivity, in this case n+ implants 28, forming the “N” regions. Together, these structures form an array of PIN diodes 26.

By applying a voltage of approximately 100 V, the lightly doped intrinsic region can be completely depleted, resulting in an electric field across its entire 300 μm thickness. Carriers generated in the intrinsic region are swept out by this electric field to form the signal current.

There is an indium bump 30 on each of the n+ diodes 26, and a corresponding indium bump 32 in each pixel 34 of the readout chip 36. The two chips 20 and 36 are aligned and pressure is applied, which pressure welds the corresponding indium bumps 30 and 32 together. This connects the diode array chip 20 and the CMOS APS readout chip 36 both electrically and mechanically, resulting in a hybrid.

An electrical schematic is shown in FIG. 3. The readout chip 36 uses a single transistor 38 connected as a source-follower in each readout pixel to buffer the signal from the diode array 20. The n+ implant 28 of the diode array 20 is connected through the bump bond 30 and 32 to the gate of this source-follower 38. A select transistor 40 is located in each pixel and acts as a switch. When enabled in turn, the select transistor 40 connects the source of the buffer transistor 38 to a common column bus 42 for output. There is also a reset transistor 44 connecting the buffer transistor 38 gate to a common reset voltage 46. When enabled, the reset transistor 46 drains off any signal charge, and restores the gate and diode to the reset voltage level.

1. Pixelated High-resistivity Silicon Diodes

The detector diodes 26 are fabricated from a chip of high resistivity silicon. The low doping of the chip allows the active depletion region to extend through the entire 300 μm thickness of the chip, providing a large depletion depth for the detection of high energy particles and X-rays. The large depletion depth also eliminates the need for wafer thinning of the detector.

In addition, the detector diode chip may be divided into square pixels rather than long strips. Square pixels reduce the area of the diode resulting in a reduction of the capacitance. The capacitance of a 50 μm x 50 μm diode with a 300 μm depletion depth (using the relative dielectric constant of silicon of 11.8) is about 0.87 femtofarads.

2. Delta-doping

The exposed surface of the high resistivity silicon is delta-doped. Delta-doping greatly decreases the dead layer at the detector surface, and allows the collection of charge from low energy particles 54 and UV photons 56 that produce charge very near the surface.

A schematic cross section and band structure of a detector structure without delta doping is shown in FIG. 4. A native oxide layer 58 is apparent on the exposed surface 60 of the chip. A backside potential well 52 of at least 0.5 μm exists that acts as a dead layer. The potential well traps carriers created near the surface 60, making the detector blind to UV photons and low energy particles. FIG. 4 also shows the conduction band 62, the valence band 64, and the Fermi level 66.

The resulting potential well after delta-doping is shown in FIG. 5. As may be seen in that figure, the backside dead layer is reduced to a few angstroms.

The resulting effect on quantum efficiency for UV photons is demonstrated in FIG. 6. FIG. 6 shows a plot of quantum efficiency versus wavelength for a thinned, back-illuminated CCD with delta-doping. The plot shows that the delta-doped detector is sensitive to wavelengths at least down to Lyman α (121.6 nm), and may extend indefinitely beyond that into the X-rays, where the absorption depth dependence reverses, increasing with decreasing wavelength. Without delta-doping, the CCD would cut off at wavelengths longer than 400 nm.

Recently, delta-doping has also been shown to dramatically reduce the low energy cut-off for detecting low energy particles. In typical silicon strip detectors, the particle energies must be greater than about 10 keV to penetrate the detector dead layer and be detected. Delta-doped CCDs are able to detect and provide energy resolution of low energy protons down to 1 keV, and of low energy electrons down to 50 eV.

3. Readout Using CMOS Active Pixel Sensor Electronics

The diode array 20 is connected by a moldable metal contact, such as by bump bonding, to a CMOS APS readout chip 36. An APS readout chip 36 may be fabricated using
a standard process available from a commercial CMOS
foudry. The schematic of the pixel electronics is shown in
FIG. 3. The layout of the readout chip 36 is shown in FIG.
7. FIG. 7 shows chip 36 including a pixel array 70, column
processing circuitry 72, and a column decoder 74. Ordinary
digital logic is used to raster scan through the pixel array.
The column processing circuitry 72 may provide for direct
incorporation of features such as double correlated sam-
pling.

The CMOS APS readout chip 36 may use only milliwatts
of power, as compared to watts for a typical CCD. It also
allows a more flexible readout scheme than the strictly
sequential readout used by a CCD. Like the CCD, however,
the CMOS APS readout chip 36 can preserve the low
capacitance of the detector diodes, resulting in a read noise
of 10 electrons or less, as opposed to hundreds or thousands
of electrons read noise for a conventional strip detector.

Guarded Bump Bond Connectors

A guarding technique may be used to reduce the capaci-
tance associated with the readout. This technique is shown
in the prior art FIG. 8(a).

In prior art FIG. 8(a), the bump-bond 32 is separated from
a metallization layer 80 by an insulator 82. The bump-bond
32 connects to a source-follower which serves as a near-
unity-gain buffer.

In the guarded pixel technique shown in FIG. 8(b), the
output of this buffer is used to power a guard metal layer 86
that lies underneath the bump bond metallization. Each pixel
may have its own guard metal. By actively forcing the area
around the bond to follow the bond potential, the effect of
parasitic capacitance is reduced by \((1-A_v)\), where \(A_v\) is the
gain of the source-follower 84. In the absence of the
feedback, the detector capacitance would be very high
causing a large increase in noise. The body of the source-
follower is also tied to the source, to reduce the body effect,
and make the gain closer to unity.

The guarded pixel readout provides a detector with high
signal-to-noise ratio ("SNR"). The high SNR is accom-
plished by minimizing the detector capacitance through
feedback from a node 87 into the guard metal.

Although the present invention has been described with
respect to specific embodiments, those skilled in the art will
recognize that variations of the embodiments also fall within
the scope of the present invention. For example, while the
device described is envisioned as a bump-bonded hybrid, it
is also possible to make a monolithic detector using a
CMOS-compatible process starting with high-resistivity sil-
icon substrates. Accordingly, the scope of the present inven-
tion is limited only by the claims appended hereto.

what is claimed is:

1. A delta-doped hybrid advanced detector, comprising:
a silicon wafer having a first surface and a second surface,
the first surface substantially uniformly doped with
dopants of a first conductivity, and the second surface
doped with dopants of a second conductivity different
from the first conductivity, in an array, to form an array
of diodes;
a readout circuit array, each circuit in the array connected
to respective ones of the array of diodes.
2. The detector of claim 1, wherein the first surface doping
is p-type.
3. The detector of claim 2, wherein the p-type doping is
boron.
4. The detector of claim 1, wherein the second surface
doping is n-type.
5. The detector of claim 1, wherein the silicon wafer and
the readout circuit array are indium bump-bonded.

6. The detector of claim 1, wherein the readout circuit
array is a CMOS device.
7. The detector of claim 6, wherein the readout circuit
array is an array of CMOS active pixel sensor devices.
8. The detector of claim 7, wherein the readout circuit
array include, for each circuit:
   a buffer transistor connected as a source-follower to buffer
   the signal from the diode array, wherein the gate of this
   buffer transistor is connected to the diodes of the array
   on the second surface;
a select transistor connected between the source of the
   buffer transistor and a common bus; and
   a reset transistor connected between the gate of the buffer
   transistor and a common reset voltage.
9. The detector of claim 1, wherein the silicon wafer is at
least partially lightly doped.
10. The detector of claim 9, wherein the light doping is on
the order of \(10^{12}\) dopant atoms per cubic centimeter.
11. The detector of claim 1, wherein each of the diodes in
the array is substantially square.
12. The detector of claim 5, further comprising:
a guard metallization layer substantially adjacent the
bump bond; and
a transistor connected between the bump bond and the
guard metallization layer,
such that the area adjacent the bump bond has a potential
substantially near the bump bond potential.
13. A method of fabricating a delta-doped detector, com-
prising:
   (A) providing a silicon wafer;
   (B) doping a first surface of the silicon wafer with dopants
of a first conductivity using CMOS fabrication tech-
niques;
   (C) doping a second surface of the silicon wafer using
CMOS fabrication techniques, with dopants of a sec-
ond conductivity, in an array of locations to form a
plurality of diodes; and
   (D) connecting a readout circuit array to the second
surface of the silicon wafer, such that respective ones of
the diodes are connected to respective ones of the
readout circuit.
14. The method of claim 13, wherein the first conductivity
is p-type and the second conductivity is n-type.
15. The method of claim 13, wherein the connecting
includes connecting a plurality of CMOS active pixel sen-
sors to ones of the array of diodes.
16. The method of claim 13, wherein the connecting
includes bump-bonding the readout circuit array to the
silicon wafer at a bump-bonding location.
17. The method of claim 16, further comprising deposit-
ing a guard metallization layer adjacent the bump-bonding
location, and connecting a transistor between the guard
metallization layer and the bump-bonding location.
18. The method of claim 13, wherein the readout circuit
array is formed by:
   depositing on a semiconductor wafer using CMOS fab-
   rication techniques;
   a buffer transistor connected as a source-follower to buffer
the signal from the diode array, wherein the gate of this
buffer transistor is connected to the diodes of the array
on the second surface;
a select transistor connected between the source of the
buffer transistor and a common bus; and
a reset transistor connected between the gate of the buffer
transistor and a common reset voltage.
19. A guarded detector with reduced capacitance, comprising:
   a metal moldable contact between a detector and a readout circuit array;
   a guard metallization layer substantially adjacent the metal moldable contact; and
   a transistor connected between the metal moldable contact and the guard metallization layer,
   such that the area adjacent the metal moldable contact has a potential substantially near the bump bond potential.

20. The detector of claim 19, wherein the metal moldable contact is an indium bump bond.

21. The detector of claim 20, wherein the readout circuit array is a CMOS device.

22. The detector of claim 21, wherein the readout circuit array is an array of CMOS active pixel sensor devices.

23. A hybrid advanced detector, comprising:
   a silicon wafer formed of a high-resistivity bulk crystal and having a first surface and a second surface, the first surface on one side of the wafer and the second surface on a second side of the wafer, the second surface doped with dopants in an array to form an array of diodes; a readout circuit array, each circuit in the array connected to respective ones of the array of diodes.

24. The detector of claim 23, wherein said first surface is substantially uniformly doped with dopants, thereby forming the delta-doped first surface.

* * * * *