The present invention discloses a new family of switching amplifier classes called “class E/F amplifiers.” These amplifiers are generally characterized by their use of the zero-voltage-switching (ZVS) phase correction technique to eliminate the loss normally associated with the inherent capacitance of the switching device as utilized in class-E amplifiers, together with a load network for improved voltage and current wave-shaping by presenting class-F impedances at selected overtones and class-E impedances at the remaining overtones. The present invention discloses a several topologies and specific circuit implementations for achieving such performance.
FIG. 4C
using active devices (i.e. transistors, vacuum tubes), that 40 voltage across the switch (and hence across the capacitance)

bandwidth, frequency response, etc. and is chosen accord-

power amplifier

arbitrarily small by choosing a faster device or increasing

switching amp1ifiers, the loss associated with

transmitters), where low Power consumption and low dis-

sipation are crucial, high efficiency switching amplifiers are allows this class to readily accommodate the switching

invention Pursuant to ARO-ARMY RESEARCH OFFICE

switching times in the active device and package parasitic

in which the Contractor has elected to retain title. sibly the most appropriate known types are class E and F

amplifier. The active device acts substantially as a switch 65 unlike the turn-on loss, this loss mechanism can be made

subject to the Provisions of public Law 96-512 (u.s.c 202)

mission system

advantages they allow. form as linear amplifiers, switching amplifiers or as a

More Particularly, RF Power amplification can be realized where C, is the capacitance shunting the switch and V is the

capacitance shunting the power switch. A capacitance, C, shunts the power switch. C, is connected to the load

device is powered by a dc power supply 3, and has an output connected to the input of the load network 7. The output of

the load network 7 is connected to the load 8, such as an antenna. As the switch 5 is cyclically operated at the desired

output frequency, or fundamental frequency, f, the dc

energy is converted into ac energy at this switching frequency and its harmonics. The load network 7 may employ

one or more filters to control the power dissipation caused by

switching action (i.e. the efficiency of the device), reduce the level of the harmonic overtones at the load, and/or provide

impedance transformation. The design of the load network determines the behavior of the voltage and currents in the

switching amplifier 6, and thus the class of operation by

which the amplifier is denoted.

Realizing highly efficient switching operation at high

frequencies, however, has been challenging due to finite switching times in the active device and package parasitic

impedances. Nonetheless, among the known types of power

amplifiers, when an application requires highly power-

efficient amplification at high operating frequencies, osten-

sibly the most appropriate known types are class E and F

amplifiers.

Class E Amplifiers

The class E amplifier achieves high efficiency at high

frequencies by essentially eliminating the dominant cause of

the switching power dissipation that occurs in other types of

switching amplifiers, namely the loss associated with capacitive discharge. In virtually every switching-mode

power amplifier, a capacitance, C, shunts the power switch.

At a minimum, this capacitance is the inherent parasitic

capacitance, C, of the circuit components (transistor) and

writing; the circuit designer might intentionally wish to add

additional capacitance. In other types of switching amplifi-

ers (other than the Class E amplifier), this shunt capacitance

is typically undesirable. The reason is that if the switch is

turned on when the voltage across the switch and its shunt

capacitance is nonzero, the energy stored in the charged

capacitance will be dissipated as heat; the energy is C, V^2/2,

where C, is the capacitance shunting the switch and V is the

voltage across the switch (and hence across the capacitance)

when the switch is turned on. If the switching frequency is

f, the power dissipation is C, V^2 f /2. Note that the power

dissipation is directly proportional to the switching frequency.

Thus, for a high-frequency power amplifier, this power
dissipation can become a severe drawback, often

becoming the dominant power loss mechanism. Moreover,

while the switch is discharging this capacitor, the switch is

subjected to both the capacitor voltage and the discharge

current, simultaneously. If the simultaneous voltage and

current are large enough, they can cause destructive failure

and/or performance degradation of the power transistor.

These difficulties can be avoided by ensuring Zero-

Voltage-Switching (ZVS) operation, i.e. demanding that the

voltage across the switch be substantially zero when the

switch is turned on. This feature of the class-E amplifier

allows this class to readily accommodate the switching
device output capacitance without seriously degrading per-
formance by using this capacitance in the load network and

designing the load network so that the capacitor voltage is

zero at just before the device turn-on.

In addition to the problems with turning on the switch,

switching off (opening) a power switch inherently subjects it to simultaneous high voltage and high current (hence

further power dissipation and device stress). Fortunately,

unlike the turn-on loss, this loss mechanism can be made

arbitrarily small by choosing a faster device or increasing

the device drive level sufficiently so as to reduce the device

device.
turn-off time. Although it is possible to design a switching amplifier to achieve ZCS (zero-current switched) operation, wherein the device current is zero just before the transistor switches off thereby eliminating turn-off loss, it is believed to be impossible to achieve ZVS and ZCS conditions simultaneously. While the turn-off loss can be reduced by other means, the turn-on loss is dependent only on the switching voltage and the capacitance, \( C_p \), which cannot be reduced arbitrarily as it is an inherent property of the active device. Therefore, ZVS switching has been found to be the most appropriate for high-efficiency operation using modern high-speed devices. By properly choosing the relative values of the circuit components (including the switch capacitance, \( C_p \), the load resistance, \( R_L \), and load inductance, \( L_p \)), class E therefore allows for ZVS switching to reduce switching loss using a very simple circuit.

Thus, with relatively simple circuit topology, class E operation achieves low power dissipation and low device stress by (a) incorporating the switch shunt capacitance as part of a network, allowing its detrimental effects to be accounted for and minimized and (b) using a resonant load network whose transient response after the switch turn-off brings the switch voltage back to zero (or nearly zero) at the time the switch will next be turned on. A schematic of a typical class E amplifier circuit is shown in the simplified diagram of FIG. 2. The power amplifier 10 includes a switching device 12 and a load network 20. DC power is supplied to the device 12 via a choke 14. The network includes a simple filter 24 which is connected in series to an RL load, represented by \( L_p \), \( R_L \), respectively. As a class E device, the filter acts as a short circuit at the fundamental frequency, and an open circuit at all harmonics. The inherent shunt capacitance, \( C_{out} \), of the active device 12 (e.g. between the anode and cathode of a three terminal transistor) is incorporated into the network as all or part of capacitor \( C_2 \) which may include additional capacitance added by the designer. Thus, the impedance looking into the load network, \( Z_{out} \), is: \( f_o \), \( Z_{out}=R_s+j\omega L_p \) \| \( (1+j\omega C_o) \) which if properly designed is a substantially inductive load (i.e. a load consisting of both a resistance and an inductance), i.e. \( Z_{out}=R_s+j\omega L_p \) and at all harmonic overtones, \( Z_{out}=1/j\omega C_s \). The inductance of the fundamental frequency load, when properly sized relative to the capacitance \( C_p \) and the effective load resistance \( R_{eq} \) performs a phase correction of the fundamental frequency harmonic components, allowing the ZVS operation to be achieved.

### Class F and F-1 Amplifiers

Class F is another well-known class of switching mode amplifiers. The class F amplifier derives its improved efficiency by using a multiple resonator load network to control the harmonic content of the active device’s output voltage and/or current waveforms. In realizing a class F circuit, the active device operates primarily as a switch and the load network, generally, is designed to yield open-circuit impedances at odd harmonics of the fundamental frequency and short circuit impedances for even harmonics and/or current waveforms. This results in a combination of higher efficiency and higher power output. Additionally, resonant circuits are provided at all even harmonics up to the \( N^{th} \) harmonic to short circuit the active device at these frequencies, thereby allowing the current waveform to approximate a half-sinusoid, further increasing the efficiency without any decrease in output power. A high Q filter circuit is tuned to the fundamental frequency to reject harmonics at the load and yield a sinusoidal output signal. In this configuration, the device’s inherent parasitic capacitance must be kept small in order to avoid shorting the resonant circuit at the odd harmonics. Although this problem can be somewhat minimized by resonating this capacitance with the load network, this technique further increases the complexity of the network. Additionally, if the active device is to be driven very hard so that it switches very quickly, a large number of harmonics must be tuned in order to achieve the benefit of class F operation. As a consequence of these limitations, class F is normally used only in applications where the transistor speed is relatively slow compared to the frequency of operation and using relatively small (i.e. low capacitance) devices, so that only a few harmonics need be tuned and so that the effect of the capacitance is small.

A variation to the conventional class F amplifier is to invert the impedances at the harmonic overtones. Thus, the load network is designed to yield open circuit impedances at every even harmonic up to the \( N^{th} \) harmonic and short circuit impedances at every odd harmonic up to the \( N^{th} \) harmonic. Such an amplifier is called the inverse class-F, or class F-1 amplifier and one implementation is shown schematically in FIG. 3. In particular, this class F-1 amplifier 40 includes a switching device 42 and load network 50 that comprises a filter 46 in series with the output of the switch and the resistive load 52 and a second filter 48 in parallel with the load 52. The series filter 46 presents relatively open circuit impedances for even harmonics and short circuit impedances for all other harmonics. The parallel filter 48 presents relatively short circuit impedances for all odd harmonics and open circuit impedances otherwise. Thus, the impedance looking into the load network, \( Z_{out} \), is: \( f_o \), \( Z_{out}=R_s \) at all even harmonics \( Z_{out}=0 \) (open); and at all odd harmonics \( Z_{out}=0 \) (short). This amplifier class has many of the benefits of class F, and additionally has the property of near-ZVS operation, although this quality is difficult to achieve in the presence of a large parasitic device capacitance \( C_{out} \). Although class F-1 has been largely ignored for many years, several recent works have shown that this class of operation compares favorably to class F using modern solid-state devices.

When class E and F power amplifier performances are compared, a significant advantage of a class E amplifier over a class F amplifier is its circuit topology, which incorporates the switching device output parasitic capacitance as part of its circuit. Thus, class E amplifiers do not lose power efficiency due to the charging and discharging of this parasitic capacitor as can occur in amplifier classes such as class F and class F-1 which do not account for the capacitor’s effect, nor do they require elaborate resonant circuits to reduce the effect of this capacitance. In addition, as seen above, the class E design is relatively simple, consisting of just a few components (at least one less filter than in the class F design). Unlike class F and F-1 designs, the class E design receives the full promised benefits of its operating class with this simple circuit, whereas the class F and F-1 approaches
must incorporate increasingly larger numbers of circuit elements in order to approach the ideal class F performance. On the other hand, due to its anode (i.e., transistor drain or collector) voltage and current wave forms, class F amplifiers deliver significantly higher power and promise higher power-efficiency than class E amplifiers when they are using the same transistor under the same supply conditions. To gain this advantage, class F and F^-1 circuits can be quite complex and can use many more components than class E devices.

Thus, it would be highly desirable to have a power amplifier capable of very efficiently providing high power at high frequencies and that incorporates some of the best features of both class E and class F amplifiers.

SUMMARY OF THE INVENTION

The present invention, which addresses these needs, resides in a high efficiency switching power amplifier for amplifying a high frequency input signal having at least one fundamental frequency, and that is adapted to drive a load. The amplifier includes a high-speed active device and a hybrid class E/F load network. The active device comprises a switching component that operates substantially as a switch and a parasitic capacitance, \( C_{\text{out}} \), in parallel with the switching component. The hybrid class E/F load network connected to the active device.

In one embodiment, the hybrid class E/F load network is configured to present to the switching component of the active device, at all harmonic frequencies substantially present in at least one of the voltage and current waveforms of the active device, a substantially inductive load at each fundamental frequency, a substantially open circuit at a predetermined number, \( N_{o} \), of even harmonic overtones of each fundamental frequency, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an \( N_{o} \). In this embodiment, \( N_{o}=1 \), then \( N_{o}=0 \).

More specifically, the load network includes a two port filter network having an input port and an output port, the input port being connected to the active device in parallel with the parasitic output capacitance of the active device and the output port being connected to the load. The load network may also be configured to provide wideband tuning of an input signal having a fundamental frequency range from \( f_{1} \) to \( f_{2} \), where \( f_{1}<f \leq f_{2} \).

In another embodiment of the present invention, the hybrid class E/F load network connected to the active device is configured to present to the active device a substantially inductive load at the fundamental frequency of operation, a substantially open circuit at a predetermined number of even harmonic overtones of the fundamental frequency, a substantially short circuit at a predetermined number of odd harmonic overtones of the fundamental frequency, and a substantially capacitive impedance load at the remaining harmonic overtones.

In yet another implementation of the present invention, the hybrid class E/F load network is configured to present to the switching component, at all harmonic frequencies that are substantially present in at least one of the voltage and current waveforms of the active device, a substantially inductive load at each fundamental frequency of operation that results in substantially zero-voltage-switching (ZVS) operation of the active device, impedances substantially larger in magnitude than \( 1/(2\pi f_{c}C_{\text{out}}) \) at a predetermined number, \( N_{e} \), of even harmonic overtones of each fundamental frequency, impedances substantially smaller in magnitude than \( 1/(2\pi f_{c}C_{\text{out}}) \) at a predetermined number, \( N_{o} \), of odd harmonic overtones of each fundamental frequency, and an impedance substantially equal to \( 1/(2\pi f_{c}C_{\text{out}}) \) at the remaining harmonic overtones of each fundamental frequency.

In yet another implementation of the present invention, a multiple active device high efficiency switching power amplifier for amplifying a high frequency input signal having at least one fundamental frequency and adapted to drive a load is disclosed. In this case, a first high-speed active device has a parasitic output capacitance, \( C_{\text{out}} \), and adapted to operate substantially as a switch, and a second high-speed active device having a parasitic output capacitance, \( C_{\text{out}} \), and adapted to operate substantially as a switch, are provided together with a hybrid three-port class E/F load network. The network has a first port connected to the first active device, a second port connected to the second active device, and a third port connected to the load, such that when the first and second active devices are driven in a push-pull configuration, the network presents to the switching component of the active device an effective input impedance that provides a substantially inductive load in series with the substantially resistive load at all fundamental frequencies; a substantially open circuit at one or more even harmonics for each fundamental frequency up to an \( N_{o} \) harmonic, a substantially short circuit at one or more odd harmonics for each fundamental frequency up to an \( N_{o} \) harmonic, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an \( N_{o} \) harmonic.

In a more detailed implementation of the push-pull amplifier, the amplifier further includes a transformer connected to the outputs of the two active devices and the load such that the load is dc isolated from the outputs of the two active devices via the transformer.

In a detailed embodiment of one aspect of the present invention, a quasi-class E/F high efficiency amplifier for amplifying an input signal having at least one fundamental frequency and adapted to drive a load is disclosed. This amplifier includes a high-speed active device that comprises a switching component that operates substantially as a switch and a parasitic capacitance, \( C_{\text{out}} \), in parallel with the switching component and an LC parallel tank circuit that is resonant at the second harmonic of the fundamental frequency. The active device is connected in series to the load through the LC parallel tank circuit.

A method of amplifying an RF signal with an active device switch is also disclosed. The method includes amplifying the signal with an active device that comprises a switching component that operates substantially as a switch and a parasitic capacitance, \( C_{\text{out}} \), in parallel with the switching component. The method includes tuning the amplified signal to provide a substantially inductive load to the switching component at the fundamental frequency, tuning the amplified signal to provide a substantially open circuit to the active device at selected even harmonic overtones, tuning...
the amplified signal to provide a substantially short circuit to the active device at selected odd harmonic overtones; and providing substantially capacitive loading to the active device for the non-selected harmonic overtones.

Several detailed implementations of the hybrid class E/F load network of the amplifier of the present invention are disclosed. In one embodiment, the network is configured to present to the switching component, at all harmonic frequencies substantially present in at least one of the voltage and current waveforms of the active device, a substantially inductive load at each fundamental frequency, a substantially open circuit at the 2nd harmonic, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥3.

In an alternative implementation, the network is configured to present to the switching component, a substantially inductive load at each fundamental frequency; a substantially short circuit at the 3rd harmonic, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥3.

In a third detailed implementation, the hybrid class E/F load network is configured to present to the switching component a substantially inductive load at each fundamental frequency, a substantially open circuit at the 3rd harmonic, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥4.

In a fourth detailed embodiment, the hybrid class E/F load network is configured to present to the switching component a substantially open circuit at the 4th harmonic, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥4.

In a fifth detailed embodiment, the hybrid class E/F load network is configured to present to the switching component a substantially inductive load at each fundamental frequency a substantially open circuit at the 4th harmonic, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥4.

In a sixth embodiment, the hybrid class E/F load network is configured to present to the switching component a substantially inductive load at each fundamental frequency a substantially short circuit at the 3rd harmonic, a substantially open circuit at the 4th harmonic, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥4.

In a seventh detailed embodiment, the hybrid class E/F load network is configured to present to the switching component a substantially inductive load at each fundamental frequency a substantially short circuit at the 3rd harmonic, a substantially open circuit at the 2nd and 4th harmonics, and a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥4.

In an eighth detailed embodiment, the hybrid class E/F load network is configured to present to the switching component a substantially inductive load at each fundamental frequency a substantially short circuit at all odd harmonic overtones up to an Nth harmonic, a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥5.

In a ninth disclosed detailed embodiment, the hybrid class E/F load network is configured to present to the switching component a substantially inductive load at each fundamental frequency a substantially short circuit at all odd harmonic overtones up to an Nth harmonic, a substantially capacitive impedance load at the remaining harmonic overtones, up to a predetermined number, N_s, of even harmonic overtones for each fundamental frequency up to an Nth harmonic, a substantially capacitive impedance load at the remaining harmonic overtones, up to an Nth harmonic, where N≥5 and 0≤N_s≤(N-2)/2.

Other features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified block diagram of conventional RF power transmission system that incorporates a switching power-amplifier connected to a load;

FIG. 2 is a conceptual block diagram of a conventional class E power amplifier circuit;

FIG. 3 is a conceptual block diagram of a conventional class F power amplifier circuit;

FIG. 4 is a conceptual block diagram showing one circuit topology of the novel class E/F power amplifier of the present invention;

FIG. 4B is a schematic of one preferred implementation of a novel class E/F amplifier using two resonators to accomplish the harmonic tuning;

FIG. 4C is a schematic of one preferred implementation of a novel class E/F amplifier using a dual-resonant filter to accomplish the harmonic tuning;

FIG. 4D is a schematic of one preferred implementation of a novel class E/F amplifier using using a push-pull amplifier configuration;

FIG. 5 is a conceptual schematic of an alternative design to the class E/F_dd push-pull amplifier circuit shown in FIG. 4, wherein the load is coupled to the circuit via a transformer;

FIG. 7 is a conceptual schematic of a class E/F_dd push-pull amplifier which is an improvement to the circuit shown in FIG. 5, wherein even harmonic tuning is included;

FIG. 8 is a conceptual schematic a class E/F_dd amplifier, which is yet another improvement push-pull amplifier circuit shown in FIG. 5, wherein second harmonic tuning is included; and

FIG. 9 is a conceptual schematic of a novel quasi class E/F amplifier circuit designed according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention allows the achievement of higher performance than either the conventional class E or class F-3 amplifiers by incorporating some of the best features of both in a single design.

In general, the present invention employs the inductive-load phase correction technique of the class E amplifier to achieve ZVS switching conditions in the presence of a significant active device output capacitance, while simultaneously allowing some of the harmonic tuning benefits of the class F-3 amplifier. The invention allows the efficiency and output power of the active device to be improved by tuning some of the harmonics like a class-F-1 amplifier (i.e. open-circuit for even harmonics, short-circuit for odd harmonics), while allowing the remaining un-tuned harmonics to be capacitive as in a class-E amplifier. Since the
un-tuned harmonics are capacitive, this tuning strategy allows the device capacitance to be easily incorporated into the circuit as in class-E, and the circuit can remain relatively simple since tuning circuits are required only for those harmonics tuned to open-circuit or short-circuit. Like class-E amplifiers, the amplifiers of the present invention may approach 100% efficiency with a simple circuit consisting of a finite number of elements, whereas class-F and class-F-1 designs can only approach 100% as the number of harmonics tuned approaches infinity. Additionally, the invention allows ZVS operation by tuning the fundamental frequency to present an inductive load (i.e. a load consisting of both an inductance and a resistance) to the device, where the inductance and resistance are appropriately sized relative to the capacitance \( C \), so as to offset the capacitive effect of the un-tuned harmonics and bring the voltage to zero just before the switch closes each cycle. This inductance can be achieved by placing an appropriately-sized inductor in series with the load, but other solutions such as a shunt inductor or transmission line segments may also be used and are thus within the scope of the present invention.

The topology of one such preferred embodiment is seen in FIG. 4. The switching power amplifier 100 includes an active device. The active device comprises a switching component 102 that operates substantially as a switch (hereinafter the term “switch” will be used interchangeably with the term “switching component” to denote that portion of the active device that operates substantially as a switch) and a parasitic capacitance, \( C_{\text{par}} \), in parallel with the switching component. It should be understood that in all of the following implementations of the present invention, the impedances presented are with respect to the switching component of the active device and thus includes the inherent parasitic capacitance of the device. Moreover, the term active device is to be understood in the broadest sense to include any appropriate three terminal active device such as a FET or CMOS transistor.

The device is connected to an output circuit load network 110. The network includes an even harmonic filter 108 in series with a “negative capacitance” filter 107, which are in parallel with the switch 102 and the shunt capacitance, denoted as \( C_{\text{sh}} \) (which may equal \( C_{\text{par}} \), the switch’s inherent capacitance or may be \( C_{\text{par}} \)+added capacitance), an odd harmonic filter 111 also in parallel with the switch, a fundamental frequency filter 112 in series with the output of the switch and the load and added inductance \( L_{s} \) in series with the primary resistive load 116. The even harmonic filter 108 presents a substantially short circuit at selected even harmonics and an open otherwise. Thus, at these harmonics the “negative capacitance” filter 107, having an impedance \(-1/joC_{s}\), at these harmonics is in parallel with the shunt capacitance \( C_{\text{sh}} \) with an impedance \( 1/joC_{s} \), and so the combined impedance of these two elements is substantially equal to an open-circuit. The odd harmonic filter 111 presents a short circuit at the selected odd harmonics and an open otherwise, short-circuiting the active device at these harmonics. The series fundamental frequency filter 112 presents to the switch a short circuit at the fundamental frequency and an open circuit otherwise. The phase-control inductance, denoted as inductor \( L_{s} \), is placed in series with the resistive load, denoted as resistor \( R_{s} \), 116.

Taken together, as seen in FIG. 4, this network thus presents a substantially inductive load at the fundamental frequency \((Z_m=\omega L_{s})\) and capacitively impedance to ground at the remaining overtones \((Z_{m=\infty}>1/joC_{s})\). Power amplifiers using this novel technique and topology will be classified as class E/F amplifiers. As this topology covers a family of amplifiers, specific implementations may be denoted as class E/F_{1,2,4,m} wherein the various subscripts are numbers denoting the harmonics for which the amplifier’s load network has class F-1 impedances. For instance, class E/F_{2,3,5} would describe an amplifier with a load network presenting to the active device an inductive load at the fundamental, open circuit at the second harmonic, short circuit at the third and fifth harmonics, and a capacitive load for the remaining overtones.

The advantages of this new class of amplifiers are numerous and may include: (a) higher efficiency and/or output power when compared to a similar class E amplifier; (b) reduced circuit complexity with correspondingly lower efficiency and/or output power when compared to a similar class F or class F-1 amplifier; (c) reduced peak voltage relative to the DC voltage when compared to a similar class E amplifier; (d) reduced peak current relative to the DC current when compared to a similar class E amplifier, and (e) allows for the incorporation of the switch’s parasitic capacitance into the circuit while simultaneously achieving zero voltage switching (ZVS), unlike a class F or class F-1 amplifier.

Moreover, the number of even and odd harmonic overtones that are controlled may be adjusted. Realizing that higher-order harmonics tend to have less effect on the efficiency than the lower-order ones, and that the finite active device switching speed will effectively reduce the generation of higher-frequency harmonic components, the class E/F switching power amplifier of the present invention may include a switching device connected to the output circuit presenting an inductive load at the fundamental frequency, an open circuit at selected even harmonic overtones up to \( N^{th} \) harmonic, shorts to ground at selected odd harmonic overtones up to \( N^{th} \) harmonic, and capacitive loads at the remaining overtones up to the \( N^{th} \) harmonic. The impedances of the output circuit above \( N^{th} \) harmonic may be any impedance where \( N \) is a number equal to or greater than 3.

It should be understood that the advantages of the present invention are measured relative to the performance characteristics of conventional class E and class F (and/or F-1) power amplifiers. Although the performance is generally best when tuned-harmonics have been completely short-circuited or open-circuited, this condition is not usually possible to achieve in practice and the designer must be content with reducing or increasing the magnitude of the impedances as much as possible respectively. Thus the present invention broadly contemplates load networks that present impedances other than those described in connection with FIG. 4. Thus, for example, the filters 108, 110 and 112 of FIG. 4 may be designed to present (a) impedances larger than those presented by class E amplifiers at selected even harmonic overtones \((Z_{m}>1/joC_{s})\) but not necessarily infinite), (b) impedances that are smaller than those presented by class E amplifiers \((Z_{m}<1/joC_{s})\) at selected odd harmonic overtones \((Z_{m}=1/joC_{s})\) at the remaining overtones. Again, the resistance and inductance of the inductive load at the fundamental frequency are selected so as to achieve ZVS switching conditions. Such amplifiers may be classified as “quasi-class E/F” power amplifiers. It should be understood by those skilled in the art that these amplifiers can be easier to design and implement than their similar class E/F amplifiers.
filter counterparts shown in FIG. 4 as they can use fewer components and lower quality components. They may even provide better performance than "true" class B/F amplifiers for some applications, such as when design factors (e.g., available component sizes, low component quality factors, etc.) other than the active device efficiency and output power are motivating the requirements of the load network.

Specific Implementations

The novel circuit topology of the present invention may be implemented in a variety of circuits. Single-active-device designs such as shown in FIG. 4 can be used to implement E/F designs in a very straightforward manner. For instance, to construct an E/F amplifier, a circuit such as shown in FIG. 4B may be employed. The circuit consists of the active device 102 in parallel with a shunt capacitance C, 106, to which are connected a series LC resonator 111 tuned to short-circuit the third harmonic, and an inductive load, through a second series LC resonator 112 tuned to resonate at the fundamental frequency. The inductive load consists of the load to be driven R, 116 and a phase-correction inductor L, 114. A choke 104 provides connection to the dc power supply. Thus the circuit satisfies the E/F conditions by providing to the switch a short-circuiting at the third harmonic, an inductive load at the fundamental, and capacitive impedances at the remaining harmonics. It should be understood that the capacitance C, may not be an explicit component added by the designer, but may consist partially or entirely of the active device's parasitic output capacitance. Of course, many variations of this circuit are readily devised by one skilled in the art, such as combining the inductance of the fundamental frequency resonator 112 and the phase-correction inductor, L, 114 into one component, thereby reducing the component count.

FIG. 4C shows another example of a single-active-device design, in this case an E/F amplifier implementation. This circuit consists of the active device 102 connected to a capacitance C, and three resonant circuits. The first resonant circuit is a series LC filter 111 tuned to the third harmonic so as to short-circuit the active device at this frequency. The second is also a series LC resonator 113 tuned to the second harmonic, which is connected to the active device in series with an inductor 115 with a value of \( \frac{1}{4\omega_0^2 C_5} \). This circuit will provide the active device with an open-circuit at the second harmonic by resonating with the capacitance C, at this frequency. The third circuit is a series LC resonator 112 tuned to the fundamental frequency, to which is connected an inductive load consisting of an inductance L, 114 and the resistive load to be driven R, 116. A choke 104 provides connection to the dc power supply. Thus the circuit satisfies the E/F conditions by open-circuiting the active device at the second harmonic, short-circuiting the active device at the third harmonic, providing an inductive load at the fundamental, and providing capacitive impedances at the remaining harmonics. Again, it should be understood that the capacitance C, may not be an explicit component added by the designer, but may consist partially or entirely of the active device's parasitic output capacitance.

Such direct implementations as shown in the previous two examples are not the only means to implement class E/F amplifiers. For instance, FIG. 4D shows an alternate implementation for E/F amplifier using a dual-resonant filter network 118 to accomplish both second and third harmonic tunings. Such a filter can be implemented as shown in the figure using only two inductors L, and L, and one capacitor, C,. This network also passes dc currents, and so it can also replace the choke by placing it between the active device and the dc voltage supply. The fundamental frequency filter, shunt capacitance and load inductance are similar to the equivalent components in FIGS. 4B and 4C.

Moreover, a very wide range of E/F designs can be accomplished using push/pull techniques. Due to the different symmetries of the even and odd harmonics of push/pull amplifiers, the push/pull approach can greatly simplify the selective tuning of even and odd harmonics. In one such circuit, shown conceptually in FIG. 5, the class E/F amplifier includes two switching devices 122, 126 connected in a push pull configuration, each with a shunt capacitor 124, 128, respectively. Both an inductive load 130, represented by a resistor 132 and inductor 134, and a resonant circuit 140 are connected between the switches. The filter 140 acts (a) to short-circuit the two switches together for all odd harmonic overtones, (b) as an open circuit at the fundamental, and (c) has arbitrary impedances at the remaining overtones. To provide DC power, one or more chokes 142, 144 may be placed in such a way as to allow direct current into both switches.

In FIG. 5, the loads and resonators are effectively removed from the circuit at the even harmonic overtones due to differential symmetry considerations, leaving each active device at these frequencies with a capacitive load consisting only of its shunt capacitance C, . This is because the even harmonic voltages of a push/pull amplifier's active devices must be 180° out-of-phase, thus if each is shorted to the other then both must be zero. Similarly, the fundamental frequency filter, shunt capacitance may be employed, The circuit consists of the active device 102 in parallel with a shunt capacitance C, to which is connected a series LC resonator 111 tuned to short-circuit the active device at the second harmonic, short-circuiting the active device at the third harmonic, providing an inductive load at the fundamental, and providing capacitive impedances at the remaining harmonics. Again, it should be understood that the capacitance C, may not be an explicit component added by the designer, but may consist partially or entirely of the active device's parasitic output capacitance.

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Second, the loaded Q of the LC parallel resonant circuit may be relatively low, even as low as one (although the third-harmonic in very low-Q cases is not very well shorted, making this case a quasi-class EF design). This permits the use of very low unloaded-Q inductors allowing the use of this topology for applications like Si (silicon) substrate-based integrated circuits where any typical inductor presents a very low unloaded-Q of around 5, making the use of a low loaded-Q filter a necessity. A conventional approach using a class E or class F amplifier generally requires filters with loaded Q of at least 3.

Third, the series inductor in the load may be represented as an equivalent parallel inductor and incorporated into the LC tank, reducing the number of components further.

In a variation to the circuit shown in FIG. 5, FIG. 6 shows yet another novel circuit topology of a power amplifier circuit 150 that implements the class EF amplifier with two switching devices 152, 156 connected in a push-pull configuration, each with a shunt capacitor 154, 158, respectively. In particular, connected between the switches are both the primary 170 of a transformer and a resonant circuit 160 which short-circuits the two switches together for all odd harmonic overtones, presents an open circuit at the fundamental, and has arbitrary impedances at the remaining overtones. Connected to the secondary 172 of the transformer parasitics into the design. The design, operation, and performance of such amplifiers follow exactly the principles of the class EF amplifier concept may be extended to allow also for added switching devices connected in a push-pull configuration, each with a shunt capacitor, as shown in FIG. 6. Between the switches are both a resistive load and the resonant circuit 170 and for the load inductance 164, reducing the part count and allowing for the incorporation of transformer parasitics into the design.

The design shown in FIG. 5. In this design (a) the output load is DC isolated from the switching circuit and supply; (b) the output load may be connected in unbalanced mode; and (c) the transformer turn ratio may be used to help match the switch output impedance to the load impedance.

In yet another embodiment, the present invention may use additional tuning circuits in parallel with each switch of the circuits shown in FIGS. 5 and 6 so as to selectively open circuit a number of even harmonic overtones. FIG. 7 shows a schematic diagram of a circuit 180 for accomplishing this as well as a possible implementation strategy. By placing additional circuits 210, 212 and 220, 222 which supply a suitable inductive impedance in parallel with the switching devices’ 182 and 186 parallel capacitances 184 and 188, respectively, at various even harmonic overtones, the class EF amplifier concept may be extended to allow also for the open-circuiting of any number of even harmonics, providing potential additional performance benefits. The denotation class EF\textsubscript{N1, N2, . . . oed} is suggested for such amplifiers, where the numerical subscripts identify the even harmonic overtones being open circuited. In addition to the benefits described in connection with the circuits shown in FIGS. 5 and 6, this improvement offers increased efficiency over class EF\textsubscript{ed}.

It should be understood by those skilled in the art that as a new class of amplifiers, the present invention encompasses a virtually unlimited number of specific class EF networks. However, for practical design considerations, the present invention specifically discloses several lower-order harmonic tuning networks. Specifically, these networks include those that present: (a) a substantially open circuit at the 2\textsuperscript{nd} harmonic; (b) a substantially short circuit at the 3\textsuperscript{rd} harmonic; (c) a substantially short circuit at the 3\textsuperscript{rd} harmonic and a substantially open circuit at the 2\textsuperscript{nd} harmonic; (d) a substantially open circuit at the 4\textsuperscript{th} harmonic; (e) a substantially open circuit at the 2\textsuperscript{nd} and 4\textsuperscript{th} harmonics; (f) a substantially short circuit at the 3\textsuperscript{rd} harmonic and a substantially open circuit at the 4\textsuperscript{th} harmonic; (g) a substantially short circuit at all odd harmonic overtones up to the N\textsuperscript{th} harmonic; and (h) a substantially short circuit at the 2\textsuperscript{nd} harmonic, a substantially capacitive impedance at the remaining harmonic overtones, up to an N\textsuperscript{th} harmonic, where N is greater than or equal to 5; and (b) a substantially short circuit at all odd harmonic overtones up to the N\textsuperscript{th} harmonic, a substantially open circuit at a predetermined number, \textit{Nz}, of even harmonic overtones for each fundamental frequency up to an N\textsuperscript{th} harmonic, a substantially capacitive impedance load at the remaining harmonic overtones, up to an N\textsuperscript{th} harmonic, where \textit{Nz} \equiv 5 and 0\textless \textit{Nz} \textless (N-2)/2. It is thus understood that many other networks and related circuits that tune other numbers of even and/or odd harmonics are within the spirit and scope of the invention.

In yet another improvement, circuit size and losses of the amplifier shown in FIG. 5 may be decreased by replacing the DC feed choke(s) with two inductors from the supply voltage to the respective switching devices. As shown in FIG. 8, if each inductor, 230, 232, is made to resonate at the second harmonic with the switching device’s parallel capacitors C\textsubscript{3} and C\textsubscript{4}, respectively, the resulting class EF\textsubscript{ned} amplifier benefits from decreased switch losses and possibly reduced losses due to the choke’s series resistance.

In yet another implementation of the present invention, a wideband class EF\textsubscript{ned} amplifier may be constructed in such a way as to have class EF\textsubscript{ned} impedances relative to the switch over a range of switching frequencies from f\textsubscript{1} to f\textsubscript{2}, where f\textsubscript{1} < 3 f. The circuit consists of two switching devices connected in a push-pull configuration, each with a shunt capacitor, as shown in FIG. 5. Between the switches are both a resistive load and a resonant circuit which short-circuits the two switches together for all frequencies greater than or equal to 3 f\textsubscript{1}, and approximates the required inductance to meet the ZVS requirement from f\textsubscript{1} to f\textsubscript{2}. To provide DC potential, one or more chokes may be placed in such a way as to allow direct current into both switches. Constructed in this way, the circuit works as described in connection with FIG. 5 over the switching frequency range from f\textsubscript{1} to f\textsubscript{2}.

FIG. 9 shows a novel implementation of a quasi class EF amplifier consisting of a switch or transistor 300 with parallel capacitor 302. They are connected to the supply through a choke 304. The switch or transistor is connected in series to the load 310 through an LC parallel resonant circuit 306 at the second harmonic. A filtering circuit may be added to avoid the higher order harmonic interference to the load, if the application requires it. After the component values are properly adjusted, this topology provides to the switch or transistor an inductive load at fundamental frequency, capacitive load at second harmonic, low impedance at third harmonic, and uncontrolled low impedances at higher order harmonics. This complies with requirements of quasi-class EF amplifiers and offers several advantages. First, this modified quasi-class EF circuit may be implemented using a relatively small number of components. Second, there is only one tuned component in the circuit.
Accordingly, the invention is defined only by the following claims.

1. A switching power amplifier for amplifying a high frequency input signal having at least one fundamental frequency, one or more tuned harmonics, and one or more untuned harmonics, comprising:
   a high-speed active device that includes a switching component that operates substantially as a switch; and
   a load network connected to the active device, wherein the load network provides an open circuit for even tuned harmonics, a short circuit for odd tuned harmonics, and a capacitive load for the untuned harmonics.

2. The switching power amplifier of claim 1 wherein the load network provides a substantially inductive load at each fundamental frequency.

3. The switching power amplifier of claim 1 wherein the load network provides a substantially inductive load at each fundamental frequency, and the substantially inductive load is matched to the capacitive load.

4. The switching power amplifier of claim 1 wherein the load network provides:
   a substantially inductive load at each fundamental frequency;
   a substantially short circuit at a 3rd harmonic; and
   a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 3.

5. The switching power amplifier of claim 1 wherein the load network provides:
   a substantially inductive load at each fundamental frequency;
   a substantially short circuit at a 3rd harmonic; and
   a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 4.

6. The switching power amplifier of claim 1 wherein the load network provides:
   a substantially inductive load at each fundamental frequency;
   a substantially open circuit at a 2nd harmonic and a 4th harmonic; and
   a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 4.

7. The switching power amplifier of claim 1 wherein the load network provides:
   a substantially inductive load at each fundamental frequency;
   a substantially short circuit at a 3rd harmonic; and
   a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 3.

8. The switching power amplifier of claim 1 wherein the load network provides:
   a substantially inductive load at each fundamental frequency;
   a substantially open circuit at a 2nd harmonic and a 4th harmonic; and
   a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 5.

9. The switching power amplifier of claim 1, wherein the load network provides:
   a substantially inductive load at each fundamental frequency;
   a substantially open circuit at all odd harmonics up to an Nth harmonic; and
   a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 5.

10. The switching power amplifier of claim 1, wherein the load network provides:
    a substantially inductive load at each fundamental frequency;
    a substantially short circuit at all odd harmonics up to an Nth harmonic; and
    a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 5.

11. The switching power amplifier of claim 1, wherein the load network provides:
    a substantially inductive load at each fundamental frequency;
    a substantially open circuit at all odd harmonics up to an Nth harmonic; and
    a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 5.

12. The switching power amplifier of claim 1, wherein the load network provides:
    a substantially inductive load at each fundamental frequency;
    a substantially short circuit at all odd harmonics up to an Nth harmonic; and
    a substantially capacitive impedance load at the remaining harmonics, up to an Nth harmonic, where N ≥ 5 and 0 < N ≤ (N − 2)/2.
13. A switching power amplifier for amplifying a high frequency input signal having at least one fundamental frequency, comprising:
   a high-speed active device that includes a switching component; and
   a load network connected to the active device, wherein the load network presents to the switching component, at all harmonic frequencies substantially present in at least one of the voltage and current waveforms of the active device,
   a substantially inductive load at each fundamental frequency;
   a substantially open circuit at a predetermined number, N\textsubscript{\text{E}}, of even harmonic overtones for each fundamental frequency,
   a substantially short circuit at a predetermined number, N\textsubscript{\text{O}}, of odd harmonic overtones for each fundamental frequency, and
   a substantially capacitive impedance load at a predetermined number of remaining harmonic overtones.

14. The amplifier of claim 13, wherein N\textsubscript{\text{E}} \leq 3 and 1 \leq N\textsubscript{\text{E}} + N\textsubscript{\text{O}} \leq N - 2.

15. The amplifier of claim 13, wherein if N\textsubscript{\text{E}} = 1, then N\textsubscript{\text{O}} > 0.

16. The amplifier of claim 13, wherein the load network includes a two port filter network having an input port and an output port, the input port being connected to the active device and the output port being connected to the load.

17. A method of amplifying an RF signal with a high speed active device, comprising:
   tuning a load network connected to the active device so as to provide a substantially open circuit to the active device at selected even harmonics N\textsubscript{\text{E}};
   tuning the load network signal to provide a substantially inductive load to the active device at the fundamental frequency.

18. The method of claim 17 further comprising tuning the load network to provide a substantially inductive load to the active device at the fundamental frequency.

19. The method of claim 17 wherein N\textsubscript{\text{E}} \geq 0, N\textsubscript{\text{O}} \geq 0, and the total number of tuned harmonic overtones, N\textsubscript{\text{E}} + N\textsubscript{\text{O}}, is at least one and less than the total number of harmonic frequencies substantially present.

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