SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE SENSOR

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Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

Related U.S. Application Data

Continuation of application No. 08/188,032, filed on Jan. 28, 1994, now Pat. No. 5,471,515, and a continuation of application No. 08/789,608, filed on Jan. 24, 1998, now Pat. No. 5,841,126.

Provisional application No. 60/101,678, filed on Jan. 26, 1996.

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ABSTRACT

Single substrate device is formed to have an image acquisition device and a controller. The controller on the substrate controls the system operation.

66 Claims, 10 Drawing Sheets
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FIG. 1
FIG. 2
FIG. 4A

FIG. 4B
FIG. 7
FIG. 8

256 x 256 PIXEL ARRAY

COLUMN SIGNAL CONDITIONING

DECODER

COUNTER

LATCHES

TIMING & CONTROL

ROW DRIVERS

DECODER

COUNTER

LATCHES

CLK

RUN

DEFAULT LOAD

ADDRESS

DATA MODE -5V
<table>
<thead>
<tr>
<th>Array Size</th>
<th>256 x 256</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Size</td>
<td>20.4 μm</td>
</tr>
<tr>
<td>Technology</td>
<td>1.2 μm n-well CMOS (HP)</td>
</tr>
<tr>
<td>Maximum Clock Rate</td>
<td>10 MHz</td>
</tr>
<tr>
<td>Minimum Clock Rate</td>
<td>none</td>
</tr>
<tr>
<td>Maximum Pixel Rate</td>
<td>2.5 MHz</td>
</tr>
<tr>
<td>Maximum Integration Delay</td>
<td>$16 \times 10^9$ clock periods or 1600 secs at 10 MHz</td>
</tr>
</tbody>
</table>

**FIG. 9**
1
SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE SENSOR


ORIGIN
The invention described herein was made in performance of work under NASA contract and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the contractor has elected to retain title.

FIELD OF THE INVENTION
The present invention relates to a single chip imaging sensor.

BACKGROUND AND SUMMARY OF THE INVENTION
Imaging technology is the science of converting an image to a signal indicative thereof. Imaging systems have broad applications in many fields, including commercial, consumer, industrial, medical, defense and scientific markets.

The original image sensors included an array of photosensitive elements in series with switching elements. Each photosensitive element received an image of a portion of the scene being imaged. That portion is called a picture element or pixel. The image obtaining elements produce an electrical signal indicative of the image plus a noise component. Various techniques have been used in the art to minimize the noise, to thereby produce an output signal that closely follows the image.

Size minimization is also important. The development of the solid state charge coupled device ("CCD") in the early 1970's led to more compact image systems. CCDs use a process of repeated lateral transfer of charge in an MOS electrode-based analog shift register. Photo-generated signal electrons are read after they are shifted into appropriate positions. However, the shifting process requires high fidelity and low loss. A specialized semiconductor fabrication process was used to obtain these characteristics.

CCDs are mostly capacitive devices and hence dissipate very little power. The major power dissipation in a CCD system is from the support electronics. One reason for this problem is because of the realities of forming a CCD system.

The specialized semiconductor fabrication process alluded to above is not generally CMOS compatible. Hence, the support circuitry for such a CCD has been formed using control electronics which were not generally CMOS compatible. The control electronics have dissipated an inordinate percentage of the power in such imaging devices. For example, CCD-based camcorder imaging systems typically operate for an hour on an 1800 mAh 6 V NiCad rechargeable battery, corresponding to 10.8 W of power consumption. Approximately 8 watts of this is dissipated in the imaging system. The rest is used by the tape recording system, display, and autofocus servos.

Space-based imaging systems often have similar problems. The space based systems operate at lower pixel rates, but with a lower degree of integration, and typically dissipate 20 watts or more.

The CCD has many characteristics which cause it to act like a chip-sized MOS capacitor. The large capacitance of the MOS device, for example, requires large clock swings, ΔV, of the order of 5–15 V to achieve high charge transfer efficiency. The clock drive electronics dissipation is proportional to CAV^2, and hence becomes large. In addition, the need for various CCD clocking voltages (e.g. 7 or more different voltage levels) leads to numerous power supplies with their attendant inefficiencies in conversion.

Signal chain electronics that perform correlated double sampling ("CDS") for noise reduction and amplification, and especially analog to digital converters (ADC), also dissipate significant power.

The inventors also noted other inefficiencies in imaging systems. These inefficiencies included fill factor inefficiencies, fixed pattern noise, clock pick up, temporal noise and large pixel size.

Active pixel sensors, such as described in U.S. Pat. No. 5,471,515, the disclosure of which is incorporated by reference herein, use special techniques to integrate both the photodetector and the readout amplifier into the pixel area or adjacent the pixel area. This allows the signal indicative of the pixel to be read out directly. These techniques have enabled use of a logic family whose fabrication processes are compatible with CMOS. This has enabled the controlling circuitry to be made from CMOS or some other low power-dissipating logic family.

The inventors of present invention have recognized techniques and special efficiencies that are obtained by specialized support electronics that are integrated onto the same substrate as the photosensitive element. Aspects of the present invention include integration, timing, control electronics, signal chain electronics, A/D conversion, and other important control systems integrated on the same substrate as the photosensitive element.

It is hence an object of the present invention to provide for the integration of an entire imaging system on a chip.

BRIEF DESCRIPTION OF THE DRAWINGS
FIG. 1 shows a basic block diagram of a CMOS active pixel circuit;
FIG. 2 shows a graph of typical APS quantum efficiency;
FIG. 3 shows the block diagram of the overall chip including drivers and controlling structures;
FIGS. 4A and 4B show the timing diagrams for photogate operation and photodiode operation, respectively;
FIG. 5 shows a schematic of the active pixel sensor unit cell and readout circuitry;
FIG. 6 shows a timing diagram for setup and readout;
FIG. 7 shows a drawing of an actual layout of the pixel and control circuitry;
FIG. 8 shows a block diagram of a CMOS APS chip; and
FIG. 9 shows an exemplary pixel layout.

DESCRIPTION OF THE PREFERRED EMBODIMENTS
An active pixel sensor is herewith described with reference to FIGS. 1–4.

A block diagram of a CMOS active pixel circuit is shown in FIG. 1. The device has a pixel circuit 150, and a column circuit 155. Incident photons pass through the photogate ("PG") 100 in the pixel circuit 150 and generate electrons which are integrated and stored under PG 100. A number of the pixel circuits are arranged in each row of the circuit. One of the
rows is selected for readout by enabling the row selection transistor 102 ("RS").

In the preferred embodiment, the floating diffusion output node 104 ("FD") is first reset by pulsing reset transistor ("RS"). The resultant voltage on FD 104 is read out from the pixel circuitry onto the column bus 112 using the source follower 110 within the pixel. The voltage on the column bus 112 is sampled onto a first holding capacitor 114 by pulsing transistor SHR 116. This initial charge is used as the baseline.

The signal charge is then transferred to FD 104 by pulsing PG 100 low. The voltage on FD 104 drops in proportion to the number of photoelectrons and the capacitance of FD. The new voltage on the column bus 112 is sampled onto a second capacitor 118 by pulsing SHR 120. The difference between the voltages on first capacitor 114 and second capacitor 118 is therefore indicative of the number of photoelectrons that were allowed to enter the floating diffusion.

The capacitors 114, 118 are preferably 1–4 pF capacitors. All pixels on a selected row are processed simultaneously and sampled onto capacitor at the bottom of their respective columns. The column-parallel sampling process typically takes 1–10 µsec, and preferably occurs during the so-called horizontal blanking interval of a video image.

Each column is successively selected for read-out by turning on column selection p-channel transistors ("CS") 130. The p-channel source-followers 122, 124 in the column respectively drive the signal (SIG) and horizontal reset (RSR) bus lines. These lines are loaded by p-channel load transistors which can be sent directly to a pad for off-chip drive, or can be buffered.

Noise in the sensor is preferably suppressed by the above-described correlated double sampling ("CDS") between the pixel output just after reset, before and after signal charge transfer to FD as described above. The CDS suppresses kT/C noise from pixel reset, suppresses 1/f noise from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage.

The inventors found, however, that kT/C noise may be reintroduced by sampling the signal onto the capacitors 114, 118 at the bottom of the column. Typical output noise measured in CMOS APS arrays is of the order of 14–170 µV/√Hz, corresponding to noise of the order of 13–25 electrons r.m.s. This is similar to noise obtained in most commercial CCDs, through scientific CCDs have been reported similarly there is one capacitor associated with each column. This provides for the sequential readout of rows using the column. The capacitors are preferably included within the column signal conditioner 328. Column decoders 326 also allow selection of only a certain column to be read. There are two parts of each column selection: where to start reading, and where to stop reading. Preferably the operation is carried out using counters and registers. A binary up-counter within the decoder 326 is preset to the start value. A preset number of rows is used by loading the 2’s complement. The up counter then counts up until an overflow.

An alternate loading command is provided using the DEFAULT LOAD input line 332. Activation of this line forces all counters to a readout window of 128×128.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus 330. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. The counter can hence provide very large integration delays. The input clock can be any frequency up to about 10 MHz. The pixel readout rate is tied to one-fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration.
time. The integration time is therefore equal to the delay time and the readout time for a 2.5 MHz clock. The maximum delay time is $2^{12}/2.5$ MHz, or around 28 minutes. These values therefore easily allow obtaining a 30 Hz frame.

The timing and control circuit controls the phase generation to generate the sequences for accessing the rows. The sequences must occur in a specified order. However, different sequences are used for different modes of operation. The system is selectable between the photodiode mode of operation and the photogate mode of operation. The timing diagrams for the two gates are respectively shown in FIGS. 4a and 4b. FIG. 4a shows an operation to operate in the photogate mode and FIG. 4b shows operating in the photodiode mode. These different timing diagrams show that different column operations are possible. Conceptually this is done as follows. Column fixed pattern noise is based on differences in source follower thresholds between the different transistors. For example, if the base bias on a transistor is VI, the output is VI plus the threshold.

The column signal conditioning circuit contains a double-delta sampling fixed pattern noise ("FPN") suppression stage that reduces FPN to below $0.2\%$ sat with a random distribution. Since the APS is formed of a logic family that is compatible with CMOS, e.g., NMOS, the circuit can be formed of CMOS. This allows power dissipation in the timing and control digital circuitry to be minimized and to scale with clock rate.

An active pixel sensor includes both a photodetector and the readout amplifier integrated within the same substrate as the light collecting device, e.g., the photodiode. The readout amplifier is preferably within and/or associated with a pixel. A first embodiment of the present invention is a 128x128 CMOS photodiode type active pixel sensor that includes an integrated CMOS photogate system. The timing and control circuit controls the phase generation to generate the sequences for accessing the rows. The sequences must occur in a specified order. However, different sequences are used for different modes of operation. The system is selectable between the photodiode mode of operation and the photogate mode of operation. The timing diagrams for the two gates are respectively shown in FIGS. 4a and 4b. FIG. 4a shows an operation to operate in the photogate mode and FIG. 4b shows operating in the photodiode mode. These different timing diagrams show that different column operations are possible. Conceptually this is done as follows. Column fixed pattern noise is based on differences in source follower thresholds between the different transistors. For example, if the base bias on a transistor is VI, the output is VI plus the threshold.

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When the outputs are differentially amplified off-chip, the transistor VLN and two output branches to store the reset using 1.2 μm n-well CMOS. The maximum clock rate is 10 MHz during the readout cycle reducing column fixed parameters. The output has two differential analog channels. Normal read operation. This value is then stored on the other produce a 256x256 array size. This embodiment also uses a vs normal read operation. This value is then stored on the other produce a 256x256 array size. This embodiment also uses a and output source followers are common to the entire array. After a row has been selected, each pixel is reset (RESET) that for photodiode operation. The differencing mode alters used to store the signal from the previous frame and the integration delay is 1.6~10^-6 clock periods. column of pixels. The load transistors of the second set of transistors to perform the functions of readout, selection, and and the reset value is sampled (SHR) onto the holding output voltage is given by: 

\[ V_{\text{OUT}} = \frac{1}{2} (V_{\text{col}+} - V_{\text{col}-}) \]

This is the recommended time for setting the operating parameters. However, these parameters can be set at any time because of the asynchronous nature of operation. When RUN is activated, the chip begins continuous readout of frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion and then stops.

The 256x256 CMOS APS uses a system having a similar block diagram to those described previously. The pixel unit cell has a photogate (PG), a source-follower input transistor, a row selection transistor and a reset transistor. A load transistor VLN and two output branches to store the reset and signal levels are located at the bottom of each column of pixels. Each branch has a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed pattern noise (not kTC noise) from the pixel.

A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array. After a row has been selected, each pixel is reset (RESET) and the reset value is sampled (SHR) onto the holding capacitor CR. Next, the charge under each photogate in the row is transferred to the floating diffusion (FD). This is followed by sampling this level (SHS) onto holding capaci- tor CS. These signals are then placed on the output data bus by the column select circuitry. In the Photodiode mode this process, is reversed; first the charge under the photogate is read out and then the reset level is sampled. This non-corrected double sampling mode would be primarily used with a photodiode, i.e., non active pixel sensor, pixel.

In the differencing mode, the capacitors CS and CR are used to store the signal from the previous frame and the current frame. This is achieved by altering the timing in the following way: Rather than starting with a reset operation, the signal on the floating diffusion is read out to one of the sample and hold capacitors. This represents the previous pixel value. The reset is then performed followed by a normal read operation. This value is then stored on the other sample and hold capacitor. The difference between these two signals is now the frame to frame difference.

\[ V_{\text{OUT}} \text{ (signal)} \text{ and } V_{\text{R_OUT}} \text{ (reset), and digital outputs of FRAME and READ. The inputs to the chip are asynchronous digital signals. The chip includes addressing circuitry allowing readout of any area of interest within the 256x256 array. The decoder includes counters that are preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. This counter allows forming very large integration delays. The input clock can be any frequency up to about 10 MHz. The pixel readout rate is tied to one fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. A 30 Hz frame rate can be achieved without difficulty. The chip is idle when the RUN command is deactivated.
A simplified expression for the output of the reset branch of the column circuit is given by:

$$V_{col\_reset} = \alpha V_{\text{pchg}} - \beta V_{p}$$

where $\alpha$ is the gain of the pixel source-follower, $\beta$ is the gain of the column source-follower, $V_p$ is the voltage on the floating diffusion after reset, $V_{\text{pchg}}$ is the threshold voltage of the pixel source-follower n-channel transistor, and $V_{p}$ is the threshold voltage of the column source-follower p-channel transistor. Similarly, the output voltage of the signal branch of the column circuit is given by:

$$V_{col\_signal} = \alpha V_{\text{pchg}} - \beta V_{p}$$

where $V_{\text{pchg}}$ is the voltage on the floating diffusion with the signal charge present and $V_{p}$ is the threshold voltage of the column source-follower p-channel transistor. Experimentally, the peak-to-peak variation in $V_{col\_signal}$ is typically 10–20 mV. It is desirable to remove this source of column-to-column fixed pattern noise.

Sequential readout of each column is as follows. First a column is selected. After a settling time equivalent to one-half the column selection period, the DDS is performed to remove column fixed pattern noise. In this operation, a DDS switch and two column selection switches on either side are used to short the two sample and hold capacitors CS and CR. Prior to the DDS operation the reset and signal outputs ($V_{col\_reset}$ and $V_{col\_signal}$) contain their respective signal values plus a source follower voltage threshold component. The DDS switch is activated immediately after CLAMP is turned off. The result is a difference voltage coupled to the output drivers (VR\_OUT and VS\_OUT) that is free of the voltage threshold component.

This chip uses a similar pixel cell to that shown in FIG. 9. FIG. 9 shows the layout of the pixel cell. PG and RESET are routed horizontally in polysilicon while the pixel output is routed vertically in metal. Metal2 was routed within the pixel for row selection. Metal2 was also used as a light shield and covers most of the active area outside of the pixel array. The designed fill factor of the pixel is approximately 20%.

According to another feature, a logo can be formed on the acquired image by using a light blocking metal light shield. The light shield is formed to cover certain pixels in the shape of the logo to be applied. This blocks out those underlying pixels in the array, thereby forming a logo in the shape of the pixel source follower gate (e.g. threshold voltage of approx. 0.8 volts). This corresponds to a full well of approximately 75,000 electrons. This can be increased by operating at a larger supply voltage, gaining about 47,000 e- per supply volt.

Dark current was measured at less than 500 pA/cm². Conversion gain (q/V/e-) was obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1%—similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer.

The quantum efficiency of the detector was measured using a CVI ¼ monochromator and a tungsten/halogen light source, calibrated using a photodiode traceable to NIST standards.

What is claimed is:

1. A single chip camera device, comprising:
   - a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
   - said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;
   - said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,
   - said control portion also including, integrated in said subrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and further comprising double sampling charge storage elements on said substrate.

2. A camera device as in claim 1, wherein said timing circuit includes a timer for first sampling a reset level on a first of said charge storage elements, and then for second sampling a signal level on a second of said charge storage elements.

3. A single chip camera device, comprising:
   - a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
   - said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;
   - said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,
   - said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said array of photoreceptors are controlled to output an entire row of said photoreceptors substantially simultaneously; and
   - a plurality of double sampling charge storage elements integrated on said substrate; one for each of said columns.

4. A camera device as in claim 3, wherein said timing circuit includes a timer for first sampling all reset levels in a specific column on first charge storage elements, and then for second sampling all signal levels on second charge storage elements.

5. A single chip camera device, comprising:
   - a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
   - said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a pho-
to read a next consecutive row, said latch element and said counter both being integrated in said substrate.

5. A camera device as in claim 4, wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated in said substrate.

6. A camera device as in claim 5, wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated in said substrate.

7. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout,

wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout,

wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated in said substrate.

8. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout,

wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout,

wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated in said substrate.

9. A camera device as in claim 8, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop column decoder counters.

10. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, for operation with photodiodes.

11. A camera device as in claim 10, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

12. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, for operation with photodiodes.

13. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout,

wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout,

wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated in said substrate.
substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

14. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceptors;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

15. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceptors;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and
further comprising fixed pattern noise reduction circuits, on said substrate.

16. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceptors;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, further comprising a noise reduction circuit,
wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

17. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceptors;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

18. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceptors;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and second mode of operation, different that said first mode of operation, for operation with photodiodes.

19. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceptors;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing present of at least one of a start address for output or a stop address for output;
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

20. A camera device as in claim 19, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

21. A camera device as in claim 20, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.
A single chip camera device, comprising:

- A substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
- Said image acquisition portion integrated in said substrate including an array of photoreceptors;
- Said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;
- Said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

A camera device as in claim 32, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

A single chip camera device, comprising:

- A substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
- Said image acquisition portion integrated in said substrate including an array of photoreceptors;
- Said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals;
- Said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors in a first mode or in a second mode, depending on a type of photoreceptor being used.

A camera device as in claim 34, wherein said photoreceptor is one of a photodiode or a photogate, and said array is controlled into said first mode for said photogate and in said second mode for said photodiode.

A camera device as in claim 35, further comprising a correlated double sampling circuit.

A camera device as in claim 35, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

A camera device as in claim 19, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop values.

A camera device as in claim 19, wherein said photoreceptors are photodiodes.

A camera device as in claim 19, wherein said photoreceptors are photogates.

A camera device as in claim 19, wherein said photoreceptors are either photogates or photodiodes, further comprising a mode selector device which selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

A camera device as in claim 25, further comprising a correlated double sampling circuit integrated on the chip.

A camera device as in claim 19, further comprising a correlated double sampling circuit integrated on the chip.

A camera device as in claim 19, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

A single chip camera device, comprising:

- A substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
- Said image acquisition portion integrated in said substrate including an array of photoreceptors;
- Said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;
- Said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

A camera device as in claim 29, wherein said readout amplifier is preferably within and/or associated with one element of the array.

A single chip camera device, comprising:

- A substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
- Said image acquisition portion integrated in said substrate including an array of photoreceptors;
- Said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;
- Said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

A single chip camera device, comprising:

- A substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
- Said image acquisition portion integrated in said substrate including an array of photoreceptors;
- Said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said readout amplifier integrated within the same substrate as the photoreceptor.

A camera device as in claim 53, wherein said readout amplifier is preferably within and/or associated with one element of the array.

A camera device as in claim 53, wherein said photoreceptors are photodiodes.

A camera device as in claim 53 wherein said photoreceptors are photogates.

A camera device as in claim 43, further comprising a correlated double sampling circuit.

A camera device as in claim 43, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

A single chip camera device, comprising:
a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceptors;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, said control portion including common logic elements to control row and address decoders and delay counters.

A camera device as in claim 43, wherein said signal controlling device includes a column-parallel read out device, which reads out a column of said photoreceptors at substantially the same time.

A camera device as in claim 44, further comprising a noise reduction circuits, on chip.

A camera device as in claim 45, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

A camera device as in claim 45, wherein said noise reduction circuit is a fixed pattern noise reduction circuit.

A camera device as in claim 45, wherein said noise reduction circuit is a column to column fixed pattern noise reduction circuit.

A camera device as in claim 43, wherein said signal controlling device includes a column selector allowing selection of a desired row for readout, and a row selector which allows selection of a desired row for readout.

A camera device as in claim 49 wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

A camera device as in claim 49, wherein said column selector includes presettable start and stop column decoder counters, which are preset to start and stop at any desired value.

A camera device as in claim 51, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop column decoder counters.

A camera device as in claim 43, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

A camera device as in claim 53, wherein said readout amplifier is preferably within and/or associated with one element of the array.

A camera device as in claim 53, wherein said photoreceptors are photodiodes.
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceivers to output their signals,
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceivers, controlling a timing of operation of said array of photoreceivers;
said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously, further comprising a mode selector device, selecting a mode of operation of said chip.

64. A single chip camera device, comprising:
a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceivers arranged in rows and columns;
a charge storage element, associated with each said column;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceivers to output their signals,
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceivers, controlling a timing of operation of said array of photoreceivers;
said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously,
wherein said photoreceivers are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

65. A single chip camera device, comprising:
a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;
said image acquisition portion integrated in said substrate including an array of photoreceivers;
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceivers to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceivers, controlling a timing of operation of said array of photoreceivers, wherein said timing circuit allows changing an integration time for said array of photoreceivers.

66. A method of controlling a single chip camera, comprising:
integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceivers, and a signal controlling device, controlling said photoreceivers and a timing circuit integrated within the same substrate that houses the array of photoreceivers, controlling a timing of operation of said array of photoreceivers;
determining a first mode of operation for said photoreceivers being photogates, and a second mode of operation for said photoreceivers being photodiodes;
using said on-chip timing and control circuit to control sequences for accessing rows in a specified order depending on said mode of operation, using a first sequence for said first mode of operation for photogates, and a second mode of operation for said second mode for photodiodes, a timing for said first mode being different than a timing for said second mode.

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