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Shor et al.

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[54] **METHOD OF FABRICATING POROUS SILICON CARBIDE (SIC)**

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[51] **Int. Cl.**^{6} **C25F 3/12**
[52] **U.S. Cl.** **204/129.3**; 204/129.55;
204/129.65; 204/129.75
[58] **Field of Search** 204/129.55, 129.3,
204/129.75, 129.65; 205/123–124

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[57] **ABSTRACT**

Porous silicon carbide is fabricated according to techniques which result in a significant portion of nanocrystallites within the material in a sub 10 nanometer regime. There is described techniques for passivating porous silicon carbide which result in the fabrication of optoelectronic devices which exhibit brighter blue luminescence and exhibit improved qualities. Based on certain of the techniques described porous silicon carbide is used as a sacrificial layer for the patterning of silicon carbide. Porous silicon carbide is then removed from the bulk substrate by oxidation and other methods. The techniques described employ a two-step process which is used to pattern bulk silicon carbide where selected areas of the wafer are then made porous and then the porous layer is subsequently removed. The process to form porous silicon carbide exhibits dopant selectivity and a two-step etching procedure is implemented for silicon carbide multilayers.
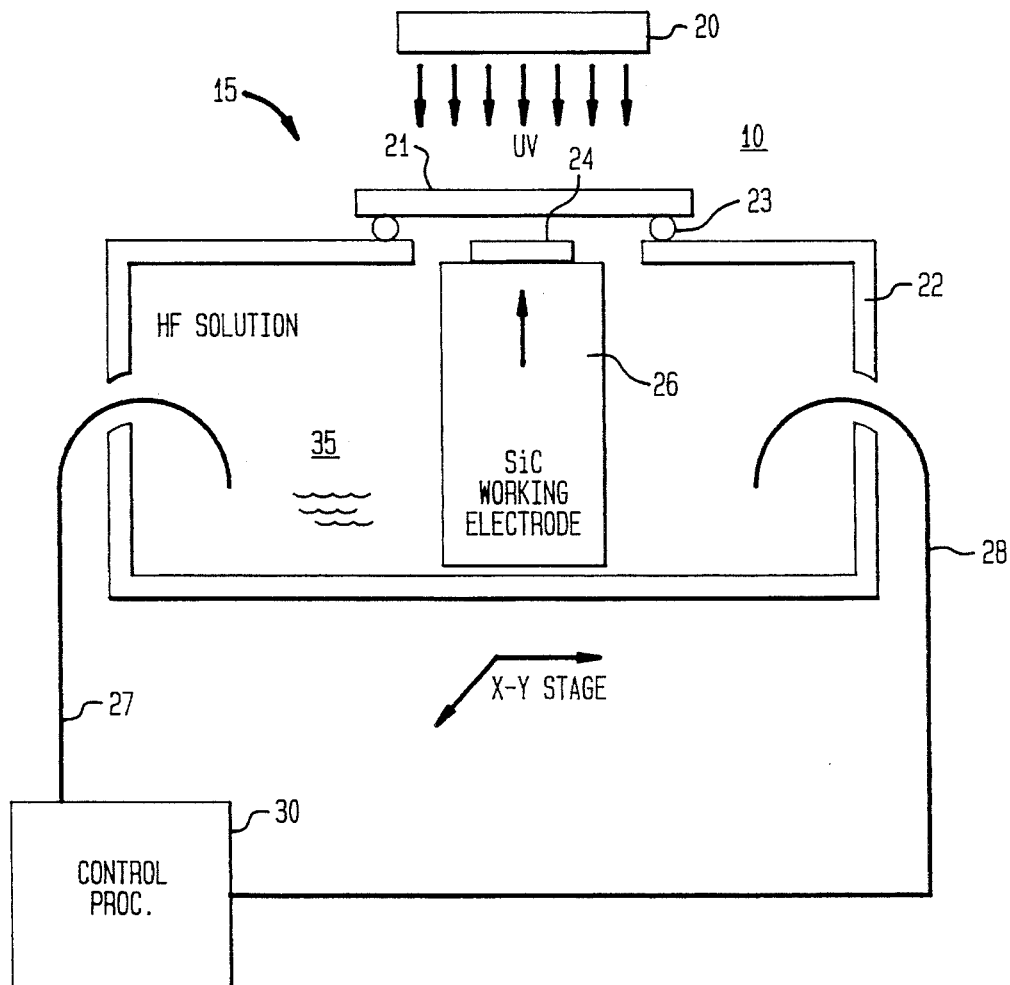
34 Claims, 3 Drawing Sheets

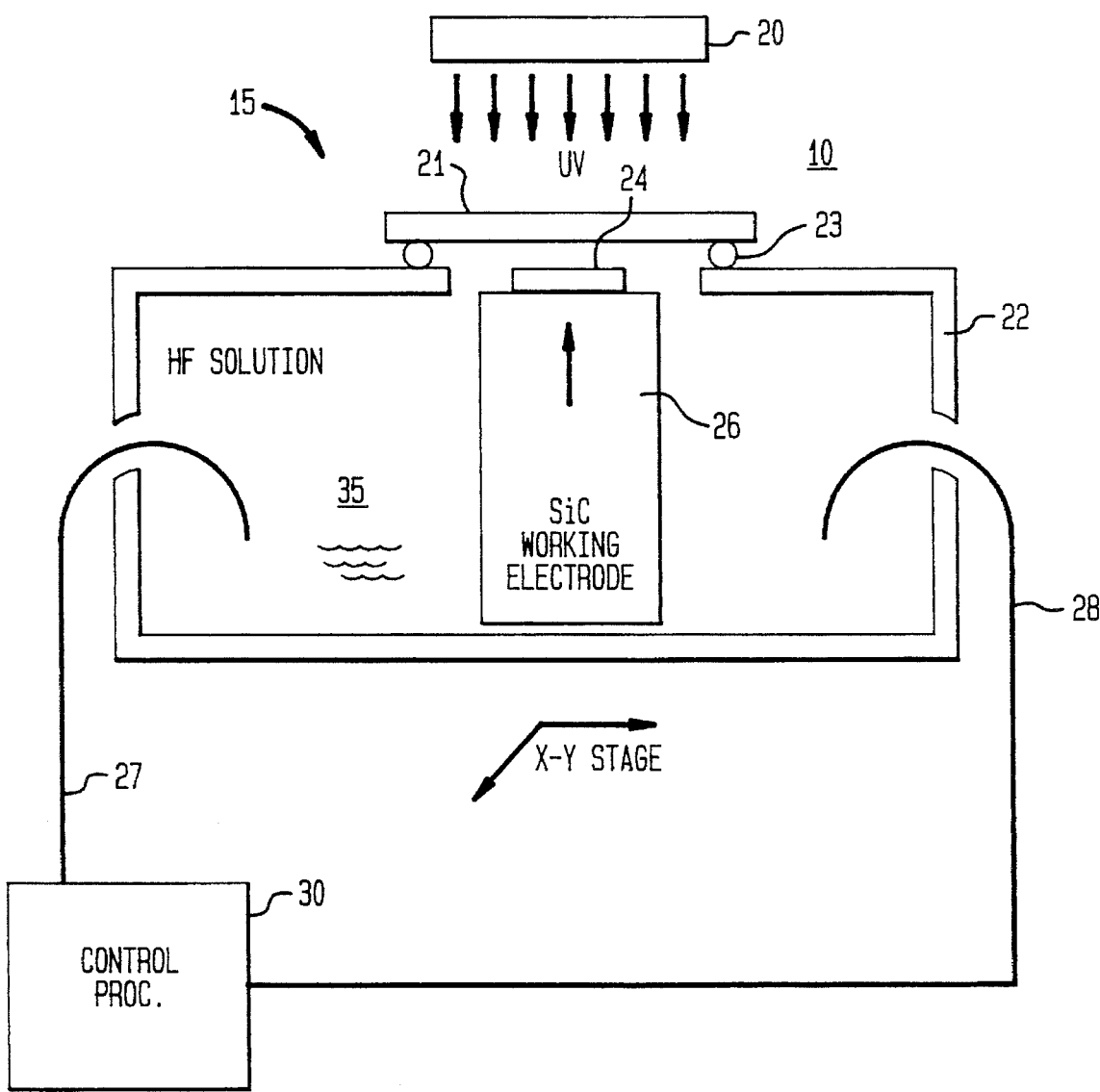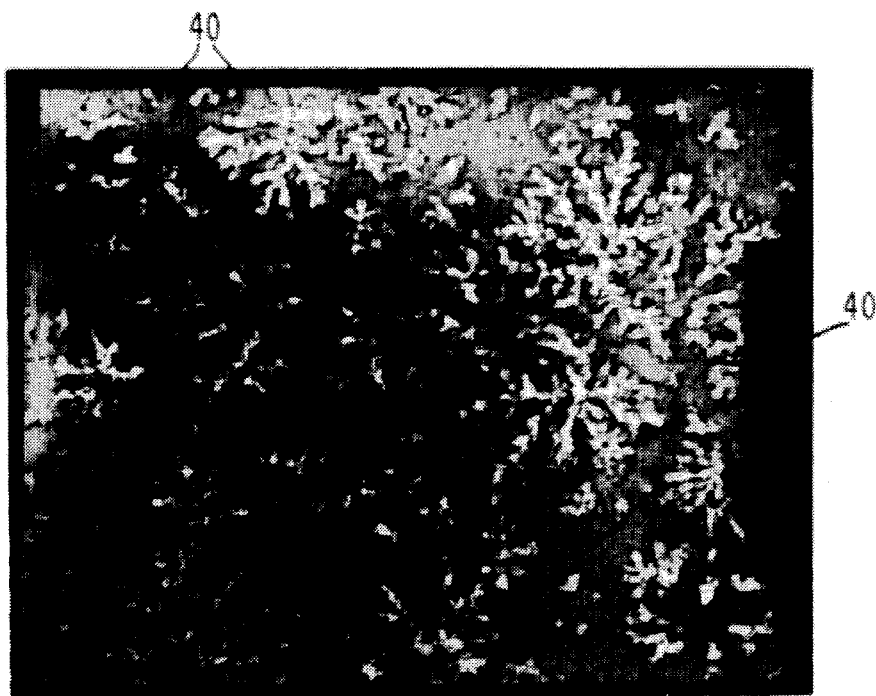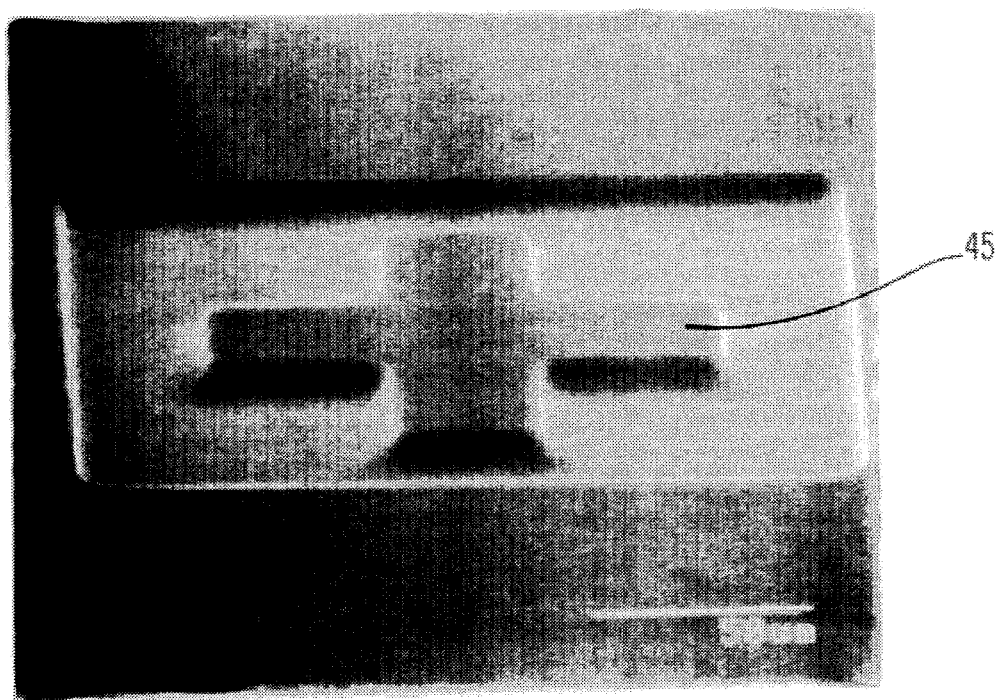## FIG. 1

FIG. 2

FIG. 3

FIG. 4

n-SiC — 52

p-SiC — 51

n-SiC — 50

FIG. 5A

MASK — 54

n-SiC — 52

p-SiC — 51

n-SiC — 50

FIG. 5B

n-SiC — 52

p-SiC — 51

n-SiC — 50

FIG. 6

n-SiC — 52

p-SiC — 51

n-SiC — 50

FIG. 7

n-SiC — 52

p-SiC — 51

— 70

SiO_2

METHOD OF FABRICATING POROUS SILICON CARBIDE (SIC)

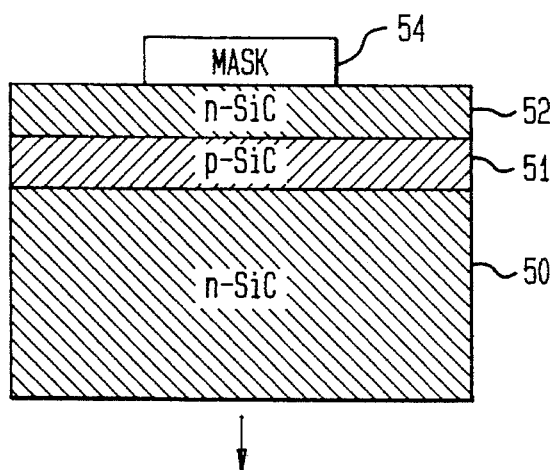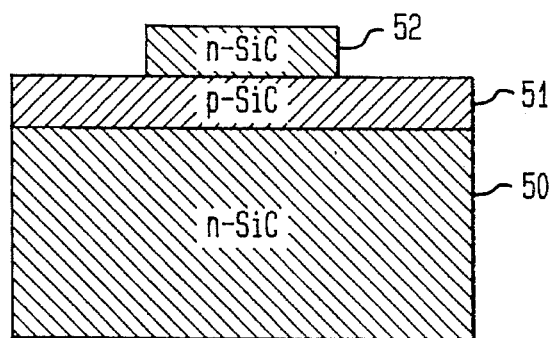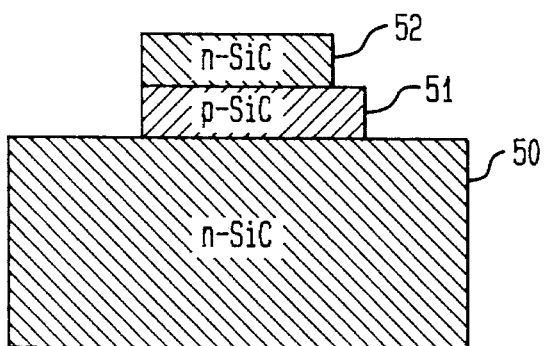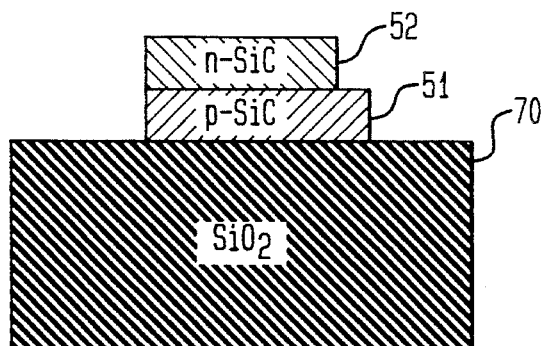This invention is the subject matter of a NASA contract, contract No. NAS-3-26599 and the U.S. Government may have rights thereunder.

This application is a continuation-in-part of application Ser. No. 07/957,519 filed Oct. 6, 1992, now U.S. Pat. No. 5,298,767.

RELATED APPLICATIONS

The assignee herein, Kulite Semiconductors Products is the record owner of U.S. Patent application entitled "HIGH TEMPERATURE TRANSDUCERS AND METHODS OF FABRICATING THE SAME EMPLOYING SILICON CARBIDE", Ser. No. 07/694,490, filed or May 2, 1991 for Anthony D. Kurtz et al, now U.S. Pat. No. 5,165,283. See also U.S. patent application 07/777,157 filed on Oct. 16, 1991 entitled "METHOD FOR ETCHING OF SILICON CARBIDE SEMICONDUCTOR USING SELECTIVE ETCHING OF DIFFERENT CONDUCTIVITY TYPES" by J. S. Shor et al., now abandoned and assigned to Kulite.

FIELD OF THE INVENTION

This invention relates to semiconductor devices in general and more particularly, to semiconductor devices which employ single crystal silicon carbide (SiC) and methods of making porous silicon carbide.

BACKGROUND OF THE INVENTION

In the recent literature, there has been much interest in electrochemical processes which cause semiconductors, such as silicon, to become porous. Various articles have appeared in Applied Physics Letters and other publications relating to such devices. See for example, an article by V. Lehman and U. Gosele, Applied Physics Letters, Volume 58, Page 856 (1991). See also an article in Volume 57 of Applied Physics Letters, by L. T. Canham, Page 1046 (1990). The prior art was cognizant of the fact that in certain instances, porous silicon exhibits unique properties which are superior to those of bulk silicon. For example, high efficiency luminescence has been observed in porous silicon above the 1.1 eV band-gap of bulk material, which suggests that optical devices can be fabricated based on the use of porous silicon. Control of the pore size on the nanometer scale can allow porous materials to be used as filters in solid state chemical sensors.

In any event, there are several theories for the formation mechanisms of pores in silicon. A good reference is the article by R. L. Smith and S. D. Collins appearing in the Journal of Applied Physics, Volume 8, R1 (1992). Studies suggest that the depletion regions of pores overlap, causing a carrier depletion in the interpore region, and thus the current is confined to the pore tips. In an article that appeared in the Journal of the Electrochemical Society, Volume 138, Page 3750 (1991) by X. G. Zhang, there was indicated that pore propagation is attributed to a higher electric field at the pore tips which causes dissolution to occur more rapidly through the intermediate step of silicon dioxide formation, while along the pore walls dissolution occurs through the slower process of direct dissolution.

Demonstrations of room temperature visible luminescence from porous silicon have generated much interest in using the material for optoelectronics. Initially, there was of course much conjecture about the mechanisms which pro-

vide the visible luminescence. However, a general consensus has been reached among most researchers that at least a portion of the luminescence is associated with quantum structures (wires or dots) in the porous silicon. These quantum structures would allow a relaxation of the momentum selection rules by confining the charges spatially, thus allowing direct band-gap transitions. Additionally, the charge confinement would increase the effective band-gap, thereby pushing it into the visible region. The quantum confinement theory has been supported by considerable theoretical and experimental evidence.

Researchers, such as C. Tsai, K. H. Li and D. S. Kinosky, et al., in an article in Applied Physics Letters, Volume 60, Page 1770 (1992) have shown that surface chemistry, specifically hydrogen termination, play an important role in the luminescence. This suggests that luminescence in porous silicon may have similar mechanisms as a-Si, which exhibits band gap widening into the visible region when hydride species are formed on the surface. A portion of the visible luminescence of porous Si may be associated with the SiH. It has yet to be conclusively determined whether the hydrogen termination serves only to passivate the surface or whether there is a contribution to the luminescence by amorphous Si hydride. Nevertheless, it is very clear that microcrystals of<5 nm dimension will exhibit band-gap widening and above band-gap luminescence.

There has been interest in SiC as a semiconductor material since the 1950's. Its wide band-gap, high thermal conductivity, high breakdown electric field and high melting point make SiC an excellent material for high temperature and high power applications. SiC also exhibits interesting optical properties, such as deep UV absorption, visible transparency and blue photo- and electro-luminescence. However, good quality crystals were unavailable, causing the early research efforts to stagnate. Recent developments in single crystal epilayer and boule growth have generated new interest in SiC. This has resulted in the development of SiC blue LED's, UV photodiodes and high temperature electronic components. However, due to its indirect band-gap, the efficiency of SiC optoelectronic devices is limited. Thus, research is underway to develop other wide band-gap semiconductors, such as SiC_xAlN_y and III–V nitrides for optical applications. However, the crystal growth technology for these materials is still very underdeveloped. Porous SiC could be very useful, since it has superior optical properties than SiC, and may benefit from the relatively mature growth and processing technology that SiC has to offer. Devices which would benefit from these superior optical qualities include LED's, Lasers, and Photodetectors. Furthermore, SiC is very difficult to etch because of its chemical inertness. Therefore, porous SiC could also be used to pattern this material for electronic device fabrication.

There have been several reports on the electrochemical dissolution of SiC. Recently, Shor, et al. used laser assisted electrochemical etching to rapidly etch high relief structures in SiC. See an article by J. S. Shor et al., in Journal of Electrochemical Society, Volume 139, Page 143, May 22, 1992. M. M. Carrabba et al., in an article in Electrochemical Society Extended Abstracts, Volume 89-2, Page 727 (1989), reported etching diffraction gratings in n-type β- and α-SiC at anodic potentials with a uniform light source. The fundamental electrochemical studies indicate that the presence of HF in aqueous solutions is important to etch SiC electrochemically. Glerria and Mereming in Volume 65 of the Journal of Electroanl Chem., on Page 163 (1975) reported that α-SiC dissolves in aqueo US H_2SO_4 solutions at anodic potentials through the formation of a passivating layer,

which was suggested to be SiO_2, since it dissolved in HF.

The present invention relates to the formation of porous SiC, a new material. It is indicated that porous SiC material itself, as well as a process to fabricate the porous SiC is provided. Porous SiC can be employed for UV and blue light sources such as LED's and diode-lasers. Porous SiC can be utilized as a filter in chemical processes and can be used to provide heterojunction devices using the porous SiC/bulk SiC interface. As will be described, the methods employ a selective etching of bulk SiC by forming a porous layer on the surface, oxidizing it and stripping it in hydrofluoric (HF) acid. One can also provide dielectric isolation of SiC devices on a wafer by oxidizing a buried porous SiC layer.

SUMMARY OF THE INVENTION

This invention relates to porous SiC, its fabrication, and utilization in semiconductor devices. Three applications of porous SiC are disclosed in this light.

1) Porous SiC can be fabricated in a manner which will result in a significant portion of nanocrystallites within the material in the sub 10-nm regime. This will result in bandgap widening and a much more efficient luminescence from the material. As such, porous SiC has superior properties than bulk SiC for semiconductor light sources, such as LEDs and Lasers. Thee use of porous SiC in these devices enable them to operate at UV wavelengths. When passivated, porous SiC exhibits a much brighter blue luminescence (by a factor of 50) than bulk material, enabling more efficient blue light sources. The enhanced properties of porous SiC are also useful for photodetectors.

2) Porous SiC also is useful as a sacrificial layer for the patterning of SiC. SiC is a very inert material, and as such, is difficult to etch by conventional methods. Porous SiC, however, can be removed from its bulk substrate by oxidation and other methods. Therefore, a two step process can be used to pattern bulk SiC, whereby selected areas of the wafer are made porous, and then the porous layer is subsequently removed. The process to form porous SiC exhibits dopant selectivity (i.e. one conductivity type becomes porous while another is unaffected). Thus, using the two step etching procedure, dopant selective etch-stops may be implemented for SiC multilayers.

3) Porous SiC can be oxidized at a much faster rate (several orders of magnitude) than bulk SiC. This property can be utilized to fabricate dielectrically isolated SiC layers and/or selectively introduced thick sections of SiO_2 into a SiC wafer. SiC-on-insulator is fabricated by oxidizing a buried porous layer which is underneath a non-porous SiC layer. The porous layer is oxidized completely, and the remaining structure is dielectrically isolated SiC. This aspect of porous SiC is very useful in the fabrication of high temperatures/power/frequency electronic components.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a diagram depicting a process for forming porous SiC utilizing an electrochemical cell.

FIG. 2 is a top plan view transmission electron micrograph of a porous SiC layer formed by the process described in FIG. 1.

FIG. 3 is a top plan view electron micrograph of a pattern etched into a layer of SiC.

FIGS. 4–7 depict various steps in employing SiC to form a dielectrically isolated SiC device (e.g. the diode) according to this invention.

DETAILED DESCRIPTION OF THE INVENTION

This descriptio is divide into four parts for clarity: 1) the fabrication method of porous SiC, 2) the use of porous SiC for optoelectronic devices, 3) the use of porous SiC for patterning or shaping SiC and 4) the use of porous SiC to achieve dielectrically isolated SiC layers and devices.

Fabrication of Porous SiC

Referring to FIG. 1, there is shown apparatus which can be used to form porous SiC. The formation of porous SiC occurs under electrochemical anodization. There are wide variety of fabrication conditions that result in pore formation, and the microstructure, pore size, pore spacing and morphology of the material is dependent on the process parameters. Referring to FIG. 1, there is shown an electrochemical cell 22. The cell 22 may be fabricated from an electrolyte-resistant, dielectric material, such as Teflon plastic material (trademark of dupont Company). The cell 22 has a lead 27 which is a platinum wire counter-electrode and a lead 28 which is a saturated calomel reference electrode. Both leads are directed to a control processor apparatus 30 to control the entire process as will be explained. The cell 22 contains a electrolyte 35. The electrolyte 35 used in cell 22 may be a hydrofluoric acid (HF) solution which is relatively dilute, as for example a 2.5% HF or any other acidic solution containing F^- or Br^- ions otherwise capable of dissolving SiO_2. A semiconductor wafer such as n-type 6H-SiC samples are contacted electrically with nickel ohmic contacts and are placed in a carrier 24 which carrier is as indicated placed within the electrochemical cell 22. The semiconductor sample is encapsulated in black wax so that only the bare semiconductor surfaces are exposed as the ohmic contacts and the leads are protected. Thus as seen in FIG. 1, the semiconductor wafers are positioned and mounted in the carrier module 24 which is positioned on the top surface of a pedestal 26 which is located in the cell 22. The semiconductor acts as the working electrode in this arrangement. Care must be taken, that all surfaces not to be etched, which may corrode in the electrolyte, must be covered with the black wax or other encapsulant. The semiconductor SiC is preferably biased with respect to the saturated calomel reference electrode 28 at a suitable potential for the n-type layer to photo corrode. The bias voltage is provided to the control processor 30. In this embodiment an anodic potential is applied to the semiconductor. In the case of n-type SiC, ultraviolet or UV light from source 20 illuminates the sample surface in order for dissolution to occur. The light is directed through a sapphire window 21 where it impinges upon the surface of the semiconductor supported by the carrier 24. In p-SiC, dissolution can occur in the dark. The depth of the porous layer and its structure (e.g. pore size and interpore spacing) is determined by the anodization time, the UV light intensity, the applied potential, the pH and the doping levels of the crystals. As such the porosity, interpore spacings, and morphology can be controlled by varying these parameters properly. As indicated, the semiconductor is subject to electrochemical etching in the electrolyte 35, preferably while being exposed to UV light. UV light is provided from the UV light source 20 through the light transmissive cover 21 sealed to the top of the cell 22 by means of seals 23. The UV exposure generates

holes in the semiconductor in the area which is exposed by the ultraviolet light. In any event, for a more detailed description of anodic dissolution of SiC, see the above-noted application which was filed on Oct. 16, 1991 entitled METHODS FOR ETCHING OF SILICON CARBIDE SEMICONDUCTOR USING SELECTIVE ETCHING OF DIFFERENT CONDUCTIVITY TYPES, Ser. No. 07/777, 157. Again refer, ring to FIG. 1, it is indicated that pore formation will occur under the following process conditions. For n-type 6H-SiC the anode potential is equal to 0–2 V_{sce} (sce=saturated calomel electrode) which is applied by the control processor 30. The UV intensity from light sourede 20 is maintained between 50–500 mW/cm². The UV wavelength is selected in the range of 250–400 nanometers. The carrier concentration of the silicon carbide wafer is $3\times10^{18}/$ cm³. The concentration of the HF solution 35 is equal to 2.5% in water. In order to obtain porous p-type silicon for p-type 6H-SiC, the anodic potential is equal to 1.8 to 2.8 V_{sce} the carrier concentration is equal to $2-3\times10^{18}/cm^3$ and the HF concentration is equal to 2.5% in water. The conditions for porous film formation are not limited to those delineated above, but pore formation has been directly observed under the above conditions. Under some of these conditions, pores spacings which are below 10 nm will result.

It should be noted that the potential of pore formation in n-SiC is lower than that of p-SiC. Therefore a porous layer can be formed on a pn junction, such that the n-SiC side of the junction becomes porous and the p-SiC is unaffected. This can also be accomplished in reverse by anodizing the p-SiC between 1.8–2.8V_{sce} in the absence of UV, such that the p-SiC becomes porous and the n-SiC is unaffected.

Referring to FIG. 2, there is shown a top plan view transmission electron micrograph of a porous SiC layer formed in a n-type 6H-SiC at V=1.4 V_{sce}, I=300 mW/cm² of UV (250–400 nm), and $N_{d=}3\times10^{18}$ cm⁻³ in 2.5% HF. The bright areas 40 are voids or pores in the SiC. The pores may range in size between 10 and 100 nm. The spacing between these pores range between about 5 nm to 100 nm. This indicates that both quantum crystalline structures (less than 10 nm) and enlarged crystalline structures can be fabricated. The pore size, shapes and spacings are very much a function of the processing conditions. Electron diffraction of the porous areas prove that the material is single crystal 6H-SiC. Thus, as one can ascertain from the micrograph of FIG. 2, one can produce porous SiC as disclosed therein and according to the above-noted process. In any event, porous SiC has the potential to be utilized as a UV generation medium in light emitting diodes (LED's) and laser diodes. Such devices would be extremely useful in optical storage, optoelectronic communication systems, laser bumping systems, sensor/ detectors and materials processing. These devices may emit light in the UV wavelength.

Optoelectronics from Porous SiC

Semiconductor optoelectronics has, by and large, been limited to III–V compounds due to their direct band-gap. For SiC, a porous structure could increase its already wide band-gap (3 eV for 6H-SiC) and allow direct gap transitions, facilitating which efficient UV/near UV luminescence. These luminescent properties are useful in LED or a Laser, thus greatly enhancing current optoelectronic capabilities by including deeper wavelengths in semiconductor light sources. These direct bandgap transitions also enable more efficient blue LEDs to be fabricated when porous SiC is used rather than bulk SiC.

SiC has unique optical properties, such as blue electroluminescence, which have facilitated the development of blue LED's. However, due to the indirect band-gap of SiC (3 eV for 6H-SiC), the LED's are inefficient. By electrochemically fabricating a microcrystalline porous structure in SiC, it is possible to increase both the band-gap and quantum efficiency, resulting in UV, or deep Blue luminescence. This luminescence will enable the development of semiconductor UV and blue light sources and UV/blue optoelectronic devices from porous SiC.

As noted earlier, porous microcrystalline SiC structures can be electrochemically fabricated with pore spacings of "quantum" dimensions (less than 10 nm) in accordance with the present invention. Such structures exhibit luminescence above the band gap. Moreover, the luminescence in the blue range of the spectrum (approximately 2.8 eV) is greatly enhanced by passivating such structures with a passivating agent such as oxygen or hydrogen. Passivation enables the microcrystalline structures to satisfy the conditions for quantum confinement by preventing surface recombination at dangling bond. Passivating agents that may be employed for this purpose include atomic hydrogen, deposited by a plasma or by a HF dip, oxygen, formed by thermal oxidation or anodically, or any other passivating agent which will pin the dangling bond sites. The enhanced luminescence can be utilized in the fabrication of a variety of optoelectronic devices such as blue semiconductor light sources (e.g., light emitting diodes) and semiconductor lasers. It should also be noted that there are a wide variety of conditions which will result in this superior form of porous silicon carbide. Essentially, any thin insulating layer deposited or grown on the porous surface, could provide the desired passivation layer. Thus, the resulting thin passivation layer may be comprised of SiN, SiH, SiO_n, or the like.

Laser diodes and LED's have been used extensively in a wide diversity of applications ranging from displays to optical communication systems. Porous SiC UV sources will extend the wavelength capability of this device below the blue wavelengths currently available from single crystal SiC and ZnSe. Such light sources could be useful in a variety of applications. For example, UV sources would enable a smaller spatial volume in optical recording, thus enhancing both spatial resolution and information packing densities in optical storage. UV LED's and lasers are also useful for optical communications and as higher energy pump sources for LASER's and possibly phosphors.

Currently, efforts are underway to develop direct band gap materials with large band gaps, such as GaN, AlN and ZnSe, which have band gaps between 3.2–6.4 eV for UV and near UV optoelectronics. A microcrystalline SiC structure would be useful in applications (e.g. blue and UV optoelectronics) for which the other wide gap materials are being investigated. SiC has much more sophisticated device technology associated with it than these other materials and thus offers considerable advantages over these other materials.

Porous SiC is also useful for photodetectors. Porous SiC has a very low reflectivity compared to bulk SIC, which allow more of the incident radiation to be collected. The wider bandgap of the porous SiC enables the easy fabrication of heterojunction photodetectors, which are know to exhibit superior properties than homojunction detectors.

Patterning of SiC using Porous SiC

SiC is a very difficult material to pattern into device structures because of its chemical inertness. By selectively fabricating a porous layer into a silicon wafer, oxidizing the layer and removing the oxide in HF, deep etched features can be patterned.

Referring to FIG. 3, there is shown a SEM micrograph of a pattern etched into n-type 6H-SiC, by the intermediate step of forming a porous layer. A metal mask was deposited on the SiC provided as described above, and patterned using standard photolithographic processes. The etching conditions to form porous SiC were I=500 mW/cm^2 of UV (250–400 nm), V=1.5 V$_{sce}$, 2.5% HF for 30 minutes. The mask was subsequently removed and the SiC was thermally oxidized in a steam ambient for 4 hrs. at 1150° C. to fully oxidize the porous layer, and form a thin oxide (<1000 Å) on the parts of the surface previously covered by the metal. The oxide was etched for 2 min in buffer HF, resulting in the pattern **45** formed on the SiC. These conditions are an example of how SiC can be etched by the two step process of 1) forming a porous layer on the surface and 2) removing the porous layer. Furthermore, by employing the selective anodization conditions discussed earlier, a layer of one conductivity type can be etched, while a second layer of a different conductivity type acts as an etch-stop.

Dielectric Isolation Using Porous SiC

The following steps exhibit how porous SiC can be used to dielectrically isolate SiC devices. In this case the device described is a pn-junction diode, but the principles are equally applicable to other devices as well. Referring to FIG. 4, one proceeds with an n-SiC wafer **50**, two epilayers, one p-type **51** and one n-type **52** are grown by chemical vapor deposition. In FIG. 5a, a mask **54** in placed on the top n-type epilayer **52** and defined using photolithography. In FIG. 5b, the n-SiC layer **52** is etched by the previously mentioned methods. In FIG. 6, the p-SiC layer **51** is patterned in a similar manner. In FIG. 7, the bottom n-SiC **52** becomes porous and p-SiC **51** remains inert. The top n-SiC epilayer does not come into contact with the solution. The porous layer is then oxidized, resulting in a dielectrically isolated pn-junction. The pn-junction is comprised of single crystal SiC layers (which are not porous).

As one can ascertain, the techniques described above can be implemented by many different procedures as briefly alluded to. Reference is again made to U.S. patent application 07/694,490 entitled HIGH TEMPERATURE TRANSDUCER AND METHODS OF FABRICATING THE SAME EMPLOYING SILICON CARBIDE, filed on May 2, 1992 and assigned to assignee herein. In that application, a pertinent reference was cited and entitled GROWTH AND CHARACTERIZATION OF CUBIC SiC SINGLE CRYSTAL FILMS ON SILICON by J. Anthony Powell et al., published in the Journal of Electrochemical Society, Solid States Science and Technology, June 1987, Volume 134, No. 6, Pages 1558–1565. This article contains an extensive bibliography and approaches using SiC in various applications and in the processing of SiC. As is well known, one can grow silicon carbide of either n or p-type by means of chemical vapor deposition techniques (CVD). Such techniques are well known for growing silicon carbide on silicon wafers, see for example the above-noted article. The doped gas employs tri-methyl aluminum. In a similar manner, the growth of silicon carbide layers on n-type silicon carbide is also known and can be accomplished by conventional CVD techniques. There are various articles in the prior art which teach the growth of films of silicon carbides. See for example an article by J. A. Powell, L. G. Matus and M. A. Kuczmarsld in the Journal of the Electrochemical Society, Volume 134, Page 1558 (1987). See also an article by L. G. Matus, J. A. Powell, C. S. Salupo, Applied Physics Letters, Volume 59, Page 1770 (1991). Such articles, as well as the

above-noted applications, teach the growth of layers of silicon carbide utilizing either p or n-type silicon carbide on silicon wafers or wafers of silicon carbide. In any event, such techniques employ standard masking techniques as for example, standard photolithographic processes which are also well known in the art.

Thus there is described at least one useful device utilizing porous SiC, but many other devices are in fact contemplated. There is described the use of porous SiC to pattern SiC. There is described a method of forming SiC-on-insulator structures using porous SiC. There is described a method and technique for the formation of porous SiC, a material that can have wide spread utility. The material as well as the process, will enable the formation of various devices with great potential use.

What is claimed is:

1. A method of fabricating porous SiC comprising the steps of:

placing a wafer of silicon carbide in a electrochemical cell;

electrochemically etching said wafer for a period sufficient to form pores on a exposed surface of said wafer; and

illuminating said exposed surface of said wafer with ultraviolet (UV) light.

2. The method according to claim **1**, wherein said wafer is n-type SiC.

3. The method according to claim **2**, wherein said n-type SiC has a carrier concentration of about 3×10^{18}/cm^3 with said SiC being 6H-SiC.

4. The method according to claim **1** wherein said wafer is p-type SiC.

5. The method according to claim **4**, wherein said p-type SiC has a carrier concentration of between 2 to 3×10^{18}/cm^3.

6. The method according to claim **5**, wherein said step of electrochemically etching includes applying an anodic potential of from 2 to 3 V at a saturated reference electrode for 1 to 60 minutes.

7. The method according to claim **1**, wherein the intensity of said UV light is between 50–500 mW/cm^3 and the wavelength is between 250–400 nanometers.

8. The method according to claim **1**, wherein said step of electrochemically etching includes applying an anodic potential to said wafer in said cell.

9. The method according to claim **8**, wherein said potential is between 0–3 volts.

10. The method according to claim **1**, wherein said etching employs hydrofluoric acid (HF).

11. The method according to claim **10**, wherein said HF is 2.5% in water.

12. The method according to claim **1**, further including oxidizing porous portions of said wafer after said etching step to convert said porous silicon carbide into silicon dioxide.

13. The method according to claim **12**, further including densifying the regions of silicon dioxide.

14. The method according to claim **13**, wherein said densifying step comprises annealing said regions of silicon dioxide.

15. The method according to claim **1**, wherein pores of submicron dimensions are formed during said etching step.

16. The method according to claim **1**, wherein a monocrystalline layer of porous silicon carbide is formed during said etching step.

17. The method according to claim **1**, wherein said pores spacings are less than 10 nm.

18. The method according to claim **1**, further including the

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step of passivating a surface of said layer.

19. The method according to claim **18**, wherein said passivating step comprises forming a thin insulating layer on the surface of the said porous layer.

20. A process for etching silicon carbide comprising:

providing a substrate or epilayer of silicon carbide, said silicon carbide being of a first conductivity type;

selectively anodizing said substrate electrochemically to form porous regions of silicon carbide thereon; and

removing said porous regions from substrate.

21. The process according to claim **20**, further including the step of oxidizing said porous regions prior to said removing step.

22. An etch stop process comprising the steps of:

providing a SiC layer of a first conductivity type, on top of a layer of SiC of a second conductivity type; and

anodizing the first layer so that the second layer remains inert, to form porous SiC in place of the first layer; and

removing the porous layer.

23. The process according to claim **22**, wherein said porous regions are defined photolithographically prior to said anodizing step.

24. The process to claim **2** for providing a heterojunction of porous SiC and non-porous SiC.

25. A method of fabricating porous SiC comprising the steps of:

placing a wafer of silicon carbide in a electrochemical cell;

electrochemically etching said wafer for a period sufficient to form pores on a exposed surface of said wafer

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wherein said pores define spacings of less than 1 micron.

26. The method according to claim **25** further including the step of:

illuminating said exposed surface of said wafer with ultraviolet (UV) light.

27. The method according to claim **25**, wherein said step of electrochemically etching includes applying an anodic potential to said wafer in said cell.

28. The method according to claim **27**, wherein said potential is between 0–3 volts.

29. The method according to claim **25**, further including oxidizing porous portions of said wafer after said etching step to convert said porous silicon carbide into silicon dioxide.

30. The method according to claim **29**, further including densifying the regions of silicon dioxide.

31. The method according to claim **30**, wherein said densifying step comprises annealing said regions of silicon dioxide.

32. The method according to claim **25**, wherein a monocrystalline layer of porous silicon carbid, is formed during said etching step.

33. The method according to claim **25**, further including the step of passivating a surface of said layer.

34. The method according to claim **33**, wherein said passivating step comprises forming a thin insulating layer on the surface of the said porous layer.

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