REAL-TIME SOFTWARE RECEIVER

Inventors: Brent M. Ledvina, Ithaca, NY (US); Mark L. Psilak, Brooktondale, NY (US); Steven P. Powell, Ithaca, NY (US); Paul M. Kintner, Jr., Ithaca, NY (US)

Assignee: Cornell Research Foundation, Inc., Ithaca, NY (US)

Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

Appl. No.: 10/753,927
Filed: Jan. 8, 2004

Prior Publication Data

Related U.S. Application Data
Provisional application No. 60/439,391, filed on Jan. 10, 2003.

Int. Cl.
H03K 9/00 (2006.01)

U.S. Cl. 375/316; 375/147; 375/343; 455/130

Field of Classification Search 375/316, 375/147, 343; 455/130; 324/357.12

References Cited
See application file for complete search history.

U.S. PATENT DOCUMENTS
FOREIGN PATENT DOCUMENTS

OTHER PUBLICATIONS

ABSTRACT
A real-time software receiver that executes on a general purpose processor. The software receiver includes data acquisition and correlator modules that perform, in place of hardware correlation, baseband mixing and PRN code correlation using bit-wise parallelism.

27 Claims, 14 Drawing Sheets
OTHER PUBLICATIONS


Title: Real-Time Software Receiver. Applicants: Brent M. Ledvina et al.


* cited by examiner
DATA BUFFERING AND ACQUISITION SYSTEM

FIG. 2A

SOFTWARE CORRELATOR

FIG. 2B
<table>
<thead>
<tr>
<th>Quantity</th>
<th>Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Times</td>
<td>$t_0$, $t_1$, $t_2$, $t_3$, $t_4$, $t_5$, $t_6$, $t_7$</td>
</tr>
<tr>
<td>RF Signal</td>
<td>1 1 -1 -1 -1 1 1 1</td>
</tr>
<tr>
<td>Word Representation of Signal</td>
<td>1 1 0 0 0 1 1 1</td>
</tr>
<tr>
<td>PRN Code replica</td>
<td>1 -1 -1 1 1 1 1</td>
</tr>
<tr>
<td>Word Representation of PRN Code replica</td>
<td>1 0 0 0 1 1 1 1</td>
</tr>
<tr>
<td>Product of Signal and PRN Code replica</td>
<td>1 -1 1 1 -1 1 1 1</td>
</tr>
<tr>
<td>Word Representation of Product</td>
<td>0 1 0 0 1 0 0 0</td>
</tr>
</tbody>
</table>

**FIG. 2C**
FIG. 2D
FIG. 3B
FIG. 3C PRIOR ART
REPRESENT SAMPLE SIGNAL DATA 21 FROM AT LEAST ONE CHANNEL AS SIGNAL SIGN 21A AND, IF PRESENT, SIGNAL MAGNITUDE 21B AND SELECT CARRIER REPLICA 25 BASED ON ITS FREQUENCY'S PROXIMITY TO A DESIRED CARRIER REPLICA FREQUENCY, REPRESENT CARRIER REPLICA 25 AS CARRIER REPLICA SIGN 25A AND CARRIER REPLICA MAGNITUDE 25B.

MIX SIGNAL DATA 21 TO BASEBAND \( \rightarrow \) COMPUTE BASEBAND MIXED SIGN 23A = XOR (CARRIER REPLICA SIGN 25A, SIGNAL SIGN 21A); COMPUTE BASEBAND MIXED MAGNITUDE 23B/C = \( f \) (CARRIER REPLICA MAGNITUDE 25B, SIGNAL MAGNITUDE 21B).

SELECT PRN CODE FROM PRN CODE TABLE 28 OR COMPUTE IT USING REAL-TIME OVER-SAMPLED PRN CODE GENERATOR 30A; REPRESENT PROMPT PRN CODE SIGN 29 AS PROMPT SIGN 29A; REPRESENT EARLY-MINUS-LATE PRN CODE 35 AS EARLY-MINUS-LATE PRN SIGN 35A AND EARLY-MINUS-LATE PRN ZERO MASK 35B.

DE-SPREAD BY MIXING IN-PHASE AND QUADRATURE BASEBAND MIXED SIGNALS 23 WITH PROMPT PRN CODE 29 AND EARLY-MINUS-LATE PRN CODE 35: COMPUTE FULLY MIXED PROMPT INTEGRAND SIGN 31A = XOR (BASEBAND MIXED SIGN 23A, PROMPT PRN CODE SIGN 29A); COMPUTE FULLY MIXED PROMPT INTEGRAND MAGNITUDE 31B/C = \( f \) (BASEBAND MIXED MAGNITUDE 23B/C); COMPUTE FULLY MIXED EARLY-MINUS-LATE INTEGRAND SIGN 33A = XOR (BASEBAND MIXED SIGN 23A, EARLY-MINUS-LATE PRN CODE SIGN 35A); COMPUTE FULLY MIXED EARLY-MINUS-LATE INTEGRAND HIGH/LOW MAGNITUDE 33B/C = \( f \) (BASEBAND MIXED MAGNITUDE 23B/C); COMPUTE FULLY MIXED EARLY-MINUS-LATE ZERO MASK 33D = \( f \) (EARLY-MINUS-LATE PRN CODE ZERO MASK 35B); RESULT IS FULLY MIXED IN-PHASE AND QUADRATURE PROMPT INTEGRANDS 31 AND FULLY MIXED EARLY-MINUS-LATE INTEGRANDS 33.

COMPUTE IN-PHASE AND QUADRATURE PROMPT INTEGRAND VALUE WORDS 27 AND EARLY-MINUS-LATE INTEGRAND VALUE WORDS 37: PROMPT INTEGRAND VALUE WORDS 27 = \( f \) (FULLY MIXED PROMPT INTEGRAND SIGN 31A, FULLY MIXED PROMPT INTEGRAND MAGNITUDE 31B/C); COMPUTE EARLY-MINUS-LATE INTEGRAND VALUE WORDS 37 = \( f \) (FULLY MIXED EARLY-MINUS-LATE INTEGRAND SIGN 33A, FULLY MIXED EARLY-MINUS-LATE INTEGRAND MAGNITUDE 33B/C, FULLY MIXED EARLY-MINUS-LATE INTEGRAND ZERO MASK 33D).

FIG. 4A
SUM OVER EACH INTEGRAND VALUE WORD 27/37 THE NUMBER OF ONE BITS (OR ZERO BITS) BY USING THE ONE BITS SUMMATION TABLE 38 OR A PROCESSOR COMMAND: COMPUTE PROMPT INTEGRAND VALUE-WORD ONE-BITS COUNTS = f (PROMPT INTEGRAND VALUE WORD 27); COMPUTE EARLY-MINUS-LATE INTEGRAND VALUE-WORD ONE-BITS COUNTS = f (EARLY-MINUS-LATE INTEGRAND VALUE WORD 37).

SUM OVER ACCUMULATION INTERVAL THE NUMBER OF ONE BITS (OR ZERO BITS) IN EACH PROMPT INTEGRAND VALUE WORD 27 AND EARLY-MINUS-LATE INTEGRAND VALUE WORD 37 TO PRODUCE ACCUMULATIONS 41 AND 49: COMPUTE PROMPT ACCUMULATIONS 41 = Σ (PROMPT VALUE-WORD ONE-BITS COUNTS); SUM IS OVER ALL WORDS IN ACCUMULATION INTERVAL; COMPUTE EARLY-MINUS-LATE ACCUMULATIONS 49 = Σ (EARLY-MINUS-LATE INTEGRAND VALUE WORD ONE-BITS COUNTS); SUM IS OVER ALL WORDS IN ACCUMULATION INTERVAL.

MULTIPLY VALUE WORD ONES ACCUMULATIONS 41 AND 49 BY CORRESPONDING VALUES 41A AND SUM OVER ALL VALUE WORDS FOR IN-PHASE AND QUADRATURE PROMPT WORDS AND EARLY-MINUS-LATE WORDS: SUMMED PROMPT ACCUMULATION 45 = Σ (VALUE 41A* [PROMPT ACCUMULATION 41]); SUM IS OVER ALL VALUES; SUMMED EARLY-MINUS-LATE ACCUMULATION 47 = Σ (VALUE 41A* [EARLY-MINUS-LATE ACCUMULATION 49]); SUM IS OVER ALL VALUES, RESULTS ARE IN-PHASE AND QUADRATURE SUMMED PROMPT ACCUMULATION 45 AND SUMMED EARLY-MINUS-LATE ACCUMULATION 47.

ROTATE THE IN-PHASE AND QUADRATURE PROMPT ACCUMULATIONS 45 AND EARLY-MINUS-LATE ACCUMULATIONS 47.

YES OR NO CHANNELS?

RESET FOR ANOTHER ACCUMULATION INTERVAL.

TIME PERIOD ELAPSED?

SLEEP

FIG. 4B
<table>
<thead>
<tr>
<th>Table Element</th>
<th>Code Time Offset</th>
<th>Bit Sequence of ( L ) Code Chips (first is left-most, last is right-most)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( x(1) )</td>
<td>( \Delta t_{0;\min} )</td>
<td>0 0 ... 0 0 0 0 0</td>
</tr>
<tr>
<td>( x(2) )</td>
<td>( \Delta t_{0;\min} )</td>
<td>0 0 ... 0 0 0 0 1</td>
</tr>
<tr>
<td>( x(3) )</td>
<td>( \Delta t_{0;\min} )</td>
<td>0 0 ... 0 0 0 1 0</td>
</tr>
<tr>
<td>( x(4) )</td>
<td>( \Delta t_{0;\min} )</td>
<td>0 0 ... 0 0 0 1 1</td>
</tr>
<tr>
<td>( \vdots )</td>
<td>( \vdots )</td>
<td>( \vdots )</td>
</tr>
<tr>
<td>( x(2^L) )</td>
<td>( \Delta t_{0;\min} )</td>
<td>1 1 ... 1 1 1 1 1</td>
</tr>
<tr>
<td>( x(2^L+1) )</td>
<td>( \Delta t_{0;\min+1} )</td>
<td>0 0 ... 0 0 0 0 0</td>
</tr>
<tr>
<td>( x(2^L+2) )</td>
<td>( \Delta t_{0;\min+1} )</td>
<td>0 0 ... 0 0 0 1 0</td>
</tr>
<tr>
<td>( \vdots )</td>
<td>( \vdots )</td>
<td>( \vdots )</td>
</tr>
<tr>
<td>( x(2^L \times k_{\text{tot}}) )</td>
<td>( \Delta t_{0;\min+\max} )</td>
<td>1 1 ... 1 1 1 1 1</td>
</tr>
</tbody>
</table>

**FIG. 5**
FIG. 6
INITIALIZE TIME OFFSET INDEX $k_{f(t)}$ AND AUXILIARY TABLE INDEX $\mu_i$ BY EVALUATING EQUATIONS 51a-52b

COMPUTE DATA WORD MIDPOINT INDEX $k_{\text{mid}}$, CODE DOPPLER CORRECTION CONSTANTS $\alpha_{fa}$ AND $b_{fa}$, NOMINAL CHIPS PER DATA WORD $L_{typ}$, NUMBER OF FINE TIME INCREMENTS PER CHIP $\Delta k_{fe}$, NOMINAL CHANGE IN FINE TIME OFFSET $\Delta k_{ftyp}$, AND MINIMUM AND MAXIMUM FINE TIME OFFSET $k_{f_{\text{min}}}$ and $k_{f_{\text{max}}}$, USING EQUATIONS 48a-48e AND 50a-50e THESE ARE USED TO DETERMINE THE INDEX INTO PROMPT SIGN, EML ZERO MASK, AND EML SIGN TABLES

COMPUTE $k_{f_{\text{nom}}}$, $\mu_{\text{nom}}$, $\eta_{fs}$, $k_{fs}$, $\mu_s$, $k_s$, and $i_s$, FOR $\nu = 1, ..., N$ BY ITERATING EQUATIONS 53a, 53b, 57a-c, 49, 55, 45 TO COMPUTE INDICES INTO PROMPT SIGN, EARLY-MINUS-LATE ZERO MASK, AND EARLY-MINUS-LATE SIGN TABLES

COMPUTE $x_{p_{fs}}$, $x_{emiz_{fs}}$, and $x_{emiz_{fs}}$, FOR $\nu = 1, ..., N$ BY EVALUATING EQUATIONS 56a-c TO COMPUTE THE PROMPT SIGN, EARLY-MINUS-LATE ZERO MASK, AND EARLY-MINUS-LATE SIGN DATA WORDS

END

FIG. 7
REAL-TIME SOFTWARE RECEIVER

CROSS REFERENCE TO RELATED APPLICATIONS

The present application claims priority to U.S. Provisional Application No. 60/439,391 filed Jan. 10, 2003 entitled REAL-TIME SOFTWARE RECEIVER which is incorporated herein in its entirety by reference.

STATEMENT OF GOVERNMENT INTEREST

This invention was made with United States Government support from the Office of Naval Research (ONR) under contract numbers N00014-02-1-1822 and from the National Aeronautics and Space Administration (NASA) under contract numbers NCC5-563, NAG5-11819, and NAG5-12089. The United States Government has certain rights in the invention.

BACKGROUND OF THE INVENTION

This invention relates generally to software radio receivers, and more specifically to a software receiver for positioning systems.

A typical positioning system receiver, such as is used in the Global Positioning System (GPS), includes an antenna, a radio frequency (RF) section, a correlator, a signal tracking and demodulation component, and a component to compute the navigation solution. The antenna, which is possibly followed by a pre-amplifier, receives L-band GPS signals. The RF section filters and down converts the GHz GPS signal to an intermediate frequency in the MHz range. The RF section also digitizes the signal. The correlator separates the down-converted signal into different channels (ten or more in modern receivers) allocated to each satellite. For each satellite, the correlator mixes the Doppler-shifted intermediate frequency signal to baseband by correlating it with a local copy of the carrier replica signal and it distinguishes the particular satellite by correlating the signal with a pseudo-random number (PRN) code. Software routines cause the carrier replica and PRN replica signals to track the actual received signal, extract the navigation message, and compute the navigation solution.

Baseband mixing is a multiplication of an input signal by a complex exponential where the frequency of the complex exponential approximately matches that of the input signal. The resultant signal is centered at baseband. A complex signal can be broken down into cosine and sine signal components, resulting in separate in-phase and quadrature components. The frequency of the baseband mixed signal must be controllable to within a few millihertz in the case of a phase-locked loop for use in a precision navigation system, and the baseband mixed signal must have a continuously varying phase. In a hardware correlator, local oscillators generate cosine and sine signal components that have precise frequency control and a continuous phase. Generating cosine and sine signal components on the fly with the correct frequency and phase is too time consuming to be feasible for a software correlator. Instead, the software correlator generates cosine and sine signal components on a grid of frequencies off-line. These signal components must be stored on a time grid of points sampled at the RF front-end sampling frequency, for example, at 5.714 MHz for one particular RF front-end hardware configuration, and the signals must last for a typical accumulation period, e.g., for a 0.001 second coarse/acquisition (C/A) PRN code period when working with GPS L1 civilian signals. It takes tens of gigabytes of memory or more in order to brute-force store all frequencies on a one mHz grid ranging from -10 KHz to +10 KHz, which is the needed frequency range when tracking GPS satellites from a terrestrial receiver, and additional storage is required to store a grid of possible starting phases at each frequency point.

PRN code mixing is a multiplication of a baseband mixed signal by a prompt +1/-1 PRN code or by a +2/-2 early-minus-late PRN code, where the code timing and frequency approximately match that of the input signal. The resultant signal is a constant in the case of prompt PRN code mixing, and an approximately linear function of the code timing error in the case of early-minus-late mixing. A receiver accumulates both of these correlation outputs. The magnitude of the prompt accumulation indicates signal strength and whether a signal has been detected, and its in-phase (real) and quadrature (imaginary) components are used to measure carrier phase and Doppler shift. The magnitude of the early-minus-late accumulation measures the code timing error; it will be zero when the timing error is zero.

The code phase of the baseband mixing signal must be controllable to within a percent or less of a PRN code chip for use in a precision navigation system. In a hardware correlator, local oscillators generate the prompt and early-minus-late PRN code replicas. A software correlator can either compute and store PRN code replicas, or compute them in real-time.

The current Global Positioning System is slated to realize expanded capabilities that include new civilian codes on the L2 frequency, a new L5 frequency, and new codes (M-code, CL and CM codes) on the L2 frequency. Some of these upgrades are slated to start within one to three years. A hardware correlator requires hardware modifications in order to use these new signals. In the near term, a receiver designer will be faced with a complex trade-off in order to decide whether the extra complexity is worth the improved performance that will accrue only very slowly as new GPS satellites replace older models. One way to avoid the complex trade-off is to use a software receiver that can receive and process new signals without the need for a new correlator chip set.

A software receiver is flexible because its software components can be easily modified. One application of a software receiver is to merge together numerous devices that use wireless digital communication protocols to form a single device. For example, a cell phone, GPS receiver, and Personal Data Assistant (PDA) could become a single device that plays the role of all three. Another use of a software receiver is to shorten development and to-market times for new wireless devices. For example, as new frequencies and codes are added to GPS, a software receiver having a software correlator simply needs to be reprogrammed, while a hardware approach would require a brand new correlator chip design. New PRN codes can be used simply by making software changes. Thus, software receiver technology lessens the risks involved for designers during the period of transition to the new signals. Furthermore, a software receiver could be reprogrammed to use the Galileo system (European GPS) or GLONASS (Russian GPS).

In the recent past, GPS software receivers have been developed that either post-process stored signals or operate in real-time. Previous real-time software receivers function with a limited number of channels (4-6) or require high-end computer speeds or digital signal processor (DSP) chips such as are disclosed in Real-Time GPS Software Radio
The system and method of the present invention can also include a table of pre-computed baseband mixing sine waves, algorithms that can produce correlation accumulation outputs that are equivalent to what would be produced by a continuously variable sine wave, and a method of use of the table and algorithms. Thus, in the present invention, a relatively small set of sine wave values need to be pre-computed and saved, which can conserve computer memory and processing time.

The system and method of the present invention also includes a system and method for tracking the phase of each PRN code replicas in software in order to track the timing of any given “chip” of the PRN code replica as measured with respect to a pre-specified set of sample times at which the basic raw data comes out of the RF front end (a chip is an element of a PRN code). The PRN code phase is kept track of via a variable for each channel, that indicates the PRN code start time with respect to the RF sample times. The system and method of the present invention allow for the synchronization of the measurements of PRN code phase, carrier phase, and carrier frequency for each satellite relative to these sample times.

The method for tracking the phase of each PRN code replica and the phase of each carrier replica includes the steps of latching all the C/A code phases, carrier phases, epoch counters, and carrier frequencies for each satellite at a pre-specified time, and computing the pseudo range to each satellite using the C/A code phase and epoch counters. The method also includes the step of tracking and updating code and carrier phases by estimating code chipping rate and carrier Doppler shift inputs. The method further includes the step of computing the carrier phase at the pre-specified time for each satellite as a function of the updated code chipping rate and the pre-specified time. The method further includes the step of computing the carrier phase at the pre-specified time as a function of the updated carrier phase, the Doppler shift, and the pre-specified time. The timing of the PRN code phase (or chip location) is the most fundamental of GPS measurements for use in navigation data processing. The monitoring of these times in software allows complete control of the precision with which they can be measured, and it allows precise synchronization of these times with the measurement times of data from other sensors, such as inertial measurement units. This feature gives an enhanced ability to develop what are known as deeply coupled systems that must fuse GPS data with data from other types of sensor systems.

The software correlator of the present invention can advantageously be easily adapted to accept signals at any frequency, new PRN codes, or even signals for different
types of devices. Thus, the same processing hardware could use the software correlator to implement such devices as a GPS receiver, a cell phone, or both. To allow for new codes, new frequencies, and new types of functionality, small changes can be made in the software correlator, or different versions of the software correlator can be run on the same processor. Hardware-correlator-based receivers of the prior art can deal only with frequencies and PRN codes that are hard-wired into their designs. Also, the system and method of the present invention could be implemented within systems such as GLONASS receivers, cell phones and cell base stations, pagers, wireless Ethernet (e.g. 802.11a standards), Bluetooth™, Blackberry® wireless internet devices, and satellite radio/phones (e.g. INMARSAT®). In fact, the system and method of the present invention are applicable to any sort of telecommunication system/device that uses spread spectrum, code division multiple access (CDMA) PRN codes for the transmission of information, either wired or wireless.

For a better understanding of the present invention, together with other and further objects thereof, reference is made to the accompanying drawings and detailed description. The scope of the present invention is pointed out in the appended claims.

DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1 is a schematic block diagram of the hardware environment of a typical software receiver;
FIGS. 2A and 2B are schematic diagrams of bit-wise mappings of signal and carrier replica sign and magnitude bits to computer data words;
FIG. 2C is a graphic representation of a plot of bit-wise parallel radio frequency signal and PRN code replica storage and mixing;
FIG. 2D is a graphic representation of a plot of sections of prompt, early, late, and early-minus-late PRN code signals and 16-bit word representations of their over-sampled equivalents;
FIGS. 3A and 3B are data flow diagrams illustrating the bit-wise parallelism process (replicated twice, once for the in-phase carrier replica and once for the quadrature carrier replica) of the present invention;
FIG. 3C is a graphic representation of a plot of a prior art optimal 2-bit representation of a sine wave presented to enhance the reader’s understanding of the present invention;
FIGS. 4A and 4B are flowcharts of the method for computing correlation accumulations through bit-wise parallel computations of the present invention;
FIG. 5 is a schematic diagram of a look-up table layout as a function of code time offset and chip bit pattern;
FIG. 6 is a graphic representation of a plot illustrating the timing relationship between data word samples and the sequence of prompt code chips that defines an accumulation interval;
FIG. 7 is a flowchart of the method for computing bit-wise parallel representations of the over-sampled prompt PRN code replica and the over-sampled early-minus-late PRN code replica for an entire accumulation interval using the real-time over-sampled PRN code generation algorithm.
FIG. 8 is a graphic representation of a plot that illustrates the location in time at which the code phase of each signal is computed; and
FIGS. 9A and 9B are graphic representations of plots of correlations of the true sampled code with prompt (FIG. 9A) and early-minus-late (FIG. 9B) versions of the true and table look-up codes, the latter being generated by the new real-time over-sampled PRN code generator.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is now described more fully hereinafter with reference to the accompanying drawings, in which the illustrative embodiment of the present invention is shown. The following configuration description is presented for illustrative purposes only. Any computer configuration satisfying the speed and interface requirements herein described may be suitable for implementing the system of the present invention. The equations herein are stated in general terms, but have parameters that are specific to the GPS L1 C/A signal for illustrative purposes only. For example, the 0.001 sec. accumulation interval seen in many of the equations is the nominal C/A code period. Also, the C/A PRN code of the illustrative embodiment can be replaced by the PRN code of any other CDMA signaling system.

By way of introductory explanation, RF signal processing equations and terms are herein provided. The time-domain L1 C/A signal received from, for example, a satellite, is represented by:

\[
y(t) = \sum_j A_j D_j C_j \left[ \frac{\tau_j - \tau_{\text{ref}}}{\tau_{\text{ref}} - \tau_{j+1}} \right] \cos(\omega_j t + \phi_j) + \sigma_j
\]

where \(t\) is the sample time, \(A_j\) is the amplitude, \(D_j\) is the navigation data bit, \(C_j\) is the C/A code, \(\tau_j\) and \(\tau_{j+1}\) are the start times of the received \(k\)th and \((k+1)\)th C/A code periods, \(\omega_j\) is the intermediate frequency corresponding to the L1 carrier frequency, \(\phi_j(t)\) is the carrier phase perturbation due to accumulated delta range, \(\sigma_j\) is the receiver noise, and the subscript \(j\) refers to a particular GPS satellite. The summation is over all visible GPS satellites. The negative sign in front of \(\phi_j(t)\) comes from the high-side mixing that occurs in the RF front-end that has been used in the illustrative embodiment. The signal in equation (1) is the output of a typical RF front-end.

A GPS receiver works with correlations between the received signal and a replica of it. The correlations are used to acquire and track the signal. The replica is composed of two parts, the carrier replica and the C/A PRN code replica. Two carrier replica signals are used, an in-phase signal and a quadrature signal. When mixed with the received signal from the RF front end they form the in-phase and quadrature baseband mixed signals represented by:

\[
y_{\text{I}}(t) = C \left[ 0.001 \left( \frac{t - \tau_j}{\tau_{j+1} - \tau_j} \right) \cos(\omega_j t + \phi_j) \right]
\]

\[
y_{\text{Q}}(t) = C \left[ 0.001 \left( \frac{t - \tau_j}{\tau_{j+1} - \tau_j} \right) \sin(\omega_j t + \phi_j) \right]
\]

where equations (2) and (3) apply during the \(k\)th C/A code period. In these equations \(\tau_{j+1}\) and \(\tau_j\) are the receiver’s...
estimates of the start times of the kth and k+1th code periods, \( \phi_{ik} \) is the estimated carrier phase at time \( \tau_{ik} \) and \( \omega_{Dopp} \) is the estimated carrier Doppler shift during the kth code period.

A typical receiver computes the estimates \( \hat{\tau}_{ik} \), \( \hat{\tau}_{ik+1} \), \( \hat{\phi}_{ik} \) and \( \hat{\omega}_{Dopp} \) by various conventional means that are described in GPS Receivers, A. J. Van Dierendonck, Global Positioning System: Theory and Applications, B. W. Parkinson and J. J. Spilker, Jr., Eds., vol. I, American Institute of Aeronautics and Astronautics, 1996, Chapter 8, pp. 329-406 (Dierendonck), incorporated herein in its entirety by reference. These include open-loop acquisition methods and closed-loop signal tracking methods such as a delay-locked loop to compute \( \hat{\tau}_b \) and \( \tau_{b+1} \) and a phase-locked loop or a frequency-locked loop to compute \( \hat{\phi}_b \) and \( \phi_{Dopp} \).

Both prompt and early-minus-late correlations are needed to track the carrier frequency, carrier phase, and code phase in a GPS receiver. A typical receiver uses the PRN code and carrier replicas to compute the following in-phase and quadrature correlation accumulations:

\[
I_{jk}(\Delta) = \sum_{r=q}^{q+p} y(r)C_r \left[ 0.00, \left( I_{jk} + \Delta - \frac{\tau_{jk}}{\tau_{jk+1}} - \frac{\tau_{jk+1}}{\tau_{jk}} \right) \cos(\omega_{Dopp}r) 
- \phi_{jk} \right]
\]

\[
Q_{jk}(\Delta) = \sum_{r=q}^{q+p} y(r)C_r \left[ 0.00, \left( I_{jk} + \Delta - \frac{\tau_{jk}}{\tau_{jk+1}} - \frac{\tau_{jk+1}}{\tau_{jk}} \right) \sin(\omega_{Dopp}r) 
- \hat{\phi}_{jk} \right]
\]

where \( jk \) is the index of the first RF front-end sample time that obeys \( \tau_{jk} \leq \tau_b \) and \( N_b+1 \) is the total number of samples that obey \( \tau_{jk} \leq \tau_b \leq \tau_{jk+1} \). The time offset \( \Delta \) causes the replica PRN code to play back early if it is positive and late if \( \Delta \) is negative. The prompt correlations are defined by equations (4) and (5) with \( \Delta = 0 \). The early-minus-late correlations are \( I_{jk}(\Delta_{m/l}) = I_{jk}(-\Delta_{m/l}) \) and \( Q_{jk}(\Delta_{m/l}) = Q_{jk}(-\Delta_{m/l}) \), where \( \Delta_{m/l} \) is the spacing between the early and late PRN carrier replicas. The present invention describes herein is an efficient technique for the receiver to accumulate \( I_{jk} \) and \( Q_{jk} \) in software.

Referring now to FIG. 1, the operational platform of the software receiver 10 of the present invention includes an antenna 11, conventional RF front-end 13, a data acquisition (DAQ) system 17, a microprocessor 16, a software correlator 19, and application-specific code 15. Conventional RF front-end 13 interfaces with antenna 11 and with (DAQ) system 17. DAQ system 17 includes a system of shift registers and a data buffer. Microprocessor 16 executes software correlator 19, which includes a set of specially developed bit-wise parallel algorithms, and application-specific code 15, such as the GPS navigation and tracking functions. In the illustrative embodiment, conventional GPS software functions (signal tracking, data extraction, navigation solution, etc.) are provided by the MITEL® GPS Architect software ported to RTLINUX® (see A Coming of Age for GPS: A RTLINUX BASED GPS RECEIVER, Ledvina et al., Proceedings of the Workshop on Real Time Operating Systems and Applications and Second Real Time Linux Workshop (in conjunction with IEEE RTSS 2000) Nov. 27-28, 2000), but can be provided by any equivalent configuration.

Continuing to refer to FIG. 1, conventional RF front-end 13 can, for example, be a MITEL® GP2015 RF front-end, which down converts the nominal 1575.42 MHz GPS signal 12 to an intermediate frequency of (88.54-63)x10^6 Hz-4053968254 MHz and then performs analog-to-digital conversion. The resultant, digitized signal data 21 has a pre-determined number of bits/sample, such as two binary bits/sample, a sign bit and a magnitude bit, or one bit/sample. The shift registers in the DAQ system 17 parallelize the magnitude and sign data bit streams into separate words, which the DAQ system 17 reads into the memory of the microprocessor 16 using DMA. To make the process of reading data into the microprocessor 16 more efficient and to prepare for efficient correlation calculations, DAQ system 17 can read a pre-specified number of bits of buffered samples, such as thirty-two bits, at a time. The exemplary thirty-two bits include sixteen sign bits and sixteen magnitude bits.

Referring now to FIGS. 1 and 2A, the shift registers in DAQ system 17 (FIG. 1) buffer signal data 21 (FIGS. 1 and 2A) and pack signal sign 21A (FIG. 2A) and signal magnitude 21B (FIG. 2B) into separate words, that represent the integer values +1 and -1 as is shown in Table 1. In the case of the 1-bit signal, the bit stream representing the samples is packed into successive words to prepare the signal for bi-wise parallel processing. DAQ system 17 also provides for accurate timing by, for example, synchronizing signal sign 21A and signal magnitude 21B to a (407)x10^6 Hz=5.714 MHz clock signal, which can be, for example, a third output from conventional RF front-end 13 (FIG. 1). DAQ system 17 can convert the 5.71424 MHz clock signal down to 357.14 KHz by use of, for example, a divide-by-16 counter for a 16-bit word, which can provide a signal indicating when the buffer is full. DAQ system 17 can use any method for providing a buffer full indication.

<table>
<thead>
<tr>
<th>Signal Sign 21A</th>
<th>Signal Magnitude 21B</th>
<th>RF Signal Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>-3</td>
<td>-3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>-1</td>
<td>-1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

With further reference to FIG. 1, in the illustrative embodiment, the DAQ system 17 can consist of an interface card and driver software that can be compatible with, for example, a 1.73 GHz AMD ATHLON processor running RTLINUX®, but could be compatible with any operating system and any processor that can accommodate real-time operations. The interface card can, for example, be a NATIONAL INSTRUMENTS® PCI-DIO-32HS digital I/O card. Pertinent features of this card are the thirty-two digital input lines, DMA, and availability of a driver for RTLINUX®, perhaps gotten from the suite of open-source drivers and application interface software for interface cards known as COMEDI (Control and MEasurement Device Interface). Modifications to the conventional COMEDI driver for the PCI-DIO-32HS card include increasing the number of input bits from sixteen to thirty-two, enabling DMA, and modifying the driver to support continuous interrupt-driven acquisition.

With still further reference to FIG. 1, microprocessor 16 can be, for example, a 1.73 GHz AMD ATHLON™ proces-
In the illustrative embodiment in which the system and method of the present invention are used in a GPS (or similar) environment, microprocessor 16 can store the most recent twenty-one milliseconds of signal data 21 (FIGS. 1 and 2A) in the circular buffer, but could store more or less. The present invention does not fix the size of the circular buffer, nor the amount of RF data that can be stored there. The circular buffer allows the processing of code periods that start and stop at different times for different satellites during different iterations of a regularly scheduled program thread. DMA memory space can be written to directly by DAQ system 17 using a DAQ software driver, which fills the circular buffer. Communication between software correlator 19 and application-specific code 15 can be performed using operating system-provided shared memory capability. For example, the mbuff driver, included with RTLINUX®, can be used to create and manage this shared memory space. Any memory management system that accommodates real-time processing can be used. If the mbuff driver is used, kernel modules can share memory and the kernel can be restricted from swapping the shared memory space to long-term storage.

Continuing with the analogy to hardware correlation, and still referring primarily to FIG. 1, in hardware correlation, the correlator receives frequency and phase information from tracking and acquisition loops that are part of application code, and Numerically Controlled Oscillators (NCOs) generate signals that correspond to the written frequencies and phases. In contrast, software correlator 19 includes simulated carrier and code NCOs that receive their frequency commands from application-specific code 15. Software correlator 19 uses these frequency commands to reconstruct carrier replica signal 25 (FIG. 3A) and prompt PRN code 29 and early-minus-late PRN code 35 (FIG. 3A) which it mixes with the signal data 21 (FIG. 2A) resulting in fully mixed prompt integrand 31 and fully mixed early-minus-late integrand 33 (FIG. 3A).

To further continue the analogy, a hardware correlator generates in-real-time a particular C/A code replica at the correct Doppler shifted frequency and phase. In contrast, software correlator 19 can generate C/A codes off-line and store them in a memory table, the pre-computed oversampled PRN code table 28 in this embodiment. The pre-computed oversampled PRN code table 28 is used to select PRN codes with the correct timing relationship to the sample times of signal data 21 (FIG. 3A). The codes are then used to form correlations with baseband mixed signals 23 (FIG. 3A), the result from which is summed to produce the standard in-phase and quadrature, summed prompt accumulation 45 (FIG. 3B) and summed early-minus-late accumulation 47 (FIG. 3B) that are equivalent to what would be produced by a continuously variable sine wave. These are provided to application-specific code 15, such as conventional GPS software that executes signal tracking and navigation functions. In a second approach, software correlator 19 can generate the PRN carrier replicas on-line at the code chip rate and can use tabulated functions to re-sample the code at the sample rate of the RF front-end for purposes of calculating accumulations. Real-time oversampled PRN code generator 30A (FIG. 3A) is used in place of pre-computed oversampled PRN code table 28 (FIG. 3A) in this latter approach. This latter method can be used with longer PRN codes, such as the new civilian GPS L5 CL codes.

With still further reference to FIG. 1, since the received L1 raw signal 12 can have an uncertain carrier phase, software correlator 19 computes both in-phase (I) and quadrature (Q) accumulations, as defined in equations (4) and (5). Software correlator 19 begins the accumulation process by using carrier replica signal 25 (FIG. 3A), which it gets from pre-stored carrier replica table 30 (FIG. 3A). The carrier replicas in this table fall on a rough frequency grid, and they all start with a particular phase, for example a phase of zero. The baseband mixing process involves selecting a carrier replica signal 25 (FIG. 3A) from carrier replica table 30 (FIG. 3A) that is at the frequency that is as close to "ideal" as possible. In the case of a 175 Hz grid spacing, the baseband mixing process selects a signal that is maximally within ±87.5 Hz of the ideal signal. The rough frequency grid can have a spacing of, for example, 175 Hz but could be larger or smaller depending on (a) the frequency range needed to cover, for example, ±10 KHz, (b) the amount of space available for storing pre-computed signals, and (c) other design decisions. The pre-computed signals in carrier replica table 30 (FIG. 3A) each may occupy 180 32-bit words in order to be guaranteed to cover the full 5,714 RF front-end samples that occur in one PRN code period for any possible code period start time within the thirty-two samples of the initial word. Thus, 180×4×720 bytes could be required for each bit of each pre-computed carrier replica signal 25 that is stored in the table. The sine and cosine waves of carrier replica signals 25 (FIG. 3A) each have 2-bit representations, which translates into a storage requirement of 2880 bytes for the carrier replica signals 25 at a given Doppler shift. There are 115 Doppler shifts that may be stored in order to cover the -10 KHz to +10 KHz range with a 175 Hz grid spacing. This translates into 323 Kbytes of storage for all of the carrier replica signals 25. This approach avoids the need to pre-compute sine waves with a prohibitively large number of possible frequencies and phase offsets and it avoids the need to compute sine waves in real-time. Instead, the errors created by using pre-defined sine wave replicas are compensated for by post-processing calculations, as described below.

In any case, and continuing to refer to FIG. 1, the resulting accumulations are

\[
i_{i,j}(\Delta) = \sum_{\Delta t \in \Delta} y(t) C_{i,j} \cos(\omega_{i,j} t - \phi_{i,j} + \phi_{i,j}(\Delta))
\]

where

\[
i_{i,j}(\Delta) = \sum_{\Delta t \in \Delta} y(t) C_{i,j} \cos(\Delta t - \phi_{i,j} + \phi_{i,j}(\Delta))
\]
where $\omega_{gk}$ is the grid frequency that is closest to the estimated frequency $\omega_{doppk}$ and where $\omega_{doppk}$ is the time at which this carrier replica signal 25 (FIG. 3A) has zero carrier phase. Software correlator 19 rotates these accumulations in order to create accurate approximations of what would have been computed had the estimated carrier phase time history in equations (4) and (5) been used:

$$I_d(\lambda) = I_d(\lambda) \cos(\Delta \phi_{avg}) + Q_d(\lambda) \sin(\Delta \phi_{avg})$$  

$$Q_d(\lambda) = -I_d(\lambda) \sin(\Delta \phi_{avg}) + Q_d(\lambda) \cos(\Delta \phi_{avg})$$  

where $\Delta \phi_{avg}$ is the average phase difference between the grid carrier phase and the estimated carrier phase averaged over the accumulation interval:

$$\Delta \phi_{avg} = \frac{\phi_{gk} + \phi_{gk-1} - \phi_{doppk}}{2} - \phi_{doppk}$$  

$$\phi_{doppk} = \frac{\phi_{gk} + \phi_{gk-1} - \phi_{doppk}}{2} + \phi_{doppk}$$

Note that equations (8), (9), and (10) are an illustrative example of how software correlator (19) can rotate its I and Q accumulations in order to correct for phase and frequency errors in its table of pre-computed carrier replica signals. There exist other formulas that yield equivalent results, and this patent disclosure covers all such techniques.

The validity of equations (8) and (9) is dependent on the assumption that

$$1 - \cos[\frac{1}{2}(\omega_{gk} - \omega_{doppk})(\phi_{gk-1} - \phi_{doppk})] \leq 1$$

For example, a 175 Hz grid spacing and a nominal C/A PRN code period of 0.001 sec yields a value on the left-hand side of inequality (11) of 0.04, which respects the assumed limit.

Note that equations (8) and (9) can be derived from equations (4) and (5) as follows. First, the carrier phase of the grid signal in the arguments of the cosine and sine terms of equations (6) and (7) are added to and subtracted from the arguments of the cosine and sine terms in equations (4) and (5). Next, trigonometric identities are used to split the resulting cosine and sine terms into sums of products of cosine and sine functions. In each product, one of the terms involves an argument like the arguments in the trigonometric terms in equations (6) and (7). The other trigonometric terms are then approximated by either $\cos(\Delta \phi_{avg})$ or $\sin(\Delta \phi_{avg})$. These approximations are valid because of the inequality in equation (11) and because the average of $\sin \left\{ \omega_{doppk} \right\}$ over the accumulation interval is zero.

A decrease in the carrier to noise ratio C/N0, which characterizes the receiver's sensitivity, is caused by the use of an inexact baseband mixing frequency. The worst-case decrease is expressed as a function of the frequency grid spacing $\Delta f$ and is given by

$$\Delta SNR = 20 \log \left( \frac{\sin(\Delta f/T)}{\pi \Delta f/T} \right)$$

where $\Delta f$ is in units of Hz, and $T$ is the integration period. Thus, a $\Delta f$ of 175 Hz causes a worst-case C/N0 loss of 0.11 dB for $T=0.001$ sec.

Referring now to FIGS. 2A, 2B, and 3A, PRN codes (composed of prompt PRN codes 29 (FIG. 3A) and early-minus-late PRN codes 35 (FIG. 3A)) are either pre-computed or generated in real-time. Pre-computing involves, for each satellite, computing an entire PRN code, storing the PRN code appropriately for easy retrieval, and referencing the PRN code, possibly by means of indices that are computed based on, for example, the incoming RF signal data 21 (FIGS. 2A and 3A). Pre-computing can be most advantageously used when the PRN code is not very long. Generating PRN codes in real-time can be a more appropriate solution when the PRN codes are very long (and thus would require an unacceptable amount of storage), or perhaps when too many PRN codes are required for the amount of storage available, or for any other reason, but real-time PRN code generation can entail an additional computational cost. Both pre-computing and real-time determination of PRN codes are described herein with respect to a bit-wise parallel implementation.

Continuing to refer primarily to FIGS. 2A, 2B, and 3A, in order to perform bit-wise parallel operations, software correlator 19 (FIG. 1) stores pre-computed carrier replica sign 25A (FIGS. 2B and 3A) and carrier replica magnitude 25B (FIGS. 2B and 3A) in data words. Simple representations of signal data 21 (FIGS. 2A and 3A) and carrier replica signal 25 (FIGS. 2B and 3A) in terms of one, two, or more bits are suitable for using bit-wise parallelism to perform the calculations described herein. Bit-wise parallel operations work with representations of the data that store successive samples in successive bits of a word. For example, thirty-two samples (bits) of the RF front-end output are stored in two N=32-bit words, signal sign 21A (FIGS. 2A and 3A) and signal magnitude 21B (FIGS. 2A and 3A), or simply a single 32-bit word if signal data 21 consists of a single data bit. Carrier replica sign 25A (FIGS. 2B and 3A) and carrier replica magnitude 25B (FIGS. 2B and 3A) are stored, for example in tables, in separate words, with each 32-bit word storing thirty-two sign or magnitude bits that tabulate to thirty-two successive samples of the corresponding cosine or sine wave. Similarly, tables can store prompt PRN code 29 (FIG. 3A) and early-minus-late PRN code 35 (FIG. 3A), which are composed of prompt PRN code sign 29A (FIG. 3A), early-minus-late PRN code sign 35A (FIG. 3A), and early-minus-late PRN code zero mask 35B (FIG. 3A). The data words that comprise the bit-wise parallel representations of these three signal types, the original RF signal data 21 (FIGS. 2A and 3A), the carrier replica signal 25 (FIGS. 2B and 3A), and the de-spreading prompt PRN code 29 (FIG. 3A) and early-minus-late PRN code 35 (FIG. 3A), are the inputs to the calculations of software correlator 19 (FIG. 1).
magnitude 23B (FIG. 3A), and baseband mixed low magnitude 23C (FIG. 3A). The second bit-wise parallel signal type is the fully mixed integrand, of which there are four signals: in-phase and quadrature fully mixed prompt integrand 31 (FIG. 3A) and in-phase and quadrature fully mixed early-minus-late integrand 33 (FIG. 3A). The former are stored as 3-bit representations in the illustrative embodiment as fully mixed prompt integrand sign 31A (FIG. 3A), fully mixed prompt integrand high magnitude 31B (FIG. 3A), and fully mixed prompt integrand low magnitude 31C (FIG. 3A). The latter are stored as 3.5-bit representations in the illustrative embodiment as fully mixed early-minus-late integrand sign 33A (FIG. 3A), fully mixed early-minus-late integrand high magnitude 33B (FIG. 3A), fully mixed early-minus-late integrand low magnitude 33C (FIG. 3A), and fully mixed early-minus-late integrand zero mask 33D (FIG. 3A). This representation is called a 3.5-bit representation because the sign, high-magnitude, and low-magnitude bits are ignored if the corresponding zero mask bit has the value zero. The third bit-wise parallel signal type is a value word, of which there are two types: prompt integrand value words 27 (FIG. 3B) and early-minus-late integrand value words 37 (FIG. 3B). Each fully mixed integrand is used to construct value words, one word for each possible value that the integer integrand can take on. There are eight possible values for the integrands of the illustrative embodiment: -1, -2, -3, -6, 1, 2, 3, and 6 for the in-phase and quadrature fully mixed prompt integrands 31 (FIG. 3A) and -2, -4, -6, -12, 2, 4, 6, and 12 for the in-phase and quadrature fully mixed early-minus-late integrands 33 (FIG. 3A). Each bit-wise parallel value word contains a one bit for each sample time when the integrand value equals the value of the word value, but it contains a zero bit for all other sample times. The storage of raw data and intermediate results in bit-wise parallel format allows the EXCLUSIVE OR operations that are involved in mixing to operate on thirty-two samples at a time if microprocessor 16 (FIG. 1) has a bit-wise EXCLUSIVE OR command. Other bit-wise commands are used to perform additional software correlation operations in parallel on sets of two thirty-two samples.

At this point, the problem of over-sampling is introduced. Referring now to FIGS. 2c and 2d, the problem of over-sampling is illustrated with respect to bit-wise parallelism as follows. There is normally more than one RF data sample per PRN code chip. The three successive -1 values 73 (FIG. 2c) at sample times t1 to t3 all occur during the same PRN code chip as do the four successive +1 values 75 (FIG. 2c) at times t4 through t7. The difference in the number of samples for the two code chips arises because the PRN code chip period is not an integer multiple of the sample period. Analogously, referring to FIG. 2d, where sample interval Δt 63 is less than actual PRN code chip length Δt 65, over-sampling is indicated because the RF sampling frequency f s/Δt is greater than the PRN code chip encoding frequency f c/Δt. PRN codes for CDMA signaling are sequences of +1 and -1 values, the elements of which are chips. Over the time intervals of interest, a carrier replica progresses through its chips at a constant chip rate of f c=1/Δt chips/second. The time interval Δt is the actual PRN code chip length 65 (FIG. 2d). Software correlator 19 (FIG. 1) normally receives PRN code, and attempts to align it with the prompt replica version of the code, prompt PRN code 29 (FIG. 2d). It makes use of the signal’s correlation with prompt PRN code 29 (FIG. 2d) and with early-minus-late PRN code 35 (FIG. 2d) in order to determine a chipping rate f c that tends to align prompt PRN code 29 (FIG. 2d) as desired. Conventional methods for determining f c are well-known in the art. Chips of early code 69B (FIG. 2d) start and stop 0.5Δt ol seconds before the corresponding chips of prompt PRN code 29 (FIG. 2d), and the chips of late code 69C (FIG. 2d) start and stop 0.5Δt ol seconds after prompt PRN code 29 (FIG. 2d). Early-minus-late PRN code 35 (FIG. 2d) is the difference between early code 69B (FIG. 2d) and late code 69C (FIG. 2d). Example segments of these four types of replica codes are depicted in FIG. 2d.

Referring to FIGS. 1, 2a, 2c, and 2d software correlator 19 (FIG. 1) receives, through conventional RF front end 13 and DAQ system 17, signal data 21 (FIG. 1), the raw data 12 (FIG. 1) of which is sampled at the rate f s=1/Δt Hz. In order to process the resulting RF signal data 21, software correlator 19 (FIG. 1) needs prompt PRN code 29 (FIG. 2d) and early-minus-late PRN code 35 (FIG. 2d) replicas sampled at the same times as raw signal 12 (FIG. 1). FIG. 2d depicts sixteen sample times as vertical dash-dotted lines. Referring to FIG. 2d, prompt PRN code 29 (FIG. 2d) can be represented by its prompt PRN code sign 29A (FIG. 2d) at the sample times. The bit value one represents +1, and the bit value zero represents -1. Prompt PRN code sign 29A (FIG. 2d), shown at the sixteen sample times—starting with three 1s, continuing with ten 0s, and finishing with another three 1s—is a 16-bit word stored as the integer $2^{15}2^{14}2^{13}2^{2}2^{1}2^{0}=57351$. Early-minus-late PRN code 35 (FIG. 2d) requires a 1.5-bit representation. A zero mask bit is set to zero if early-minus-late PRN code 35 takes on the value zero, and it is set to one if early-minus-late PRN code 35 equals +2 or -2. Early-minus-late PRN code zero mask 35B (FIG. 2d) at sixteen sample times shown in FIG. 2d is equivalent to $2^{13}2^{12}2^{11}2^{10}=12292$. A 2's sign bit is set to one if early-minus-late PRN code 35 (FIG. 2d) equals +2 at the sample time, and it is set to zero if the code equals -2. The 2's sign bit is irrelevant if the corresponding early-minus-late PRN code zero mask 35B (FIG. 2d) bit equals zero. Early-minus-late PRN code sign 35A (FIG. 2d) for sixteen sample times contains X values that indicate bits whose values are irrelevant because the corresponding early-minus-late PRN code zero mask 35B (FIG. 2d) bits are zero. In an illustrative embodiment, all the X values become zero, thus the equivalent integer for early-minus-late PRN code sign 35A (FIG. 2d) is $2=4$.

Continuing to refer to FIG. 3A, an alternative to taking the prompt PRN code 29 and early-minus-late PRN code 35 from pre-computed over-sampled PRN code table 28 is to generate prompt PRN code sign 29A, early-minus-late PRN code sign 35A, and early-minus-late PRN code zero mask 35B using real-time over-sampled PRN code generator 30A (FIG. 3A). Shown in FIG. 3A are two circles and a loose arrow with a quarter circle pointer. These are the symbols for a switch and indicate the ability of the system to choose possible alternate sources of PRN code. Using the real-time over-sampled PRN code generator 30A includes a step of generating the PRN code chips in real-time by conventional means. For example, the GPS civilian L2 C1 and CM codes are generated by a 27-bit feedback shift register (see The New L2 Civil Signal, R. D. Fontana et al., Proceedings of the ION GPS 2001, Sep. 11–14, 2001, Salt Lake City, Utah, pp. 617–631). The method further includes the steps of choosing chip values from the PRN code, where the chip values correspond to a data interval that contains the samples of a data word and where the chips have a known timing relative to the data interval, transforming the relative timing into a
time grid index, and translating the PRN code chip values and the time grid index for the data interval into the PRN code's over-sampled bit-wise parallel format. These latter steps can be carried out efficiently by using a table look up function. One table each for prompt PRN code sign 29A, early-minus-late PRN code sign 35A, and early-minus-late PRN code zero mask 35B can constitute integer values that constitute the bit-wise parallel representation of the PRN code for the sample times associated with the data words in question. Indices into each 1-dimensional table are functions of (a) the time offset between the first PRN code chip and the first sample time of the given data word, and (b) the bit pattern of the PRN code chips that span the sample times of the data word. The sizes of the tables are independent of the period of the PRN code that is being over-sampled. The tables can be re-used for multiple PRN codes in a multi-channel receiver. The computation and use of the tables are discussed in more detail later.

Continuing with the description of bit-wise parallelism with respect to the operations of software correlator 19 (FIG. 1), and continuing to refer to FIG. 3A, the specially-developed algorithms described herein make use of bit-wise parallelism so that a single programming language statement, such as a C code command, can partially process up to thirty-two samples at a time. Previously referred-to carrier replica signal 25 in the form of cosine and sine signals are stored as binary carrier replica sign 25A and carrier replica magnitude 25B. The format of this representation is defined in Table 2 and illustrated in FIG. 3C. The format is defined in Table 2 and illustrated in FIG. 3C which is a reconstructed carrier and carrier replica in the form of representative sine signal 51 (FIG. 3C) shown in optimal 2-bit representation 53 (FIG. 3C) that has the minimum square error. The format of Table 2 assumes that the cosine and sine signals have an amplitude of approximately 2.4. Note that other representations, beyond 2-bit representation, are possible. In general, more bits yield a better SNR, but can also require a larger number of computations for the correlation operations.

**TABLE 2**

<table>
<thead>
<tr>
<th>Carrier Replica Sign (25A)</th>
<th>Carrier Replica Magnitude (25B)</th>
<th>Carrier Replica Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>−1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>−2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>+1</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td>+2</td>
</tr>
</tbody>
</table>

Continuing to refer to FIG. 3A, multiplication of the RF front-end output representation, the signal sign 21A and signal magnitude 21B, of Table 1 by the sine wave representation, carrier replica sign 25A and carrier replica magnitude 25B, of Table 2 yields baseband mixed signals 23, consisting of baseband mixed sign 23A, baseband mixed high magnitude 23B, and baseband mixed low magnitude 23C, that can take on the values −6, −3, −2, −1, +1, +2, +3, and +6, as shown in Table 3. Baseband mixed high magnitude 23B is simply signal magnitude 21B, and baseband mixed low magnitude 23C is carrier replica magnitude 25B. Thus, these two magnitude bits are available without the need for computation. Baseband mixed sign 23A is the result of an EXCLUSIVE OR operation between signal sign 21A and carrier replica sign 25A. Notice how the relationship of the sign bit value with the actual sign gets reversed from that of Tables 1 and 2.

**TABLE 3**

<table>
<thead>
<tr>
<th>Baseband Mixed Sign 23A</th>
<th>Baseband Mixed High Magnitude 23B</th>
<th>Baseband Mixed Low Magnitude 23C</th>
<th>Baseband Mixed Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>+1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>+2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>+3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>+1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>−2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>−3</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>−6</td>
</tr>
</tbody>
</table>

Continuing to refer to FIG. 3A, and continuing to describe the bit-wise parallel algorithms, the required amount of storage for tables of pre-computed prompt PRN code 29 and early-minus-late PRN code 35 can be greatly reduced by making two simplifications. First, the prompt PRN code 29 is stored as prompt PRN code sign 29A. This representation is shown in Table 4. The early-minus-late PRN code 35, on the other hand, is stored in a two-bit representation (actually a 1.5 bit representation): early-minus-late PRN code sign 35A and early-minus-late PRN code zero mask 35B, as denoted in Table 5. Note that the X in the first column of Table 5 indicates that zero or one can be placed in this location without affecting the corresponding code value. The X signifies a lack of effect of the sign bit on the code value when the zero mask bit equals zero. This is why the early-minus-late PRN code 35 representation is referred to as a 1.5-bit representation. This X value will affect the corresponding fully mixed early-minus-late integrand sign 33A, but it will not affect any of the early-minus-late value words because the zero value in the corresponding zero mask location will null out the corresponding bit of all early-minus-late value words.

**TABLE 4**

<table>
<thead>
<tr>
<th>Prompt PRN Code Sign 29A</th>
<th>Prompt Code Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+1</td>
</tr>
<tr>
<td>0</td>
<td>−1</td>
</tr>
</tbody>
</table>

**TABLE 5**

<table>
<thead>
<tr>
<th>Early-minus-late PRN Code Sign 35A</th>
<th>Early-minus-late PRN Code Zero Mask 35B</th>
<th>Early-Minus-Late Code Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>−2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>+2</td>
</tr>
</tbody>
</table>

Another simplification in the pre-computed over-sampled PRN code table 28, and continuing to refer to FIG. 3A, can be to ignore code Doppler shift variations. All signals in the table are assumed to have zero Doppler shift; i.e., all C/A codes in the table assume that τp,sn=τp,sn=0.001 sec. Note that the period of 0.001 is applicable for accumulations that use
the full 1023 chips of the C/A code only. Any other type of code or accumulation interval may have a different period. The code phase errors due to this assumption can be eliminated by choosing a replica code from the pre-computed over-sampled PRN code table 28 whose midpoint occurs at the desired midpoint time \((\frac{\tau_S + \tau_{\text{rep}}}{2})\). The only other effect of this assumption can be a small correlation power loss, which is no more than 0.014 dB if the magnitude of the Doppler shift is less than 10 KHz. The pre-computed over-sampled PRN code table 28 stores over-sampled bit-wise parallel representations of chips \(c(t)\) through \(C(M)\). The table must allow for the retrieval of over-sampled bit-wise parallel code replicas for a range of start times of code chip \(c(t)\) that span the entire first data sample word in the accumulation interval \(W\), \(95\) (FIG. 6).

The table may contain code replicas whose different phases yield start times that span only a single sample interval of data word \(W\), \(95\) (FIG. 6), which is only \(1/n\) of the required number of start times. In this case the software correlator may apply bit shift operations to a tabulated PRN code replica from that sample interval in order to generate the over-sampled bit-wise parallel PRN code replica that applies when chip \(c(t)\) starts in a different sample interval of data word \(W\), \(95\) (FIG. 6).

Continuing to refer to FIG. 3A, and further continuing to describe the bit-wise parallel algorithms, prompt PRN code \(29\) and early-minus-late PRN code \(35\) replicas can be mixed with the baseband mixed signals \(23\) to form fully mixed prompt integrand \(31\) by an EXCLUSIVE OR operation and bit re-definitions. An EXCLUSIVE OR between prompt PRN code sign \(31\) and baseband mixed sign \(23\) produces fully mixed prompt integrand sign \(31\) given in Table 6. The fully mixed prompt integrand high magnitude \(31B\) and fully mixed prompt integrand low magnitude \(31C\) are baseband mixed high magnitude \(23B\) and baseband mixed low magnitude \(23C\), also given in Table 6. Note that the Table 6 representation is identical to that of Table 3 except for the inversion in the meaning of the sign bits. The number of magnitude bits is dependent upon the design of the system and no set number of magnitude bits is required by the present invention. A change in the number of magnitude bits will cause a change in the number of entries of the equivalent of Table 6 and it will affect the possible values of the integrand.

TABLE 6

<table>
<thead>
<tr>
<th>Sign, high-magnitude, low-magnitude</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prompt Fully Mixed Prompt</td>
<td>1</td>
</tr>
<tr>
<td>Prompt Fully Mixed Prompt Integrand</td>
<td>1</td>
</tr>
<tr>
<td>Prompt Fully Mixed Prompt Integrand High Magnitude</td>
<td>1</td>
</tr>
<tr>
<td>Prompt Fully Mixed Prompt Integrand Low Magnitude</td>
<td>1</td>
</tr>
<tr>
<td>Prompt Fully Mixed Prompt Integrant Value</td>
<td>1</td>
</tr>
</tbody>
</table>

Still continuing to refer to FIG. 3A, the mixing of the early-minus-late PRN code \(35\) with the baseband mixed signals \(23\) forms fully mixed early-minus-late integrands \(33\). Fully mixed early-minus-late integrand sign \(33A\) is an EXCLUSIVE OR between early-minus-late PRN code sign \(35A\) and baseband mixed sign \(23A\). Fully mixed early-minus-late integrand high magnitude \(33B\) and fully mixed early-minus-late integrand low magnitude \(33C\) are, as above, baseband mixed high magnitude \(23B\) and baseband mixed low magnitude \(23C\). Fully mixed early-minus-late integrand zero mask \(33D\) is early-minus-late PRN code zero mask \(23B\). The resulting representation is given in Table 7. As in Table 5, each \(X\) entry in the table indicates that the corresponding bit can be either zero or one without affecting the corresponding integrand value.

TABLE 7

| Sign, high-magnitude, low-magnitude, and zero mask bit combinations of the fully mixed early-minus-late integrands \(33\) and their corresponding values. |
|------------------------------------|-------|
| Early-Minus-Late (EML) Integrand Sign \(33A\) | Value |
| EML | High Magnitude | 33B |
| EML | Low Magnitude | 33C |
| EML | Zero Mask | 33D |
| Early-Minus-Late Integrant Value | 1 |

Referring now to FIGS. 3A, 3B, 4A, and 4B, the method for computing in-phase and quadrature accumulations for every accumulation period, for example every millisecond for GPS C/A code, by use of bit-wise parallelism includes the steps of selecting carrier replica signal \(25\) (FIG. 3A) according to the proximity of its frequency to the desired frequency, and representing sample signal data \(21\) (FIG. 3A) and carrier replica signal \(25\) (FIG. 3A) from at least one channel as bits in signal sign \(21A\) (FIG. 3A) and, if present, signal magnitude \(21B\) (FIG. 3A) and carrier replica sign \(25A\) (FIG. 3A) and carrier replica magnitude \(25B\) (FIG. 3A) (method step \(101\), FIG. 4A). Note that carrier replica signal \(25\) (FIG. 3A) is chosen so that its frequency is close to the correct signal frequency. The method also includes the step of mixing signal data \(21\) (FIG. 3A) to baseband by computing in-phase and quadrature baseband mixed sign \(23A\) (FIG. 3A) and in-phase and quadrature baseband mixed high and low magnitude \(23B/C\) (FIG. 3A) (method step \(103\), FIG. 4A).
Referring again to FIGS. 3B and 4A, method step 109 (FIG. 4A) calls for computing value words. This computation starts by performing bit-wise parallel Boolean logic for each of the possible values in the right-hand column of the prompt integrand representation in Table 6. A 32-bit prompt integrand value word 27 (FIG. 3B) is computed for each thirty-two samples and each row of Table 6. The prompt integrand value word 27 (FIG. 3B) contains ones for the sample times when the actual integrand equals the corresponding value in the right-hand column of Table 6, and zeros for the remaining times when the actual integrand does not equal this value. The prompt integrand value words 27 (FIG. 3B) corresponding to the possible Table 6 values are formed by method step 109 (FIG. 4A) as follows:

- MINUSONE = [NOT(SIGN) AND NOT(HIGHMAG) AND NOT(LOWMAG)]
- MINUSTWO = [NOT(SIGN) AND NOT(HIGHMAG) AND LOWMAG]
- MINUSTHREE = [NOT(SIGN) AND [HIGHMAG AND NOT(LOWMAG)]
- MINUSIX = [NOT(SIGN) AND [HIGHMAG AND NOT(LOWMAG)]
- PLUSONE = [SIGN AND [HIGHMAG AND NOT(LOWMAG)]
- PLUSIX = [SIGN AND [HIGHMAG AND NOT(LOWMAG)]
- PLUSTWO = [SIGN AND [LOWMAG]
- PLUSTHREE = [SIGN AND [HIGHMAG AND NOT(LOWMAG)]
- PLUSIX = [SIGN AND [HIGHMAG AND LOWMAG]
- MINUSTWELVE = [ZEROMASK AND NOT(SIGN) AND NOT(HIGHMAG) AND NOT(LOWMAG)]
- MINUSFOUR = [ZEROMASK AND NOT(SIGN) AND NOT(HIGHMAG) AND LOWMAG]
- MINUSSEVEN = [ZEROMASK AND NOT(SIGN) AND [HIGHMAG AND NOT(LOWMAG)]
- MINUSFOUR = [ZEROMASK AND NOT(SIGN) AND [HIGHMAG AND NOT(LOWMAG)]
- PLUSFOUR = [ZEROMASK AND [HIGHMAG AND NOT(LOWMAG)]
- PLUSFOUR = [ZEROMASK AND [HIGHMAG AND LOWMAG]
Additional zero masking can occur in the first and last words of an accumulation interval. This is true because the start and stop times of an accumulation interval do not normally fall at the boundaries of data words. Therefore, the bits in the first word that precede the accumulation interval may need to get zero masked as might the bits in the last word that come after the end of the accumulation interval.

Referring primarily to FIGS. 3B and 4B, the one bits counting operations of method step 111 (FIG. 4B) form the count of the number of one bits in each of the eight value words. If there are no such counting operations in the instruction set of microprocessor 16 (FIG. 1), the counting can be accomplished using a table look-up. In the case of a table look-up, prompt integrand value words 27 and early-minus-late integrand value words 37 (FIG. 3B) can be used as addresses in one bits summation table 38 (FIG. 3B), and one bits summation table 38 (FIG. 3B) can output the number of one values (or zeros) in the address. For example, if the table look-up operation is called BITSUM, the following computations can be performed to compute one-bits counts:

\[
\text{ONESCOUNT} = \text{BITSUM}(\text{VALUEWORD})
\]

where the output of the table ONECOUNT is the number of one bits in the word VALUEWORD. This operation is repeated for each of the prompt integrand value words 27 (FIG. 3B) and early-minus-late integrand value words 37 (FIG. 3B) in order to accomplish method step 111 (FIG. 4B). Selection of table width, for example 16-bit or 32-bit, depends on the amount of memory available and other design decisions. If the table width is smaller than the number of bits in a value word, then multiple calls of the table are used in order to sum up the total number of one values in a given value word. Each call takes as input only a portion of the bits in the value word.

Continuing to refer primarily to FIGS. 3B and 4B, the accumulation operations of method steps 113 (FIG. 4B) and 115 (FIG. 4B) sum the one bit counts for each prompt integrand value word 27 (FIG. 3B) and for each early-minus-late integrand value word 37 (FIG. 3B) over the entire accumulation interval, multiply each result by the value 41A (FIG. 3B) that is associated with the value word, and sum all of these scaled value accumulations to form the accumulations of equations (6) and (7), summed prompt accumulation 45 (FIG. 3B) and summed early-minus-late accumulation 47 (FIG. 3B). For example, the following computations can be performed to compute the in-phase summed prompt accumulation 45 in equation (6) as follows:

\[
l_{k,l}(0) = -\sum_{i=1}^{N_k} \text{ONESCOUNT}(-i)_{k,l} - \sum_{i=1}^{N_k} \text{ONESCOUNT}(+1)_{k,l} + \sum_{i=1}^{N_k} \text{ONESCOUNT}(+2)_{k,l} - \sum_{i=1}^{N_k} \text{ONESCOUNT}(+3)_{k,l} + \sum_{i=1}^{N_k} \text{ONESCOUNT}(+4)_{k,l} - \sum_{i=1}^{N_k} \text{ONESCOUNT}(+5)_{k,l} + \sum_{i=1}^{N_k} \text{ONESCOUNT}(+6)_{k,l}
\]

where 1 is the index of successive bit-wise parallel data words in the accumulation interval, \(N_k\) is the total number of data words in the interval, and ONECOUNT\((k)_{i}\) is the ones count for the corresponding value word 41 (FIG. 3B) associated with value \(k\) 41A (FIG. 3B) for the \(i\)th data word interval and the in-phase summed prompt accumulation 45 (FIG. 3B). The quadrature summed prompt accumulations 45 (FIG. 3B) and the in-phase and quadrature summed early-minus-late accumulations 47 (FIG. 3B) are calculated in a similar manner. The only difference is in the actual ONECOUNT values used and, for the case of early-minus-late signals, the set of \(k\) values 41A (FIG. 3B).

Continuing to refer primarily to FIGS. 4A and 4B, the method of the present invention can be adapted to work with a different number of bits in the representation of the RF front-end output and of the baseband mixed signals. An increase above two bits can make the logic more complex and may decrease the time savings over straight integer arithmetic. A decrease to a 1-bit representation can have the opposite effect. For example, if the RF front-end uses 1-bit digitization rather than 2-bit digitization while carrier replica signal 25 (FIG. 2B) retains its 2-bit digitization, then the operation count can decrease by a factor of almost two for the 1-bit method, which can make the logic execute about 4.2 times faster than straight integer arithmetic.

Returning to the discussion of determining PRN code, and now referring again FIGS. 2C, 2D, and 3A, the real-time generation of bit-wise parallel over-sampled prompt PRN code sign 29A (FIGS. 2D and 3A), early-minus-late PRN code sign 35A (FIGS. 2D and 3A), and early-minus-late PRN code zero mask 35B (FIGS. 2D and 3A) can be carried out by real-time over-sampled PRN code generator 30A (FIG. 3A). The inputs to this calculation are the actual PRN code chip length 65 (FIG. 2D), \(\Delta_t\), the sample interval 63 (FIG. 2D), \(\Delta_t\), the nominal early-to-late code delay 61 (FIG. 2D), \(\Delta_{emr}\), the end time of the first code chip relative to the first sample time, or put another way, the time lag \(\Delta_{t_1}\) 67 (FIG. 2D) from the first RF sample time to the end time of the first prompt PRN code chip, and prompt code chips 91 (FIGS. 2D and 6). The outputs are the three integers that store the prompt PRN code sign 29A (FIGS. 2D and 3A), early-minus-late PRN code zero mask 35B (FIGS. 2D and 3A), and early-minus-late PRN code sign 35A (FIGS. 2D and 3A), which are all in bit-wise parallel format.

Referring again to FIGS. 2C and 2D, table look-ups can be used to translate a PRN code and its timing information to bit-wise parallel representations of its over-sampled prompt and early-minus-late versions. The required table
look-ups can be simplified by recognizing that the following parameters are substantially constant, for the purposes of this calculation: sampling interval \(63\) (FIG. 2D), \(\Delta t_c\), the nominal chip length, \(\Delta t_{\text{prompt}}\), the early-minus-late code delay \(61\) (FIG. 2D), \(\Delta t_{\text{nom}}\) used by software correlator \(19\) (FIG. 1), and the maximum number of chips that span a data word of microprocessor \(16\) (FIG. 1). The difference between the actual chipping rate \(\Delta t\) (reciprocal of \(\Delta t_c\)) and the nominal chipping rate \(\Delta t_{\text{nom}}\) (reciprocal of \(\Delta t_{\text{nom}}\)) that is used for the above simplification can be accommodated by correcting the look-up table for each signal component yields a single integer result for prompt PRN code sign \(29\) (FIGS. 2D and 3A), another single integer result for early-minus-late code zero mask \(35\) (FIGS. 2D and 3A), and yet another single integer result for early-minus-late PRN code sign \(35\) (FIGS. 2D and 3A).

Time lag \(67\) (FIG. 2D), \(\Delta t_c\), can take on an infinite number of values in the continuous range:

\[
-\frac{1}{2} \Delta t_{\text{nom}} < \Delta t_c < \frac{1}{2} \Delta t_{\text{nom}}
\]  

(31)

This range’s lower limit guarantees that the end time of the first late chip occurs no earlier than the first sample time. A lower time lag \(67\) (FIG. 2D) \(\Delta t_c\) value would make the first chip irrelevant to the prompt PRN code \(29\) (FIG. 2D), early code \(69\) (FIG. 2D), and late code \(69\) (FIG. 2D) at all of the sample times. The upper limit in equation (31) guarantees that the start time of the first late chip occurs no later than the first sample. A larger value of \(\Delta t_c\) would leave the late code \(69\) (FIG. 2D) at the first sample time undefined based on the available code chips.

Referring now to FIG. 5, to create an electronically processable table, the continuous range of \(\Delta t_c\) values can be replaced with a discrete grid having \(m\) equally spaced points per sample interval \(63\) (FIG. 2D), \(\Delta t_c\). The integer \(m\) is chosen to be large enough so that the granularity \(\Delta t_c/m\) gives sufficient PRN code timing resolution. In GPS applications \(m\) is usually chosen to be large enough so that the counter bit and the corresponding bit sequence, are either zero or one, with zero representing a -1 PRN code value and one representing a +1 PRN code value, and they are listed in order of increasing time. The corresponding array index of the \(x(i)\) table \(81\) is:

\[
[[k, \text{C}(1), \text{C}(2), \ldots, \text{C}(L)] = 1 + (k - k_{\min}) \times 2^L + \sum_{j=1}^{L} C(j)2^{L-j}
\]

(36)

This equation can be inverted to give the code time offset \(83\) grid index \(k\) and the corresponding bit sequence \(85\) as functions of the \(x(i)\) table \(81\) index \(i\):

\[
k(i) = k_{\min} + \text{floor}[(i - 1)/2^L]
\]

(37a)
where \( \text{mod}(x, y) = y - x \times \text{floor}(y/x) \) is the usual remainder function.

Continuing to refer to FIG. 5, the following computations generate the \( x(i) \) table elements of the three tables. Given \( i \), the corresponding code time offset \( k(i) \) is computed from equation (37a) and is used to generate three sequences of chip indices:

\[
j_e(n, i) = 2 + \text{floor}(n - \frac{k(i)}{m}) \text{ for } n = 1, 2, 3, \ldots, n_s
\]

\[
j_l(n, i) = 2 + \text{floor}(n - \frac{k(i)}{m}) \text{ for } n = 1, 2, 3, \ldots, n_s
\]

\[
j_m(n, i) = 2 + \text{floor}(n - \frac{k(i)}{m}) \text{ for } n = 1, 2, 3, \ldots, n_s
\]

where \( n \) is the index of the sample time within the over-sampled data word. The integer \( j_e(n, i) \) is the index of the PRN code chip that applies at sample \( n \) for the prompt PRN code \( 29 \) (FIG. 2D), and \( j_l(n, i) \) and \( j_m(n, i) \) are defined similarly for the early code \( 69B \) (FIG. 2D) and late code \( 69C \) (FIG. 2D), respectively. The formulas in equations (38a)-(38c) amount to time measurements of each sample given in units of chip lengths past the first chip. These indices, in turn, can be used to determine the chip values that apply at the sample times:

\[
C_e(n, i) = C[j_e(n, i); i] \text{ for } n = 1, 2, 3, \ldots, n_s
\]

\[
C_l(n, i) = C[j_l(n, i); i] \text{ for } n = 1, 2, 3, \ldots, n_s
\]

\[
C_m(n, i) = C[j_m(n, i); i] \text{ for } n = 1, 2, 3, \ldots, n_s
\]

where \( C_e(n, i) \) is the over-sampled prompt PRN code \( 29 \) (FIG. 2D), and \( C_l(n, i) \) and \( C_m(n, i) \) are, respectively, the early code \( 69B \) (FIG. 2D) and late code \( 69C \) (FIG. 2D). Each of these code bit values is either zero or one, as dictated by the outer mod(2) operation in equation (37b). These over-sampled chip values can, in turn, be used to formulate tabulated functions \( x_p(i), x_{emlm}(i), \) and \( x_{emlzm}(i) \) that generate the unsigned integers that constitute the bit-wise parallel code representations of the three tables:

\[
x_p(i) = \sum_{n=1}^{n_s} C_p(n, i) \times 2^{n-1}
\]

\[
x_{emlm}(i) = \sum_{n=1}^{n_s} \text{mod}[C_p(n, i) + C_l(n, i); 2] \times 2^{n-1}
\]

\[
x_{emlzm}(i) = \sum_{n=1}^{n_s} \text{mod}[C_p(n, i) + C_l(n, i); 2] \times 2^{n-1}
\]

where \( x_p(i) \) is the entry of the prompt sign table, \( x_{emlm}(i) \) is the entry of the early-minus-late zero mask table, and \( x_{emlzm}(i) \) is the entry of the early-minus-late 2's sign table. Note that the formula used in equation (40c) is only an example illustrative embodiment of the early-minus-late 2's sign table calculation. It places zeros in all of the \( X \) entries of early-minus-late PRN code sign \( 35A \) (FIG. 2D). There exist alternate formulas that are equally correct but that do not place zeros in the \( X \) entries.

The table layout in FIG. 5 is only an illustrative embodiment of how one can construct a table that can be used to translate PRN code chip values and timing information into data words that store the bit-wise parallel representations of the over-sampled prompt PRN code sign \( 29A \) (FIG. 2D), early-minus-late PRN code zero mask \( 35B \) (FIG. 2D), and early-minus-late PRN code sign \( 35A \) (FIG. 2D). Other table layouts are also possible. Possible illustrative index calculations are described below for indexing into the tables for PRN code retrieval during accumulation calculations. If another table layout is used, then different indexing calculations might be needed. Furthermore, different indexing calculations can be used even for the illustrative table layout shown in FIG. 5.

Referring now primarily to FIG. 6, accumulation calculations, as have been previously outlined herein and elsewhere, work with a fixed sequence of code chips. The prompt version of this sequence has a specified timing relationship to the incoming RF signal data. This relationship can be pre-determined by a code search algorithm if software receiver \( 10 \) (FIG. 1) is in acquisition mode or by its delay-locked loop if it is in tracking mode. Software correlator \( 19 \) (FIG. 1) can calculate an accumulation using prompt code chips \( 91 \) (FIG. 6) through \( C(M) \). The timing of the prompt replicas of prompt code chips \( 91 \) (FIG. 6) defines the accumulation interval. The chip sequence starts at start lag \( 93 \) (FIG. 6) \( \Delta t_{start} \) seconds past the first sample of data word \( W_1 \) (FIG. 6), it chips at the constant chipping rate \( f_c = 1/\Delta t_c \), and it ends at end time \( 97 \) (FIG. 6), which occurs \( \Delta t_{start} + M \Delta t_e \) seconds after the first sample of data word \( W_1 \) (FIG. 6). The end of the \( M \)th prompt code chip can occur during data word \( W_N \) (FIG. 6), which implies that

\[
N = \text{ceil}\left( \frac{\Delta t_{start} + M \Delta t_e}{\Delta t_e} \right)
\]

where the ceil( ) function rounds to the nearest integer towards +\( \infty \). Some of the initial bits of data word \( W_1 \) (FIG. 6) and some of the final bits of data word \( W_N \) (FIG. 6) may not be included in the accumulation. Let \( n_{ref} \) be the number of initial bits of data word \( W_1 \) (FIG. 6) that are excluded, and let \( n_{off} \) be the number of final bits of data word \( W_N \) (FIG. 6) that are excluded. The timing relationship in FIG. 6 implies that those numbers are:

\[
n_{off} = \text{ceil}\left( \frac{\Delta t_{start}}{\Delta t_e} \right)
\]

\[
n_{ref} = n_t - \text{ceil}\left( \frac{\Delta t_{start} + M \Delta t_e}{\Delta t_e} \right)
\]

These sample counts can be used to develop additional zero mask words that software correlator \( 19 \) (FIG. 1) uses to properly process the first and last data words during its bit-wise parallel accumulation calculations, as defined in A 12-Channel Real-Time GPS L1 Software Receiver, B. M.
Applied Parallel Algorithms for Efficient Software Correlation

...with the sample time, but it will not get correlated with that term in the right-hand side of the equation.

The table of equation (43) can be constructed by using the following iterative procedure:

\[ \Delta t_m = \sum_{j=1}^{k_m} (\mu_j + j - L) 2^{L-1} \text{ for } \mu = 1, 2, 3, \ldots, (M + L + 1) \]  

For each of these undefined code chips, they can be used to specify the over-sampled codes only for the first \( n_{ws} \) samples of data word \( W_c \).

The algorithm that iteratively determines \( k_{w1} \) must keep track of the code/sample time offset \( \Delta t_{ws} \) for data word \( W_c \).

\[ k_{w1} = \text{round} \left( \frac{\Delta t_{ws}}{\Delta t_f} \right) \times \frac{m_f}{\Delta t_f} \]
be used to determine $k_1$ from an iteratively determined $k_{int}$. Several constants are required by the iterative procedure that determines $k_{int}$, $k_1$, and $\mu_i$. The first five constants are used to account for the difference between the nominal chip length $\Delta_{c, nom}$ used to generate the $x(i)$ tables, and the actual chip length $65$ (FIG. 2D), $\Delta_t$, used in the accumulation:

$$k_{int, round} = k_{int}$$

$$\lambda = \frac{\Delta_t - \Delta_{c, nom}}{\Delta_t}$$

$$a_{f_t} = \text{ceil} \left( \left( k_{int} - \frac{m_f k_{int}}{m} \right) \right) \times \text{sign}(\lambda)$$

$$b_{f_t} = \left\{ \begin{array}{ll}
1 & \text{if } \Delta_t = \Delta_{c, nom} \\
2^{a_{f_t} \text{floor}(a_{f_t} / \text{sign}(\lambda))} & \text{if } \Delta_t \neq \Delta_{c, nom}
\end{array} \right.$$  

$$a_{f_t} = \text{round}(a_{f_t})$$

where the $\text{sign}(\cdot)$ function returns $+1$ if its input argument is positive, zero if the argument is zero, and $-1$ if the argument is negative. The index $k_{int}$ is approximately half the length of a data word as measured in units of $\Delta_t$ seconds. During an accumulation, the rational factor $a_{f_t} b_{f_t}$ gets multiplied by the time offset between the end time of the first code chip and the midpoint of the data word. The result is a time perturbation that removes the average effect of the difference between the actual and nominal PRN code chipping rates. The time perturbation can be used to compute a corrected $k_{int}$ value:

$$k_{int, c, round} = k_{int} + \left( k_{int} - k_{int, round} \right) a_{f_t} b_{f_t}$$

Equation (48d) picks $b_{f_t}$ to equal a power of two so that the integer division by $b_{f_t}$ in equation (49) can be accomplished using a rightward bit shift operation. The $\text{round}(\cdot)$ operation in equation (49) can be accomplished as part of the division if one first adds $\text{sign}(b_{f_t} a_{f_t}) b_{f_t} / 2$ to the quantity $(k_{int, c} - k_{int}) a_{f_t}$ before performing the rightward bit shift that constitutes division by $b_{f_t}$. This approach can give the correct $k_{int, c}$ because the signs of $(k_{int, c} - k_{int})$ and $b_{f_t}$ are both positive and because the rightward bit shift has the effect of rounding the signed division result towards zero. An alternate implementation of the round function could be used for applications that do not guarantee $k_{int, c} > k_{int}$. Such applications are normally associated with $L \leq 2$ PRN code chips per data word.

Five additional constants can be used to define the $k_1$ and $\mu_1$ iterations:

$$L_{int} = \text{round} \left( \frac{n \Delta_t}{\Delta_t} \right)$$

$$\Delta k_1 = \text{round} \left( \frac{m_f \Delta_t}{\Delta_t} \right)$$

$$\Delta k_{f_1} = \text{round} \left( \frac{m_f \Delta_t}{\Delta_t} \right)$$

The constant $L_{int}$ is the typical number of code chips per data word. It is the nominal increment to $\mu_1$ per data word. The constant $\Delta k_1$ equals the number of fine-scale time intervals per PRN code chip. The constant $\Delta k_{f_1}$ is used to adjust $k_{int}$ up or down if it falls outside of the limits:

$$k_{int} < k_{int, low}$$

$$k_{int} > k_{int, high}$$

The constant $\Delta k_{f_1}$ is the nominal increment to $k_1$ per data word. The limits $k_{int, low}$ and $k_{int, high}$ are approximately the limits $k_{int, low}$ and $k_{int, high}$ from equations (33a) and (33b) re-scaled to the new fine time scale and adjusted for the difference between the nominal code chipping rate of the $x(i)$ tables and the actual chipping rate of the accumulation. The extra $-2$ term on the right-hand side of equation (33a) is compensated for by the increase to $k_{int}$ on the right-hand side of equation (50d) and the decrement to $k_{int}$ on the right-hand side of equation (50e). The original $-2$ term and the increment and decrement have been included because they ensure that $k_1$ values which respect the limits in equation (50d) and (50e) are transformed into $k_1$ values that respect the limits in equations (33a) and (33b).

The iteration begins by initializing $k_1$ and $\mu_1$ for the first data word. The nominal initial values are:

$$k_{int, low} = \text{round} \left( \left( \frac{\Delta_{c, nom}}{\Delta_t} \right) + 1 \right) \left( \frac{\Delta_{c, nom}}{\Delta_t} \right) \left( \frac{\Delta_{c, nom}}{\Delta_t} \right)$$

$$\mu_{int, low} = \text{floor} \left( \frac{\Delta_{c, nom}}{\Delta_t} \right) + 1$$

It is possible that $k_{int, low}$ from equation (51a) can violate its upper limit $k_{int, max}$. Therefore, the following conditional adjustment can be implemented in order to finish the initialization.

$$k_1 = \begin{cases}
  k_{int, low} & \text{if } k_{int, low} \leq k_{int, max} \\
  k_{int, low} - \Delta k_1 & \text{if } k_{int, low} > k_{int, max}
\end{cases}$$

$$\mu_1 = \begin{cases}
  k_{int, low} + \Delta k_{f_1} & \text{if } k_{int, low} \leq k_{int, max} \\
  k_{int, low} + 1 & \text{if } k_{int, low} > k_{int, max}
\end{cases}$$

Given this initialization, the calculation of $(k_{f_2}, \mu_2)$, $(k_{f_3}, \mu_3)$, $(k_{f_4}, \mu_4)$, ..., $(k_{f_N}, \mu_N)$ proceeds according to the following iteration:

$$k_{int, c} = k_{int, c} + \Delta k_{f_1}$$

$$\mu_{int, c} = \mu_{int, c} + \Delta k_{f_1}$$

for $v = 2, 3, 4, \ldots, N$
The table look-up calculations finish with the computation of \( k_v, i_v, \) and the actual table look-ups:

\[
k_v = \text{round} \left( \frac{\text{msk}_v(k_f_v)}{m_f} \right) \quad \text{for } v = 1, 2, 3, \ldots, N \tag{55}\]

The \text{round()} operation in equation (55) can be implemented by adding \( m_f/2 \) to \( \text{msk}_v(k_f_v) \) before the rightward bit shift that constitutes division by \( m_f \). The result of the division will be the correct value of \( k_v \), for any sign of \( k_f_v \), if the computer works with 2’s complement notation for signed integers and if the rightward bit shift fills in the leftmost bit of the sign bit.

Given \( k_v \) from equation (55) and \( \mu_v \) from equation (54b), one can use equation (45) to compute \( i_v \). This value, in turn, can be used to index into the tables to determine the prompt PRN code sign 29 (FIGS. 2D and 3A), \( x_{p,v} \), the early-minus-late PRN code short mask 35B (FIGS. 2D and 3A), \( x_{emlz,v} \), and the early-minus-late PRN code sign 35A (FIGS. 2D and 3A), \( x_{emlm,v} \), that correspond to data word \( W_v \):

\[
x_{p,v} = x_{p,v}(i_v) \quad \text{for } v = 1, 2, 3, \ldots, N \tag{56a}
\]

\[
x_{emlz,v} = x_{emlz,v}(i_v) \quad \text{for } v = 1, 2, 3, \ldots, N \tag{56b}
\]

\[
x_{emlm,v} = x_{emlm,v}(i_v) \quad \text{for } v = 1, 2, 3, \ldots, N \tag{56c}
\]

The conditionals in equations (54a) and (54b) can be reduced to a single conditional per data word by introducing the new accumulation interval. Normally the sign of \( \Delta k_{f,c} \) does not vary from accumulation interval to accumulation interval. The only variable quantity that affects \( \Delta k_{f,c} \) is \( \Delta \Delta k_{f,c} \), which normally does not vary significantly.\( \Delta \Delta k_{f,c} \) is a function of the number of chip cycles included in each accumulation interval. The \text{round()} function is normally zero, in which case equations (57b) and (57c) leave \( k_{f,c} \) equal to \( k_{f,c-1} \) and \( \mu_{c-1} = \mu_{c} \) equal to \( \mu_{c-1} \).

The value of \( \mu_{c-1} \) can be computed at the beginning of the accumulation because the sign bit of the 2’s compliment representation of \( k_{f,c-1} \) is fixed for a given accumulation interval. (Normally the sign of \( \Delta k_{f,c} \) does not vary from accumulation interval to accumulation interval or from channel to channel for a given receiver because the only variable quantity that affects \( \Delta k_{f,c} \) is actual chip length.) If \( \Delta k_{f,c} < 0 \), then the proper formula for determining \( k_{f,c} \) and \( \mu_{c} \) can be chosen by considering the inequality \( k_{f,c-1} < k_{f,c} \). Conversely, if \( \Delta k_{f,c} > 0 \), then the proper formula can be determined by considering the inequality \( k_{f,c-1} > k_{f,c} \).

The decision about which condition to check can be made at the beginning of the accumulation because \( \Delta k_{f,c} \) is calculated prior to execution of the iteration in equations (45a)–(45c). When using a processor that creates instruction pipelines, “if” statements can disrupt the pipeline. In this case equations (54a) and (54b) can be replaced with the following computations:

\[
\eta_c = \begin{cases} 
\text{max}(0, \text{sign}(k_{f,c-1} - k_{f,c})) & \Delta k_{f,c} < 0 \\
0 & \Delta k_{f,c} = 0 \\
\text{min}(0, \text{sign}(k_{f,c-1} - k_{f,c})) & \Delta k_{f,c} > 0 
\end{cases} \quad \text{for } v = 2, 3, 4, \ldots, N \tag{57a}
\]

The \text{min()} and \text{max()} functions return, respectively, the minimum or maximum of their two input arguments. The variable \( \eta_c \) is normally zero, in which case equations (57b) and (57c) leave \( k_{f,c} \) equal to \( k_{f,c-1} \) and \( \mu_{c} \) equal to \( \mu_{c-1} \).

The value of \( \mu_{c} \) is normally equal to the sign bit of the 2’s compliment representation of \( k_{f,c-1} \). Similarly, \( \eta_c \) for the third condition is equal to the sign bit of the 2’s compliment representation of \( k_{f,c-1} \). In either case, \( \eta_c \) (or its negative) can be computed in two operations.

Summarizing the real-time over-sampled PRN code generation process (FIG. 3A) and the filtering process (FIG. 7), to compute prompt PRN code 29 (FIG. 3A) and early-minus-late PRN code 35 (FIG. 3A) for an entire accumulation interval, the method includes the steps of computing equations (44a)–(44c) (method step 201, FIG. 7) to construct the table of \( \Delta(\mu) \) values. The method further includes the step of computing the auxiliary constants (method step 202, FIG. 7) in equations (48a)–(48e) and (50a)–(50e). The method further includes the steps of initializing \( k_{f,c} \) and \( \mu_c \) (method step 205, FIG. 7) by evaluating equations (51a)–(52b). The method further includes the step of computing equations (53a), (53b), (57a)–(57c), (49), (55), and (45) (method step 207, FIG. 7) to compute, for each iteration, \( k_{f,c} \), \( k_{f,c-1} \), \( \mu_c \), \( \mu_{c-1} \), and \( \Delta \mu_{c-1} \). The method further includes the step of computing equations (56a)–(56c) (method step 209, FIG. 7) to compute, for each iteration, \( x_{p,v} \), \( x_{emlz,v} \), and \( x_{emlm,v} \).

As mentioned already, it may prove efficient to interleave the equations (44a–c) iterations and the accompanying shift register iterations between the iterations that compute \( k_{f,c-1} \) through \( x_{emlm,v} \) in this scenario. As a result, \( \mu_c \) can be computed from equation (57c). Afterwards, the shift register iterations that generate code chips \( C(\mu_{c-1}, \Delta \mu_{c-1}) \) though \( C(\mu_{c-2}, -1) \) can be performed, and these chip values can be used to iterate equations (44a–c) from \( \mu_{c-2} \) to \( \mu_{c-1} \) in order to determine \( \Delta(\mu_c) \) from \( \Delta(\mu_{c-2}) \).
The software correlator 19 (FIG. 1) of the present invention can advantageously be easily modified to work with signals at different frequencies, new PRN codes, or even different signals for different types of devices. Thus, the same hardware could use the software correlator 19 (FIG. 1) to implement such devices as a GPS receiver, a cell phone, or both. To allow for new codes, new frequencies, and new types of functionality, small changes can be made in the software correlator 19 (FIG. 1), or different versions of the software correlator 19 (FIG. 1) can be run on the same processor. The changes involve using a different baseband mixing frequency and a different PRN code in the correlation, and perhaps changes that would provide the new signals of interest to the software correlator 19 (FIG. 1). In order for the present invention to work with signals at different frequencies, new PRN codes, or signals for different devices, two fundamental changes need to be made. First, the baseband mixing frequency must be tailored to that of the signal data 21, which also involves pre-computing and storing sine and cosine tables at this new frequency. Second, new pre-computed over-sampled PRN code tables 28 (FIG. 3A) must be constructed. The size of the new tables should match the oversampled accumulation period, or at least one over-sampled period of the PRN code. As an alternative to generating new pre-computed over-sampled PRN code tables 28 (FIG. 3A), the new PRN codes can be generated in real-time by over-sampled PRN code generator 30A (FIG. 3A).

Also, the system and method of the present invention could be implemented within systems such as GLONASS receivers, cell phones and cell base stations, pagers, wireless Ethernet (e.g. 802.11x standards), Bluetooth®, BlackBerry® wireless internet devices, and satellite radio/phones (e.g. INMARSAT®). In fact, the system and method of the present invention are applicable to any sort of telecommunications system/device that uses spread spectrum, code division multiple access (CDMA) pseudo random number codes for the transmission of information, either wired or wireless.

Referring now to FIG. 8, navigation calculations require measured values of the PRN code phase 55, carrier phase, and carrier frequency. The measurements for all tracked satellites must be taken at exactly the same time. A time interval counter (TIC) function provides a periodic timing scheme to synchronize these measurements at time t_TIC. At time t_TIC, the TIC function latches all of the PRN code 45, carrier phases, and carrier frequencies along with the code epoch counters, and software correlator 19 (FIG. 1) makes these available to application-specific code 15 (FIG. 1), for example, GPS receiver software. GPS receiver software uses the code phase and epoch counters to compute the pseudo range to each satellite. Software correlator 19 (FIG. 1) keeps track of the code and carrier phase of each signal as determined by the code chip generation rate and the carrier Doppler shift inputs. The quantity \( f_{\text{chip}} \), the estimated code chip generation rate of software receiver 10 for satellite j during its kth PRN code period, can be determined either by an acquisition search procedure, or if tracking, by a delay-locked loop. Likewise, \( \omega_{\text{Doppler}} \), the associated carrier Doppler shift, can be defined by an acquisition procedure or, if tracking has commenced, by a phase-locked loop or a frequency-locked loop: These determinations are made by application-specific code 15 (FIG. 1). Software correlator 19 (FIG. 1) can use these two frequencies to update quantities that keep track of its code and carrier phases according to the formulas:

\[ T_{k+1} = T_k + \frac{1023}{f_{\text{chip}}} \]  

\[ \phi_{k+1} = \phi_k + \omega_{\text{Doppler}}(T_{k+1} - T_k) \]

Software correlator 19 (FIG. 1) can keep a running track of these quantities and can initialize these iterations as part of the signal acquisition calculations that it carries out in conjunction with application-specific code 15 (FIG. 1). The quantities \( T_{jk} \) and \( \phi_{jk} \) are either sent to software correlator 19 by application-specific code 15, or they are initialized arbitrarily by software correlator 19 and application-specific code 15 executes feedback control of \( f_{\text{chip}} \) and \( \omega_{\text{Doppler}} \) to force the sequences defined by equations (58) and (59) to converge to appropriate values. Information about the previously-described conventional method can be found in Dierendorf.

The TIC time \( t_{\text{TIC}} \) (FIG. 8) can occur at, for example, the millisecond boundaries of the receiver clock. At each time \( t_{\text{TIC}} \), the PRN code phase 55 (FIG. 8) of each signal is computed in the following manner:

\[ \psi_{\text{TIC}} = 1023 \left( \frac{T_{\text{TIC}} - T_{\text{jk-1}}}{f_{\text{chip}} + T_{\text{jk-1}} - T_{\text{jk}}} \right) \]

where \( \psi_{\text{TIC}} \) is the PRN code phase 55 (FIG. 8) in chips of signal j at TIC time \( t_{\text{TIC}} \). The epoch counters, which are simply a running total of the number of code periods 57 (FIG. 8), are incremented at each code start/stop time.

The carrier phase calculation at time \( t_{\text{TIC}} \) (FIG. 8) is similar to the PRN code phase 55 (FIG. 8) calculation:

\[ \phi_{\text{TIC}} = \phi_{\text{jk-1}} + \omega_{\text{Doppler}}(t_{\text{TIC}} - t_{\text{jk-1}}) \]

where \( \phi_{\text{TIC}} \) is the carrier phase at time \( t_{\text{TIC}} \). The Doppler shift that gets returned at time \( t_{\text{TIC}} \) (FIG. 8) is \( \omega_{\text{Doppler}} \).

With respect to the performance of the system and method of the present invention, a sample screen-shot from the illustrative embodiment of the present invention is provided in Table 8. This table illustratively shows the tracking of nine channels. The roof-mounted L1 antenna of the illustrative embodiment can have a pre-amp with 26 dB of gain. The software correlator 19 (FIG. 1) of the present invention can provide positional accuracy on the order of 10-15 meters when working in conjunction with application-specific software 15 (FIG. 1).

Table 8

<table>
<thead>
<tr>
<th>Lat</th>
<th>Lon</th>
<th>Spd</th>
<th>SVs</th>
<th>8th</th>
<th>Orzak</th>
<th>FLL</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>42.44354</td>
<td>-76.48143</td>
<td>0.5</td>
<td>327</td>
<td>3D</td>
<td>GDOP</td>
<td>1.9</td>
<td>17/10/02</td>
</tr>
<tr>
<td>269.6560</td>
<td>ROC</td>
<td>-0.7</td>
<td>HI</td>
<td>DO</td>
<td>OscErr</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>ELEV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TABLE 8-continued

<table>
<thead>
<tr>
<th>CH</th>
<th>SV</th>
<th>ELV</th>
<th>AZI</th>
<th>DOFF</th>
<th>NCO</th>
<th>UEER</th>
<th>SF</th>
<th>PERR</th>
<th>PERRR</th>
<th>LOCK</th>
<th>SNR</th>
<th>IS4</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>67</td>
<td>237</td>
<td>-528</td>
<td>-927</td>
<td>4</td>
<td>1</td>
<td>9.0</td>
<td>0.7</td>
<td>16.9</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>22</td>
<td>64</td>
<td>47</td>
<td>1644</td>
<td>-2045</td>
<td>4</td>
<td>1</td>
<td>14.3</td>
<td>0.6</td>
<td>18.0</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>50</td>
<td>152</td>
<td>2174</td>
<td>1778</td>
<td>2</td>
<td>1</td>
<td>5.5</td>
<td>-0.4</td>
<td>18.4</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>25</td>
<td>22</td>
<td>106</td>
<td>-2650</td>
<td>3050</td>
<td>2</td>
<td>1</td>
<td>42.9</td>
<td>0.2</td>
<td>13.2</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>17</td>
<td>1</td>
<td>62</td>
<td>1722</td>
<td>1331</td>
<td>2</td>
<td>1</td>
<td>7.5</td>
<td>-0.4</td>
<td>8.1</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>15</td>
<td>2</td>
<td>81</td>
<td>2278</td>
<td>1887</td>
<td>2</td>
<td>1</td>
<td>-5.2</td>
<td>-0.7</td>
<td>7.4</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>27</td>
<td>12</td>
<td>295</td>
<td>2969</td>
<td>2575</td>
<td>0</td>
<td>1</td>
<td>0.0</td>
<td>0.0</td>
<td>8.0</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>13</td>
<td>4</td>
<td>303</td>
<td>3665</td>
<td>1966</td>
<td>2</td>
<td>0</td>
<td>0.0</td>
<td>0.0</td>
<td>14.9</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>31</td>
<td>22</td>
<td>185</td>
<td>3860</td>
<td>3464</td>
<td>2</td>
<td>1</td>
<td>-11.0</td>
<td>-0.5</td>
<td>15.9</td>
<td>-1.000</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>20</td>
<td>4</td>
<td>219</td>
<td>-3806</td>
<td>-3483</td>
<td>2</td>
<td>1</td>
<td>27.5</td>
<td>0.3</td>
<td>9.8</td>
<td>-1.000</td>
<td></td>
</tr>
</tbody>
</table>

Two comparison tests illustrate the performance of the system and method of the present invention. In the first test, a first configuration includes a MITEL® GP2021 hardware correlator, but is in all other ways identical to a second configuration that includes the software correlator 19 (FIG. 1) of the present invention. The two configurations differ in SNR by less than 1 dB and in navigation solutions by no more than 5–10 meters. In the second test, timing studies using the system of the present invention show that processing six channels uses only about 20% of the processor’s capacity, while Akos 2001a report a real-time software GPS receiver that would require 100% of the capacity of a 1.73 GHz microprocessor to implement a 6-channel GPS receiver when processing data from an RF front-end with a sampling frequency of 5.714 MHz.

Referring now to FIGS. 9A and 9B, among other indicators that could assess the accuracy of the PRN code generated by real-time over-sampled PRN code generator 30A (FIG. 3A), which includes prompt PRN code sign 29A (FIG. 3A), early-minus-late PRN code sign 35A (FIG. 3A), and early-minus-late PRN code zero mask 35B (FIG. 3A), is the low distortion of the generated codes versus the true codes. Although the invention has been described with respect to this paradox lies in the averaging effect of the accumulations. The length of a code chip equals 134.992269 code offset time grid intervals for the example shown in FIGS. 9A and 9B. The non-integer nature of this number causes the accumulation its way through successive data words. This dithering tends to average out the table granularity errors, and this averaging can reduce the net timing error by an order of magnitude or more, as shown in FIG. 9B. Although the invention has been described with respect to various embodiments, it should be realized this invention is also capable of a wide variety of further and other embodiments.

What is claimed is:

1. A software receiver comprising:
   a receiver capable of receiving a radio signal;
   means for digitizing the radio signal; and
   means for using bit-wise parallelism to provide a software correlator capable of mixing the digitized radio signal to form a baseband signal.

2. The software receiver of claim 1 wherein said software correlator comprises:
   means for computing correlations between the baseband signal and at least one pseudo-random number (PRN) code using the bit-wise parallelism.

3. The software receiver of claim 2 wherein said software correlator further comprises:
   means for computing accumulations from the correlations using the bit-wise parallelism.

4. The software receiver of claim 3 further comprising:
   application-specific code capable of computing navigation data using the accumulations.

5. The software receiver of claim 1 wherein said means for digitizing comprises:
   means for down-converting the radio signal to an intermediate frequency; and
a digitizer capable of digitizing the intermediate frequency.

6. The software receiver of claim 5 wherein said digitizer produces at least one bit/sample.

7. The software receiver of claim 5 wherein said digitizer is an analog to digital converter.

8. The software receiver of claim 1 wherein said bit-wise parallelism accommodates multi-bit signals.

9. A method for processing at least one radio frequency (RF) signal over an accumulation period comprising the steps of:

receiving at least one RF signal;

mixing the at least one RF signal to form a baseband mixed signal using bit-wise parallelism;

computing a fully mixed prompt integrand as a function of the baseband mixed signal and a pre-selected pseudo-random number (PRN) code using the bit-wise parallelism;

computing a fully mixed early-minus-late integrand as a function of the baseband mixed signal and the pre-selected PRN code using the bit-wise parallelism;

computing in-phase summed accumulations and quadrature summed accumulations over the accumulation period, the in-phase summed accumulations and quadrature summed accumulations being functions of the fully mixed prompt integrand and the fully mixed early-minus-late integrand; and

rotating the in-phase summed accumulations and quadrature summed accumulations to correct for effects of frequency and phase granularity of the baseband mixed signal.

10. A communications network comprising at least one node for carrying out the method according to claim 9.

11. A computer data signal embodied in electromagnetic signals traveling over a computer network carrying information capable of causing a computer system in the network to practice the method of claim 9.

12. A computer readable medium having instructions embodied therein for the practice of the method of claim 9.

13. The method of claim 9 wherein said step of computing a fully mixed prompt integrand comprises the step of:

generating the pre-selected pseudo-random number (PRN) code using the bit-wise parallelism, said step of generating the pre-selected PRN code comprising the steps of:

formulating a tabulated function for use in translating code chip and timing values into PRN code using the bit-wise parallelism;

computing a fully mixed prompt PRN code in real-time; choosing at least one prompt PRN code from the at least one prompt PRN code, the at least one chip value corresponding to at least one data interval that contains at least one sample of a data word, the at least one chip value having a known timing relative to the at least one data interval;

transforming the known timing into a time grid index; and

translating the at least one chip value and the time grid index during the at least one data interval into the PRN code using the bit-wise parallelism for the at least one data interval, said step of translating resulting from the use of the tabulated function.

14. The method of claim 13 further comprising the step of: computing the time grid index as a function of a time offset index k, and an auxiliary table index μ.

15. The method of claim 13 further comprising the step of: computing the time grid index iteratively as a function of a previously-computed time grid index, the at least one prompt PRN code, and the timing values associated with the at least one prompt PRN code.

16. A software receiver comprising:

a front-end device capable of receiving a radio signal, said front-end device capable of converting the radio signal into signal data;

data acquisition device capable of receiving the signal data, said data acquisition device capable of providing the signal data to a microprocessor;
at least one shift register capable of packing the signal data into at least one data word;

a baseband mixer capable of computing at least one baseband mixed signal as a function of the at least one data word by using bit-wise parallel processing;
a correlator capable of computing correlations between the baseband mixed signal and a pseudo-random number (PRN) code replica signal; and

an accumulator capable of computing summed accumulations by accumulating the correlations.

17. The software receiver of claim 16 wherein the signal data further comprises a signal sign.

18. The software receiver of claim 16 wherein the signal data further comprises a signal sign and at least one signal magnitude.

19. The software receiver of claim 16 wherein said correlator uses the bit-wise parallel processing for computing the correlations.

20. The software receiver of claim 16 wherein said accumulator accumulates the correlations by an electronic mechanism.

21. The software receiver of claim 16 wherein the radio signal can be received from a global positioning source.

22. The software receiver of claim 16 wherein said correlator can be adapted to perform functions selected from a group consisting of accepting the radio signal at any frequency, accepting any PRN code, and accepting the radio signal from any device that generates a radio signal.

23. The method of claim 9 wherein said step of computing in-phase and quadrature summed accumulations comprises the steps of:

representing a carrier replica signal from at least one channel from a plurality of channels as a carrier replica sign and a carrier replica magnitude;

representing the at least one RF signal from the at least one channel of the plurality of channels as at least one signal word;

computing a baseband mixed sign as a function of the carrier replica sign and the at least one signal word;

computing a baseband mixed magnitude as a function of the at least one signal word; selecting a pseudo-random number (PRN) code having a prompt PRN code and an early-minus-late PRN code;

representing the prompt PRN code as a prompt PRN code sign;

computing a fully mixed prompt integrand sign as a function of the baseband mixed sign and the prompt PRN code sign;

computing a fully mixed early-minus-late integrand sign as a function of the baseband mixed sign and the early-minus-late PRN code sign;

representing the early-minus-late PRN code as an early-minus-late PRN code sign and an early-minus-late PRN code zero mask; and

computing a fully mixed early-minus-late integrand sign as a function of the baseband mixed sign and the early-minus-late PRN code sign;
computing at least one set of prompt integrand value words as a function of the fully mixed prompt integrand sign and the baseband mixed magnitude;
computing at least one set of early-minus-late integrand value words as a function of the fully mixed early-minus-late integrand sign, the baseband mixed magnitude, and early-minus-late PRN code zero mask;
computing prompt in-phase and quadrature summed accumulations for the plurality of channels for an accumulation interval as functions of the number of significant bits in the at least one set of prompt integrand value words; and
computing early-minus-late in-phase and quadrature summed accumulations for the plurality of channels as functions of the number of significant bits in the at least one set of early-minus-late integrand value words and as functions of the values associated with the at least one set of early-minus-late integrand value words.

24. The method of claim 23 further comprising the step of: selecting the significant bits from a group consisting of zeros and ones.

25. The method of claim 23 further comprising the step of: retrieving the carrier replica signal from a carrier replica table, the carrier replica table representing a coarse grid of frequencies.

26. The method of claim 23 further comprising the step of: representing the signal word from the at least one channel as a signal sign and a signal magnitude; and computing at least one baseband mixed magnitude as a function of the carrier replica magnitude and the signal magnitude.

27. The method of claim 26 further comprising the step of: retrieving the carrier replica signal from a carrier replica table, the carrier replica table representing a coarse grid of frequencies.