Determined the Best-Fit FPGA for a Space Mission: An Analysis of Cost, SEU Sensitivity, and Reliability

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Outline

- FPGA selection for flight missions
- Differentiating FPGAs
- Cost Analysis
- SEE Analysis
- Expanding Evaluation Criteria
  - Limitations of Bit Error Rate Calculators
  - SET Performance Degradation Metric
  - Availability Calculation
- Applying Evaluation criteria to the selection process

To be presented at Microelectronics Reliability & Qualification Workshop (MRQW), Dec. 4-5, 2007, Manhattan Beach, CA
Flight Project FPGA Selection

- Primary Considerations
  - Criticality
  - Number of Mega-Operations Per Second (MOPS)
    - Internal clock frequency
    - Number of operations performed at each clock edge
  - Area/Power restraints
  - Cost

- Analysis
  - SEE and Reliability testing
  - Integrating traditional SEE metrics with obtainable MOPs

FPGA Characterization: Understanding the Differences to Develop a Comprehensive Analysis
Configuration: A Major Difference between FPGA Classes

- FPGAs contain groups of preexisting logic: HARDWARE

- Configuration:
  - Arrangement of preexisting logic
  - Defines Functionality
  - Defines Connectivity

- Common types
  - One time configurable
  - Re-configurable
Antifuse FPGA Devices (Actel and Aeroflex)

**Pros:**
- Most common FPGA devices utilized for space missions - **Heritage**
- Configuration is fused (no transistors) and is thus "HARDEND" – not affected by SEUs
- Logic has embedded mitigation at each DFF (either TMR or DICE) – eases the design phase

**Cons:**
- One time programmable – can complicate the design/debug phase
- **Very expensive**

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SRAM-Based FPGA’s

**Pros:**
- The ability to reconfigure a function while in-flight is of great advantage to many missions
- Device is Less expensive
- Easier to debug/correct (with no mitigation)
- Performance (MOPS):
  - Speed
  - Increased User Device Resources

**Cons:**
- Configuration is SRAM-based – increased sensitivity to radiation (vs. antifuse)
- Additional design complexity necessary for mitigation
- Additional hardware necessary for (re)configuration
What Xilinx Does Well: Frequency and Number of Mega-Operations per Second:
\[ \text{NMOPS} = f^*k \]

\[ T_{\text{clockperiod}} = \frac{1}{f} \]

K: Resource and speed Dependent

Xilinx Virtex Series can supply a high frequency (f) with a large K value. NMOPS is very large compared to many other FPGA manufacturers

Xilinx FPGAs in Space: Configuration and Scrubbing

Minimal Requirements for Flight:
- Full Reconfigure
- To increase availability: use Scrubber
- Configuration Manager can be combined with external scrubber

Extra circuitry is required regardless in order to configure/reconfigure
Criticality and Xilinx: Proposed Solution: Full TMR

- Triple the design within the Xilinx FPGA device (including I/O)
- User implemented (can lengthen design cycle)
- Will consume $\gg 3x$ of original area
- Difficult to implement multiple clock domains
- Use an external FPGA device to scrub the configuration memory

Cost Analysis

- Missions do not generally require a large number of replicated FPGA devices
- Cost of a mission will not rely on FPGA device cost
- Design cycle can grossly affect cost:
  - Complexity of design architecture:
    - One FPGA can not handle required number of operations per second.
    - Chosen FPGA can not handle availability specifications – additional/complex mitigation is required.
  - Complexity of verification
  - Complexity of Board
  - Poor choice in emulation or engineering models
- Choose the FPGA that best meets requirements!
Determining Reliability and Availability: Radiation Testing and SEE Analysis

Investigating Radiation Effects (SEE Analysis)

- Determine Bit sensitivity
  - Flip Flops
  - Configuration (SRAM based technology)
- Availability analysis
  - Given a function to implement – what is the percentage of time the output is correct vs. incorrect
  - Determine an availability rating that considers
    - Operational Frequency
    - Fluence
    - Repair time
    - Burst time
What Function to Implement for Testing?

Simple Architecture
- No functional Masking
- Easy to baseline across FPGAs
- Reduces Test time
- Increases state space coverage

Complex Architecture
- Functional Masking
- Minimal state space coverage (short test runs, reset upon error)
- Only significant for specific design

Actual flight Architecture
- Usually not available at test time
- Can be very expensive to test
- Can not cover a significant amount of state space while testing
- Usually have to start from scratch at every error event

Simple Architecture: Windowed Shift Register

N levels of combinatorial logic between DFFs
N = 0, 4, 8, and 20

Possible Transients
Calculating Error Cross Sections

Traditional error calculation:

\[ \sum \frac{\text{Events}}{\text{Fluence}} \]

Error calculation: Bursts within data

\[ \sum \frac{\text{Events}}{\text{TF} - (\text{TB} \times \text{FLUX})} \]

- Analysis of event frequency
- Cross-section fed to error rate calculator: based off of a cumulative distribution probability function (P(T>t))
- We are not analyzing how long we are in error

Clock Frequency Effects

54 MeV cm²/mg:

Aeroflex:
- \( \sigma \) decreases as Frequency increases
- Most significant with larger chains of combinatorial logic and data pattern fluctuation

Actel:
- \( \sigma \) decreases as Frequency decreases

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Error Cross-Section Results Prove for Antifuse Devices...

- Static testing is not sufficient
- Static simulation is not sufficient
- Assumptions of frequency response can not automatically be made
- Actel produced expected (traditional) response
- Aeroflex – unexpected... combinatorial logic acts as transient filter

REAG Testing of Xilinx SRAM-Based FPGAs.
**Scrubbing Facts:**

- Most SRAM based FPGA faults are believed to occur in configuration memory.
- Correction of fault can only be accomplished by:
  - Reconfiguration – can be costly (time wise)
  - Scrubbing
- Reconfiguration brings down the system
- While scrubbing, the system is fully operational.
- Scrubbing does not reduce the probability of an upset occurring
- Frequency of scrubbing can reduce the amount of time the upset is present in the configuration memory
- Unable to scrub everything

**Warning:** High Current spikes observed by Xilinx consortium:

- Observed @ fluence $=1 e08$ ($1 e05 < $flux $< 1 e06$): FLUX is extremely accelerated for scrubbing mitigation technique
- Readback+CRC is performed at every frame – different than blind-scrubber of REAG
- REAG did not observe event... tests performed with flux $< 1 e03$

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**Non-TMR Windowed Architecture**

N levels of logic between DFFs... 2 strings each: $N = 0, 8,$ and $20$

**Upon Error:**

- Long string of '0's or '1's:
- REAG uses alternating data inputs to achieve accurate cross-sections
Error Cross Section Calculation:
Dealing with Bursts

\[ \sigma \equiv \frac{NE}{TFL - (TB \times FLUX)} \]

- Cross-section based off of functional upsets (shift register)
- Simultaneous Multiple errors exist in shift register
- Count burst as one error event
- Burst can potentially mask faults
  - could have a much higher frequency of events
  - just masked by burst
  - Will be further investigated by fault injection

Can not make direct comparison with Antifuse device bit error rate

\[ \sigma \text{, cm}^2/\text{Device} \]

Evaluation Criteria and Device Selection
Limitations with Error Cross Sections as sole Evaluation Criteria

Frequency Effect Analysis and Successful Operations per second:
DUTA @ 100MHz over 1E07 fluence: no bursts 10 errors
DUTB @ 50MHz over 1E07 fluence: no bursts 5 errors

\[ \sigma_A = 2 \times \sigma_B \]; Assumes constant error rate per frequency

Common Interpretation: Cross Section increases with Frequency – Decrease Clock Rate for Critical Missions

- However, B has to run twice as long as A to complete the same number of successful operations.
- Illustrates that per number of completed operations, each has the same probability to accumulate an equivalent number of errors

In this case: Slower Clock does not influence errors per successful operation

Limitations with Error Cross Sections as sole Evaluation Criteria (Continued)

- Burst Analysis:
  - Cross section probability calculation is based off of Event frequency (not event duration).
  - Cross section does not consider burst or repair time (availability)
Bit Error Rate Misconceptions:

- Given a Bit Error rate of 5e-08, what does this mean???

AntiFuse
- Bit Error Rate is based on DFFs
- Number of DFFs will be from a few hundred to 10's of thousands
- Comes out to about 1 error every 10,000 days or better

SRAM
- Generally pertains to configuration bit rate
- If for example 1e7 bits can affect the design upon upset – then can have 1 upset every 2 days

SET Performance Metric:

- Given a failure rate (worse-case is bit-error rate): MTTF
- Determines required operational frequency and necessary parallelism

\[ f \times k = \frac{N O P_{\text{target}}}{M T T F} \]

\[ \frac{1}{1.0} = \frac{1.0}{1.0 - \left( \sum_{i=1}^{n} E C_i \right) \times A c c} \]

- NOP\text{\_target}: Targeted Number of operations
- \( F \times k \): operational frequency \times implemented number of operations (each cycle)
- \( E C_i \): Number of clock cycles of error per event i
- \( C y c_{\text{rad}} \): Total number of operational clock cycles during irradiation
- Acc: Acceleration Factor
Availability Calculation using Radiation Data

\[ A = \frac{MTTF}{MTTR + MTTF} \]

A = 1 is a perfect system

A: Steady State Availability

<table>
<thead>
<tr>
<th>LET = 8MeV·cm²/mg</th>
<th>MTTR</th>
<th>MTTF</th>
<th>A steady State</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTAX @ 150MHz</td>
<td>6.67 \times 10^{-2}</td>
<td>3.6 \times 10^{-6} AccR</td>
<td>(3.6 \times 10^{-6} AccR)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(6.67 \times 10^{-2} - 3.6 \times 10^{-6} AccR)</td>
</tr>
<tr>
<td>Aeroflex @ 100MHz</td>
<td>10^{-3}</td>
<td>6.0 \times 10^{-6} AccA</td>
<td>(6.0 \times 10^{-6} AccA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(10^{-3} - 6.0 \times 10^{-6} AccA)</td>
</tr>
<tr>
<td>Xilinx @ 100MHz</td>
<td>1.6 \times 10^{-2}</td>
<td>41 AccX</td>
<td>(41 AccX)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(1.6 \times 10^{-2} \times 41 AccX)</td>
</tr>
</tbody>
</table>

Mission Device Selection

- Xilinx showed a relatively low availability rating at 100MHz.
  - If used at full rate, will achieve much higher operations per second.
  - Higher MOPS can include scheduled downtime and may be a great fit
- Criticality and reliability play a major role in device selection
  - Missions have traditionally chosen antifuse devices for critical specifications.
    - Actel has been in the forefront
    - Aeroflex is very promising with its combinatorial transient filtering.
  - For less critical functionality, SRAM devices are being heavily investigated
### Embedded vs. User Implemented TMR

<table>
<thead>
<tr>
<th></th>
<th>Clock Speeds</th>
<th>Contains Mitigation</th>
<th># FLIP FLOPS</th>
<th># User TMR FLIP FLOPS</th>
</tr>
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<tbody>
<tr>
<td>ACT2</td>
<td>&lt;10 MHz</td>
<td>NO</td>
<td>&lt;400 to 1000</td>
<td>&lt;400 to 1000</td>
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<tr>
<td>RTXSX</td>
<td>&lt;50 MHz</td>
<td>Yes</td>
<td>&lt;2000 to 4000</td>
<td>&lt;2000 to 4000</td>
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<tr>
<td>RTAX5</td>
<td>&lt;200 MHz</td>
<td>Yes</td>
<td>21,000</td>
<td>21,000</td>
</tr>
<tr>
<td>XILINX V4 – LX25</td>
<td>&lt;400 MHz</td>
<td>NO</td>
<td>22,000</td>
<td>5,000</td>
</tr>
<tr>
<td>XILINX V4 – FX60</td>
<td>&lt;400 MHz</td>
<td>NO</td>
<td>52,000</td>
<td>10,000</td>
</tr>
</tbody>
</table>

*Not datasheet clock speeds ... actual design clock speeds*

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### Understand Requirements – Select Wisely

- **If criticality (reliability and availability) is essential:**
  - Antifuse FPGAs provide safer solutions
  - Antifuse FPGAs can shorten the design cycle – More Cost Effective
    - Verification is eased (mitigation is embedded and does not have to be verified)
    - Board design is simplified – do not have to triple I/O (signal integrity requirements)
    - Multiple clock domains are easier to implement

- **If MOPS is essential**
  - SRAM based design can ease the design cycle (without additional TMR)
  - Available IP cores
  - Re-programmability
  - Number of high speed available resources
  - SRAM based FPGA currently provide the fastest internal clocking (internal DLL + multiple embedded Power PCs)
Summary

- Each FPGA type has its advantages; SEE analysis must take this into account for a comprehensive comparison.
- Sensitivity calculations are provided to missions to assist in the selection process.
  - Test to determine additional mitigation schemes required per FPGA.
  - Bit Error calculations.
  - Availability and degradation analysis.
- Formulae have been presented:
  - Adjust Bit error calculations due to long bursts.
  - SET Performance degradation Metric.
  - Availability.
- Mission Cost and design cycle are directly related.
  - Keep designs simple.
  - Each FPGA has its advantages.
  - Choose the best fit FPGA for your mission specifications.

Thank You ....
Questions?