



Radiation Testing, Characterization and Qualification Challenges for Modern Microelectronics and Photonics Devices and Technologies

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Lewis M. Cohn, Defense Threat Reduction Agency

To be presented by Kenneth A. LaBel at the Government Microcircuit Applications & Critical Technology Conference (GOMAC), March 17-20, 2008, Las Vegas, NV.



Outline of Presentation

- Introduction
- Single Event Effect (SEE) Testing and Complex Device Packages
 - Packaging material
 - Thermal control
 - Particle interarrival angle
 - The direction the particle enters the device
- SEE Sensitive Devices
 - Optical devices and the increased sensitivity of CMOS
 - Changing the way we test and predict space performance
- The Impact of System-on-a-Chip (SOC) Device Complexity
 - Example: Field Programmable Gate Array (FPGA) complexity
 - Fault Isolation
 - Data Interpretation
 - Statistical Data Gathering
 - Total Ionizing dose (TID) test logistics
- Considerations

Disclaimer:

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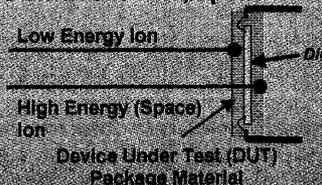


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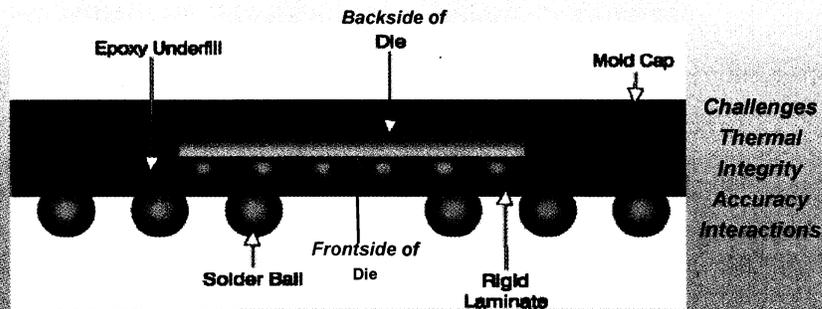


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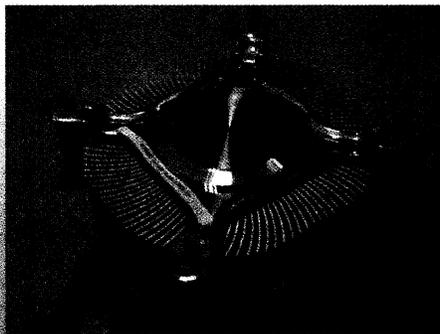
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external fans, TECs, spray cooling
Real limitation for test facilities in a vacuum!

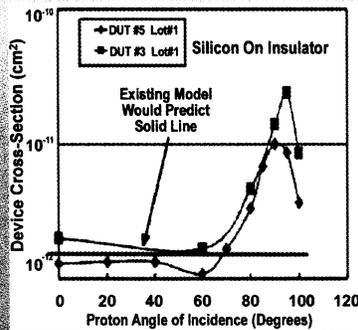
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9



Simulating the Space Environment

- As pointed out, heavy ion test facilities use a unidirectional beam to simulate the space environment
 - Part is usually tilted to simulate angular space effects
- The underlying assumption is often false



Challenges

- Tilting part = Increasing path through device (Ion range limitation)
- Asymmetry of transistors = Test in both tilt axes PLUS rotation
- Backside/frontside = Impossible to perform without major effort
- Modeling = Hard to model w/o detailed technology/circuit knowledge

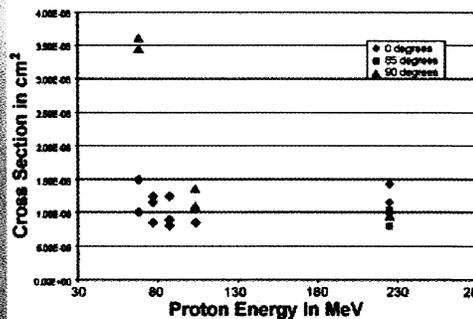
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Are We Approaching a Meltdown?

- With scaling, increased speed, reduced Vdd, electrical margins have eroded decreasing the amount of charge required to cause an SEU
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Energy and angular Proton effects in an optocoupler – an indication of direct ionization



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Lower and higher proton energies may be required

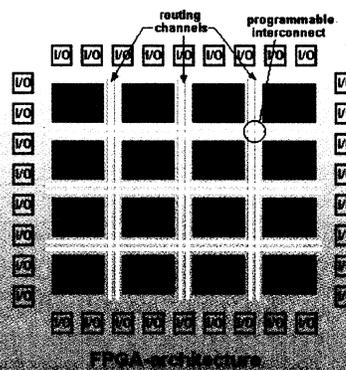
Space prediction tools need updating to accommodate

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SOC: Are We Doomed to the Unknown?

- Using an FPGA as an example, the block diagram looks deceptively simple
 - Silicon with logic modules, I/O, and routing
- So, what's the problem?
 - It's not just logic, it's
 - Logic (user configurable)
 - Processors
 - Gbps I/O
 - Other embedded IP, and
 - It can store the configuration for this SOC internally
 - This can be SRAM-like for reconfigurability



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SOC: Radiation Implications



- How does this highly multi-functional device relate to SEE test and radiation performance?
 - Myriad of potential failure modes can occur
 - Change of configuration memory,
 - State machine errors,
 - Logic errors related to
 - Cell spacing (multi-bit upsets or MBUs) or
 - Operating speed (SEU event may last longer than one clock period),
 - Software interrupts, and more
 - In the following charts, we will consider four implications to testing a SRAM-like FPGA with embedded IP



Question we will answer –
How is SRAM-like configuration memory like an umbrella?

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SOC: SEE Test Issue 1 – Fault Isolation



- Fault isolation (root cause)
 - Understanding what within the device is causing an event.
 - Hitting a specific transistor with an ion and observing effect.
 - The current SEE test facilities are ill-equipped for this purpose
 - Higher energy microbeam facilities where you can focus a particle to a small spot size to identify what is upsetting as well as penetrating through layers of silicon would be advantageous
 - Other tools, such as two photon absorption (TPA) lasers may also be useful
 - Beware: SOCs are usually in packages such as FBGs and the challenges discussed earlier play into this discussion as well.
 - Device complexity does not lead to full silicon testability
 - Errors can be masked (i.e., hit to configuration may mask state machine errors)
 - Hidden registers
 - Complete testing, as discussed in 2007, is impossible



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SOC: SEE Test Issue 2 – Data Interpretation



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 - With the vast array of user configurability, operating modes, speed of operation, and so forth, it is impossible to cover all the bases for each potential application of the device.
- What does this imply? Is all existing SOC test data useless?
 - A data point is just a data point
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 - Testing has to take place using all designs, functions, speeds, etc... of the actual application
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Data Mining –
Now an exercise
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 - What may happen is that SEUs may occur during a test in these “smaller” circuit portions, but are lost when the “bigger” area is upset.
- In addition, if we observe an anomaly on a specific output, where could it come from?
 - I/O error
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- A radiation test should be designed to bound the worst-case
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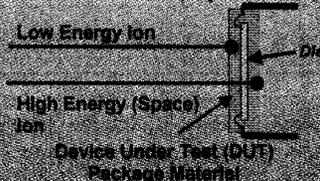


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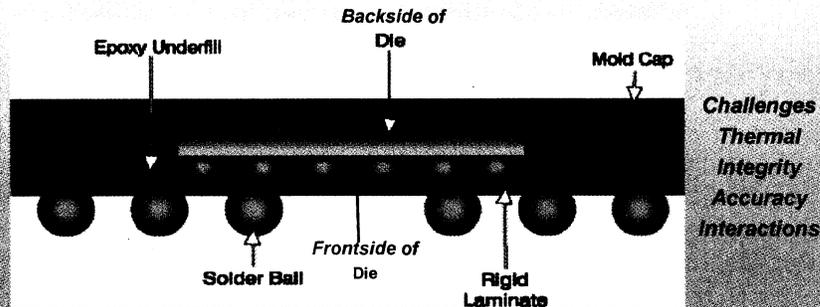


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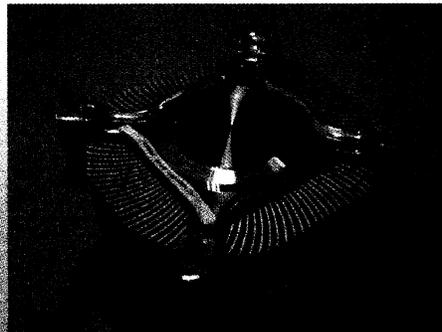
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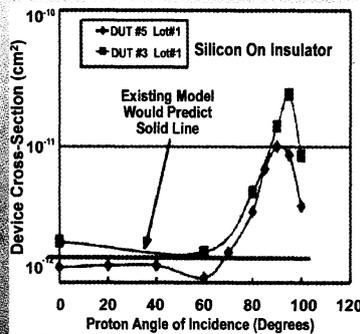
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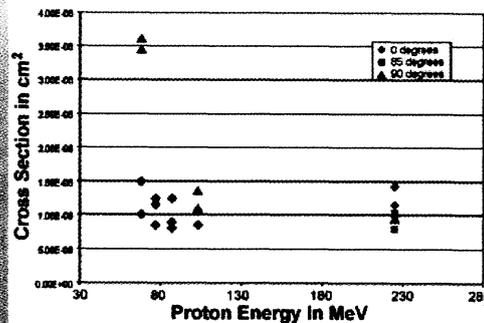
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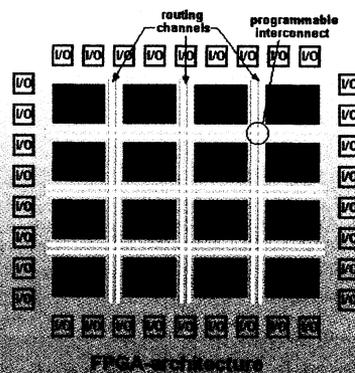
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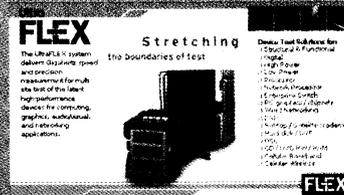
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SOC: TID Test – Parametric Data Gathering

- Given the speed, logic size, IP, etc. in these devices, trying to reproduce the manufacturers detailed test vectors and parametric measurements would require years and years of effort as well as millions of dollars.
- Simplified tests are often undertaken looking primarily at functional go/no-go and limited parameters.
- These data must be viewed in the limited regard in which they were taken.
- Working with the device manufacturer and using their test system should be considered for these complex devices.

Million \$ Testers –
High cost,
Years of code development



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Considerations

- We have discussed just a few of the emerging challenges related to modern radiation effects testing
 - Device packaging and complexity
 - Emerging SEU mechanism concerns
- These are just the tip of the iceberg and should not be viewed as a comprehensive discussion
- The final thought is that radiation data must be very carefully scrutinized to understand what the data does or does not contain
 - In addition, the application-specific orientation of radiation data continues to grow

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